



VT1536A

Isolated Digital Input/Output Signal Conditioning Plug-on

User's and SCPI Programming Manual

Where to Find it - Online and Printed Information:

| | |
|---|--|
| System installation (hardware/software) | VXIbus Configuration Guide* HP VIC (VXI installation software)* |
| Module configuration and wiring | This Manual |
| SCPI programming | This Manual |
| VXIplug&play programming | VXIplug&play Online Help |
| VXIplug&play example programs | VXIplug&play Online Help |
| VXIplug&play function reference | VXIplug&play Online Help |
| Soft Front Panel information | VXIplug&play Online Help |
| VISA language information..... | Agilent/HP VISA User's Guide |
| Agilent/HP VEE programming information..... | Agilent/HP VEE User's Manual |

**Supplied with HP Command Modules , Embedded Controllers, and VXLink.*



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VT1536A Isolated Digital Input/Output SCP

Introduction

The VT1536A is an eight-channel Isolated Digital I/O SCP. Channels are switch configurable as either input or output on a channel-by-channel basis.

Input-configured channels provide:

- Optically coupled isolation
- Individual switch selectable threshold levels of 5, 12, 24 and 48 VDC
- Two programmable debounce timers (150 μ s to 2.4 s); one for the SCP's lower 4 channels and one for the SCP's higher 4 channels.
- Programmable polarity

Output-configured channels provide:

- SPST Solid-state relay output
- 200 mA current carrying capability
- Relays protected by active voltage clamping
- Programmable polarity

About this Manual

This manual shows you how to configure the Signal Conditioning Plug-on (SCP) using SCPI commands and explains the capabilities of this SCP.

The contents of this manual are:

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- Setting Configuration Switches page 4
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Identifying the Plug-on

You'll find the VXI Technology part number on the connector side of the SCP. For the VT1536A, the part number is: VT1536A.

Setting Configuration Switches

Each channel has a four-switch package that configure its input threshold voltage level and I/O direction.

Locating switches Figure 1 shows the location of each channel's configuration switch package.

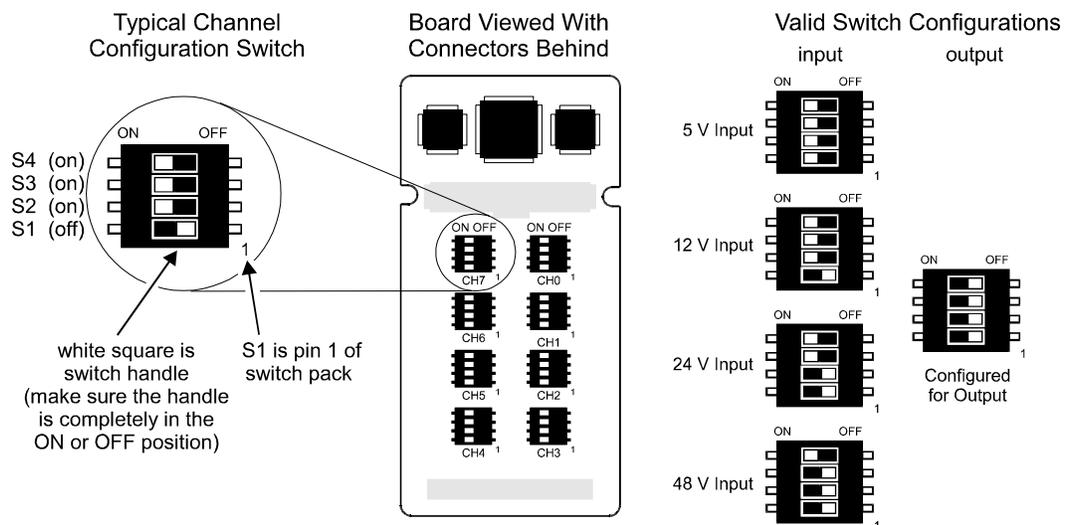


Figure 1 Locating and Setting Threshold Switches

Important!

Make certain that you slide the switch handles completely to the ON or OFF position! Verify switch settings with the `INP:THReshold:LEVel?` command.

An invalid switch setting will cause the related channel to behave as an input with unknown threshold level.

Configuring for Input

Refer again to Figure 1 for the four valid input threshold, switch configurations. Table 1 shows the "input zero" and "input one" levels for the nominal threshold settings.

Table 1 Input Threshold Voltage Levels

| Nominal Threshold Level | Input One VDC Minimum | Input Zero VDC Maximum |
|-------------------------|-----------------------|------------------------|
| 5 | 2.1 | 1.4 |
| 12 | 7 | 2 |
| 24 | 13 | 3 |
| 48 | 25 | 5 |

Configuring for Output

By turning all four of its threshold-setting switches OFF, a channel is configured as an output channel.

Installation

After the switches have been configured, the installation for this Plug-on is common to several others and is covered in Chapter 1 of your VXI Module User's Manual.

Connecting To The Terminal Module

To get started on field wiring to the VT1536A SCP you'll need to know that input-configured channels ARE POLARIZED. That is the H terminal must be driven positive relative to the L terminal. Output-configured channels are not polarized. For more information see "Input and Output Characteristics" on page 7.

The SCP connections for the Terminal Modules are shown on the self-adhesive labels that come with the SCP. Use these to label terminal definitions on your terminal module. The connections are shown in Figure 2.

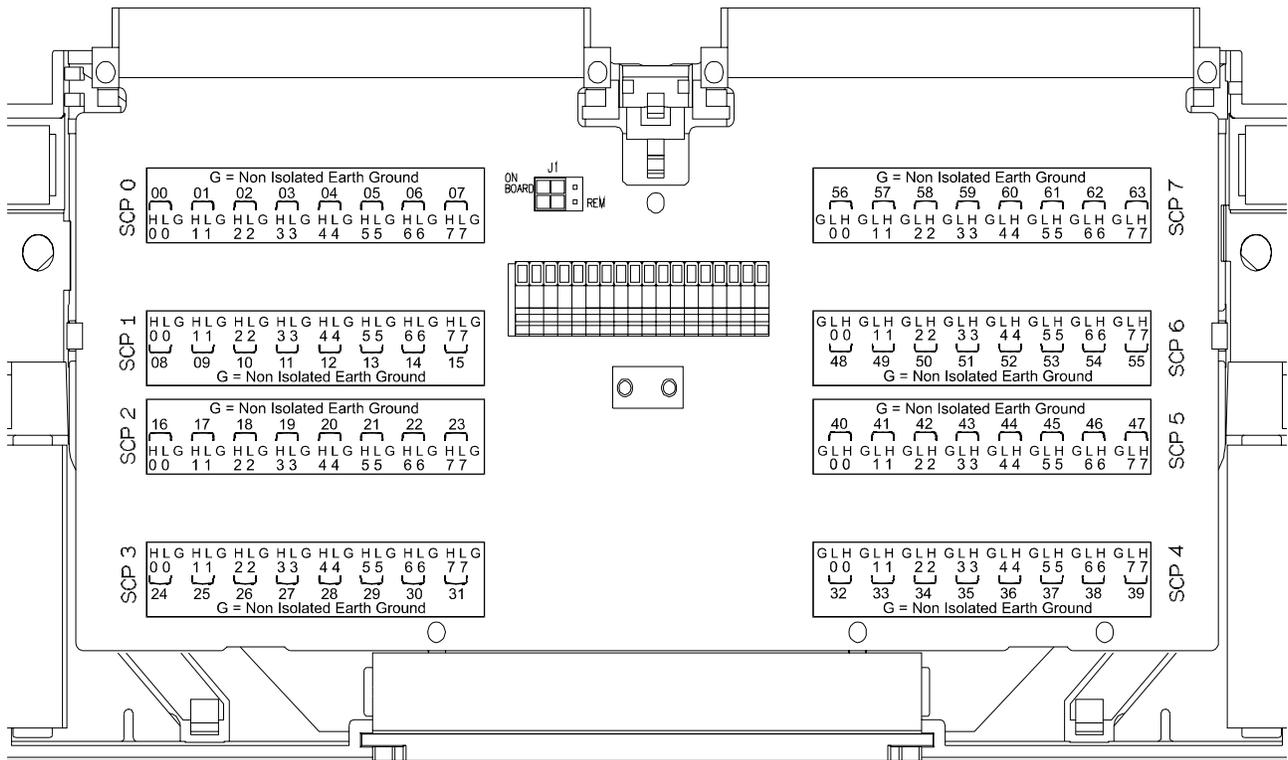


Figure 2 VT1415A/19A/22A Terminal Module Connections

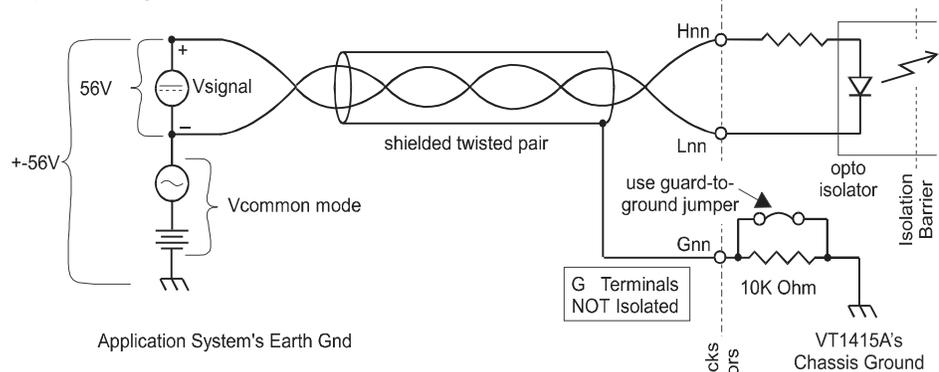
Recommended Signal Connections

Figure 3 shows the recommended method of wiring isolated digital I/O channels, as well as the maximum voltage limitations for the VT1536A.

Figure 3 shows the shields connected directly to the VT1415A/19A ground. This is to limit potential noise on the isolated digital wiring from affecting low-level analog channel wiring within the Terminal Module.

Note The VT1536A is a true isolated SCP. There is no electrical connection between each channel's Hi/Lo terminals and VT1415A/19A's chassis ground. However the G (analog guard) terminals are connected through 10 kOhm resistors to chassis ground within the VT1415A/19A. These terminals are NOT isolated.

Input Configured VT1536A Channel



Output Configured VT1536A Channel

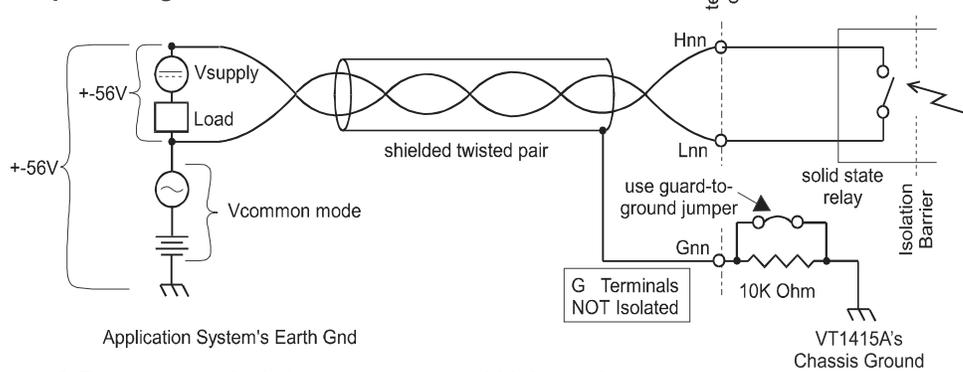


Figure 3 Recommended Connections and Voltage Limits

Input and Output Characteristics

This section describes the electrical characteristics of the SCP's input and output sections, as well as the operation of the input debounce timers. Figure 4 shows a simplified schematic of one VT1536A channel.

Input Characteristics

The input section drives an opto-isolator through a resistor threshold setting network. Your system must provide at least 1 mA of current to drive the opto-isolator. The threshold setting network controls this drive current for various input voltages ranging from 5 to 48 Volts (see Table 1 on page 5). Your input voltage must be polarized positive to the Hnn terminal, and negative to the Lnn terminal.

Output Characteristics

The opto-isolated output provides a Solid-State relay and relay protection voltage clamping diode. The solid state relay is non-polarized. The voltage clamping diode limits voltage at the relay output to 80 V_{PEAK} (begins to conduct at about 60 V_{PEAK}). The SS relay's on-resistance is 10 Ω, off-resistance is at least 10¹⁰Ω. The relay's turn-on time is 3 milliseconds.

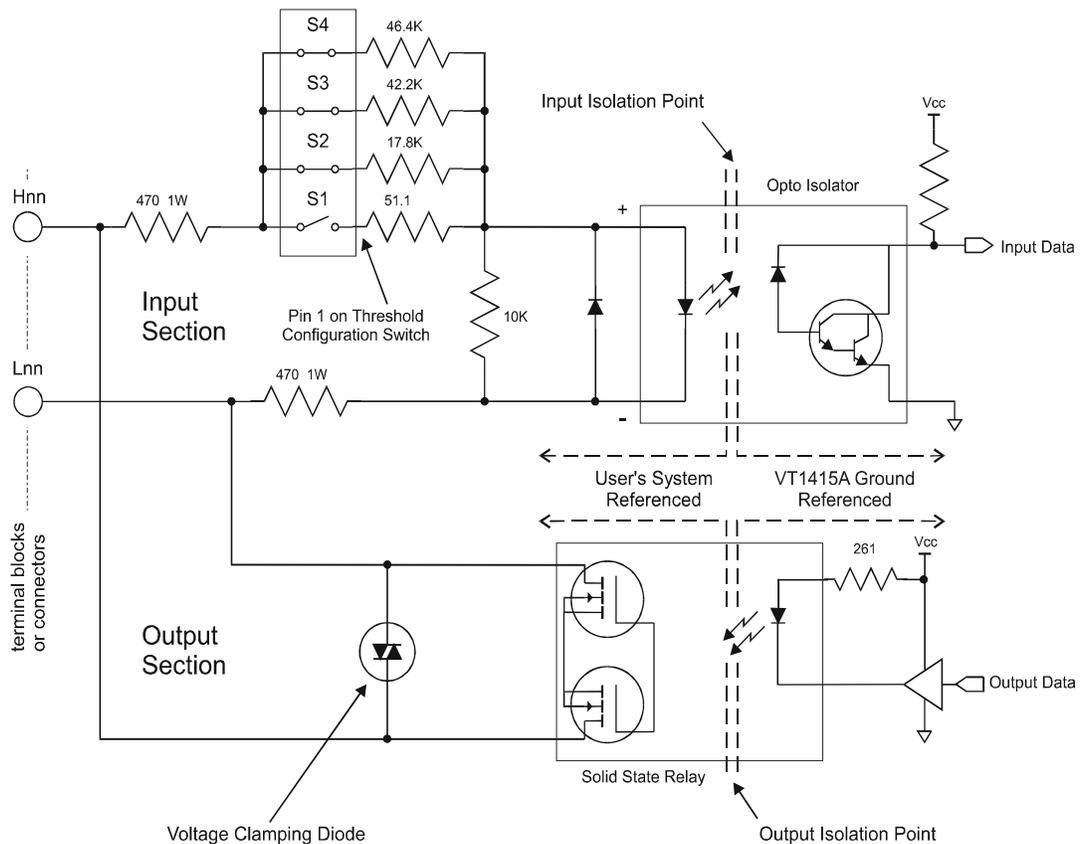


Figure 4 The VT1536A Input and Output Sections

Output Voltage Clamp

The output section incorporates a "crowbar" protection type voltage clamping diode. In normal operation with the relay voltage at or below 56 Volts peak, the diode has virtually no effect (other than about 10 nanoamperes of leakage current). At 60 Volts, the diode starts to conduct to limit further voltage excursions. In this region, the diode effectively clamps momentary voltage spikes from inductive loads. If an overvoltage condition occurs that drives a voltage surge in the diode to 80 Volts, the diode will latch-on, clamping the voltage to a few volts. This latched-on condition will continue until the current surge through the diode is reduced to less than 150 mA, whereupon the diode returns to its off state.

Debounce Function

Setting the appropriate debounce period ensures that the VT1415A/19A algorithm reads only the most current VALID digital input state as latched into the SCP channel. By "valid" we mean that the signal has not made any 0-to-1 or 1-to-0 transitions for the duration of the debounce period (the signal has settled). If the algorithm reads a channel that has not yet settled, it will receive the previously latched valid state (no change).

Debounce is controlled using VT1415A/19A SCPI commands. When the debounce feature is enabled, inputs are tested for debounce, and valid states are latched every $1 \frac{1}{3}$ debounce periods. This debounce-and-latch rate is

completely asynchronous with the VT1415A/19A algorithm execution rate as set by the Trigger Timer (TRIG:TIMER command). Long debounce periods combined with fast Trigger Timer settings would have the algorithm executing several times for each input debounce-and-latch period. Conversely, short debounce periods and slow Trigger Timer rates would allow multiple debounce-and-latches per algorithm execution.

Debounce Example

Figure 5 demonstrates the use of debounce. Here we show a system that uses a digital line to sense a switch an operator would throw to signal the algorithm to shut down a process. The digital line runs through an electrical environment that could cause a false shut-down signal when a large motor starts. The motor start period is at most 0.5 seconds. The algorithm executes every 100 ms so without debounce it could sense this electrical noise as a false shut-down signal. If we set the debounce period to 1.228 seconds, the VT1536A will ignore the motor start-up noise and will only latch signal states that last as long or longer than the debounce period.

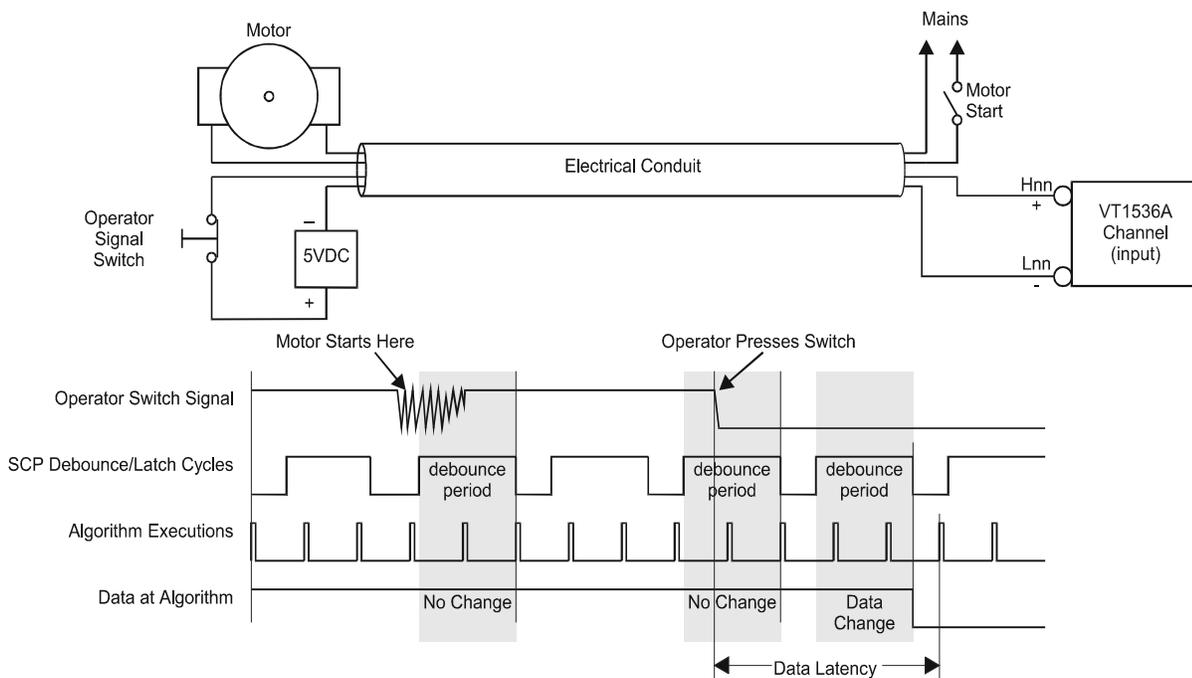


Figure 5 Example Using Debounce Feature

Data Latency

With the debounce feature on, the data latency (the time from valid signal transition to acquisition by the algorithm) is up to 1.333 times the debounce period plus one VT1415A/19A trigger repetition period (TRIG:TIM:PERIOD).

With the debounce feature off (INPut:DEBounce 0,(@<ch_list>)), the latency is only the algorithm repetition rate.

- INP:THR:LEV? returns a numeric value which is one of 5, 12, 24, 48 or 0 (zero) where zero means that the channel is configured as an output and non-zero values indicate the input threshold in volts.

Note If an invalid switch combination is set, INP:THR:LEV? will NOT return a value and will generate the error 3105 "Invalid SCP switch setting". This error will also be generated when *RST is executed. Channels associated with this error will behave as input channels with unknown threshold levels.

To query the threshold level on the second channel at SCP position 2 send:

INP:THR:LEV? (@117) *query 2nd chan on SCP pos. 2*
enter statement here *returns 0 | 5 | 12 | 24 | 48*

Configuring Input Channel Polarity

To configure input channel polarity use the command:
INPut:POLarity INVerted | NORMal,(@<ch_list>)

To configure the first 2 channels on an VT1536A in SCP position 4 to input Normal polarity (opto on=logical 1) and its next 2 channels to input inverted polarity (opto off=logical 1) send:

INP:POL NORM,(@132,133) *NORM is *RST default*
INP:POL INV,(@134,135)

There is also the query form; INPut:POLarity? (@<channel>), where <channel> must specify a single channel. INP:POL? returns NORM | INV.

Note The INPut:POL command will generate the error 3107, "Channel data direction conflicts with command" if any channel in <ch_list> is configured as an output.

Setting Debounce Time

For a description of the debounce function See "Debounce Function" on page 8. The VT1536A has two debounce timers. One for the lower four channels, and one for the upper four channels. To set the debounce timers use the command:

INPut:DEBounce:TIME <time>,(@<ch_list>)

- <time> can be one of 16 possible numeric values or MIN and MAX:

Note Because the clock that generates the debounce period is asynchronous to your input signal, there is a region of uncertainty relative to the nominal debounce period selected. This is reflected in the "Minimum" and "Maximum" debounce period columns in Table 2.

Choose a value from the “Minimum Period” column in Table 2 that is longer than your input signal’s undesired transition period when you want to exclude these short term input signal transitions.

Choose a value from the “Maximum Period” column in Table 2 that is shorter than your input signal’s expected transition period when you want to be certain to include these desired input signal transitions.

The values to send to the VT1536A are in the “Nominal” column in Table 2 below.

Table 2 Nominal Debounce Period and Uncertainties

| Minimum Period | Nominal Value | Maximum Period |
|----------------|---------------|----------------|
| debounce off | 0 | debounce off |
| 0.08 ms | 0.15 ms | 0.18 ms |
| 0.20 ms | 0.30 ms | 0.35 ms |
| 0.45 ms | 0.60 ms | 0.65 ms |
| 0.95 ms | 1.20 ms | 1.30 ms |
| 1.90 ms | 2.40 ms | 2.50 ms |
| 4.10 ms | 4.80 ms | 5.00 ms |
| 8.20 ms | 9.60 ms | 9.85 ms |
| 16.4 ms | 19.2 ms | 19.7 ms |
| 32.8 ms | 38.4 ms | 39.4 ms |
| 65.5 ms | 76.6 ms | 78.7 ms |
| 131 ms | 153.6 ms | 158 ms |
| 262 ms | 307.2 ms | 315 ms |
| 525 ms | 614.4 ms | 630 ms |
| 1.05 s | 1.2288 s | 1.26 s |
| 2.10 s | 2.4576 s | 2.52 s |

-- Sending 0 or MIN turns debounce off. Sending MAX selects 2.458 seconds.

-- If a value is sent that is slightly greater than one of these values, the next higher value (or MAX) is selected. Values outside of the range 0 - 2.4576 will generate the error -222, "Data out of range".

- *<ch_list>* must contain all 4 of the upper-bank channels, or all 4 of the lower-bank channels, or all 8 channels for a given SCP. This is because the VT1536A has two debounce timers, one for its lower 4 channels and one for its upper 4 channels.

Note The INP:DEB:TIME generate the error 3108, "E1536 debounce - each referenced 4 Ch bank must contain at least one input". This error indicates that you tried to set a debounce time for a bank of channels that contains no input configured channel.

To set the debounce period to 153.6 ms for the lower 4 channels on an VT1536A in SCP position 0 send:

```
INP:DEB 0.1536,(@100:103)
```

To set the debounce period to 1.229 seconds for the upper 4 channels on an VT1536A in SCP position 3 send:

```
INP:DEB 1.229,(@128:131)
```

There is also the query form;
INPut:DEBounce:TIME? (@<channel>)
where <channel> must specify a single channel. INP:DEB:TIME? returns the currently set debounce period.

Configuring Output Channel Polarity

To configure output channel polarity use the command:
OUTPut:POLarity INVerted | NORMal,(@<ch_list>)

To configure the fifth and sixth channels on an VT1536A in SCP position 4 to output normal polarity (logical 1=relay on) and its next 2 channels to output inverted polarity (logical 1=relay off) send:

```
OUTP:POL NORM,(@136,137)           NORM is *RST default  
OUTP:POL INV,(@138,139)
```

There is also the query form; OUTPut:POLarity? (@<channel>), where <channel> must specify a single channel. OUTP:POL? returns "NORM" or "INV".

Notes

1. The OUTPut:POL command will generate the error 3107, "Channel data direction conflicts with command" if any channel in <ch_list> is configured as an input.
 2. An output channel's SS relay will not change from the *RST state (open) regardless of its POLarity setting, until an algorithm writes a value to that channel.
-

Programming with the VT1415A/19A Algorithm Language

The following example shows the command sequence (platform/language independent) to transfer the digital states from the lower 4 channels (inputs) to the upper 4 channels (outputs). In other words, the state you input to one of the lower 4 channels will drive the corresponding output channel. The example assumes that the SCP is installed in SCP position 0 (covers channels 0 through 7), the first four channels are configured as inputs, and the last four are configured as outputs (See "Setting Configuration Switches" on page 4.).

```
*RST                               reset module to default states  
ALG:DEF 'ALG1','O104=I100; O105=I101; O106=I102; O107=I103;' defines the algorithm  
INIT                               start algorithm (using default trig sys setup)
```

When the algorithm is run, digital states input to channels 0 through 3 will be output on channels 4 through 7.

*RST and *TST? (Important!)

The *RST/Power-up state and *TST? command reset the VT1415A/19A to its default state. This will cause all output-configured channel solid-state relays to "open" (turn off), disable debounce, and restore channel polarity to normal. Keep this in mind when applying the VT1536A SCP to your system and design the "open" state as the safe state for your system.

Note *RST will report error 3105, "Invalid SCP switch setting" if one or more configuration switches are set to invalid configurations.

Specifications

SCP Power Supply Requirements

| +5 Vmax | +24 Vtyp | +24 Vmax | -24 Vtype | -24 Vmax |
|---------|----------|----------|-----------|----------|
| 0.072 | not used | | not used | |

Output Characteristics

(see also Figure 4)

| Characteristic | Specification |
|----------------------------|-------------------------------|
| Maximum Continuous Voltage | 56 VDC (39 V _{RMS}) |
| Peak Current Load | 200 mA |
| Relay On Resistance | 10 Ω |
| Turn On/Off Time | 3 ms |
| Clamping Voltage* | 60 V |

* See "Output Voltage Clamp" on page 8.

Input Characteristics

(see also Figure 4)

| Characteristic | Specification |
|----------------------------|--|
| Maximum Continuous Voltage | 56 VDC (39 V _{RMS}) |
| Maximum Input Zero | See Table 1 on page 5 |
| Minimum Input One | See Table 1 on page 5 |
| Input Debounce Time | 150 μs - 2.4 s. See Table 2 on page 12 |

Notes:
