

**2-Mbit (256K x 8) MoBL<sup>®</sup> Static RAM**

**Features**

- **Very high speed: 45 ns**
  - **Wide voltage range: 2.20V – 3.60V**
- **Pin-compatible with CY62138CV30**
- **Ultra-low standby power**
  - **Typical standby current: 1  $\mu$ A**
  - **Maximum standby current: 7  $\mu$ A**
- **Ultra-low active power**
  - **Typical active current: 2 mA @ f = 1 MHz**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in Pb-free 36-ball BGA package**

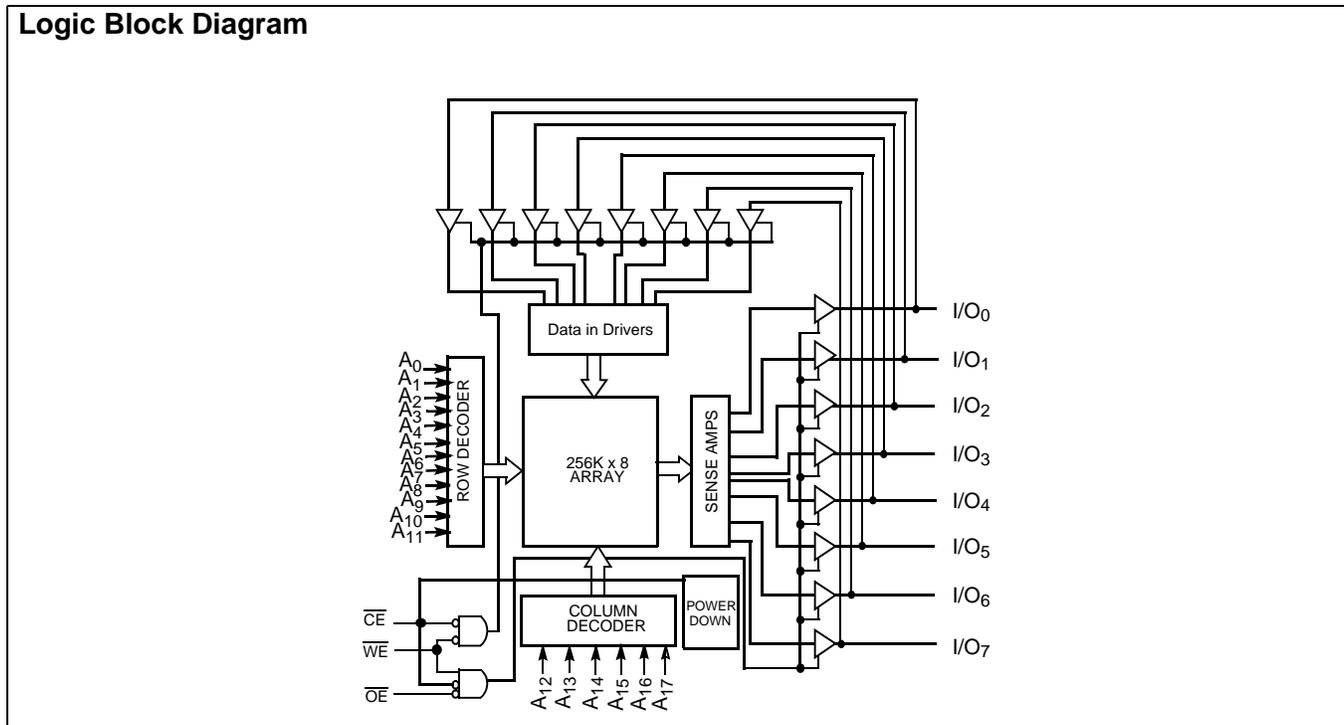
**Functional Description<sup>[1]</sup>**

The CY62138EV30 is a high-performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption when deselected ( $\overline{\text{CE}}$  HIGH).

Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

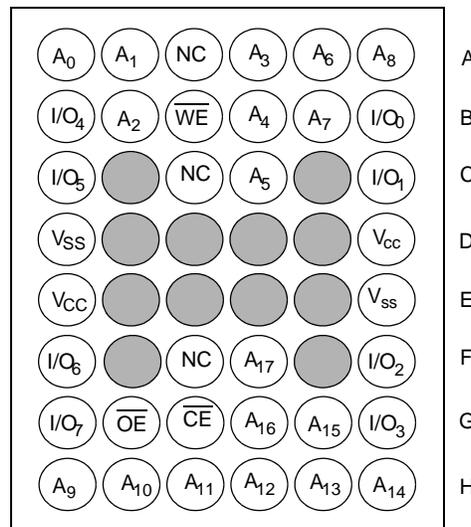


**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2]</sup>**

**FBGA**  
**Top View**



**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
	Min.	Typ. <sup>[3]</sup>	Max.		f = 1 MHz		f = f <sub>max</sub>		Standby I <sub>SB2</sub> (μA)	
					Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.
CY62138EV30LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7

**Notes:**

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... 55°C to +125°C
- Supply Voltage to Ground Potential ..... -0.3V to  $V_{CC(MAX)}$  + 0.3V
- DC Voltage Applied to Outputs in High-Z State<sup>[4,5]</sup> ..... -0.3V to  $V_{CC(MAX)}$  + 0.3V

- DC Input Voltage<sup>[4,5]</sup> ..... -0.3V to  $V_{CC(MAX)}$  + 0.3V
- Output Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current..... > 200 mA

Product	Range	Ambient Temperature	$V_{CC}$ <sup>[6]</sup>
CY62138EV30LL	Industrial	-40°C to +85°C	2.2V to 3.6V

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62138EV30-45			Unit
			Min.	Typ. <sup>[3]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA, V <sub>CC</sub> = 2.20V	2.0			V
		I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> = 2.70V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA, V <sub>CC</sub> = 2.20V			0.4	V
		I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 2.70V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V	1.8		V <sub>CC</sub> + 0.3V	V
		V <sub>CC</sub> = 2.7V to 3.6V	2.2		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.2V to 2.7V	-0.3		0.6	V
		V <sub>CC</sub> = 2.7V to 3.6V	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , V <sub>CC</sub> = V <sub>CCmax</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels		15	20	mA
		f = 1 MHz		2	2.5	mA
I <sub>SB1</sub>	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, and WE), V <sub>CC</sub> = 3.60V		1	7	μA
I <sub>SB2</sub>	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V		1	7	μA

**Capacitance** for all packages<sup>[7]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ.)</sub>	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

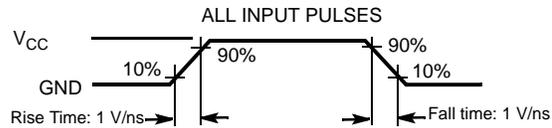
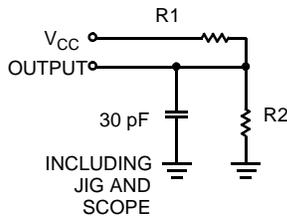
**Notes:**

4. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
5. V<sub>IH(max.)</sub> = V<sub>CC</sub>+0.75V for pulse durations less than 20 ns.
6. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min.)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.

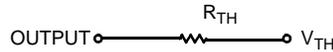
### Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	72	$^{\circ}\text{C}/\text{W}$
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		8.86	$^{\circ}\text{C}/\text{W}$

### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

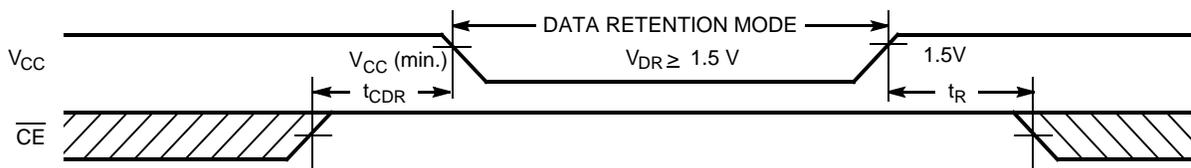


Parameters	2.50V	3.0V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

### Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[3]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1\text{V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{V}$ , $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$		0.8	3	$\mu\text{A}$
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[8]}$	Operation Recovery Time		$t_{RC}$			ns

### Data Retention Waveform



**Notes:**

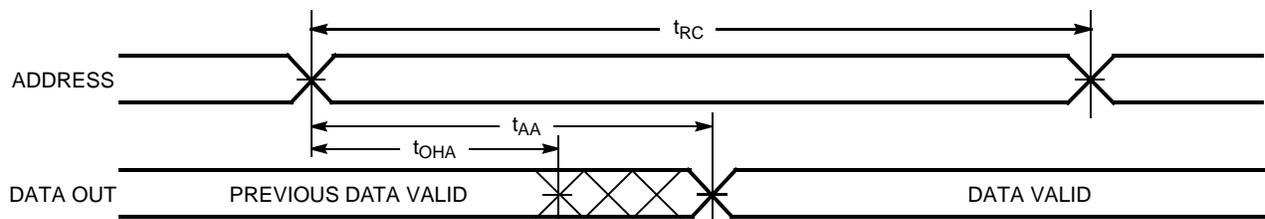
- 7. Tested initially and after any design or process changes that may affect these parameters.
- 8. Full Device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 100 \mu\text{s}$  or stable at  $V_{CC(min.)} \geq 100 \mu\text{s}$ .

**Switching Characteristics** (Over the Operating Range)<sup>[9]</sup>

Parameter	Description	45 ns		Unit
		Min.	Max.	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	45		ns
$t_{AA}$	Address to Data Valid		45	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[10]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[10,11]</sup>		18	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[10]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[10, 11]</sup>		18	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-up		45	ns
<b>Write Cycle<sup>[12]</sup></b>				
$t_{WC}$	Write Cycle Time	45		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	35		ns
$t_{AW}$	Address Set-up to Write End	35		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		ns
$t_{SD}$	Data Set-up to Write End	25		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[10, 11]</sup>		18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[10]</sup>	10		ns

**Switching Waveforms**

**Read Cycle No. 1 (Address Transition Controlled)<sup>[13, 14]</sup>**

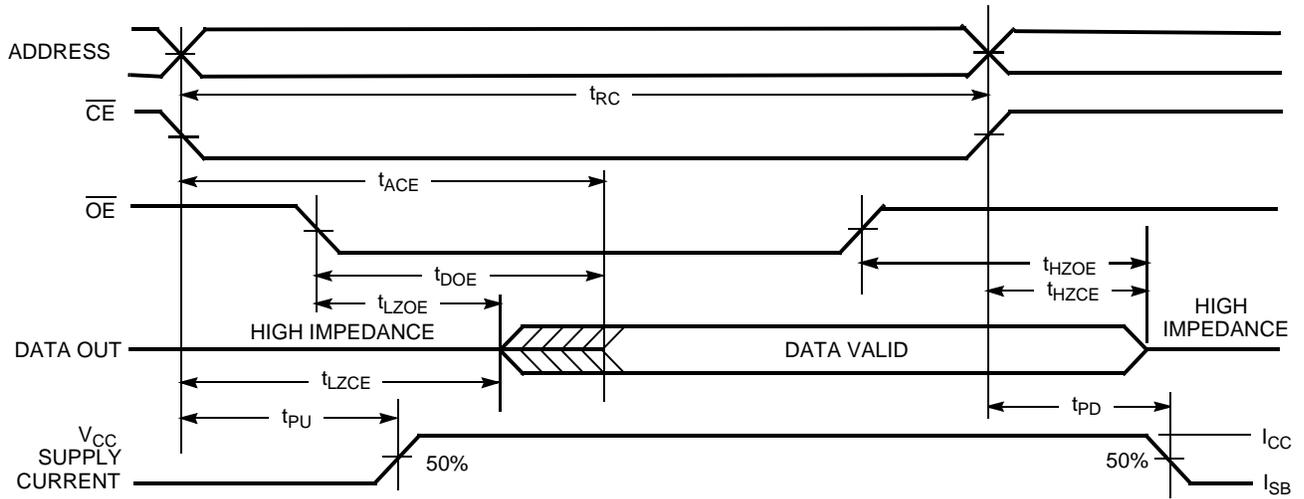


**Notes:**

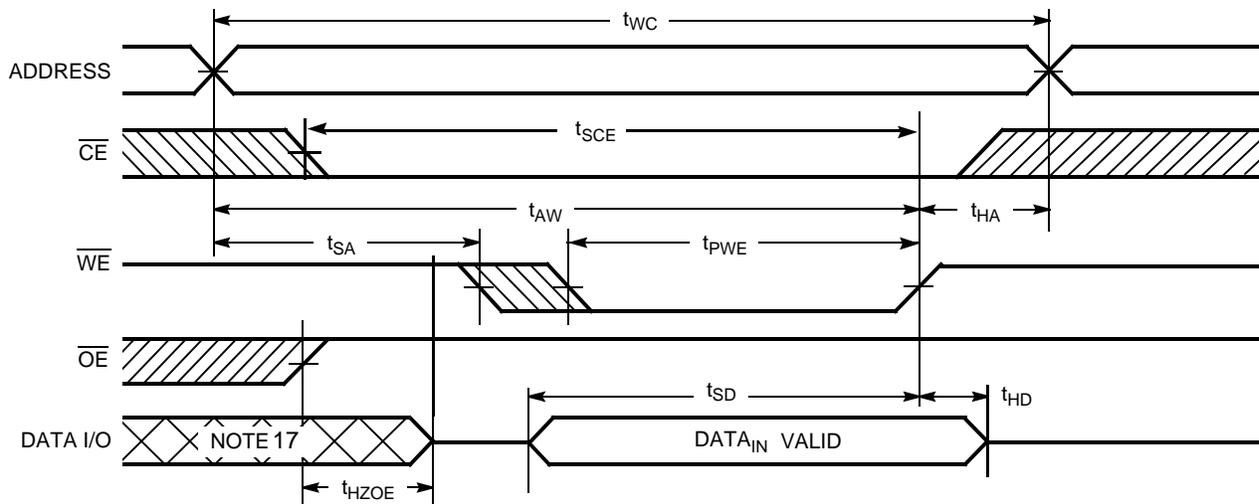
9. Test Conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
10. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
11.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enter a high-impedance state.
12. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $CE = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
13. Device is continuously selected.  $\overline{OE}$ ,  $CE = V_{IL}$ .
14.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms** (continued)

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)**<sup>[14, 15]</sup>



**Write Cycle No. 1 ( $\overline{WE}$  Controlled)**<sup>[16, 18]</sup>

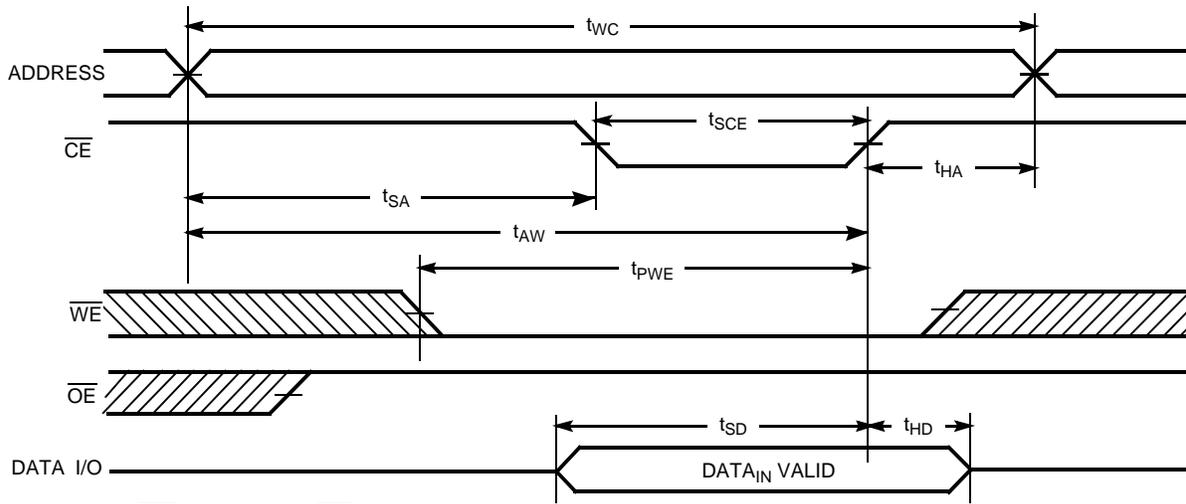


**Notes:**

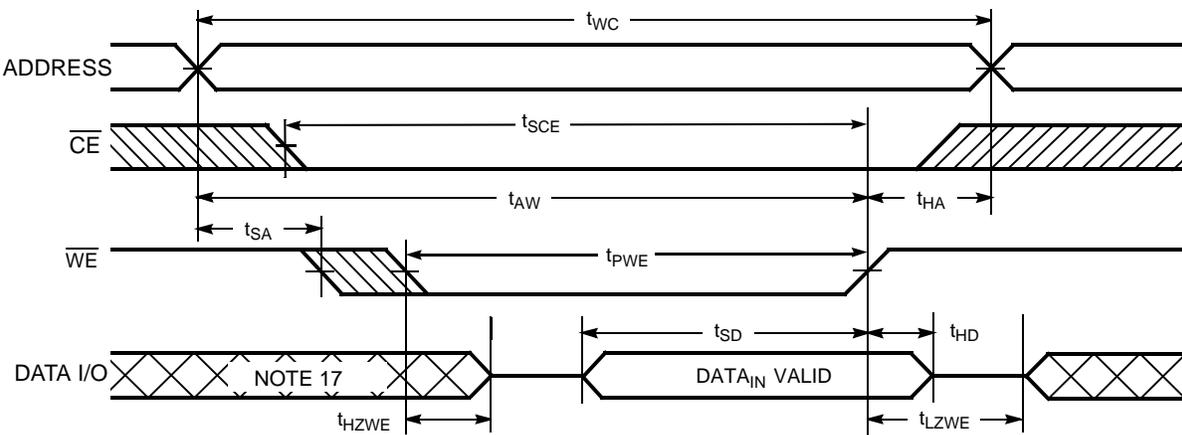
- 15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 16. Data I/O is high impedance if  $OE = V_{IH}$ .
- 17. During this period, the I/Os are in output state and input signals should not be applied.
- 18. If CE goes HIGH simultaneously with WE HIGH, the output remains in high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 2 (CE Controlled)<sup>[16, 18]</sup>**



**Write Cycle No. 3 (WE Controlled, OE LOW)<sup>[18]</sup>**



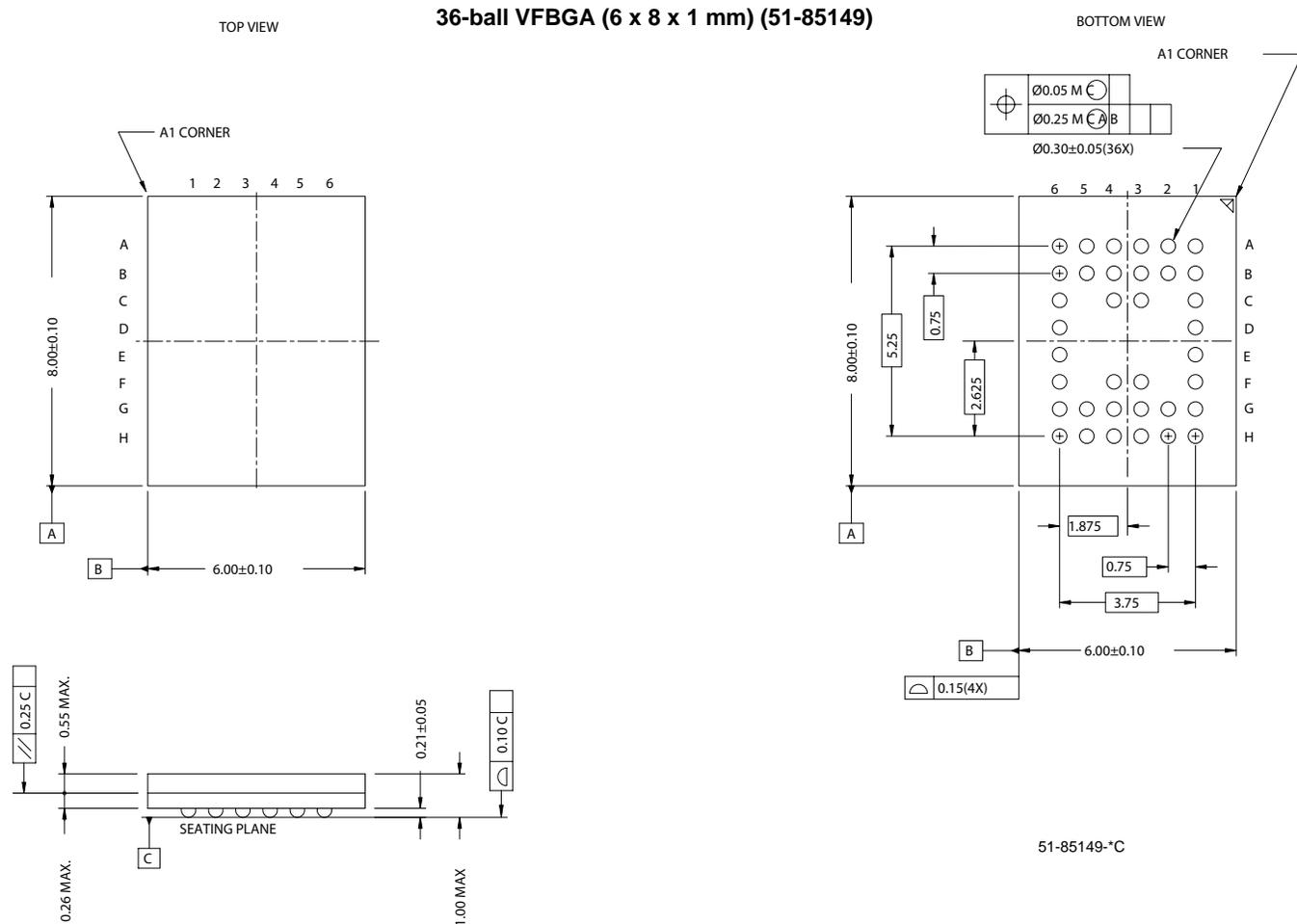
**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	Data Out ( $I/O_0-I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	Data in ( $I/O_0-I/O_7$ )	Write	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138EV30LL-45BVXI	51-85149	36-ball Very Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-free)	Industrial

**Package Diagrams**



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**Document History Page**

Document Title: CY62138EV30 2-Mbit (256K x 8) MoBL® Static RAM				
Document Number: 38-05577				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	237432	See ECN	AJU	New data sheet
*A	427817	See ECN	NXR	<p>Removed 35 ns Speed Bin</p> <p>Removed "L" version</p> <p>Removed 32-pin TSOPII package from product Offering.</p> <p>Changed ball C3 from DNU to NC.</p> <p>Removed the redundant footnote on DNU.</p> <p>Moved Product Portfolio from Page # 3 to Page #2.</p> <p>Changed I<sub>CC</sub> (Max) value from 2 mA to 2.5 mA and I<sub>CC</sub> (Typ) value from 1.5 mA to 2 mA at f = 1 MHz</p> <p>Changed I<sub>CC</sub> (Typ) value from 12 mA to 15 mA at f = f<sub>max</sub>=1/t<sub>RC</sub></p> <p>Changed I<sub>SB1</sub> and I<sub>SB2</sub> Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA.</p> <p>Changed V<sub>CC</sub> stabilization time in footnote #7 from 100 μs to 200 μs</p> <p>Changed the AC test load capacitance from 50pF to 30pF on Page# 4</p> <p>Changed V<sub>DR</sub> from 1.5V to 1V on Page# 4.</p> <p>Changed I<sub>CCDR</sub> from 1 μA to 3 μA in the Data Retention Characteristics table on Page # 4.</p> <p>Corected t<sub>R</sub> in Data Retention Characteristics from 100 μs to t<sub>RC</sub> ns</p> <p>Changed t<sub>OHA</sub>, t<sub>LZCE</sub>, t<sub>LZWE</sub> from 6 ns to 10 ns</p> <p>Changed t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZWE</sub> from 15 ns to 18 ns</p> <p>Changed t<sub>LZOE</sub> from 3 ns to 5 ns</p> <p>Changed t<sub>SCE</sub> and t<sub>AW</sub> from 40 ns to 35 ns</p> <p>Changed t<sub>SD</sub> from 20 ns to 25 ns</p> <p>Changed t<sub>PWE</sub> from 25 ns to 35 ns</p> <p>Updated the Ordering Information table and replaced Package Name column with Package Diagram.</p>