HEWLETT PACKARD

DIGITAL OUTPUT CARD
MODEL 69731B

OPERATING MANUAL

FOR SERIAL NUMBERS 2139A-00101

AND ABOVE.*

*For cards with serial prefixes above 2139A-00101, a manual change page may be included.

*For cards with serial prefixes below 2139A, refer to Appendix A.

Manual Part No. 69731-90003
Microfiche Part No. 69731-90004

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

BEFORE APPLYING POWER.

Verify that the product is set to match the available line voltage and the correct fuse is installed.

GROUND THE INSTRUMENT.

This product is a Safety Class 1 instrument (provided with a protective earth terminal). To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument must be connected to the ac power supply mains through a three-conductor power cable, with the third wire firmly connected to an electrical ground (safety ground) at the power outlet. For instruments designed to be hard-wired to the ac power lines (supply mains), connect the protective earth terminal to a protective conductor before any other connection is made. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury. If the instrument is to be energized via an external autotransformer for voltage reduction, be certain that the autotransformer common terminal is connected to the neutral (earthed pole) of the ac power lines (supply mains).

INPUT POWER MUST BE SWITCH CONNECTED.

For instruments without a built-in line switch, the input power lines must contain a switch or another adequate means for disconnecting the instrument from the ac power lines (supply mains).

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified service personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power, discharge circuits and remove external voltage sources before touching components.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

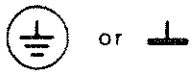
DO NOT EXCEED INPUT RATINGS.

This instrument may be equipped with a line filter to reduce electromagnetic interference and must be connected to a properly grounded receptacle to minimize electric shock hazard. Operation at line voltages or frequencies in excess of those stated on the data plate may cause leakage currents in excess of 5.0 mA peak.

SAFETY SYMBOLS.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual (refer to Table of Contents).

Indicates hazardous voltages.



Indicate earth (ground) terminal.

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

Instruments which appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

SECTION I
GENERAL INFORMATION

1-1 SCOPE OF MANUAL

1-2 This manual covers the Installation, Pre-Operation, and Theory of operation for the Digital Output card, Model 69731B. Servicing instructions and information on the programming of the card are not included. This manual also covers Model 69731A provided the differences explained in Appendix A are incorporated. Programming examples of the Digital Output card are shown in Chapter 7 of the 6942A Multiprogrammer User's Guide. Additional documents that contain general information on I/O cards are:

- 6942A Multiprogrammer User's Guide for HP 9825/35/45 Controllers (HP 06942-90003).
- 6942A Multiprogrammer User's Guide for HP 85 Controllers (HP 06942-90011).
- 6942A Multiprogrammer User's Guide for HP 9826 Controllers (HP 06942-90013).
- 6942A Multiprogrammer Technical Data (HP 5952-4034).
- 6942A Multiprogrammer Installation and Assembly Level Service Manual (HP 6942A-90006).

1-3 Any of these manuals can be ordered directly from your local Hewlett-Packard sales office. Give the applicable HP manual part number as indicated above.

1-4 DESCRIPTION

1-5 The Digital Output card provides sixteen programmable TTL, DTL, or CMOS compatible output data lines. As shipped, the card is configured so that all 16-output data lines are positive true TTL logic connected via pull-up resistors to +5 Vdc. An output data line goes high when the bit position corresponding to that data line is specifed as a "1" in an output type instruction issued at the Controller.

1-6 Various jumpers on the card permit the user to change the operation of the data lines as follows:

a. A single jumper (W51) can be installed to invert the logic sense of all 16-data lines to negative true logic. When this card is shipped as part of Option 042 (AC Power Controller, Model 14570A), jumper W51 is installed at the factory.

b. When a bias voltage greater than the local +5 Vdc is required, jumper W16 is removed to disconnect the +5 Vdc, and another jumper, W15, is installed to connect an externally supplied voltage of up to 30 Vdc to all pull-up resistors. For example, a 15 Vdc external bias can be connected to the edge connector (in lieu of the card +5 V) to make the output logic levels compatible with external CMOS logic operating at +15 V.

c. Any or all data lines can be converted to open-collector outputs by clipping out the applicable data line, pull-up resistors. The data line can then be used to drive loads that are connected to an external voltage of up to 40 Vdc and up to 100mA. For example, this type of connection is desirable when a data line is required to drive a small lamp or relay load connected to its own supply voltage.

d. By installing a single jumper, W52, a diode is automatically connected in parallel with every pull-up resistor. This is desirable when the output lines are used to drive relays and a diode is required in shunt with the relay coil. The external relay voltage would be connected back to the card via an external bias connection (pin V at the edge connector) with jumper W15 installed and jumper W16 removed.

1-7 Typical applications of how the data lines can be connected in a manner different from their "as shipped" configuration are given in Figure 3-5.

1-8 Data words are transferred to the Digital Output card using subaddress 0. The data word sent can be readback using subaddress 3. Readback of data from first rank storage allows the user to check the validity of data before the data is advanced to second rank storage. Cycling a Digital Output card transfers the data from first rank storage to second rank storage. The output data lines are driven by the data stored in second rank storage. The card can be cycled by either a programmed instruction or by an External Trigger (EXT) Signal.

1-9 Another external signal, External Enable (EEN), permits the user to set all output lines to logic zero (or to logic high if jumper W51 is installed). A contact closure or low logic level applied between the External Enable pin and the common pin at the card's edge connector forces this condition.

1-10 Separate Gate and Flag external signals are available to permit 'handshaking of data' between the customer's logic and the card logic to insure reliable data transfers. As shipped, the GATE output line is jumpered (W10) to the Flag input line. To enable handshaking operations, jumper W10 must be removed.

1-11 A breadboard area of drilled and plated-through circuit pads is available for customers who want to install converter modules or other special-purpose circuits. One column of circuit pads (six for +5 V, six for ground) are dedicated for power connections. Jumpers in series with the output data lines can be removed so that interconnections can be made

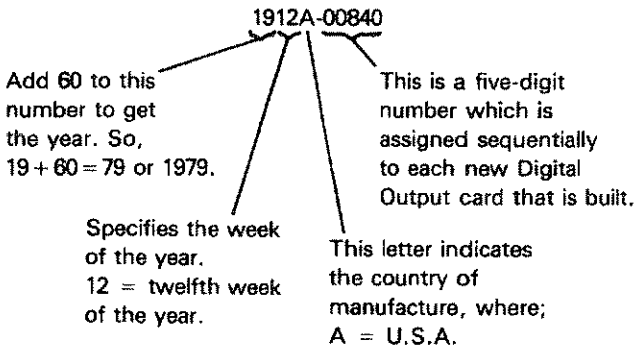
between the breadboard circuits and the external edge connector.

1-12 SPECIFICATIONS

1-13 Specifications and other supplemental data for the Digital Output card are given in Table 1-1.

1-14 CARD AND MANUAL IDENTIFICATION

1-15 Hewlett-Packard I/O cards are identified by a two-part serial number, for example, 1912A-00840. This number appears on a label affixed to the component side of the circuit card. The breakdown of the serial number is explained using the example number 1912A-00840.



1-16 The first part of this serial number (year and week) indicates the last date when a significant design change was made

Table 1-1. Specifications and Supplemental Data

DIGITAL OUTPUTS:

TTL Logic Levels - As shipped, all data line outputs are jumper connected as positive true with 5.1KΩ pull-up resistors connected to +5 V. In the high state, the outputs will source up to 200μA at 3.8 V minimum. In the low state, the outputs will sink up to 100 mA at 0.5 V maximum.

Open Collector - Any or all output lines can be converted to open-collector outputs by clipping out the associated 5.1kΩ resistor. The maximum collector voltage is 40 volts, and the maximum sink current is 100 mA.

External Bias - Up to 30 V maximum when using card pull-up resistors.

CARD'S EXTERNAL I/O CONTROL LINES:

EXTERNAL ENABLE (Input Signal) - When high, the output data lines are enabled; when low, the output data lines are low.
High = 2.0 V to 5.0 V. (or no connection)
Low = 0.0 V to 0.5 V. (or short to ground)

EXTERNAL TRIGGER (Input Signal) - Edge sensitive signal used to transfer data from first to second rank storage and to the card's output terminals.

TRIGGER POLARITY SELECT (Input Signal) - Defines the true state of the EXTERNAL TRIGGER. High means High true EXTERNAL TRIGGER.
High = 2.0 V to 5.0 V (or no connection).
Low = 0.0 V to 0.5 V (or short to ground).
The driving signal must sink 1 mA in the low state.

GATE (Output Signal) - Output data is valid when gate goes high.
High = 3.7 V while sourcing 200μA.
Low = 0.5 V while sinking 7 mA.

$\overline{\text{GATE}}$ (Output signal) - Same as GATE, but logic sense is inverted (low true).

FLAG (Input Signal) - indicates that data has been accepted.
High = 2.0 V to 5.0 V (or open circuit).
Low = 0.0 V to 0.5 V (or contact closure to ground).
The driving signal must sink 1 mA in the low state.

FLAG POLARITY SELECT (Input Signal) - Defines the true state of the FLAG signal.
High means High true FLAG. Low means Low true FLAG.
High = 2.0 V to 5.0 V (or not connection).
Low = 0.0 V to 0.5 V (or short to ground).
The driving signal must sink 1 mA in the low state.

END OF PROCESS (Output Signal) - This signal goes high to indicate that the card has completed its operation. After a minimum of 2μs it is reset low by the Multiprogrammer.
High = 3.7 V while sourcing 2002ms.
Low = 0.5 V while sinking 7 mA.

BUSY (Output Signal) - This signal goes high while the card is busy performing its operation.

High = 3.7 V while sourcing 200μA.
Low = 0.5 V while sinking 7 mA.

TEMPERATURE RANGE:
From 0°C to +70°C operating in the mainframe (allows 15°C internal rise in temperature when operating in the mainframe at up to +55°C ambient); From −40°C to +80°C storage.

CARD DIMENSIONS:
Card - 299.722mm x 132.08mm (11.8 in. x 5.2 in.).
Card Breadboard Area - 98.4mm x 60.3mm (3-7/8 in x 2-3/8 in.).

+5 V Current Requirement: 750 mA. Max.

1-17 Each I/O card is equipped with a handle that is marked to identify the card type (e.g. Digital Output). The handle is located at the card's outer edge and facilitates the removal and installation of the card.

1-18 OPTIONS

1-19 To obtain additional Installation and Operation Manuals when the Digtial Output card is shipped, request Option 910 when ordering the card. One additional manual will be shipped with each Option 910 ordered.

1-20 ACCESSORIES

1-21 One external connector is shipped with each I/O card. Order model 14703A when extra connectors are required to fabricate cables for several different applications.

1-22 A deinsertion tool is available to remove the contacts from the connector. This tool can be ordered from Hewlett-Packard (HP P/N 8710-0690).

SECTION II
INSTALLATION

2-1 INSPECTION

2-2 When the Digital Output card is received, inspect the card for any obvious defects that may have been incurred during shipment. Save the shipping carton and packing foam in the event that the card may have to be returned to Hewlett-Packard in the future.

2-3 Also check that the following items have been received with the Digital Output card:

- I/O card connector assembly. An instruction sheet is provided with the I/O card connector assembly and shows how to assemble the connector. This information is also available in Chapter 2 of the "6942A Multiprogrammer User's Guide". The parts list in Section V of this manual lists all the parts and the corresponding Hewlett-Packard part numbers for the connector assembly.
- Installation and Operation Manual (HP 69731-90001).
- If applicable, one or more manual change sheets may be included with the manual. If a change sheet is included, check to see if the change applies to the serial number of the card you received.

2-4 INSTALLATION PREREQUISITES

2-5 Before you install the Digital Output card in a 6942A or 6943A chassis, consider the following prerequisite steps:

a. Determine which I/O slot will be used. An I/O card can be installed in slots 0 through 15. The card assumes the address of the slot (and unit) in which it is inserted. Also, a card in slot 0 has the highest priority, slot 1 the next highest priority, and slot 15 the lowest.

b. For the slot position selected, record the following:

1. card type.
2. card's subaddress (write = 0, read = 3).
3. card's address, where;

CARD ADDRESS = SLOT. + (FRAME NO. X100) + (SUBADDRESS X 0.1)

(For example, 205.0 is the card address for a card in slot No. 5, frame number 2, referencing subaddress 0 as in a write operation.)

c. If the Digital Output card is being used to control an AC Power Controller, Model 14570A, refer to Section III for special considerations that are to be followed to assure proper operation.

2-6 AS-SHIPPED JUMPER CONNECTIONS

2-7 The Digital Output card has various jumpers that define the values of the wake-up codes, the logic level of various control signals, and the manner in which the output data lines are to be operated. The card is shipped with jumpers set to specify the values listed below:

WAKE-UP CODES:

Data Type Code = 3 (Unsigned Binary Data) jumpers W39, W41, and W43 installed.
LSB Code = 1 (Unity) jumpers W48, W49, and W50 installed.

EXTERNAL CONTROL LINES:

Trigger Polarity Select line = logic high (jumper W9 removed).
Flag Polarity Select line = logic high (jumper W21 removed).
Gate output line connected to Flag input line (jumper W10 installed).

OUTPUT DATA LINES ARE CONFIGURED AS:

Positive true logic, (Invert/$\overline{\text{Invert}}$ Gates jumper, W51 removed).
TTL logic level, (+5 V Bias jumper W16 installed).
External Bias disconnected, (jumper W15 removed).
Diode Insertion disabled, (jumper W52 removed).

NOTE

To change any of these jumpers, refer to Section III, Card Jumpers, for further details.

2-8 Once these prerequisites have been checked, you can proceed to install the card in the mainframe by performing the installation procedure in paragraph 2-9.

2-9 INSTALLATION PROCEDURE

2-10 To install the Digital Output card in the mainframe chassis, perform the following steps:

a. Turn off mainframe power.

CAUTION

To prevent an accidental short from damaging a card or a mainframe, always turn off Multiprogrammer power before installing or removing I/O cards.

b. Remove the rear cover of the mainframe by loosening the four, quarter-turn fasteners.

c. Position the card so its handle is at the bottom, and the component side of the card is toward the right.

d. Slide the card into the desired slot position until the card just touches the backplane connector.

NOTE

A notch in the card edge and a key in the connector prevent the card from being installed upside down or in an illegal slot position.

e. With the card touching the connector, rotate the card handle downward until it engages the groove at the bottom of the I/O slot. Rotate the handle upward to insert the card into the backplane connector. (To remove a card, the handle is rotated downward.)

f. Install mainframe rear cover.

g. After the card is installed, you can proceed to make a partial test of the card by performing the functional test described in the next paragraph.

2-11 FUNCTIONAL CHECKOUT

2-12 After the card is installed, the user can run either of two self tests described in the 6942A Multiprogrammer User's Guide. These tests are:

a. The Self-Test Error Detection and Card Identifier Utility Program. This test is described in Chapter 2 of the 6942A Multiprogrammer User's Guide. This test checks the card control chip and the first rank storage register.

b. Example 7-18 in Chapter 7 of the 6942A User's Guide can be run to test the programmed logic levels of the output data lines.

SECTION III
PRE-OPERATING INSTRUCTIONS

3-1 INTRODUCTION

3-2 The purpose of this section is to provide the User with additional information that may be required for any of the following reasons:

- The User wishes to change the card jumpers from their "as shipped" positions to some new positions.
- The User requires additional information on the edge connector I/O signals.
- The User intends to control an AC Power Controller, Model 14570A and wishes to know what special considerations apply.

3-3 Since any of the above reasons affect the operation of the card, the information in this Section should be read before implementing any card changes. The following topics are covered in the order mentioned:

- Definition of all card jumpers.
- Card's External Edge Connector.
- Output Data Line Driver Applications.
- External I/O Control Signals.
- AC Power Controller Considerations.

3-4 CARD JUMPERS (See Figure 3-1)

3-5 As mentioned in Section II, the Digital Output card is shipped with certain jumpers in place. When the User wishes to change a jumper(s), the information in the following paragraphs should be referenced to find the location of the applicable jumper(s) and also to see what jumper arrangements are possible. The jumpers are described in the following order:

a. Bidirectional Data Transceivers
b. External I/O Control Signal Jumpers.
c. Output Data Line Jumpers.
d. Wake-Up Code Jumpers.
e. Breadboard Jumpers and Connection Pads.

3-6 Bidirectional Data Transceivers Jumper, W38

3-7 This jumper is installed at the factory and, normally, is never removed. This jumper establishes pin 19 of tri-state integrated circuits U7 and U25 (see Figure 6-2) at ground. With pin 19 grounded the open or isolated state of the transceivers is not used. Jumper W38 is temporarily removed during fac-

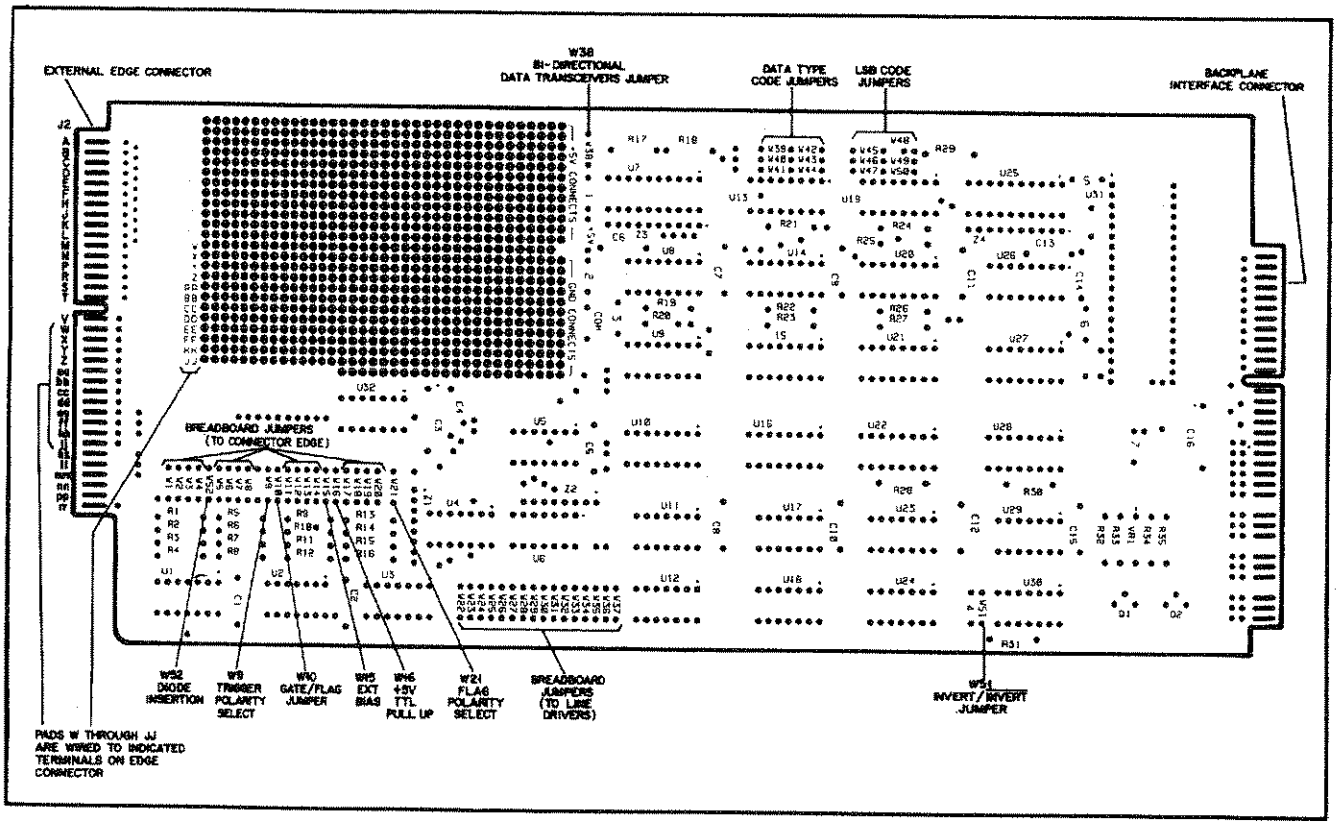


Figure 3-1. Digital Output Card, Jumper Locations

tory testing to allow the outputs of the transceivers to assume an open state for test purposes.

3-8 External I/O Control Signal Jumpers

3-9 The following paragraphs describe those jumpers that affect the control signals at the external edge connector.

3-10 **Trigger Polarity Select Jumper, W9.** This jumper is removed prior to shipment making the Trigger Polarity Select (TPS) control line a logic high. If this jumper is installed, the TPS control line is held at a logic low level. The purpose of the Trigger Polarity Select signal is discussed in Table 3-3.

3-11 **Flag Polarity Select Jumper, W21.** This jumper is removed prior to shipment making the Flag Polarity Select (FPS) control line a logic high. If this jumper is installed, FPS is held at a logic low level. The purpose of this control signal is discussed in Table 3-3.

3-12 **Gate/Flag Jumper, W10.** This jumper is installed when the card is shipped. With this jumper installed, the GATE control signal is connected directly to the FLAG control line. This jumper can be removed by the customer if external handshaking is desired. Further information is given in Table 3-3.

3-13 Output Data Line Jumpers (See Figure 3-2)

3-14 The following paragraphs explain those jumpers that affect the operation of the output data lines. Figure 3-2 is a simplified schematic showing these jumers and the driver logic for a typical data line (B0 in this example). The jumpers are shown as the card is shipped from the factory.

3-15 **Invert/$\overline{\text{Invert}}$ Gates Jumper, W51.** This jumper is installed at the factory when the card is shipped as part of Option 042 (used with AC Power Controller, Model 14570A). Otherwise, jumper W51 is removed at the factory. When this jumper is installed, the logic sense of all 16-data lines is inverted to negative true.

3-16 **+5 V TTL/CMOS Pull-Up Resistor Jumper, W16.** This jumper is installed when the card is shipped. It connects all pull-up resistors to the +5 V supply voltage.

NOTE

If some output lines are to be wired as open collector, the applicable pull-up resistor must be removed.

3-17 **Diode Insertion Jumper, W52.** This jumper is removed when the card is shipped. If this jumper is installed, diodes internal to the line driver integrated circuits; U1, U2, U3, U32 are connected in parallel with the output pull-up resistor.

3-18 **External Bias Jumper, W15.** This jumper is not installed when the card is shipped. When a bias voltage greater than 5 V is required, jumper W16 is removed and jumper W15 is installed. With W15 installed all pull-up resistors are connected to the EXT BIAS voltage (at pin V) except for those lines whose pull-up resistors have been removed.

NOTE

Jumpers W15 and W16 should never be installed at the same time.

3-19 WAKE-UP CODE JUMPERS

3-20 These jumpers determine the data type and LSB wake-up codes that are read from the card and stored in memory after power turn on. The user can override the values stored in memory by using a Set Format (SF) instruction. This is useful in applications that require a data format code or LSB

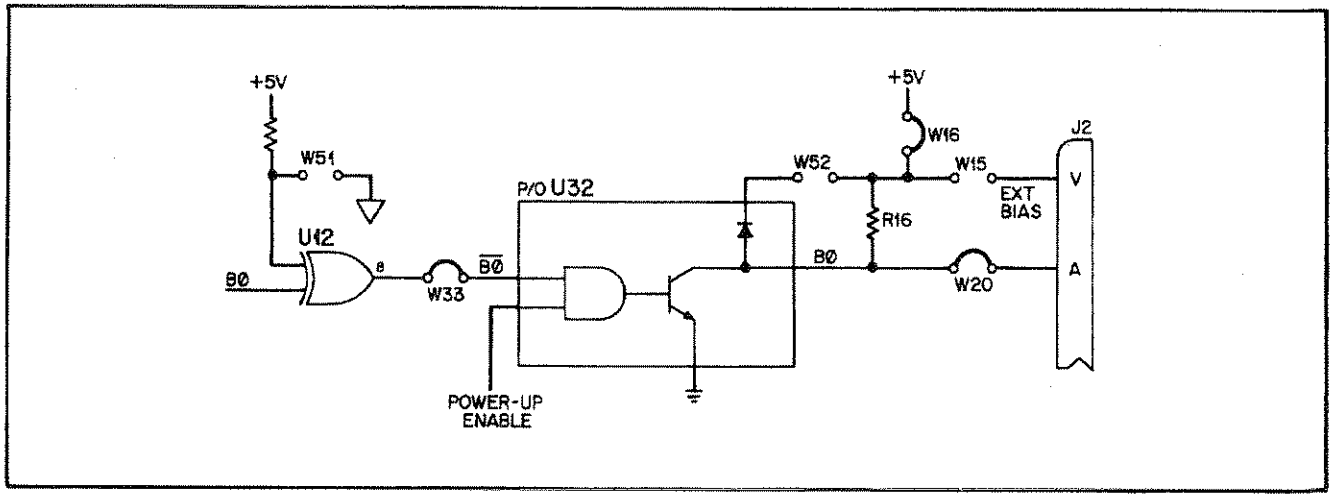


Figure 3-2. Output Data Line Jumpers (As Shipped Configuration)

value different from the values set at the factory. Any of the data types of Table 3-1 can be used. Programmed LSB values are not limited to those in Table 3-2. Any desired LSB value between 0.001 and 65.535 can be programmed. This allows the user to express programmed data in units appropriate to the process to which the card is dedicated.

3-21 If a new Data Type or LSB code will always be used, the jumpers on the card can be changed to reflect these new codes. This is more efficient than having the software constantly override the factory set values.

3-22 Data Type Code Jumpers, W39 through W44. These jumpers specify the data type code sent to the Multiprogrammer as part of the wake-up code sequence. The Digital Output card is shipped with jumpers W39, W41, and W43 installed and, jumpers W40, W42, and W44 removed. The Multiprogrammer interprets these jumpers as data type code = 3 meaning an unsigned binary number.

3-23 These jumpers can be changed to specify a different data type code. For example, data type code = 7 could be selected to program a bit pattern in octal form. Table 3-1 shows which jumpers must be in and which jumpers must be removed to select other data type codes.

3-24 LSB Code Jumpers, W45 through W50. The Digital Output card is shipped with LSB Code jumpers, W48, W49, and W50 installed and W45, W46 and W47 removed. These jumpers specify a LSB code 1 (unity). Table 3-2 shows the other valid LSB Codes and required jumpers.

Table 3-1. Data Type Code Jumpers

DATA TYPE CODE	DESCRIPTION	JUMPER ARRANGEMENT					
		W8	W7	W6	W5	W4	W3
1	Programmed positive or negative number is stored on card in two's complement form.	Out	Out	Out	In	In	In
2	Programmed positive or negative number is stored on the card in sign-magnitude form.	Out	Out	In	In	In	Out
3*	Programmed positive or negative number is stored Stored on card in unsigned binary form.	Out	In	Out	In	Out	In
4	(Special autorange code used only with 69736A Timer/Pacer Card).						
6	Programmed positive number is stored on card in unsigned BCD form.	In	Out	In	Out	In	Out
7	Programmed octal integer is stored on card in unsigned binary form.	In	In	Out	Out	Out	In

*When the card is shipped, its jumpers are arranged to select the starred data type when power is applied to the system.

Table 3-2. LSB Code Jumpers

LSB CODE	LSB VALUE	JUMPER ARRANGEMENT					
		W50	W49	W48	W47	W46	W45
0	0.001	Out	Out	Out	In	In	In
1	0.025	Out	Out	In	In	In	Out
2	0.1	Out	In	Out	In	Out	In
3	0.5	Out	In	In	In	Out	Out
4	0.01	In	Out	Out	Out	In	In
5	0.05	In	Out	In	Out	In	Out
6	0.005	In	In	Out	Out	Out	In
7*	1.0	In	In	In	Out	Out	Out

*When the card is shipped, its jumpers are arranged to select the starred LSB value when power is applied to the system.

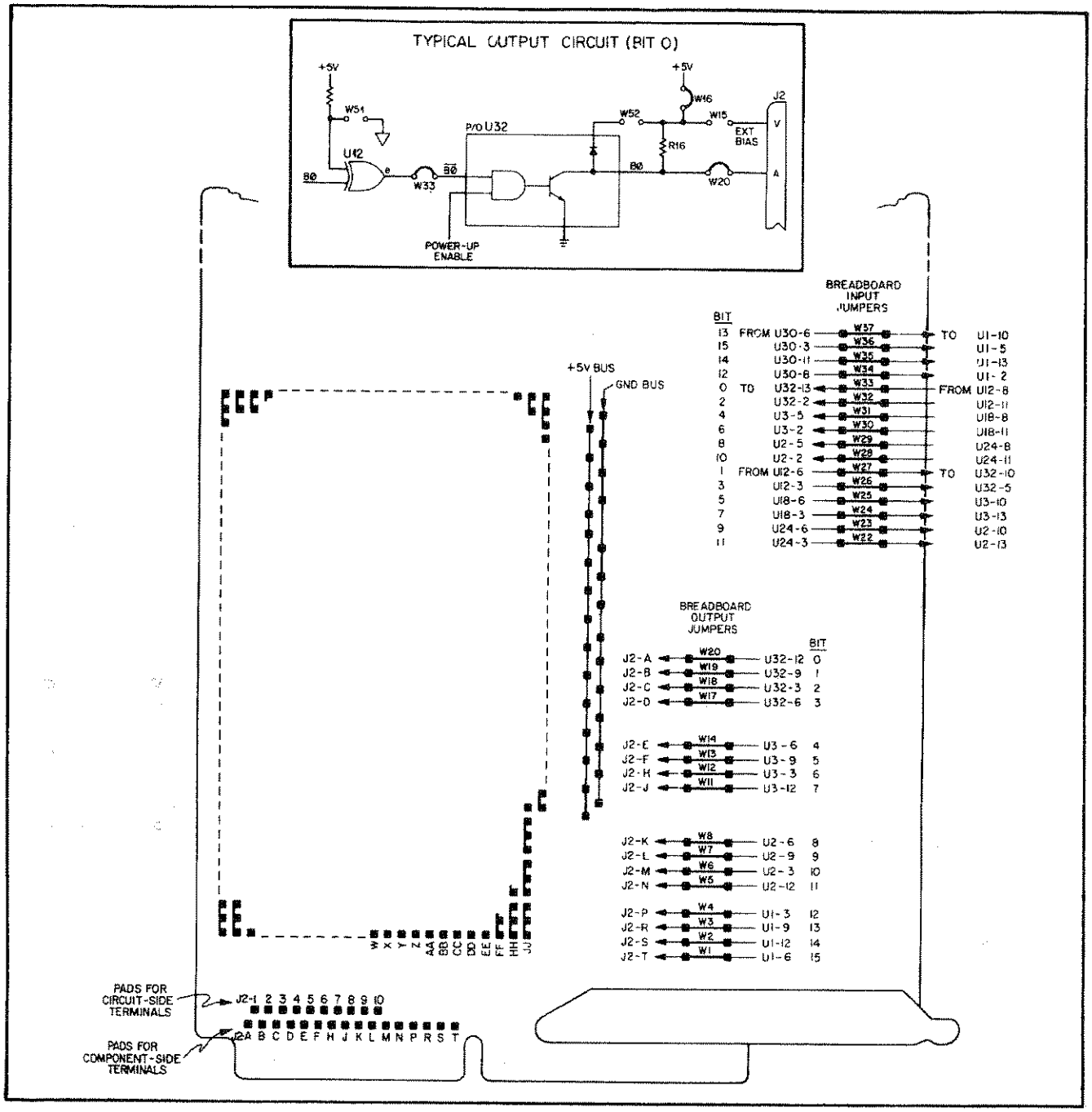


Figure 3-3. Digital Output Card, Breadboard Circuit Connections

3-25 Breadboard Jumpers and Connection Pads

3-26 The Digital Output card contains an area of drilled and plated-through printed circuit pads for breadboarding custom output circuits. Figure 3-3 shows the circuit connections that have been provided on the card.

3-27 Interconnections can be made between the breadboard logic and the output data lines by removing the appropriate jumpers that are in series with the data lines and then adding the necessary wire runs. For example, to connect output data line B0 to the breadboard logic, jumper W20 (Figure 3-2) would be removed so connections can be made to and from the jumper pads.

3-28 The invert gates (U12, 18, 24, and 30) are low-power Schottky TTL devices, type SN74LS86N. The card's output buffers (U1, U2, U3 and U32) are TTL nand drivers with high-voltage open-collector outputs. They can sink 100 milliamps at collector voltages up to 40 volts.

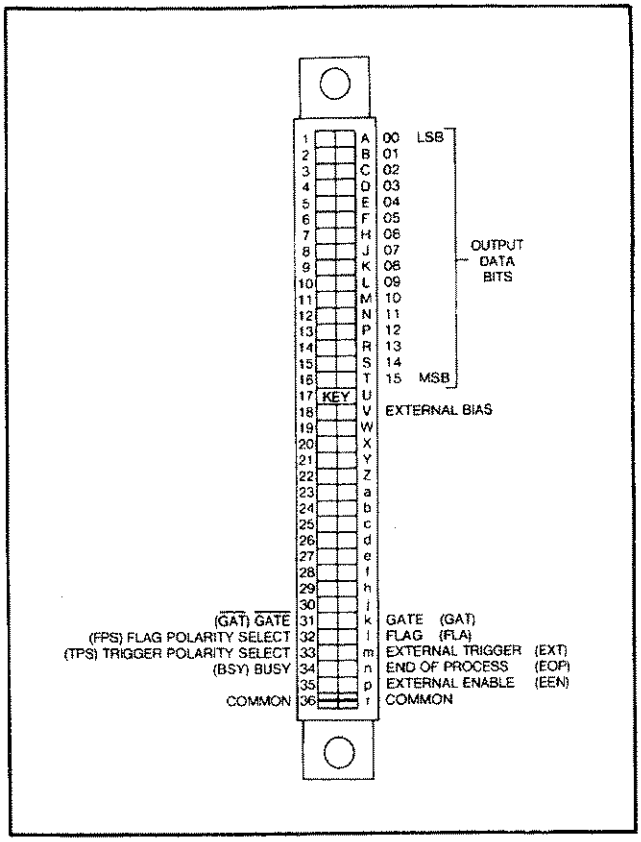


Figure 3-4. Digital Output Card, External Edge Connector

3-29 CARD'S EXTERNAL EDGE CONNECTOR

3-30 One dual 36-pin edge connector is supplied with each I/O card for interfacing field wiring to the card. Instructions for making up the mating connector and hood assembly are provided in Chapter 2 of the 6942A User's Guide. The pin assignments of the I/O signals available at the card's external edge connector are shown in Figure 3-4. (The lettered pins correspond to the component side of the card.)

3-31 OUTPUT DATA LINE DRIVER APPLICATIONS

3-32 The card's output data lines can be used to supply TTL or CMOS logic levels, or to drive small relays or lamps. Figure 3-5 shows several circuits each using a different combination of data line jumpers to achieve the desired application. The circuits are labelled (a) through (c):

a. A relay driver circuit using 28 Vdc to operate the relay. The 28 Vdc connects to the card via jumper W15. A diode shunts the relay coil since jumper W52 is installed. Pull-up resistor R16 is disconnected.

b. A CMOS compatible logic line where a 15 VDC bias is used in place of the +5 Vdc local pull-up resistor.

c. A lamp driver circuit where a 6 Vdc voltage is required by the lamp. The output line is operating as open collector. Resistor R16 is removed entirely from the card. Other output lines are still connected to the +5 Vdc pull-up bus.

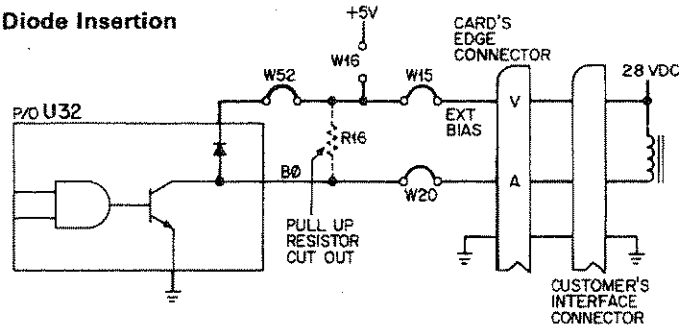
3-33 EXTERNAL I/O CONTROL SIGNALS (Figure 3-6)

3-34 Table 3-3 describes the control signals which interface between the Digital Output card and the Customer's equipment. The electrical specifications for these signals are given in Table 1-1 of Section I.
The pin numbers given in Table 3-3 correspond to those on the I/O Edge Connector shown in Figure 3-4.

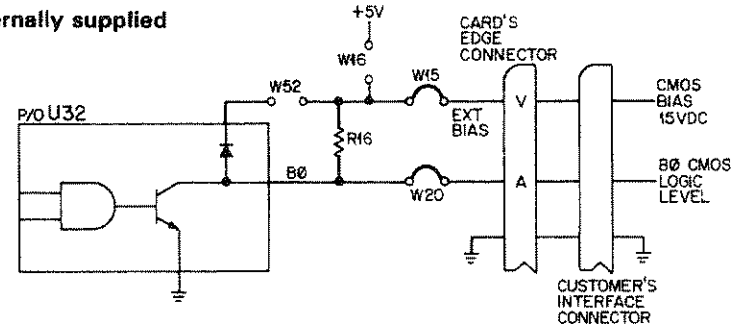
3-35 INTERFACING TO AN AC POWER CONTROLLER

3-36 When the Digital Output card is used to control an AC Power Controller, Model 14570A, install jumper W51. This jumper is required since the AC Power Controller input lines are activated by negative true logic levels. When installed jumper W51 inverts the logic sense of all output data lines. If this card is shipped as part of Option 042 (Model 14570A), jumper W51 is installed at the factory.

(a) Relay Driver with Diode Insertion



(b) CMOS BIAS Externally supplied



(c) Lamp Driver Using Open Collector (Pull-Up Resistor Removed)

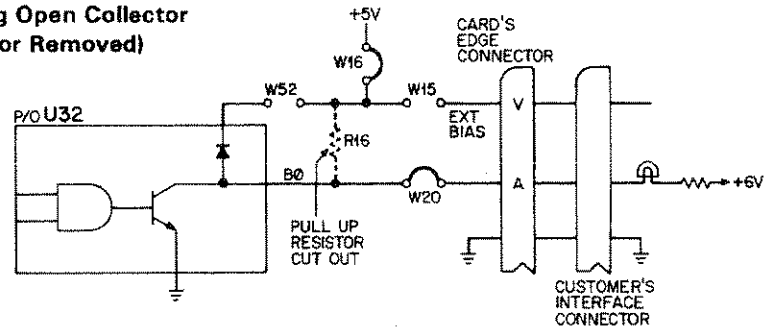


Figure 3-5. Typical Output Data Line, Driver Applications

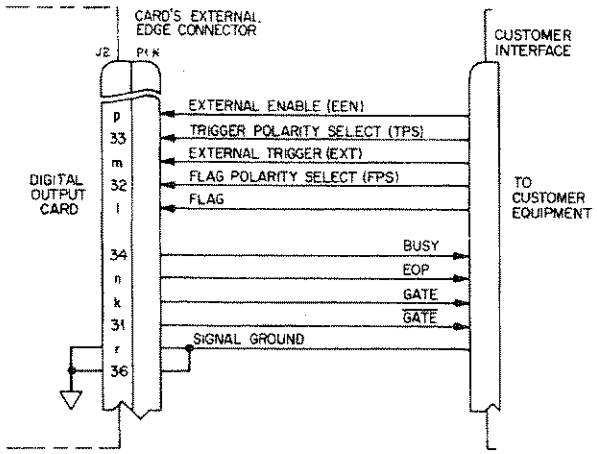


Figure 3-6. External I/O Control Signals

Table 3-3. Card's External I/O Control Signals

I/O Control Signal	Pin No.	TTL Level	
EXTERNAL ENABLE also EEN (card input)	p	High	With pin p at a logic high, the output data lines are connected to second rank storage when the card is cycled provided the System Enable, SYE, line is high.
		Low	If pin p is made low, the output data lines immediately go to the logic low state (or logic high if jumper W51 is installed).
TRIGGER POLARITY SELECT also TPS(card input).	33	High	With TPS high, a low-to-high transition of the EXTERNAL TRIGGER line cycles the card.
		Low	If pin 33 is made low (or jumper W9 is installed), a high-to-low transition of the EXTERNAL TRIGGER line cycles the card.
EXTERNAL TRIGGER also EXT (Card input)	m	edge sensitive trigger	This signal can be used to cycle the card externally for example, after a Write First (WF) rank instruction is issued at the controller. The TRIGGER POLARITY SELECT line determines the triggering edge.
BUSY (card output) also BSY	34	High	Busy goes high when the card is cycled either by an instruction or externally by the EXTERNAL TRIGGER line. While BUSY is high, the output data lines are being selected.
		Low	Busy goes low when GATE goes high (unless jumper W10 is removed).
FLAG POLARITY SELECT also FPS (Card Input)	32	High	With pin 32 high a low-to-high transition of the FLAG control signal is required to clear BUSY and set EOP.
		Low	If jumper W21 is installed, or if a low logic level is applied to pin 32, a high-to-low transition of the FLAG control signal is required to set EOP and clear Busy.
FLAG (Card Input)	l	Edge sensitive trigger	A low-to-high or high-to-low edge (determined by FPS) sets EOP and clears the GATE and BUSY control lines.
GATE (Card Output) also GAT	k	High	Goes high when the card is cycled and indicates that the output data lines have valid data.
		Low	Goes low when the FLAG signal is received.
$\overline{\text{GATE}}$ (Card Output) also $\overline{\text{GAT}}$	31		Logical inverse of GATE signal at pin k.
END-OF-PROCESS also EOP (Card Output)	n	High	Goes high when Busy goes low. EOP remains high for a minimum of 2μs and stays high for a time dependent on the program. Pin n going high can be used as an indication that the operation is completed.
		Low	EOP is set low by the Multiprogrammer in response to an interrupt request.
COMMON	r 36		Signal return for all control signals and data lines.

SECTION IV
THEORY OF OPERATION

4-1 INTRODUCTION

4-2 This section explains the theory of operation for the Digital Output card. The theory assumes that the reader is familiar with the instruction set and the basic operation of the 6942A Multiprogrammer. First, a brief description is given covering the basic operation and features of the card. A detailed block diagram discussion then follows. This section concludes with an example of the processing of an output bit instruction.

4-3 OVERALL OPERATION

4-4 Power Turn-On

4-5 When power is applied to the Digital Output card, the circuits on the card are first cleared. A power-up delay circuit holds the 16-output data lines at logic low (or logic high if jumper W51 is installed) until +5 V is reached (within a few milliseconds). A self-test is then initiated by the Multiprogrammer to test the circuits of the Digital Output card. The self-ID, data type, size, and LSB parameters of the card are read and stored in Multiprogrammer memory as part of the wake-up sequence.

4-6 First Rank Storage

4-7 When the Digital Output card is addressed in any output type instruction (OP, OS, OB, OI, WC, or WF), a 16-bit data word is sent to the card and is stored in a register called first rank storage. The data word in first rank storage can be read at any time with a Read Value (RV) instruction. If a WF output instruction were issued at the controller, this instruction would be completed with the loading of first rank storage. For any other output instruction, a "cycle" operation (described in the next paragraph) begins shortly after the data word is loaded into first rank storage.

4-8 Cycling The Card

4-9 In a cycle operation, the 16-bit data word in first rank storage is transferred to a second register called second rank storage. Immediately after this transfer, several events take place simultaneously as part of the cycling operation:

a. A CARD ENABLE signal goes high (if not already high from a previous cycle) and allows the data word in second rank storage to select the data lines. A "1" (or high) in any bit position of the data word in second rank storage makes the data line associated with that bit position a logic high. A "0" (or low) in any bit position makes the data line a logic low. The data lines remain at the selected logic levels until: (1) they are re-programmed, (2) a power-up reset occurs, (3) a Sytem Disable (SD) instruction is issued, or (4) the External Enable line at the edge connector is made low.

b. BUSY and GATE signals go high and are sent to the external edge connector. BUSY indicates that the data lines are currently being selected. GATE is an ancillary signal that can be used by the external logic to trigger a read data-lines operation

4-10 As mentioned previously, a cycle operation occurs automatically for all output instructions except a WF instruction. With a WF instruction, the cycle operation is normally initiated in one of two ways. (See Figure 4-1):

1. By the controller by issuing a Cycle (CY) instruction to specifically cycle the card, or
2. Externally at the external interface connector by appling an EXTERNAL TRIGGER signal. When an External Trigger is applied, an additional signal called TRIGGER POLARITY SELECT determines whether cycling will occur on the low-to-high or high-to-low transition of the External Trigger pulse.

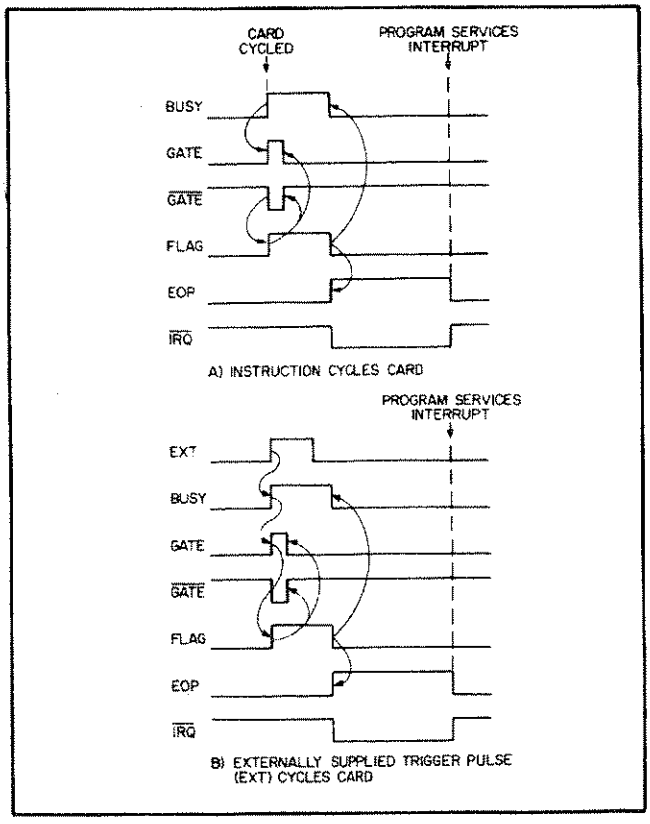


Figure 4-1. Card Cycling and BUSY/EOP Timing

4-11 Gate/Flag Handshake

4-12 When the GATE signal is sent to the edge connector. A FLAG signal is immediately returned via jumper W10 and indicates that the operation is completed. If jumper W10 is removed, the FLAG control signal must be returned by the customer's external logic.

4-13 End-Of-Process

4-14 An End-Of-Process (EOP) signal is generated when the FLAG control signal is received. The EOP signal is sent to the external interface connector and indicates that the operation is completed.

4-15 Interrupt Request

4-16 When the EOP signal occurs, an Interrupt Request (IRQ) is returned to the Multiprogrammer to indicate the completion of the operation provided the card was armed. OB, OI, OP, and OS output instructions arm the card when the first rank storage register is loaded. For WF, WC and CY instructions, the card must be armed before an interrupt can be generated. An Arm Card (AC) instruction issued at the controller can be used to arm the card prior to cycling the card. After a program interrupt request is made, the Multiprogrammer will respond by disarming the card, clearing EOP and the group address flag (GAFF).

4-17 The GAFF flag is internal to the Universal control Chip on the card and is set by instructions, such as; WC, OS, OP, to allow multiple cards to be cycled in parallel (or simultaneously). Refer to Chapter 4 in the 6942A Multiprogrammer User's Guide for more information on cycling cards in parallel.

4-18 Data-Lines Quick-Disconnect

4-19 This feature permits either the Controller or the customer logic to place all data output lines in a logic low state. The Controller can do this by issuing a System Disable (SD) instruction which forces Card Enable low. The external logic can do this by making the External Enable signal low.

4-20 Self-ID/Status Word

4-21 When the Multiprogrammer performs a self test, or when the controller issues a Read Status (RS) instruction, the Digital Output card returns a 16-bit status word to the Multiprogrammer. This word contains information on the operational status of the card and shows how the card is hardware configured. The status word is discussed in more detail in the detailed block diagram discussion.

4-22 DETAILED BLOCK DIAGRAM DISCUSSION (FIGURE 4-2)

4-23 The Digital Output card consists of the following functional circuits:

a. Universal control chip (UCC).
b. Tri-state bidirectional data transceivers.
c. First rank storage register.
d. Second rank storage register.
e. Output enable gates.
f. Invert/$\overline{\text{invert}}$ gates.
g. Nand gate line drivers.
h. Power-up delay monitor circuit.
i. First rank return buffers.
j. Self-ID/status return buffers.

4-24 When the Digital Output card is installed in a slot position in the Multiprogrammer, 6942A, or in the Extender chassis, 6943A, the card is assigned the address of that slot position. Once installed, the card connects to the data lines, B0-B15, to the control lines, and to the power input lines of the backplane.

4-25 The following paragraphs describe the functional circuits shown in Figure 4-2. The functional schematic in Section VI should also be referenced.

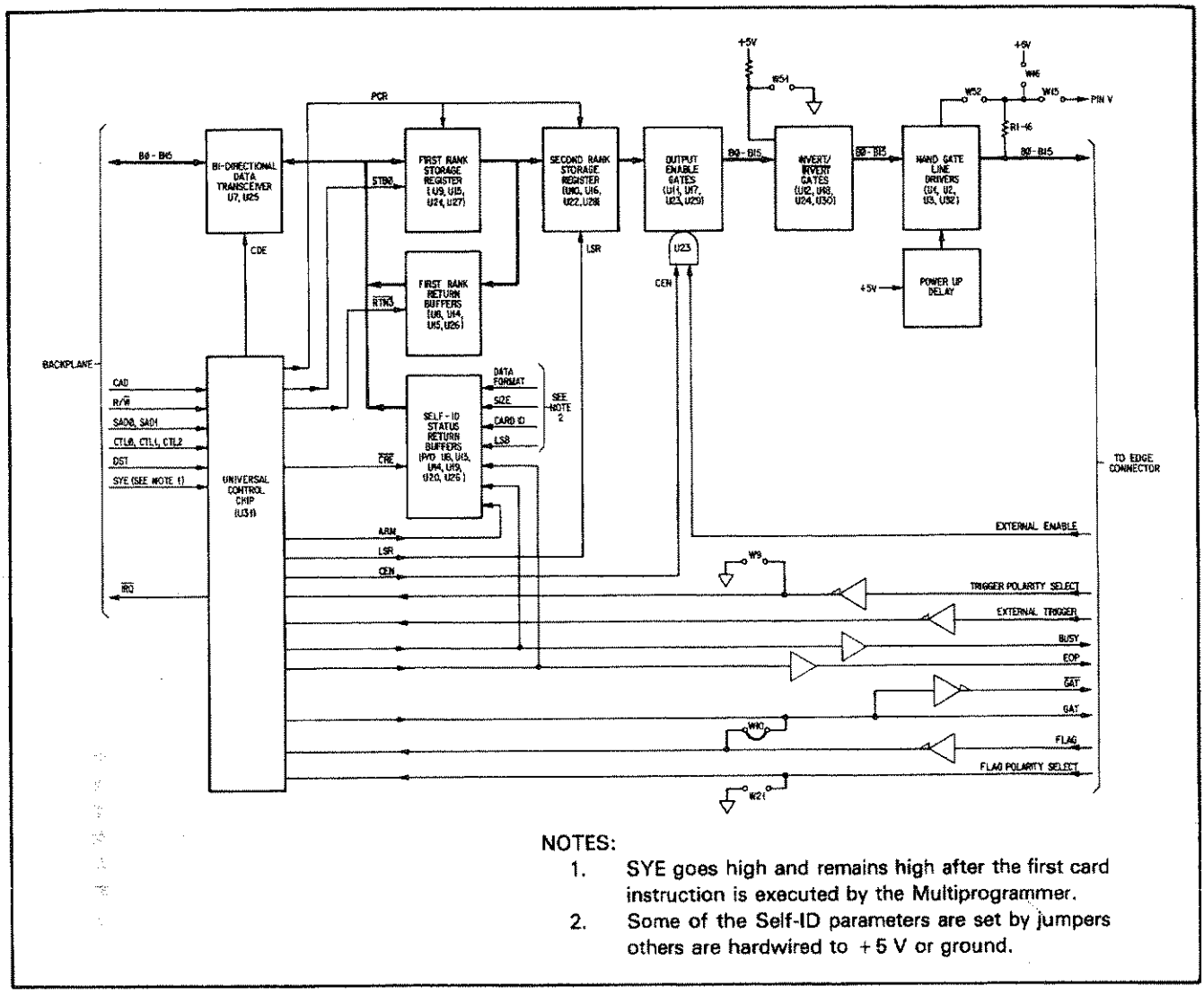
4-26 Universal Control Chip (UCC)

4-27 This control chip (U24) supervises all the operations taking place on the Digital Output card. The UCC establishes the timing sequence for the various control signals used on the card.

4-28 When power is applied to the card, the PCR control signal goes high and clears all circuits on the card. The card is then ready to process any instruction issued at the controller that addresses the card. When an instruction is issued, the following input control lines set up the UCC for a particular operation:

CAD	-	This is the card address lines which goes high to select the Digital Output card when the card is addressed in an instruction.
R/$\overline{\text{W}}$	-	This is the read/write line. It is high for a read first rank operation and is low for a write operation.
SAD0,SAD1	-	These two lines supply a subaddress to the card. For a read data operation, subaddress 3 (binary 11) is sent. For a write operation, subaddress 0 (binary 00) is sent.
CTL0, CTL1, CTL2	-	These lines supply a 3-bit control code to the UCC to indicate what operation is to be performed. Depending on the instruction issued, one or more codes are sent in succession.

4-29 The data values on the above control lines are loaded into the UCC when a data strobe (DST) pulse occurs. The control lines are then decoded to produce the various control signal outputs required for the indicated operation. A description of these control signals as they relate to the function being performed is included in the following paragraphs.



NOTES:

1. SYE goes high and remains high after the first card instruction is executed by the Multiprogrammer.
2. Some of the Self-ID parameters are set by jumpers others are hardwired to +5 V or ground.

Figure 4-2. Digital Output Card, Detailed Block Diagram

4-30 Tri-State Bidirectional Data Transceivers

4-31 The tri-state bidirectional transceivers control the direction of data flow to and from the card over the B0-B15 data lines. A CDE control signal is used to switch the direction of the data lines. During a write operation, control signal, CDE, is low and the B0-B15 data lines are connected to the input of the first rank storage register. During a read operation, CDE goes high and the B0-B15 data lines are connected to the output of the first rank return buffer and to the output of the self-ID/status return buffer. Although the transceivers are tri-state logic, jumper W1 establishes pin 19 at ground so that the isolated or open state condition is never used.

4-32 First Rank Storage Register

4-33 When any output instruction is executed, a data word is placed on the B0-B15 data lines to the first rank storage register. Subaddress 0 (Write) is decoded from the SAD0, SAD1 lines to produce a STB0 pulse. The leading edge of STB0 loads the first rank storage register with the data on the B0-B15 lines. The data word stored in first rank storage can be read at any time with a Read Value (RV) instruction. The first rank storage register is cleared only on power turn on.

4-34 Second Rank Storage Register

4-35 This register is loaded with the data word from the first rank storage register only when a cycle operation is initiated. A cycle operation occurs automatically as part of any output instruction except for a WF output instruction. After STB0 goes high, the Multiprogrammer sends another control code to initiate a cycle operation. An LSR strobe pulse is produced to begin the cycle sequence. The leading edge of LSR loads the second rank storage register. Second Rank Storage is cleared only on power turn on.

4-36 Output Enable Gates

4-37 These gates have two purposes: first, they prevent

the data lines from being selected until the programmed data word is loaded into second rank storage (cycled) and the External Enable signal is high. Second, these gates can disconnect the data output lines from second rank storage when either the CARD ENABLE (CEN) or the EXTERNAL ENABLE signal goes low. CEN goes high with the first cycle card operation and remains high unless an System Disable (SD) instruction is issued to make SYE low, or a power reset occurs.

4-38 Invert/$\overline{\text{Invert}}$ Gates

4-39 These are exclusive or gates which invert the logic levels on the B0-B15 data lines. When jumper W51 is installed no inversion takes place.

4-40 Nand Gate Line Drivers

4-41 These gates have three purposes:

a. During Power-Turn-On, these gates hold the output lines low (or high if jumper W51 is installed) until the +5 V supply voltage has reached a TTL logic threshold voltage.

b. Provide up to 100 mA drive current for the data output lines at up to 30 Vdc collector voltage.

c. When jumper W52 is installed, diodes internal to these circuits are connected in parallel with each output pull-up resistor.

4-42 Power-Up Monitor Circuit

4-43 This circuit monitors the +5 V supply voltage on power turn on. The Nand GATE Line Driver outputs are held at a logic low level until +5 V is reached.

4-44 First Rank Return Buffers

4-45 These buffers are used to place the contents of the first rank storage register on the B0-B15 data lines. When a Read Value, (RV) instruction is issued, subaddress 3 is decoded from the SAD0, SAD1 lines to produce a low $\overline{\text{RTN3}}$ logic level. This control signal enables the tri-state output of the first rank return buffers. CDE is also high and the data word in first rank storage is sent to the Multiprogrammer via the first rank return buffers.

4-46 Self-ID/Status Return Buffers

4-47 These buffers are also tri-state and their outputs are held in an open or isolated condition while the $\overline{\text{CRE}}$ control line is high. When a self-ID status operation is decoded from the control lines, $\overline{\text{CRE}}$ goes low and $\overline{\text{RTN3}}$ is high. This connects the inputs of the self-ID status return buffers to the B0-B15 data lines. The self-ID/status word sent to the Multiprogrammer is shown below.

4-48 The 16-bits (B0-B15) are readback during self test or when an RS instruction is programmed. During self-test, bits B3-B15 are stored in the Multiprogrammer memory while status bits B0-B2 are ignored. When a Read Status (RS) instruction is issued, status bits B3-B15 are ignored.

4-49 The self-ID bits, B3-B15, specify the "wake-up" values of the LSB, card ID, size, and data-type parameters. The values of the parameters determine how the Multiprogrammer firmware will process the data it sends to or receives from the card. Status bits, B0-B2, are used by the Multiprogrammer to check the status of the card during operation. The status information is provided by UCC outputs, ARM, BSY, and EOP.

4-50 PROCESSING AN OUTPUT BIT (OB) INSTRUCTION

4-51 This discussion explains the processing of a typical output type instruction. Assume that an Output Bit (OB) instruction is issued at the controller which addresses the Digital Ouptut card in slot 1. Assume that data lines B0, B5, and B7, are to be set high while the remaining data lines are to be left unchanged. The format of the Controller instruction is...

"OB,1,0,1,5,1,7,1T"

4-52 When this instruction is executed, the following operations occur in the sequence indicated:

a. Addressing the Digital Output card - the slot position specified by the OB instruction is decoded and the CAD line to the Digital Output card goes high and selects the card in slot 1. In addition, the R/$\overline{\text{W}}$ line, SAD0, SAD1 lines, and the three-bit, control-code lines are decoded.

LSB	CARD IDENTIFICATION	SIZE	DATA	ARM	BUSY	EOP
15-13	12-7	6	5-3	2	1	0
jumpers set this field to 111 which corresponds to unity.	Hardwired to binary code of 101010 which corresponds to an ID of decimal 42.	Hardwired to binary 1 which signifies a 16-bit data word.	jumpers set this field to 010 which is incremented to 3 by the program (unsigned binary).	These are one bit flags where 1 = true 0 = false		

b. Reading First Rank Storage - CDE goes high and $\overline{RTN3}$ goes low. The content of the first rank storage register is placed on the B0-B15 lines to the Multiprogrammer. The Multiprogrammer reads this data word so that any data lines which were previously high will remain high in addition to those data lines which the OB instruction commands to go high.

c. Loading First Rank Storage - next, a 16-bit data word with 1's in bit positions 0,5,7, and any other bit position that contained a "1" from the previous read is placed on the B0-B15 data lines to the first rank storage register. CDE is low, the R/$\overline{W}$ line is low, and the subaddress lines SAD0 and SAD1 are zero. Decoding these lines results in the STB0 strobe pulse going high and first rank storage is loaded with the 16-bit data word. The arm control line is also set high at this time.

d. Cycling the card - shortly after STB0, the Multiprogrammer sends another control code to initiate a cycle operation. An LSR strobe pulse occurs and transfers the data from first rank storage to second rank storage. BUSY, GATE, and CEN go high and data lines B0, B5, and B7 go high (provided EXTERNAL ENABLE and SYE are also high). Those data lines that were previously high will also be high.

e. End-of-Process and Interrupt Request - When Busy goes high, the Flag signal also goes high. EOP goes high and BUSY goes low. Since ARM is also high, an program interrupt request ($\overline{IRQ}$) is sent to the Multiprogrammer.

f. Clearing the UCC - After the program services the interrupt request, a clear control code is returned. The storage registers are not affected, but the ARM, EOP, and GAFF lines are cleared.

SECTION V
PARTS LIST

5-1 INTRODUCTION

5-2 This section contains information on ordering replacement parts for the Digital Output card Model 69731B. Table 5-1 lists the electrical and mechanical components of the card. Table 5-2 lists the parts comprising the external I/O connector assembly supplied with the card. Figure 5-1 illustrates how the parts in Table 5-2 are assembled.

5-3 HOW TO ORDER PARTS

5-4 You can order parts from your local Hewlett-Packard sales office. Refer to the list of sales offices at the end of this manual for the office nearest you. When ordering parts include the following information:

a. the Hewlett-Packard part number.
b. a description of the part.
c. the quantity desired.
d. the model number of the card (69731B) on which the part is used.

5-5 If you wish to order a part directly from the manufacturer, locate the manufacturer's supply code in Table 5-1 and use this code to find the manufacturer's address in Table 5-3.

Table 5-1. Digital Output Card, Model 69731B, Parts List

Ref. Desig.	HP Part No.	Qty	Description	Mfr. Code	Mfr. Part No.
C1, C2 C4-C15	0160-4722	14	Capacitor, ceramic 0.1μf +80 −20%, 50 Vdc	28480	
C3, C16	0180-0291	2	Capacitor, tantalum 1.0μf 10%, 35 Vdc	56289	150D105X9035A2
Q1, Q2	1854-0823	2	Transistor, NPN Silicon	28480	
R1-R16 R18 R21-R27 R29, R31	0683-5125	26	Resistor, 5.1k 5% 0.25 watt	01121	CB5125
R17	0683-1035	1	Resistor, 10k, 5% 0.25 W	01121	CB1035
R32, R33	0683-1025	2	Resistor, 1K ohms, 5% 0.25 W	01121	CB1025
R34	0683-4705	1	Resistor, 47Ω 5% 0.25 W	01121	CB4705
R35	0683-2015	1	Resistor, 200Ω 5% 0.25W	01121	CB2015
U1-U3 U32	1820-2129	4	IC Line Driver, Quad	56289	UHP-407
U4	1820-1416	1	IC Hex Schmitt Trigger Inverters	01295	SN74LS14N
U5	1820-1197	1	IC Quad 2-input positive nand gate	01295	SN74LS00N
U6	1820-1200	1	IC Hex Inverter - Open	01295	SN74LS05N
U7, U25	1820-2075	2	IC Octal Bus Transceiver Tri-state output	01295	SN74LS245N
U8, U13 U14, U19 U20, U26	1820-2257	6	IC Hex Non-Inverting	0471	MC14503BCP
U9, U10 U15, U16 U21, U22 U27, U28	1820-1544	8	IC CMOS 4-bit D-type	04713	MC14076BCL
U11, U17 U23, U29	1820-1201	4	IC quad 2-input positive and gate	01295	SN74LS08N
U12, U18 U24, U30	1820-1211	4	IC Quad 2-input exclusive or gates	01295	SN74LS86N
U31	1820-2302	1	IC Card Control Chip	28480	
VR1	1902-0062	1	Diode Zener, 3.74 V	28480	
X31	1200-0552	1	Socket, IC, 40 pin	28480	
Z1	1810-0206	1	Network, Resistor	01121	208A103
Z2	1810-0205	1	Network, Resistor	01121	208A472
Z3, Z4	1810-0280	2	Network, Resistor	01121	210A103

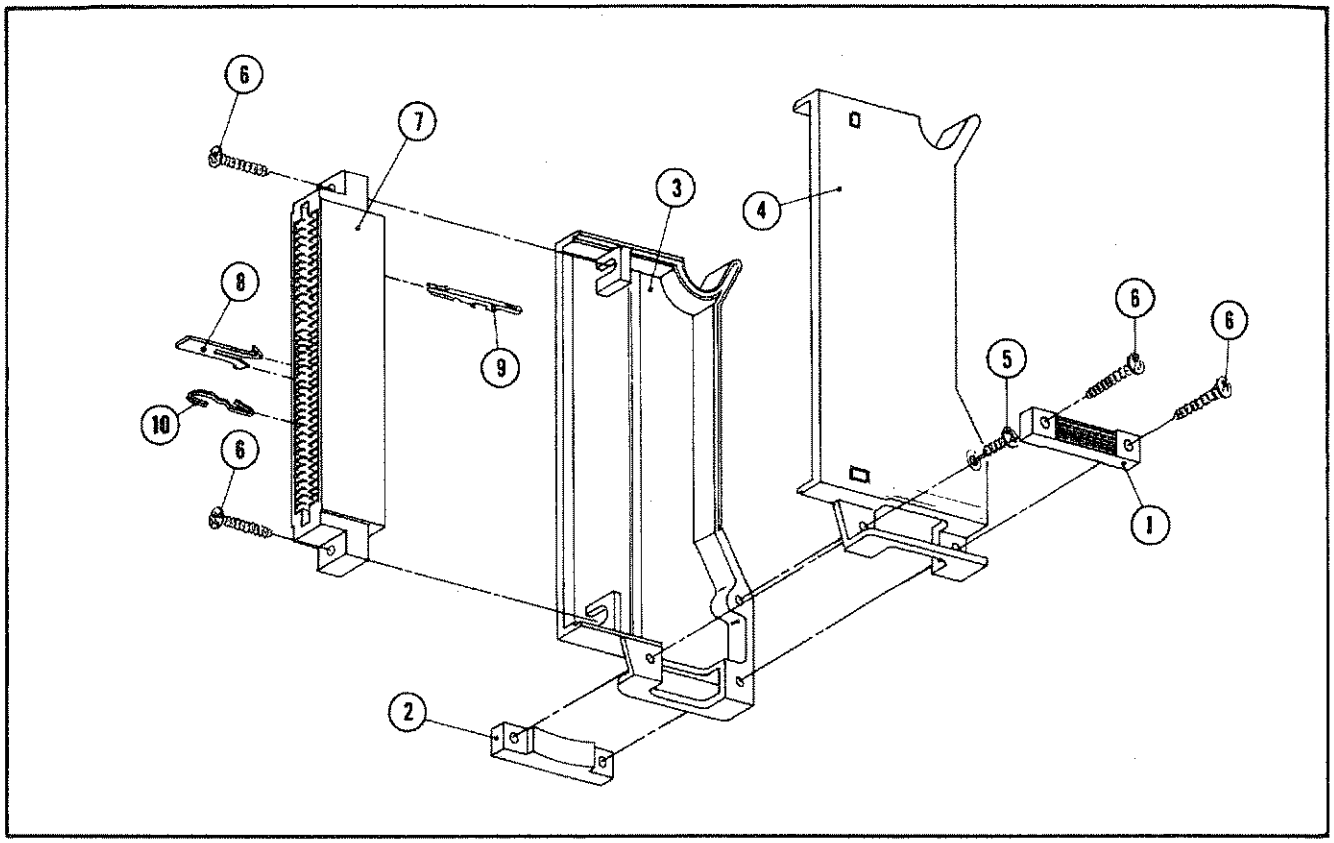


Figure 5-1. Connector Assembly, (HP, P/N 50600-28069 Exploded View

Table 5-2. Parts List for External Connector Assembly*
(HP Part No. 5060-2806)

HP Part No.	Index No.	Description	Qty.
1251-6307		Hood Assembly**	
	1	. . Strain relief	
	2	. . Cable clamps	
	3	. . Right hood assy.	
	4	. . Left hood assy.	
	5	. . Screw, 7/16 inch.	
	6	. . Screws, 11/16 inch.	
121-6059	7	Connector Pin Housing	1
1251-6056	8	Connector Key	1
1251-6183	9	Solder Pins, plated	45
1251-6380	10	Springs retaining	6

* Can be ordered as Model 14703A, Card Edge Connector
** Item 1251-6307 consists of index items 1 through 6.

Table 5-3. Manufacturer's Federal Supply Codes

Code	Manufacturer	Address
01121	Allen Bradley Co.	Milwaukee, Wis.
01295	Texas Instruments, Inc. Semiconductor-Components Division	Dallas, Texas
04713	Motorola Semiconductor Products Inc.	Phoenix, Arizona
14908	Electronic instruments and Specialty Corp.	Stonham, Ma
16299	Corning Glass Works, Electronic Component Division	Bradford, Pa.
27014	National Semiconductor Corp.	Santa Clara. Calif.
28480	Hewlett-Packard Co.	Palto Alto, Calif.
56289	Sprague Electric Co.	North Adams, Ma