EM78612

Universal Serial Bus Microcontroller

Product Specification

DOC. VERSION 1.0

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Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial Version	2006/03/22

1 General Description

The EM78612 is a series of Universal Serial Bus 8-bit RISC microcontrollers. It is specifically designed for USB low speed device application and to support legacy device such as PS/2 mouse. The EM78612 also support one device address and two endpoints..

The EM78612 is implemented on a RISC architecture. It has five-level stack and six interrupt sources. The amount of General Input/Output pins is up to12. Each device has 80 bytes SRAM. The ROM size of the EM78612 is 2K.

These series of chips have Dual Clock mode which allows the device to run on low power saving frequency.

2 Features

- Low-cost solution for low-speed USB devices, such as mouse, joystick, and gamepad.
- USB Specification Compliance
  - Universal Serial Bus Specification Version 1.1
  - USB Device Class Definition for Human Interface Device (HID), Firmware Specification Version 1.1
  - Support 1 device address and 2 endpoints (EP0 and EP1)
- USB Application
  - USB protocol handling
  - USB device state handling
  - Identifies and decodes Standard USB commands to EndPoint Zero
- PS/2 Application Support
  - Built-in PS/2 port interface
- Built-in 8-bit RISC MCU
  - 5 level stacks for subroutine and interrupt
  - 6 available interrupts
  - 8-bit real time clock/counter (TCC) with overflow interrupt
  - Built-in RC oscillator free running for WatchDog Timer and Dual clock mode
  - Two independent programmable prescalers for WDT and TCC
  - Two methods of power saving:
    1. Power-down mode (SLEEP mode)
    2. Low frequency mode.
  - Two clocks per instruction cycle
- I/O Ports

- Up to 12 general purposes I/O pins grouped into two ports (Port 6 and 7).
- Up to 2 LED sink pins
- Each GPIO pin of Ports 6 & Port 7 has an internal programmable pull-high resistor
- Each GPIO pin of Ports 6 has an internal programmable pull- low resistor
- Each GPIO pin wakes up the MCU from sleep mode by input state change

■ Internal Memory
- Built-in 2048*13 bits MASK ROM
- Built-in 80 bytes general purpose registers (SRAM)
- Built-in USB Application FIFOs.

■ Operation Frequency
- Normal Mode: MCU runs on the external oscillator frequency
- Dual Clock Mode: MCU runs at the frequency of 256 KHz (or 32KHz, 4KHz, 500Hz), emitted by the internal oscillator with the external ceramic resonator turned off to save power.

■ Built-in 3.3V Voltage Regulator
- For MCU power supply
- Pull-up source for the external USB resistor on D-pin.

■ Package Type
- 16 pin PDIP(300MIL) / SOP(150MIL) (EM78612 AP / AM)
- 18 pin PDIP(300MIL) / SOP(300MIL) (EM78612 BP / BM)
- 20 pin PDIP(300MIL) / SOP(300MIL) (EM78612 CP / CM)
- 20 pin SSOP(209MIL) (EM78612 FM)

3 Applications

This microcontroller is designed for USB low speed device application or non-USB embedded device. It is also suitable for PS/2 mouse application.

4 Pin Configuration

EM78612A∗

P61	1●	16	P60
P62	2	15	P64
P63	3	14	P65
P70	4	13	P71
P72	5	12	D+/P50
VSS	6	11	D-/P51
V3.3V	7	10	V_{DD}
OSCI	8	9	OSCO

EM78612B∗

P60	1●	18	P64
P61	2	17	P65
P62	3	16	P66
P63	4	15	P67
P70	5	14	P71
P72	6	13	D+/P50
V_{SS}	7	12	D-/P51
$V_{3.3V}$	8	11	V_{DD}
OSCI	9	10	OSCO

EM78612C∗

P60	1●	20	P64
P61	2	19	P65
P62	3	18	P66
P63	4	17	P67
P70	5	16	P71
P72	6	15	P73
NC	7	14	D+/P50
V_{SS}	8	13	D-/P51
$V_{3.3V}$	9	12	V_{DD}
OSCI	10	11	OSCO

5 Pin Description

OSCI	I	6MHz / 12MHz ceramic resonator input.
OSCO	I/O	Return path for 6MHz / 12MHz ceramic resonator.
$V_{3.3V}$	O	3.3V DC voltage output from internal regulator. **This pin should be tied to a 4.7 μF decoupling capacitor to GND.**
P60 ~ P67	I/O	Port6 offers up to 8 GIOP pins. The pull high resistors (**132K** Ohms) and pull low resistors (**10K** Ohm) are selected through pin programming.
P70 ~ P73	I/O	Port7 offers up to 4 GIOP pins. The sink current of P70 & P71 are programmable for driving LED. Each pin has pull high resistors (**132K** Ohm) that can be selected through pin programming.
D+ / P50	I/O	USB Plus data line interface or PS/2 line interface are user-defined through firmware setting. When the EM78612 is running under PS/2 mode, this pin will have an internal pulled-high resistor (2.2K Ohm), with V_{DD}=5.0V. When this pin is used as a PS/2 line interface, it will generate an interrupt when its state changes (Port5 state change interrupt enable).
D- / P51	I/O	USB Minus data line interface or PS/2 line interface are user-defined through firmware setting. When the EM78612 is running under PS/2 mode, this pin will have an internal pulled-high resistor (2.2K Ohm), with V_{DD}=5.0V. When this pin is used as a PS/2 line interface, it will generate an interrupt when its state changes (Port5 state change interrupt enable). When the EM78612 is running under USB mode, this pin will have an internal pulled-high resistor, 1.5k Ohm, with $V_{3.3}$=3.3V.
V_{DD}	-	Connects to the USB power source or to a nominal 5V-power supply. Actual V_{DD} range can vary between 4.4V and 5.2V.
V_{SS}	-	Connects to ground.

Table 5-1 Pin Descriptions

6 Function Block Diagram

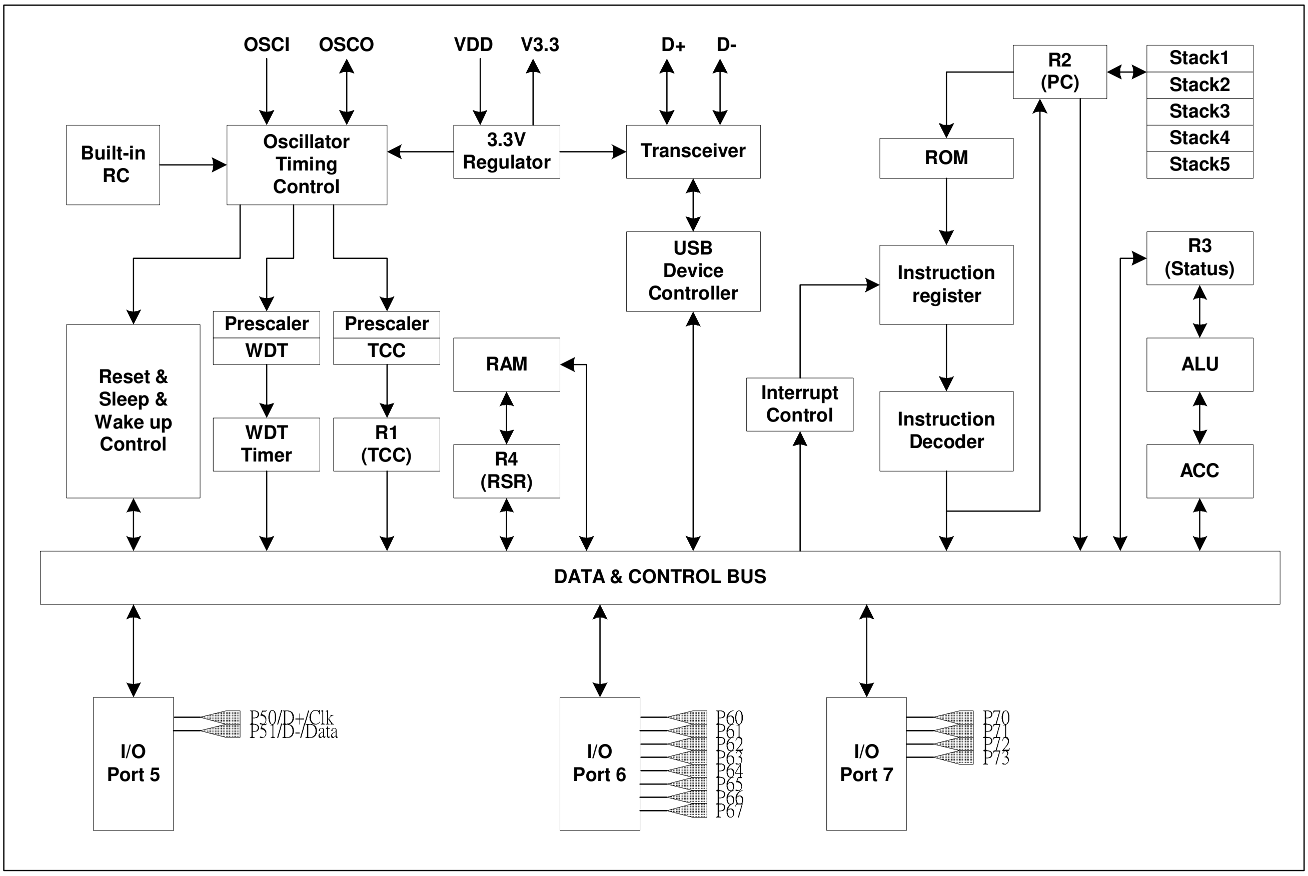


Figure 6-1 EM78612 Series Function Block Diagram

7 Function Description

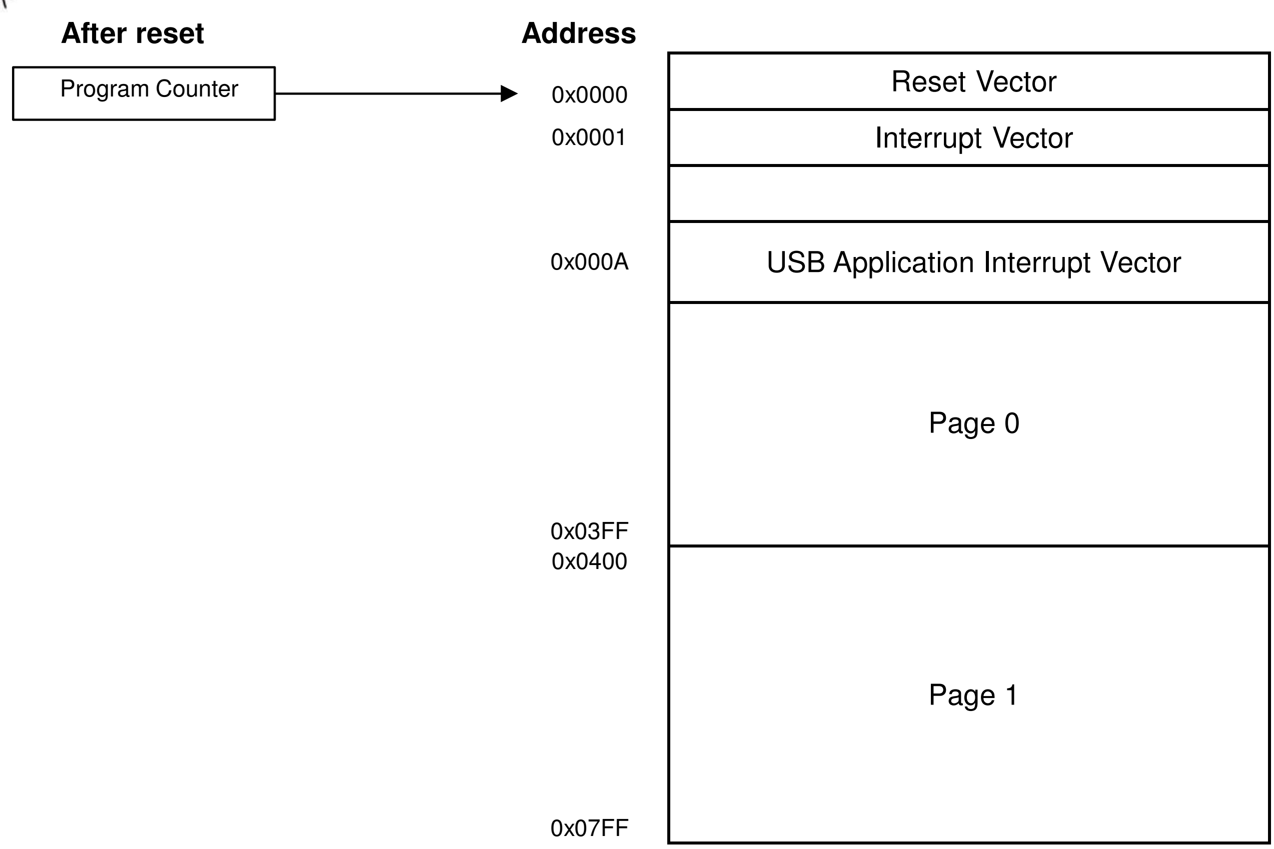
The memory of EM78612 is organized into four spaces, namely; User Program Memory in 2048*13 bits MASK ROM space, Data Memory in 80 bytes SRAM space, and USB Application FIFOs (for EndPoint0 and EndPoint1). Furthermore, several registers are used for special purposes.

7.1 Program Memory

The program space of the EM78612 is 2K words, and is divided into two pages. Each page has 1K words long. After Reset, the 12-bit Program Counter (PC) points to location zero of the program space.

It has two interrupt vectors, i.e., Interrupt Vectors at 0x0001 and USB Application Interrupt Vectors at 0x000A. The Interrupt Vector applies to TCC Interrupt, and Port 5 State Changed Interrupt. The USB Application Interrupt Vector is for USB EndPoint Zero Interrupt, USB Suspend Interrupt, USB Reset interrupt, and USB Host Resume Interrupt.

After an interrupt, the MCU will fetch the next instruction from the corresponding address as illustrated in the following diagram.



7.2 Data Memory

The Data Memory has 80 bytes SRAM space. It is also equipped with USB Application FIFO space for USB Application. The Figure 7-1 (next page) shows the organization of the Data Memory Space.

7.2.1 Special Purpose Registers

When the micro-controller executes the instruction, specific registers are invoked for assistance, such as; Status Register which records the calculation status, Port I/O Control Registers which control the I/O pins' direction, etc. The EM78612 series provides a lot more of other special purpose registers with different functions.

There are 15 Special Operation Registers which are located from Address 0x00 to 0x0F. On other hand, 10 more Special Control Registers are available to control functions or I/O direction. These are arranged from Address 0x05 to 0x0F.

> **Note**
>
> *that Special Control Registers can only be read or written by two instructions; IOR and IOW.*

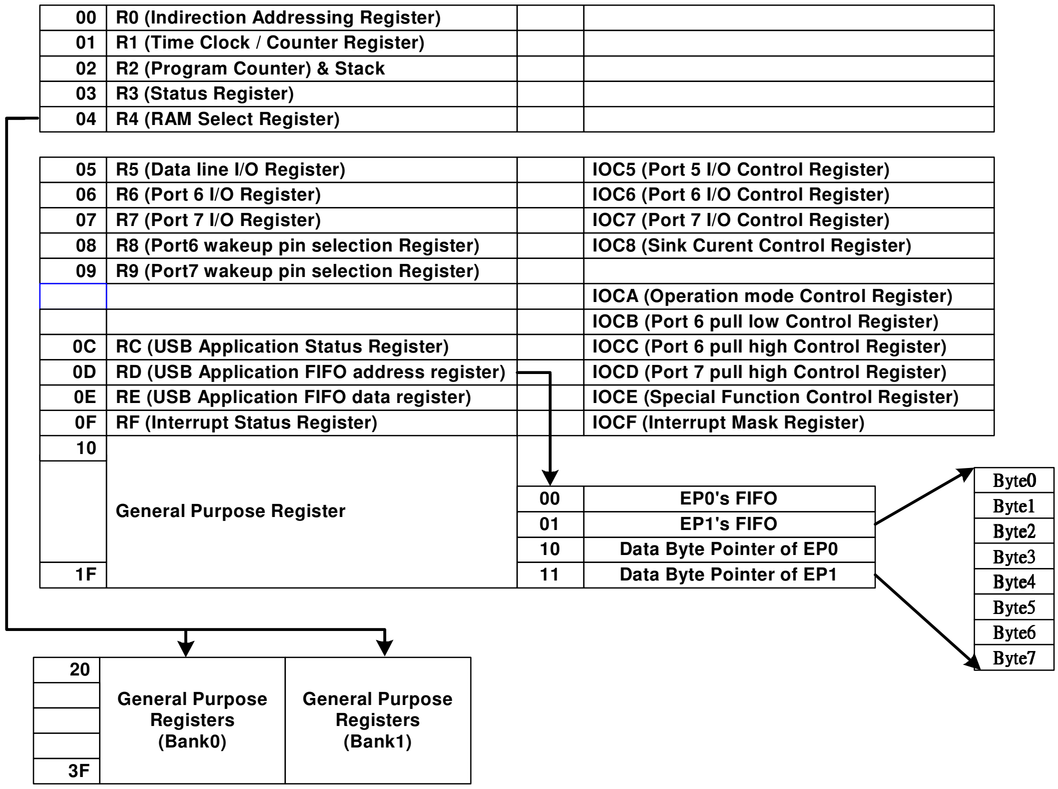


Fig 7-1 The Organization of EM78612 Data RAM

7.2.1.1 Operation Registers in Bank 0

The following introduces each of the Operation Registers under the Special Purpose Registers. The Operation Registers are arranged according to the order of registers' address. Note that some registers are read only, while others are both readable and writable.

R0 (Indirect Address Register) Default Value: (0B_0000_0000)

R0 is not a physically implemented register. Its major function is to be an indirect address pointer. Any instruction using R0 as a pointer actually accesses the data pointed by the RAM Select Register (R4).

R1 (Time / Clock Counter) Default Value: (0B_0000_0000)

This register TCC, is an 8-bit timer or counter. It is readable and writable as any other register. The Timer module will increment every instruction cycle . The user can work around this by writing an adjusted value. The Timer interrupt is generated when the R1 register overflows from FFh to 00h. This overflow sets bit TCIF(RF[0]). The interrupt can be masked by clearing bit TCIE (IOCF[0]).After Power-on reset and WatchDog reset, the initial value of this register is 0x00.

R2 (Program Counter & Stack) Default Value: (0B_0000_0000)

The EM78612 Program Counter is an 11-bit long register that allows access to 2K bytes of Program Memory with 5 level stacks. The eight LSB bits, 00~07, are located at R2, while the one MSB bits, 10, is located at R3 [5].The Program Counter is cleared after Power-on reset or WatchDog reset. The first instruction that is executed after a reset is located at Address 00h.

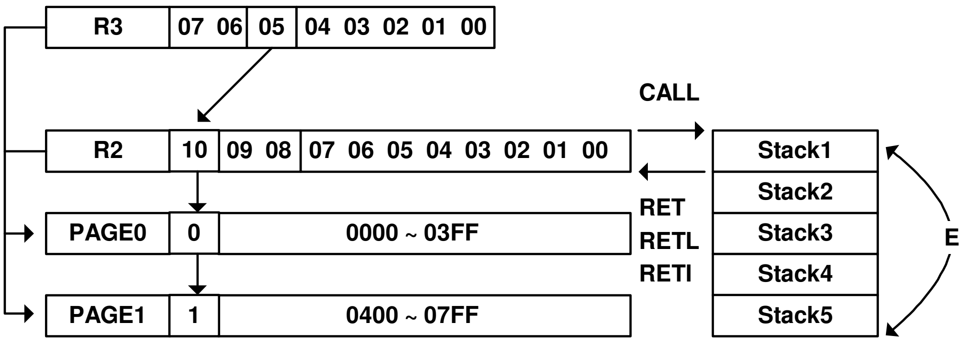


Fig 7-2 The Structure of ROM Page

R3 (Status Register) Default Value:(0B_0001_1000)

-	-	PS0	T	P	Z	DC	C

R3 [0] Carry y/Borrow flag. For ADD , SUB Instructions

1 = A carry-out from the Most Significant bit of the result occurred

0 = No carry-out from the Most Significant bit of the result occurred

NOTE

For Borrow, the polarity is reversed.For rotate (RRC, RLC) instructions, this bit is loaded with either the high or low-order bit of the source register

R3 [1] Auxiliary carry /borrow flag. For ADD , SUB Instructions

1 = A carry-out from the 4th low-order bit of the result occurred

0 = No carry-out from the 4th low-order bit of the result

NOTE

For Borrow, the polarity is reversed.

R3 [2] Zero flag. It will be set to 1 when the result of an arithmetic or logic operation is zero.

R3 [3] Power down flag. It will be set to 1 during Power-on phase or by “WDTC” command and cleared when the MCU enters into Power down mode. It remains in previous state after WatchDog Reset.

1: Power-on.

0: Power down

R3 [4] Time-out flag. It will be set to 1 during Power-on phase or by “WDTC” command. It is reset to 0 by WDT time-out.

1: WatchDog timer without overflow.

0: WatchDog timer with overflow.

The various states of Power down flag and Time-out flag at different conditions are shown below:

		Condition
1	1	Power-on reset
1	1	WDTC instruction
0	*P	WDT time-out
1	0	Power down mode
1	0	Wakeup caused by port change during Power down mode

*P: Previous status before WDT reset

R3 [5] Page selection bit. This bit is used to select a page of program memory (refer to R2, Program Counter).

PS0	Program Memory Page [Address]
0	Page 0 [0000-03FF]
1	Page 1 [0400-07FF]

R3 [6,7] Reserved registers.

R4 (RAM Select Register) Default Value: (0B_0xxx_xxxx)

7	6	5	4	3	2	1	0
-	BK0	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0

R4 (RAM select register) contains the address of the registers.

R4 [0~5] are used to select registers in 0x00h~0x3Fh. The address 0x00~0x1F is common space. After 0x1Fh, SRAM is grouped into two banks.

R4 [6] are used to select register banks. To select a registers bank, refer to the following examples and the table below**:**

R4=01111100 points to the register 0x3C in Bank 1.

R4[6]Bk0	RAM Bank #
0 1	Bank 0 Bank 1

R5 (Data Line I/O Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	D- or DATA	D+ or CLK

R5 [0] USB D+ line register or PS/2 clock interface register.

R5 [1] USB D- line register or PS/2 data interface register.

These two bits are BOTH writable and readable when the MCU is operating under PS/2 mode. But under USB Mode, these two bits cannot be accessed.

R5 [2~7] NON Used .The value is zero.

R6 (Port 6 I/O Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60

R7 (Port 7 I/O Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
-	-	-	-	P73	P72	P71	P70

R8 (Port 6 Wake-up Pin Selection Register) Default Value: (0B_1111_1111)

7	6	5	4	3	2	1	0
/Wu67	/wu66	/Wu65	/Wu64	/Wu63	/Wu62	/Wu61	/Wu60

R8 [0 ~ 7] Select which of the Port 6 pins are to be defined to wake-up the MCU from sleep mode. When the state of the selected pins changes during sleep mode, the MCU will wake-up and execute the next instruction automatically.

1: Disable the wake-up function

0: Enable the wake-up function

R9 (Port 7 Wake-up Pin Selection Register) Default Value: (0B_1111_1111)

7	6	5	4	3	2	1	0
-	-	-	-	/Wu73	/Wu72	/Wu71	/Wu70

R9 [0 ~ 3] Select which of the Port 7 pins are to be defined to wake-up the MCU from sleep mode. When the state of the selected pins changes during sleep mode, the MCU will wake-up and execute the next instruction automatically.

1: Disable the wake-up function

0: Enable the wake-up function

RC (USB Application Status Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
EP0_W	EP0_R	EP1_R	0	Device_Resume	Host_Suspend	EP0_Busy	Stall

RC [0] Stall flag. When MCU receives an unsupported command or invalid parameters from host, this bit will be set to 1 by the firmware to notify the UDC to return a STALL handshake. When a successful SETUP transaction is received, this bit is cleared automatically. This bit is both readable and writable.

RC [1] EP0 Busy flag. When this bit is equal to "1," it indicates that the UDC is writing data into the EP0'FIFO or reading data from it. During this time, the firmware will avoid accessing the FIFO until UDC finishes writing or reading. This bit is only readable.

RC [2] Host Suspend flag. If this bit is equal to 1, it indicates that USB bus has no traffic for the specified period of 3.0 ms. This bit will also be cleared automatically when a bus activity takes place. This bit is only readable.

∗ *This bit should be used in Dual Mode*

RC [3] Device Resume flag. This bit is set by firmware to general a signal to wake-up the USB host and is cleared as soon as the USB Suspend signal becomes low. This bit can only be set by firmware and cleared by the hardware.

∗ *This bit should be used in Dual Mode*

RC [4] Undefined Register. The default value is 0.

RC [5,6] EP1_R / EP0_R flag. These two bits inform the UDC to read the data written by firmware from the FIFO. Then the UDC sends the data to the host automatically. After UDC finishes reading the data from the FIFO, this bit is cleared automatically.

Therefore, before writing data into the FIFO, the firmware will first check this bit to prevent overwriting the existing data. These two bits can only be set by the firmware and cleared by the hardware.

RC [7] EP0_W flag. After the UDC completes writing data to the FIFO, this bit will be set automatically. The firmware will clear it as soon as it gets the data from EP0's FIFO. Only when this bit is cleared that the UDC will be able to write a new data into the FIFO.

Therefore, before the firmware can write a data into the FIFO, this bit must first be set by the firmware to prevent UDC from writing data at the same time. This bit is both readable and writable.

RD (USB Application FIFO Address Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
0	0	0	UAD4	UAD3	UAD2	UAD1	UAD0

RD [0~4] USB Application FIFO address registers. These five bits are the address pointer of USB Application FIFO.

RD [5~7] Undefined registers. The default value is zero.

RE (USB Application FIFO Data Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
UD7	UD6	UD5	UD4	UD3	UD2	UD1	UD0

RE (USB Application FIFO data register) contains the data in the register of which address is pointed by RD.

NOTE

For example, if we want to read the fourth byte of the EndPoint Zero, we will use the address of EP0 (0x00) and Data Byte Pointer of EP0 (0x10) to access it.

```
// Read the 4rd byte of the EP0 FIFO
// First, assign the data byte pointer of EP0 register (0X10) with 0X03.
   MOVA, @0X10
   MOVRD, a        // Move data in A to RD register
   MOVA, @0X03
   MOVRE , A       // Move data in A to RE register

// Then read the content from EP0 FIFO (0x00) 4rd byte
   MOVA, @0X00
   MOVRD, A       // Assign address point to EP0 FIFO
   MOVA, RE       // Read the fourth byte data (byte3) of the EP0 FIFO
   MOV A, 0X0E// Read the fifth byte data (byte4) of the EP0 FIFO
```

RF (Interrupt Status Register) Default Value: (0B_0000_0000)

-	--	Port 5 State Change_IF	USB Host Resume_IF	USB Reset_IF	USB Suspend_IF	EP0_IF	TCC_IF

RF [0] TCC Overflow interrupt flag. It will be set while TCC overflows, and is cleared by the firmware.

RF [1] EndPoint Zero interrupt flag. It will be set when the EM78612 receives Vender /Customer Command to EndPoint Zero. This bit is cleared by the firmware.

RF [2] USB Suspend interrupt flag. It will be set when the EM78612 finds the USB Suspend Signal on USB bus. This bit is cleared by the firmware.

RF [3] USB Reset interrupt flag. It will be set when the host issues the USB Reset signal.

RF [4] USB Host Resume interrupt flag. It is set only under Dual Clock mode when the USB suspend signal becomes low.

RF [5] Port 5 State Change interrupt flag. It is set when the Port 5 state changes . (Port 5 state change interrupt only work in PS/2 mode.)

RF [6] *Default value is zero and do not modify it.*

R10~R1F are General purpose registers. These registers can be used no matter what Bank Selector is. There are 2 banks(BK0 & BK1) **R20~R3F** General purpose registers, Select by R4 [6].

7.2.1.2 Control Registers in Bank 0

Special purpose registers for special control purposes are also available. Except for the Accumulator (A), these registers must be read and written by special instructions. One of these registers, CONT, can only be read by the instruction "CONTR" and written by "CONTW" instruction. The remaining special control registers can be read by the instruction "IOR" and written by the instruction "IOW."

A (Accumulator Register)

The accumulator is an 8-bit register that holds operands and results of arithmetic calculations. It is not addressable.

CONT (Control Register)

7	6	5	4	3	2	1	0
RW_E	/INT	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0

NOTE

The CONT register can be read by the instruction "CONTR" and written by the instruction "CONTW."

CONT [0~2] WatchDog Timer prescaler bits. These three bits are used as the prescaler of WatchDog Timer.

CONT [3~5] TCC Timer prescaler bits.

The relationship between the prescaler value and these bits are as shown below:

PSR2/TSR2	PSR1/TSR1	PSR0/TSR0	TCC Rate	WDT Rate (8mS)
0	0	0	**6MHz / 2**	**8 ms**
0	0	1	**6MHz / 4**	**16 ms**
0	1	0	**6MHz / 8**	**32 ms**
0	1	1	**6MHz / 16**	**64 ms**
1	0	0	**6MHz / 32**	**128 ms**
1	0	1	**6MHz / 64**	**256 ms**
1	1	0	**6MHz / 128**	**512 ms**
1	1	1	**6MHz / 256**	**1024 ms**

CONT [6] Interrupt enable control bit. This bit toggles Interrupt function between enable and disable. It is set to 1 by the interrupt disable instruction "DISI" and reset by the interrupt enable instructions "ENI" or "RETI."

0: Enable the Interrupt function.

1: Disable the Interrupt function.

CONT [7] Remote wake-up enable bit. This bit is set to 1, if host enables device to remote wake-up PC. It could be modified by SetFeature() & ClearFeature() Request.

IOC5 ~IOC7 I/O Port Direction Control Registers

Each bit controls the I/O direction of three I/O ports (Port5~Port7) respectively. When these bits are set to 1, the relative I/O pins become input pins. Similarly, the I/O pins becomes outputs when the relative control bits are cleared.

1: Input direction.

0: Output direction.

IOC5 (Data Line I/O Control Register) Default Value: (0B_0000_0011)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	P51	P50

IOC5 [2~7] Undefined registers. The default value is 0.

IOC6 (Port 6 I/O Control Register) Default Value: (0B_1111_1111)

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60

IOC7 (Port 7 I/O Control Register) Default Value: (0B_0000_1111)

7	6	5	4	3	2	1	0
-	-	-	-	P73	P72	P71	P70

IOC8 (Sink Current Control Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
0	0	Sink1.1	Sink1.0	0	0	Sink01	Sink0.0

IOC8 [0,1][4,5] are P70/P71 sink current control registers. Four levels are offered for selection:

Sink0.1/1.1	Sink0.0/1.0	Sink Current
0	0	3mA±10%
0	1	6mA±10%
1	0	12mA±10%
1	1	25mA±10%

The default current after Power-on reset is 3mA.

IOCA (Operation Mode Control Register) Default Value: (0B_1100_0011)

7	6	5	4	3	2	1	0
Dual_Frq.1	Dual_Frq.0	0	0	0	0	PS/2	USB

IOCA [0,1] These two bits are used to select the operation mode. The definition of these two control registers is described in the table below.

IOCA[1]	IOCA[0]	Operation Mode
0	0	Detect Mode
0	1	USB Mode

1	0	PS/2 Mode
1	1	USB Test Mode

IOCA [2~5] Undefined registers. The default value is 0.

IOCA [6,7] Select the operation frequency in Dual Clock Mode. Four frequencies are available and can be chosen as Dual Clock mode for running the MCU program.

Dual_Frq.1	Dual_Frq.0	Frequency
0	0	500Hz
0	1	4kHz
1	0	32kHz
1	1	256kHz

IOCB (Port 6 Pull-Low Control Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60

IOCB [0~7] Select whether the 10K Ohm pull-low resistor of Port 6 individual pin is connected or not.

1: Enable the pull-low function.

0: Disable the pull-low function.

IOCC (Port 6 Pull-High Control Register) Default Value: (0B_0000_0000)

PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60

IOCC [0~7] Select whether the 132K Ohm pull-high resistor of Port 6 individual pin is connected or not.

1: Enable the pull-high function.

0: Disable the pull-high function.

IOCD (Port 7 Pull-High Control Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
-	-	-	-	PH73	PH72	PH71	PH70

IOCD [0~3] Select whether the 132K Ohm pull-high resistor of Port 7 individual pin is connected or not.

1: Enable the pull-high function.

0: Disable the pull-high function.

IOCE (Special Function Control Register) Default Value: (0B_1111_0000)

7	6	5	4	3	2	1	0
/Dual clock	/WUE	WTE	RUN	0	0	0	0

IOCE [0~3] Undefined register. The default value is zero.

IOCE [4] Run bit. This bit can be cleared by the firmware and set during power-on, or by the hardware at the falling edge of wake-up signal. When this bit is cleared, the clock system is disabled and the MCU enters into power down mode. At the transition of wake-up signal from high to low, this bit is set to enable the clock system.

1: Run mode. The EM78612 is working normally.

0: Sleep mode. The EM78612 is in power down mode.

IOCE [5] WatchDog Timer enable bit. The bit disable/enables the WatchDog Timer.

1: Enable WDT.

0: Disable WDT.

NOTE

If the Code Option WTC bit is "0," WDT is always disabled.

IOCE [6] Enable the wake-up function as triggered by port-change. This bit is set by UDC.

1: Disable the wake-up function.

0: Enable the wake-up function.

IOCE [7] Dual clock Control bit. This bit is used to select the frequency of system clock. When this bit is cleared, the MCU will run on very low frequency save power and the UDC will stop working.

1: Selects EM78612 to run on normal frequency.

0: Selects to run on slow frequency.

IOCF (Interrupt Mask Register) Default Value: (0B_0000_0000)

7	6	5	4	3	2	1	0
-	-	Port 5 State Change_IE	USB Host Resume_1E	USB Reset_IE	USB Suspend_IE	EP0_IE	TCC_IE

IOCF [0~5] TCC / EP0 / USB Suspend / USB Reset / USB Host Resume / Port 5 State Change enable bits. These eight bits respectively control the function of TCC interrupt, EP0 interrupt, USB Suspend interrupt, USB Reset interrupt, USB Host Resume interrupt, Port5 State Change interrupt, Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

1: Enable Interrupt.

0: Disable Interrupt.

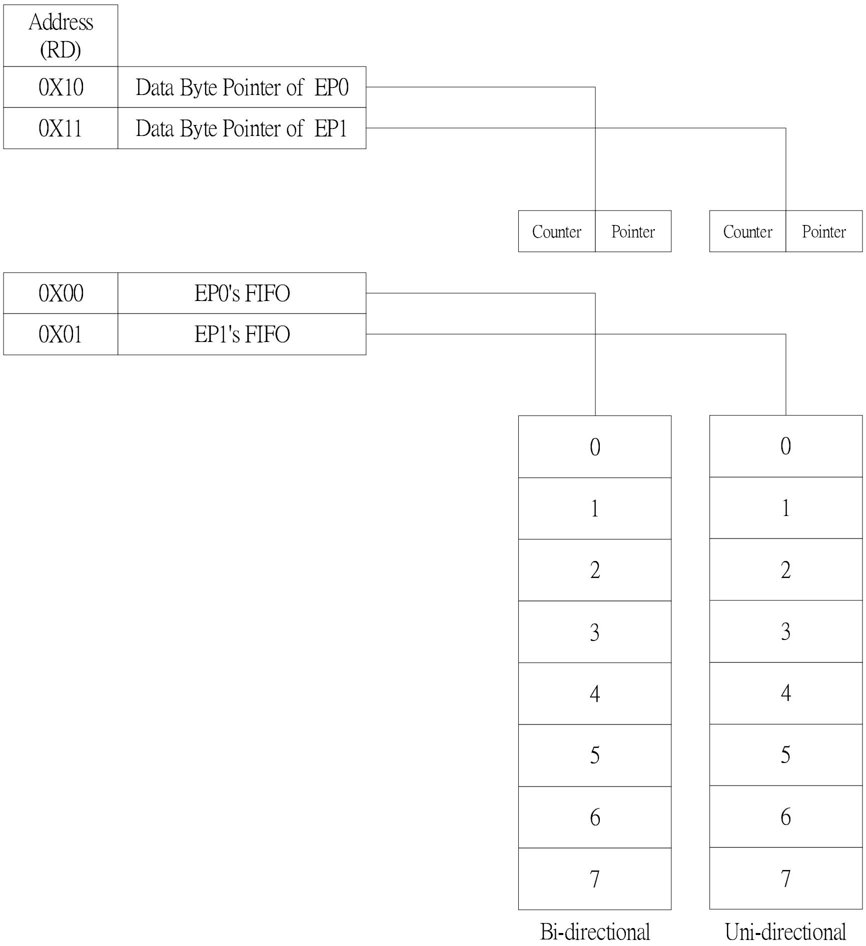
IOCF[6] Default value is zero and do not modify it.

Only when the global interrupt is enabled by the ENI instruction that the individual interrupt will work. After DISI instruction, any interrupt will not work even if the respective control bits of IOCF are set to 1.

The USB Host Resume Interrupt works only under Dual clock mode. This is because when the MCU is under sleep mode, it will be waked up by the UDC Resume signal automatically.

7.2.2 USB Application FIFOs

For USB Application, EM78612 provides an 8-byte First-In-First-Out (FIFO) buffer for each endpoint. The buffer cannot be accessed directly. However, a corresponding Data Byte Pointer register for each endpoint is made available to address the individual byte of the FIFO buffer. The content of the individual byte will map to a special register.



7.3 I/O Ports

The EM78612 has up to twelve General Purposes I/O pins, which are classifies into two port groups; Port 6 and Port 7. Each pin has an internal resistor that can be individually selected by user.

The following describes the important features o EM78612 I/O pins.

7.3.1 Programmable Large Current

Port 7 has two pins; P70 and P71 that can drive large current of up to 30mA. The range of driving current is from 3mA to 30mA, which is programmable. Use IOC8 [0,1] and IOC8 [4,5] to control the sink current of P70/P71. The default current is 3mA.

7.3.2 Wakeup by Port Change Function

Each of the GPIO pins in Port 6 and Port 7 can wakeup the MCU through signal change from input pin. This function is used to wake-up the MCU automatically from sleep mode. It also supports the remote wake-up function for USB application.

Any of the Individual pins of Port 6 and Port 7 can be defined to wakeup the MCU by setting their respective bits, R8 and R9.

7.4 USB Application

EM78612 is specially designed for USB device application and has many powerful functions that help the firmware to free itself from complex situation in various aspects of USB application.

7.4.1 Detect PS/2 or USB Mode

When the EM78612 is connected to the bus, the firmware should detect and identify which type of bus (USB or PS/2) it is connected to. The conditions that influence detect function are described below:

1. After a Power-on reset, the initial value of IOCA [0,1] is 0b00. Thus the operation mode is "Detect mode" and the D+ and D- I/O pins are internal pulled high by 200K Ohm to VDD.
2. The firmware checks the state of R5 [0,1]. If the state with which these two bits is 0b00, set the IOCA [0] to "1" to define the "USB mode." Otherwise, set the IOCA [1] to "1," to define "PS/2 mode."
3. When the operation mode is defined as "USB mode," the D- I/O pin is internal pulled high by a 1.5K Ohm resistor to 3.3V, which is output from a built-in regulator.
4. If the operation mode is in "PS/2 mode," both of the PS/2 interface I/O pins are internal pulled high by a 2.2K Ohm resistor to V_{DD}.

NOTE

The firmware should set the operation mode, either in USB mode or PS/2 mode, at the beginning of program.

An additional mode, "USB Test Mode" is also available. This mode has no load on D+ and D- I/O pins, and can only be used in USB Application case. Therefore, an external 1.5K Ohm resistor is needed to pull up D- IO pin to 3.3V.

Under "PS/2 mode," both PS/2 pins are programmed to generate an interrupt. After setting the Port 5 State change to Interrupt Enable bit, the MCU will interrupt while the state of these two pins changes.

7.4.2 USB Device Controller

The USB Device Controller (UDC) built-in in the EM78612 can interpret the USB Standard Command and response automatically without involving firmware. The embedded Series Interface Engine (SIE) handles the serialization and deserialization of actual USB transmission. Thus, a developer can concentrate his efforts more in perfecting the device actual functions and spend less energy in dealing with USB transaction.

The UDC handles and decodes most Standard USB commands defined in the USB Specification Rev1.1. If UDC receives an unsupported command, it will set a flag to notify MCU the receipt of such command. The Standard Commands that EM78612 supports includes; **Clear Feature, Get Configuration, Get Interface, Get Status, Set Address, Set Configuration, Set Feature, and Set Interface.**

Each time UDC receives a USB command, it writes the command into EP0's FIFO. Only when it receives unsupported command that the UDC will notify the MCU through interrupt.

Therefore, EM78612 is very flexible under USB application because the developer can freely choose the method of decoding the USB command as dictated by different situation.

7.4.3 Device Address and Endpoints

EM78612 supports one device address, two endpoints, EP0 for control endpoint, and EP1 for interrupt endpoint. Sending data to USB host in EM78612 is very easy. Just write data into EP's FIFO, then set flag, and the UDC will handle the rest. It will then confirm that the USB host has received the correct data from EM78612.

7.5 Reset

The EM78612 provides three types of reset**:** (1) Power-on Reset, (2) WatchDog Reset, and (3) USB Reset.

7.5.1 Power-On Reset

Power-on Reset occurs when the device is attached to power and a reset signal is initiated. The signal will last until the MCU becomes stable. After a Power-on Reset, the MCU enters into following predetermined states (see below), and then, it is ready to execute the program.

A. The program counter is cleared.

B. The TCC timer and WatchDog timer are cleared.

C. Special registers and Special Control registers are all set to initial value.

The MCU also has a low voltage detector that detects low output power condition. Whenever the output voltage of the 3.3V regulator decreases to below 2.2V, a reset signal is set off.

7.5.2 WatchDog Reset

When the WatchDog timer overflows, it causes the WatchDog to reset. After it resets, the program is executed from the beginning and some registers will be reset. The UDC however, remains unaffected.

7.5.3 USB Reset

When UDC detects a USB Reset signal on USB Bus, it interrupts the MCU, then proceed to perform the specified process that follows. After a USB device is attached to the USB port, it cannot respond to any bus transactions until it receives a USB Reset signal from the bus.

7.6 Power Saving Mode

The EM78612 provides two options of power saving modes for energy conservation, i.e., Power Down mode, and Dual Clock mode.

7.6.1 Power Down Mode

The EM78612 enters into Power Down mode by clearing the RUN register (IOCE[4]). During this mode, the oscillator is turned off and the MCU goes to sleep. It will wake up when signal from USB host is resumed, or when the WatchDog resets, or the input port state changes.

If the MCU wakes up when I/O port status changes, the direction of I/O port direction should be set at input direction, then read the state of port. For example:

```
// Set the Port 6 to input port
MOV     A,@0XFF
IOW     PORT6
// Read the state of Port 6
MOV     PORT6,PORT6
// Clear the RUN bit
IOR     0X0E
AND     A,@0B11101111
IOW     0X0E
```

:
:

7.6.2 Dual Clock Mode

The EM78612 has one internal oscillator for power saving application. Clearing the Bit IOCE [7] will enable the low frequency oscillator. At the same time, the external oscillator will be turned off. Then the MCU will run under very low frequency to conserve power. Four types of frequency are available for selection in setting Bits IOCA [6, 7].

The USB Host Resume Interrupt can only be used in this mode. If this interrupt is enabled, the MCU will be interrupted when the USB Host Resume signal is detected on USB Bus.

7.7 Interrupt

The EM78612 has two interrupt vectors, one is in 0x0001, and the other is in 0x000A. When an interrupt occurs while the MCU is running, it will jump to the interrupt vector (0x0001 or 0x000A) and execute the instructions sequentially from interrupt vector. RF is the interrupt status register that records the interrupt status in the relative flags/bits.

The interrupt condition could be one of the following:

1. TCC Overflow When the Timer Clock / Counter Register (R1) overflows, the status flag RF[0] will be set to 1. Its interrupt vector is 0X0001.
2. EP0 Interrupt When the UDC successfully received a setup transaction from host to EndPoint0, the status flag RF[1] will be set to 1. Its interrupt vector is 0X000A.
3. USB Suspend When UDC detects a USB Suspend signal on USB bus, the status flag RF[2] will be set to 1. Its interrupt vector is 0X000A.
4. USB Reset When the UDC detects a USB Reset signal on USB bus, the status flag RF[3] will be set to 1. Its interrupt vector is 0X000A.
5. USB Host Resume When UDC detects that the USB bus has left the Suspend condition, the status flag RF[4] will be set to 1. Its interrupt vector is 0X000A.
6. Port 5 State Change When the input signals in Port 5 changes, the status flag RF[5] will be set to 1. Its interrupt vector is 0X0001.

IOCF is an interrupt mask register which can be set individually bit by bit. While their respective bit is written to 0, the hardware interrupt will inhibit, that is, the EM78612 will not jump to the interrupt vector to execute instructions. But the interrupt status flags still records the conditions no matter whether the interrupt is masked or not. The interrupt status flags must be cleared by firmware before leaving the interrupt service routine and enabling interrupt.

The global interrupt is enabled by the ENI (RETI) instruction and is disabled by the DISI instruction.

- Interrupt flag. If a bit of RF is asserted, it means the relative interrupt requested.
- The priority of USB, TCC interrupt is **USB > TCC.**
- The additional hardware process step of the interrupt occurred including

  A、Disable interrupt means reserving next time interrupt process until the instruction "RETI" executed.

  B、Jump to interrupt vector.

  C、Push "Accumulator", "R3" and "R4". Steps "A", "B", and "C" are executed at the same time.

  D、Clear "R3"and"R4".

  E、If the instruction "RETI" is executed, pop "Accumulator", "R3" and "R4".

  F、Return to main program and enable interrupt. Step "E" and "F" are executed at the same time.

8 Absolute Maximum Ratings

Symbol	Min	Max	Unit
Temperature under bias	0	70	ºC
Storage temperature	-65	150	ºC
Input voltage	-0.5	6.0	V
Output voltage	-0.5	6.0	V

9 DC Electrical Characteristic

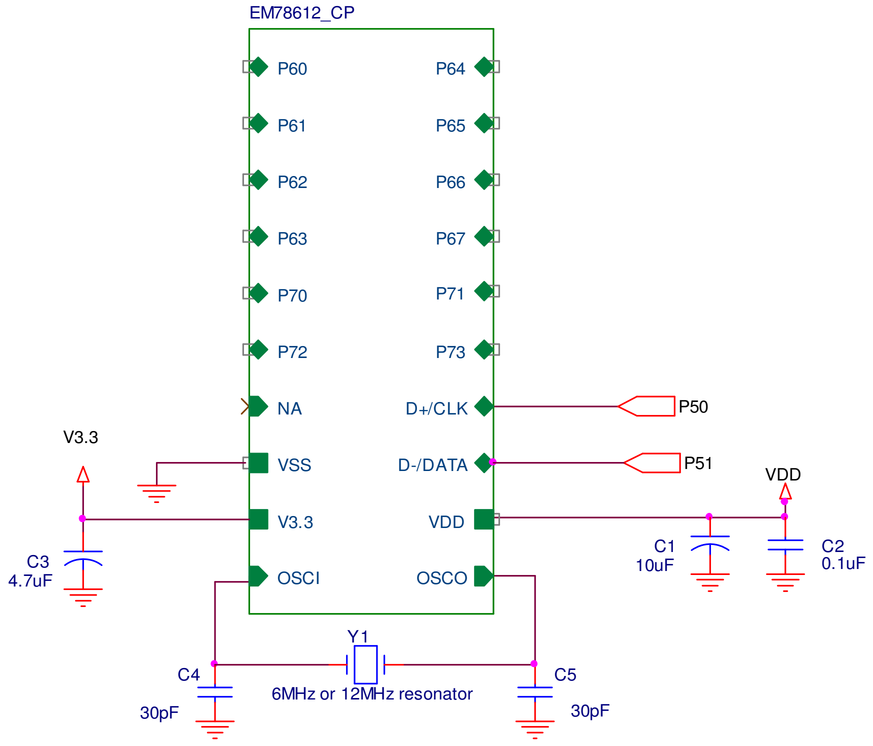
(T = 25℃, VDD = 5V, VSS = 0V)

Symble	Parameter	Condition	Min	Type	Max	Unit
3.3V Regulator						
V_{Rag}	Output voltage of 3.3v Regulator	V_{DD} = 5V	3.0	3.3	3.6	V
V_{ResetL}	Low Power Reset detecting low Voltage			-		V
V_{ResetH}	Low Power Reset detecting high Voltage			-		V
Ireg	3.3V Regulator driving capacity	V3.3 = 3.3V	-	-	100	mA
MCU Operation						
I_{IL}	Input Leakage Current for input pins	VIN= V_{DD},VSS	-	-	±1	μA
V_{IHX}	Clock Input High Voltage	OSCI	2.5	-	-	V
V_{ILX}	Clock Input Low Voltage	OSCI	-	-	1.0	V
I_{CC1}	V_{DD} operating supply current – Normal frequency operation mode	Freq. = 6MHz	-	-	10	mA
I_{SB}	Operating supply current 1 – Power down mode	WDT disabled	-	-	100	μA
GPIO Pins						
V_{IH}	Input High Voltage	Port 5	2.0	-	-	V
V_{IL}	Input Low Voltage	Port 5	-	-	0.8	V
V_{IH}	Input High Voltage	Port 6 & 7	2.0	-	-	V
V_{IL}	Input Low Voltage	Port 6 & 7	-	-	0.8	V
I_{OH1}	Output High Voltage (Port 6 & P72~P73)	V_{OH1} = 2.4V V_{REG} = 3.3V		11		mA
I_{OL1}	Output Low Voltage (Port 6)	V_{OL2} = 0.4V V_{REG} = 3.3V		11		mA
I_{OH2}	Output High Voltage (Port5)	V_{OH2} = 2.4V V_{DD} = 5V		7		mA
I_{OL2}	Output Low Voltage (Port5)	V_{OL2} = 2.4V V_{DD} = 5V		13		mA
R_{PH}	Pull-high resister	The input pin with internal pull-high resistor of Port6 or Port7 is connected to V_{SS}.		100		KΩ
R_{PL}	Pull-low resister	The input pin with internal pull-low resistor of Port6 is connected to V_{DD}.		8		KΩ

Symble	Parameter	Condition	Min	Type	Max	Unit
USB Interface						
V_{OH}	Static Output High	USB operation Mode	2.8	-	3.6	V
V_{OL}	Static Output Low		-	-	0.3	V
V_{DI}	Differential Input Sensitivity		0.2	-	-	V
V_{CM}	Differential Input Command Mode Range		0.8	-	2.5	V
V_{SE}	Single Ended Receiver Threshold	USB operation Mode	0.8	-	2.0	V

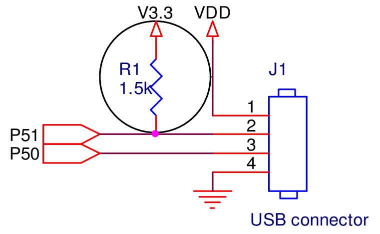
C_{IN}	Transceiver Capacitance		-	-	20	pF
V_{RG}	Output Voltage of Internal Regulator		3.0	-	3.6	V
R_{PH}	Pull-high resister (D-)			1.5		KΩ
Programmable Large Current						
I_{Sink1}	P70, P71 Output Sink Current	V_{OUT} = 0.4V, IOC8[0,1] or IOC8[4,5] = 00	-30%	3	+30%	mA
I_{Sink2}	P70, P71 Output Sink Current	V_{OUT} = 0.4V, IOC8[0,1] or IOC8[4,5] = 01	-30%	6	+30%	mA
I_{Sink3}	P70, P71 Output Sink Current	V_{OUT} = 0.4V, IOC8[0,1] or IOC8[4,5] = 10	-30%	12	+30%	mA
I_{Sink4}	P70, P71 Output Sink Current	V_{OUT} = 0.4V, IOC8[0,1] or IOC8[4,5] = 11	-30%	25	+30%	mA

10 Application Cricuit




```
Note :
A. Place C1 and C2 close to MCU VDD pin.
B. Place Y1, C4 and C5 close to MCU OSCI pin.
C. In USB application, it is necessary to place C3 close to MCU V3.3 pin.
D. Port6 and Port7 are 3.3V level I/O.
E. Port60 is input only and without internal pull-high and pull-low resistor.
```

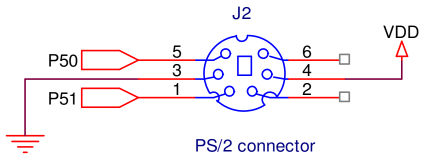
USB Application




```
Note1. IF IOCA = USB mode, MCU D- pin internal
pull-high to V3.3 with 1.5k resistor.

Note2. IF IOCA = USB test mode, it is necessary that
D- pin external pull-high to V3.3 with 1.5k
resistor.
```

PS/2 Application




```
Note3. IF IOCA = PS/2 mode, MCU CLK and DATA pin
internal pull-high to VDD with 4.7k resistor.
```

Appendix

A. Special Register Map

Operation Registers

0x00	R0	Indirect Addressing Register								0B_0000_0000
0x01	R1(TCC)	Timer/Clock Counter								0B_0000_0000
0x02	R2(PC)	Program Counter								0B_0000_0000
0x03	R3(STATUS)	-	-	PS0	T	P	Z	DC	C	0B_0001_1xxx
0x04	R4(RSR)	-	BK0	Select the register(address: 00~3F) in the indirect addressing mode						0B_0xxx_xxxx
0x05	R5(Port5)	-	-	-	-	-	-	P51/D- /DATA	P50/D+ /CLK	0B_0000_0000
0x06	R6(Port6)	P67	P66	P65	P64	P63	P62	P61	P60	0B_0000_0000
0x07	R7(Port7)	-	-	-	-	P73	P72	P71	P70	0B_0000_0000
0x08	R8(Port6 Wake-up Pin Selection)	/Wu67	/Wu66	/Wu65	/Wu64	/Wu63	/Wu62	/Wu61	/Wu60	0B_1111_1111
0x09	R9(Port7 Wake-up Pin Selection)	-	-	-	-	/Wu73	/Wu72	/Wu71	/Wu70	0B_1111_1111
0x0C	RC	EP0_W	EP0_R	EP1_R	0	Device Resume	Host _SUSPEND	UDC _Writing	STALL	0B_0000_0000
0x0D	RD	USB Application FIFO Address Register								0B_0000_0000
0x0E	RE	USB Application FIFO Data Register								0B_0000_0000
0x0F	RF	-	EP1_IF	Port5 state change_IF	USB Host Resume_ IF	USB Reset_IF	USB Suspend_IF	EP0_IF	TCC_IF	0B_0000_0000

Control Registers

	CONT	RW_E	INT	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0	0B_0100_0000
0x05	IOC5	Port5 Direction Control Register								0B_0000_0011
0x06	IOC6	Port6 Direction Control Register								0B_1111_1111
0x07	IOC7	Port7 Direction Control Register								0B_0000_1111
0x08	IOC8 (Sink Current)	-	-	Sink[71]_1	Sink[71]_0			Sink[70]_1	Sink[70]_0	0B_0000_0000
0x09	IOC9	Reserved								
0x0A	IOCA	Dual_Frq.1	Dual_Frq.0	-	-	-	-	PS/2	USB	0B_1100_0000
0x0B	IOCB	/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60	0B_0000_0000
0x0C	IOCC	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60	0B_0000_0000
0x0D	IOCD	-	-	-	-	/PH73	/PH72	/PH71	/PH70	0B_0000_0000
0x0E	IOCE	/Dual clock	/WUE	WTE	RUN	0	0	0	0	0B_1111_0000
0x0F	IOCF	0	EP1_IE	Port5_State_ Change_IE	USB HOST Resume_IF	USB Reset_IE	USB Suspend_IE	EP0_IE	TCC_IE	0B_0000_0000

B. Instruction Set

Each instruction in the instruction set is a 11-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consisting of 2 oscillator periods), unless the program counter is changed by-

(a) Executing the instruction "MOV R2,A", "ADD R2,A", "TBL", or any other instructions that write to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2", ····).

(b) execute CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) which were tested to be true.

Under these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

(1). Every bit of any register can be set, cleared, or tested directly.

(2). The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator that selects the value for the bit located in the register "R" and affects operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

Note

1 This instruction is applicable to IOCx only.

2 This instruction is not recommended for RE, RF operation.

C. Code Option Register

EM78612 has one CODE option registers, which are not part of the normal program memory. The option bits cannot be accessed during normal program execution.

8	7	6	5	4	3	2	1	0
			R.S.	**Package_1**	**Package_0**	**OST_1**	**OST_0**	**Frequency**

Bit 0 (Frequency) : Frequency Selection.

0: The MCU run on 12 MHz
1: The MCU run on 6 MHz

Bit 2~1 (OST_1 ~ OST_0) : Oscillator Start-up Time.

00: 500us
01: 2ms
10: 8ms
11: 16ms

Bit 4~3 (Package_1 ~ Package_0) : Package type selector.

00 : 16 pins
01 : 18 pins
10 : 20 pins
11 : No define

Bit 5 (R.S.) : Resistor Switch. enable of Transceiver.

0: Disconnect internal USB D- pull high Register
1: Connect internal USB D- pull high Resister

Bit 8~6 :The values are fixed.