Errata

This errata sheet is for MB90480/485 Series Hardware Manual Rev.7 (CM44-10121-7E)

F^{2}MC-16LX
16-BIT MICROCONTROLLER
MB90480/485 Series
HARDWARE MANUAL

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<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>507</td><td>24.1</td><td>"Table 24.1-1 Function of Pins" was corrected as indicated by the shading below.

(Error)
<table>
<tr><th>Pin</th><th>Function</th><th>Additional information</th></tr>
<tr><td>MD2,MD1 ,MD0</td><td>Mode pin</td><td>Setting MD2=1, MD1=1, and MD0=0 to enter the serial programming mode.</td></tr>
<tr><td>X0,X1</td><td>Oscillation pin</td><td>As, in the serial programming mode, CPU internal operation clock is the PLL clock multiplied-by-1, the internal operation clock frequency is equal to the oscillation clock frequency. Consequently, the frequencies that can be input to the high-speed oscillation input pin for serial writing are from 4.5 MHz to 25 MHz.</td></tr>
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<tr><td></td><td></td><td></td></tr>
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[mcu_doc0743]</td></tr>
</table>

FUJITSU

Corrections of Hardware Manual

MB90480

hm90480-cm44-10121-7e-corr-x1-00

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Addendum, MB90480 Hardware Manual (CM44-10121-7E)

This is the Addendum for the Hardware Manual CM44-10121-7E of the MB90480 microcontroller series. It describes all known discrepancies of the MB90480 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90480001	25.06.04	1.00	6	Low power consumption mode Transition to standby mode, Standby Cancel failure behavior
HWM90480002	25.06.04	1.00	27	I2C INTERFACE, Note added
HWM90480003	04.08.04	1.00	3.6	Interrupt by µDMA, usage of µDMA

HWM90480001 TOP

Transition to standby mode

The definition of Standby Cancel Failure is that the CPU will execute wrong instructions when an interrupt is executed during transition to Standby mode[1] at a certain time.

[1]:Definition of Standby mode
Main sleep mode, PLL sleep mode, Sub-sleep mode
Time base timer mode, Watch mode, Main watch mode
Main stop mode, PLL stop mode, Sub-stop mode
*Main watch mode is only for MB90370 series.

In the following cases, no problem occurs:
-Standby mode is not used
-Standby mode is released only by external reset

For further information refer to Hardware Manual chapter: ‘Low power consumption mode.’

HWM90480002 TOP

CHAPTER 27 I2C INTERFACE (ONLY MB90485 SERIES)

Restriction of specification at sending General Call Address for MCU with I2C

When using Multi-Master mode for I2C and another Master is sending a General Code Address at same time as Fujitsu MCU, an arbitration lost* occurs after 2nd byte.
Under following conditions the restriction do not exist:
- No usage of I2C peripheral
- Usage of I2C with Single Master system
- Usage of I2C with Multi Master system, no General Call Address used
- Usage of I2C with Multi Master system, General Call Address used by Fujitsu MCU, only
- Usage of I2C with Multi Master system, General Call Address used. If the value of data, send by Fujitsu MCU, is smaller than another transfer data, the arbitration lost does not occur.

*: If the data value is smaller than another one, oneself never has "Arbitration lost" because one with large transmission data value will have "Arbitration lost".

Chapter 3.6 Interrupt by µDMA

There might be problems when using µDMA with UART or PPG.

1) Detailed of bug for uDMA transmission

Fujitsu found the bug, as uDMA transmission is not operated normally for MB90480/485 series. The bug has two combinations as following.
1.uDMA and UART (Synchronization/Asynchronization) transmission
2.uDMA and PPG
Also we have already checked the combination between uDMA and other resource. But there was no bug for other combination.

Resource	Result
External interrupt	○
PWC0	○
PPG0/1	×
PPG2/3	×
PPG4/5	×
Input capture 0 load	○
Input capture 1 load	○
UART(Synchronization/Asynchronization) receive completed	○
UART(Synchronization/Asynchronization) transmit completed	×
Output compare 0 match	○
Output compare 1 match	○
Output compare 2 match	○
Free-run timer / Reload timer	○
SIO1	○
SIO2	○
A/D	○

Table 1. Check list of combination between uDMA and other resource

1-1) Detailed of bug with combination between uDMA and UART (Synchronization/Asynchronization) transmission
When the serial data is sent continuously from UART (Synchronization/Asynchronization) with using uDMA, Fujitsu found that less bytes than set bytes is outputted for FLASH device. The root cause of this behavior is to operate continuously next uDMA transmission, because interrupt clear timing of UART (Synchronization/Asynchronization) transmission is delayed. However for Evaluation device, when [debug mode] is used, expected data is outputted because internal operating is low speed. And when [native mode] is used, the behavior of bug is occurred for FLASH and MASK device. And at using only UART (Synchronization/Asynchronization) (not using uDMA), this bug is not occurred.

1-2) Detailed of bug with combination between uDMA and PPG
When the output of PPG is changed continuously with using uDMA, Fujitsu found that expected waveform is not outputted. This behavior is the root cause of specification as interrupt source of PPG is not cleared by uDMA. However at using only PPG (not using uDMA), this bug is not occurred.

2) Target devices of bug

Target devices of this bug is as following.

Series	Devices
MB90480/485series	MB90F481, MB90F482, MB90V480, MB90486, MB90487, MB90487A, MB90488A, MB90F488, MB90V485

Table 2. Target devices of bug

3) Countermeasure and revising schedule

For this bug, Fujitsu consider that provisional countermeasure is possible by following method.

3-1) Provisional countermeasure plan with combination between uDMA and UART (Synchronization/Asynchronization) transmission (Software countermeasure)
At using EI2OS of secret function for MB90480/485series, the behavior of bug is avoided. EI2OS has same function as uDMA, and same data transmission as uDMA is possible. However note that execution time of transmission between EI2OS and uDMA is different.

		With using uDMA		With using EI^{2}OS	
IOA updated / fixed selection		Fixed	Updated	Fixed	Updated
BAP updated / fixed selection	Fixed	17	19	32	34
	Updated	19	21	34	36

Table 3. Execution time of transmission (Unit: Machine clock cycle)

3-2) Permanent countermeasure with combination between uDMA and UART (Synchronization/Asynchronization) transmission (Hardware revision)
For countermeasure of bug with combination between uDMA and UART (Synchronization/Asynchronization) transmission, Fujitsu revise MB90485series as high priority. Revision schedule of MB90485series is as following. Also countermeasure device of this bug is added “B” suffix to end of part number.

Part number after revision	Providing schedule
MB90486B (MASK)	2004/08/M: from reception
MB90487B (MASK)	2004/08/M: from reception
MB90488B (MASK)	2004/08/M: from reception
MB90F488B (FLASH)	2004/08/12: provide ES
MB90V485B (EVA)	2004/08/13: provide ES

Table 4. Part number after revision and schedule

3-3) Countermeasure with combination between uDMA and PPG
Fujitsu consider as the restriction of specification for usage with combination between uDMA and PPG. Therefore Fujitsu doesn’t implement permanent countermeasure (hardware revision). Use the interrupt of PPG but not uDMA.