INTEGRATED CIRCUITS

DATA SHEET

TDA8928J
Power stage 2 x 10 or 1 x 20 W class-D audio amplifier

Preliminary specification
Supersedes data of 2004 Feb 04

2004 May 05

Philips Semiconductors

PHILIPS

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1 FEATURES

- High efficiency (> 90 %)
- Supply voltage from ±7.5 V to ±30 V
- Very low quiescent current
- High output power
- Diagnostic output
- Usable as a stereo Single-Ended (SE) amplifier
- Electrostatic discharge protection (pin to pin)
- No heatsink required.

2 APPLICATIONS

- Television sets
- Home-sound sets
- Multimedia systems
- All mains fed audio systems.

3 GENERAL DESCRIPTION

The TDA8928J is a switching power stage for a high efficiency class-D audio power amplifier system.

With this power stage a compact 2 × 10 W self oscillating digital amplifier system can be built, operating with high efficiency and very low dissipation. No heatsink is required. The system operates over a wide supply voltage range from ±7.5 V up to ±30 V and consumes a very low quiescent current.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_P	supply voltage		±7.5	±12.5	±30	V
$I_{q(tot)}$	total quiescent current	no load connected; V_P = ±12.5 V	–	25	45	mA
η	efficiency	P_o = 10 W; R_L = 8 Ω; V_P = ±12.5 V	–	90	–	%
Stereo single-ended configuration						
P_o	output power	R_L = 8 Ω; THD = 10 %; V_P = ±12.5 V	9	10	–	W
		R_L = 16 Ω; THD = 10 %; V_P = ±12.5 V	–	5	–	W

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8928J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 7.7 mm)	SOT243-3
TDA8928ST	RDBS17P	plastic rectangular DIL-bent-SIL power package; 17 leads (row spacing 2.54 mm)	SOT577-2

6 BLOCK DIAGRAM

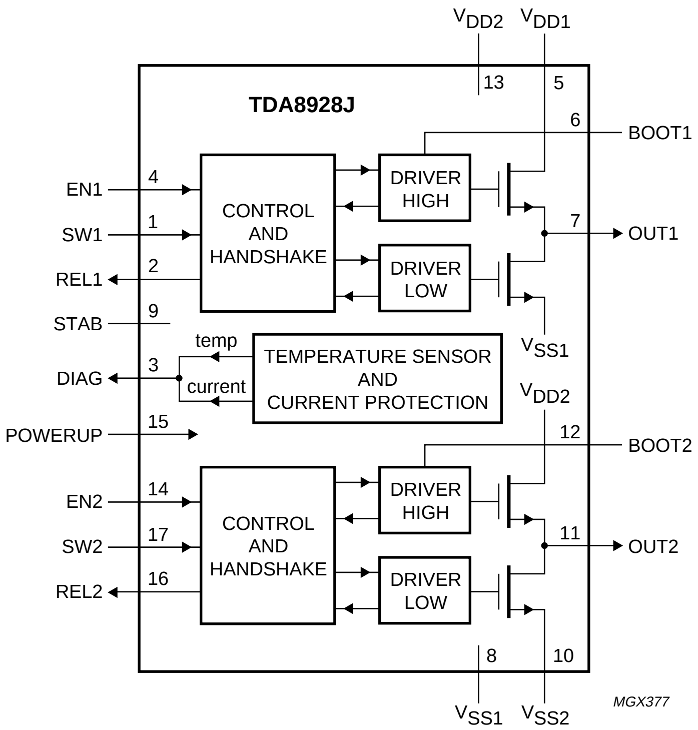


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
SW1	1	digital switch input; channel 1
REL1	2	digital control output; channel 1
DIAG	3	digital open-drain output for overtemperature and overcurrent report
EN1	4	digital enable input; channel 1
V_{DD1}	5	positive power supply; channel 1
BOOT1	6	bootstrap capacitor; channel 1
OUT1	7	PWM output; channel 1
V_{SS1}	8	negative power supply; channel 1
STAB	9	decoupling internal stabilizer for logic supply
V_{SS2}	10	negative power supply; channel 2
OUT2	11	PWM output; channel 2
BOOT2	12	bootstrap capacitor; channel 2
V_{DD2}	13	positive power supply; channel 2
EN2	14	digital enable input; channel 2
POWERUP	15	enable input for switching on internal reference sources
REL2	16	digital control output; channel 2
SW2	17	digital switch input; channel 2

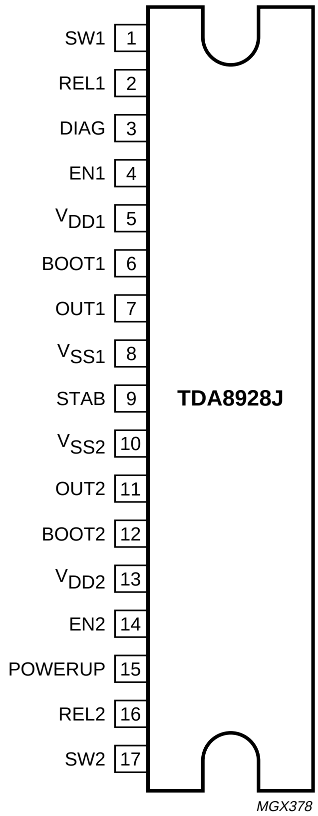


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

The TDA8928J is a two-channel audio power amplifier system using class-D technology.

The power stage TDA8928J is used for driving the loudspeaker load. It performs a level shift from the low-power digital PWM signal, at logic levels, to a high-power PWM signal that switches between the main supply lines. A 2nd-order low-pass filter converts the PWM signal into an analog audio signal across the loudspeaker.

8.1 Power stage

The power stage contains high-power DMOS switches, drivers, timing and handshaking between the power switches and some control logic (see Fig.1).

The following functions are available:

- Switch (pins SW1 and SW2): digital inputs; switching from V_{SS} to V_{SS} + 12 V and driving the power DMOS switches
- Release (pins REL1 and REL2): digital outputs; switching from V_{SS} to V_{SS} + 12 V; follow pin SW1 and SW2 with a small delay. Note: for self oscillating applications this pin is not used
- Power-up (pin POWERUP): must be connected to a continuous supply voltage of at least V_{SS} + 5 V with respect to V_{SS}
- Enable (pins EN1 and EN2): digital inputs; at a level of V_{SS} the power DMOS switches are open and the PWM outputs are floating; at a level of V_{SS} + 12 V the power stage is operational
- Diagnostics (pin DIAG): digital open-drain output; pulled down to V_{SS} if the maximum temperature or maximum current is exceeded.

8.2 Protection

Temperature and short-circuit protection sensors are included in the TDA8928J. The diagnostic output is pulled down to V_{SS} in the event that the maximum current or maximum temperature is exceeded. The system shuts itself down when pin DIAG is connected to pins EN1 and EN2.

8.2.1 MAXIMUM TEMPERATURE

Pin DIAG becomes LOW if the junction temperature (T_j) exceeds 150 °C. Pin DIAG becomes HIGH again if T_j is dropped to approximately 130 °C, so there is a hysteresis of approximately 20 °C.

8.2.2 MAXIMUM CURRENT

When the loudspeaker terminals are short-circuited this will be detected by the current protection. Pin DIAG becomes LOW if the output current exceeds the maximum output current of 2 A. Pin DIAG becomes HIGH again if the output current drops below 2 A. The output current is limited at the maximum current detection level when pin DIAG is connected to pins EN1 and EN2.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rate System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	±30	V
$V_{P(sc)}$	supply voltage for short-circuits across the load		–	±30	V
I_{ORM}	repetitive peak current in output pins		–	2	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
$V_{esd(HBM)}$	electrostatic discharge voltage (HBM)	note 1			
		all pins with respect to V_{DD} (class 1a)	–500	+500	V
		all pins with respect to V_{SS} (class 1a)	–1500	+1500	V
		all pins with respect to each other (class 1a)	–1500	+1500	V
$V_{esd(MM)}$	electrostatic discharge voltage (MM)	note 2			
		all pins with respect to V_{DD} (class B)	–250	+250	V
		all pins with respect to V_{SS} (class B)	–250	+250	V
		all pins with respect to each other (class B)	–250	+250	V

Notes

1. Human Body Model (HBM); R_s = 1500 Ω; C = 100 pF.
2. Machine Model (MM); R_s = 10 Ω; C = 200 pF; L = 0.75 μH.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air	1.5	K/W

11 QUALITY SPECIFICATION

In accordance with *“SNW-FQ611”* if this device is used as an audio amplifier.

12 DC CHARACTERISTICS

V_P = ±12.5 V; T_{amb} = 25 °C; measured in test diagram of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		±7.5	±12.5	±30	V
$I_{q(tot)}$	total quiescent current	no load connected	–	25	45	mA
		outputs floating	–	5	10	mA
Internal stabilizer logic supply (pin STAB)						
$V_{O(STAB)}$	stabilizer output voltage	referenced to V_{SS}	11.7	13	14.3	V
Switch inputs (pins SW1 and SW2)						
V_{IH}	HIGH-level input voltage	referenced to V_{SS}	10	–	15	V
V_{IL}	LOW-level input voltage	referenced to V_{SS}	0	–	2	V
Control outputs (pins REL1 and REL2)						
V_{OH}	HIGH-level output voltage	referenced to V_{SS}	10	–	15	V
V_{OL}	LOW-level output voltage	referenced to V_{SS}	0	–	2	V
Diagnostic output (pin DIAG, open-drain)						
V_{OL}	LOW-level output voltage	I_{DIAG} = 1 mA; note 1	0	–	1.0	V
I_{LO}	output leakage current	no error condition	–	–	50	µA
Enable inputs (pins EN1 and EN2)						
V_{IH}	HIGH-level input voltage	referenced to V_{SS}	9	–	15	V
V_{IL}	LOW-level input voltage	referenced to V_{SS}	0	5	–	V
$V_{EN(hys)}$	hysteresis voltage		–	4	–	V
$I_{I(EN)}$	input current		–	–	300	µA
Switching-on input (pin POWERUP)						
$V_{POWERUP}$	operating voltage	referenced to V_{SS}	5	–	12	V
$I_{I(POWERUP)}$	input current	$V_{POWERUP}$ = 12 V	–	100	170	µA
Temperature protection						
T_{diag}	temperature activating diagnostic	$V_{DIAG} = V_{DIAG(LOW)}$	150	–	–	°C
T_{hys}	hysteresis on temperature diagnostic	$V_{DIAG} = V_{DIAG(LOW)}$	–	20	–	°C
Current protection						
$I_{O(ocpl)}$	overcurrent protection level		–	2.1	–	A

Note

1. Temperature sensor or maximum current sensor activated.

13 AC CHARACTERISTICS

$V_P = \pm 12.5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Single-ended application; note 1						
P_o	output power	$R_L = 8\ \Omega$				
		THD = 0.5 %	7[2]	8	–	W
		THD = 10 %	9[2]	10	–	W
		$R_L = 16\ \Omega$				
		THD = 0.5 %	–	4	–	W
		THD = 10 %	–	5	–	W
THD	total harmonic distortion	$P_o = 1$ W; note 3				
		$f_i = 1$ kHz	–	0.05	0.1	%
		$f_i = 10$ kHz	–	0.2	–	%
η	efficiency endstage	$P_o = 2 \times 10$ W; $f_i = 1$ kHz; note 4	–	90	–	%

Notes

1. $V_P = \pm 12.5$ V; $R_L = 8\ \Omega$; $f_i = 1$ kHz; $f_{osc} = 310$ kHz; $R_s = 0.1\ \Omega$ (series resistance of filter coil); $T_{amb} = 25$ °C; measured in reference design (SE application) shown in Fig.5; unless otherwise specified.
2. Indirectly measured; based on $R_{ds(on)}$ measurement.
3. Total Harmonic Distortion (THD) is measured in a bandwidth of 22 Hz to 20 kHz (AES 17 brickwall filter). When distortion is measured using a low-order low-pass filter a significantly higher value will be found, due to the switching frequency outside the audio band. Measured using the typical application circuit, given in Fig.5.
4. Efficiency for power stage.

14 SWITCHING CHARACTERISTICS

$V_P = \pm 12.5$ V; $T_{amb} = 25$ °C; measured in Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PWM outputs (pins OUT1 and OUT2); see Fig.3						
t_r	rise time		–	30	–	ns
t_f	fall time		–	30	–	ns
t_{blank}	blanking time		–	70	–	ns
t_{PD}	propagation delay	from pin SW1 (SW2) to pin OUT1 (OUT2)	–	200	–	ns
$t_{W(min)}$	minimum pulse width		–	220	270	ns
$R_{ds(on)}$	on-resistance of the output transistors		–	0.2	0.4	Ω

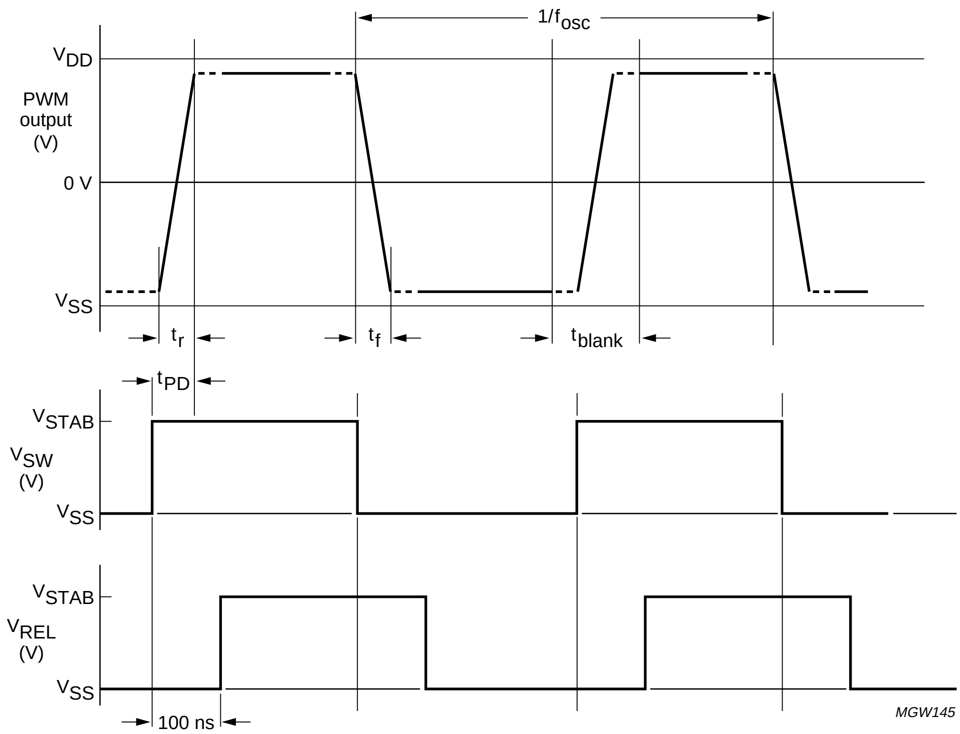


Fig.3 Timing diagram PWM output, switch and release signals.

15 TEST AND APPLICATION INFORMATION

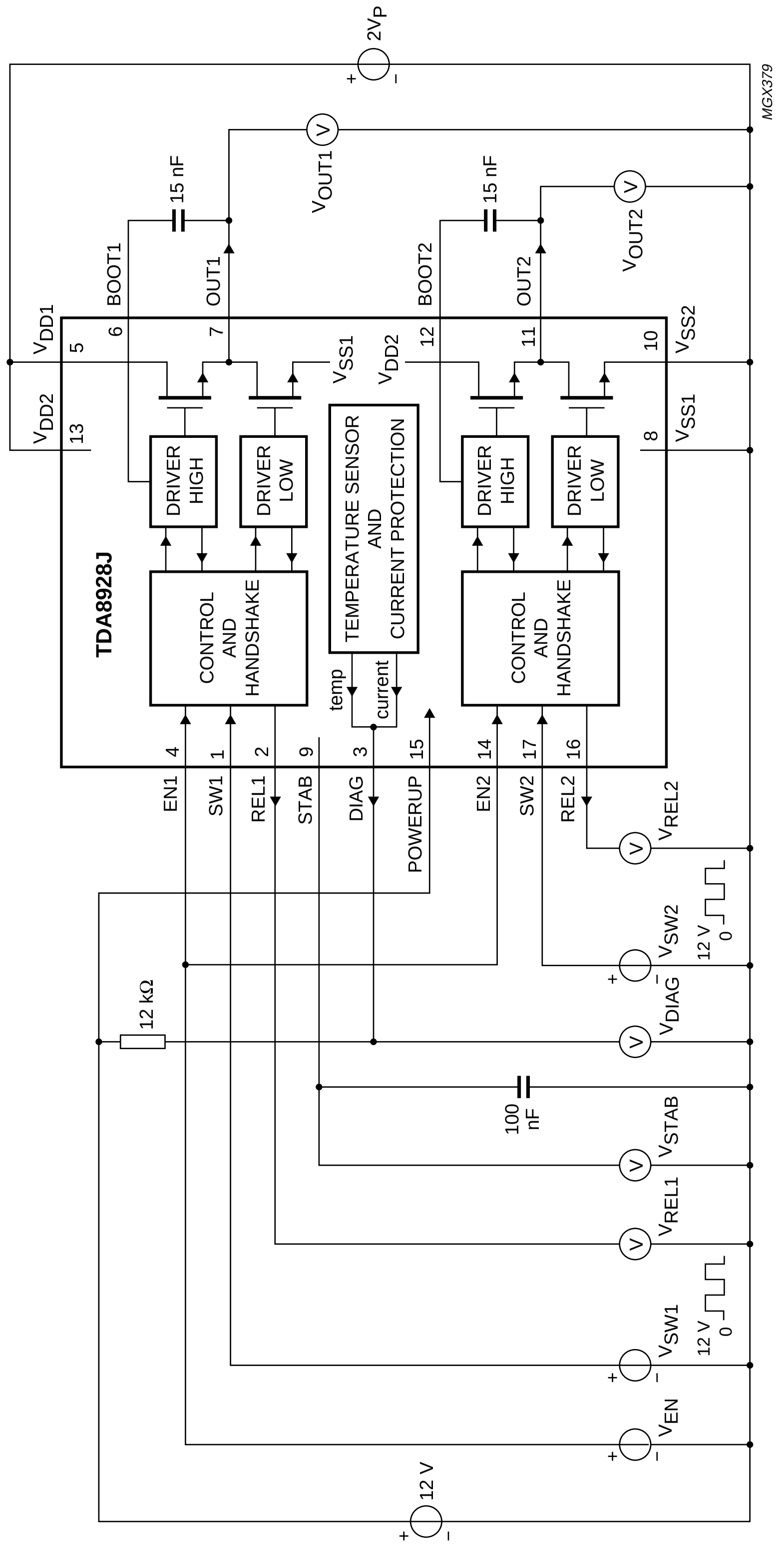


Fig.4 Test diagram.

15.1 SE application

For a SE application the application diagram as shown in Fig.5 can be used.

15.2 Package ground connection

The heatsink of the TDA8928J is connected internally to V_{SS}.

15.3 Output power

The output power in SE self oscillating class-D applications can be estimated using the formula

$$P_{o(1\%)} = \frac{\left[\frac{R_L}{(R_L + R_{ds(on)} + R_s)} \times V_P\right]^2}{2 \times R_L}$$

The maximum current $I_{O(max)} = \frac{[V_P]}{R_L + R_{ds(on)} + R_s}$ should not exceed 2 A.

Where:

R_L = load impedance

R_s = series resistance of filter coil

$P_{o(1\%)}$ = output power just at clipping.

The output power at THD = 10 %: $P_{o(10\%)} = 1.25 \times P_{o(1\%)}$.

15.4 Reference design

The reference design for a self oscillating class-D system for the TDA8928J is shown in Fig.5. The Printed-Circuit Board (PCB) layout is shown in Figs 6, 7 and 8. The bill of materials is given in Section 15.4.2.

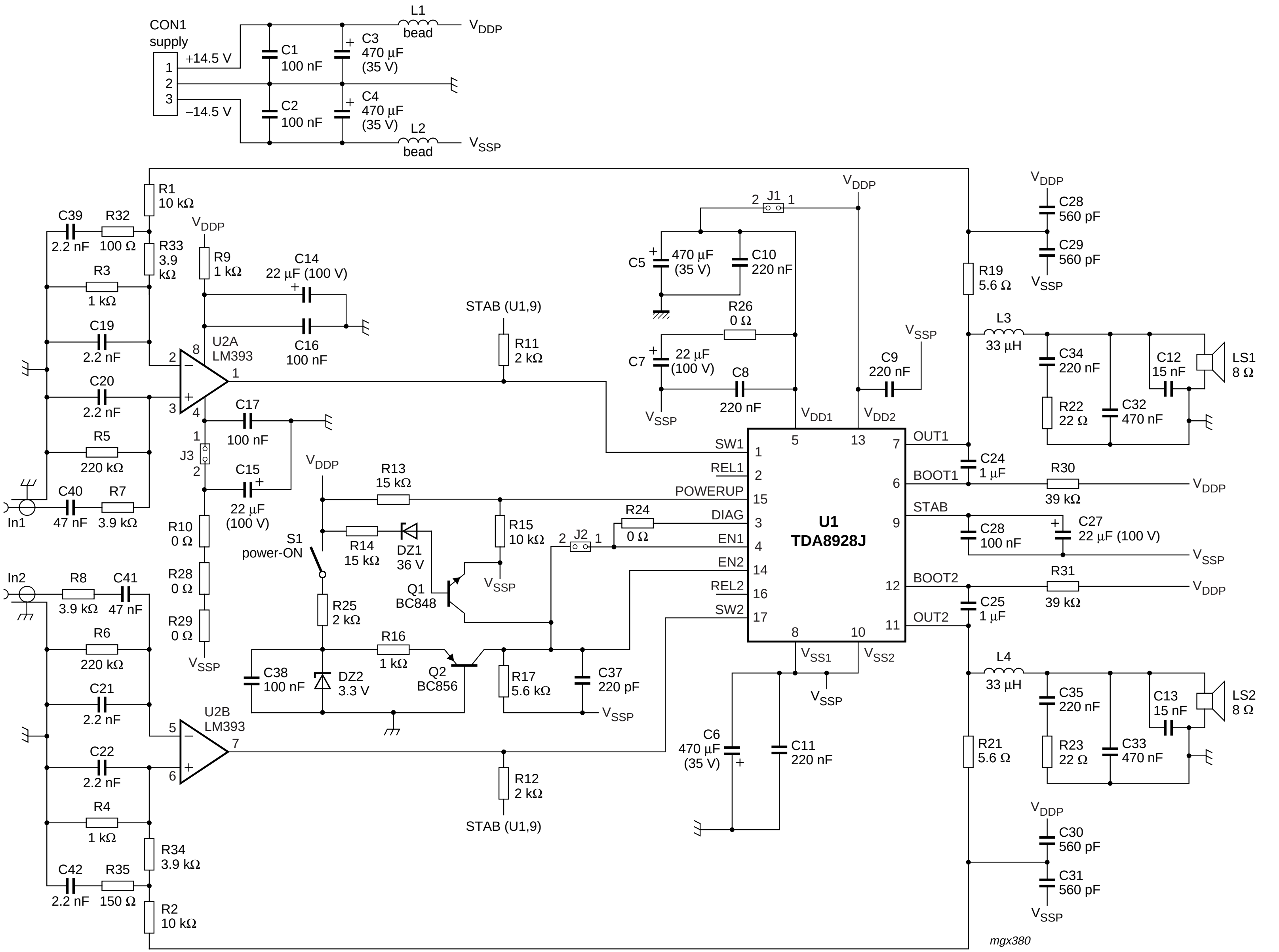
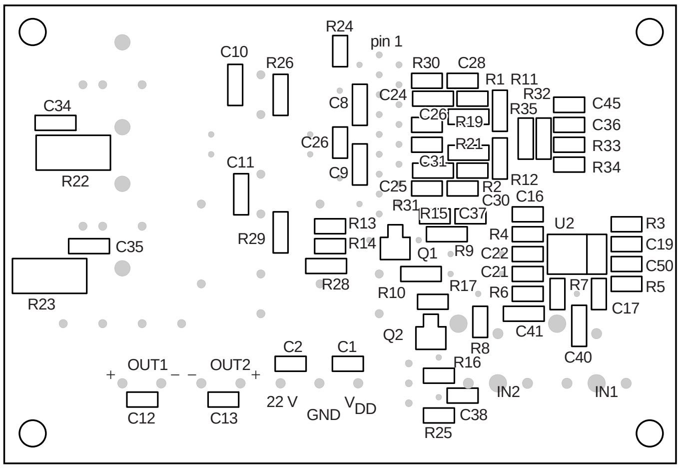


Fig.5 Single-ended self oscillating class-D system application diagram for TDA8928J.

15.4.1 PRINTED-CIRCUIT BOARD

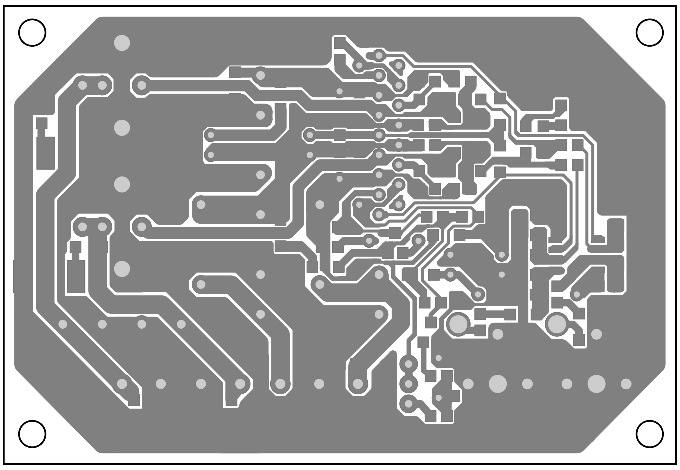
The printed-circuit board dimensions are 8.636 × 5.842 cm; single-sided copper of 35 µm; silk screen on both sides; 79 holes; 94 components (32 resistors and 41 capacitors).



Bottom silk

MDB615

Fig.6 Printed-circuit board (bottom silk) layout for TDA8928J.



Bottom copper

MDB617

Fig.7 Printed-circuit board (bottom copper) layout for TDA8928J.

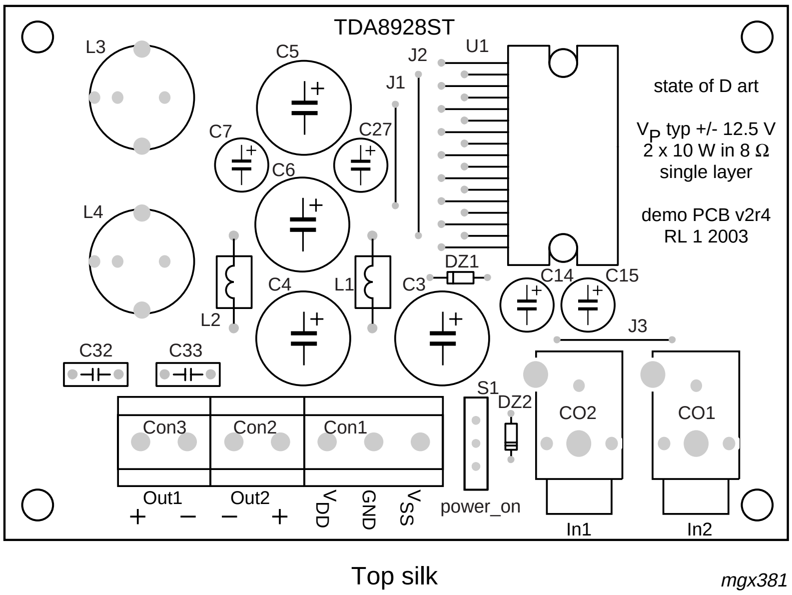


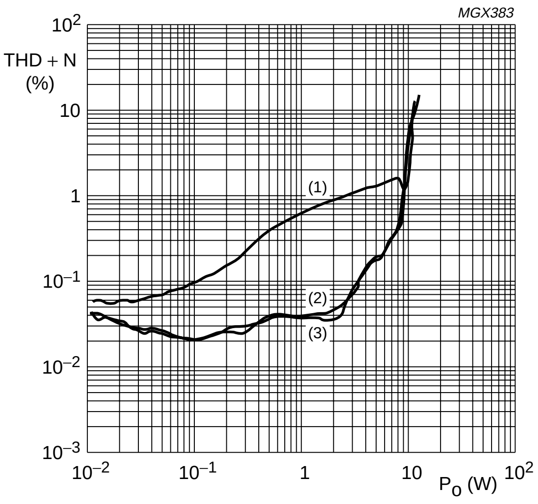
Fig.8 Printed-circuit board (top silk) layout for TDA8928ST.

15.4.2 BILL OF MATERIALS

COMPONENT	DESCRIPTION	TYPE	COMMENTS
U1	TDA8928ST	Philips Semiconductors, SOT577-2	
U2	LM393AD	National, SO8	alternatives: TI semiconductors and On semiconductors
DZ1	36 V Zener diode	BZX-79C36V, DO-35	used as jumper
DZ2	3.3 V Zener diode	BZX-79C3V3, DO-35	used as jumper, optional
Q1	BC848 transistor	NPN, SOT23	
Q2	BC856 transistor	PNP, SOT23	
L1, L2	bead	Murata BL01RN1-A62	used as jumper
L3, L4	33 µH coil	Toko 11RHBP-330M ws	totally shielded
S1	power-on switch	PCB switch, SACME 09-03290-01	optional
Con1	V_{SS}, GND, V_{DD} connector	Augat 5KEV-03	optional
Con2, Con3	Out2, Out1 connector	Augat 5KEV-02	optional
CO1, CO2	In1, In2 connector	Cinch Farnell 152-396	optional
J1, J2, J3	wire	Jumpers, D = 0.5 mm	
Capacitors			
C37	220 pF, 50 V	SMD0805	
C28, C29, C30, C31	560 pF, 100 V	SMD0805	50 V is OK

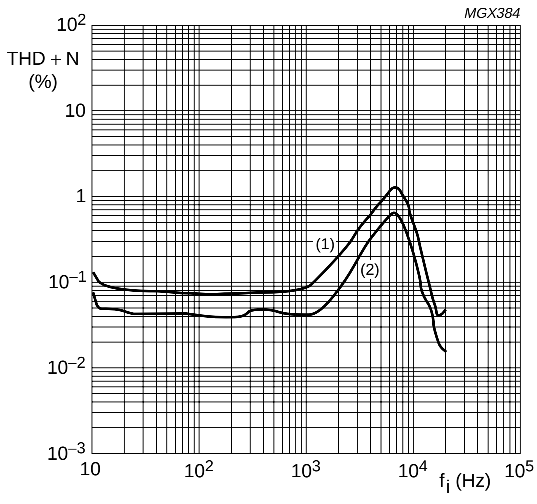
COMPONENT	DESCRIPTION	TYPE	COMMENTS
C19, C20, C21, C22, C39, C42	2.2 nF, 50 V	SMD0805	
C12, C13	15 nF, 50 V	SMD0805	
C40, C41	47 nF, 50 V	SMD1206	
C1, C2, C16, C17, C26, C38	100 nF, 50 V	SMD0805	
C8, C9, C10, C11, C34, C35	220 nF, 50 V	SMD1206	C8 to C11 used as jumper
C32, C33	470 nF, 63 V	MKT	
C24, C25	1 μF, 16 V	SMD1206	1206 due to supply range
C7, C14, C15, C27	22 μF, 100 V	Panasonic NHG Series ECA1JHG220	63 V is OK
C3, C4, C5, C6	470 μF, 35 V	Panasonic M Series ECA1VM471	
C18, C23, C36	these capacitors have been removed		
Resistors			
R10, R26, R28, R29	0 Ω	SMD1206	used as jumpers
R24	0 Ω	SMD0805	short-circuited in a new printed-circuit board layout
R19, R21	5.6 Ω, 0.25 W	SMD1206	1206 due to dissipation
R22, R23	22 Ω, 1 W	SMD2512	2512 due to dissipation
R35	150 Ω	SMD1206	used as jumper
R32	100 Ω	SMD1206	used as jumper
R9	1 kΩ	SMD1206	used as jumper
R3, R4, R16	1 kΩ	SMD0805	
R11, R12	2 kΩ	SMD1206	used as jumpers
R25	2 kΩ	SMD0805	
R7, R8, R33, R34	3.9 kΩ	SMD0805	
R17	5.6 kΩ	SMD0805	
R1, R2, R15	10 kΩ	SMD0805	
R13, R14	15 kΩ	SMD0805	
R30, R31	39 kΩ	SMD0805	
R5, R6	220 kΩ	SMD0805	
R18, R20, R27	these resistors have been removed		

15.5 Curves measured in reference design



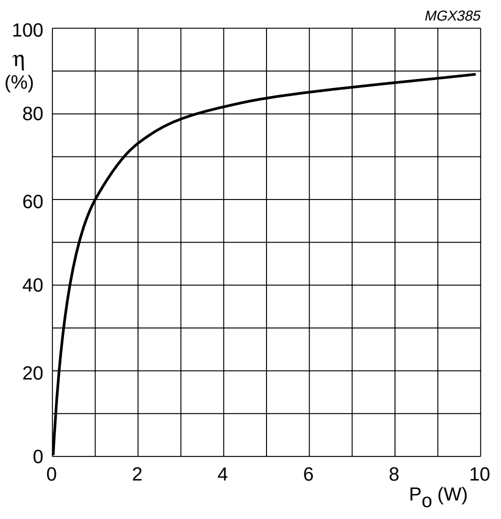
2 × 8 Ω SE; V_P = ±12.5 V.
(1) 6 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.9 THD + N as function of output power.



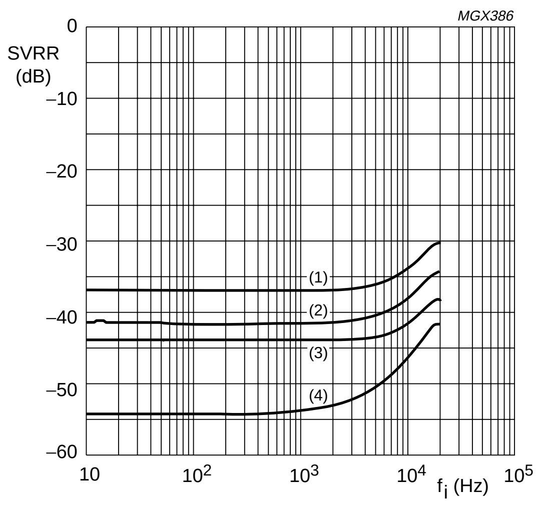
2 × 8 Ω SE; V_P = ±12.5 V.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.10 THD + N as function of frequency.



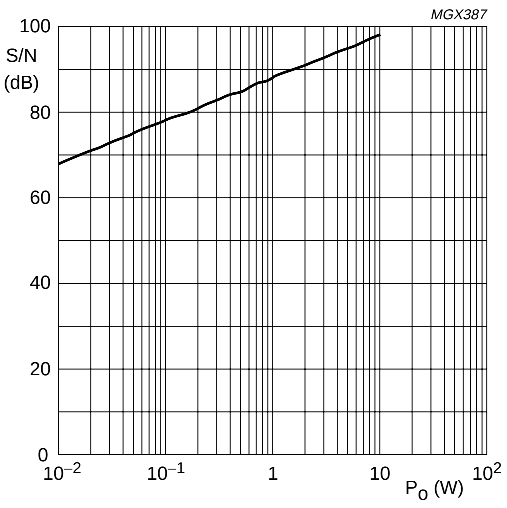
2 × 8 Ω SE; V_P = ±12.5 V; f_i = 1 kHz.

Fig.11 Efficiency as function of output power.



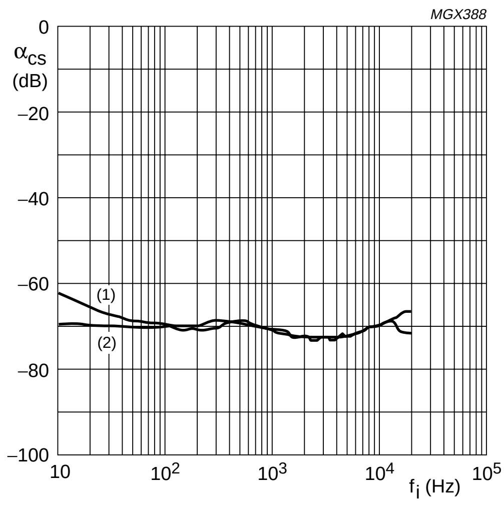
V_P = ±12.5 V; $V_{ripple(p-p)}$ = 2 V.
(1) Both supply lines in phase.
(2) One supply line (V_{SS}) rippled.
(3) One supply line (V_{DD}) rippled.
(4) Both supply lines in antiphase.

Fig.12 SVRR as function of frequency.



$2 \times 8\ \Omega$ SE; $V_P = \pm 12.5$ V.

Fig.13 S/N as function of output power.

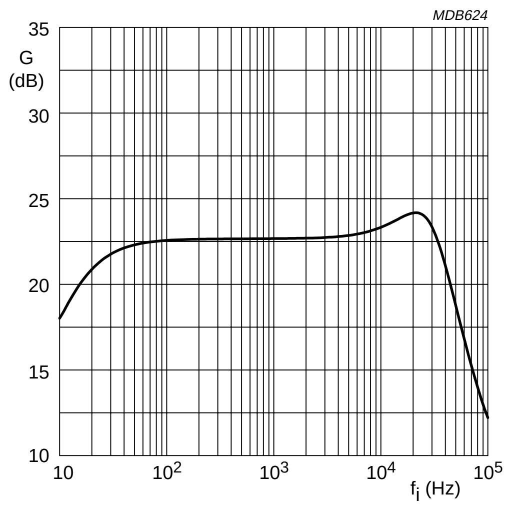


$2 \times 8\ \Omega$ SE; $V_P = \pm 12.5$ V.

(1) $P_o = 1$ W.

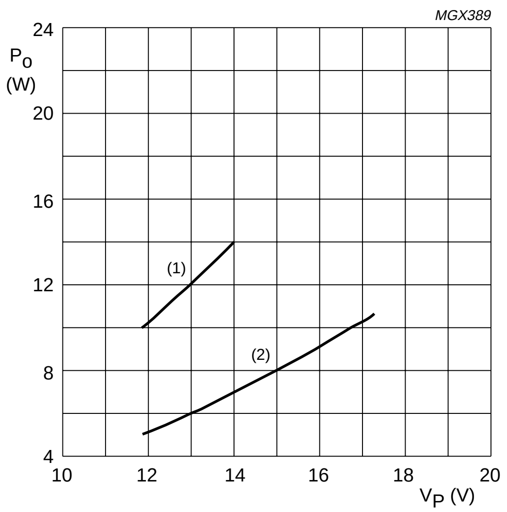
(2) $P_o = 10$ W.

Fig.14 Channel separation as function of frequency.



$2 \times 8\ \Omega$ SE; $V_P = \pm 12.5$ V; $V_i = 100$ mV.

Fig.15 Gain as function of frequency.



THD + N = 10 %; $f_i = 1$ kHz.

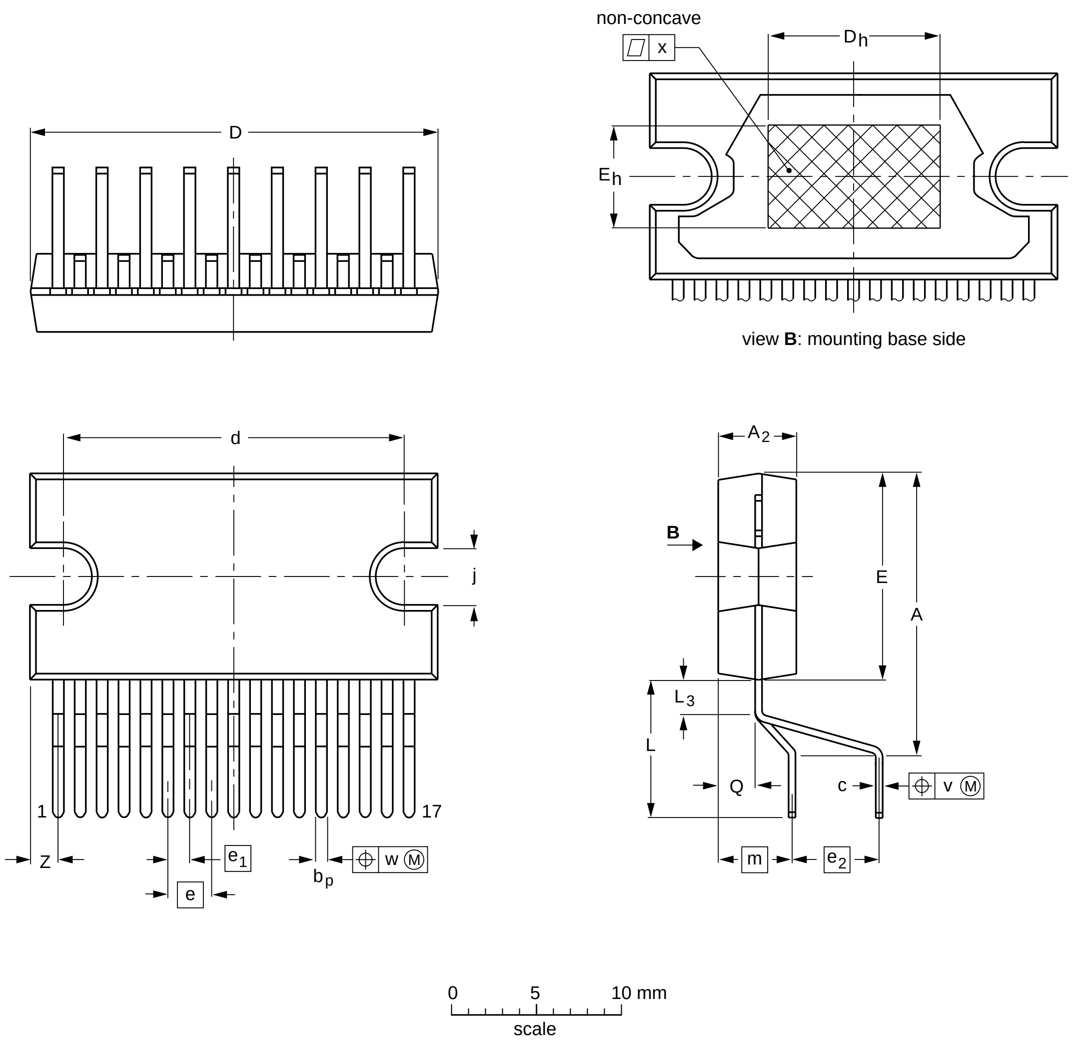
(1) $2 \times 8\ \Omega$ SE.

(2) $2 \times 16\ \Omega$ SE.

Fig.16 Output power as function of supply voltage.

16 PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 7.7 mm) SOT243-3



DIMENSIONS (mm are the original dimensions)

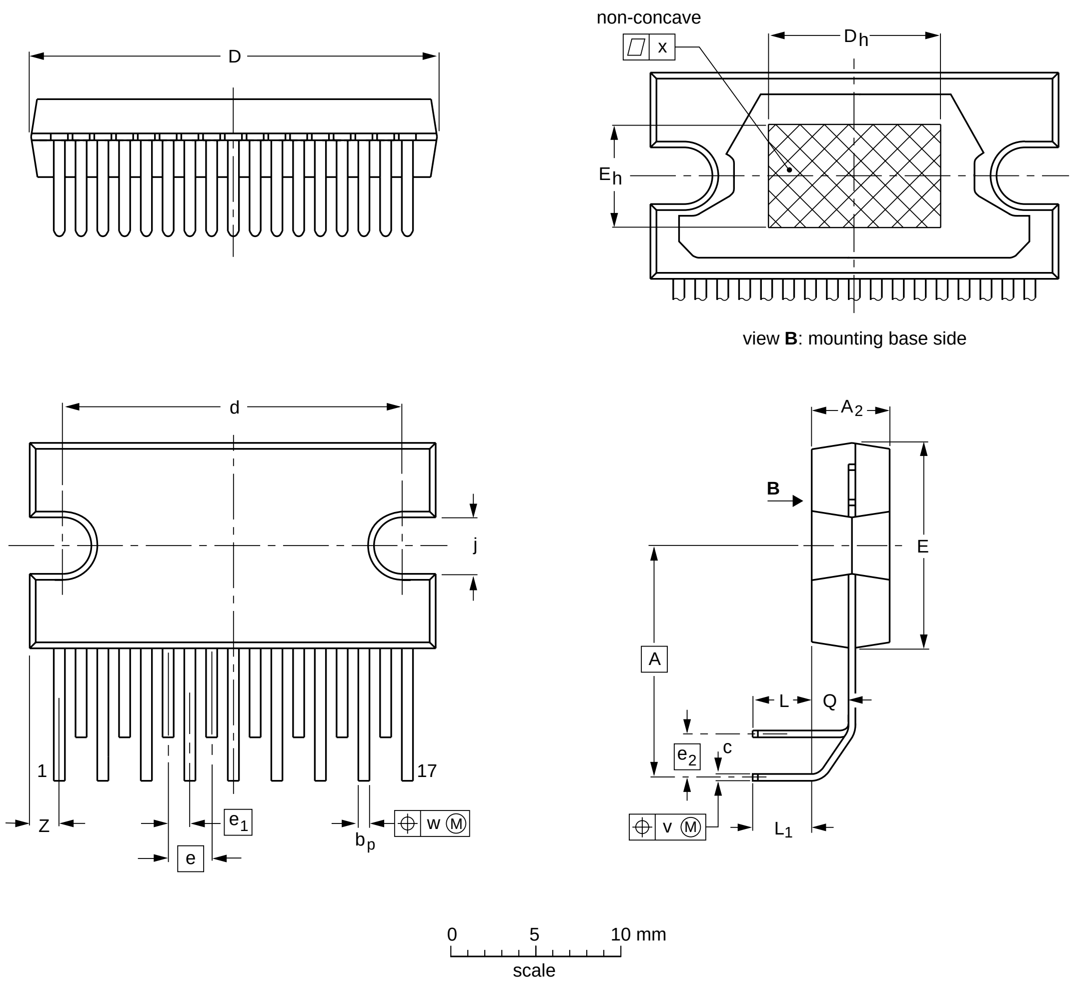
UNIT	A	A_2	b_p	c	D[(1)]	d	D_h	E[(1)]	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	Z[(1)]
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT243-3						~~99-12-17~~ 03-03-12

RDBS17P: plastic rectangular-DIL-bent-SIL power package; 17 leads (row spacing 2.54 mm) **SOT577-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_1	Q	v	w	x	$Z^{(1)}$
mm	13.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	2.54	6	3.4 3.1	3.75 3.15	3.75 3.15	2.1 1.8	0.6	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT577-2						~~01-01-05~~ 03-03-12

17 SOLDERING

17.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

17.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

17.4 Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
CPGA, HCPGA	–	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable(1)
PMFP(2)	–	not suitable

Notes

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
2. For PMFP packages hot bar soldering or manual soldering is suitable.

18 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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