Application Report
SLLA032

# TNETE2201 EVM Kit Setup and Usage

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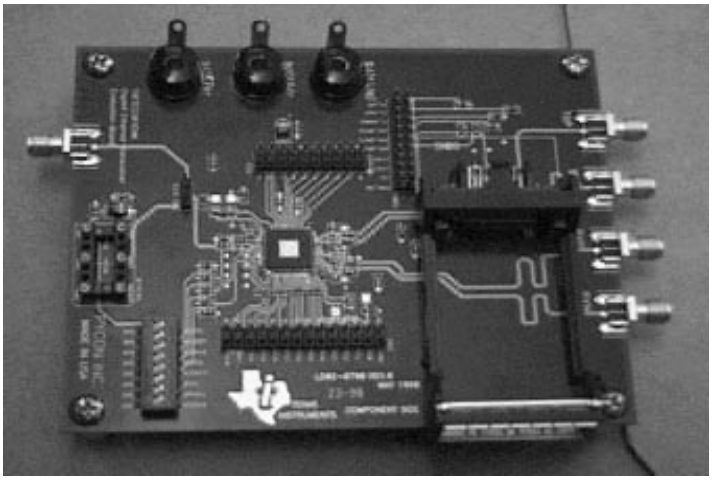
## Abstract

The Texas Instruments (TI™) TNETE2201 EVM (evaluation module) kit is a tool used to evaluate and design high-speed prototypes using the TNETE2201 Ethernet Transceiver IC (10 mm x 10 mm TQFP plastic package). The EVM kit is used to evaluate device parameters while acting as a guide for high-speed board layout. The high-speed interface is selectable between a 50-Ω SMA connector and a GBIC standard interface. The GBIC standard also provides a 75-Ω copper interface module and various fiber optic options. Overall, the designer can use the EVM kit as a tool for successful evaluation and design of an end product.



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# Introduction

The TNETE2201 EVM kit can act as a daughter board that plugs into new or existing designs. By providing the appropriate cabling, the EVM kit can interface with just about any test equipment or other reference designs. The EVM kit's high-speed serial interface can use either the GBIC (Gigabit Interface Converter) standard interface or a 50-ohm SMA connection. In addition, the GBIC specification allows the designer to choose either a 75-ohm copper module or a selection of fiber-optics modules.

As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled for both 50-ohm and 75-ohm high-speed transmission lines. In addition, the 50-ohm impedance mismatches are reduced by designing the component pad size to be as close as possible to the width of the connecting transmission line. Vias are minimized and, when necessary, placed as close as possible to the device drivers. Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission line effects are crucial when designing high-speed boards.

Some of the advanced features offered by the EVM kit include:

- PCB (printed circuit board) designed for speeds in excess of 1.25 Gbps
- Flexible—The EVM can be configured to operate with multiple device types and with copper or fiber interfaces.
- Integrated GBIC Interface eliminates the need for two boards.
- All input/output signals are accessible for rapid prototyping.
- Clock input is selectable for either 8/14 pin crystal or external clock input.
- Power can be supplied either by banana jacks or a 20-pin connector.
- Series terminated parallel outputs

# Board Layout and Configuration

The TNETE2201 EVM kit is designed to give the developer many options for operation. Many of these options are selectable by DIP switch and others may require board component removal or additions. The following sections provide guidelines to configure the EVM kit for different modes of operation.

The EVM kit is normally delivered in a default configuration that requires external clock and data inputs. The high-speed serial input and output are routed through the 50-ohm transmission line path. The GBIC interface is not connected and would require some resistor modifications to be functional. The default setup is useful for testing the board and interface IC. The designer might consider testing the bit error rate, jitter, and eye-diagram characteristics of the system. The TNETE2201 EVM is shipped with certain components installed for default operation. Table 1 lists the default configuration.

*Table 1. Default Setup as Shipped*

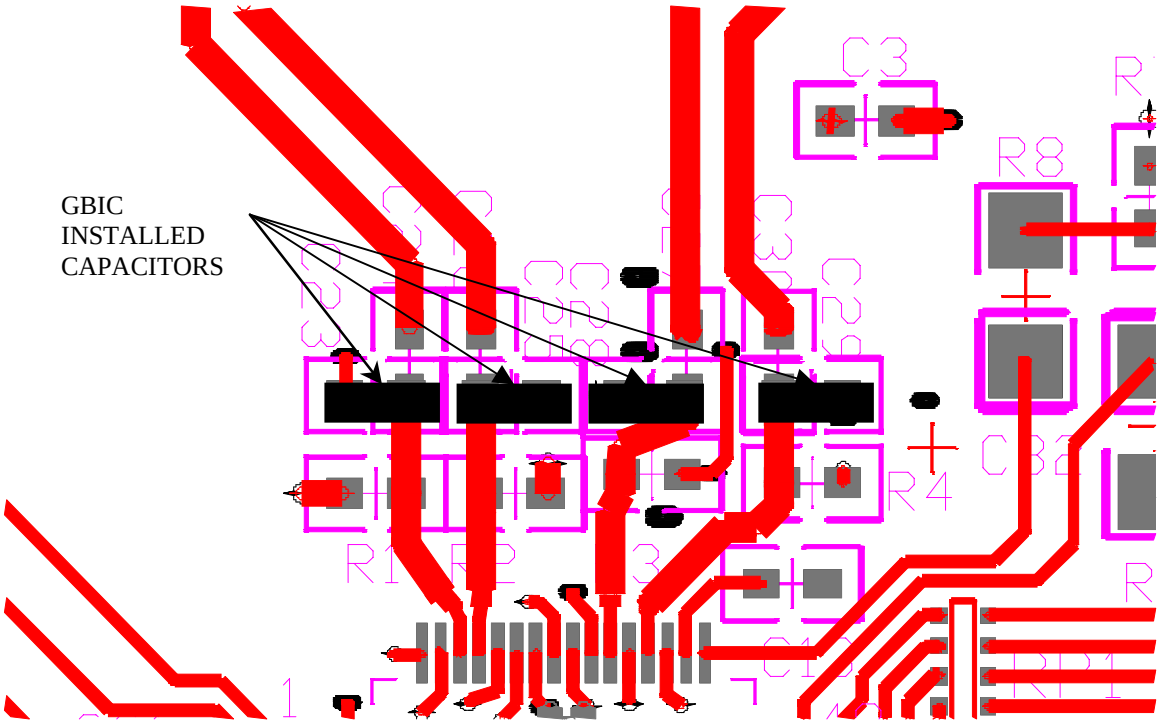
| Designator | Function | Condition (TNETE2201) |
|---|---|---|
| P5 | CLK SEL | Jumper installed between Pins 2 and 3 |
| R1 | TX Termination | 200 ohm installed |
| R2 | TX Termination | 200 ohm installed |
| R5 | Bias Net | 365 ohm installed |
| R6 | Bias Net | 562 ohm installed |
| R8 | WIZ OPTION | Not installed |
| R9 | WIZ OPTION | Not installed |
| R16 | CAP OPTION | Zero ohm installed |
| R17 | Bias Net | Not installed |
| R21 | WIZ OPTION | Not installed |
| R22 | WIZ OPTION | Not installed |
| C13 | Vcc Decouple | 0.01 µF installed |
| C23 | GBIC OPTION | Not installed |
| C24 | SMA OPTION | 0.01 µF installed |
| C25 | GBIC OPTION | Not installed |
| C26 | SMA OPTION | 0.01 µF installed |
| C27 | SMA OPTION | 0.01 µF installed |
| C28 | GBIC OPTION | Not installed |
| C29 | GBIC OPTION | Not installed |
| C30 | SMA OPTION | 0.01 µF installed |
| C31 | RX Termination | 0.01 µF installed |
| C32 | TX PLL Cap | 0.0022 µF installed |
| C33 | REF CLK Bias Net | Zero 0hm installed |
| C34 | TX PLL Cap | 0.0022 µF installed |
| L1 | Filter/Bias | Ferrite installed |
| X1 | OSC | Not installed (not provided) |
| DIP1-1 | PRBSEN | X (OFF) |
| DIP1-2 | TXRRAMP | X (OFF) |
| DIP1-3 | TXDIR | X (OFF) |

| Designator | Function | Condition (TNETE2201) |
|---|---|---|
| DIP1-4 | LCKREFN | X (OFF) |
| DIP1-5 | TESTEN | ON |
| DIP1-6 | SYNCEN | X (OFF) |
| DIP1-7 | LOOPEN | ON |
| DIP1-8 | CLKEN | X (OFF) |

Note: X is a don't care state (default position).

The GBIC Configuration requires a modification of the steering capacitors C23 through C30. This requires removing C24, C26, C27, and C30 and soldering these capacitors in locations C23, C25, C28, and C29 (see Figure 1).

*Figure 1. GBIC Setup Modifications*




## Test Configuration and Results

The serial Bit Error-rate Ratio Test (BERT) is useful for evaluating device and board characteristics. Using this test, we can determine the eye diagram characteristics of the system, as shown in Figure 3. The test setup is illustrated in Figure 2.

The HP71603B 3-Gbps Serial BERT outputs a high-speed serial stream to the test board where the data is converted by the TNETE part to a 10-bit parallel format. The parallel data is then looped back from the receiver to the transmitter. The pulse generator provides a clock input to the transmitter. The external clock source is necessary because the receiver's recovered clock is half the frequency necessary for transmission.

Both the pulse generator and the BERT are synchronized with an external clock source. The operator adjusts the variable phase delay to ensure that the clock meets the setup and hold time of the data. The parallel data along with the clock is routed to the transmitter where the data is serialized and captured by the oscilloscope. Figure 3 shows an example eye diagram taken using this technique.

*Figure 2. Bit Error-Rate Ratio Test Configuration*

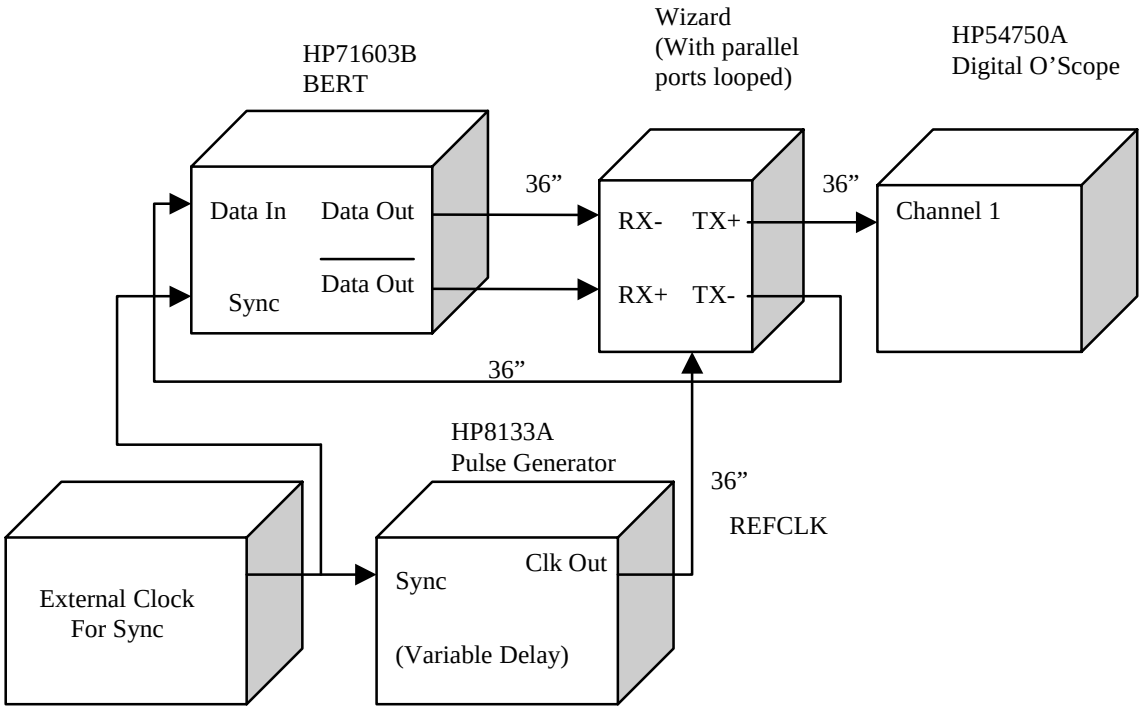
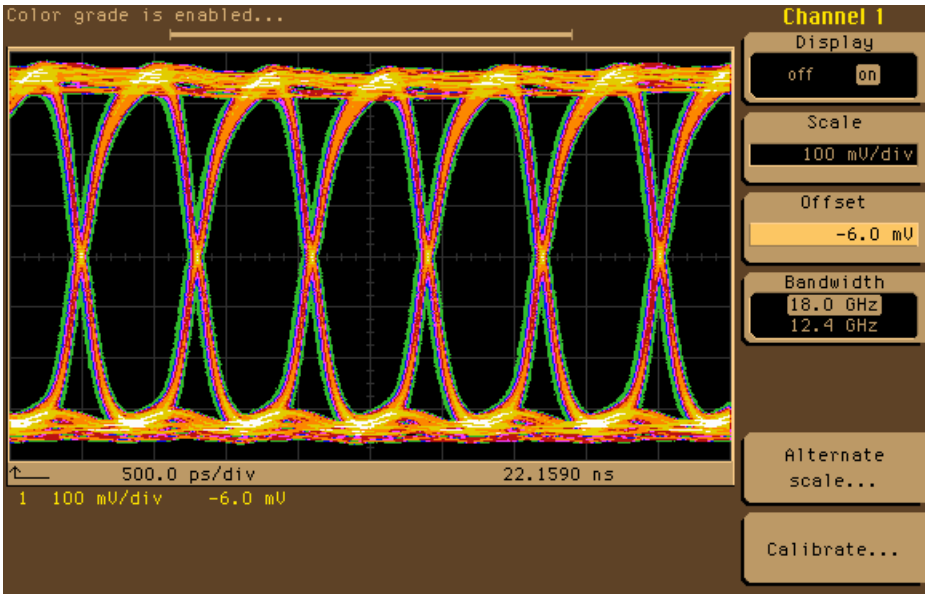



*Figure 3. Eye Diagrams of High-Speed Serial Outputs*



# Board Layouts, Schematics, and Bill of Materials

| SYM | REVISIONS |
|---|---|
| A | ECNXXXXXX, 00/00/9X,MPK |

NOTES:

1. All capacitors are 0.01 unless otherwise specified
2. Do not thermal relief the Banana Jack holes

| | | |
|---|---|---|
| DRAFTSMAN: BBarrie | DATE 03/04/98 | TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS — CODE IDENTITY NUMBER 01295 |
| DESIGNER: BBarrie | DATE 00/00/9X | TITLE: SCHEMATIC, TENETE2201 EVM BOARD |
| CHECKER: ICHKDIT | DATE 00/00/9X | |
| ENGINEER: BBarrie | DATE 00/00/9X | |
| APPROVED: OK/W/ME | DATE 00/00/9X | |
| RELEASED: MIKE KORSON | DATE 00/00/9X | SCALE N — C SIZE — XXXXXXXX — A REV — SHEET 01/01 |

PAGE:01
03:29:22
07/10/98

07/10/98 15:29:30 Electronics Design System Page: 0001

Bill of Materials

<<<From Job: fcge>>>

01-31xxx-xxx

TEXAS INSTRUMENTS INCORPORATED

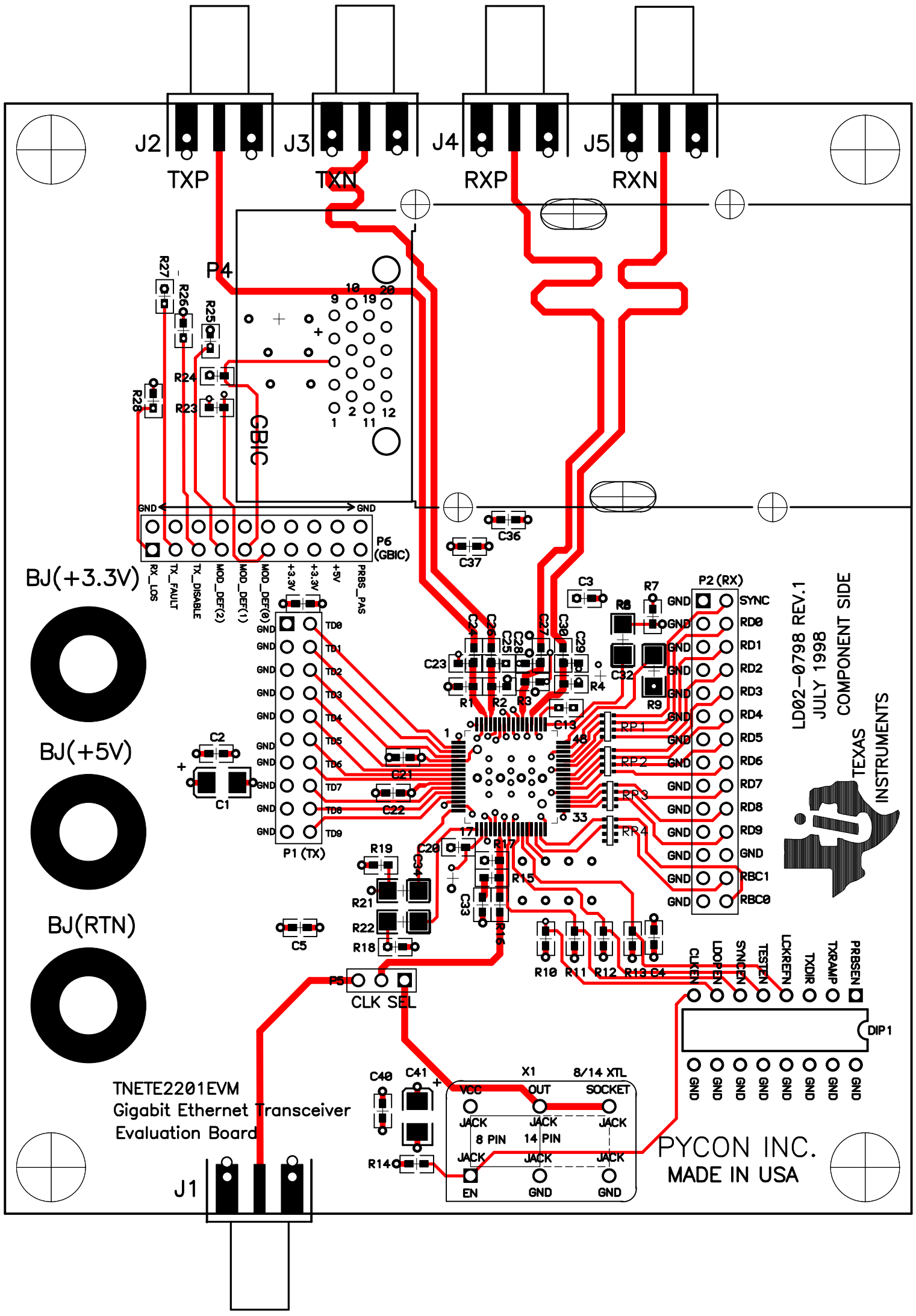
Mixed Signal Products

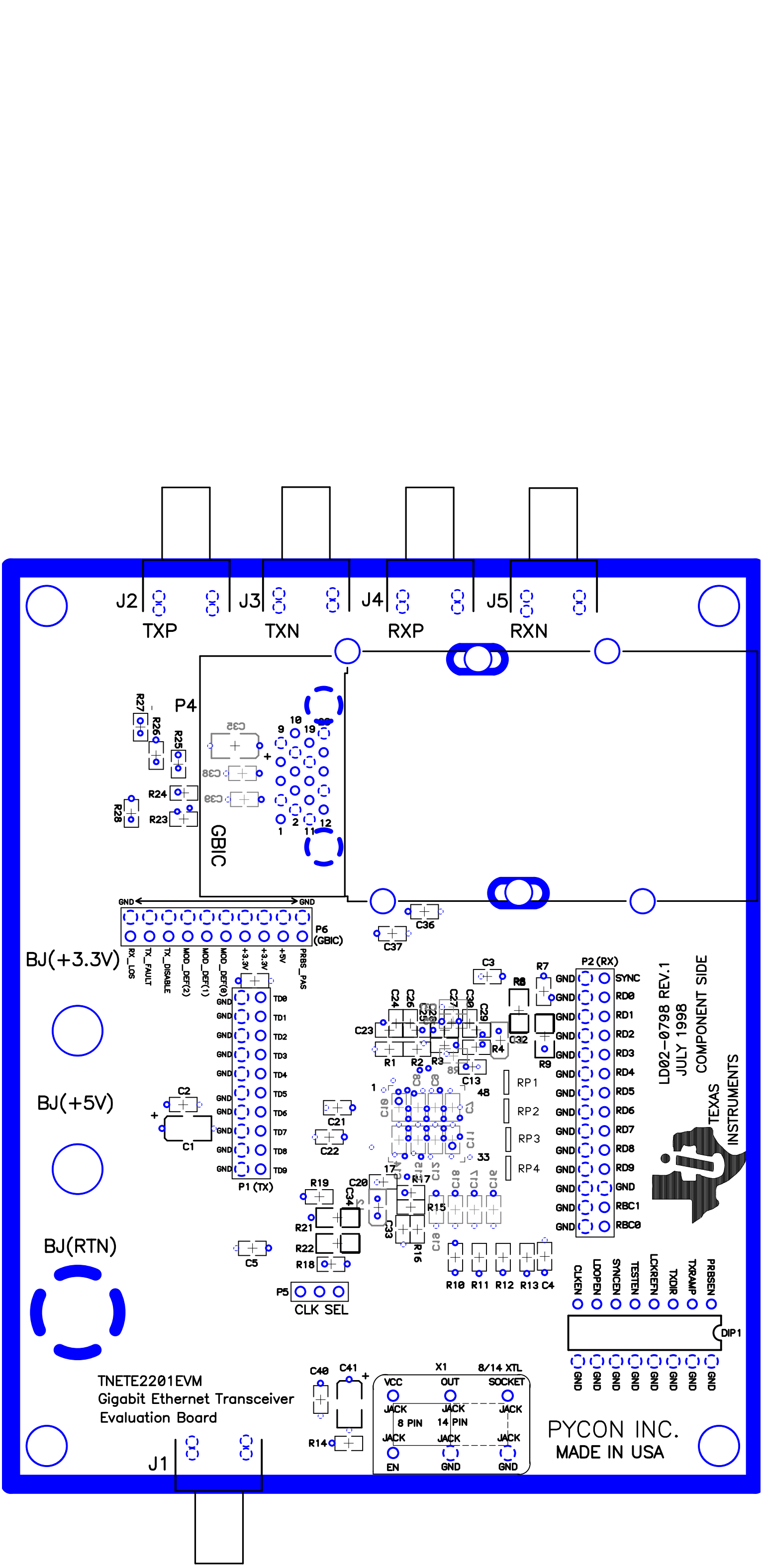
T.I. Internal Data ENGINEER: RELEASED:_____

| ITEM | QTY | MFG | MFG PART# | Ref Des | DESCRIPTION | VALUE or FUNCTION | SOCKET |
|---|---|---|---|---|---|---|---|
| 1 | 3 | PANASONIC | ECS-T1CX106R | C1,C35,C41 | CAPACITOR,TANT,SMT | 20%, 16V, 10uF | |
| 2 | 2 | AVX | 12061C222JATMA | C32,C34 | CAPACITOR,SMT1206 | 100V, 5%, 0.0022uF | |
| 3 | 35 | AVX | 06033G103JATMA | C2-C31,C36,C37 | CAPACITOR,SMT0603 | 25V,5%,0.01uF | |
| * | | | | C38-C40 | | | |
| 4 | 1 | AMP | 787653 | P4 | CONNECTOR,20PIN | RECEPT,R/A,20PIN,AMP | |
| 5 | 3 | CONCORD | 01-2520-3-044 | BJ(+5V) | CONNECTOR | BANANA,FEMALE,SWAGE MOUNT | |
| * | | | | BJ(RTN) | | | |
| * | | | | BJ(+3.3V) | | | |
| 6 | 5 | EFJOHNSON | 142-0701-801 | J1-J5 | CONNECTOR | SMA JACK,END LAUNCH,.062P | |
| 7 | 2 | MURATA ERIE | BLM21B03-PT | L1,L2 | FILTER,SMT0805 | FERRITE,6 OHMS@100MHz | |
| 8 | 2 | SAMTEC | TSW-110-07-G-D | P1,P6 | HEADER,2X10,.1CTRS | HEADER 2X 10 .1CTR | |
| 9 | 1 | SAMTEC | TSW-1-14-05-G-D | P2 | HEADER,MALE,2X14 | HEADER,MALE,2X14,.1CTRS | |
| 10 | 1 | ANY | HEADER,MALE,3PI | P5 | HEADER | MALE,3PIN,.100CC | |
| 11 | 1 | | DUT_PQFP_PJD64 | U1 | IC,TQFP,PJD,64PIN | DUT-USER DEFINED | |
| 12 | 3 | JUMPER | JUMPER-0603 | R16,R17 | JUMPER,SMT0603 | USER DEFINED JUMPER 0603 | |
| 13 | 1 | VARIES | OSC-COMBO-106.2 | X1 | OSCILLATOR,106.25MHz | OSC COMBO-106.25MHz | AMP/50935/X8 |
| 14 | 4 | | RES1206(UN) | R8,R9,R21,R22 | RESISTOR,SMT,1206 | UN-INST | |
| 15 | 4 | AVX/KYOCERA | CRA3A4E500GI | RP1-RP4 | RES,SMT,8PIN,50OHM | SERIES CHIP RES ARRAY SMT | |
| 16 | 14 | DALE | CRCW06034701F | R7,R10-R14,R18 | RESISTOR,SMT,1/16W,1 | 4.70K OHM | |
| * | | | | R19,R23,R24 | | | |
| * | | | | R25-R28 | | | |
| 17 | 3 | DALE | CRCW060349R9F | R3,R4,R15 | RESISTOR,SMT,0603 | 49.9 OHM | |
| 18 | 2 | DALE | CRCW0603200F | R1,R2 | RESISTOR,SMT,0603 | 200 OHM | |
| 19 | 1 | DALE | CRCW0603365F | R5 | RESISTOR,SMT,0603 | 365 OHM | |
| 20 | 1 | DALE | CRCW0603562F | R6 | RESISTOR,SMT,0603 | 562 OHM | |
| 21 | 1 | C&K | BD08 | DIP1 | SWITCH,SPST,DIP16 | SWITCH,16P,SPST X 8 | |

Total Part Count: 90

Total Parts Cost: 0


J2
TXP
J3
TXN
J4
RXP
J5
RXN
P4
GBIC
P6 (GBIC)
BJ(+3.3V)
BJ(+5V)
BJ(RTN)
P1 (TX)
P2 (RX)
P5
CLK SEL
DIP1
X1
8/14 XTL
SOCKET
8 PIN
14 PIN
TNETE2201EVM
Gigabit Ethernet Transceiver
Evaluation Board
J1
PYCON INC.
MADE IN USA
LD02-0798 REV.1
JULY 1998
COMPONENT SIDE
TEXAS INSTRUMENTS


J2
TXP
J3
TXN
J4
RXP
J5
RXN
P4
GBIC
P6 (GBIC)
GND
GND
RX_LOS
TX_FAULT
TX_DISABLE
MOD_DEF(2)
MOD_DEF(1)
MOD_DEF(0)
+3.3V
+3.3V
+5V
PRBS_PAS
BJ(+3.3V)
BJ(+5V)
BJ(RTN)
P1 (TX)
TD0
TD1
TD2
TD3
TD4
TD5
TD6
TD7
TD8
TD9
P2 (RX)
SYNC
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
RD8
RD9
RBC1
RBC0
RP1
RP2
RP3
RP4
P5
CLK SEL
CLKEN
LDOPEN
SYNCEN
TESTEN
LCKREFN
TXDIR
TXRAMP
PRBSEN
DIP1
X1
8/14 XTL
VCC
OUT
SOCKET
8 PIN
14 PIN
EN
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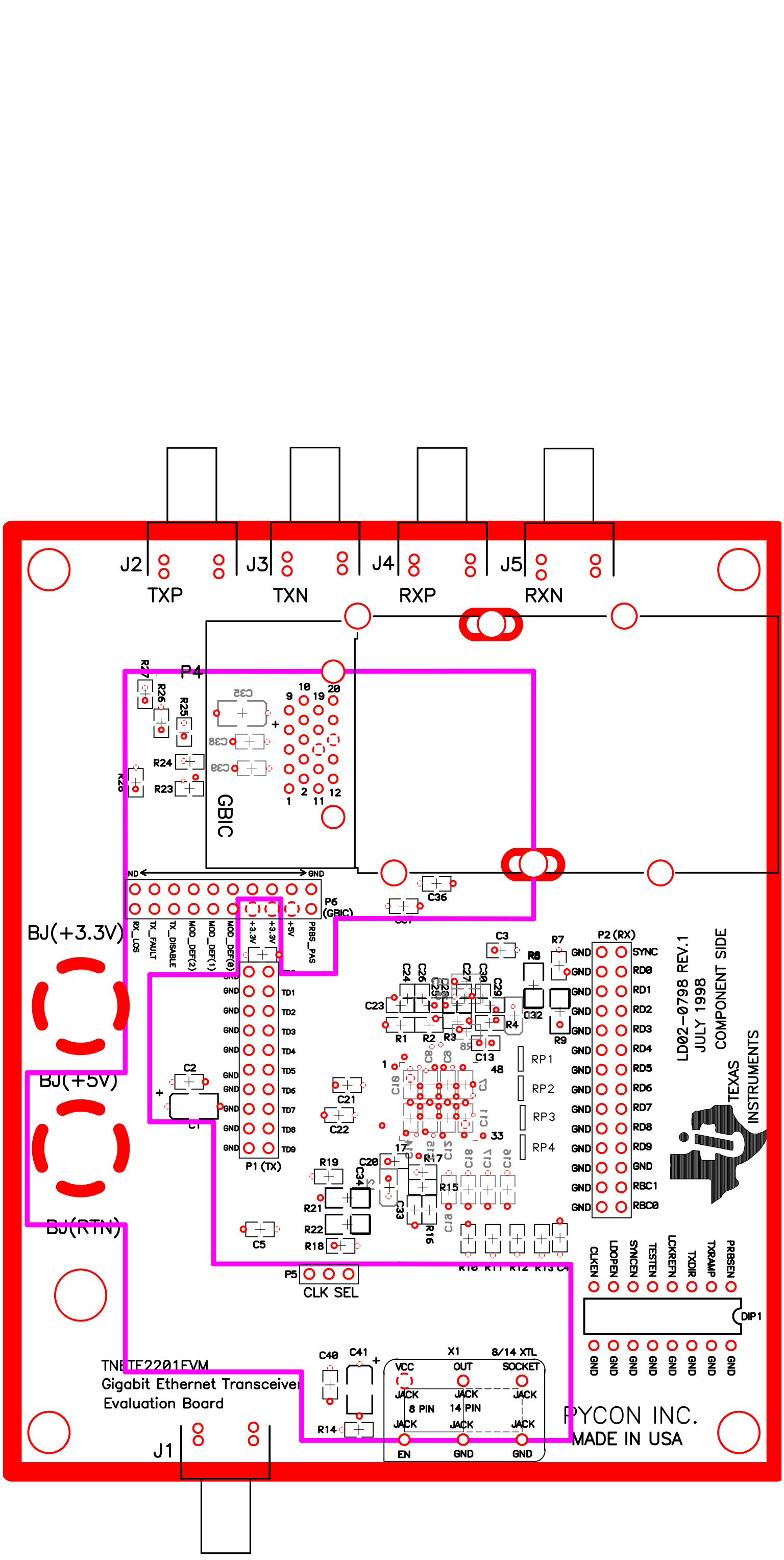
J2
TXP
J3
TXN
J4
RXP
J5
RXN
P4
GBIC
P6 (GBIC)
RX_LOS
TX_FAULT
TX_DISABLE
MOD_DEF(2)
MOD_DEF(1)
MOD_DEF(0)
+3.3V
+3.3V
+5V
PRBS_PAS
BJ(+3.3V)
BJ(+5V)
BJ(RTN)
P1 (TX)
TD1
TD2
TD3
TD4
TD5
TD6
TD7
TD8
TD9
P2 (RX)
SYNC
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
RD8
RD9
RBC1
RBC0
RP1
RP2
RP3
RP4
P5
CLK SEL
CLKEN
LDOPEN
SYNCEN
TESTEN
LCKREFN
TXDIR
TXAMP
PRBSEN
DIP1
X1
8/14 XTL
VCC
OUT
SOCKET
8 PIN
14 PIN
EN
J1
LD02-0798 REV.1
JULY 1998
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TEXAS INSTRUMENTS
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Evaluation Board
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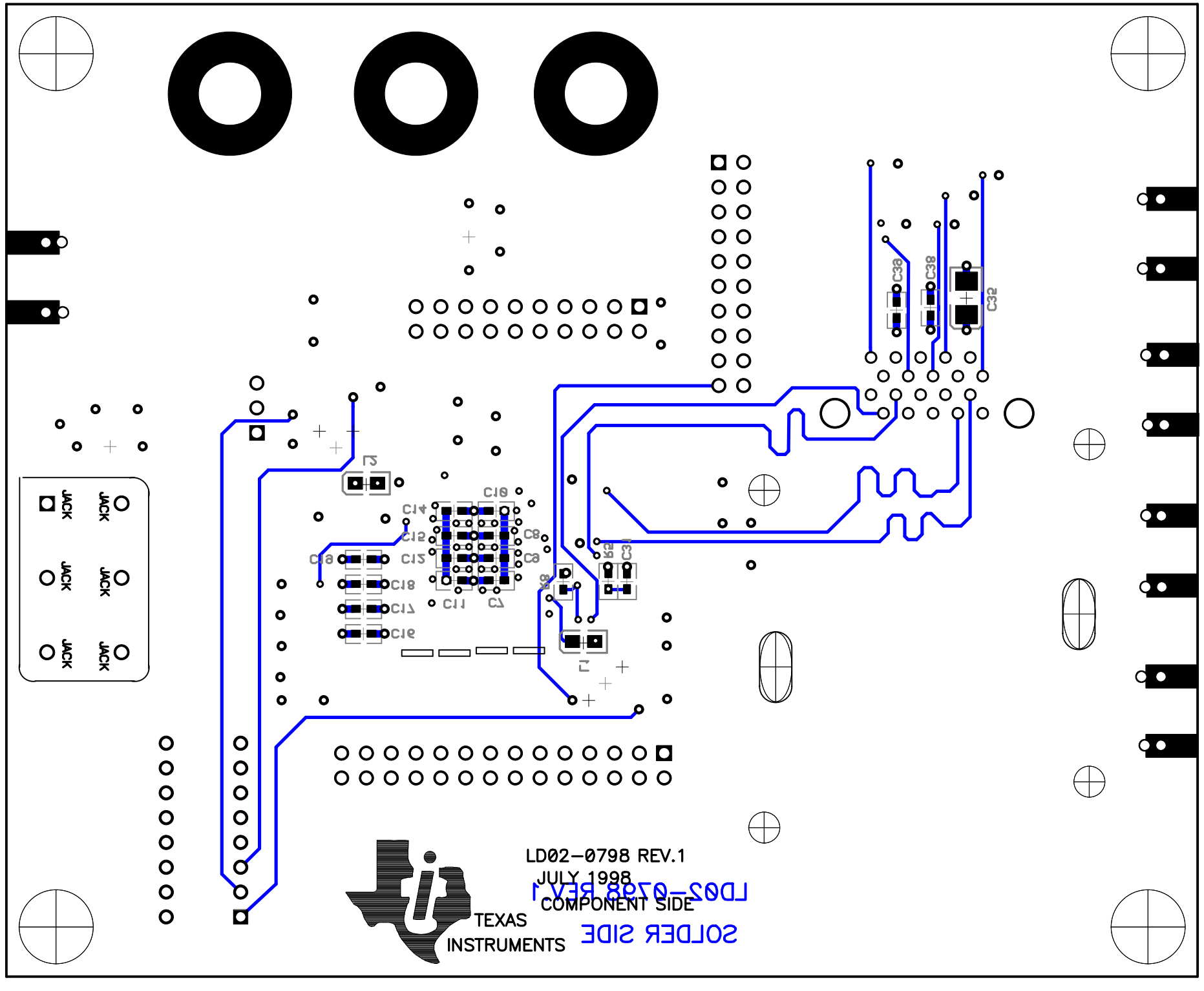
MADE IN USA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INSTRUMENTS
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India 000-117
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New Zealand 000-911
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Philippines 105-11
TI Number -800-800-1450
Singapore 800-0111-111
TI Number -800-800-1450
Taiwan 080-006800
Thailand 0019-991-1111
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