4 Channel Input Buffer Board

Model SDAIBB

Document No. SDAIBB1300

This product designed and manufactured in Ottawa, Illinois USA
of domestic and imported parts by

B&B Electronics

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Table of Contents

Chapter 1: General Information

Introduction

The SDAIBB is a data acquisition module with four input buffers with selectable gains and selectable output offsets. The gain can be set from 1 to 1000 with a single resistor change. Gains of 1 and 22.28 are provided. The output can be offset by the provided 0 V for positive ended systems, by the provided 2.5 V for plus/minus applications, or by a user selected amount that is brought in on terminal blocks or solder pads. The SDAIBB is designed to amplify single ended or differential signals in the range of –0.15 to +5.0 V into +0.01 to +5.0 V signals that are compatible with the B&B line of data acquisition products. Sensor and power supply connections are made through terminal blocks or solder pads. A/D connections are made through DB25 connectors and are designed to connect to many of the B&B data acquisition products. All lines on the DB25 connectors are carried through, allowing boards to be "stacked" for expanding the number of channels or bringing other lines in or out. Three SDAIBB boards will fill all 11 channels of the 232SDAxx or 485SDAxx modules.

Specifications

Number of Channels	4
Gain	1 to 1000 1 and 22.28 provided
Max. Gain Error	0.35%
Max. Gain Drift	25 ppm
Max. Input Offset Voltage	200 µV
Max. Input Offset Voltage Drift	2 µV/°C
Input Impedance	2 GΩ, 2pF
Input Voltage Range	
Gain = 1	-0.15 to +5.00 V
Gain > 1	-0.15 to +4.60 V
Output Voltage Range	
Gain = 1	0.01 to 5.00 V
Gain > 1	0.01 to 4.95 V

Power Supply

Input Voltage	
Single Module	10 to 30 VDC
Three Modules	12 to 30 VDC
Input Current	8 mA max. per Module
Current Draw From Precision 5 V	0.5 mA per board
Max. Current Throughput	1 A

Connections

Analog Input	Terminal Blocks/Solder Pads
Analog Output	DB25 Male Connector and DB25 Female Connector
Power	Terminal Blocks/Solder Pads Pins 2 and 7 of the Male DB25

Environment

Operating Temperature	-40 to +85 °C
Storage Temperature	-65 to +125 °C

Size	5.6 x 2.75 in. 14 x 7 cm

Chapter 2: Connections

Power Supply Connections

A single SDAIBB board requires 8 mA at 10 to 30 VDC, and can be brought directly into the board through terminal blocks or solder pads marked POWER and GND or passed from another board connected to the male side of the board. See Figure 1 for a system where the power is brought directly onto the board. When passing power through from another board, POWER is carried through on pin 2 and GND is carried through on pin 7. Powers flows in on the male DB25 connector and out on the female DB25 connector with a 0.5 VDC drop across the board. This allows multiple boards to be powered with a single power supply by cascading them. See Table 4 for a list of B&B data acquisition products that carry power through on pins 2 and 7. Using these devices, you can power an entire system with a single power supply as shown in Figure 2.

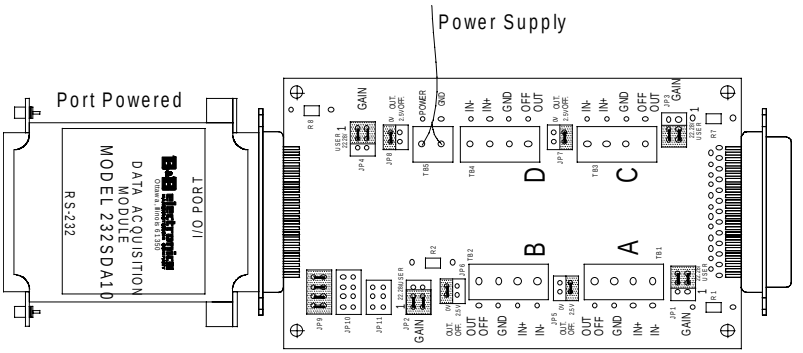

Figure 1: Port Powered SDA and Powered Board

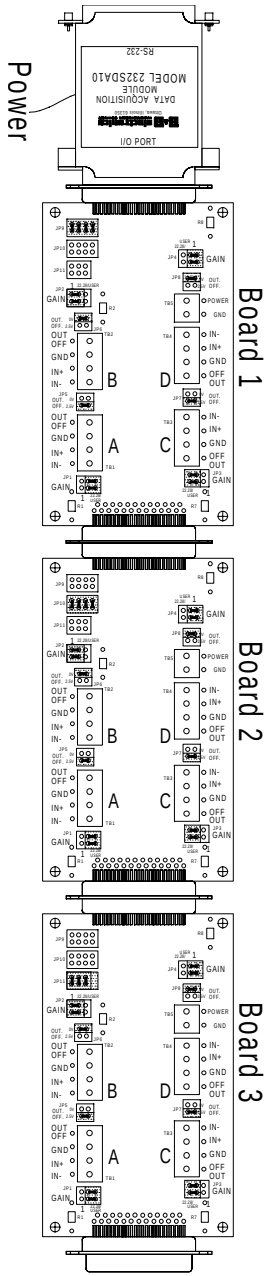

Figure 2: Single Power Supply System with 11 Channels Supported

Input Voltage Connections

The SDAIBB can receive signals in the range of –0.15 to +5 VDC when set to unity gain, and –0.15 to +3.5 VDC when set to any other gain. **Note: This voltage reading is taken from GND on the SDAIBB to Input+ and GND to Input- voltages. It is *not* the differential voltage from Input- to Input+.** Signals are brought into the buffer by terminal blocks or solder pads. The terminal blocks are labeled Input+, Input-, GND, and Output Offset. See Figures 3, 4, and 5 for typical input configurations. The voltage that will be amplified is the reading taken from Input- to Input+. GND is connected to the ground of the SDAIBB and is provided for making a common reference for the SDAIBB and the input device. The Output Offset is an input that shifts the output of the SDAIBB. This feature is discussed further in Chapter 3, Output Offset.

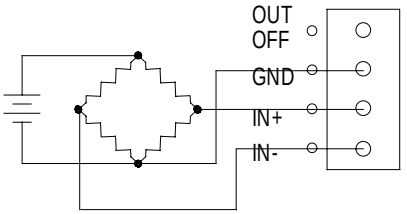

Figure 3: Differential Signal with GND

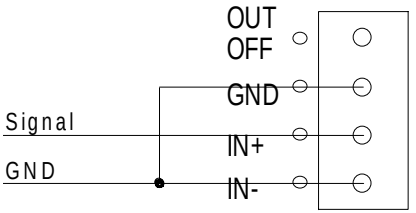

Figure 4: Single Ended Signal

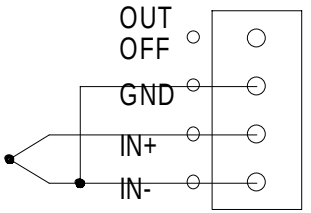

Figure 5: Floating Differential Signal

Output Voltage Connections

The SDAIBB outputs voltages from +0.1 to +5.0 VDC at unity gain, and +0.1 to +4.95 VDC at any other gain. All lines are carried straight through on the DB25 connectors, allowing for the addition of extra channels by connecting on another board.

The SDAIBB output connections are jumper selectable to line up with the channels of the B&B line of SDAxx data acquisition devices. When the 4-position shunt is set to JP9, input buffer A is connected to channel 0 on pin 8, B is connected to channel 1 on pin 9, C is connected to channel 2 on pin 10, and buffer D is connected to channel 3 on pin 11. Setting the 4-position shunt to JP10 connects the buffers to channels 4 to 7 (pins 12, 13, 21, and 22 respectively), and setting the shunt to JP11 connects the buffers to channels 8 to 10 (pins 23 to 25). See Table 1 for a list of the connections when the jumper is on JP9,

Table 2 for when the jumper is on JP10, and Table 3 for when the jumper is on JP11. **Note: When the 4-position jumper is on JP11, buffer D is not connected to any pins on the DB25 connector.**

For a listing of which modules the SDAIBB can connect to and which channels are compatible on each module, see Table 4.

Table 1: Connections when the 4-position shunt is on JP9

Pin	Connection	Pin	Connection
1	---	14	---
2	Power	15	---
3	---	16	---
4	---	17	---
5	---	18	---
6	---	19	---
7	GND	20	---
8	A output	21	---
9	B output	22	---
10	C output	23	---
11	D output	24	---
12	---	25	---
13	---		

Table 2: Connections when the 4-position shunt is on JP10

Pin	Connection	Pin	Connection
1	---	14	---
2	Power	15	---
3	---	16	---
4	---	17	---
5	---	18	---
6	---	19	---
7	GND	20	---
8	---	21	C output
9	---	22	D output
10	---	23	---
11	---	24	---
12	A output	25	---
13	B output		

Table 3: Connections when the 4-position shunt is on JP11

Pin	Connection	Pin	Connection
1	---	14	---
2	Power	15	---
3	---	16	---
4	---	17	---
5	---	18	---
6	---	19	---
7	GND	20	---
8	---	21	---
9	---	22	---
10	---	23	A output
11	---	24	B output
12	---	25	C output
13	---		

Table 4: Models Compatible with SDAIBB

Model	Channel Select Jumper Connections Supported	Channels Supported	Power on pins 2 and 7	2.5V Output Offset Available
485SDA10	JP9, JP10, JP11	0-10	Yes	Yes
485SDA12	JP9, JP10, JP11	0-10	Yes	Yes
232SDA10	JP9, JP10, JP11	0-10	Yes	Yes
232SDA12	JP9, JP10, JP11	0-10	Yes	Yes
232SPDA	JP9	0-3	Yes	Yes
232SPDACL	JP9	0-3	Yes	Yes
485SPDA	JP9	0-3	Yes	Yes
485SPDACL	JP9	0-3	Yes	Yes
232OPSDA	*	4 and 5	No	No
ADIO12	JP9	4-7	No	No
ADIO10	JP9	4-7	No	No

Set the jumper for any position and use the solder pads on the DB25 connector to bring out connections for channels 4 and 5. The other channels already have selectable gains.

To support all 11 channels on the SDAxx modules connect 3 SDAIBBs to the I/O port of the SDAxx as shown in Figure 2 on page 4 and set one board to JP9, one to JP10, and the last to JP11. This will provide 11 independent buffered inputs.

Chapter 3: Configuration

Output Offset

The output offset is the amount by which the output is shifted. Equation 1 shows how the output offset affects the output of the buffer. The negative output rail will clip any reading that has a negative input differential unless the buffer's output offset is raised. For this purpose, output offsets of 0 V and 2.5 V are individually jumper selectable for each channel on the SDAIBB when mated with a compatible data acquisition model. JP5 corresponds to channel A, JP6 corresponds with channel B, JP7 corresponds with channel C, and JP8 corresponds with channel D.

An output offset of 0 V is always available. See Table 4 for a list of models that support the 2.5 V output offset. An output offset of 0 V is used for positive only differentials, and an output offset of 2.5 V provides the maximum input range for signals that run equally positive and negative.

A different output offset may be brought in on the terminal blocks with the output offset jumper removed on the corresponding channel.

Equation 1: $V_{out} = (IN_{+} - IN_{-})Gain + OutputOffset$

Gain Selection

The gain is individually selectable on each buffer with a two-position jumper. Gains of 1 and 22.28 are conveniently provided on the unit for each buffer. JP1 controls the gain on channel A, JP2 controls B, JP3 controls C, and JP4 controls D. Unity gain is ideal for eliminating the impedance mismatch between input devices and the data acquisition module. Table 5 shows the maximum voltage ranges that can be amplified by the provided gain of 22.28. To change the gain, leave the jumper in the User/22.28 gain position, remove the through-hole 4.7 kΩ resistor, and replace it with the appropriate value. See Table 6 for some standard inputs, gains, and appropriate resistor values to achieve the expected gain.

Table 5: Values for Use with the Provided Gain of 22.28

VCM	VDIFF	Out Ref	1% Resistor	Calculated Gain	Output Range
27.5 mV max	+55 mV	0 V	4.7 kΩ	22.28	0.01 – 1.23 V
0 V	±52 mV	2.5 V	4.7 kΩ	22.28	1.32 - 3.68 V
2.5 V	±110 mV	2.5 V	4.7 kΩ	22.28	0.03 - 4.97 V

Table 6: Gains and Resistor Values for Standard Inputs

V_{CM}	V_{DIFF}	Out Ref	G_{MAX}	Closest 1% Resistor	Calculated Gain	Output Range
5mV max	+10 mV	0V	119	866 Ω	116.47	0.01 - 1.16 V
50mV max	+100mV	0V	12.8	8.66 kΩ	12.55	0.01 - 1.25 V
0.5V max	+1 V	0V	2.18	86.6 kΩ	2.15	0.01 - 2.18 V
0V	±10 mV	2.5V	118	866 Ω	116.47	1.34 - 3.66 V
0V	±100 mV	2.5V	11.8	9.31 kΩ	11.74	1.32 - 3.67 V
2.5V	±10 mV	2.5V	247	412 Ω	243.72	0.06 - 4.94 V
2.5V	±100 mV	2.5V	24.7	4.32 kΩ	24.15	0.09 - 4.91 V
2.5V	±1 V	2.5V	2.47	69.8 kΩ	2.43	0.07 - 4.93 V

Change R1 to change the gain on channel A, R2 to change channel B, R7 to change channel C, and R8 to change channel D. The following sections explain how to calculate the gain and gain resistor for other input ranges.

Maximum Gain

The maximum gain for a known differential voltage and common mode voltage can easily be determined using the following set of equations. Equation 5 calculates the maximum gain based on the positive internal rail of the amplifier. Equation 6 gives the maximum gain based on the negative internal rail of the amplifier. Equation 7 calculates the maximum gain without overflowing the output range of the SDAIBB. The smallest maximum gain value calculated using these equations is the maximum gain that may be used.

$$\textbf{Equation 2: } G_{MAX} = \frac{2(4.4V - V_{CM})}{V_{DIFF}}$$

$$\textbf{Equation 3: } G_{\max} = \frac{2(V_{cm} + 0.59V)}{V_{DIFF}}$$

$$\textbf{Equation 4: } G_{MAX} = 4.94V \Big/ InputRange$$

G is the gain, V_{cm} is the common mode voltage, and V_{diff} is the differential voltage.

Example: Find the maximum allowable gain for a differential voltage of ±10 mV and a common mode voltage of 2.5 V.

From Equation 5: $G_{MAX} = \frac{2(4.4 - 2.5)}{0.01} = 380$

From Equation 6: $G_{\max} = \frac{2(2.5 + 0.59)}{0.01} = 618$

From Equation 7: $G_{MAX} = 4.94 \Big/ 0.02 = 247$

The minimum value calculated is 247, so the maximum allowable gain is 247.

Gain Resistor Determination

Replacing a single resistor changes the gain on each buffer. Change R1 to modify the gain on channel A, R2 to change channel B, R7 to change channel C, and R8 to change channel D. Use Equation 8 to determine the value of the gain resistor to attain a calculated gain. To use this gain value, place the gain jumper corresponding to the correct channel in the User/22.28 position. JP1 corresponds to channel A, JP2 corresponds to channel B, JP3 corresponds to channel C, and JP4 corresponds to channel D.

Equation 8: $R_G = 100k\Omega / (G-1)$

Equation 9: $G = 1 + 100k\Omega / R_G$

R_G is the value of the gain resistor in ohms.

Example: Find the appropriate 1% resistor for a maximum gain of 150 and calculate the actual gain.

From Equation 8: $R_G = 100000 / (150-1) = 671.141$

The nearest 1% resistor that will produce a gain of 150 or less is 681Ω.

From Equation 9: $G = 1 + 100000 / 681 = 147.8$

The nearest 1% resistor is 681Ω with a resulting gain of 147.8.

Maximum and Minimum Common Mode Voltage

If the differential voltage range and desired gain are known, the maximum and minimum common mode voltage can be determined. Equation 10 is used to calculate the maximum common mode voltage knowing the gain and the differential voltage. Equation 11 is used to calculate the minimum common mode voltage. Remember that when Input+ or Input- is connected to GND on the SDAIBB the common mode voltage changes as the differential voltage changes.

Equation 10: $$V_{CMMAX} = 4.4V - \frac{V_{DIFF} \times G}{2}$$

Equation 11: $$V_{CMMIN} = -0.590V + \frac{V_{DIFF} \times G}{2}$$

Example: Find the allowable range of the common mode voltage for a input range of ±100 mV with a gain of 10.

From Equation 10: $$V_{CMMAX} = 4.4 - \frac{0.1 \times 10}{2} = 3.9V$$

From Equation 11: $$V_{CMMIN} = -0.590 + \frac{0.1 \times 10}{2} = -0.09V$$

The common mode voltage must be between –0.09 and 3.9 V.

Maximum Differential

To determine the maximum differential voltage that can be amplified, the gain and the common mode voltage must be known first. Using this information, the most positive the differential voltage may be is calculated using Equation 12. Equation 13 is used to calculate the most negative that the differential voltage may swing. These two values are still limited by the maximum allowable swing given by Equation 14.

Equation 12: $|V_{DIFF}| = \frac{2(4.4 - V_{CM})}{G}$

Equation 13: $|V_{DIFF}| = \frac{2(V_{CM} + 0.590V)}{G}$

Equation 14: $InputRange \leq {}^{4.94V}\!/_{G}$

Example: Find the allowable swing of a signal with a common mode voltage of 1V with a gain of 50.

From Equation 12: $|V_{DIFF}| = \frac{2(4.4-1)}{50} = 0.136$

From Equation 13: $|V_{DIFF}| = \frac{2(1+0.590)}{50} 0.0636$

From Equation 14: $InputRange \leq {}^{4.94}\!/_{50} = 0.0988$

The differential voltage can swing as negative as –0.0636 V and as positive as 0.136 V. However, this full range cannot be achieved with the same output offset setting due to the 0.0988 V range from Equation 14. To find the output offset voltage that allows the lower end of this range, use Equation 1 with Vout set to 0.01 V.

$$V_{out} = (IN_+ - IN_-)G + OutputOffset$$

Rearranged to calculate the desired output offset it looks like this

$$OutputOffset = V_{out} - V_{DIFF} \times G$$

Substitute in the appropriate values and solve for the output offset.

$$OutputOffset = 0.01 - (-0.0636) \times 50 = 3.19V$$

Example Board Setup

Figure 6 is an example of one possible configuration for the SDAIBB without modifying the board. Table 7 lists the setup for each channel.

Table 7: Setup for Figure 6

Channel	Output Pin	Gain	Output Offset
A	8	22.28	2.5 V
B	9	1	0.0 V
C	10	1	2.5 V
D	11	22.28	0.0 V

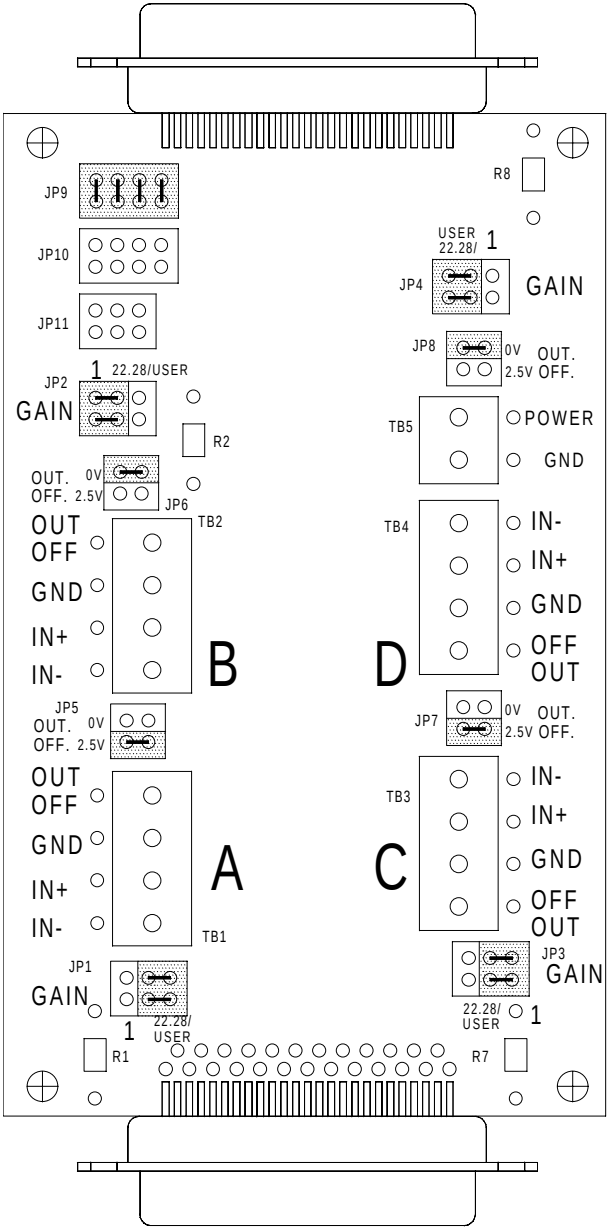
JP9
JP10
JP11
JP2
GAIN
1
22.28/USER
R2
OUT.
OFF.
0V
2.5V
JP6
TB2
OUT
OFF
GND
IN+
IN-
B
JP5
OUT.
OFF.
0V
2.5V
A
TB1
JP1
GAIN
1
22.28/
USER
R1
R8
USER
22.28/
1
JP4
GAIN
JP8
0V
2.5V
OUT.
OFF.
TB5
POWER
GND
TB4
IN-
IN+
GND
OFF
OUT
D
JP7
0V
2.5V
OUT.
OFF.
TB3
IN-
IN+
GND
OFF
OUT
C
JP3
GAIN
22.28/
USER
1
R7

Figure 6

Appendix A: Glossary

Common Mode Voltage (V_{CM})**:** The voltage about which a differential voltage swings. When this is measured on the SDAIBB it is calculated with all voltage readings taken in reference to GND of the SDAIBB as $(IN_+ + IN_-)/2$. Note that when one of the inputs is connected to GND of the SDAIBB the common mode voltage changes as the differential voltage changes.

Differential Voltage (V_{DIFF})**:** The difference in voltage across two points such as the two leads on a thermocouple. When this is measured on the SDAIBB it is calculated with all voltage readings taken in reference to GND of the SDAIBB as $IN_+ - IN_-$.

Gain (G)**:** The amount by which the input is multiplied before it is output.

$$Gain = \frac{V_{out}}{IN_+ - IN_-}$$

Impedance Mismatch: When the output impedance of sensor is different enough from the input impedance of the data acquisition device to cause improper sensor readings.

Negative Input Differential: When the voltage and IN- is higher than the voltage at IN-. $IN_+ - IN_- \leq 0$

Negative Rail: The lowest possible voltage that can be output. For the SDAIBB there is a negative rail internal to the buffer and a negative rail on the output of the buffer.

Positive Rail: The highest possible voltage that can be output. For the SDAIBB there is a positive rail internal to the buffer and a positive rail on the output of the buffer.

Appendix B: Error Budget Calculations

Important Specs @ 25°C:

V *offset in* (V_{OSI})	200 µV
V *offset out* (V_{OSO})	1000 µV
I *offset* (I_{OS})	2nA
Gain Error	0.35%
Gain Nonlinearity	50ppm
0.1Hz to 10Hz Noise	3.0µV p-p
CMR	84dB @ 60 Hz

Error Contributions that can be Removed With Calibration

Equation 15: $V_{OS} = \dfrac{V_{OSI} + V_{OSO}/G}{V_{in}}$

Equation 16: $I_{OS} = \dfrac{\text{Sensor Impedance} \times I_{os}}{V_{in}}$

Equation 17: $\text{Gain Error} = 3500\,ppm$

Equation 18: $\text{CMR Error} = \dfrac{4\,ppm \times V_{CM}}{V_{in}}$

V_{in} is the input voltage.

Error Contributions that Cannot be Removed with Calibration

Equation 19: $\text{Gain Nonlinearity} = 50\,ppm$

Equation 20: $0.1\text{Hz} - 10\text{Hz noise} = 3000nV/V_{in}$

Example: Calculate the error budget for a 350Ω, 100mV load cell with a common mode voltage of 2.5V using a gain of 22.28.

From Equation 15: $V_{OS} = \frac{200\mu V + {}^{500\mu V}\!/_{22.28}}{100mV} = 2449\,ppm$

From Equation 16: $I_{OS} = \frac{350\Omega \times 2nA}{100mV} = 7\,ppm$

From Equation 17: Gain Error = $3500\,ppm$

From Equation 18: CMR Error = $\frac{4\,ppm \times 2.5V}{100mV} = 100\,ppm$

From Equation 19: Gain Nonlinearity = $50\,ppm$

From Equation 20: 0.1Hz - 10Hz noise = ${}^{3000nV}\!/_{100mV} = 3\,ppm$

Total Unadjusted Error = 6109ppm
Error After Calibration = 53ppm

FEDERAL COMMUNICATIONS COMMISSION
RADIO FREQUENCY INTERFACE STATEMENT

Class A Equipment

This equipment has been tested and found to comply with the limits for Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at personal expense.