

# MoBL® 1 Mbit (128K x 8) Static RAM

## Features

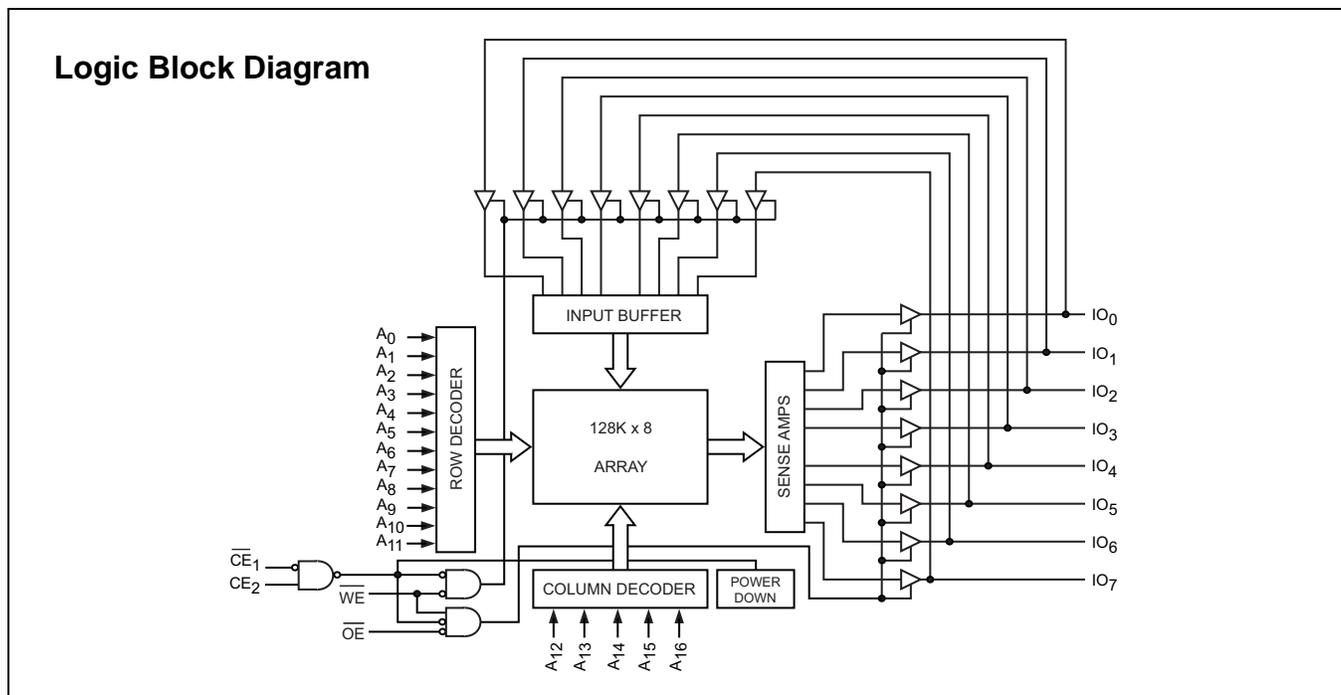
- Very high speed: 45 ns
  - Temperature ranges:
    - Industrial: -40°C to +85°C
    - Automotive-A: -40°C to +85°C
    - Automotive-E: -40°C to +125°C
- Wide voltage range: 2.20V – 3.60V
- Pin compatible with CY62128DV30
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 4  $\mu$ A
- Ultra low active power
  - Typical active current: 1.3 mA @ f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 32-pin SOIC, 32-pin TSOP I, and 32-pin STSOP packages

## Functional Description

The CY62128EV30<sup>[1]</sup> is a high performance CMOS static RAM module organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW). The eight input and output pins ( $IO_0$  through  $IO_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH and  $\overline{WE}$  LOW).

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight IO pins is then written into the location specified on the Address pin ( $A_0$  through  $A_{16}$ ).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.



### Note

1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at <http://www.cypress.com>.

Pin Configuration<sup>[2]</sup>

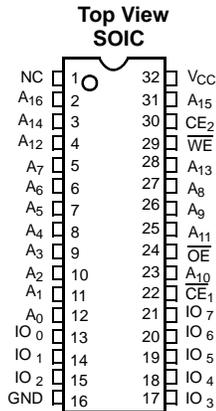
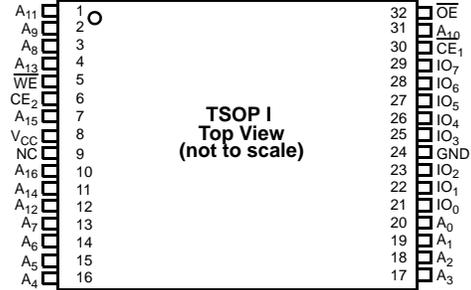
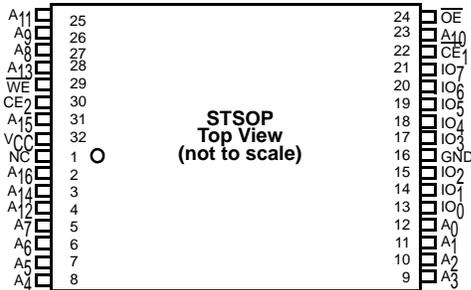


Table 1. Product Portfolio

| Product       | Range              | V <sub>CC</sub> Range (V) |                    |     | Speed (ns)         | Power Dissipation              |                    |                      |    |                               |    |
|---------------|--------------------|---------------------------|--------------------|-----|--------------------|--------------------------------|--------------------|----------------------|----|-------------------------------|----|
|               |                    |                           |                    |     |                    | Operating I <sub>CC</sub> (mA) |                    |                      |    | Standby I <sub>SB2</sub> (μA) |    |
|               |                    |                           |                    |     |                    | f = 1 MHz                      |                    | f = f <sub>max</sub> |    |                               |    |
| Min           | Typ <sup>[3]</sup> | Max                       | Typ <sup>[3]</sup> | Max | Typ <sup>[3]</sup> | Max                            | Typ <sup>[3]</sup> | Max                  |    |                               |    |
| CY62128EV30LL | Ind'I/Auto-A       | 2.2                       | 3.0                | 3.6 | 45                 | 1.3                            | 2.0                | 11                   | 16 | 1                             | 4  |
| CY62128EV30LL | Auto-E             | 2.2                       | 3.0                | 3.6 | 55                 | 1.3                            | 4.0                | 11                   | 35 | 1                             | 30 |

Notes

- 2. NC pins are not connected on the die.
- 3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.3V to  $V_{CC(max)}$  + 0.3V

DC Voltage Applied to Outputs in High-Z State<sup>[4, 5]</sup> ..... -0.3V to  $V_{CC(max)}$  + 0.3V

DC Input Voltage<sup>[4,5]</sup> ..... -0.3V to  $V_{CC(max)}$  + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (MIL-STD-883, Method 3015)

Latch up Current ..... > 200 mA

## Operating Range

| Device        | Range        | Ambient Temperature | $V_{CC}$ <sup>[6]</sup> |
|---------------|--------------|---------------------|-------------------------|
| CY62128EV30LL | Ind'l/Auto-A | -40°C to +85°C      | 2.2V to 3.6V            |
|               | Auto-E       | -40°C to +125°C     |                         |

## Electrical Characteristics

(Over the Operating Range)

| Parameter                       | Description                                   | Test Conditions  | 45 ns (Ind'l/Auto-A) |                    |                        | 55 ns (Auto-E) |                    |                        | Unit |
|---------------------------------|---|--|----------------------|--------------------|------------------------|----------------|--------------------|------------------------|------|
|                                 |   |  | Min                  | Typ <sup>[3]</sup> | Max                    | Min            | Typ <sup>[3]</sup> | Max                    |      |
| V <sub>OH</sub>                 | Output HIGH Voltage                           | I <sub>OH</sub> = -0.1 mA  | 2.0                  |                    |                        | 2.0            |                    |                        | V    |
|                                 |   | I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> ≥ 2.70V   | 2.4                  |                    |                        | 2.4            |                    |                        | V    |
| V <sub>OL</sub>                 | Output LOW Voltage                            | I <sub>OL</sub> = 0.1 mA   |                      |                    | 0.4                    |                |                    | 0.4                    | V    |
|                                 |   | I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> ≥ 2.70V  |                      |                    | 0.4                    |                |                    | 0.4                    | V    |
| V <sub>IH</sub>                 | Input HIGH Voltage                            | V <sub>CC</sub> = 2.2V to 2.7V   | 1.8                  |                    | V <sub>CC</sub> + 0.3V | 1.8            |                    | V <sub>CC</sub> + 0.3V | V    |
|                                 |   | V <sub>CC</sub> = 2.7V to 3.6V   | 2.2                  |                    | V <sub>CC</sub> + 0.3V | 2.2            |                    | V <sub>CC</sub> + 0.3V | V    |
| V <sub>IL</sub>                 | Input LOW Voltage                             | V <sub>CC</sub> = 2.2V to 2.7V   | -0.3                 |                    | 0.6                    | -0.3           |                    | 0.6                    | V    |
|                                 |   | V <sub>CC</sub> = 2.7V to 3.6V   | -0.3                 |                    | 0.8                    | -0.3           |                    | 0.8                    | V    |
| I <sub>IX</sub>                 | Input Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -1                   |                    | +1                     | -4             |                    | +4                     | μA   |
| I <sub>OZ</sub>                 | Output Leakage Current                        | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -1                   |                    | +1                     | -4             |                    | +4                     | μA   |
| I <sub>CC</sub>                 | V <sub>CC</sub> Operating Supply Current      | f = f <sub>max</sub> = 1/t <sub>RC</sub>   |                      | 11                 | 16                     |                | 11                 | 35                     | mA   |
|                                 |   | f = 1 MHz  |                      | 1.3                | 2.0                    |                | 1.3                | 4.0                    | mA   |
| I <sub>SB1</sub>                | Automatic CE Power down Current — CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2V$ , CE <sub>2</sub> < 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V<br>f = f <sub>max</sub> (Address and Data Only),<br>f = 0 (OE and WE), V <sub>CC</sub> = 3.60V |                      | 1                  | 4                      |                | 1                  | 35                     | μA   |
| I <sub>SB2</sub> <sup>[7]</sup> | Automatic CE Power down Current — CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2V$ , CE <sub>2</sub> < 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> < 0.2V,<br>f = 0, V <sub>CC</sub> = 3.60V   |                      | 1                  | 4                      |                | 1                  | 30                     | μA   |

### Notes

- V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
- Only chip enables ( $\overline{CE}_1$  and CE<sub>2</sub>) must be at CMOS level to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

## Capacitance

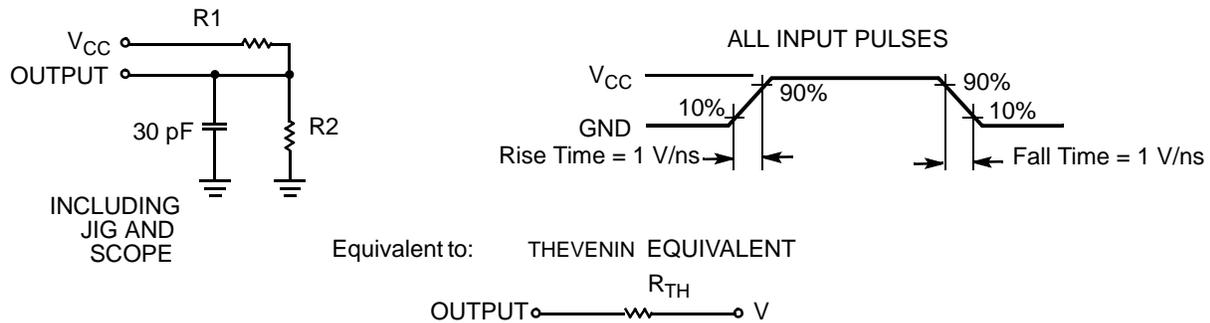
(For all packages)<sup>[8]</sup>

| Parameter | Description        | Test Conditions  | Max | Unit |
|-----------|--------------------|--|-----|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ ,<br>$V_{CC} = V_{CC(\text{typ})}$ | 10  | pF   |
| $C_{OUT}$ | Output Capacitance |  | 10  | pF   |

## Thermal Resistance

| Parameter     | Description                              | Test Conditions  | TSOP I | SOIC  | STSOP | Unit               |
|---------------|--|--|--------|-------|-------|--------------------|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board | 33.01  | 48.67 | 32.56 | $^\circ\text{C/W}$ |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case)    |  | 3.42   | 25.86 | 3.59  | $^\circ\text{C/W}$ |

Figure 1. AC Test Loads and Waveforms



| Parameters | 2.50V | 3.0V | Unit     |
|------------|-------|------|----------|
| R1         | 16667 | 1103 | $\Omega$ |
| R2         | 15385 | 1554 | $\Omega$ |
| $R_{TH}$   | 8000  | 645  | $\Omega$ |
| $V_{TH}$   | 1.20  | 1.75 | V        |

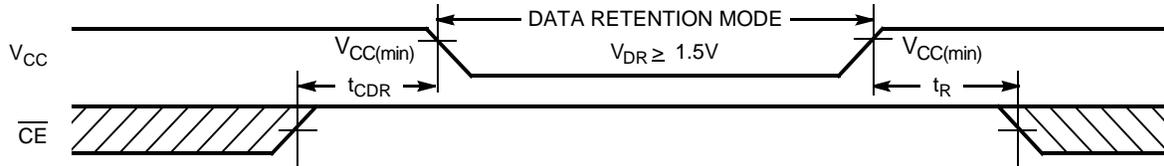
## Data Retention Characteristics

(Over the Operating Range)

| Parameter                 | Description                          | Conditions   | Min          | Typ <sup>[3]</sup> | Max | Unit          |
|---------------------------|--------------------------------------|--|--------------|--------------------|-----|---------------|
| $V_{DR}$                  | $V_{CC}$ for Data Retention          |  | 1.5          |                    |     | V             |
| $I_{CCDR}$ <sup>[7]</sup> | Data Retention Current               | $V_{CC} = 1.5\text{V}$ ,<br>$CE_1 \geq V_{CC} - 0.2\text{V}$ or $CE_2 \leq 0.2\text{V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$ | Ind'l/Auto-A |                    | 3   | $\mu\text{A}$ |
|                           |                                      |  | Auto-E       |                    | 30  | $\mu\text{A}$ |
| $t_{CDR}$ <sup>[8]</sup>  | Chip Deselect to Data Retention Time |  | 0            |                    |     | ns            |
| $t_R$ <sup>[9]</sup>      | Operation Recovery Time              |  | $t_{RC}$     |                    |     | ns            |

### Note

8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min})} \geq 100\ \mu\text{s}$  or stable at  $V_{CC(\text{min})} \geq 100\ \mu\text{s}$ .

**Data Retention Waveform** <sup>[10]</sup>

**Switching Characteristics**

 (Over the Operating Range)<sup>[10, 11]</sup>

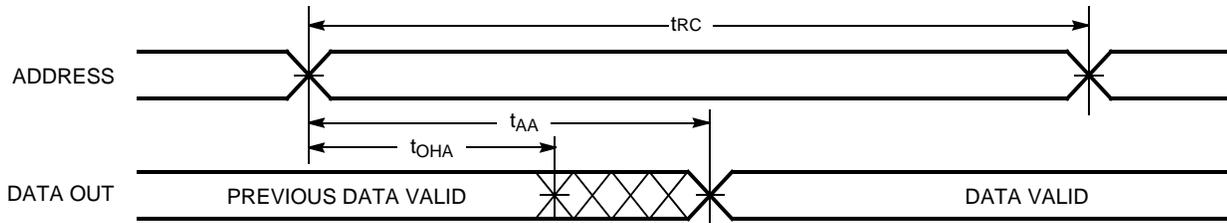
| Parameter                          | Description  | 45 ns (Ind'l/Auto-A) |     | 55 ns (Auto-E) |     | Unit |
|------------------------------------|--|----------------------|-----|----------------|-----|------|
|                                    |  | Min                  | Max | Min            | Max |      |
| <b>Read Cycle</b>                  |  |                      |     |                |     |      |
| t <sub>RC</sub>                    | Read Cycle Time                                    | 45                   |     | 55             |     | ns   |
| t <sub>AA</sub>                    | Address to Data Valid                              |                      | 45  |                | 55  | ns   |
| t <sub>OHA</sub>                   | Data Hold from Address Change                      | 10                   |     | 10             |     | ns   |
| t <sub>ACE</sub>                   | $\overline{CE}$ LOW to Data Valid                  |                      | 45  |                | 55  | ns   |
| t <sub>DOE</sub>                   | $\overline{OE}$ LOW to Data Valid                  |                      | 22  |                | 25  | ns   |
| t <sub>LZOE</sub>                  | $\overline{OE}$ LOW to Low Z <sup>[12]</sup>       | 5                    |     | 5              |     | ns   |
| t <sub>HZOE</sub>                  | $\overline{OE}$ HIGH to High Z <sup>[12,13]</sup>  |                      | 18  |                | 20  | ns   |
| t <sub>LZCE</sub>                  | $\overline{CE}$ LOW to Low Z <sup>[12]</sup>       | 10                   |     | 10             |     | ns   |
| t <sub>HZCE</sub>                  | $\overline{CE}$ HIGH to High Z <sup>[12, 13]</sup> |                      | 18  |                | 20  | ns   |
| t <sub>PU</sub>                    | $\overline{CE}$ LOW to Power Up                    | 0                    |     | 0              |     | ns   |
| t <sub>PD</sub>                    | $\overline{CE}$ HIGH to Power Up                   |                      | 45  |                | 55  | ns   |
| <b>Write Cycle</b> <sup>[14]</sup> |  |                      |     |                |     |      |
| t <sub>WC</sub>                    | Write Cycle Time                                   | 45                   |     | 55             |     | ns   |
| t <sub>SCE</sub>                   | $\overline{CE}$ LOW to Write End                   | 35                   |     | 40             |     | ns   |
| t <sub>AW</sub>                    | Address Setup to Write End                         | 35                   |     | 40             |     | ns   |
| t <sub>HA</sub>                    | Address Hold from Write End                        | 0                    |     | 0              |     | ns   |
| t <sub>SA</sub>                    | Address Setup to Write Start                       | 0                    |     | 0              |     | ns   |
| t <sub>PWE</sub>                   | $\overline{WE}$ Pulse Width                        | 35                   |     | 40             |     | ns   |
| t <sub>SD</sub>                    | Data Setup to Write End                            | 25                   |     | 25             |     | ns   |
| t <sub>HD</sub>                    | Data Hold from Write End                           | 0                    |     | 0              |     | ns   |
| t <sub>HZWE</sub>                  | $\overline{WE}$ LOW to High Z <sup>[12, 13]</sup>  |                      | 18  |                | 20  | ns   |
| t <sub>LZWE</sub>                  | $\overline{WE}$ HIGH to Low Z <sup>[12]</sup>      | 10                   |     | 10             |     | ns   |

**Notes**

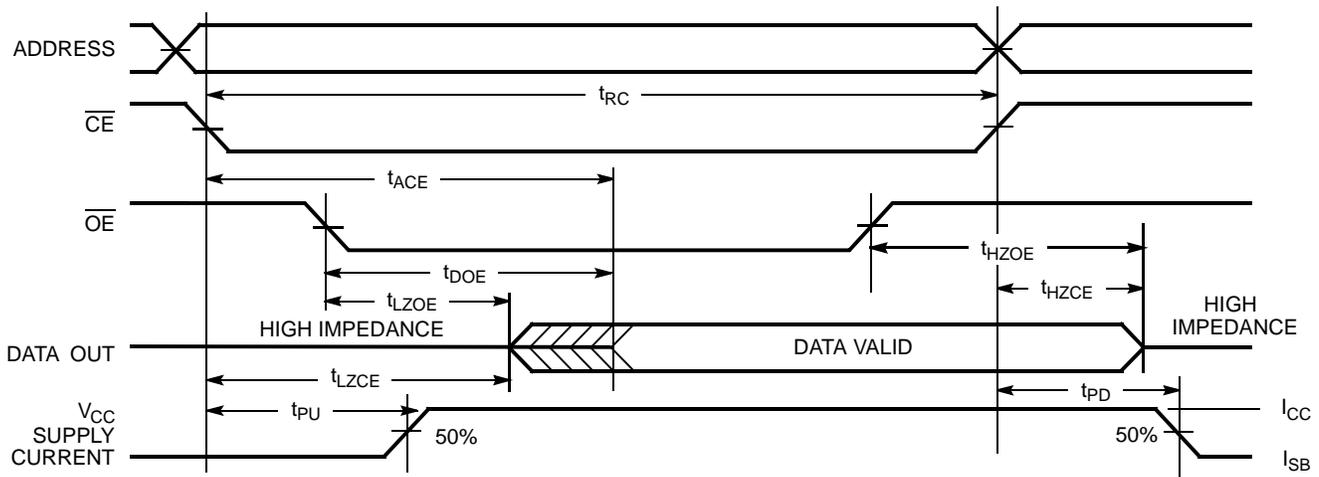
10.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
11. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" on page 4.
12. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
13.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enter a high impedance state.
14. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

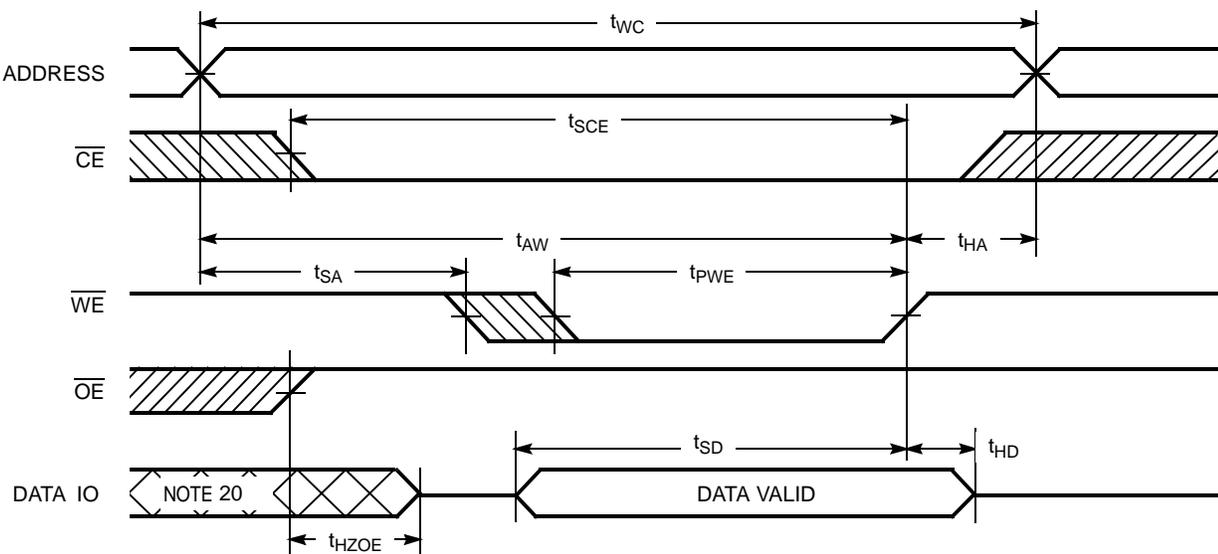
**Figure 2. Read Cycle 1 (Address transition controlled)** [15, 16]



**Figure 3. Read Cycle No. 2 ( $\overline{OE}$  controlled)** [10, 16, 17]



**Figure 4. Write Cycle No. 1 ( $\overline{WE}$  controlled)** [10, 15, 18, 19]



**Notes**

- 15. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 16.  $\overline{WE}$  is HIGH for read cycle.
- 17. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
- 18. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
- 19. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 20. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 2 ( $\overline{CE1}$  or  $CE2$  controlled) [10, 14, 18, 19]

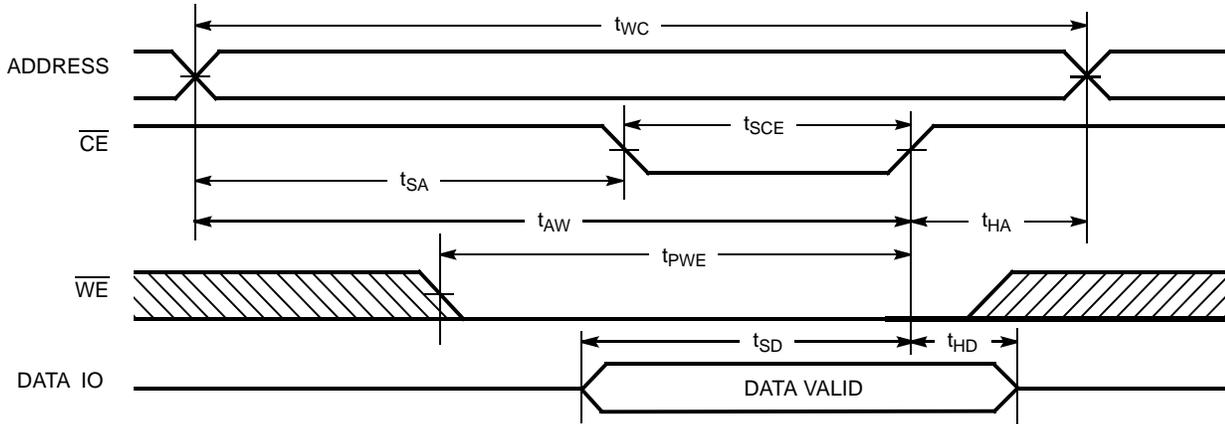


Figure 6. Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) [10, 19]

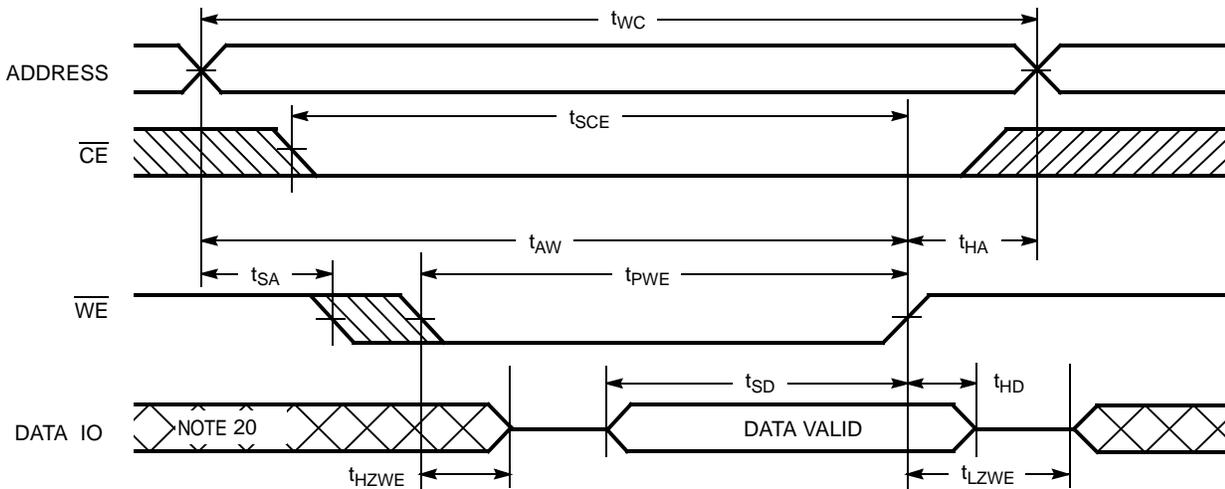


Table 2. Truth Table for CY62128EV30

| $\overline{CE}_1$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode                | Power                |
|-------------------|--------|-----------------|-----------------|----------------|---------------------|----------------------|
| H                 | X      | X               | X               | High Z         | Deselect/Power Down | Standby ( $I_{SB}$ ) |
| X                 | L      | X               | X               | High Z         | Deselect/Power Down | Standby ( $I_{SB}$ ) |
| L                 | H      | H               | L               | Data Out       | Read                | Active ( $I_{CC}$ )  |
| L                 | H      | H               | H               | High Z         | Output Disabled     | Active ( $I_{CC}$ )  |
| L                 | H      | L               | X               | Data in        | Write               | Active ( $I_{CC}$ )  |

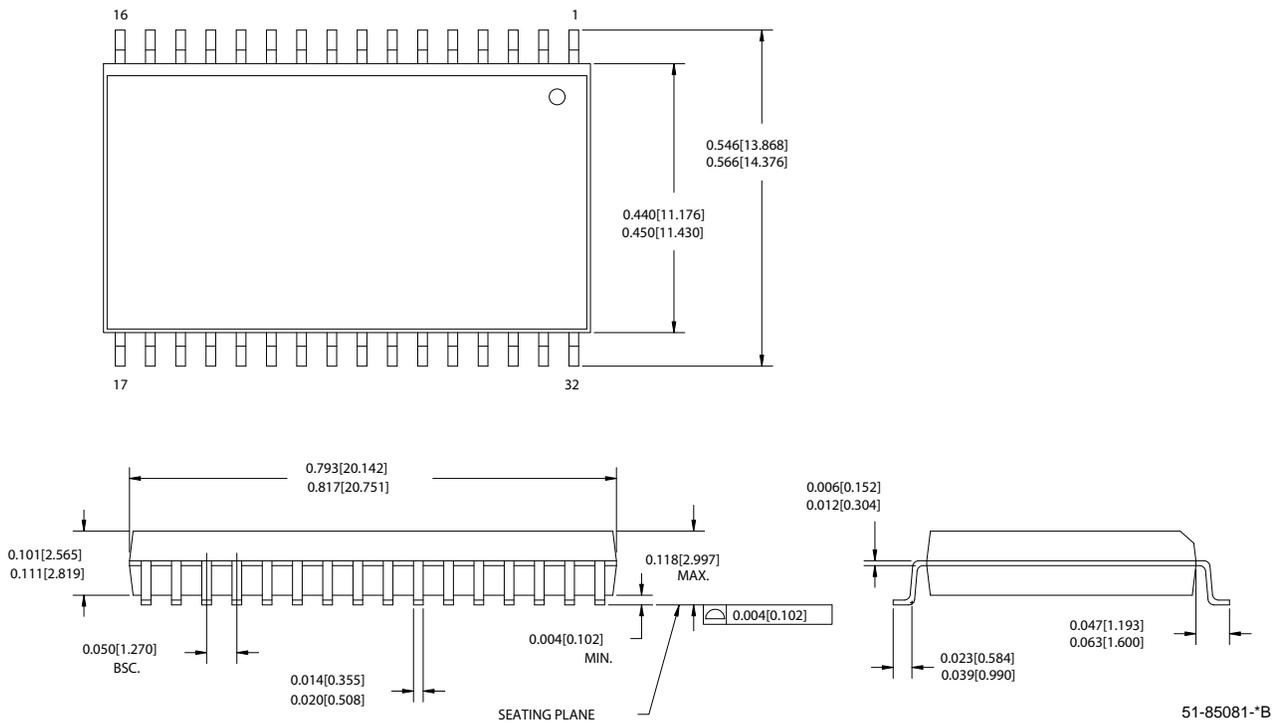
### Ordering Information

| Speed (ns) | Ordering Code        | Package Diagram | Package Type                  | Operating Range |
|------------|----------------------|-----------------|-------------------------------|-----------------|
| 45         | CY62128EV30LL-45SXI  | 51-85081        | 32-pin 450-Mil SOIC (Pb-free) | Industrial      |
|            | CY62128EV30LL-45ZXI  | 51-85056        | 32-pin TSOP Type I (Pb-free)  |                 |
|            | CY62128EV30LL-45ZAXI | 51-85094        | 32-pin STSOP (Pb-free)        |                 |
| 45         | CY62128EV30LL-45ZXA  | 51-85056        | 32-pin TSOP Type I (Pb-free)  | Automotive-A    |
| 55         | CY62128EV30LL-55ZXE  | 51-85056        | 32-pin TSOP Type I (Pb-free)  | Automotive-E    |

Contact your local Cypress sales representative for availability of these parts.

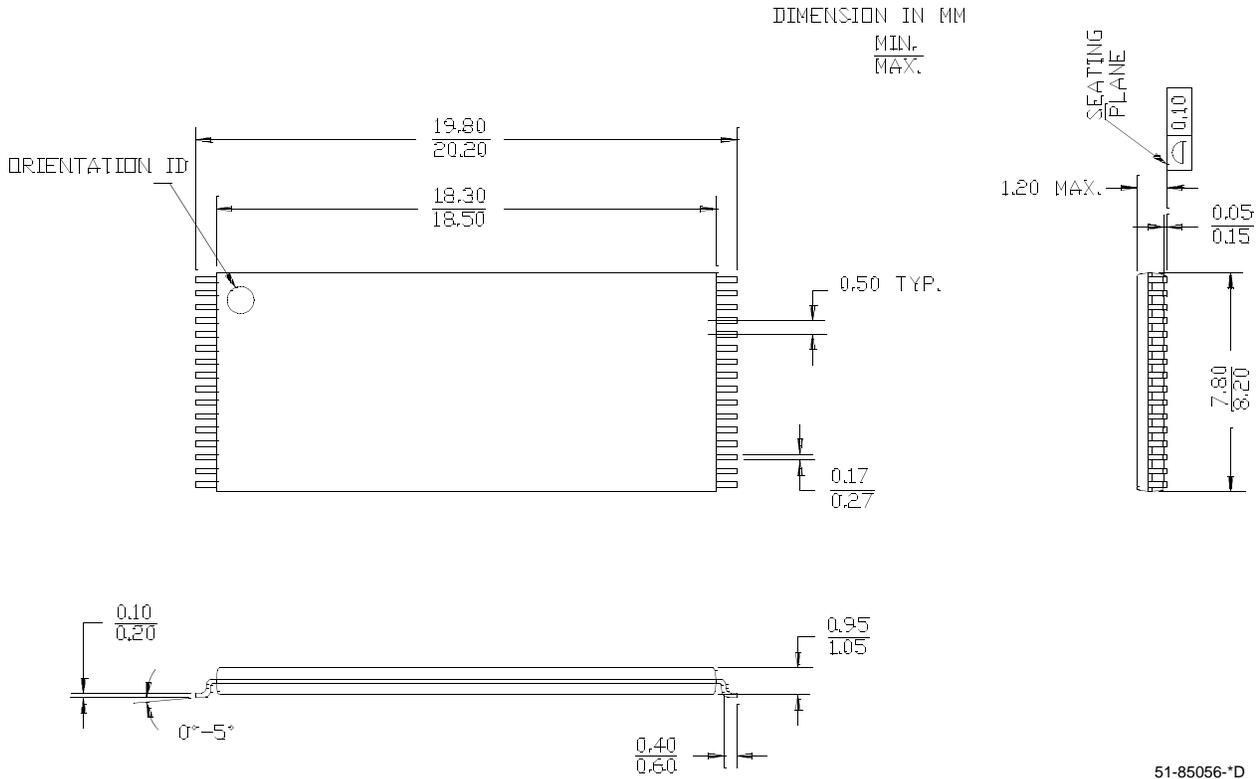
### Package Diagrams

Figure 7. 32-Pin (450 Mil) Molded SOIC, 51-85081



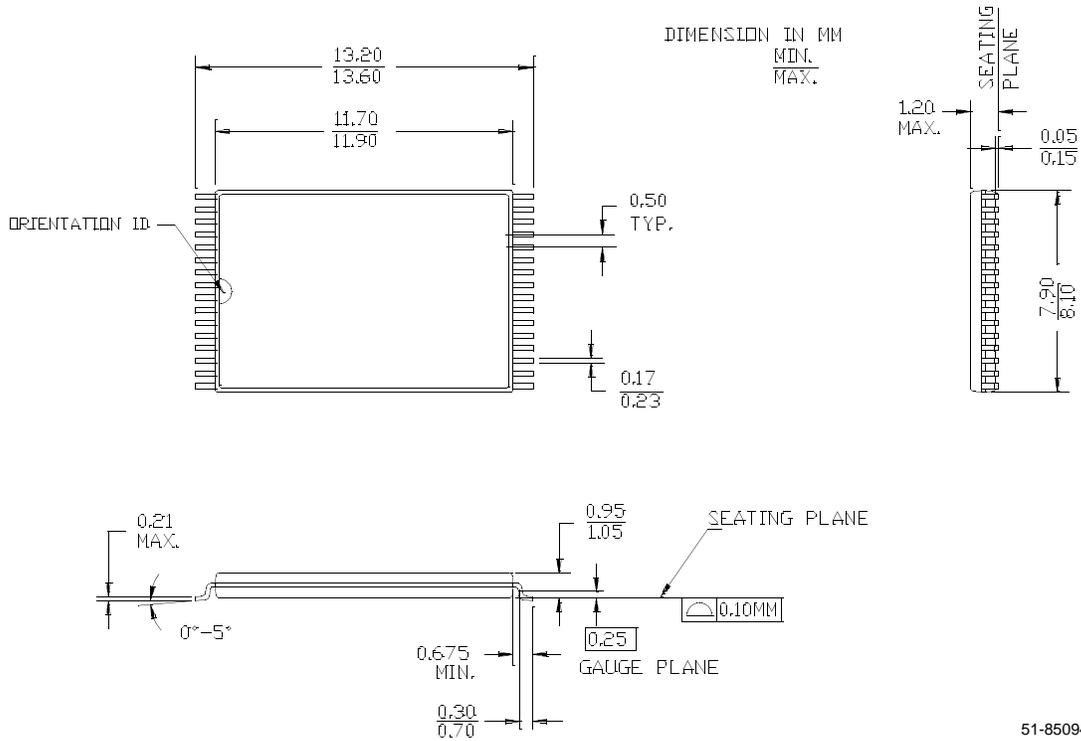
Package Diagrams (continued)

Figure 8. 32-Pin Thin Small Outline Package Type I (8 x 20 mm), 51-85056



Package Diagrams (continued)

Figure 9. 32-Pin Shrunk Thin Small Outline Package (8 x 13.4 mm), 51-85094



Document History Page

| Document Title: CY62128EV30 MoBL® 1 Mbit (128K x 8) Static RAM |         |            |                 |  |
|--|---------|------------|-----------------|--|
| Document Number: 38-05579                                      |         |            |                 |  |
| REV.   | ECN NO. | Issue Date | Orig. of Change | Description of Change  |
| **   | 285473  | See ECN    | PCI             | New Data Sheet   |
| *A   | 461631  | See ECN    | NXR             | Converted from Preliminary to Final<br>Removed 35 ns Speed Bin<br>Removed "L" version of CY62128EV30<br>Removed Reverse TSOP I package from Product offering.<br>Changed I <sub>CC (Typ)</sub> from 8 mA to 11 mA and I <sub>CC (Max)</sub> from 12 mA to 16 mA for f = f <sub>max</sub><br>Changed I <sub>CC (max)</sub> from 1.5 mA to 2.0 mA for f = 1 MHz<br>Changed I <sub>SB2 (max)</sub> from 1 μA to 4 μA<br>Changed I <sub>SB2 (Typ)</sub> from 0.5 μA to 1 μA<br>Changed I <sub>CCDR (max)</sub> from 1 μA to 3 μA<br>Changed the AC Test load Capacitance value from 50 pF to 30 pF<br>Changed t <sub>LZOE</sub> from 3 to 5 ns<br>Changed t <sub>LZCE</sub> from 6 to 10 ns<br>Changed t <sub>HZCE</sub> from 22 to 18 ns<br>Changed t <sub>PWE</sub> from 30 to 35 ns<br>Changed t <sub>SD</sub> from 22 to 25 ns<br>Changed t <sub>LZWE</sub> from 6 to 10 ns<br>Updated the Ordering Information table. |
| *B   | 464721  | See ECN    | NXR             | Updated the Block Diagram on page # 1  |
| *C   | 1024520 | See ECN    | VKN             | Added final Automotive-A and Automotive-E information<br>Added footnote #9 related to I <sub>SB2</sub> and I <sub>CCDR</sub><br>Updated Ordering Information table   |
| *D   | 2257446 | See ECN    | NXR             | Changed the Maximum rating of Ambient Temperature with Power Applied from 55°C to +125°C to -55°C to +125°C.   |

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