



# Intel<sup>®</sup> DBPXA250 and DBPXA210 Development Platform for Intel<sup>®</sup> Personal Internet Client Architecture

Specification Update

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*July 2002*

**Notice:** The Intel<sup>®</sup> DBPXA250 and DBPXA210 Development Platform for Intel<sup>®</sup> Personal Internet Client Architecture may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: **278555-002**



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# Revision History

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Date of Revision	Version	Description
May 2002	-001	Public Release
July 2002	-002	Removed 1, 2, 3, 4, 5, 6, 7, 8, 9, from Intel® BBPXA2xx Development Baseboard. Removed 1, 2, 4, 5, 6, 11, 12 from Intel® DCPXA250 processor card. Modified 12, 14 on the BBPXA2xx Development Baseboard. Modified 7, 9, 10, and 13 on the DCPXA250 processor card. Modified 1 on the DCPXA210 processor card. Added steppings matrix

# Preface

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This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

We have endeavored to include all documented errata in the consolidation process; however, we make no representations or warranties concerning the completeness of the *Intel® DBPXA250 and DBPXA210 Development Platforms for Intel® Personal Internet Client Architecture Specification Update*. This document may also contain information that was not previously published.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

## Affected Documents/Related Documents

Title	Order
Intel® DBPXA250 Development Platform for Intel® PCA User's Guide	278507
Intel® PXA250 and PXA210 Applications Processors Developer's Manual	278522
Intel® PXA250 and PXA210 Applications Processors Design Guide	278523
Intel® PXA250 and PXA210 Applications Processors Specification Update	278534

## Nomenclature

**Errata** are design defects or errors. These may cause the Intel<sup>®</sup> DBPXA250 and DBPXA210 Development Platforms for Intel<sup>®</sup> PCA behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices unless otherwise noted.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the document.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the document.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the document.

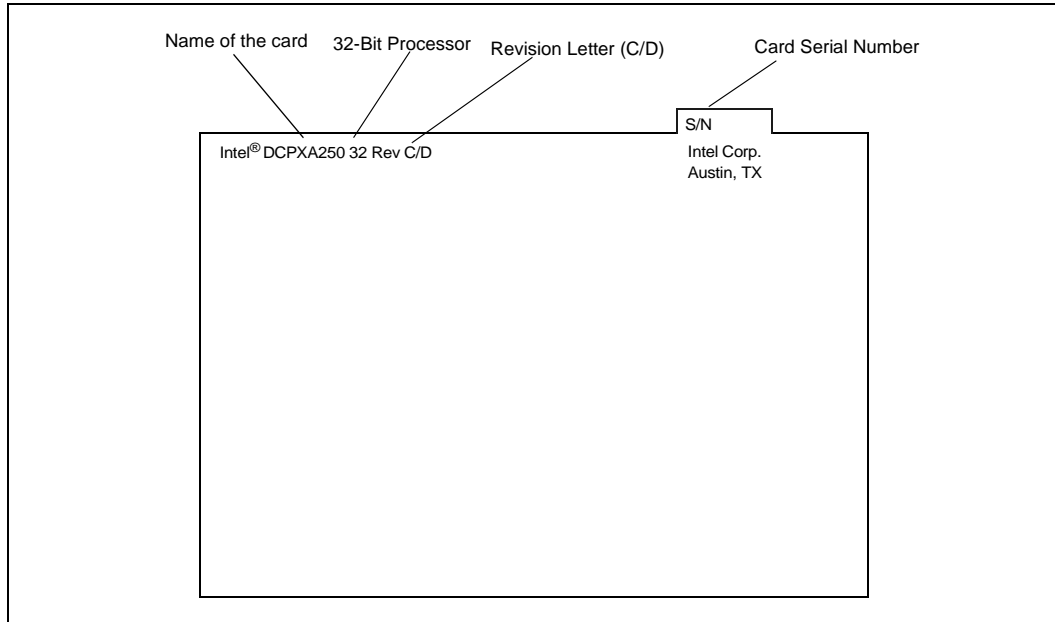
**Note:** Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

## General Information

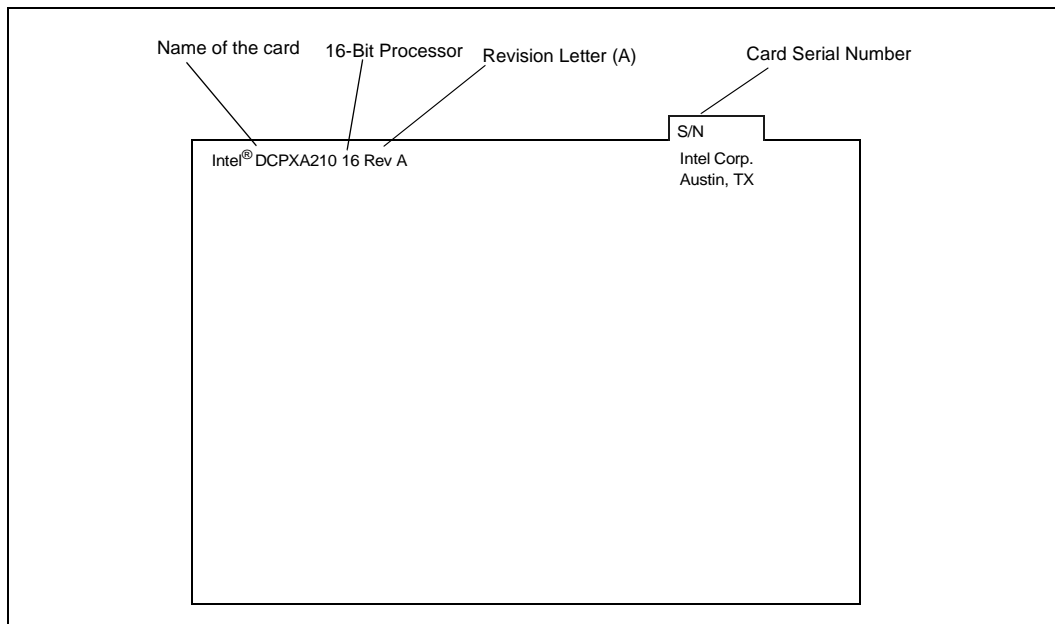
Figure 1 and Figure 2 show the markings for the DCPXA250 and DCPXA210 processor cards.

DCPXA250

**Figure 1. Intel® DCPXA250 Processor Card Markings**



**Figure 2. Intel® DCPXA210 Processor Card Markings**





# Summary of Changes

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The following tables indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel<sup>®</sup> DBPXA250 and DBPXA210 Development Platforms for Intel<sup>®</sup> PCA. This document covers these components of the development platform: the Intel<sup>®</sup> BBPXA2xx development baseboard, the Intel<sup>®</sup> DCPXA250 processor card, and the Intel<sup>®</sup> DCPXA210 processor card. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

## Codes Used in Summary Table

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.
Doc:	Intel intends to update the appropriate documentation in a future revision.
Shaded:	This item is either new or modified from the previous version of the document.

**Note:** Fixed refers to latest revision of the board and does not refer to earlier revisions. Some ECOs have specific Intel® PXA250 and PXA210 applications processors stepping requirements.

Summary of BBPXA2xx Development Baseboard ECOs					
ECO NO.	Rev A	Rev B	Refer to:	Status	ECO Description
1-9					These errata apply to a previously released stepping.
10	X	X	12	Fixed	"UCB1400 Generates Interrupts Incorrectly"
11	X	X	12	Fixed	"USB Cable Attach/Detach Detection Interrupt Is Constantly Asserted"
12	X	X	13	No Fix	"100-MHz SDRAM Failure"
13					There is no ECO 13.
14		X	13	Fixed	"LCD Touch Screen Intermittently Fails"
15		X	15	Fixed	"New Philips UCB1400 Audio Codec on BBPXA2xx Development Baseboard Requires Software Change"
16	X	X	15	No Fix	"Conditional ECO To Use 3.3-V PCMCIA Cards"
17	X	X	15	No Fix	"Conditional ECO To Use The Expansion Port J26"
18	X	X	15	No Fix	"Conditional ECO For USB "Soft Connect" Support"

Summary of DCPXA250 Processor Card ECOs					
ECO NO.	Rev C	Rev D	Refer to:	Status	ECO Description
1-2					These errata apply to a previously released stepping.
3	X		16	Fixed	"VCC_PLL And VCC_CORE Pin Voltage Must Be Equal"
4-5					These errata apply to a previously released stepping.
6	X			Fixed	"50-MHz SDRAM Requires 0-ohm Resistors"
7	X	X	17	Fixed	"For ARM* Multi-ICE* JTAG Use"
8	X		18	Fixed	"Excessive Oscillator Output Voltage to PEXTAL Pin"
9	X	X	19	Fixed	"Coin Cell Battery Issue"
10	X	X	19	Plan Fix	"Signal Integrity Problems On SDCLK"
11-12					These errata apply to a previously released stepping.
13	X	X	20	Plan Fix	"VCC Core Voltage Change"

Summary of DCPXA210 Processor Card ECOs (Sheet 1 of 2)					
ECO NO.	Rev A	Refer to:	Status	ECO Description	
1	X	21	No Fix	"For Multi-ICE JTAG Use"	
2	X	21	No Fix	"MMC MMCLK Support"	

Summary of DCPXA210 Processor Card ECOs (Sheet 2 of 2)				
ECO NO.	Rev A	Refer to:	Status	ECO Description
3	X	21	No Fix	"PLL Voltage Too High"
4	X	22	No Fix	"Remove Coin Cell Battery"
5	X	22	No Fix	"Incorrect Boot Mode Selected For PXA210 Processor"

**Table 1. Minimal Required ECOs for Intel® PXA250 and PXA210 Processor Cards and Intel® BBPXA2xx Baseboards with B1 and B2 Silicon**

Platform	B1 Stepping	B2 Stepping
BBPXA2xx Rev B	10,11, 12, 14,15	10,11, 12, 14,15
DCPXA250 D/C Rev C	3, 6, 7, 8, 9, 10, 13	3, 6, 7, 8, 9, 10, 13
DCPXA250 D/C Rev D	7, 9, 10, 13	7, 9, 10, 13
DCPXA250 D/C Rev E	—	—
DCPXA250 D/C Rev F	—	—
DCPXA210 D/C Rev A	1, 2, 3, 4, 5	1, 2, 3, 4, 5

**NOTE:** Intel recommends that customers should have the minimum platform revisions as listed below:

- B1 silicon or later
- Rev C DCPXA250 processor cards<sup>†</sup>
- Rev A DCPXA210 processor cards
- Rev B BBPXA2xx Development Baseboards

<sup>†</sup>Rev F DCPXA250 processor cards are recommended for systems using 100-MHz SDRAM

# Intel® BBPXA2xx Development Baseboard

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## 10. UCB1400 Generates Interrupts Incorrectly

**Problem:** The Philips UCB1400 interrupt signal is inverted.

**Implication:** The UCB1400 generates interrupts incorrectly.

**Workaround:** Reprogram FPGA U53/U54 with latest code. Refer to <http://developer.intel.com> for latest FPGA updates.

**Status:** Fixed

**Board Rev:** Rev A and B

## 11. USB Cable Attach/Detach Detection Interrupt Is Constantly Asserted

**Problem:** Due to the hardware implementation of the USB cable detection feature, either the attach or detach interrupt is constantly asserted depending on the attach or detach state of the cable.

**Implication:** Software does not know if there is a connect or disconnect. Incorrect USB state can be read

**Workaround:** Perform the following steps to fix the problem.

1. Replace U12, MAX6348XR40 with MAX6379XR44.
2. Update U53/U54 with the latest code. Refer to <http://developer.intel.com> for latest FPGA updates.

One bit was added in the Miscellaneous Read register, bit 9, for cable detection state. Bit 9: logic low = attach, logic high = detach. There are now two interrupt register bits both in the Interrupt Mask/Enable and Interrupt Set/Clear registers to handle USB cable attach/detach states. Bit 2 is the interrupt bit for attach and bit 6 is the interrupt bit for detach in both registers. Users must use each register's associated mask-bit accordingly. That is, users cannot clear the attach interrupt register if the USB cable is attached. Users must determine the state of the cable attach using bit 9 in the Miscellaneous Read register and then mask the associated interrupt bit in the Interrupt Mask/Enable register. Refer to the *Intel® DBPXA250 and DBPXA210 Development Platforms for Intel® Personal Internet Client Architecture User's Guide* for more information.

**Status:** Fixed

**Board Rev:** Rev A and B

**12. 100-MHz SDRAM Failure**

**Problem:** Excessive ringing on SDCLK pin.

**Implication:** SDRAM does not run at 100 MHz.

**Workaround:** For 100-MHz SDRAM development, Intel recommends using Rev F of the DCPXA250 processor card in addition to this workaround. Contact your local Intel representative for availability.

Add a resistor termination network at the end of the SDCLK1 clock line.

1. Locate C68 on the top of the BBPXA2xx development baseboard. Solder one end of a 100-ohm, 0805 resistor to the plus (+) side of C68. Point this 100-ohm, 0805 resistor straight up.
2. Solder one end of a 470-ohm, 0805 resistor to the ground side of C68. Point the 470-ohm, 0805 resistor straight up.
3. Connect the open sides of both the 100-ohm and 470-ohm resistors together with a small gauge rework-wire.
4. Connect this junction to U40, pin 44.

**Status:** No Fix

**Board Rev:** Rev A and B

**14. LCD Touch Screen Intermittently Fails**

**Problem:** LCD screen is open to excessive noise disruption on the touch screen.

**Implication:** Excessive noise disruption reduces LCD screen display quality. The touch screen may not work correctly.

**Note:** BBPXA2xx development baseboards received after December 2001 do not require this ECO. The manufacturing process was changed to incorporate this ECO.

**Workaround:** Fix this problem by covering the back light inverter with copper foil shielding tape to decrease the electrical noise transferred to the LCD and Touch Screen.

**Material Needed:**

- 1-inch heat shrink tubing.
- 2-inch wide EMI Copper Foil Shielding Tape.

**Procedure:**

1. Disassemble the BBPXA2xx development baseboard touch screen enclosure.
2. Remove the back light inverter.
3. Cut a piece of heat shrink tubing (1"x3") and place over the inverter.
4. Heat the tubing until it collapses on the inverter.
5. Cut a 2"x5" piece of copper tape and place on clear plastic disk covering the inverter. The adhesive side should face the plastic.
6. Cut a 2"x5" piece of copper tape and place on the black plastic disk under the inverter. The adhesive side should face the back of the LCD metal enclosure.
7. Reassemble the touch screen enclosure.

Figure 3. LCD Picture 1



Figure 4. LCD Picture 2

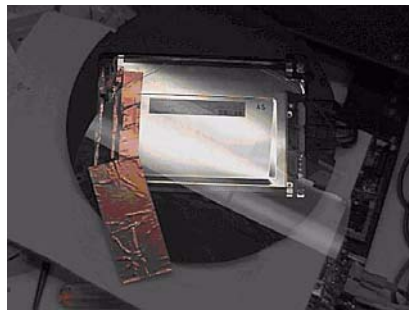
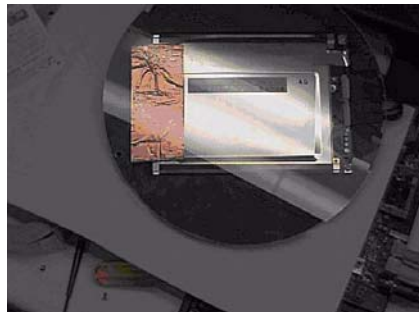


Figure 5. LCD Picture 3



Status: Fixed  
Board Rev: Rev B

**15. New Philips UCB1400 Audio Codec on BBPXA2xx Development Baseboard Requires Software Change**

**Problem:** There is a new revision of the Philips UCB1400 audio codec. BBPXA2xx development baseboards are now using UCB1400 Rev 2A (CB0829). The previous revision of the UCB1400 is Rev 1B (CA5878). There are software changes that are required to support the new revision of the UCB1400.

**Implication:** Current production versions of BBPXA2xx development baseboards use the new revision of the UCB1400.

**Workaround:** Versions of Windows CE and Diagnostic Manager released after April 1st, 2002 automatically detect the revision of the UCB1400 and configure it accordingly. Users writing their own software for the UCB1400 should refer to the latest Philips UCB1400 documentation to ensure they are configuring the new revision appropriately.

**Status:** Fixed

**Board Rev:** Rev B

**16. Conditional ECO To Use 3.3-V PCMCIA Cards**

**Problem:** The BBPXA2xx development baseboard does not support 3.3-V PCMCIA cards because it has a 5-V PCMCIA slot.

**Implication:** 3.3-V PCMCIA cards cannot be inserted into the 5-V slot.

**Workaround:** Replace 5-V PC-card header connector (part #535651-1) on the BBPXA2xx I/O board with 3.3-V PC-card header connector (part #535651-2).

**Status:** No Fix

**Board Rev:** Rev A and B

**17. Conditional ECO To Use The Expansion Port J26**

**Problem:** The BBPXA2xx development baseboard does not support interfacing to the expansion port J26. The X-RDY signal is tied low via R76B. This renders the port inactive.

**Implication:** Users of the BBPXA2xx development baseboard cannot use the expansion bus for development.

**Workaround:** Remove R76B and update U46 with the latest CPLD code. Refer to <http://developer.intel.com> for latest CPLD updates.

**Status:** No Fix

**Board Rev:** Rev A and B

**18. Conditional ECO For USB “Soft Connect” Support**

**Problem:** The UDC+ signal is pulled-up to 3.3 V via resistor R109B (bottom of the baseboard).

**Implication:** Development of applications using the USB “soft-connect” feature that are supported by some operating systems cannot be developed on the BBPXA2xx development baseboard.

**Workaround:** Lift the 1.5-Kohm resistor, R109B (turn it side ways to disconnect it from +3.3 V). The 3.3 V side is closest to the edge of the board and connect the wire from lifted side of this resistor to J20 pin5.

**Status:** No Fix

**Board Rev:** Rev A and B

# Intel® DCPXA250 Processor Card

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### 3. VCC\_PLL And VCC\_CORE Pin Voltage Must Be Equal

**Problem:** The Intel® PXA250 and PXA210 Application Processors Developer's Manual states VCC\_PLL requires VCC\_CORE voltage instead of a separate voltage supply.

**Implication:** The PXA250 processor may not work if VCC\_PLL is not equal to VCC\_CORE.

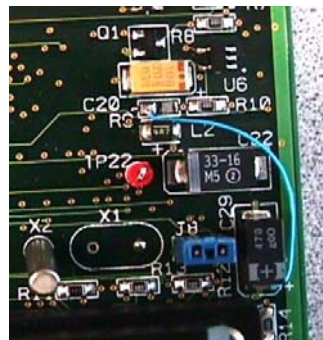
**Workaround:** Perform the following steps to fix the problem.

1. Remove R9.
2. Add a 30-AWG wire from the R9 pad (inductor L2 side) to the positive side of C29. This can be done on the top of the board.

**Status:** Fixed

**Board Rev:** Rev C

**Figure 6. R9 Pad to C29**



### 6. 50-MHz SDRAM Requires 0-ohm Resistors

**Problem:** Incorrect value resistor packs installed on Rev C DCPXA250 processor cards.

**Implication:** SDRAM at 50 MHz could fail.

**Workaround:** Replace RP7, RP8, RP9, RP12, RP13, RP15, RP16, RP17, RP18, RP19, RP20, RP21B, RP23B, RP25B, RP26B, RP27B, RP28B with a 0-ohm resistor pack (Bourns CAY16-000J4). 0-ohm resistors are recommended by the Intel® PXA250 and PXA210 Applications Processors Design Guide.

**Status:** Fixed

**Board Rev:** Rev C



**7. For ARM\* Multi-ICE\* JTAG Use**

**Problem:** JTAG connection fails when using ARM Multi-ICE tools.

**Implication:** No JTAG debugging facility is available with ARM Multi-ICE.

**Workaround:** Perform the following steps to fix the problem.

*Note:* This ECO does not affect the performance of other JTAG tools.

1. Cut the trace on the top of the processor card between U1 pin 3 and via to the right.
2. Add 30-AWG wire from the J3-3 to the via of U1 pin 1 on the bottom of the processor card.

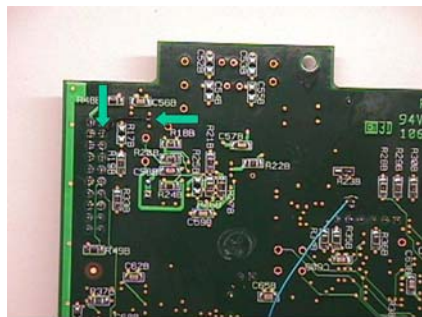
*Note:* Step 3 is not required for the Rev C and Rev D DCPXA250 processor cards and ARM Multi-ICE with their own power supply.

3. Add a 30-AWG wire from J3-2 to +3.3 V.

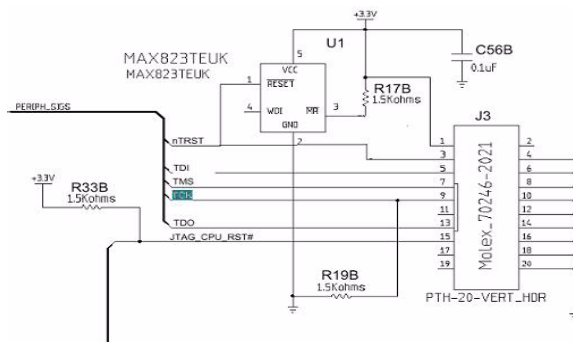
**Status:** Fixed

**Board Rev:** Rev C and D

**Figure 7. Wire From The J3-3 To The Via Of U1 Pin 1**



**Figure 8. Schematic Of JTAG Modification**



## 8. Excessive Oscillator Output Voltage to PEXTAL Pin

**Problem:** On systems using an oscillator to drive PEXTAL, the 3.3 V output from the oscillator is too high.

**Implication:** Possible damage to chip.

**Workaround:** Follow the steps below:

**Note:** These steps bring the oscillator voltage down to 1.1 V. The oscillator and core voltages need to be equal.

1. Attach one side of a 430-ohm resistor to the bottom (on the bottom of the processor card) of TP19 (ground).
2. Attach a 30-AWG wire from the remaining side of the 430-ohm to crystal X1 (The pin closest to the edge of the board).
3. Attach one side of a 620-ohm resistor to the junction of the wire and the 430-ohm resistor. The two resistors will “sandwich” the wire going to X1.
4. Attach another 30-AWG wire from the +3.3 V oscillator output (bottom of U7) to the open end of the 620-ohm resistor.

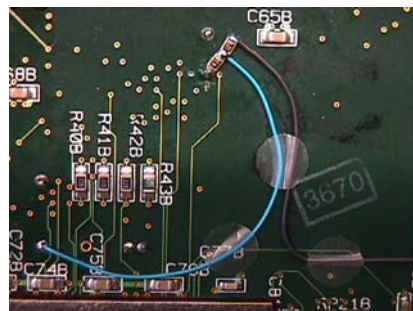
**Status:** Fixed

**Board Rev:** Rev C

**Figure 9. Voltage Divider**



**Figure 10. Close-up of Voltage Divider**



**9. Coin Cell Battery Issue**

**Problem:** Specification change to BATT\_VCC. Stop using the backup battery and connect BATT\_VCC to VCCQ.

**Implication:** VCCQ might attempt to charge battery if BATT\_VCC is lower than VCCQ

**Workaround: For Rev C boards:**

1. Remove CR2032 coin cell battery from battery holder B1.
2. Remove the 0-ohm resistor R23B.
3. Install, on the bottom of the board, a 30-AWG wire between TP11 (red) and J8 pin 1 (VCCQ).

**For Rev D boards:**

1. Remove CR2032 coin cell battery from battery holder B1.
2. Remove the 0-ohm resistor R23B.
3. Install, on the bottom of the board, a 30-AWG wire between TP11 (red) and TP30 (red).

**Status:** Fixed

**Board Rev:** Rev C and D

**10. Signal Integrity Problems On SDCLK**

**Problem:** Signal integrity problems on SDCLK.

**Implication:** Unstable operation with 100-MHz SDCLK.

**Workaround:** For 100-MHz SDRAM development, Intel recommends using Rev F of the DCPXA250 processor card in place of this procedure. Contact your local Intel representative for availability.

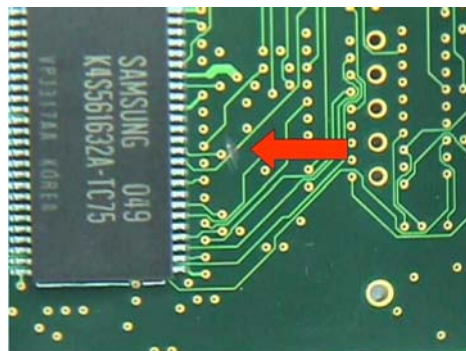
Use the following procedure to improve the SDCLK signal integrity.

1. Cut the trace exiting U10B, pin 38 on the bottom of the DCPXA250 processor card.
2. Update CPLD U4 with latest code. Refer to <http://developer.intel.com> for latest CPLD updates. This adjusts the voltage (VCC) from +1.2 V to +1.4 V.

**Status:** Plan Fix

**Board Rev:** Rev C and D

**Figure 11. U10B Trace Cut Pin 38**



**13. VCC Core Voltage Change**

**Problem:** VCC core voltage requires change.

**Implication:** Unstable operation at 400 MHz.

**Workaround:** Update U4 CPLD with latest code. Refer to <http://developer.intel.com>.

**Status:** Plan Fix

**Board Rev:** Rev C & Rev D cards

# Intel<sup>®</sup>DCPXA210 Processor Card

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## 1. For Multi-ICE JTAG Use

**Problem:** JTAG connection fails when using ARM Multi-ICE tools.

**Implication:** No JTAG debugging facility available with ARM Multi-ICE.

**Workaround:** Use the following steps to

1. Cut a trace on the front of the board between U1 pin 3 and via to the right.
2. Add 30-AWG wire from J2-3, to the bottom via of U1 pin1.

**Note:** Step 3 is not required for the Rev A DCPXA210 processor cards and ARM Multi-ICE with their own power supply.

3. Add 30-AWG wire from J2-2 to +3.3 V.

**Note:** Perform this modification only if using the ARM Multi-ICE tool. This ECO does not affect the performance of other JTAG tools.

**Status:** No Fix

**Board Rev:** Rev A

## 2. MMC MMCLK Support

**Problem:** DCPXA210 processor card does not allow simultaneous support of FFUART and MultiMedia Cards (MMC).

**Implication:** This limits peripheral support to either the FFUART or the MMC.

**Workaround:** Follow the steps below to fix the problem:

1. Remove 0-ohm resistor R17.
2. Add 30-AWG wire from R17 pad (PXA210 pin N14 side) to S5 pin 2.

**Status:** No Fix

**Board Rev:** Rev A

## 3. PLL Voltage Too High

**Problem:** The 3.3V PEXTAL output from the oscillator is too high.

**Implication:** The too high output could cause damage to the PXA250 applications processor.

**Workaround:** The voltage divider lowers the voltage from 3.3 V to approximately 1.1 V.

1. Remove the 0-ohm resistor, R54B, and replace it with a 1-kohm resistor.
2. Attach one side of a 470-ohm resistor to R54B side X1 pin 2 (PEXTAL signal).
3. Run a new wire from the open side of the 470-ohm resistor to GND.

**Status:** No Fix

**Board Rev:** Rev A

#### 4. Remove Coin Cell Battery

**Problem:** Specification change to BATT\_VCC. Discontinue to use the backup battery and connect BATT\_VCC to VCCQ.

**Implication:** VCCQ could attempt to charge battery if BATT\_VCC is lower than VCCQ.

**Workaround:** Follow the steps below to fix the problem:

1. Remove the 0-ohm resistors R29B and R38B and battery holder B1.
2. Add 30-AWG wire from TP11 (red) to TP22 (red).

**Status:** No Fix

**Board Rev:** Rev A

#### 5. Incorrect Boot Mode Selected For PXA210 Processor

**Problem:** The DCPXA210 processor card is configured to boot the PXA210 processor in 32-bit mode.

**Implication:** PXA210 does not function correctly. It only supports a 16-bit data bus.

**Workaround:** Follow the steps below to change the boot mode:

1. Remove the 0-ohm resistor, R65B.
2. Add 30-AWG wire from R65B pad attached to ball F14 to +3.3 V.

**Status:** No Fix

**Board Rev:** Rev A



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