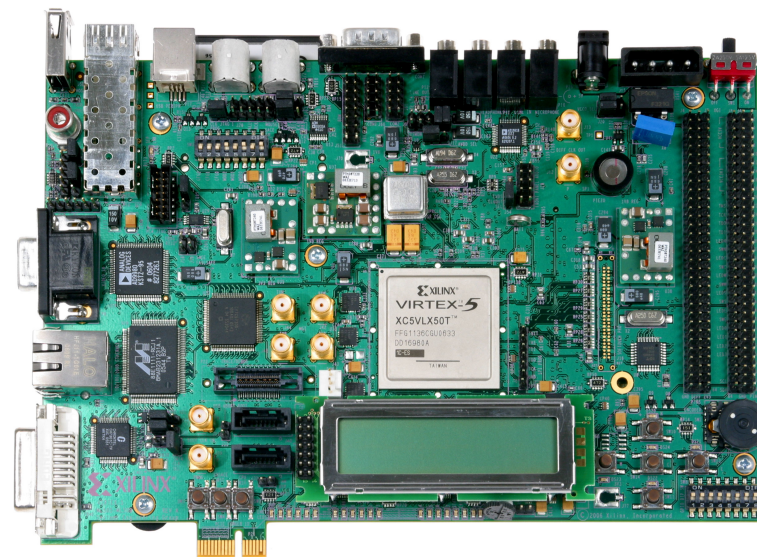




ML505/506 QuickStart

May 2008



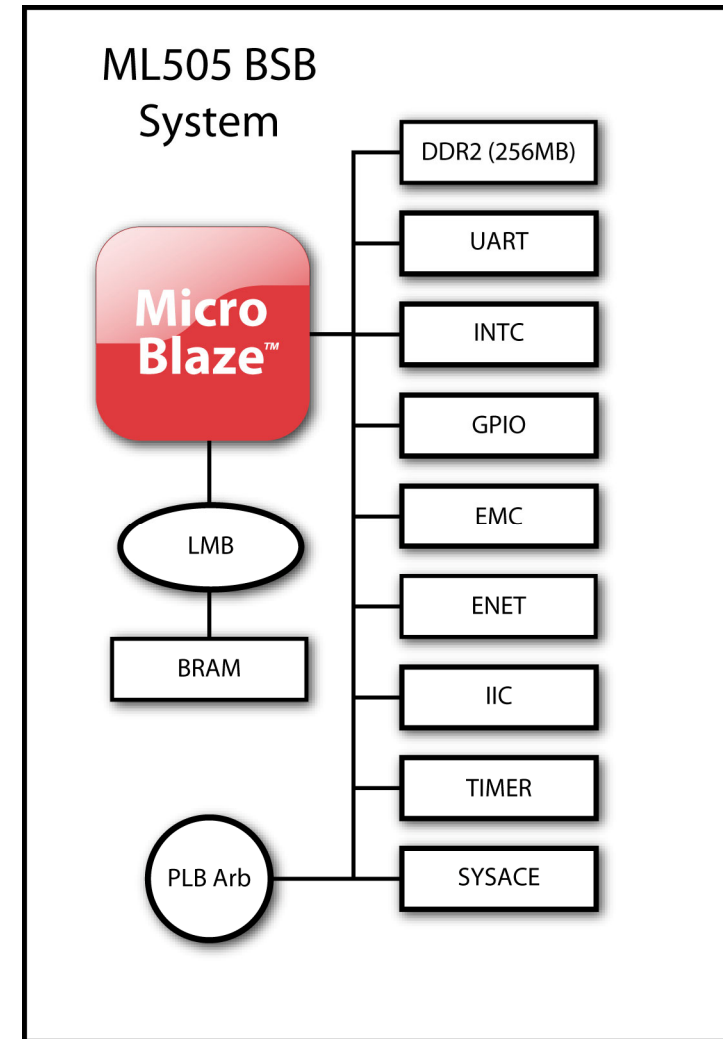
Overview

- Setup
- Boot with ACE-loader ACE File
- Observe LCD and Terminal messages
- Load new Configuration
- Re-load ACE-loader



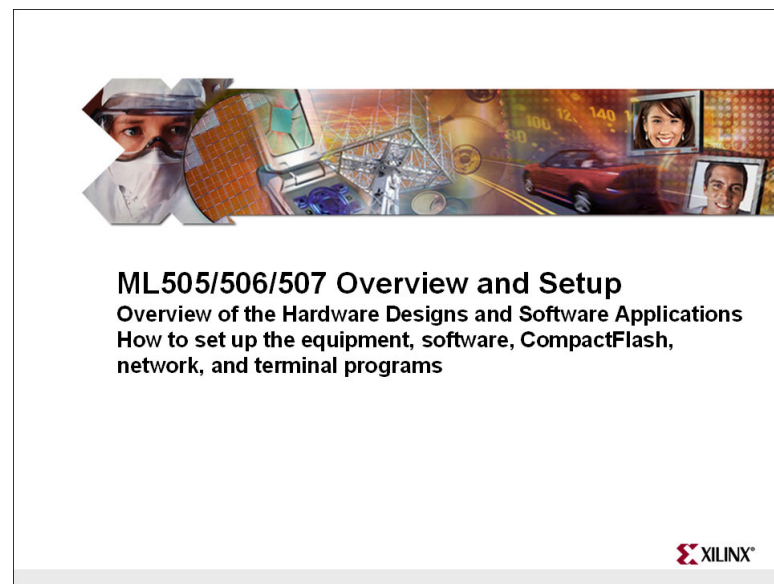
ML505 BSB Hardware

- The ML505 MicroBlaze design hardware includes:
 - DDR2 Interface (256 MB)
 - BRAM
 - External Memory Controller (EMC)
 - **ZBT SRAM**
 - Networking
 - UART
 - Interrupt Controller
 - System ACE CF Interface
 - GPIO (IIC, LEDs and LCD)
 - PLB Arbiter



Additional Setup Details

- Refer to ml505_overview_setup document for details on:
 - Software Requirements
 - ML505 Board Setup
 - **Equipment and Cables**
 - **Software**
 - **Network**
 - Terminal Programs
 - **This presentation requires the 9600-8-N-1 Baud terminal setup**



Hardware Setup

- Connect the Xilinx Parallel Cable IV (PC4) to the ML505 board
- Connect the RS232 null modem cable to the ML505 board



Hardware Setup

- The ML505 uses a DVI video interface
- Connect a DVI monitor
or
- Use a DVI/VGA adapter to connect a VGA monitor
 - <http://www.belkin.com>



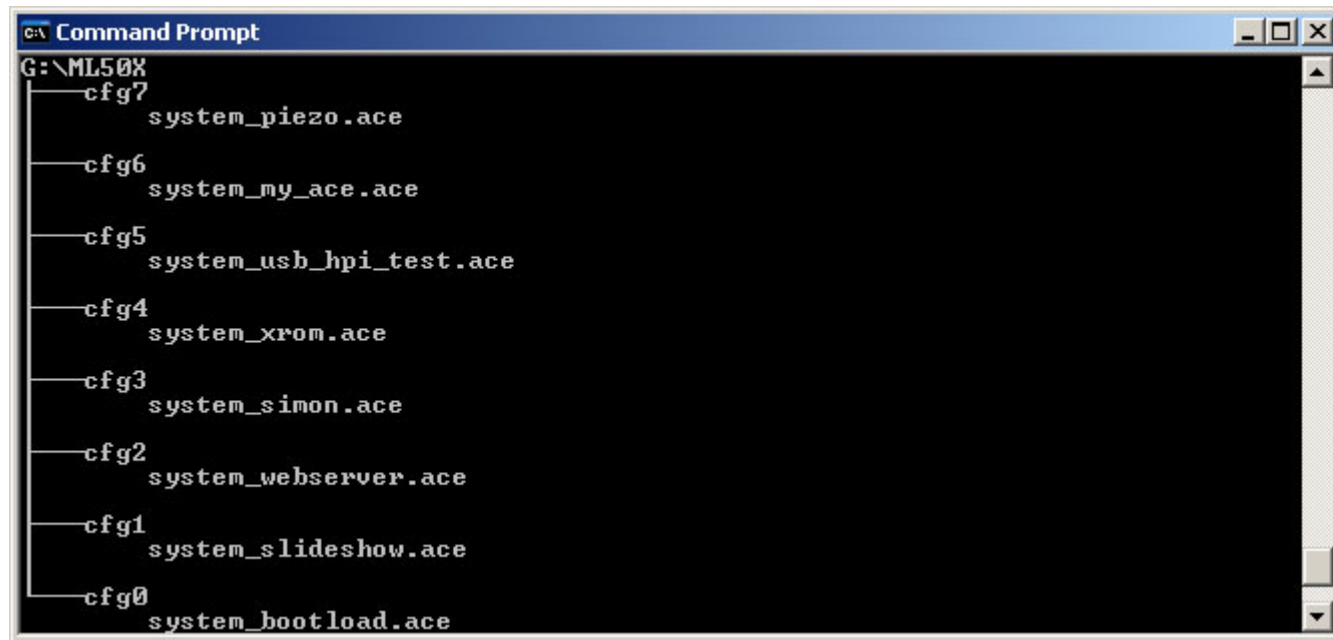
Hardware Setup

- USB Keyboard
 - www.dell.com



Factory CompactFlash

- The CompactFlash shipped with the ML505 board has the following ace files preloaded:

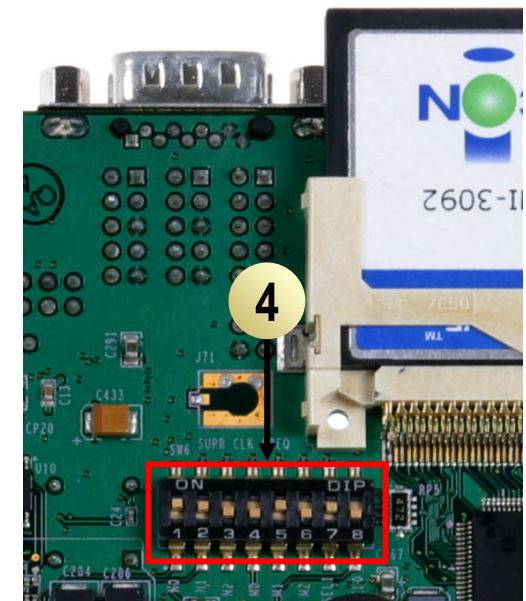
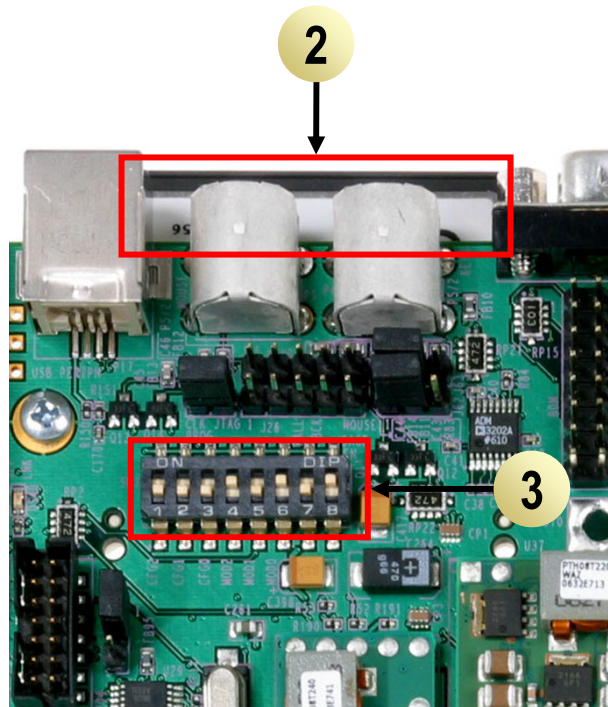
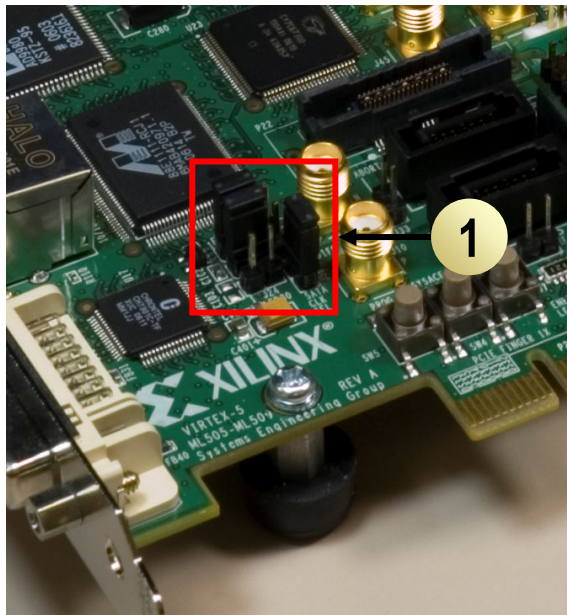


```
G:\ML50X
├── cfg7
│   └── system_piezo.ace
├── cfg6
│   └── system_my_ace.ace
├── cfg5
│   └── system_usb_hpi_test.ace
├── cfg4
│   └── system_xrom.ace
├── cfg3
│   └── system_simon.ace
├── cfg2
│   └── system_webserver.ace
├── cfg1
│   └── system_slideshow.ace
└── cfg0
    └── system_bootload.ace
```



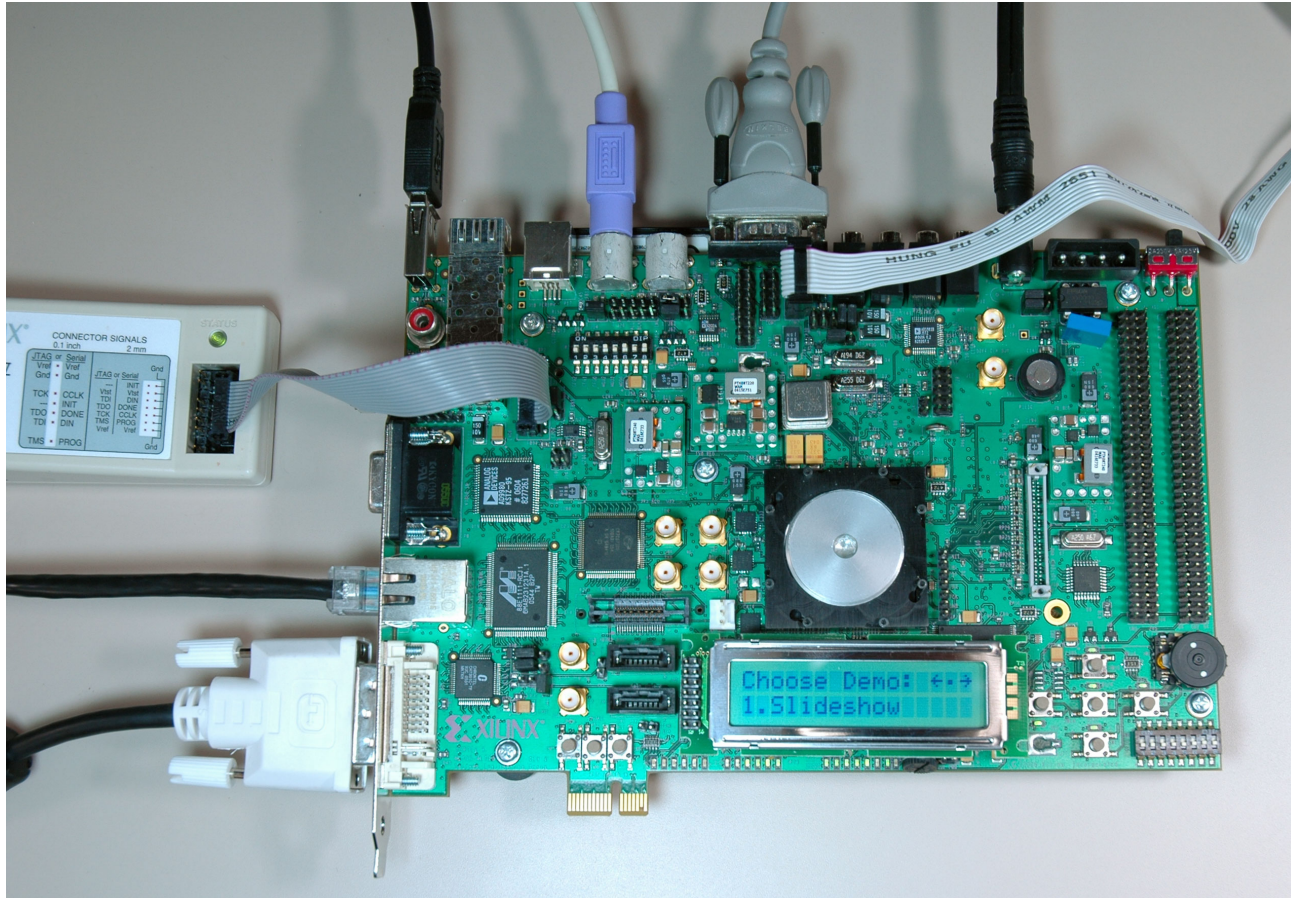
Verify Factory Default Settings

- Set the Ethernet PHY jumpers, J22, J23 to positions 1-2 (1)
- Insert the Factory CompactFlash into the ML505 board (2)
- Set the Front DIP switches (SW3) to 00010101 (1 = ON) (3)
- Set the Rear DIP switches (SW6) to 11001010 (4)
- Power-up the ML505 board



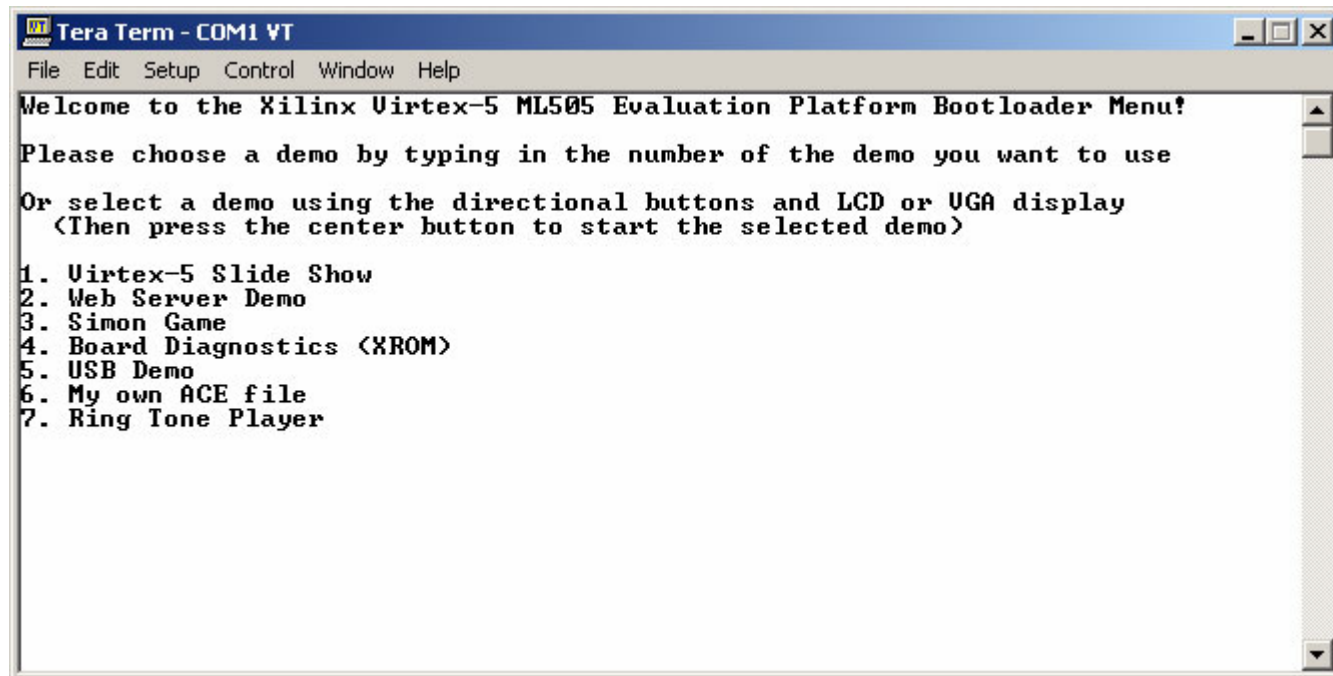
Bootload

- The `system_bootload.ace` loads:



Bootload

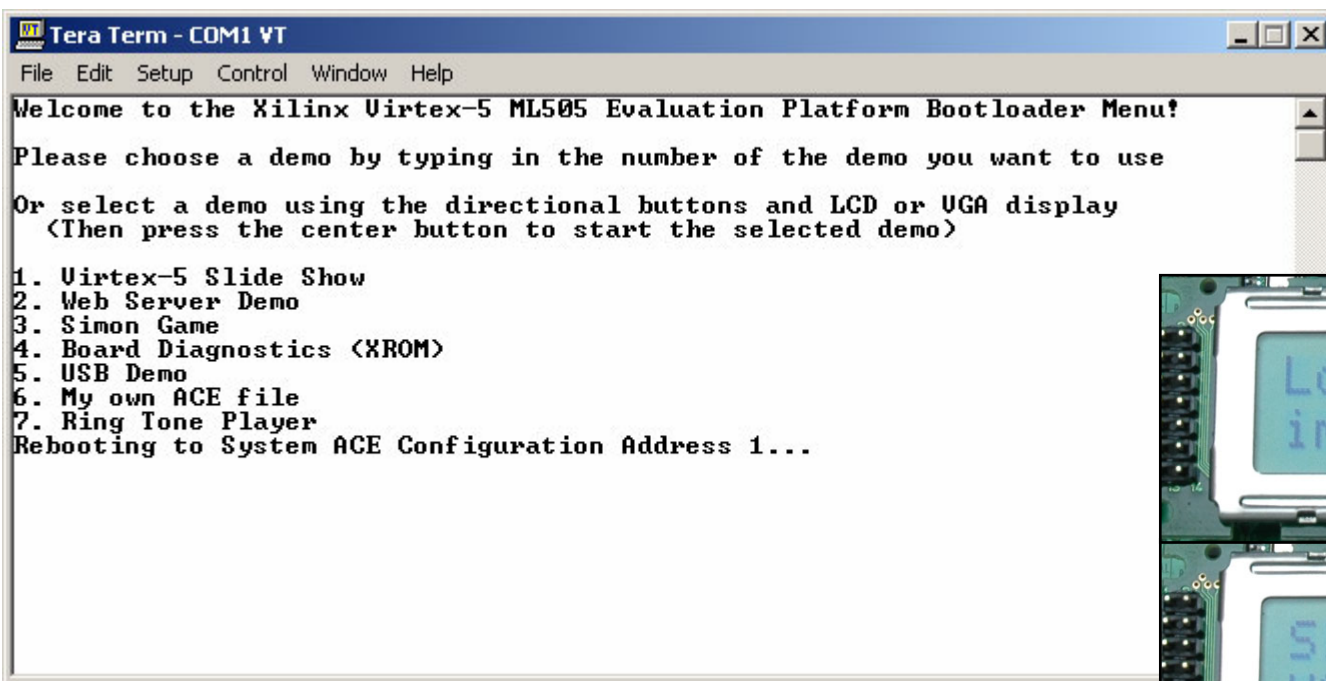
- The terminal window also reflects the bootload application
- Use the left/center/right buttons to choose an application or type a number in the terminal window
- After each demo, push the SysACE reset to return to bootload



```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Welcome to the Xilinx Virtex-5 ML505 Evaluation Platform Bootloader Menu!
Please choose a demo by typing in the number of the demo you want to use
Or select a demo using the directional buttons and LCD or VGA display
(Then press the center button to start the selected demo)
1. Virtex-5 Slide Show
2. Web Server Demo
3. Simon Game
4. Board Diagnostics (XROM)
5. USB Demo
6. My own ACE file
7. Ring Tone Player
```

Slideshow

- Type 1, to launch the slideshow application in Configuration 1
- The slideshow loads the presentation into memory then presents it



Slideshow

- The slideshow app will present a series of slides on the Monitor:

ML505 Board

Virtex-5 LXT FPGAs

Industry's First 65nm Serial I/O Solution

Available Now!

* Comparisons made to 90nm Virtex-4 FPGA devices

Platform Design Tools Deliver Greater Design Productivity

Third Party EDA Software

High QoR: 30% faster Fmax

System Generator, IP, PlanAhead, HDL Coding, Synthesis, Implementation, HW in the Loop, Verification

Virtex-5 FPGAs Provide the Right Mix of Memories

- Distributed LUT RAM
 - Fast, localized memories
 - Built-in shift register
 - Great for small FIFOs
- 550 MHz block RAM / FIFO
 - Bigger on-chip memories
 - Built-in FIFO and ECC logic
 - Great for mid-sized FIFOs/buffers
- External memory interfacing
 - Fast connection to popular standards
 - Memory controller cores
 - Ideal for large memory requirements

LOW-POWER TRANSCEIVERS

Ultimate Connectivity . . .

Low-Power Transceivers
100 Mbps - 3.2 Gbps, <100 mW

Built-in PCIe Interface

Built-in Ethernet MAC

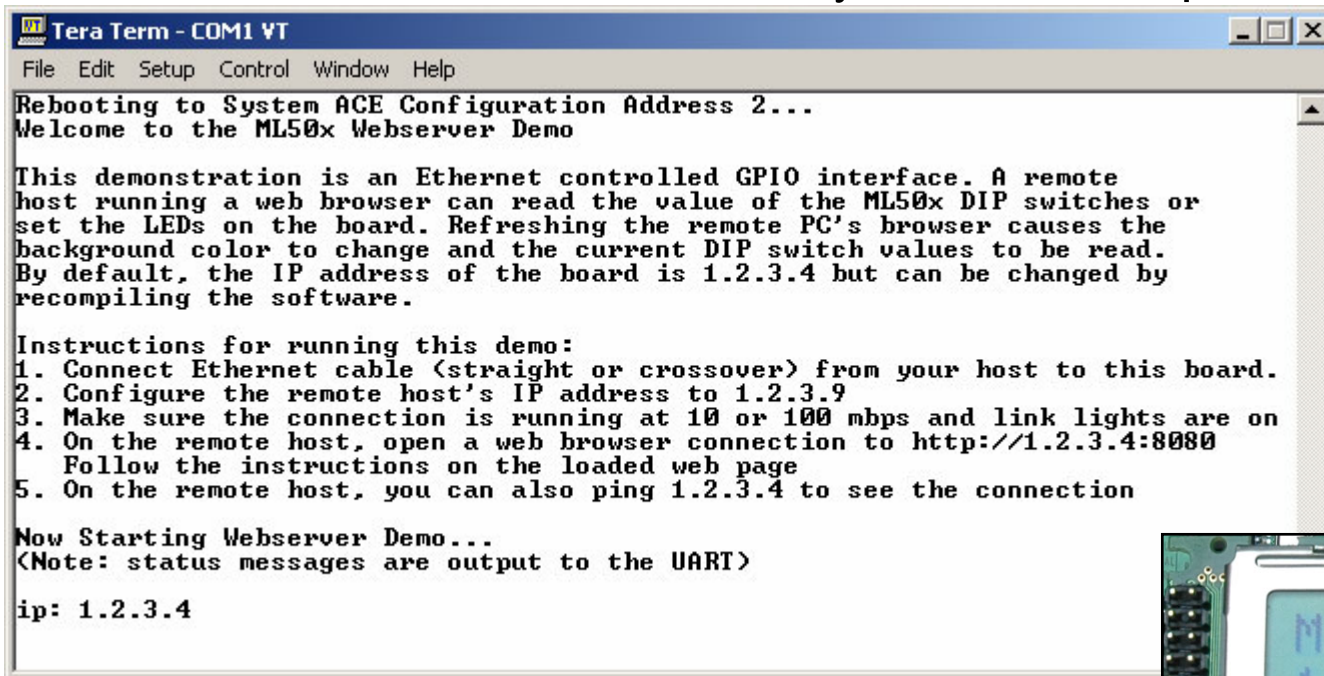
VIRTEX-5 Reduce serial I/O power, cost and complexity with the world's first 65nm FPGAs.

With a unique combination of up to 24 low-power transceivers, and built-in PCIe and Ethernet MAC blocks, Virtex-5 LXT FPGAs get your system running fast. Whether you are an expert or just starting out, only Xilinx delivers this complete solution to simplify high-speed serial design.



Web Server

- Type 2, to launch the web server application in Configuration 2
 - **Note:** You may need to turn off your browser's proxy and specify a direct connection to the Internet in your browser options



```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Rebooting to System ACE Configuration Address 2...
Welcome to the ML50x Webserver Demo

This demonstration is an Ethernet controlled GPIO interface. A remote
host running a web browser can read the value of the ML50x DIP switches or
set the LEDs on the board. Refreshing the remote PC's browser causes the
background color to change and the current DIP switch values to be read.
By default, the IP address of the board is 1.2.3.4 but can be changed by
recompiling the software.

Instructions for running this demo:
1. Connect Ethernet cable (straight or crossover) from your host to this board.
2. Configure the remote host's IP address to 1.2.3.9
3. Make sure the connection is running at 10 or 100 mbps and link lights are on
4. On the remote host, open a web browser connection to http://1.2.3.4:8080
   Follow the instructions on the loaded web page
5. On the remote host, you can also ping 1.2.3.4 to see the connection

Now Starting Webserver Demo...
(Note: status messages are output to the UART)

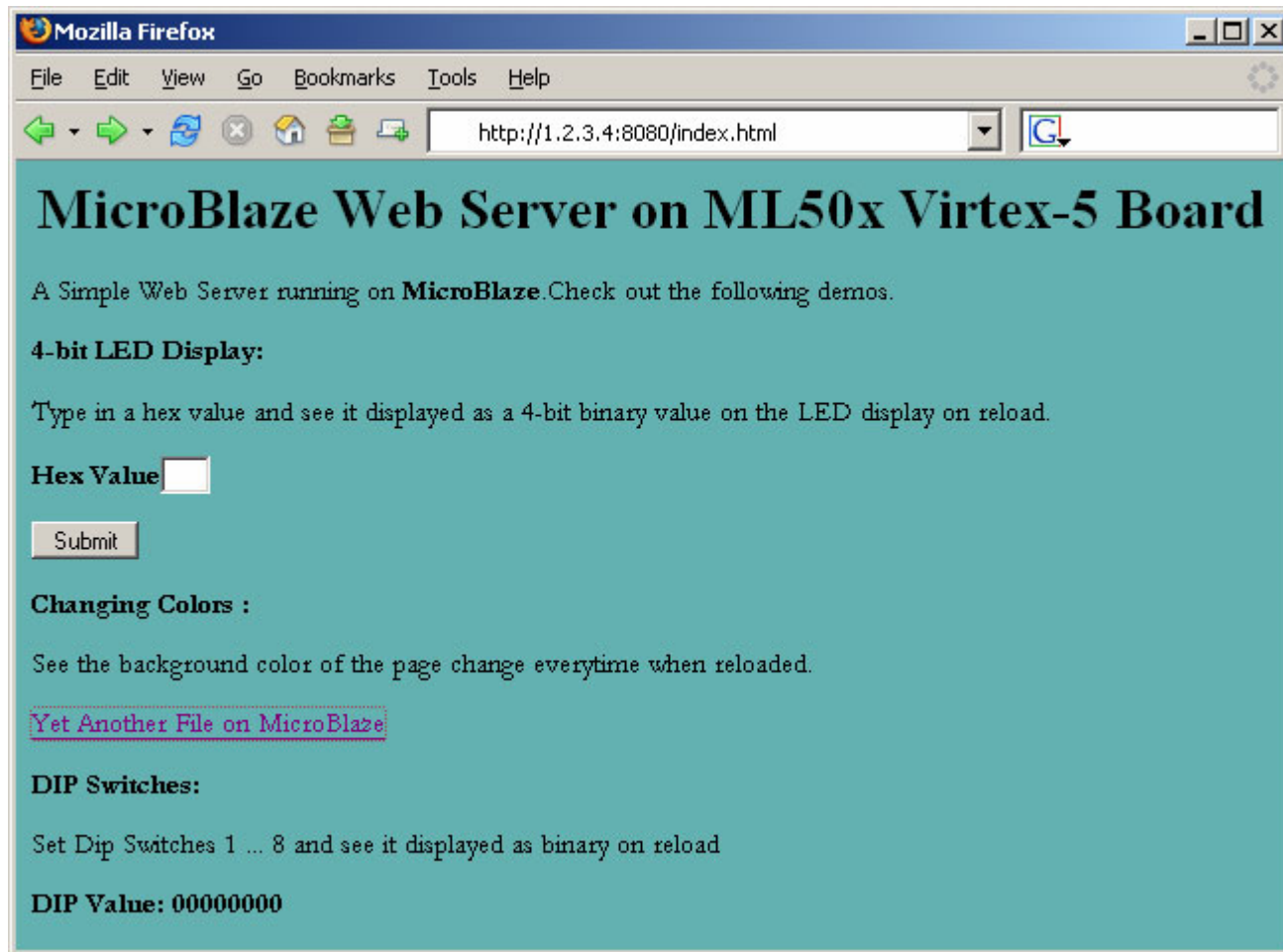
ip: 1.2.3.4
```



Note: Host IP is 1.2.3.9, subnet mask is 255.0.0.0; Ethernet connection is 100 Full Duplex

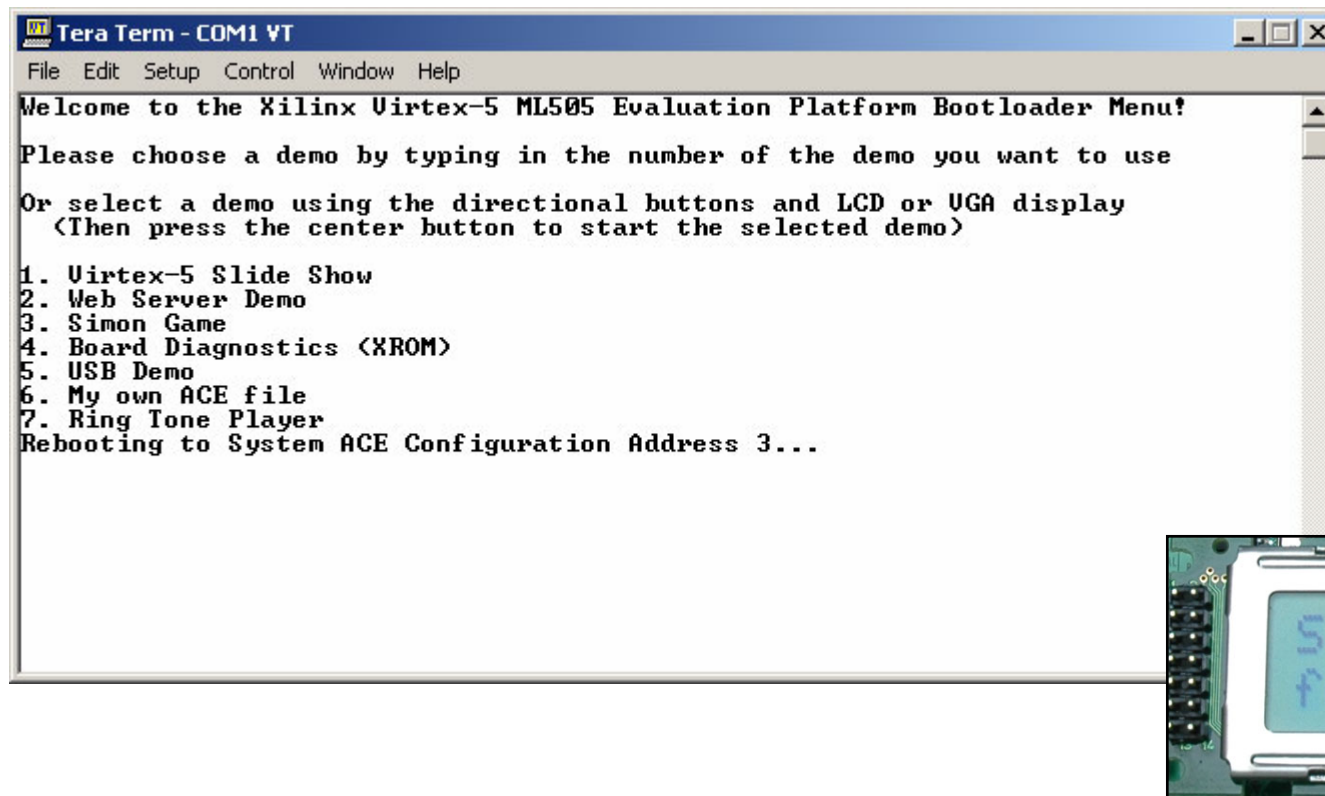
Web Server

- In your web browser, enter `http://1.2.3.4:8080/index.html`



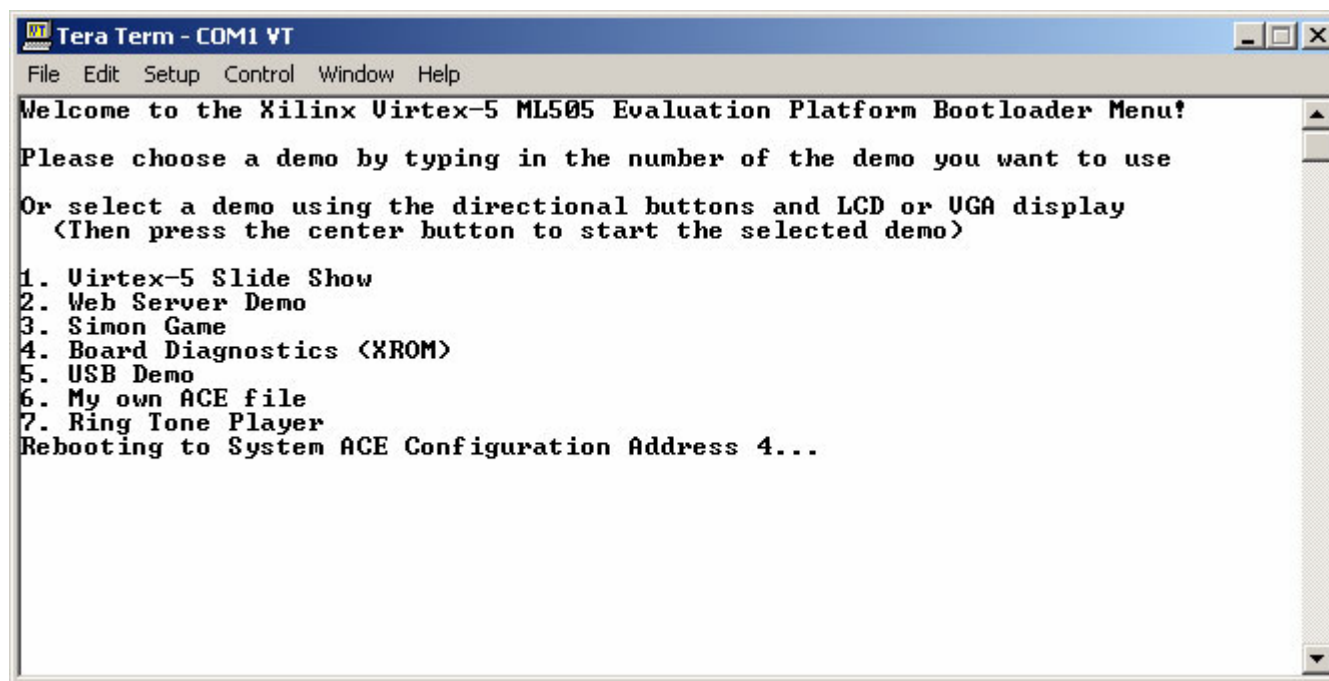
Simon

- Type 3, to launch the Simon application in Configuration 3



Board Diagnostics

- Type 4, to launch the XROM application in Configuration 4

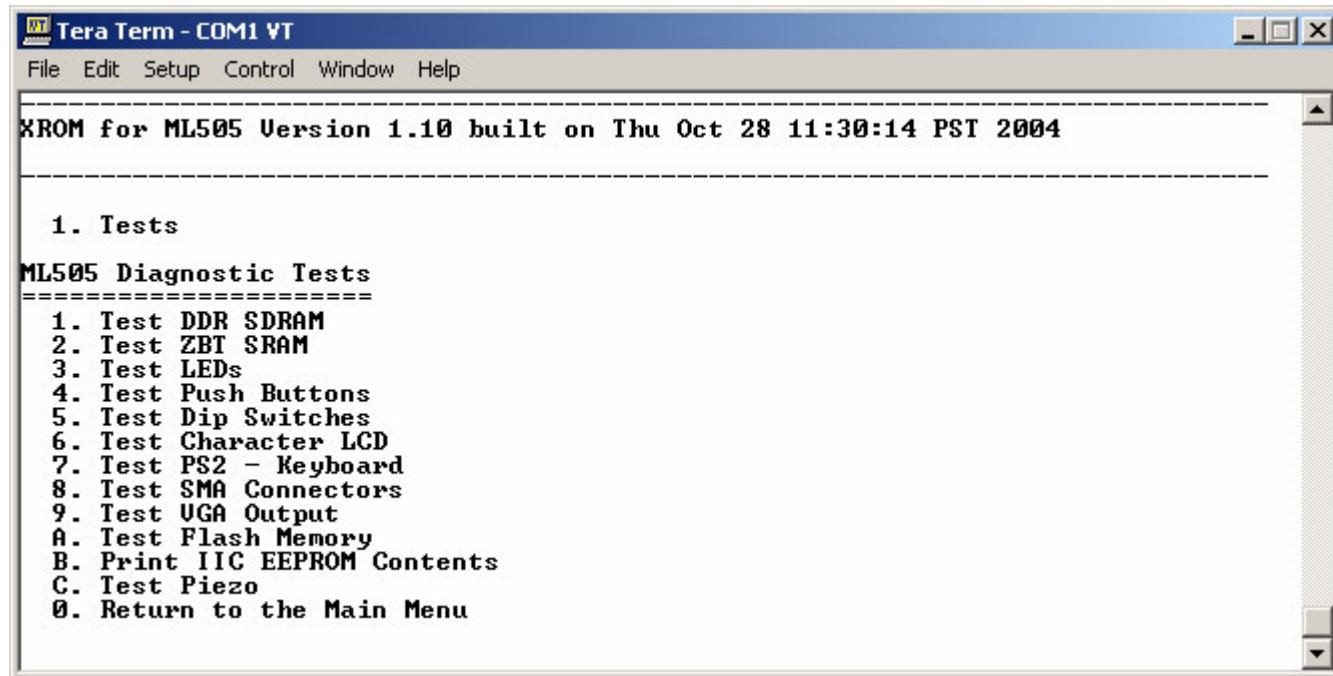


```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Welcome to the Xilinx Virtex-5 ML505 Evaluation Platform Bootloader Menu!
Please choose a demo by typing in the number of the demo you want to use
Or select a demo using the directional buttons and LCD or VGA display
(Then press the center button to start the selected demo)
1. Virtex-5 Slide Show
2. Web Server Demo
3. Simon Game
4. Board Diagnostics <XROM>
5. USB Demo
6. My own ACE file
7. Ring Tone Player
Rebooting to System ACE Configuration Address 4...
```



Board Diagnostics

- XROM includes a series of board test routines

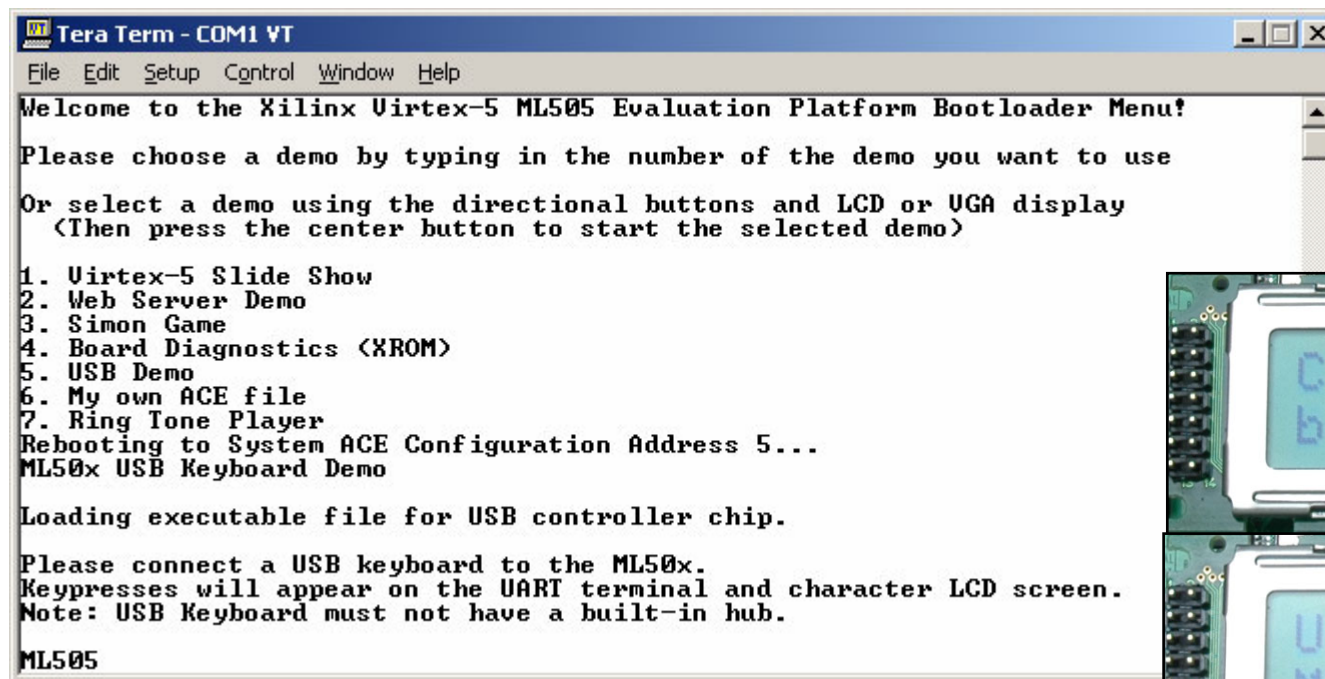


```
Tera Term - COM1 VT
File Edit Setup Control Window Help
-----
XROM for ML505 Version 1.10 built on Thu Oct 28 11:30:14 PST 2004
-----
1. Tests
ML505 Diagnostic Tests
=====
1. Test DDR SDRAM
2. Test ZBT SRAM
3. Test LEDs
4. Test Push Buttons
5. Test Dip Switches
6. Test Character LCD
7. Test PS2 - Keyboard
8. Test SMA Connectors
9. Test UGA Output
A. Test Flash Memory
B. Print IIC EEPROM Contents
C. Test Piezo
0. Return to the Main Menu
```

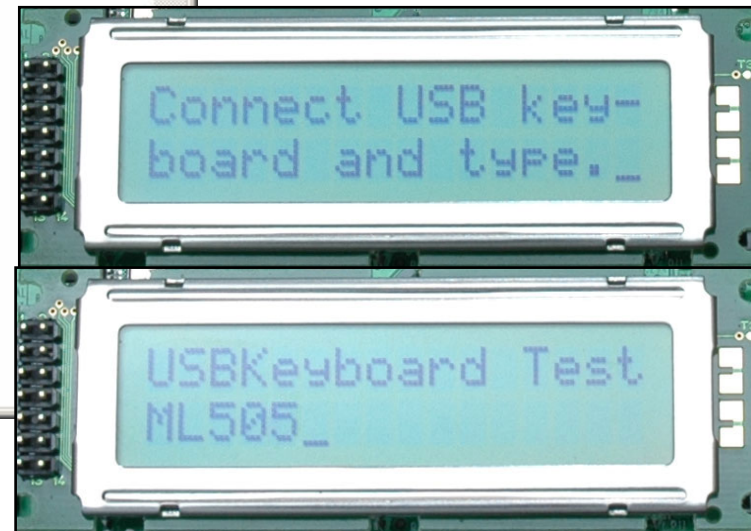


USB Keyboard

- Type 5, to launch the USB Keyboard application in Configuration 5
- Type **ML505** and view results:

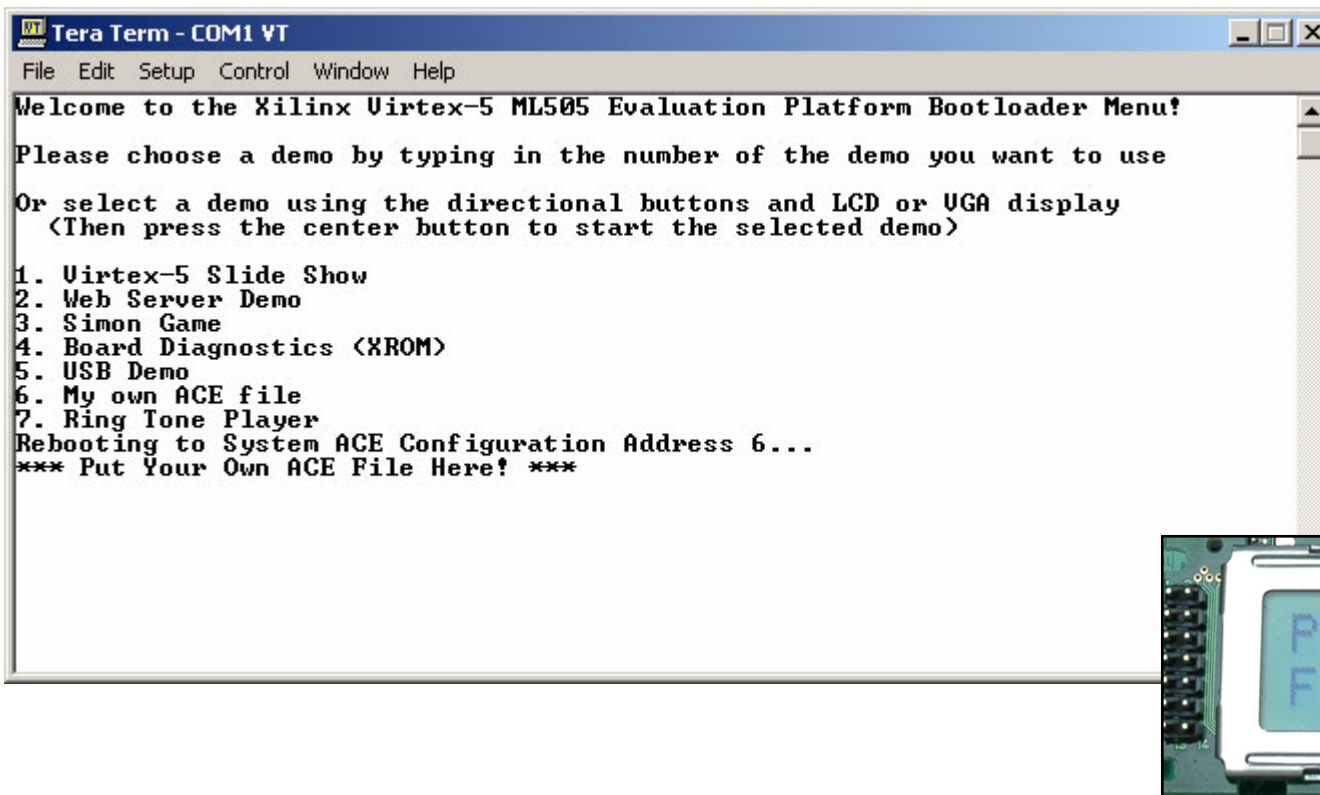


```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Welcome to the Xilinx Virtex-5 ML505 Evaluation Platform Bootloader Menu!
Please choose a demo by typing in the number of the demo you want to use
Or select a demo using the directional buttons and LCD or UGA display
(Then press the center button to start the selected demo)
1. Virtex-5 Slide Show
2. Web Server Demo
3. Simon Game
4. Board Diagnostics (XROM)
5. USB Demo
6. My own ACE file
7. Ring Tone Player
Rebooting to System ACE Configuration Address 5...
ML50x USB Keyboard Demo
Loading executable file for USB controller chip.
Please connect a USB keyboard to the ML50x.
Keypresses will appear on the UART terminal and character LCD screen.
Note: USB Keyboard must not have a built-in hub.
ML505
```



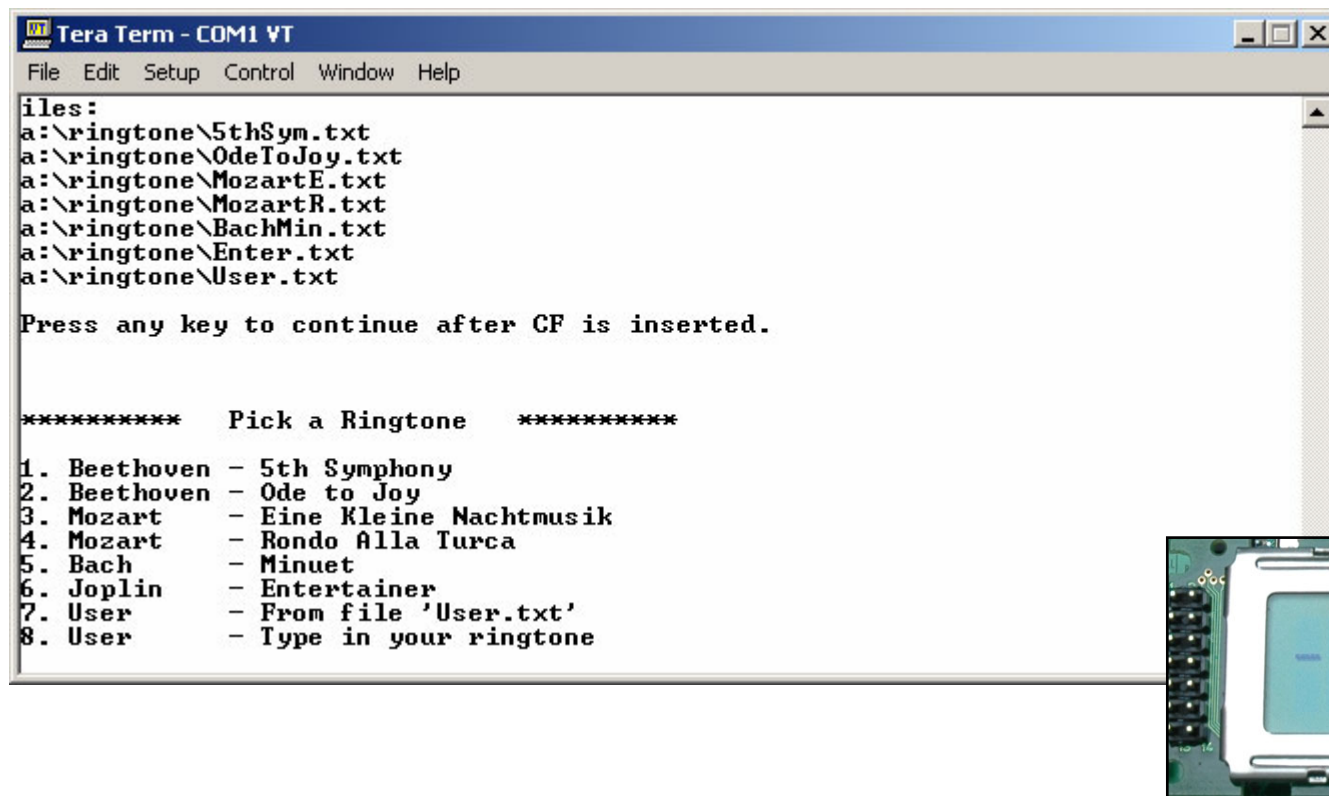
My ACE

- Type 6, to launch the My ACE application in Configuration 6



Ringtone

- Type 7, to launch the Ringtone application in Configuration 7
- Press any key then press 1-7 to play a simple melody



Documentation

- Virtex-5
 - Silicon Devices
http://www.xilinx.com/products/silicon_solutions
 - Virtex-5 Multi-Platform FPGA
http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5
 - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms
http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
 - Virtex-5 FPGA DC and Switching Characteristics Data Sheet
http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf



Documentation

- Virtex-5
 - Virtex-5 FPGA User Guide
http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
 - Virtex-5 FPGA Configuration User Guide
http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
 - Virtex-5 System Monitor User Guide
http://www.xilinx.com/support/documentation/user_guides/ug192.pdf
 - Virtex-5 Packaging and Pinout Specification
http://www.xilinx.com/support/documentation/user_guides/ug195.pdf



Documentation

- Virtex-5 RocketIO
 - RocketIO GTP Transceivers
http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTP.htm
 - RocketIO GTX Transceivers
http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTX.htm
 - RocketIO GTP Transceiver User Guide – UG196
http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
 - RocketIO GTX Transceiver User Guide – UG198
http://www.xilinx.com/support/documentation/user_guides/ug198.pdf



Documentation

- MicroBlaze
 - MicroBlaze Processor
<http://www.xilinx.com/microblaze>
 - MicroBlaze Processor Reference Guide – UG081
http://www.xilinx.com/support/documentation/sw_manuals/mb_ref_guide.pdf



Documentation

- Memory Solutions

- Demos on Demand – Memory Interface Solutions with Xilinx FPGAs

- http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35

- Xilinx Memory Corner

- http://www.xilinx.com/products/design_resources/mem_corner

- Additional Memory Resources

- <http://www.xilinx.com/support/software/memory/protected/index.htm>

- Xilinx Memory Interface Generator (MIG) 2.1 User Guide

- <http://www.xilinx.com/support/software/memory/protected/ug086.pdf>

- Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator

- http://www.xilinx.com/support/documentation/white_papers/wp260.pdf



Documentation

- Ethernet
 - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet
http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_ds550.pdf
 - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide
http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_gsg340.pdf
 - Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide
http://www.xilinx.com/support/documentation/user_guides/ug194.pdf
 - LightWeight IP (lwIP) Application Examples – XAPP1026
http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf



Documentation

- ML505/506/507
 - ML505 Overview
<http://www.xilinx.com/ml505>
 - ML506 Overview
<http://www.xilinx.com/ml506>
 - ML507 Overview
<http://www.xilinx.com/ml507>
 - ML505/506/507 Evaluation Platform User Guide – UG347
http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf
 - ML505/506/507 Getting Started Tutorial – UG348
http://www.xilinx.com/support/documentation/boards_and_kits/ug348.pdf
 - ML505/506/507 Reference Design User Guide – UG349
http://www.xilinx.com/support/documentation/boards_and_kits/ug349.pdf



Documentation

- ML505/506/507
 - ML505/506/507 Schematics
http://www.xilinx.com/support/documentation/boards_and_kits/ml50x_schematics.pdf
 - ML505/506/507 Bill of Material
http://www.xilinx.com/support/documentation/boards_and_kits/ml505_501_bom.xls

