SanDisk SD-ROM Product Manual

Revision 1.0

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1 SD-ROM Card Overview

1.1 Introduction

SanDisk SD-ROM Cards provide permanent and secure read-only data storage for consumer electronic and personal computer applications. SanDisk SD-ROM Cards are based on SanDisk's unique 3D one-time programmable (OTP) memory devices which safely store data for 100 years. This compares favorably with cards based on flash memory devices, which are typically rated to store data for 10 years or less. And unlike cards based on mask ROM memory devices, SanDisk SD-ROM Cards can be programmed immediately before shipping to end-users or retail storefronts, reducing order turn time and inventory requirements.

SanDisk SD-ROM Cards are compatible with the Secure Digital memory card specifications, with some modifications to maximize host device compatibility. Matsushita Electric Industrial Co. Ltd., SanDisk Corporation and Toshiba Corporation (SD-3C, LLC) originally defined specifications for the SD Card. SD card specifications are now maintained, controlled and assigned by the SD-3C, LLC. While a formal SD-ROM card specification does not yet exist, the SanDisk SD ROM Card has been designed to be compatible with most SD host devices today.

SanDisk SD-ROM Cards implement the 9-pin SD card interface and support a maximum operating frequency of 25 MHz and an operating voltage range of 2.7 – 3.6v. The industry-standard SD interface allows for easy integration into any design, regardless of which type of microprocessor is used. In addition to the SD interface, the SanDisk SD-ROM Card interface offers an alternate communication protocol based on the SPI standard. With some additions, the physical form factor, pin assignment, and data transfer protocol are forward compatible with current and future SanDisk SD Card products.

SanDisk SD-ROM Cards are available in 32, 64, and 128 megabyte (MB) capacities.

1.2 Feature Summary

General features of SanDisk SD-ROM Cards include:

- Archival data storage with over 100 year data storage lifetime
- Convenient form-factor, ideal for portable and stationary applications for content storage
- Card capacities of 32, 64, and 128MB
- Supports industry-standard SD and SPI interfaces
- Voltage range of 2.7 to 3.6V
- Variable clock rate of 0 - 25 MHz

1.3 SD Card Standard

SanDisk SD-ROM Cards are compatible with the SDA Physical Layer Specification, Version 2.00. This specification is available from the SD Card Association (SDA).

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2 SanDisk SD-ROM Card Functional Description

SanDisk SD-ROM Cards are compatible with the SD specifications, with some changes necessary for a read-only memory.

In an SD host system, the host controls all communication between itself and the cards. For detailed information, refer to Section 4 of the SDA Physical Layer Specification, Version 2.00.

This chapter contains the functional description for SanDisk SD-ROM Cards.

2.1 SD Bus Protocol

Communication over the SD bus is based on command and data-bit streams initiated by a start bit and terminated by a stop bit. See Section 3.6.1 of the SDA Physical Layer Specification, Version 2.00, for details.

2.2 SPI Mode

The SPI Mode is a secondary communication protocol for cards in the SanDisk SD-ROM Cards. This interface mode is an alternate to the SD protocol and is designed to communicate with an SPI channel, commonly found in Motorola and other vendors' microcontrollers. More information about SPI Mode can be found in Section 7 of the SDA Physical Layer Specification, Version 2.00.

2.3 Cyclic Redundancy Codes

Cyclic Redundancy Codes (CRC) protect against transmission errors that may occur on the bus in SD systems. Detailed information and examples for CRC7 and CRC16 are provided in Section 4.5 of the SDA Physical Layer Specification, Version 2.00.

2.4 Clock Control

The host can use the bus clock signal to SanDisk SD-ROM Cards to decrease power consumption or to control data flow on the bus. See Section 4.4 of the SDA Physical Layer Specification, Version 2.00.

2.5 Sleep Mode

SanDisk SD Cards implement a feature to automatically enter and exit from sleep mode. Upon completion of an operation, cards enter sleep mode to conserve power if no additional commands are received in less than 5 milliseconds (ms). The host does not have to take any action for this to occur; however, in order to achieve the lowest sleep current, the host should also shut down its clock to the card. In most systems, cards are in sleep mode except when accessed by the host, thus conserving power.

When the host is ready to access a card in sleep mode, any command issued to the card will cause it to exit sleep mode and respond.

2.6 Hot Insertion

SanDisk SD-ROM Cards support hot insertion into a powered host device through SD connectors that have power pins that make contact before the signal pins. This approach is similar to that used in PCMCIA and MMCA devices to allow for hot insertion. For more information, refer to Section 6.1 and Section 6.2 of the SDA Physical Layer Specification, Version 2.00.

2.7 Card State Transitions

SanDisk SD-ROM Cards operate the same as standard SD cards, where the state transition is dependent on the received command along with responses sent on the command line. The transitions are defined in Section 4.8 of the SDA Physical Layer Specification, Version 2.00

In Card Identification Mode, the host operates the card at a slower frequency as it identifies and initializes the card. For more information see Section 4.2 in the SDA Physical Layer Specification, Version 2.00.

In Data Transfer Mode, the host may increase the card interface frequency to the maximum allowed frequency; it is in this mode that the host issues data read and write and other related commands. For more detailed information, refer to Section 4.3 of the SDA Physical Layer Specification, Version 2.00.

Error conditions are described in Section 4.6 of the SDA Physical Layer Specification, Version 2.00.

2.8 Supported Commands

SanDisk SD-ROM Card support the commands in the Basic (class 0), Block Read (class 2), Application Specific (class 8), and Switch (class 10) command classes only. The commands in the Write (class 4), Erase (class 5), Write Protection (class 6), and Lock/Unlock (class 7) command classes are not applicable for a ROM card and are not supported; refer to the next section for more information.

See the SDA Physical Layer Specification, version 2.00, Section 4.7 for detailed information about card commands and Section 4.12 for timing diagrams and values.

2.9 SD-ROM Card Functional Behavior

In order to maximize compatibility and host interoperability, even though the SD-ROM card provides read-only access to its memory contents, it will appear to the host system as a standard read/write card. This is because many host devices assume all SD cards are read/write and will reject a ROM-type card.

Specifically, even though the SanDisk SD-ROM card does not support Write (class 4), Erase (class 5), Write Protection (class 6), and Lock/Unlock (class 7) commands, it will be configured to report to the host system that it supports those commands by setting the Card Command Class field in the CSD register to 5F5h. If a command from these groups is issued by the host, the card will accept the command without generating an error, but will not perform it.

In addition, the card will also appear to be non-write-protected (the PERM_WRITE_PROTECT and TEMP_WRITE_PROTECT bits in the CSD will be clear). If the host issues a write command, the card will accept the command without generating an error, but will not perform it.

Finally, the SD-ROM card does not support SD security commands. The SD_Security field in the SCR register is set to 0h, indicating no security support.

3 SanDisk SD-ROM Card Specifications

3.1 Operating Specifications

The table below summarizes the SD-ROM operating specifications.

Parameter	Value	Notes
Supply Voltage	2.0 – 3.6v	during card identification for version 1.1 cards
	2.7 – 3.6v	all supported commands
Operating Temperature	-25 – 85 °C	
Storage Temperature	-40 – 85 °C	
Data Retention	100 years minimum	
Data Endurance	$1x10^9$ read cycles	
Interface speed	0 – 25MHz	variable clock rate
Read Bandwidth	1.8MB/s minimum	sequential read, 25MHz interface speed
Read Current	50mA typical 75mA maximum	maximum at 3.6v, 85 °C
Sleep Current	250uA maximum	
Reset to Read Latency	300ms	
Read Command Response	100ms	

3.2 Memory Capacity

SanDisk SD-ROM Cards are sold preloaded with an OEM-specified image which may or may not have a file system. In general, a file system provides structure for data; the SD Card File System Specification, published by the SDA, describes the file format system that is typically implemented on SD cards.

SanDisk SD-ROM cards do not support the SD security features (CPRM), and are therefore organized as a single non-secure partition. The content data can be accessed by the host system using standard read commands.

The following table lists the available user space for 32, 64, and 128MB cards. Note that some hosts cannot handle non-standard image sizes, so the allowable space for a particular application may be less than shown in the table.

Capacity	Maximum User LBA	Maximum User Data Image Size
32 MB	63,488	31.0MB (32505856 bytes)
64 MB	129,024	63.0MB (66060288 bytes)
128 MB	260,096	127.0MB (133169152 bytes)

3.3 Register Values

The SD specifications define a set of eight registers within the card interface. However, the DSR Register is optional and is not used in the SanDisk SD Card Product Family. For specific information about all registers, refer to Section 5 of the SDA Physical Layer Specification, Version 2.00.

Register Abbreviation	Width (in bits)	Register Name
CID	128	Card IDentification
CSD	128	Card-Specific Data
SCR	64	SD Configuration Register
RCA	16	Relative Card Address
OCR	32	Operation Condition Register
SSR	512	SD Status Register
CSR	32	Card Status Register

All card registers are also accessible in SPI Mode. Their format is identical to the format in the SD Bus Mode; however, a few fields are not used in SPI Mode. In SPI Mode, the Card Status Register has a different, shorter format as well. Refer to Section 7.4 in the SDA Physical Layer Specification, Version 2.00, for more details.

3.3.1 Card Identification Register

The Card Identification (CID) Register is 16 bytes long and contains the unique card identification number and other informational data. It is programmed during card content programming and cannot be changed by card hosts.

The following table lists the default configuration of the CID register for SanDisk SD-ROM Cards. More information can be found in Section 5.2 of the SDA Physical Layer Specification, Version 2.00.

Name	Type	Size	Value	Comments
Manufacturer ID (MID)	binary	8	0x03 (SanDisk)	Controlled and assigned by SD-3C, LLC.
OEM / Application ID (OID)	ASCII	16	0x53, 0x44 (“SD”)	Identifies the card OEM and/or the card contents. Controlled and assigned by SD-3C, LLC.
Product Name (PNM)	ASCII	40	SD032 SD064 SD128	5-character ASCII string
Product Revision (PRV)	BCD	8		2-digit revision number
Serial Number (PSN)	Binary	32		32-bit unsigned integer
Reserved		4		
Manufacture Date (MDT)	Binary	12	YYM code (offset from 2000)	ex: April 2001 = 0x014
CRC7 Checksum (CRC)		7		calculated from register contents
unused (always 0)		1		

3.3.2 Card Specific Data Register

The Card Specific Data (CSD) Register configuration information is required to access card data. The CSD defines the data format, error correction type, maximum data access time, and other parameters. The field structures of the CSD Register vary depending on the physical specifications and card capacity. The CSD_STRUCTURE field in the CSD Register indicates which structure version is used. All current SanDisk SD-ROM are standard capacity cards and so implement CSD Version 1.0 structure.

The following table provides an overview of the CSD Register. More field-specific information can be found in Table 5-4 (Section 5.3.2) of the SDA Physical Layer Specification, Version 2.00.

Field	Value	Comments
CSD_STRUCTURE	1.0	CSD structure
Reserved		Reserved
TAAC	1.5ms	Data read access time – 1
NSAC	0	Data read access time – 2 in CLK cycles (NSAC*100)
TRANS_SPEED	25MHz	Maximum data transfer rate
CCC	0x5F5	Card Command Classes
READ_BL_LEN	512 bytes	Maximum read data block length
READ_BL_PARTIAL	Yes	Partial blocks for read allowed
WRITE_BLK_MISALIGN	No	Write block misalignment
READ_BLK_MISALIGN	No	Read block misalignment
DSR_IMP	No	DSR implemented
Reserved		Reserved
C_SIZE	depends on card size	Device Size
VDD_R_CURR_MIN	100mA	Maximum read current @VDD minimum
VDD_R_CURR_MAX	80mA	Maximum read current @VDD maximum
VDD_W_CURR_MIN	100mA	Maximum write current @VDD minimum
VDD_W_CURR_MAX	80mA	Maximum write current @VDD maximum
C_SIZE_MULT	depends on card size	Device size multiplier
ERASE_BLK_EN	Yes	Erase single block enable
SECTOR_SIZE	32 blocks	Erase sector size
WP_GRP_SIZE	128 sectors	Write protect group size
WP_GRP_ENABLE	Yes	Write protect group enable
Reserved		Reserved for MMC compatibility
R2W_FACTOR	x16	Write speed factor
WRITE_BL_LEN	512 bytes	Maximum write data block length
WRITE_BL_PARTIAL	No	Partial blocks for write allowed
FILE_FORMAT_GRP	0	File format group
COPY	Has been copied	Copy flag (OTP)
PERM_WRITE_PROTECT	Not protected	Permanent write protection
TMP_WRITE_PROTECT	Not protected	Temporary write protection
FILE_FORMAT	HD w/partition	File format
Reserved		Reserved
CRC	CRC7	CRC
		Not used, always “1”

3.3.3 SD Card Configuration Register

The SD Card Configuration Register (SCR) provides information about special features in the SanDisk SD Card products. For more information, refer to Section 5.6 in the SDA Physical Layer Specification, Version 2.00.

3.3.4 Card Status Register

The Card Status Register (CSR) transmits the card's status information to the host. The CSR is defined in Section 4.10.1 in the SDA Physical Layer Specification, Version 2.00.

3.3.5 SD Status Register

The SD Status Register (SSR) contains status bits that are related to the SD Card proprietary features and may be used for future applications. The SD Status structure is described in Section 4.10.2 in the SDA Physical Layer Specification, Version 2.00.

3.3.6 Relative Card Address Register

The 16-bit Relative Card Address (RCA) Register carries the card address published by the card during the card identification process. Refer to Section 5.4 in the SDA Physical Layer Specification, Version 2.00 for more information.

3.3.7 Operation Conditions Register

The Operation Conditions Register (OCR) stores a card's VDD voltage profile. Refer to Section 5.1 of the SDA Physical Layer Specification, Version 2.00 for more information.

3.4 Bus Topology

The family of SanDisk SD products supports two communication protocols: SD and SPI. For more details, refer to Section 3.5 of the SDA Physical Layer Specification, Version 2.00. Section 6 of the specification contains a bus circuitry diagram for reference.

NOTE: SD Card pin assignments are provided by the SDA Physical Layer Specification, Version 2.00; refer to Section 8.2.

#	SD Bus Mode Pin Assignment			SPI Bus Mode Pin Assignment		
	Function	**I/O Type**	**Description**	**Function**	**I/O Type**	**Description**
1	CD/DAT3[1,2]	push-pull	Card Detect / Data [bit 3]	CS[1]	input	Chip Select (active low)
2	CMD	push-pull	Command / Response	DataIn	input	Host-to-Card commands and data
3	VSS1	supply	Supply Ground	VSS1	supply	Supply Ground
4	VDD	supply	Supply Voltage	VDD	supply	Supply Voltage
5	CLK	input	Clock	SCLK	input	Clock
6	VSS2	supply	Supply Ground	VSS2	supply	Supply Ground
7	DAT0	push-pull	Data [bit 0]	DataOut	output	Card-to-Host Data and Status
8	DAT1[2]	push-pull	Data [bit 1]	RSV		Reserved
9	DAT2[2]	push-pull	Data [bit 2]	RSV		Reserved

Notes:

1. At power up this line has a 50KOhm pullup enabled in the card. This resistor serves two functions: Card Detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with the SET_CLR_CARD_DETECT (ACMD42) command.
2. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after the SET_BUS_WIDTH command. It is the responsibility of the host designer to

connect external pullup resistors to all data lines even if only DAT0 is to be used. Otherwise, non-expected high current consumption may occur due to the floating inputs of DAT1 and DAT2 (in case they are not used).

For more details regarding the SD Bus topology, refer to Section 3.5.1 of the SDA Physical Layer Specification, Version 2.00.

For more details regarding the SPI Bus topology, refer to Section 3.5.2 of the SDA Physical Layer Specification, Version 2.00.

3.5 Electrical Interface

The power scheme of SanDisk SD products is handled locally in each card and in the bus master. Refer to Section 6.4 of the SDA Physical Layer Specification, Version 2.00.

3.5.1 Power Up

Refer to Section 6.4.1 of the SDA Physical Layer Specification, Version 2.00, for information about power sequencing.

3.5.2 Bus Operating Conditions

SPI Mode bus operating conditions are identical to SD Card Bus Mode operating conditions. For details, see Section 6.6 of the SDA Physical Layer Specification, Version 2.00.

3.5.3 Bus Timing

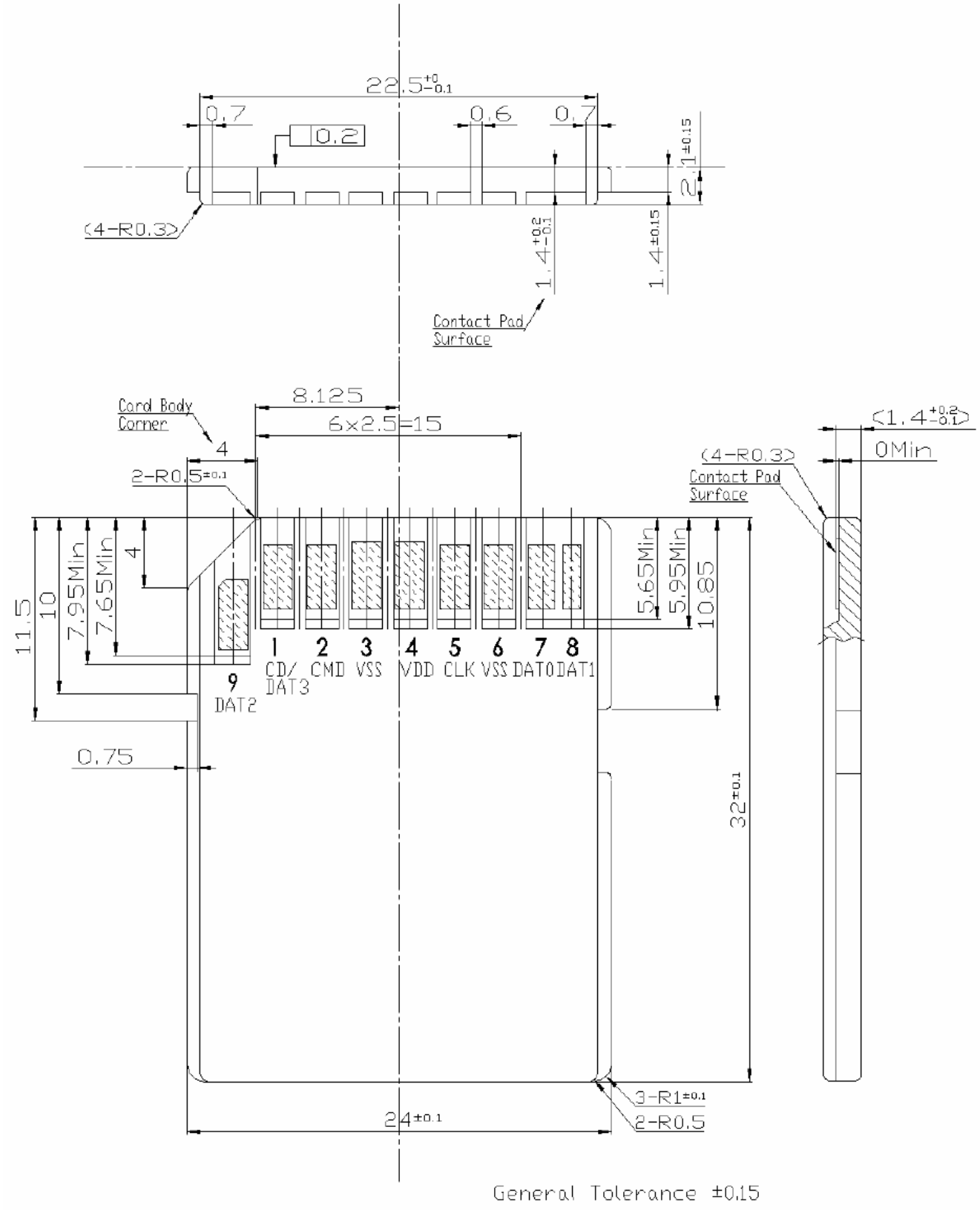
SanDisk SD-ROM cards operate at a maximum clock frequency of 25MHz. See Section 6.7 of the SDA Physical Layer Specification, Version 2.00, for bus timing specifications.

3.6 Physical / Mechanical

The following table specifies the physical attributes of the SanDisk SD Card.

Parameter	Value	Notes
Weight	2.0g maximum	
Length	32mm +/- 0.1mm	
Width	24mm +/- 0.1mm	
Thickness	2.1mm +/- 0.15mm	

SanDisk SD-ROM Cards are available in an SD card compatible form factor without a physical (sliding) write-protect switch. As shown in the following package diagram, the SD-ROM Card package has the write-protect "notch" in the write-enabled position, even though the card itself is read-only.


22.5+0 −0.1
0.7
0.6
0.7
0.2
2.1±0.15
(4-R0.3)
1.4+0.2 −0.1
1.4±0.15
Contact Pad Surface
8.125
6×2.5=15
Card Body Corner
4
2-R0.5±0.1
(1.4+0.2 −0.1)
0Min
(4-R0.3)
Contact Pad Surface
11.5
10
7.95Min
7.65Min
4
5.65Min
5.95Min
10.85
1 2 3 4 5 6 7 8
CD/ DAT3
CMD
VSS
VDD
CLK
VSS
DAT0
DAT1
9
DAT2
0.75
32±0.1
3-R1±0.1
2-R0.5
24±0.1
General Tolerance ±0.15