Pico Computing

Pico E-15

Hardware Technical Reference

Release: 1.01
For Hardware Revision: D

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Contents:

Product Overview:

The Pico family of products are revolutionary FPGA based embedded acceleration platforms. With performance that often exceeds modern microcomputers, a shockingly small form factor, and nominal power consumption that is less than one watt, the Pico family of products take computing to a whole new level.

The Pico E-15 is based on the high-performance Virtex-4 FPGA chip. This device has the performance and power consumption of a custom chip (ASIC), but is completely reconfigurable! The E-15 features four high speed converters and direct video capture.

Advanced users will enjoy the open source development kits which allow absolute control over the hardware. For those who desire a more high level approach to firmware, Viva provides a graphical development model. Impulse C™ support is also included for rapid firmware development in the C programming language. Board support packages are available for operating systems such as Linux, µC/OS, Green Hills Integrity OS™ and VX Works.

Pico E-15 Quick Reference Datasheet

FEATURES

- High-performance Virtex-4 FX-20, 40 or 60
- 256MB RAM
- 64MB Flash ROM
- Dual 12-Bit 125 MSPS A/D converters
- Dual 14-Bit 210 MSPS D/A converters
- Integrated composite video capture
- CardBus (PCI) Interface
- Open source
- Standalone operation
- Reconfigurable, high-speed digital bus

MECHANICAL

Temperature Range: 0°C to +70°C
PC Card Type II Form-Factor
Stainless steel case

POWER

Sleep: 0.001W
Nominal: 1.2W
Absolute Maximum: 7.0W
Supply Voltage: 3.3V

FPGA FEATURES

- Embedded PowerPC™ P405 processor
- Integrated DSP logic
- Integrated RAM

APPLICATIONS

- Software defined radio
- Video processing / compression
- Accelerated scientific computing
- Digital signal processing
- Impulse C™ development platform
- Viva development platform
- Embedded systems
- Encryption / decryption
- Supercomputing / cluster computing

IO Connectivity

- 10/100/1000 Ethernet
- RS-232 Asynchronous Serial
- JTAG
- SVIDEO/Composite In
- Dual High Speed Analog to Digital
- Dual High Speed Digital to Analog
- GPIO

*Operation below -0°C requires throttled RAM timing

Standard Part Numbers

	Standard Part Number
FX-20	E15FX20-256/64/JEGSAADDV10C
FX-40	E15FX40-256/64/JEGSAADDV10C
FX-60	E15FX60-256/64/JEGSAADDV10C

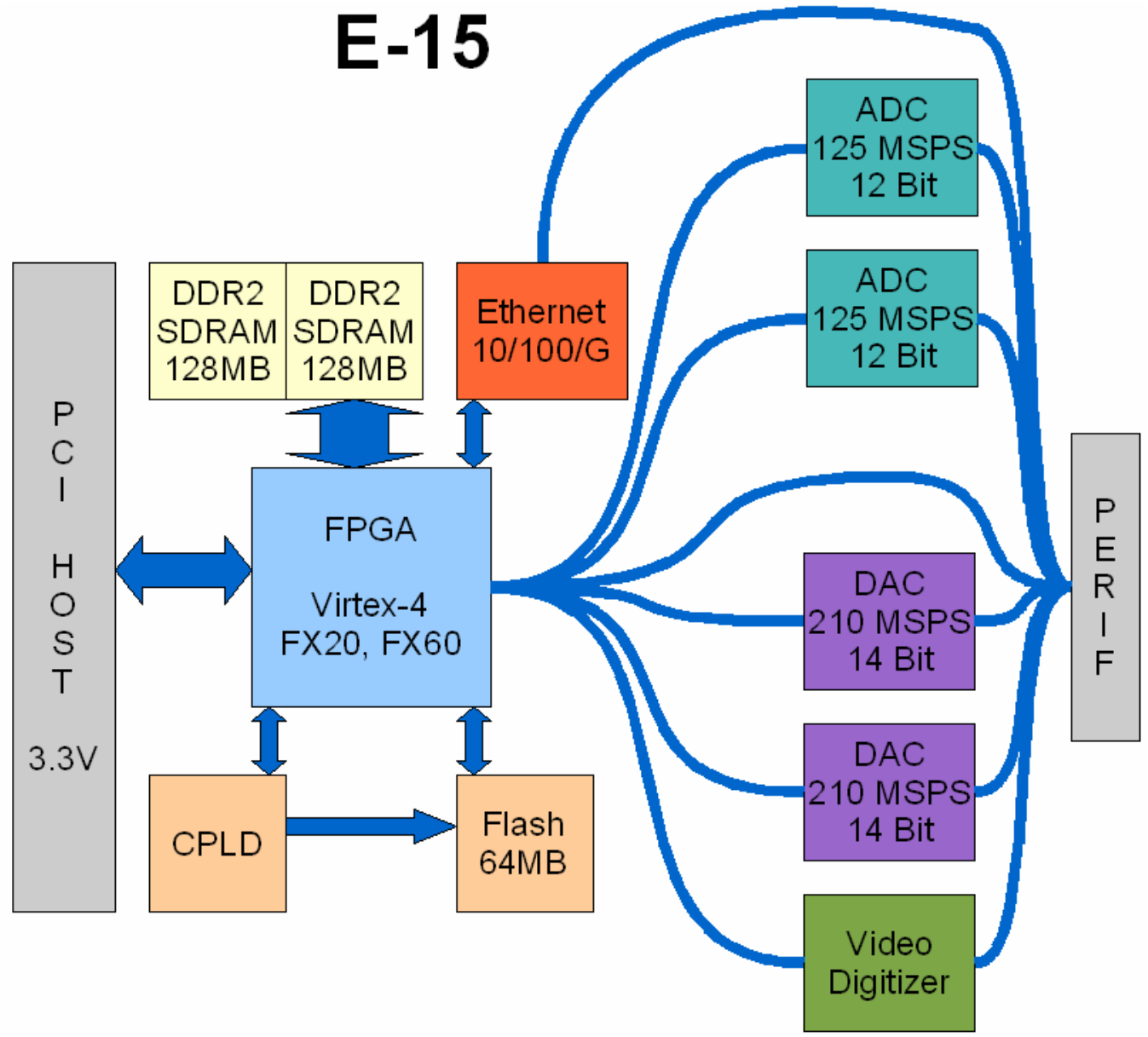
A Military version is available which includes:

- ✓ BGA underfill
- ✓ Conformal coating
- ✓ Extended temperature range

The Military version is available by special order only, and is subject to minimum quantity requirements.

System Architecture

At the core of the Pico E-15 is a Virtex-4 FPGA. The FPGA can be dynamically configured to perform any number of specialized tasks such as: protocol processing, encryption, or complex mathematical functions. Embedded systems benefit from the integrated PowerPC™ processor.



Pico E-15 Electrical Specification

	Minimum	Nominal	Maximum
DC Input Voltage	3.25V	3.3V	3.35V
Power Consumption	0.001W	1.2W	7.0W
DC Input Current	0.0003A	0.36A	2.1A
Recommended Temperature Range	0°C	10°C	70°C
FPGA Over Temperature Shutdown		70-80°C	
Maximum Storage Temperature Range	-50°C	27°C	90°C
Relative Humidity (Non-Condensing)	0%		95%

Overpower Considerations:

The Pico E-15 FX60 is designed desktop computers, and is not recommended for use in laptops. Because of the large gate count of the FX60, it can easily exceed the PCCARD maximum current consumption specification of 1A. The FX-60 features built in over-temperature shutdown to protect both the card and the host system.

The Pico E-15 FX60 should be used with an external heat sink and an extender card.

Field Programmable Gate Array

The core of the Pico E-15 is a high performance Virtex-4 FPGA. Included in the FPGA are the FPGA Fabric, an optional PowerPC ™ processor, ultra high-speed DSP slices and RAM.

FPGA Fabric:

The “Fabric” of an FPGA comprises an array of logic elements that can be connected in virtually unlimited patterns. These patterns of logic elements can be used to perform basic mathematical functions such as addition and subtraction, or can be grouped together to perform complex functions like Fast Fourier Transforms. Logic elements can even be connected to create a custom soft processor.

The advantage of the FPGA is that the internal logic can be optimized for a specific application. FPGAs are also able to execute operations in parallel, not being limited by sequential execution like a traditional processor. FPGA operations can be executed in a parallel, pipelined or even an asynchronous manner. The FPGA allows incredible application speed with very low power consumption. Your imagination is really the limit.

DSP Slice:

Embedded within the FPGA are special areas that are designed to facilitate high speed “digital signal processing.” These areas are called DSP slices. The DSP slice can be configured in a variety of different ways. For example, one DSP slice can be configured to be one tap of an FIR filter. DSP slices are fully pipelined and feature incredible speed. When configured for FIR filtering the DSP slice has a guaranteed performance of 500MHz with a latency of one cycle. An 18x18 multiply and accumulate also runs at 250MHz with a latency of two cycles. Smaller data widths allow higher clock speeds.

FPGA Resources:

Free FPGA Cores	http://www.opencores.org	repository of free, open source IP cores OPENCORES.ORG
Encryption Cores	http://www.openciphers.org	
Virtex-4 Website	http://www.xilinx.com/virtex4	

PowerPC™ Processor

PPC405x3 Processor Introduction:

FPGAs are renowned for their ability to process parallel logic, but they typically have a hard time emulating a high performance processor. To get the best of both worlds the Virtex-4™ features an embedded Power PC Processor. Since the processor shares the same die as the FPGA it seamlessly interfaces with the FPGA fabric.

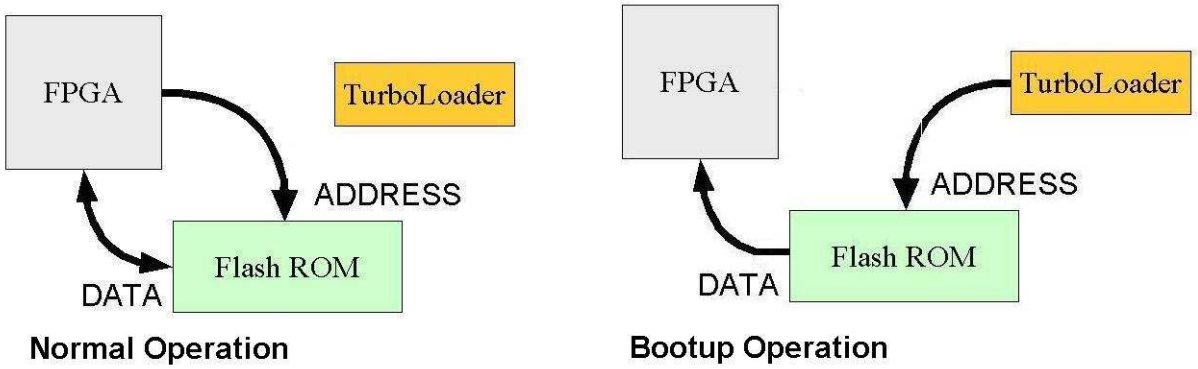
A new feature of the Virtex-4 FPGA is the addition of an auxiliary processor interface. The APU is the highest speed interface between the PowerPC™ processor and the FPGA fabric. Up to four custom instructions may be implemented in the FPGA, which are accessible from the PowerPC™.

Board support packages are currently available for µC/OS and Linux. Board support source code is available open source under the GPL.

CPLD TurboLoader

A CPLD (Complex Programmable Logic Device) is a smaller version of an FPGA (described above) with permanent Flash storage built in. The Pico E-15 contains one CPLD that loads and reconfigures the FPGA. The Pico firmware guide describes how to access the CPLD TurboLoader.

The Flash ROM's address bus can be controlled by either the TurboLoader or the FPGA (but not both). During power-up or reboot, the TurboLoader is in control of the Flash ROM Address bus. At all other times the FPGA is in control of the address bus.



CPLD Resources:

Xilinx CPLD Website	http://www.xilinx.com/cpld

Flash Memory

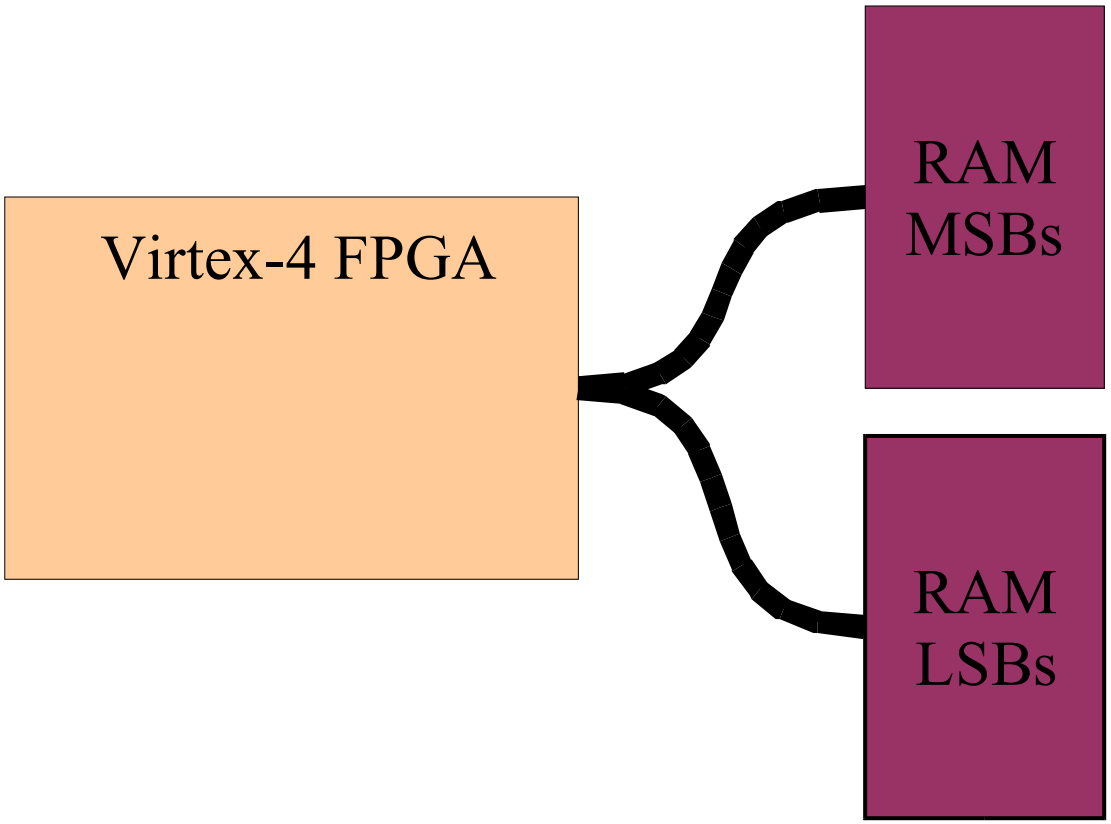
The Pico E-15 comes equipped with at least 64MB of Flash ROM. The Flash ROM is divided into 512 sectors that can be erased independently. Most of the space on the ROM is reserved for the user.

The Flash ROM's address bus can be controlled by either the TurboLoader or the FPGA (but not both). During power-up or reboot, the TurboLoader is in control of the Flash ROM Address bus. At all other times the FPGA is in control of the address bus.

The Flash ROM has a simple, open file system which allows the user to store FPGA images, ELF binary files, or other data. The primary image is used to boot the FPGA initially, and the backup image is only invoked if the primary image fails to load correctly. Executable files are in ELF format and are loaded by a loader within the secondary image. The primary image will either load the secondary image or pause for the PC to access and manage the file system.

DDR2 SDRAM Memory

The Pico E-15 comes equipped with 256MB of DDR2 SDRAM memory. There are two 1024Mb chips, each with a separate 16 bit data path to the host to form one 32 bit bank. From 0°C to +85°C, the ram can run at up to 333 MHz. For operation at temperatures below 0°C, special firmware with throttled ram timings is required. Please note that the RAM will not function below 125 MHz.



RAM Timing and Parameter Information

Parameter	Value	EDK Value 133 MHz	EDK Value 333 MHz
Registered	No	0	0
Clock Pairs	1	1	1
Memory Banks	1	1	1
IDELAY Controllers	2	2	2
Differential DQs	Yes	1	1
Open Row Management	No	0	0
On Die Termination	Disabled	0	0
ECC Support	No	0	0
TMRD	2 Clocks	15000	6000
TWR	15 nS	15000	1500
TWTR	7.5 nS	1	3
TRAS	45 nS	45000	45000
TRC	60 nS	60000	60000
TRFC	127.5 nS	12750	12750
TRCD	15 nS	15000	15000
TRRD	10 nS	10000	10000
TRP	15 nS	15000	15000
TREFI	7.8 uS	7800000	7800000
TFAW	37.5	37500	37500
CAS Latency	5 Clocks	5	5
Data Width	32 Bits	32	32
Address Width	13 Bits	13	13
Column Width	10 Bits	10	10
Bank Address Width	3	3	3
Clock Period*	5 nS	7500	3000

*Minimum RAM Speed is 125MHz

Temperature Sensor

The Pico E-15 contains one temperature sensor that directly senses the die temperature of the Virex-4 FPGA. The digital interface of the remote temperature sensing chip is connected to the Cypress PSoC. If an overtemperature condition occurs, the PSoC will shutdown the FPGA until the temperature has dropped sufficiently below the shutdown threshold.

The setpoints of the temperature shutdown circuit can be reprogrammed via the PSoC debug cable.

Electrical Specifications	Minimum	Nominal	Maximum
Temperature Sensing Range	-55°C		125°C
Resolution		0.0625°C	
Accuracy	+/- 2.4°C	+/- 1.0°C	+/- 0.0°C

Sleep Controller

The Pico E-15 contains one Cypress PSoC which is used to generate a clock for the bootloader and control the power state.

The E-15 can be placed in a state where it draws almost no power, then wakes up automatically after a set amount of time.

The sleep controller can be activated by the FPGA, or the external peripheral interface connector.

The protocol for entering sleep state is simple. Simply pulse FPGA_POWERCTL_C for as many seconds as your wish to sleep, then lower the FPGA_POWERCTL_D signal.

The Pico E-15 will awake from sleep if any of the following conditions are true:

-Power is first applied
-The sleep timer has run out
-POWERCTL_D is low and POWERCTL_C is high

The Pico E-15 will enter sleep mode if any of the following conditions are true:

-An overtemperature condition is detected
-The FPGA_POWERCTL_D pin is low
-The POWERCTL_C pin is low

Tri-Mode Ethernet Interface

The Pico E-15 features the Marvell Alaska series 88E1111 tri-mode Ethernet transceiver. Combined with the on-FPGA MAC (Middle access controller) a complete Ethernet solution is offered. Communication between the MAC and PHY takes place over an industry standard MII/GMII interface.

The Ethernet transceiver features 10/100/1000 full/half duplex operation. It will automatically configure the physical interface on the fly for crossover or straight through operation. The PHY can even automatically correct for common wiring mistakes. The PHY has a built in Time Domain Reflectometer which can diagnose cable problems and pinpoint their distance away from the transceiver.

The Ethernet interface on the Pico is magnetic-less allowing high speed, low power digital interconnect directly to Ethernet backplanes. DO NOT directly connect the Ethernet interface to a hub or switch without a magnetic isolation module.

The Marvell 88E1111 is the only user-accessible chip on the Pico E-15 that requires an NDA for access to the datasheets. If you are interested in some of the advanced features not supported by the native driver, contact Pico Computing for assistance in obtaining an NDA from Marvell. Users are advised not to contact Marvell directly.

Ethernet Resources:

Marvell 88E1111 Webpage	http://www.marvell.com/products/transceivers/singleport/88e1111.jsp

Digital Peripheral Interface

The Pico E-15 features 2 GPIO lines which are used for external peripheral support. The GPIO lines are always enabled.

All GPIO signals have user selectable pull-up, pull-down, keeper or HI-Z termination. Drive strength is also user selectable between 2 and 24mA. All GPIOs can be configured for input, output and bi-directional mode.

GPIO 1 has a 50 ohm resistor in series with the output to allow connectivity with low voltage devices which may clamp a 3.3V signal.

Electrical Specifications	Minimum	Nominal	Maximum
High Voltage	2.0V	3.3V	3.45V
Low Voltage	-0.2V	0V	0.8
Input Impedance (Pulldowns Disabled)		HI-Z	
Drive Strength (Selectable)	2 mA		24 mA
ESD Withstand Voltage (Human Body Model)			2 KV

High Speed Analog to Digital Converters

The Pico E-15 features 2 high speed analog to digital converters. The converters are optimized for high-frequency, high-performance, low-power, low-noise operation. The converters have integrated DC blocking capacitors, and thus, cannot be used on very low frequency signals. The ADC should be driven by a source with an impedance of 50 ohms.

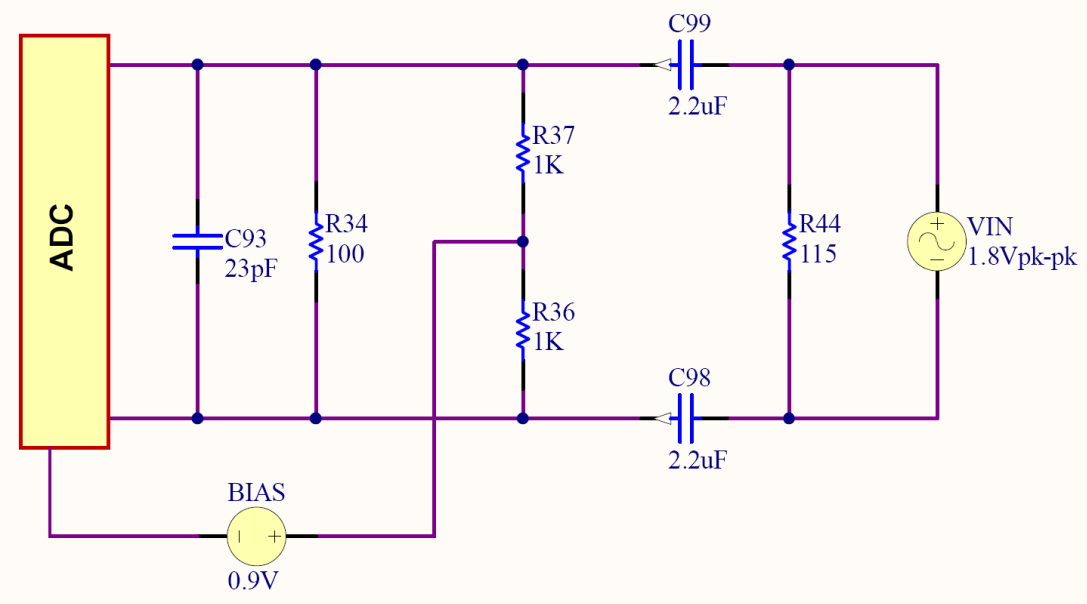
To ensure accuracy at high speeds, the low-jitter 125 MHz reference clock must be used. The converters may be tuned to different applications. For example: a lower termination impedance may be traded for more sensitivity. A wider high frequency input range may be traded for less high frequency noise rejection. Contact Pico Computing with your application requirements.

The data returning from the ADCs must be sampled on the rising edge of the appropriate clock return pin. Even when the ADCs are clocked from the same source, they will be running out of sync because of the duty cycle stabilizer (which provides greater resolution). The Pico E-15 can be special ordered with the duty cycle stabilizer perminately disabled.

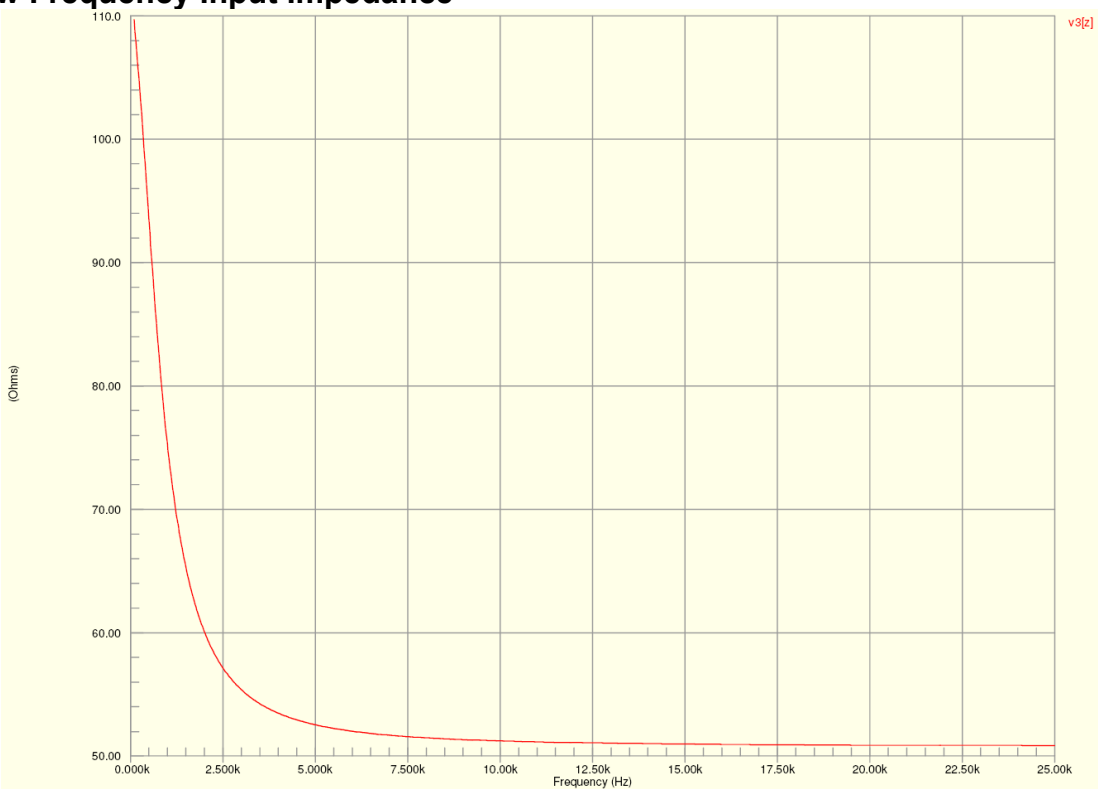
Electrical Specifications	Minimum	Nominal	Maximum
Differential AC Input Voltage	0 Vpp	1 Vpp	1.8 Vpp
Termination Resistance	45 (VHF)	50 (AC)	115(DC)
Input Frequency Range	1 KHz*	1-50 MHz	125 MHz
Bandwidth		125 MHz	225 MHz
Dielectric Surge Withstand Voltage	-14 VDC	0 VDC	14 VDC
Withstand Voltage	-4 VDC	0 VDC	4 VDC
Clock Frequency		125 MHz	125 MHz
Resolution			12 Bits
Sensativity	0.087V	0.013V	0.007V

*Lower frequencies are possible with degraded performance.

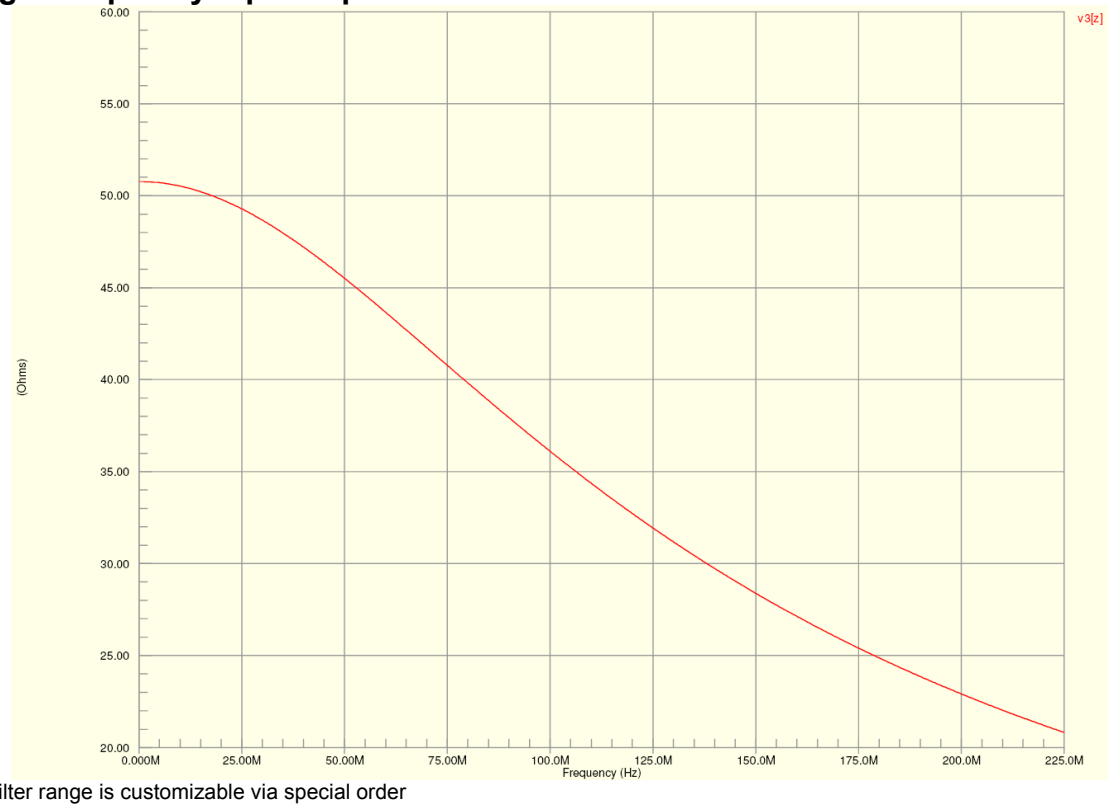
ADC Front-End Equivalent Circuit



ADC Low Frequency Input Impedance



ADC High Frequency Input Impedance*



*Low pass filter range is customizable via special order

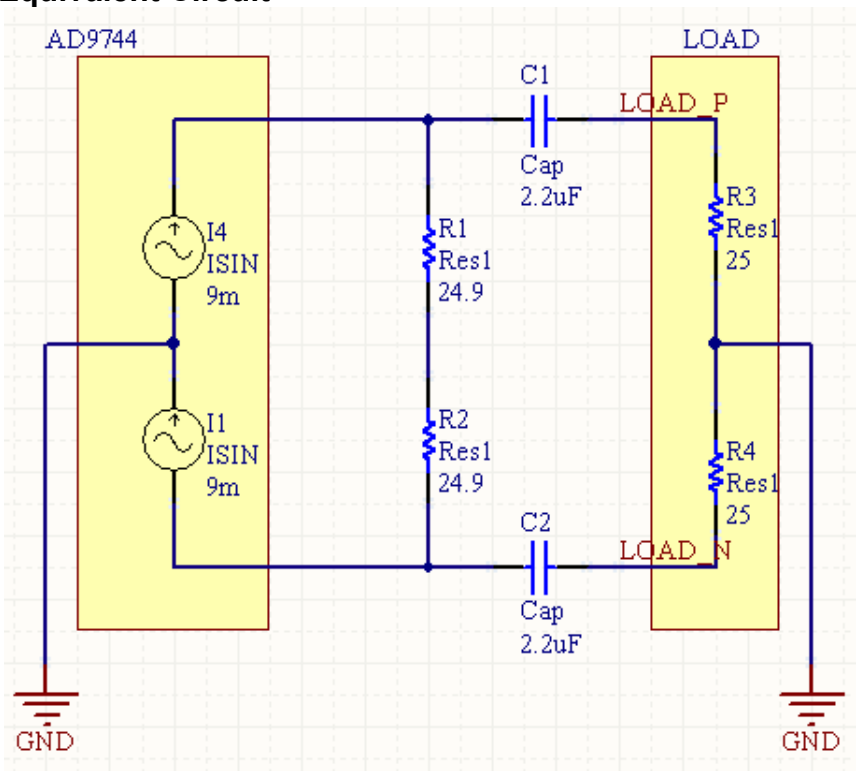
High Speed Digital to Analog Converters

The Pico E-15 features 2 high speed analog to digital converters. The converters are optimized for high-frequency, high-performance, low-power, low-noise operation. The converters have integrated DC blocking capacitors, and can not be used on low frequency signals. The DAC should be terminated into a 50 ohm load.

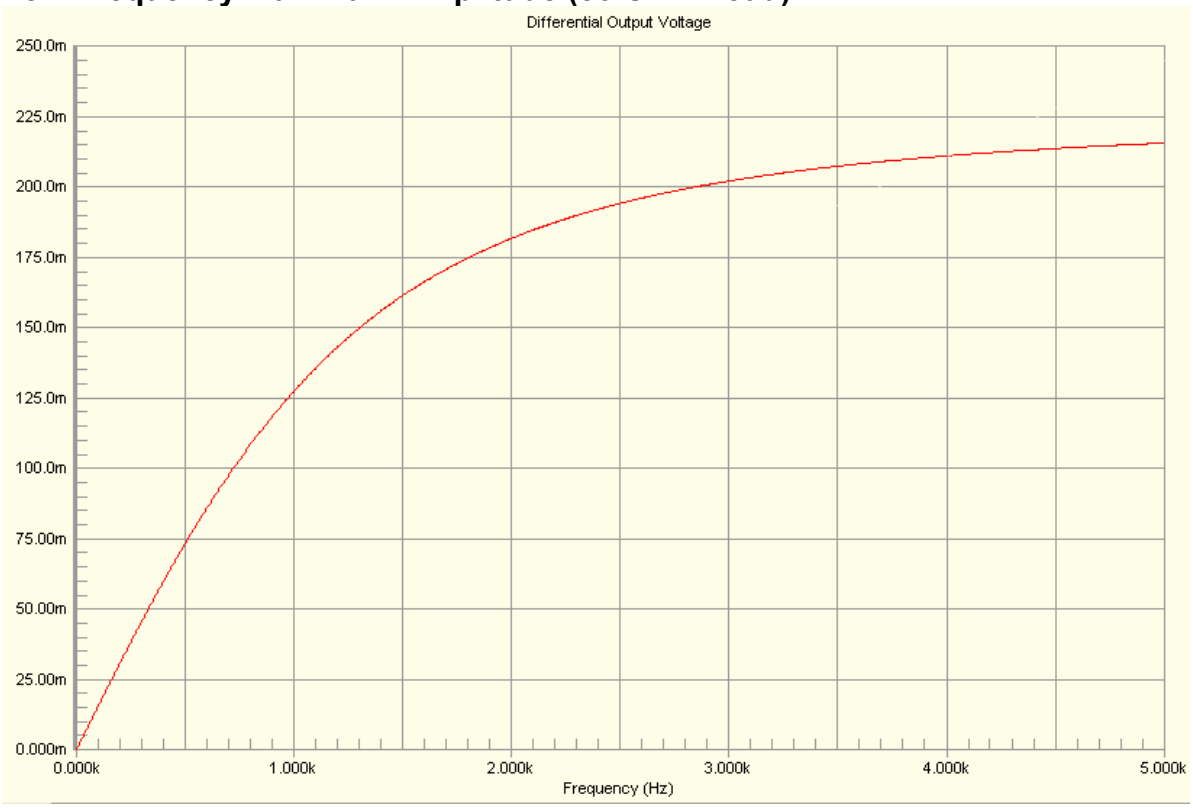
To ensure accuracy at high speeds, the low-jitter 125 MHz reference clock must be used. The DAC supports a clock frequency of up to 210 MHz.

Electrical Specifications	Minimum	Nominal	Maximum
Differential AC Output Voltage (50 Ohm Load)	0 Vpp	0.225 Vpp	0.45 Vpp
Differential AC Output Voltage (Hi-Z)	0 Vpp	1.8 Vpp	1.8 Vpp
Internal Termination Impedance		50	
Output Frequency Range (50 Ohm Load)	5 KHz		105 MHz
Bandwidth			
Noise Floor			
Dielectric Withstand Voltage (Output to GND)	-15V	0V	15V
Clock Frequency		125 MHz	210 MHz
Resolution		14 Bits	

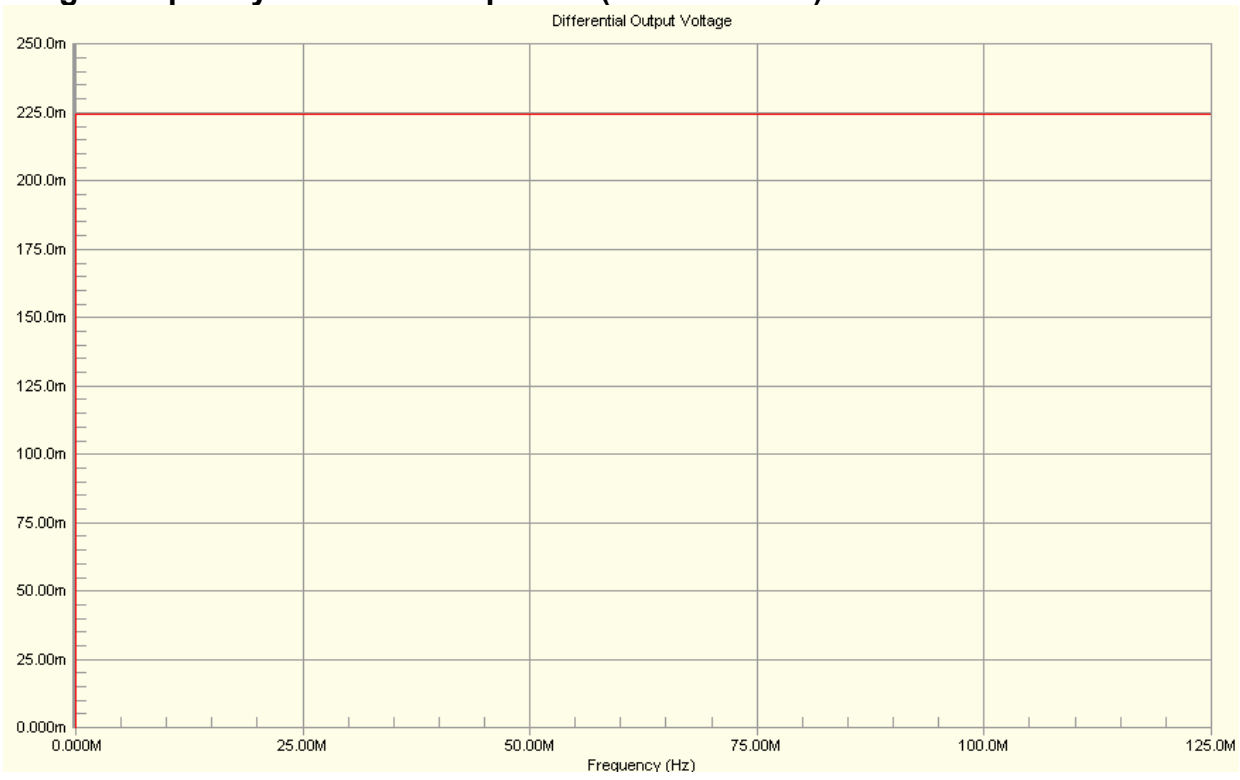
DAC Front-End Equivalent Circuit



DAC Low Frequency Maximum Amplitude (50 Ohm Load)



DAC High Frequency Maximum Amplitude (50 Ohm Load)



Video Digitizer

The Pico E-15 contains one ultra low-power video digitizer. The video digitizer accepts both SVIDEO and Composite video inputs and can decode NTSC, PAL and SECAM video standards. When using composite video, the video digitzer can switch from between two channels. The TVP5150 has an integrated I2C control interface.

Video Digitizer External Connections (SVIDEO Mode):

VIDEO_IN_Y	Video Luminence
VIDEO_IN_C	Video Chrominence
VIDEO_IN_GND	Analog Video Ground

Video Digitizer External Connections (COMPOSITE Mode):

VIDEO_IN_Y	Composite Video Channel #1*
VIDEO_IN_C	Composite Video Channel #2*
VIDEO_IN_GND	Analog Video Ground

*Unused channels must be connected to Analog Video Ground

Electrical Specifications	Minimum	Nominal	Maximum
Resolution		9 Bits	
Impedance		75 Ohms	
Maximum AC Amplitude			1.5 Vp
Maximum DC Offset	-75V	0	75V

Video Digitizer Resources:

TVP5150AM1 Homepage	http://focus.ti.com/docs/prod/folders/print/tvp5150am1.html

CardBus / Digital Bus Interface

The Pico E-15 can run as a standalone product or be connected to a host using the CardBus connector. By default, the Pico E-15 ships with firmware that is ready for use as a CardBus device.

The CardBus interface is a subset of PCI. The data path is 32 bits wide and is synchronous. The wiring of the CardBus interface supports both completion and mastering of the bus.

When the Pico E-15 is not connected to a CardBus host, the digital bus can be reconfigured to connect with a wide variety of high speed digital busses and peripherals. With proper external termination, speeds of over 100 MHz are possible. The external digital bus can only interface with 3.3V logic.

Those who are interested in alternate interfaces should contact Pico Computing. The CardBus interface source code and support is available.

Electrical Specifications (DC)	Minimum	Nominal	Maximum
Positive Supply Input Voltage (Vcc)	3.25V	3.3V	3.35V
Low Level Input Voltage	-0.2V	0V	0.7V
High Level Input Voltage	2.0V	3.3V	3.35V
Recommended Drive Strength		8mA	
Input Impedance		HI-Z	
Internal Bus Voltage		3.3V	

PCMCIA Interface Resources:

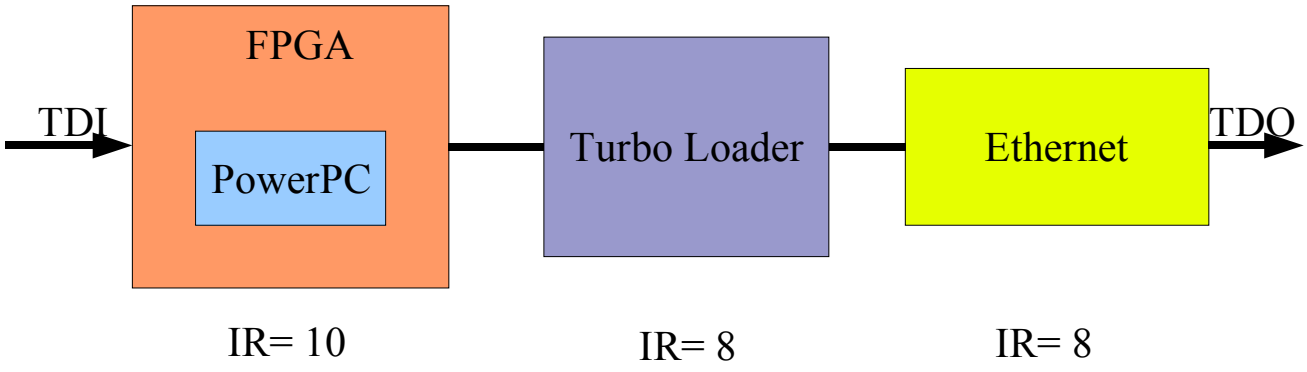
PCMCIA Website	www.pcmcia.org
PCI SIG Website	www.pci.org

JTAG Debug Interface

The Pico E-15 is equipped with a JTAG diagnostic port which allows real-time debugging of hardware, firmware and software.

Some JTAG programs require the length of the instruction register (IR). The IR length is listed below for all devices in the JTAG chain. The FPGA IR length changes depending on how many PowerPCs are internally connected to the JTAG chain in the FPGA.

Device	Instruction register bit length
FPGA	6,10 or 14 (Depends on PPC Configuration)
TurboLoader	8
Ethernet PHY	8



The Primary Image in the Flash ROM contains an embedded JTAG diagnostic port. This allows a user in Windows or Linux to debug software without an external JTAG cable. The internal JTAG diagnostic loopback looks just like a Parallel Port JTAG diagnostic cable when used with the Pico E-15 driver.

The external JTAG interface uses 1.8V logic.

PSoC Debug Interface

The Pico E-15 has a low power PSoC microcontroller (also known as the sleep controller) which controls the power to the rest of the board. The PSoC also generates a 24 MHz clock for the TurboLoader. The PSoC features an in-circuit programming interface, although it is unlinkey that a user will ever need to debug or modify the PSoC firmware.

To program the PSoC the following parts are required:

Description	Manufacturer	Part Number	Distributor
ISSP Programming Cable	Pico Computing	E15-PSoC	Pico Computing
PSoC ICE CUBE	Cypress	CY3215-DK	Digikey

Appendix A – Peripheral I/O Connector Information

Connector Information

Description	Brand	Part Number
Mating Connector	Hirose	NX-32TA-CV1(50)

*Connectors are always in stock at Pico Computing

Peripheral I/O Connector Pinout

1	VIDEO_GND	Analog Video Ground	0V DC – Ground [VIDEO]
2	VIDEO_IN_C	Analog Video Input (Chrominance)	NTSC / CAM / PAL Video
3	VIDEO_IN_Y	Analog Video Input (Luminance)	NTSC / CAM / PAL Video
4	TMS	JTAG Mode Select	LVCMOS-1.8
5	TCK	JTAG Clock	LVCMOS-1.8
6	TDI	JTAG Data In	LVCMOS-1.8
7	TDO	JTAG Data Out	LVCMOS-1.8
8	ANALOG_IN_1+	Differential Analog In #1 +	1.8V Pk-Pk 50 Ohm Analog
9	ANALOG_IN_1-	Differential Analog In #1 -	1.8V Pk-Pk 50 Ohm Analog
10	ETHER_OUT_DA-	Ethernet DA-	IEEE 802.3
11	ETHER_OUT_DA+	Ethernet DA+	IEEE 802.3
12	ETHER_OUT_DD-	Ethernet DD-	IEEE 802.3
13	ETHER_OUT_DD+	Ethernet DD+	IEEE 802.3
14	ETHER_OUT_DC-	Ethernet DC-	IEEE 802.3
15	ETHER_OUT_DC+	Ethernet DC+	IEEE 802.3
16	ETHER_OUT_DB-	Ethernet DB-	IEEE 802.3
17	ETHER_OUT_DB+	Ethernet DB+	IEEE 802.3
18	POWERCTL_R	PSoC Debug Interface Reset	LVTTL-3.3
19	ANALOG_IN_2-	Differential Analog In #2 -	1.8V Pk-Pk 50 Ohm Analog
20	ANALOG_IN_2+	Differential Analog In #2 +	1.8V Pk-Pk 50 Ohm Analog
21	2.5V	2.5V 250mA Max	2.5V DC
22	DIAG_EN_n	Diagnostic Enable	LVCMOS-1.8
23	1.8V	1.8V 250mA Max	1.8V DC
24	POWERCTL_C	PSoC Debug Clock	LVTTL-3.3
25	POWERCTL_D	PSoC Debug Data / WAKEUP	LVTTL-3.3
26	GPIO_1	General Purpose IO #1	LVTTL-3.3
27	GPIO_2	General Putpose IO #2	LVTTL-3.3
28	GND	Digital Ground	0V DC – Ground [DIGITAL]
29	ANALOG_OUT_2+	Differential Analog Out #2 +	1.8V Pk-Pk 50 Ohm Analog
30	ANALOG_OUT_2-	Differential Analog Out #2 -	1.8V Pk-Pk 50 Ohm Analog
31	ANALOG_OUT_1+	Differential Analog Out #1 +	1.8V Pk-Pk 50 Ohm Analog
32	ANALOG_OUT_1-	Differential Analog Out #1 -	1.8V Pk-Pk 50 Ohm Analog

Peripheral Connector Drawing

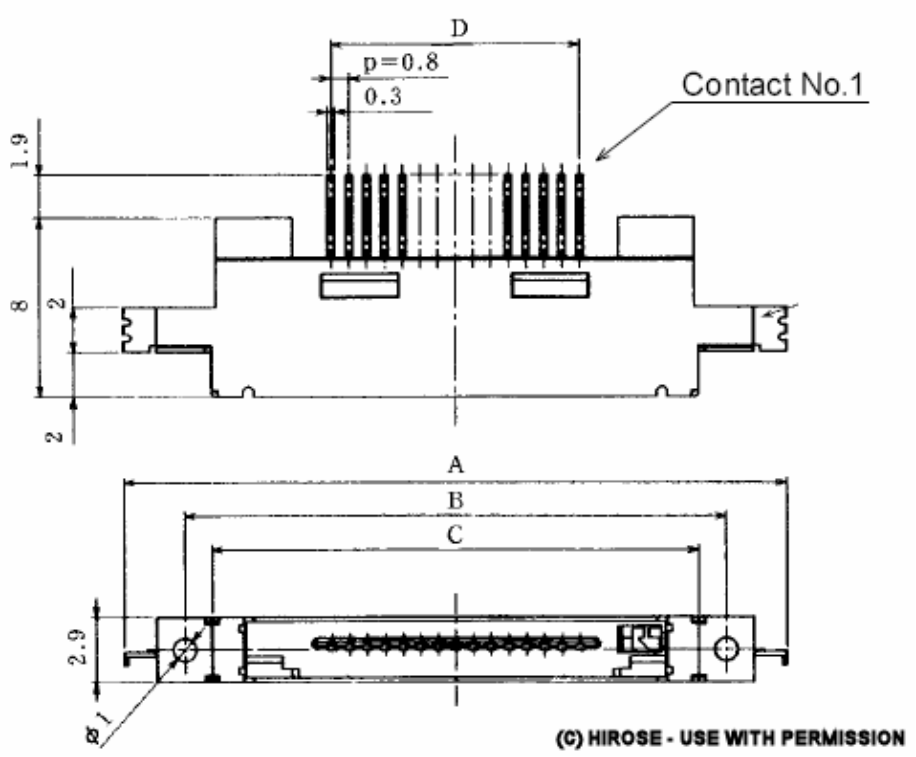


Figure 5

Appendix B – CardBus Connector Information

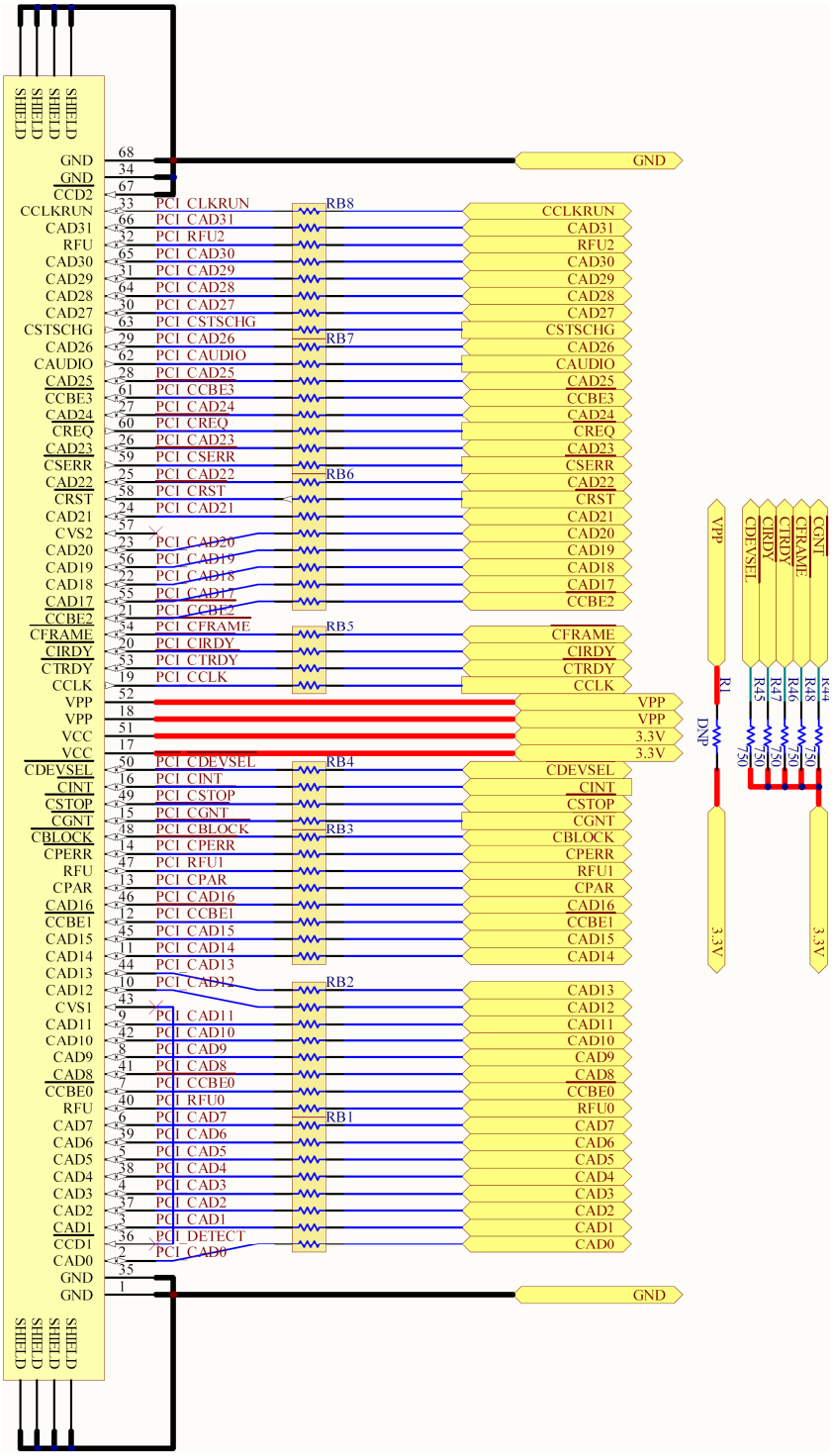
Connector Information

Description	Brand	Part Number
CardBus Socket	FCI	71299-050CALF

The CardBus Socket is typically in stock at Mouser Electronics. (http://www.mouser.com)

The function and direction of the pins on the CardBus interface can be easily changed to suit the needs of a custom interface. Series termination on the E-15 is zero ohms, but a larger value can be used if it is required for your application.

CardBus Interface Schematic



CardBus Connector Pinout

1	GND	Digital Ground
2	PCI_CAD0	Data / Address 0
3	PCI_CAD1	Data / Address 1
4	PCI_CAD3	Data / Address 3
5	PCI_CAD5	Data / Address 5
6	PCI_CAD7	Data / Address 7
7	P\C\I_\C\C\B\E\0\	Byte Enable 0
8	PCI_CAD9	Data / Address 9
9	PCI_CAD11	Data / Address 11
10	PCI_CAD12	Data / Address 12
11	PCI_CAD14	Data / Address 14
12	P\C\I_\C\C\B\E\1\	Byte Enable 1
13	PCI_CPAR	Parity Even
14	P\C\I_\C\P\E\R\R\	Parity Error
15	P\C\I_\C\G\N\T\	Access Grant
16	P\C\I_\C\I\N\T\	Interrupt Request
17	3.3V	3.3V Digital Supply
18	VPP	No Connection
19	PCI_CCLK	33 MHz
20	P\C\I_\C\I\R\D\Y\	Initiator Ready
21	P\C\I_\C\C\B\E\2\	Byte Enable 2
22	PCI_CAD18	Data / Address 18
23	PCI_CAD20	Data / Address 20
24	PCI_CAD21	Data / Address 21
25	PCI_CAD22	Data / Address 22
26	PCI_CAD23	Data / Address 23
27	PCI_CAD24	Data / Address 24
28	PCI_CAD25	Data / Address 25
29	PCI_CAD26	Data / Address 26
30	PCI_CAD27	Data / Address 27
31	PCI_CAD29	Data / Address 29
32	PCI_RFU2	Reserved
33	PCI_CLKRUN	Clock Request
34	GND	Digital Ground
35	GND	Digital Ground
36	PCI_DETECT	CardBus Detect Shorted to 46
37	PCI_CAD2	Data / Address 2
38	PCI_CAD4	Data / Address 4
39	PCI_CAD6	Data / Address 6
40	PCI_RFU0	Reserved
41	PCI_CAD8	Data / Address 8
42	PCI_CAD10	Data / Address 10
43	PCI_DETECT	CardBus Detect Shorted to 36
44	PCI_CAD13	Data / Address 13
45	PCI_CAD15	Data / Address 15
46	PCI_CAD16	Data / Address 16
47	PCI_RFU1	Reserved
48	P\C\I_\C\B\L\O\C\K\	Bus Lock

49	P\C\I_\C\S\T\O\P\	Transfer Halt
50	P\C\I_C\D\E\V\S\E\L\	Device Select
51	3.3V	3.3V Digital Supply
52	VPP	No Connection
53	P\C\I_\C\T\R\D\Y\	Target Ready
54	P\C\I_\C\F\R\A\M\E\	Frame
55	PCI_CAD17	Data / Address 17
56	PCI_CAD19	Data / Address 19
58	P\C\I_\C\R\S\T\	Reset
59	P\C\I_\C\S\E\R\R\	System Error
60	P\C\I_\C\R\E\Q\	Access Request
61	P\C\I_\C\C\B\E\3\	Byte Enable 3
62	PCI_CAUDIO	Audio
63	PCI_CSTSCHG	Status Change Interrupt
64	PCI_CAD28	Data / Address 28
65	PCI_CAD30	Data / Address 30
66	PCI_CAD31	Data / Address 31
67	GND	Digital Ground
68	GND	Digital Ground

Appendix C – FPGA Pinout

FPGA Pinout

Net	Pin	Description	Dir	I/O Standard	Term	Drive
ADC_1_CLK_IN+	K8	Differential Clock In+	O	DIFF HSTL II	Float	
ADC_1_CLK_IN-	K7	Differential Clock In-	O	DIFF HSTL II	Float	
ADC_1_CLK_RTURN	D6	Clock Return	I	LVTTL	Float	
ADC_1_D0	G7	Data In #0	I	LVTTL	Float	
ADC_1_D1	E5	Data In #1	I	LVTTL	Float	
ADC_1_D2	E7	Data In #2	I	LVTTL	Float	
ADC_1_D3	F7	Data In #3	I	LVTTL	Float	
ADC_1_D4	F8	Data In #4	I	LVTTL	Float	
ADC_1_D5	C9	Data In #5	I	LVTTL	Float	
ADC_1_D6	D9	Data In #6	I	LVTTL	Float	
ADC_1_D7	C12	Data In #7	I	LVTTL	Float	
ADC_1_D8	G9	Data In #8	I	LVTTL	Float	
ADC_1_D9	A14	Data In #9	I	LVTTL	Float	
ADC_1_D10	G10	Data In #10	I	LVTTL	Float	
ADC_1_D11	H7	Data In #11	I	LVTTL	Float	
ADC_1_OVERLOAD	H8	Over-Voltage Detect	I	LVTTL	Float	
ADC_1_POWER	L9	Power Control	I	LVTTL	Float	
ADC_2_CLK_IN+	J9	Differential Clock In+	O	DIFF HSTL II	Float	
ADC_2_CLK_IN-	K10	Differential Clock In-	O	DIFF HSTL II	Float	
ADC_2_CLK_RTURN	H4	Clock Return	I	LVTTL	Float	
ADC_2_D0	B14	Data In #0	I	LVTTL	Float	
ADC_2_D1	F10	Data In #1	I	LVTTL	Float	
ADC_2_D2	K6	Data In #2	I	LVTTL	Float	
ADC_2_D3	L7	Data In #3	I	LVTTL	Float	
ADC_2_D4	D15	Data In #4	I	LVTTL	Float	
ADC_2_D5	E15	Data In #5	I	LVTTL	Float	
ADC_2_D6	F15	Data In #6	I	LVTTL	Float	
ADC_2_D7	F14	Data In #7	I	LVTTL	Float	
ADC_2_D8	H9	Data In #8	I	LVTTL	Float	
ADC_2_D9	L10	Data In #9	I	LVTTL	Float	
ADC_2_D10	C6	Data In #10	I	LVTTL	Float	
ADC_2_D11	G11	Data In #11	I	LVTTL	Float	
ADC_2_OVERLOAD	D14	Over-Voltage Detect	I	LVTTL	Float	
ADC_2_POWER	L5	Power Control	I	LVTTL	Float	
C\B\L\O\C\K\	H6	Bus Lock	I/O	PCI33_3	Float	2mA
C\C\B\E\0\	AF13	Byte Enable 0	I/O	PCI33_3	Float	2mA
C\C\B\E\1\	J5	Byte Enable 1	I/O	PCI33_3	Float	2mA
C\C\B\E\2\	D5	Byte Enable 2	I/O	PCI33_3	Float	2mA
C\C\B\E\3\	C11	Byte Enable 3	I/O	PCI33_3	Float	2mA
C\D\E\V\S\E\L\	E3	Device Select	I	PCI33_3	Float	
C\F\R\A\M\E\	C3	Frame	I/O	PCI33_3	Float	2mA
C\G\N\T\	G5	Access Grant	I	PCI33_3	Float	

C\I\N\T\	F4	Interrupt Request	O	PCI33_3	Float	2mA
C\I\R\D\Y\	D4	Initiator Ready	I/O	PCI33_3	Float	2mA
C\P\E\R\R\	H3	Parity Error	I/O	PCI33_3	Float	2mA
C\R\E\Q\	A10	Access Request	O	PCI33_3	Float	2mA
C\R\S\T\	A8	Reset	I	PCI33_3	Float	
C\S\E\R\R\	A9	System Error	I/O	PCI33_3	Float	2mA
C\S\T\O\P\	F3	Stop Request	I/O	PCI33_3	Float	2mA
C\T\R\D\Y\	D3	Target Ready	I/O	PCI33_3	Float	2mA
CAD0	AD15	Data / Address #0	I/O	PCI33_3	Float	2mA
CAD1	AE15	Data / Address #1	I/O	PCI33_3	Float	2mA
CAD2	AF15	Data / Address #2	I/O	PCI33_3	Float	2mA
CAD3	AF14	Data / Address #3	I/O	PCI33_3	Float	2mA
CAD4	AD14	Data / Address #4	I/O	PCI33_3	Float	2mA
CAD5	AC14	Data / Address #5	I/O	PCI33_3	Float	2mA
CAD6	AA13	Data / Address #6	I/O	PCI33_3	Float	2mA
CAD7	AB12	Data / Address #7	I/O	PCI33_3	Float	2mA
CAD8	AC13	Data / Address #8	I/O	PCI33_3	Float	2mA
CAD9	AD13	Data / Address #9	I/O	PCI33_3	Float	2mA
CAD10	AC12	Data / Address #10	I/O	PCI33_3	Float	2mA
CAD11	AA12	Data / Address #11	I/O	PCI33_3	Float	2mA
CAD12	AB14	Data / Address #12	I/O	PCI33_3	Float	2mA
CAD13	AA14	Data / Address #13	I/O	PCI33_3	Float	2mA
CAD14	M6	Data / Address #14	I/O	PCI33_3	Float	2mA
CAD15	M5	Data / Address #15	I/O	PCI33_3	Float	2mA
CAD16	K3	Data / Address #16	I/O	PCI33_3	Float	2mA
CAD17	C4	Data / Address #17	I/O	PCI33_3	Float	2mA
CAD18	C7	Data / Address #18	I/O	PCI33_3	Float	2mA
CAD19	B6	Data / Address #19	I/O	PCI33_3	Float	2mA
CAD20	A7	Data / Address #20	I/O	PCI33_3	Float	2mA
CAD21	B7	Data / Address #21	I/O	PCI33_3	Float	2mA
CAD22	B9	Data / Address #22	I/O	PCI33_3	Float	2mA
CAD23	B10	Data / Address #23	I/O	PCI33_3	Float	2mA
CAD24	B11	Data / Address #24	I/O	PCI33_3	Float	2mA
CAD25	A12	Data / Address #25	I/O	PCI33_3	Float	2mA
CAD26	B12	Data / Address #26	I/O	PCI33_3	Float	2mA
CAD27	A13	Data / Address #27	I/O	PCI33_3	Float	2mA
CAD28	C8	Data / Address #28	I/O	PCI33_3	Float	2mA
CAD29	C13	Data / Address #29	I/O	PCI33_3	Float	2mA
CAD30	E10	Data / Address #30	I/O	PCI33_3	Float	2mA
CAD31	D10	Data / Address #31	I/O	PCI33_3	Float	2mA
CAUDIO	E8	Audio	O	PCI33_3	Float	2mA
CCLK	E11	CardBus 33 MHz Clock	I	PCI33_3	Float	
CCLKRUN	E13	Clock Request	O	PCI33_3	Float	2mA
CPAR	J4	Parity Even	I/O	PCI33_3	Float	2mA
CSTSCHG	D8	Status Change Interrupt	O	PCI33_3	Float	2mA
DAC_1_CLK_IN+	AC4	Differential Clock In +	O	DIFF HSTL II	Float	
DAC_1_CLK_IN-	AC3	Differential Clock In -	O	DIFF HSTL II	Float	
DAC_1_D0	W5	Data Out #0	O	LVTTL	Float	4mA
DAC_1_D1	W4	Data Out #1	O	LVTTL	Float	4mA
DAC_1_D2	Y3	Data Out #2	O	LVTTL	Float	4mA

DAC_1_D3	AA4	Data Out #3	O	LVTTL	Float	4mA
DAC_1_D4	AA3	Data Out #4	O	LVTTL	Float	4mA
DAC_1_D5	AD4	Data Out #5	O	LVTTL	Float	4mA
DAC_1_D6	AB4	Data Out #6	O	LVTTL	Float	4mA
DAC_1_D7	AD3	Data Out #7	O	LVTTL	Float	4mA
DAC_1_D8	AB7	Data Out #8	O	LVTTL	Float	4mA
DAC_1_D9	AD8	Data Out #9	O	LVTTL	Float	4mA
DAC_1_D10	AB6	Data Out #10	O	LVTTL	Float	4mA
DAC_1_D11	AD6	Data Out #11	O	LVTTL	Float	4mA
DAC_1_D12	AB5	Data Out #12	O	LVTTL	Float	4mA
DAC_1_D13	AD5	Data Out #13	O	LVTTL	Float	4mA
DAC_1_POWER	AC8	Power Control (Inverted)	O	LVTTL	Float	4mA
DAC_2_CLK_IN+	AC7	Differential Clock In +	O	DIFF HSTL II	Float	
DAC_2_CLK_IN-	AC6	Differential Clock In -	O	DIFF HSTL II	Float	
DAC_2_D0	AD9	Data Out #0	O	LVTTL	Float	4mA
DAC_2_D1	AD10	Data Out #1	O	LVTTL	Float	4mA
DAC_2_D2	AC9	Data Out #2	O	LVTTL	Float	4mA
DAC_2_D3	AD11	Data Out #3	O	LVTTL	Float	4mA
DAC_2_D4	AC11	Data Out #4	O	LVTTL	Float	4mA
DAC_2_D5	AB10	Data Out #5	O	LVTTL	Float	4mA
DAC_2_D6	AA10	Data Out #6	O	LVTTL	Float	4mA
DAC_2_D7	AA9	Data Out #7	O	LVTTL	Float	4mA
DAC_2_D8	Y8	Data Out #8	O	LVTTL	Float	4mA
DAC_2_D9	AA8	Data Out #9	O	LVTTL	Float	4mA
DAC_2_D10	AB11	Data Out #10	O	LVTTL	Float	4mA
DAC_2_D11	W9	Data Out #11	O	LVTTL	Float	4mA
DAC_2_D12	AB9	Data Out #12	O	LVTTL	Float	4mA
DAC_2_D13	AA7	Data Out #13	O	LVTTL	Float	4mA
DAC_2_POWER	Y5	Power Control (Inverted)	O	LVTTL	Float	4mA
ETHER_CLK_TERM	H14	125 MHz Clock	I	LVCMOS18	Float	
ETHER_CLK_TERM	K13	125 MHz Clock	I	LVCMOS18	Float	
ETHER_COL	F19	Colision Detect	I	LVCMOS18	Float	
ETHER_CRS	G17	Carrier Sense	I	LVCMOS18	Float	
ETHER_GTX_TERM	A17	Gigabit TX Clock	O	LVCMOS18	Float	4mA
ETHER_IRQ	E22	Interrupt Request	OD	LVCMOS18	Pullup	4mA
ETHER_MDC	F22	Management Clock	O	LVCMOS18	Float	4mA
ETHER_MDIO	G22	Management Data	I/O	LVCMOS18	Float	4mA
ETHER_RESET	F23	Reset	O	LVCMOS18	Float	
ETHER_RX0	D18	RX Data #0	I	LVCMOS18	Float	
ETHER_RX1	B16	RX Data #1	I	LVCMOS18	Float	
ETHER_RX2	A15	RX Data #2	I	LVCMOS18	Float	
ETHER_RX3	B15	RX Data #3	I	LVCMOS18	Float	
ETHER_RX4	F24	RX Data #4	I	LVCMOS18	Float	
ETHER_RX5	D16	RX Data #5	I	LVCMOS18	Float	
ETHER_RX6	C16	RX Data #6	I	LVCMOS18	Float	
ETHER_RX7	F18	RX Data #7	I	LVCMOS18	Float	
ETHER_RX_CLK	K22	RX Clock	I	LVCMOS18	Float	
ETHER_RX_DV	C17	RX Data Valid	I	LVCMOS18	Float	
ETHER_RX_ER	C18	RX Error	I	LVCMOS18	Float	
ETHER_TX0	B17	TX Data #0	O	LVCMOS18	Float	4mA

ETHER_TX1	F20	TX Data #1	O	LVCMOS18	Float	4mA
ETHER_TX2	E21	TX Data #2	O	LVCMOS18	Float	4mA
ETHER_TX3	C23	TX Data #3	O	LVCMOS18	Float	4mA
ETHER_TX4	C21	TX Data #4	O	LVCMOS18	Float	4mA
ETHER_TX5	D21	TX Data #5	O	LVCMOS18	Float	4mA
ETHER_TX6	D23	TX Data #6	O	LVCMOS18	Float	4mA
ETHER_TX7	E23	TX Data #7	O	LVCMOS18	Float	4mA
ETHER_TX_CLK	D19	TX Clock	O	LVCMOS18	Float	4mA
ETHER_TX_CTL	C19	TX Control (Enable)	O	LVCMOS18	Float	4mA
ETHER_TX_ER	E17	TX Error	O	LVCMOS18	Float	4mA
F\L\A\S\H_\B\Y\T\E\	AC17	16 / 8 Bit Mode Select	O	LVCMOS18	Float	4mA
F\L\A\S\H_\C\E\	J16	Chip Enable	O	LVCMOS18	Float	4mA
F\L\A\S\H_\O\E\	H13	Output Enable	O	LVCMOS18	Float	4mA
F\L\A\S\H_\W\E\	AD19	Write Enable	O	LVCMOS18	Float	4mA
FLASH_A0	U17	Address # 0	I/O	LVCMOS18	Float	4mA
FLASH_A1	U15	Address # 1	I/O	LVCMOS18	Float	4mA
FLASH_A2	V11	Address # 2	I/O	LVCMOS18	Float	4mA
FLASH_A3	AC18	Address # 3	I/O	LVCMOS18	Float	4mA
FLASH_A4	Y11	Address # 4	I/O	LVCMOS18	Float	4mA
FLASH_A5	V16	Address # 5	I/O	LVCMOS18	Float	4mA
FLASH_A6	W11	Address # 6	I/O	LVCMOS18	Float	4mA
FLASH_A7	AD18	Address # 7	I/O	LVCMOS18	Float	4mA
FLASH_A8	AB19	Address # 8	I/O	LVCMOS18	Float	4mA
FLASH_A9	AD20	Address # 9	I/O	LVCMOS18	Float	4mA
FLASH_A10	AB20	Address # 10	I/O	LVCMOS18	Float	4mA
FLASH_A11	Y15	Address # 11	I/O	LVCMOS18	Float	4mA
FLASH_A12	AC22	Address # 12	I/O	LVCMOS18	Float	4mA
FLASH_A13	AB21	Address # 13	I/O	LVCMOS18	Float	4mA
FLASH_A14	AA15	Address # 14	I/O	LVCMOS18	Float	4mA
FLASH_A15	AA17	Address # 15	I/O	LVCMOS18	Float	4mA
FLASH_A16	AD16	Address # 16	I/O	LVCMOS18	Float	4mA
FLASH_A17	Y12	Address # 17	I/O	LVCMOS18	Float	4mA
FLASH_A18	AA20	Address # 18	I/O	LVCMOS18	Float	4mA
FLASH_A19	Y16	Address # 19	I/O	LVCMOS18	Float	4mA
FLASH_A20	U16	Address # 20	I/O	LVCMOS18	Float	4mA
FLASH_A21	W16	Address # 21	I/O	LVCMOS18	Float	4mA
FLASH_A22	AD23	Address # 22	I/O	LVCMOS18	Float	4mA
FLASH_A23	AB15	Address # 23	I/O	LVCMOS18	Float	4mA
FLASH_A24	AB16	Address # 24	I/O	LVCMOS18	Float	4mA
FLASH_D0	V12	Data #0	I/O	LVCMOS18	Float	4mA
FLASH_D1	V13	Data #1	I/O	LVCMOS18	Float	4mA
FLASH_D2	V14	Data #2	I/O	LVCMOS18	Float	4mA
FLASH_D3	U14	Data #3	I/O	LVCMOS18	Float	4mA
FLASH_D4	W13	Data #4	I/O	LVCMOS18	Float	4mA
FLASH_D5	Y13	Data #5	I/O	LVCMOS18	Float	4mA
FLASH_D6	W14	Data #6	I/O	LVCMOS18	Float	4mA
FLASH_D7	W15	Data #7	I/O	LVCMOS18	Float	4mA
FLASH_D8	T17	Data #8	I/O	LVCMOS18	Float	4mA
FLASH_D9	J14	Data #9	I/O	LVCMOS18	Float	4mA
FLASH_D10	K12	Data #10	I/O	LVCMOS18	Float	4mA

FLASH_D11	H12	Data #11	I/O	LVCMOS18	Float	4mA
FLASH_D12	K11	Data #12	I/O	LVCMOS18	Float	4mA
FLASH_D13	J11	Data #13	I/O	LVCMOS18	Float	4mA
FLASH_D14	H11	Data #14	I/O	LVCMOS18	Float	4mA
FLASH_D15	AA19	Data #15 / Address -1	I/O	LVCMOS18	Float	4mA
FLASH_READY	AC19	Ready	I	LVCMOS18	Float	4mA
GPIO_1	T4	General Purpose I/O #1	I/O	LVTTL	Float	12mA
GPIO_2	T3	General Purpose I/O #2	I/O	LVTTL	Float	12mA
JTAG_LOOP_TCK	H16	Internal JTAG Loopback Clock	O	LVCMOS18	Float	4mA
JTAG_LOOP_TDI	J15	Internal JTAG Loopback Data In	O	LVCMOS18	Float	4mA
JTAG_LOOP_TDO	G16	Internal JTAG Loopback Data Out	I	LVCMOS18	Float	
JTAG_LOOP_TMS	G15	Internal JTAG Loopback Mode Select	O	LVCMOS18	Float	4mA
LOAD	AB17	TurboLoader Reload Request	O	LVCMOS18	Pulldown	2mA
LOOP_1	U4	Timing Loopback #1	I	LVTTL	Float	
LOOP_1	V4	Timing Loopback #1	O	LVTTL	Float	4mA
LOOP_2	V3	Timing Loopback #2	I	LVTTL	Float	
LOOP_2	W3	Timing Loopback #2	O	LVTTL	Float	4mA
PEEKABOO	AA18	TurboLoader Peekaboo Request	O	LVCMOS18	Pulldown	2mA
POWERCTL_FPGA_C	G12	PSoC Serial Interface Clock	O	LVTTL	Float	4mA
POWERCTL_FPGA_D	F13	PSoC Serial Interface Data	I/O	LVTTL	Float	4mA
RAM_A0	V23	Address #0	O	SSTL18 II	Float	12mA
RAM_A1	N22	Address #1	O	SSTL18 II	Float	12mA
RAM_A2	L18	Address #2	O	SSTL18 II	Float	12mA
RAM_A3	K23	Address #3	O	SSTL18 II	Float	12mA
RAM_A4	T24	Address #4	O	SSTL18 II	Float	12mA
RAM_A5	K21	Address #5	O	SSTL18 II	Float	12mA
RAM_A6	L19	Address #6	O	SSTL18 II	Float	12mA
RAM_A7	J19	Address #7	O	SSTL18 II	Float	12mA
RAM_A8	K18	Address #8	O	SSTL18 II	Float	12mA
RAM_A9	P24	Address #9	O	SSTL18 II	Float	12mA
RAM_A10	K20	Address #10	O	SSTL18 II	Float	12mA
RAM_A11	R23	Address #11	O	SSTL18 II	Float	12mA
RAM_A12	T23	Address #12	O	SSTL18 II	Float	12mA
RAM_BA0	T22	Bank Address #0	O	SSTL18 II	Float	12mA
RAM_BA1	T20	Bank Address #1	O	SSTL18 II	Float	12mA
RAM_BA2	J23	Bank Address #2	O	SSTL18 II	Float	12mA
RAM_C\A\S\	V24	Column Address Select	O	SSTL18 II	Float	12mA
RAM_C\S\	U20	Chip Select	O	SSTL18 II	Float	12mA
RAM_CK_N	R20	Clock -	O	DIFF SSTL18 II	Float	
RAM_CK_P	R21	Clock +	O	DIFF SSTL18 II	Float	
RAM_CKE	U21	Clock Enable	O	SSTL18 II	Float	12mA
RAM_DM0_7	AA23	Data Mask 0	O	SSTL18 II	Float	12mA
RAM_DM8_15	W18	Data Mask 1	O	SSTL18 II	Float	12mA
RAM_DM16-23	H22	Data Mask 2	O	SSTL18 II	Float	12mA
RAM_DM24-31	G24	Data Mask 3	O	SSTL18 II	Float	12mA
RAM_DQ0	Y23	Bidirectional Data #0	I/O	SSTL18 II	Float	12mA
RAM_DQ1	W21	Bidirectional Data #1	I/O	SSTL18 II	Float	12mA
RAM_DQ2	V21	Bidirectional Data #2	I/O	SSTL18 II	Float	12mA
RAM_DQ3	W23	Bidirectional Data #3	I/O	SSTL18 II	Float	12mA
RAM_DQ4	V22	Bidirectional Data #4	I/O	SSTL18 II	Float	12mA

RAM_DQ5	W24	Bidirectional Data #5	I/O	SSTL18 II	Float	12mA
RAM_DQ6	Y22	Bidirectional Data #6	I/O	SSTL18 II	Float	12mA
RAM_DQ7	AA24	Bidirectional Data #7	I/O	SSTL18 II	Float	12mA
RAM_DQ8	AC23	Bidirectional Data #8	I/O	SSTL18 II	Float	12mA
RAM_DQ9	Y20	Bidirectional Data #9	I/O	SSTL18 II	Float	12mA
RAM_DQ10	W20	Bidirectional Data #10	I/O	SSTL18 II	Float	12mA
RAM_DQ11	W19	Bidirectional Data #11	I/O	SSTL18 II	Float	12mA
RAM_DQ12	AA22	Bidirectional Data #12	I/O	SSTL18 II	Float	12mA
RAM_DQ13	AB22	Bidirectional Data #13	I/O	SSTL18 II	Float	12mA
RAM_DQ14	Y17	Bidirectional Data #14	I/O	SSTL18 II	Float	12mA
RAM_DQ15	AD24	Bidirectional Data #15	I/O	SSTL18 II	Float	12mA
RAM_DQ16	L23	Bidirectional Data #16	I/O	SSTL18 II	Float	12mA
RAM_DQ17	H17	Bidirectional Data #17	I/O	SSTL18 II	Float	12mA
RAM_DQ18	M22	Bidirectional Data #18	I/O	SSTL18 II	Float	12mA
RAM_DQ19	M24	Bidirectional Data #19	I/O	SSTL18 II	Float	12mA
RAM_DQ20	G20	Bidirectional Data #20	I/O	SSTL18 II	Float	12mA
RAM_DQ21	N24	Bidirectional Data #21	I/O	SSTL18 II	Float	12mA
RAM_DQ22	G21	Bidirectional Data #22	I/O	SSTL18 II	Float	12mA
RAM_DQ23	N23	Bidirectional Data #23	I/O	SSTL18 II	Float	12mA
RAM_DQ24	J21	Bidirectional Data #24	I/O	SSTL18 II	Float	12mA
RAM_DQ25	G19	Bidirectional Data #25	I/O	SSTL18 II	Float	12mA
RAM_DQ26	H23	Bidirectional Data #26	I/O	SSTL18 II	Float	12mA
RAM_DQ27	F17	Bidirectional Data #27	I/O	SSTL18 II	Float	12mA
RAM_DQ28	H19	Bidirectional Data #28	I/O	SSTL18 II	Float	12mA
RAM_DQ29	L24	Bidirectional Data #29	I/O	SSTL18 II	Float	12mA
RAM_DQ30	H24	Bidirectional Data #30	I/O	SSTL18 II	Float	12mA
RAM_DQ31	J24	Bidirectional Data #31	I/O	SSTL18 II	Float	12mA
RAM_DQS0_N	AD21	Bidirectional Data Strobe 0 -	I/O	DIFF SSTL18 II	Float	
RAM_DQS0_P	AC21	Bidirectional Data Strobe 0 +	I/O	DIFF SSTL18 II	Float	
RAM_DQS1_N	AC24	Bidirectional Data Strobe 1 -	I/O	DIFF SSTL18 II	Float	
RAM_DQS1_P	AB24	Bidirectional Data Strobe 1 +	I/O	DIFF SSTL18 II	Float	
RAM_DQS2_N	C24	Bidirectional Data Strobe 2 -	I/O	DIFF SSTL18 II	Float	
RAM_DQS2_P	D24	Bidirectional Data Strobe 2 +	I/O	DIFF SSTL18 II	Float	
RAM_DQS3_N	D20	Bidirectional Data Strobe 3 -	I/O	DIFF SSTL18 II	Float	
RAM_DQS3_P	E20	Bidirectional Data Strobe 3 +	I/O	DIFF SSTL18 II	Float	
RAM_R\A\S\	U19	Row Address Select	O	SSTL18 II	Float	12mA
RAM_W\E\	U24	Write Enable	O	SSTL18 II	Float	12mA
RFU0	AE13	CardBus RFU 0 / RESERVED	O	PCI33_3	Float	2mA
RFU1	J3	CardBus RFU 1 / RESERVED	O	PCI33_3	Float	2mA
RFU2	D13	CardBus RFU 2 / RESERVED	O	PCI33_3	Float	2mA
VDC_AVID	L4	Active Video Indicator	I	LVTTL	Float	
VDC_CLOCK	W10	Clock	I	LVTTL	Float	
VDC_D0	R3	YCbCr 4:4:2 #0	I/O	LVTTL	Float	4mA
VDC_D1	P5	YCbCr 4:4:2 #1	I/O	LVTTL	Float	4mA
VDC_D2	V8	YCbCr 4:4:2 #2	I/O	LVTTL	Float	4mA
VDC_D3	R5	YCbCr 4:4:2 #3	I/O	LVTTL	Float	4mA
VDC_D4	Y7	YCbCr 4:4:2 #4	I/O	LVTTL	Float	4mA
VDC_D5	U6	YCbCr 4:4:2 #5	I/O	LVTTL	Float	4mA
VDC_D6	U5	YCbCr 4:4:2 #6	I/O	LVTTL	Float	4mA
VDC_D7	P4	YCbCr 4:4:2 #7	I/O	LVTTL	Float	4mA

VDC_FID	P3	Odd / Even Field Indicator	I	LVTTL	Float	
VDC_HSYNC	L3	Horizontal Sync	I	LVTTL	Float	
VDC_INTREQ	M4	Interrupt Request	I/O	LVTTL	Float	4mA
VDC_POWER	N4	Power Control	O	LVTTL	Float	2mA
VDC_RESET	W8	Reset	O	LVTTL	Float	2mA
VDC_SCA	T9	I2C Serial Data	I/O	LVTTL	Float	4mA
VDC_SCL	T8	I2C Serial Clock	O	LVTTL	Float	4mA
VDC_VSYNC	N3	Vertical Sync	I	LVTTL	Float	

Appendix D – CPLD Pinout

CPLD Pinout

Net	Pin	Description	Dir	Standard	Term	Drive
CLOCK_24	13	Free Running 24 MHz Clock from PSoC	I	LVTTL	Float	
F\L\A\S\H_\B\Y\T\E\	35	8 Bit Mode Select	O	LVTTL		Slow
F\L\A\S\H_\C\E\	28	Chip Enable	O	LVTTL		Slow
F\L\A\S\H_\O\E\	17	Output Enable	O	LVTTL		Slow
F\L\A\S\H_\W\E\	1	Write Enable	O	LVTTL		Slow
F\P\G\A_\P\R\O\G\	30	FPGA Asynchronous Erase	O	LVTTL		Slow
FLASH_A0	15	Address 0	I/O	LVTTL	Float	Slow
FLASH_A1	12	Address 1	I/O	LVTTL	Float	Slow
FLASH_A2	10	Address 2	I/O	LVTTL	Float	Slow
FLASH_A3	7	Address 3	I/O	LVTTL	Float	Slow
FLASH_A4	8	Address 4	I/O	LVTTL	Float	Slow
FLASH_A5	11	Address 5	I/O	LVTTL	Float	Slow
FLASH_A6	9	Address 6	I/O	LVTTL	Float	Slow
FLASH_A7	5	Address 7	I/O	LVTTL	Float	Slow
FLASH_A8	47	Address 8	I/O	LVTTL	Float	Slow
FLASH_A9	48	Address 9	I/O	LVTTL	Float	Slow
FLASH_A10	32	Address 10	I/O	LVTTL	Float	Slow
FLASH_A11	33	Address 11	I/O	LVTTL	Float	Slow
FLASH_A12	45	Address 12	I/O	LVTTL	Float	Slow
FLASH_A13	46	Address 13	I/O	LVTTL	Float	Slow
FLASH_A14	44	Address 14	I/O	LVTTL	Float	Slow
FLASH_A15	37	Address 15	I/O	LVTTL	Float	Slow
FLASH_A16	39	Address 16	I/O	LVTTL	Float	Slow
FLASH_A17	6	Address 17	I/O	LVTTL	Float	Slow
FLASH_A18	4	Address 18	I/O	LVTTL	Float	Slow
FLASH_A19	24	Address 19	I/O	LVTTL	Float	Slow
FLASH_A20	14	Address 20	I/O	LVTTL	Float	Slow
FLASH_A21	2	Address 21	I/O	LVTTL	Float	Slow
FLASH_A22	43	Address 22	I/O	LVTTL	Float	Slow
FLASH_A23	34	Address 23	I/O	LVTTL	Float	Slow
FLASH_A24	38	Address 24	I/O	LVTTL	Float	Slow
FLASH_D15	36	Address -1*	I/O	LVTTL	Float	Slow
FPGA_CCLK	25	FPGA Configuration Clock	O	LVTTL		Slow
FPGA_DONE	27	FPGA Configuration Done	I	LVTTL	Float	
FPGA_INIT	26	FPGA Ready to Configure	I	LVTTL	Float	
LOAD	20	FPGA Reload Request	I	LVTTL	Float	
PEEKABOO	18	FPGA Image Address Request	I	LVTTL	Float	

*Pin D15 turns into Address -1 when the Flash ROM is in 8 bit mode.

Appendix E – PSoC Pinout

PSoC Pinout

3\.\3\V_\E\N\	23	3.3V Master Power Enable	O
CLOCK_24_HV	17	24 MHz TurboLoader Clock Out	O
POWERCTL_C	7	PSoC External Debug Clock	I/O
POWERCTL_D	10	PSoC External Debug Data	I/O
POWERCTL_FPGA_C	19	PSoC -> FPGA Clock	I/O
POWERCTL_FPGA_D	22	PSoC -> FPGA Data	I/O
POWERCTL_R	14	PSoC External Debug Reset	I
TEMP_SENSE_C\S\	24	Temperature Sensor Chip Select	O
TEMP_SENSE_SCK	4	Temperature Sensor Clock	O
TEMP_SENSE_SD	5	Temperature Sensor Data	I/O

Appendix F – Standard Part Number Listing

Standard Part Number Listing

Device	Part Number	Website
FPGA	XC4VFX20-10FG672C XC4VFX40-10FG672C XC4VFX60-10FG672C	http://www.xilinx.com/virtex4
CPLD	XC2C64A-7QFG48I	http://www.xilinx.com/cpld
RAM	EDE116ABSE-6E-E	http://www.elpida.com
ROM	S29GL512N11FAIV010	http://www.amd.com/us-en/FlashMemory
Ethernet	88E1111-BAB-I1000	http://www.marvell.com
ADC	AD9233BCPZ-125	http://www.analog.com
DAC	AD9744ACPZRL7	http://www.analog.com
VDC	TVP5150AM1PBS	http://www.ti.com
Temp Sensor	MAX6627MTA+	http://www.maxim-ic.com
Sleep Controller	CY8C21323-24LFXI	http://www.cypress.com

Appendix G – Errata

The following section lists all known errata:

All versions:
Permanent damage will result if the Pico E-15 is left un-configured and powered on for more than 10 minutes. This should not be a problem since the Pico E-15 automatically loads an FPGA image upon power-on.

Appendix H – FPGA Performance Enhancements

Overview:
Like most silicon devices, the FPGA on the Pico E-15 can be overclocked if proper cooling techniques are employed. Care must be taken to avoid thermal runaway.

Thermal Runaway:
As the die temperature of the FPGA increases, it draws more power. This extra power gets turned into heat. If thermal equilibrium is not reached with proper cooling, the FPGA will overheat. The E-15 is protected against catestropic overtemperature conditions via the integrated temperature sensor, although the limits should not routinely be pushed. The maximum FPGA core temperature is 150°C. Note that chips surrounding the FPGA can be damaged by temperatures above 70°C.

Heat Sink Placement:
The heat sink of the FPGA is internally connected via thermal grease to the case of the CardBus card on the bottom side (no markings). Placing a large heat sink on the outside of the case can allow higher performance.

Revision History

1.00.01

Initial public release

Legal Notices

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at their own expense.

CE Class A

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Pico Computing products are not authorized for use in life-critical applications, or where device failure could cause injury or disruption of service.