



# ***Intel<sup>®</sup> IXDP465 Development Platform***

**Quick Start Guide**

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*May 2005*



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## Revision History

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| Date       | Revision | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| May 2005   | 002      | Text updates for this release include: <ul style="list-style-type: none"><li>• Added paragraph about using zoom feature to read PDF in <a href="#">Section 1.0</a>. (SCR 4282)</li><li>• Added references to <i>Intel® IXDP465 Development Platform Specification Update</i>.</li><li>• Added detail to procedure in <a href="#">Section 4.0</a>.</li><li>• Added <a href="#">Section 5.1</a>, “Emulation with the Intel® IXDP465 Development Platform” on page 8.</li><li>• Clarified default settings for J127 and J128 in <a href="#">Table 4</a>. (SCR 4280)</li><li>• Added info about updating flash memory to <a href="#">Section 11.0</a>. (SCR 4281)</li><li>• Updated Figures 1-6, replacing line art with board photos.</li></ul> |
| April 2005 | 001      | Initial release of this document.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

## 1.0 Purpose

This document, the *Intel® IXDP465 Development Platform Quick Start Guide*, contains instructions for unpacking, inspecting, setting up, and starting the Intel® IXDP465 Development Platform.

Before the IXDP465 development platform is powered up for the first time, it is very important to first become familiar with the platform. Therefore, [Section 5.0](#) through [Section 8.0](#) provide the required information for powering up the platform for first time use. These sections provide the following information:

- Photo of the IXDP465 development platform setup for Quick Start operation, showing the location of factory-installed mezzanine modules and location of key interfaces to assist with connection of console, Ethernet, and power cables.
- Factory default settings of all switches and jumpers, allowing the user to ensure they were not accidentally changed during transport, or repositioned by a previous platform user.
- Location and definitions of the LCD display and all the platform LEDs, so that they can be visually monitored for proper power-up and booting.

Instructions for preparing and starting the IXDP465 development platform begin in [Section 9.0](#).

*Note:* It is *highly* recommended that a printout of this entire Quick Start Guide is obtained prior to preparing and powering up the platform for the first time. All tables in this Quick Start Guide include checkboxes so that items in the printout can be checked off to insure that all platform switches, jumpers, and LEDs operate in their default state, which will ensure a successful first-time bootup of the platform.

Use the Zoom feature in Adobe\* Reader\* to optimize viewing of the figure details contained in this document, for example, the switch and jumper locations on the IXDP465 development platform.

*Note:* If any deviations from the factory default settings of this Quick Start Guide are planned, or for more detailed information about this platform, including design definition of all boards, mezzanine cards, platform components, optional modules, optional switch and jumper settings, and overall development capabilities, please see the *Intel® IXDP465 Development Platform User's Guide*.

## 2.0 Applicable Documents and Revisions

The documents referenced below may be obtained online unless noted otherwise.

**Table 1. Reference Documents (Sheet 1 of 2)**

| Title                                                           | Document Number | Location                            |
|-----------------------------------------------------------------|-----------------|-------------------------------------|
| <i>Intel® IXDP465 Development Platform User's Guide</i>         | 306462          | Documentation Web Page <sup>†</sup> |
| <i>Intel® IXDP465 Development Platform Specification Update</i> | 306509          | Intel Representative                |
| <i>Intel® IXDP465 Development Platform Documentation Kit</i>    | N/A             | Documentation Web Page <sup>†</sup> |

† This document is available at:  
<http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm>

†† This document is available at: <http://www.intel.com/design/network/products/npfamily/ixp425swr1.htm>

Table 1. Reference Documents (Sheet 2 of 2)

| Title                                                                                 | Document Number | Location                            |
|---------------------------------------------------------------------------------------|-----------------|-------------------------------------|
| Intel® IXP4XX Product Line of Network Processors Specification Update                 | 306428          | Intel Representative                |
| Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet          | 306261          | Documentation Web Page <sup>†</sup> |
| Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual | 306262          | Documentation Web Page <sup>†</sup> |
| Intel® IXP400 Software Release - Software Release Notes                               | N/A             | Software Web Page <sup>††</sup>     |
| Intel® IXP400 Software - Software Specification Update                                | 273795          | Documentation Web Page <sup>†</sup> |
| Intel® IXP400 Software Programmer's Guide                                             | 252539          | Documentation Web Page <sup>†</sup> |

† This document is available at:  
<http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm>

†† This document is available at: <http://www.intel.com/design/network/products/npfamily/ixp425swr1.htm>

## 3.0 Known Issues

Known issues are described in the following documents:

- Silicon errata: Intel® IXP4XX Product Line of Network Processors Specification Update
- Software errata: Intel® IXP400 Software - Software Specification Update
- Platform errata: Intel® IXP465 Development Platform Specification Update

## 4.0 Inspection

Before the contents of the box are unpacked, ensure that all precautions are observed prior to removing Electrostatic Sensitive Device (ESD) assemblies from their protective packaging.

Unpack the contents of the box. After all the components are unpacked, verify that all the items listed in the packing list are present. The packing list is included in the STOP Readme First document shipped with the kit. If any item is missing, refer to [Section 12.0, “Technical Support”](#) for instructions.

After verifying all items are present:

- Inspect each item for any visible damage.
- Inspect the cable connectors to ensure that none of the pins are bent or damaged.
- Inspect the overall platform assembly to ensure that all mezzanine cards (modules) are properly seated. This can be done by first ensuring that all four 5/8 inch standoffs and nuts on each corner of the mezzanine cards are not loose. If they appear loose either due to shipping or previous handling, then they need to be re-seated per the following procedure:
  - a. Remove all four nuts, by hand-turning them in a counter-clockwise direction as viewed from the top of the assembly.
  - b. Ensure that all four 5/8 inch standoffs are tight, by hand-turning each of them in a clockwise direction while the mezzanine card is still plugged in.

- c. Re-seat the mezzanine card into the connector by applying finger pressure from one hand to the top-side of the mezzanine card directly over the connector while applying finger pressure from your other hand to the bottom-side of the base platform directly under the connector.

**Caution:** Make sure that your fingers on both hands **do not** press against installed components on the assembly.

- d. Verify that the mezzanine card is properly re-seated, by visually confirming there are no gaps between the connectors and no gaps between the four standoffs and the mezzanine card.
- e. Replace all four nuts, by hand-turning and tightening them in a clockwise direction.

If any item is damaged or missing, refer to [Section 12.0, “Technical Support”](#) for instructions.

*Note:*

A set of extra jumpers is included with the kit. These jumpers are not required for default operation of the platform as described in this manual. The extra jumpers are provided for any deviations from the factory default settings which may be required to support optional platform configurations.

## 5.0 Intel® IXDP465 Development Platform Overview

The IXDP465 development platform is used for development with the Intel® IXP46X Product Line of Network Processors, and consists of:

- one Intel® IXDP465 development platform baseboard
- one Intel® IXP465 Network Processor/DDR module (defaulted to 533 MHz operation)
- one Intel® IXPETM465 MII Ethernet PHY mezzanine card

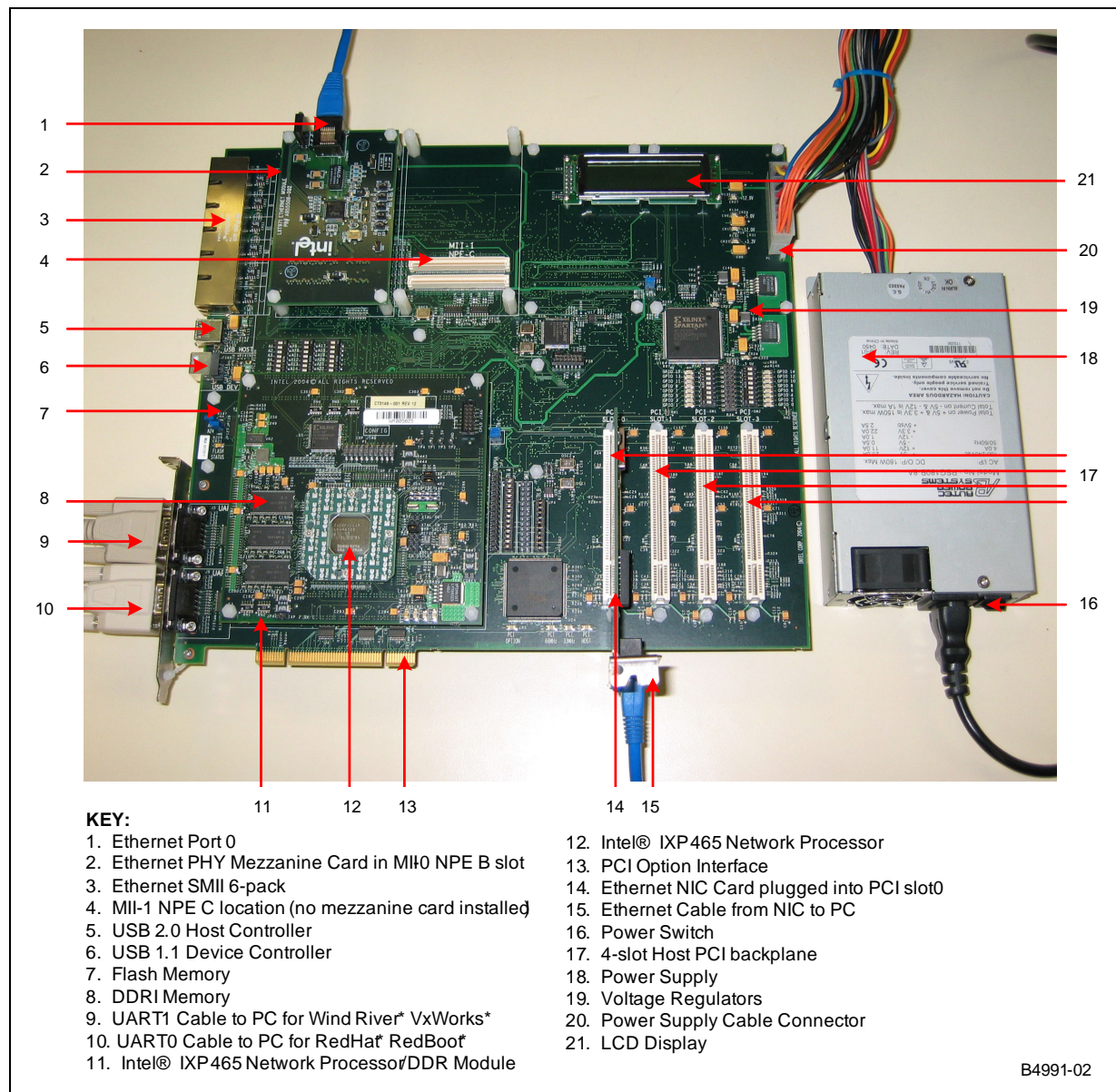
Both the Intel® IXP465 Network Processor/DDR Module and the Intel® IXPETM465 MII Ethernet PHY Mezzanine card plug into the baseboard. These three separate card assemblies are shipped pre-assembled by the factory and should appear per the photo as shown in [Figure 1 on page 8](#). The IXDP465 development platform also ships with a Intel® PRO/100+ Adapter (packaged separately).

[Figure 1](#) represents the top side view of IXDP465 development platform setup and shows all key interfaces and components. This figure should be compared against the platform that was contained in the box, so that familiarity is gained of all key platform components. The platform should also be viewed from the back side, to observe all provisions for optional mezzanine cards, but if more data is required, please see the *Intel® IXDP465 Development Platform User's Guide*.

[Figure 1](#) should also be referenced while preparing the platform for initial use per [Section 9.0](#), to use as a visual aid to validating proper setup of the IXDP465 development platform for Quick Start operation.



Figure 1. Photo of IXP465 Development Platform Setup for Quick Start Operation



## 5.1 Emulation with the Intel® IXP465 Development Platform

The Intel® IXP465 Development Platform can be used for development of products using the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors. Although the IXP465 development platform is shipped with a fully-featured Intel® IXP465 Network Processor operating at 533 MHz, the platform can also be used to develop products that require either an Intel® IXP460 Network Processor or an Intel® IXP455 Network Processor. These processors support subsets of the IXP465 processor’s features, therefore software can be used to disable certain features on the IXP465 to emulate the IXP460 and IXP455 processors.



Emulation is accomplished by accessing the EXP\_UNIT\_FUSE\_RESET register via software and writing a 1 to the fuse bit number that corresponds to the feature to be disabled. For a full description of this register, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer’s Manual*.

Table 2 shows the default fuse bit settings for the fully-featured IXP465 network processor. Other rows in the table show the fuse bit settings which can disable a feature to emulate IXP460 or IXP455 network processor operation.

**Table 2. Fuse Bit Settings for Network Processor Emulation**

| Processor               | Features of Intel® IXP45X and Intel® IXP46X Product Line of Network Processors |     |                |                   |             |                     |                        |        |          |              |                  |               |            |            |     |                  |            |          |                    |                    |
|-------------------------|--------------------------------------------------------------------------------|-----|----------------|-------------------|-------------|---------------------|------------------------|--------|----------|--------------|------------------|---------------|------------|------------|-----|------------------|------------|----------|--------------------|--------------------|
|                         | ECC/1588                                                                       | PCI | NPE-C (crypto) | NPE-B (no crypto) | NPE-A (WAN) | Ethernet C (crypto) | Ethernet B (no crypto) | UTOPIA | HSS/HDLC | Hash/AES/DES | UDC (USB Device) | RCOMP_disable | Core speed | Core speed | RSA | Ethernet B [1-3] | Ethernet A | USB Host | UCP (phy_limit[1]) | UCP (phy_limit[0]) |
| Intel® IXP465 (533 MHz) | 0                                                                              | 0   | 0              | 0                 | 0           | 0                   | 0                      | 0      | 0        | 0            | 0                | 0             | 0          | 0          | 0   | 0                | 0          | 0        | 0                  | 0                  |
| Intel® IXP460 (533 MHz) | 0                                                                              | 0   | 0              | 0                 | 1           | 0                   | 0                      | 1      | 1        | 1            | 0                | 0             | 0          | 0          | 1   | 1                | 1          | 0        | 0                  | 0                  |
| Intel® IXP455 (533 MHz) | 1                                                                              | 0   | 0              | 0                 | 0           | 0                   | 0                      | 0      | 0        | 0            | 0                | 0             | 0          | 0          | 0   | 1                | 0          | 0        | 0                  | 0                  |
| <b>Fuse Bit Number†</b> | 23                                                                             | 22  | 21             | 20                | 19          | 18                  | 17                     | 16     | 13       | 10           | 9                | 8             | 7          | 6          | 5   | 4                | 3          | 2        | 1                  | 0                  |

† Available to software via EXP\_UNIT\_FUSE\_RESET register.

## 6.0 Default Switch Settings

This section describes the factory default settings of all platform switches, to ensure they were not accidentally changed during transport, or repositioned by a previous user of the platform.

The IXDP465 development platform has all switches located on the top-side of the entire assembly. Figure 2 on page 11 identifies the exact location of all switches, clustered into two different areas, one for GPIO LED Switches and one for Expansion Bus Address Strap Switches.

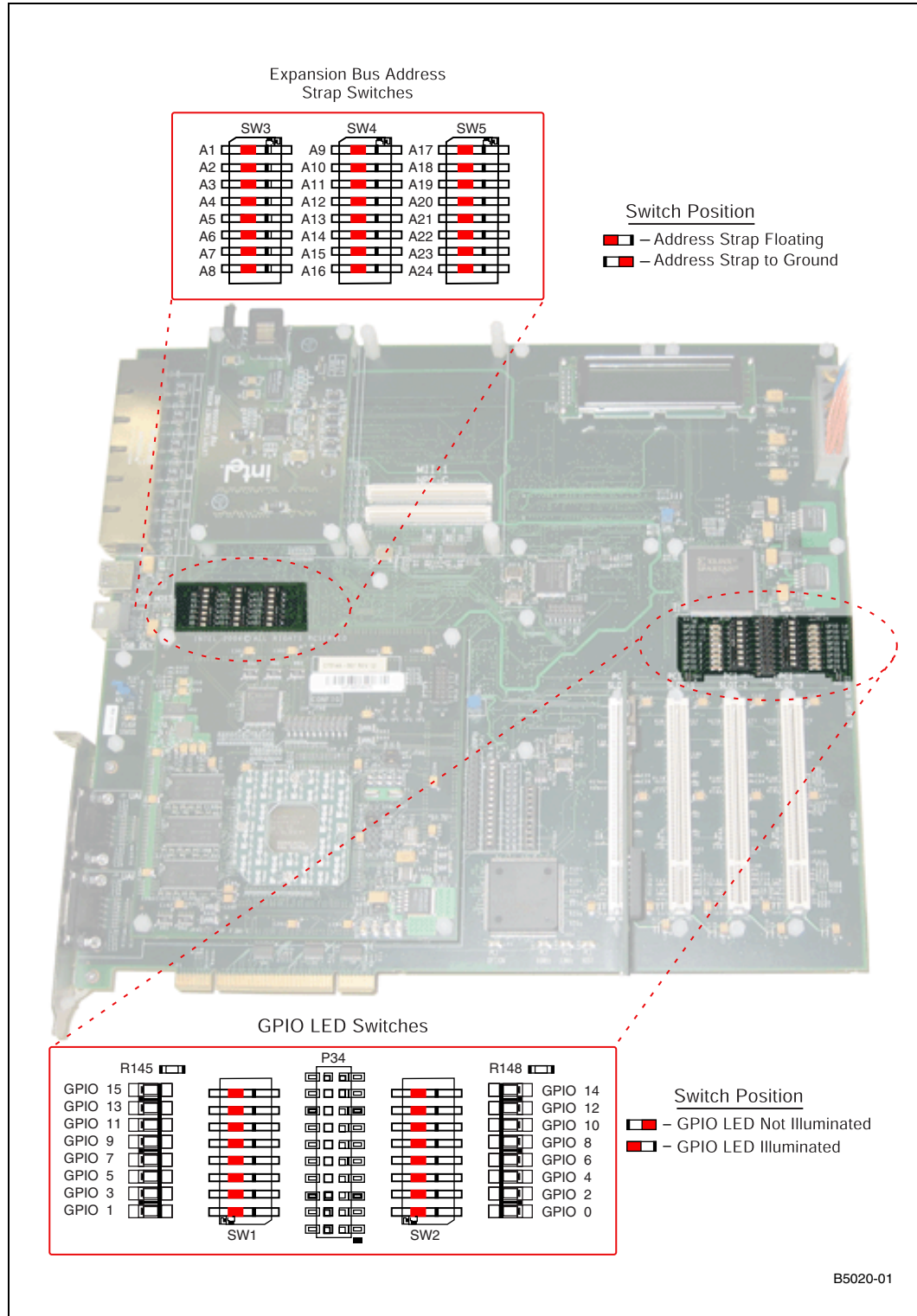
- The GPIO LED Switches (SW1, SW2) allow the choice of connecting any of the 16 GPIO signals to a LED, which can be useful for development purposes. Each GPIO has a green LED indicator attached to it, which when illuminated, indicates a “low” state. A switch is placed on each LED to allow the LED to be disconnected from the GPIO and reduce loading. See Figure 2 on page 11 for the DIP Switch locations. Although the factory default setting for these switches is “LED Illuminated,” these 16 switches can be set to other settings if desired.
- The Expansion Bus Address Strap switches (SW3, SW4, SW5) allows the choice of either floating, or a 1 K pull-down resistor on each of the 24 expansion bus address lines. If set to floating, then a weak internal pull-up resistor in the IXP465 network processor controls the strap value. For operation as defined in this guide, ensure that all switches are set as shown in Figure 2.

All platform switches are summarized in Table 3, which provides a high-level description of each switch and their factory default settings, all of which must be checked prior to powering up the platform for the first time.

**Table 3. Intel® IXDP465 Development Platform Switch Descriptions and Default Settings**

| Board Location<br>(See Figure 2)           | Ref ID | Switch Description                                                   | Default Settings                                     | Quick<br>Start<br>Check? |
|--------------------------------------------|--------|----------------------------------------------------------------------|------------------------------------------------------|--------------------------|
| GPIO LED Switches                          | SW1    | Select individual LED illumination settings of all odd GPIO signals  | All odd GPIO illuminated.<br>Switch in ON position.  | <input type="checkbox"/> |
| GPIO LED Switches                          | SW2    | Select individual LED illumination settings of all even GPIO signals | All even GPIO illuminated.<br>Switch in ON position. | <input type="checkbox"/> |
| Expansion Bus<br>Address Strap<br>Switches | SW3    | Select floating or pull down straps for EX_ADDR[8:1] signals         | All EX_ADDR floating.<br>Switch in OFF position.     | <input type="checkbox"/> |
| Expansion Bus<br>Address Strap<br>Switches | SW4    | Select floating or pull down straps for EX_ADDR[16:9] signals        | All EX_ADDR floating.<br>Switch in OFF position.     | <input type="checkbox"/> |
| Expansion Bus<br>Address Strap<br>Switches | SW5    | Select floating or pull down straps for EX_ADDR[24:17] signals       | All EX_ADDR floating.<br>Switch in OFF position.     | <input type="checkbox"/> |

Figure 2. Intel® IXDP465 Development Platform Switch Locations



B5020-01

## 7.0 Default Jumper Settings

This section defines the factory default settings for all IXDP465 development platform jumpers, to ensure they were not accidentally changed during transport, or repositioned by a previous user of the platform. The jumper settings are discussed in the following sections:

- “Intel® IXDP465 Baseboard Jumpers” on page 12
- “Intel® IXP465 Network Processor/DDR Module Jumpers” on page 15
- “Intel® IXPETM465 Ethernet PHY Mezzanine Card Jumpers” on page 17

Each section contains a jumper summary table which provides a high-level description of each jumper and their factory default settings, all of which must be checked prior to powering up the platform for the first time.

### 7.1 Intel® IXDP465 Baseboard Jumpers

The Intel® IXDP465 baseboard jumpers are located on the top-side of the platform assembly as shown in Figure 3. This figure illustrates the exact location of these jumpers clustered into three different detailed views, along with their default settings.

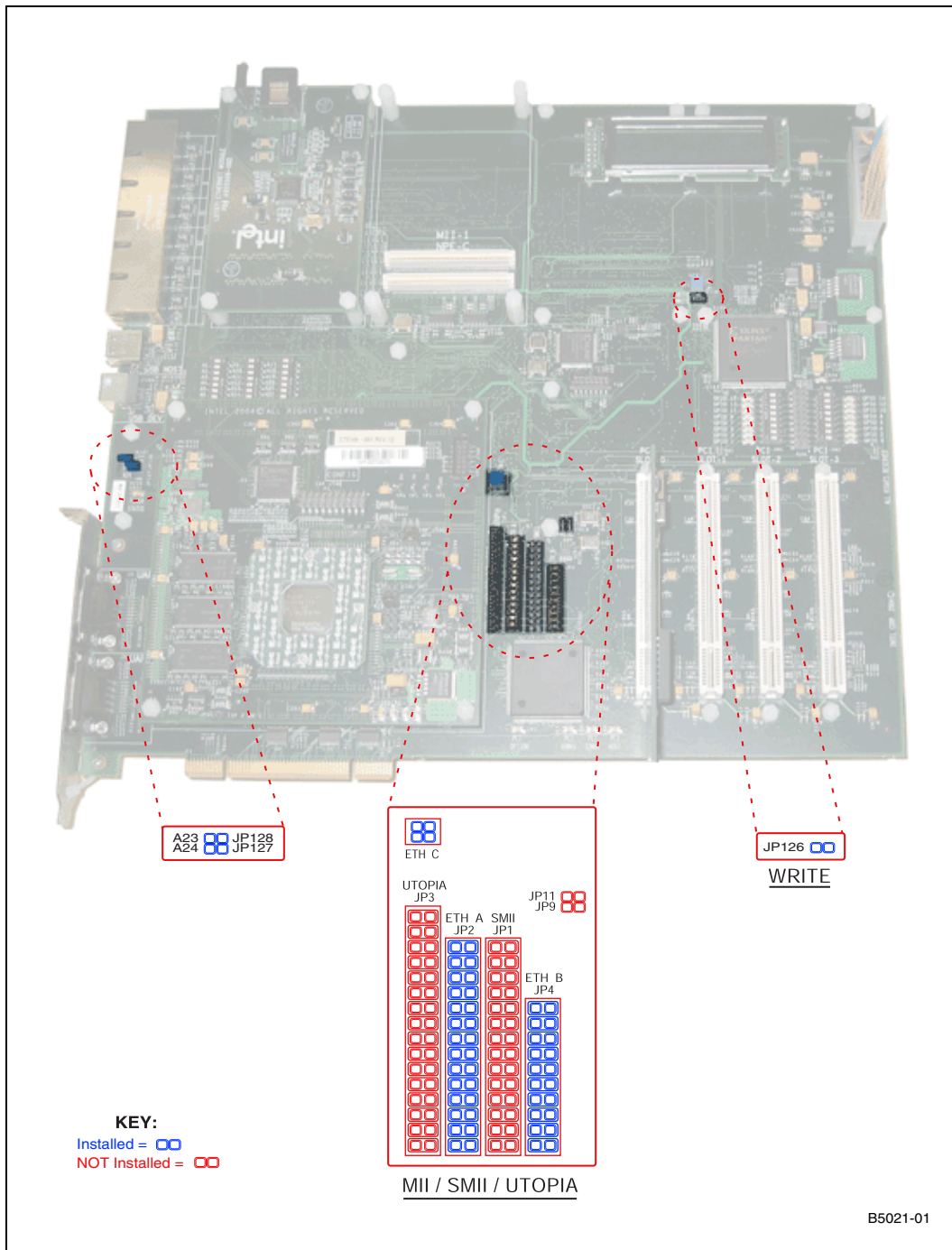
**Table 4. Intel® IXDP465 Baseboard Jumper Descriptions and Default Settings (Sheet 1 of 2)**

| Board Location<br>(See Figure 3) | Ref ID | Jumper Description<br>for Installed State                                                                                                                                                                                                                                          | Default<br>Settings | Quick Start<br>Check?    |
|----------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|--------------------------|
| WRITE                            | JP126  | Disables write protection of the I2C EEPROM device.                                                                                                                                                                                                                                | Installed.          | <input type="checkbox"/> |
| A24                              | JP127  | EX_ADDR24 jumper used in conjunction with JP128 to partition and access the flash device in any of four sections. <ul style="list-style-type: none"> <li>• For RedHat* RedBoot*, install both JP127 and JP128.</li> <li>• For Wind River* VxWorks*, install JP127 only.</li> </ul> | Installed.          | <input type="checkbox"/> |
| A23                              | JP128  | EX_ADDR23 jumper used in conjunction with JP127 to partition and access the flash device in any of four sections. <ul style="list-style-type: none"> <li>• For RedHat* RedBoot*, install both JP127 and JP128.</li> <li>• For Wind River* VxWorks*, install JP127 only.</li> </ul> | Installed.          | <input type="checkbox"/> |
| MII/SMII/UTOPIA: SMII            | JP1    | Connects SMII-specific shared NPE signals to the SMII multi-port PHY                                                                                                                                                                                                               | Not installed.      | <input type="checkbox"/> |
| MII/SMII/UTOPIA: ETH A           | JP2    | Connects ETH A-specific shared NPE signals to the NPE A mezzanine card                                                                                                                                                                                                             | Installed.          | <input type="checkbox"/> |
| MII/SMII/UTOPIA: UTOPIA          | JP3    | Connects UTOPIA-specific NPE signals to the UTOPIA mezzanine card                                                                                                                                                                                                                  | Not installed.      | <input type="checkbox"/> |

**Table 4. Intel® IXDP465 Baseboard Jumper Descriptions and Default Settings (Sheet 2 of 2)**

| Board Location<br>(See Figure 3) | Ref ID       | Jumper Description<br>for Installed State                                 | Default<br>Settings              | Quick Start<br>Check?    |
|----------------------------------|--------------|---------------------------------------------------------------------------|----------------------------------|--------------------------|
| MII/SMII/UTOPIA:<br>ETH B        | JP4          | Connects ETH B-specific shared NPE<br>signals to the NPE B mezzanine card | Installed.                       | <input type="checkbox"/> |
| MII/SMII/UTOPIA:<br>ETH C        | JP65<br>JP95 | Connects ETH C-specific shared NPE<br>signals to the NPE C mezzanine card | Installed.<br>Installed.         | <input type="checkbox"/> |
| MII/SMII/UTOPIA                  | JP9<br>JP11  | Connects a 33 MHz signal on both<br>UTP_OP_CLK and UTP_IP_CLK             | Not installed.<br>Not installed. | <input type="checkbox"/> |

Figure 3. Intel® IXDP465 Baseboard Jumper Locations



## 7.2 Intel® IXDP465 Network Processor/DDR Module Jumpers

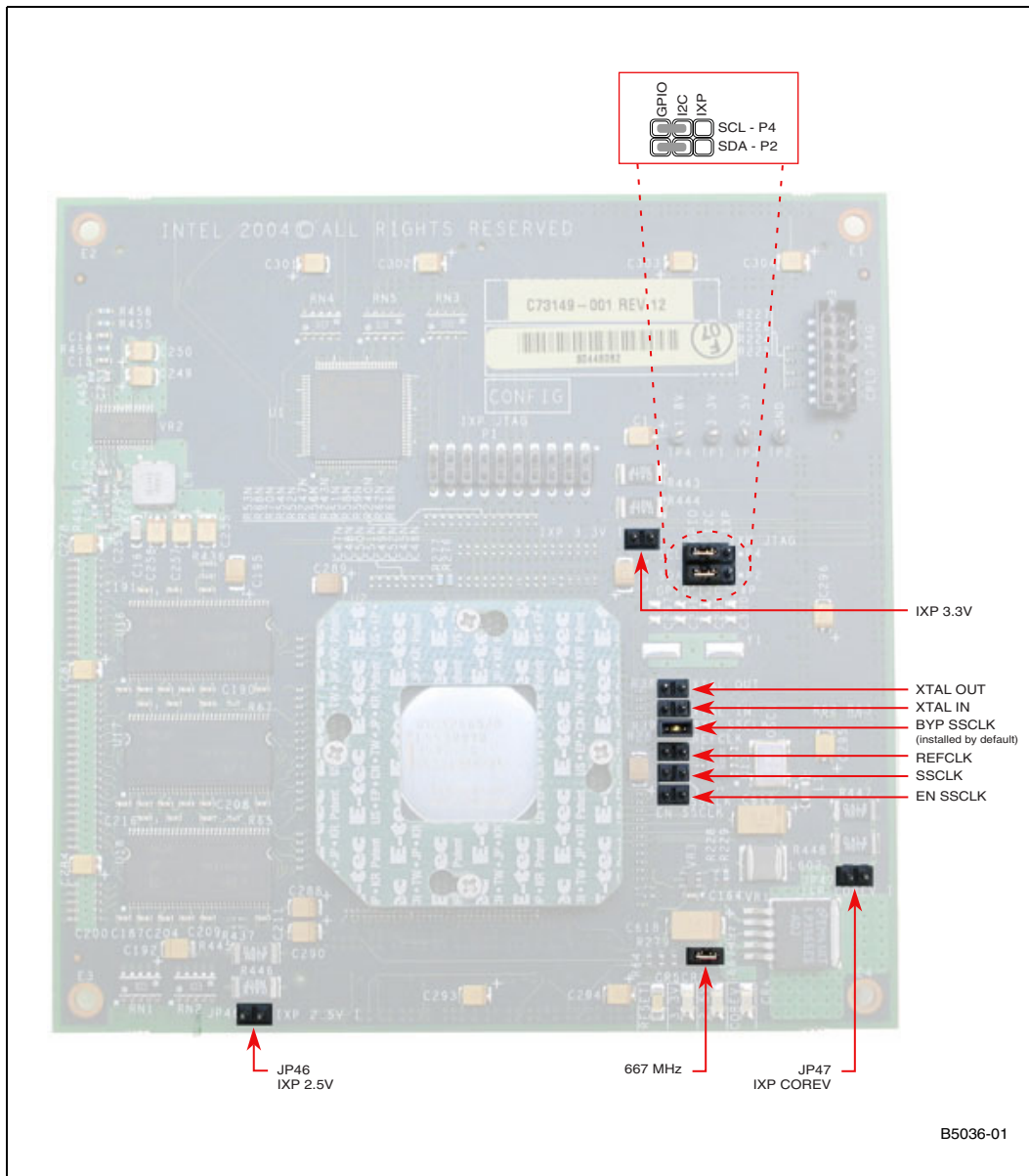
Figure 4 identifies the jumper locations and Table 5 describes the jumper settings for the Intel® IXDP465 Network Processor/DDR module.

**Table 5. Intel® IXDP465 Network Processor/DDR Module Jumper Descriptions and Default Settings**

| Board Location<br>(See Figure 4) | Ref ID | Jumper Description<br>for Installed State                                                      | Default Settings | Quick Start<br>Check?    |
|----------------------------------|--------|------------------------------------------------------------------------------------------------|------------------|--------------------------|
| SCL                              | P4     | Selects I2C pin, instead of GPIO                                                               | Shunt 1-2.       | <input type="checkbox"/> |
| SDA                              | P2     | Selects I2C pin, instead of GPIO                                                               | Shunt 1-2.       | <input type="checkbox"/> |
| IXP 3.3V                         | JP45   | Enables monitoring of +3.3V current                                                            | Not installed.   | <input type="checkbox"/> |
| XTAL OUT                         | JP50   | Reserved                                                                                       | Not installed.   | <input type="checkbox"/> |
| XTAL IN                          | JP49   | Reserved                                                                                       | Not installed.   | <input type="checkbox"/> |
| BYPSSCLK                         | JP41   | Connects oscillator to OSC_IN                                                                  | Installed.       | <input type="checkbox"/> |
| REFCLK                           | JP1    | Enables Spreadpectrum clock reference                                                          | Not installed.   | <input type="checkbox"/> |
| SSCLK                            | JP2    | Connects Spreadpectrum clock to OSC_IN                                                         | Not installed.   | <input type="checkbox"/> |
| ENSSCLK                          | JP44   | Enables Spreadpectrum clock output                                                             | Not installed.   | <input type="checkbox"/> |
| IXP COREV                        | JP47   | Enables monitoring of +1.3V/+1.4V current                                                      | Not installed.   | <input type="checkbox"/> |
| 667 MHz                          | JP48   | Enables selection of +1.3V as core voltage, instead of +1.4V as required for 667 MHz operation | Installed.       | <input type="checkbox"/> |
| IXP 2.5V                         | JP46   | Enables monitoring of +2.5V current                                                            | Not installed.   | <input type="checkbox"/> |



Figure 4. Intel® IXP465 Network Processor/DDR Module Jumper Locations



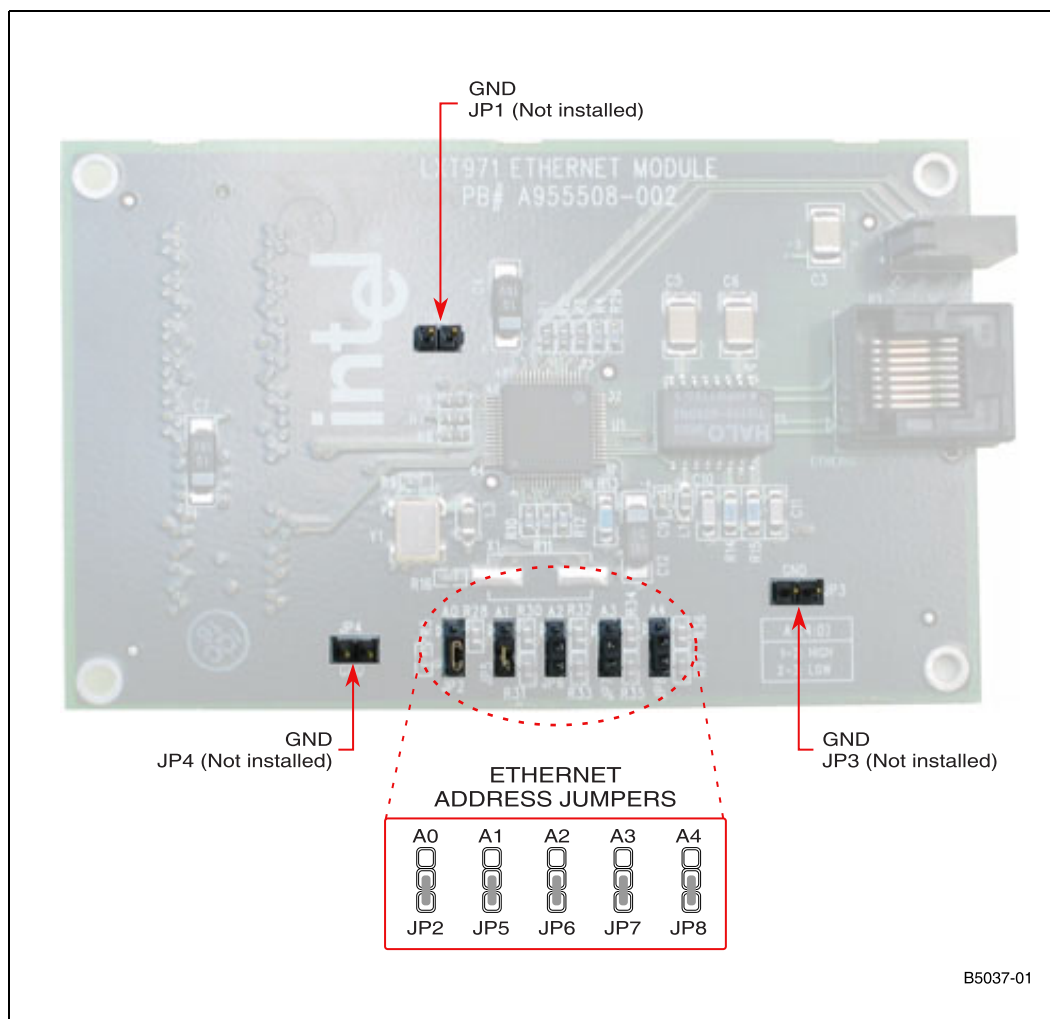
### 7.3 Intel® IXPETM465 Ethernet PHY Mezzanine Card Jumpers

Figure 5 identifies the jumper locations and Table 6 describes the jumper settings for the Ethernet card.

**Table 6. Intel® IXPETM465 Ethernet PHY Mezzanine Card Jumper Descriptions and Default Settings**

| Board Location<br>(See Figure 5) | Ref ID | Jumper Description<br>for Installed State                 | Default Settings | Quick Start<br>Check?    |
|----------------------------------|--------|-----------------------------------------------------------|------------------|--------------------------|
| GND                              | JP1    | GND                                                       | Not installed.   | <input type="checkbox"/> |
| GND                              | JP3    | GND                                                       | Not installed.   | <input type="checkbox"/> |
| A0                               | JP2    | PHY Address A0 for MII-0 NPE-B<br>Ethernet mezzanine slot | Shunt 2-3.       | <input type="checkbox"/> |
| A1                               | JP5    | PHY Address A1 for MII-0 NPE-B<br>Ethernet mezzanine slot | Shunt 2-3.       | <input type="checkbox"/> |
| A2                               | JP6    | PHY Address A2 for MII-0 NPE-B<br>Ethernet mezzanine slot | Shunt 2-3.       | <input type="checkbox"/> |
| A3                               | JP7    | PHY Address A3 for MII-0 NPE-B<br>Ethernet mezzanine slot | Shunt 2-3.       | <input type="checkbox"/> |
| A4                               | JP8    | PHY Address A4 for MII-0 NPE-B<br>Ethernet mezzanine slot | Shunt 2-3.       | <input type="checkbox"/> |
| GND                              | JP4    | GND                                                       | Not installed.   | <input type="checkbox"/> |

Figure 5. Intel® IXPETM465 Ethernet PHY Mezzanine Card Jumper Locations



## 8.0 LCD Display and LED Indicators

This section provides an overview of the LCD display, and also defines the locations, colors, and definitions of all LEDs, so that they can be visually monitored for proper power-up and booting.

The IXP465 development platform provides a 2 x16-digit LCD display that can be used for software debug. The IXP465 Expansion Data Bus directly drives this display. When booting the factory-installed boot images for either Wind River\* VxWorks\* or RedHat\* RedBoot\*, this LCD display can be monitored for visual indication of a successful boot, as described in [Section 10.0](#) of this guide.

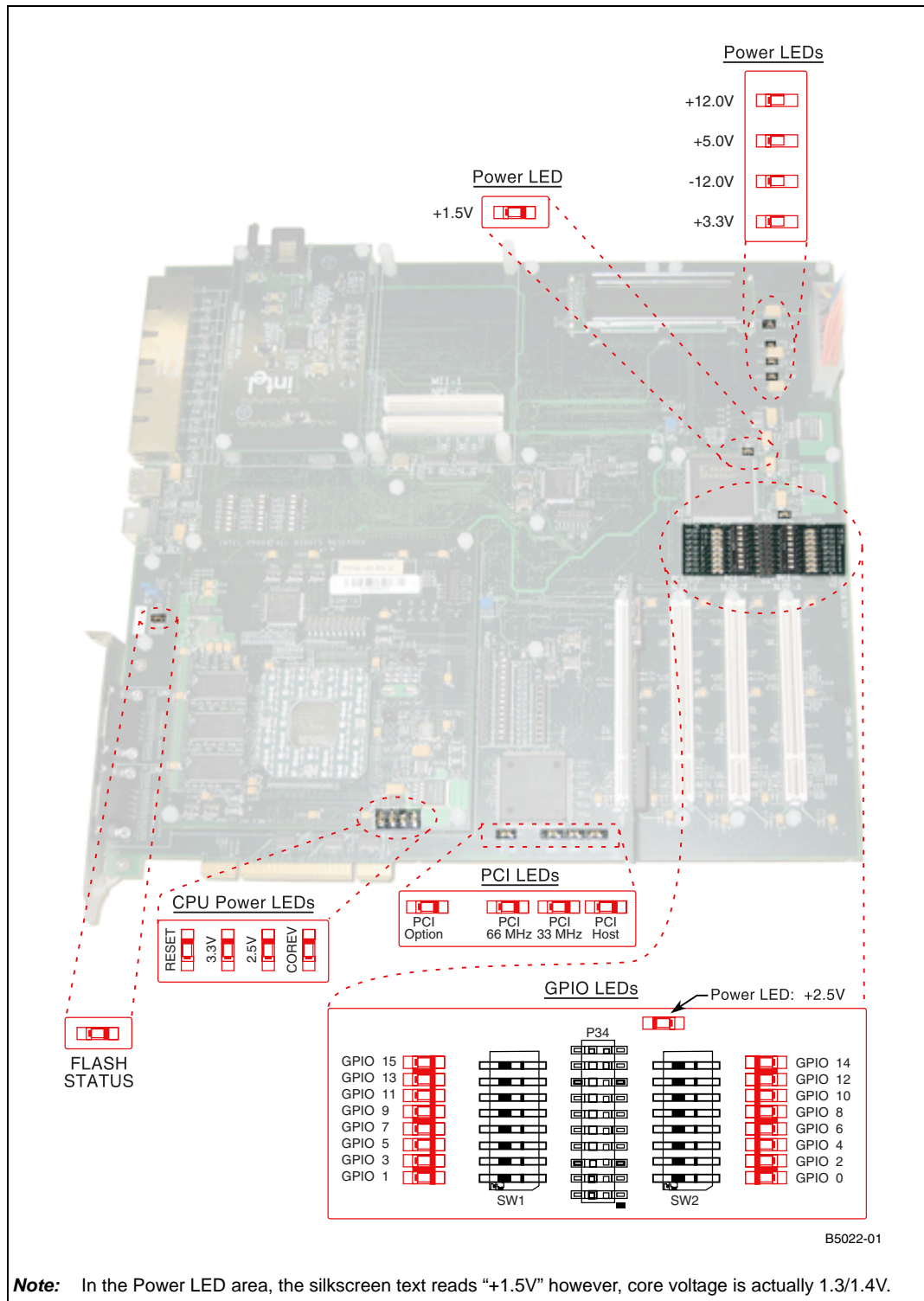
The IXP465 development platform also uses many LEDs scattered throughout the different board assemblies, each of which provides a different visual indication of status, as summarized in [Table 7](#). After powering up the platform for the first time, all of the default settings must be checked to ensure correct operation.

Figure 6 on page 20 shows the exact locations for all LEDs on the IXDP465 development platform, per the descriptions and colors summarized in Table 7.

**Table 7. Intel® IXDP465 Development Platform LED Descriptions and Default Settings**

| Board Location<br>(See Figure 6)                                                  | LED Indication when ON                 | Color  | Default Settings | Quick Start Check        |
|-----------------------------------------------------------------------------------|----------------------------------------|--------|------------------|--------------------------|
| Power LED: +12V                                                                   | +12V power is on                       | Green  | ON               | <input type="checkbox"/> |
| Power LED: +5V                                                                    | +5V power is on                        | Green  | ON               | <input type="checkbox"/> |
| Power LED: -12V                                                                   | -12V power is on                       | Green  | ON               | <input type="checkbox"/> |
| Power LED: +3.3V                                                                  | +3.3V power is on                      | Green  | ON               | <input type="checkbox"/> |
| Power LED: +1.5V <sup>†</sup>                                                     | +1.3V/+1.4V power is on                | Green  | ON               | <input type="checkbox"/> |
| PCI LED: Option                                                                   | PCI operating as option                | Green  | OFF              | <input type="checkbox"/> |
| PCI LED: 66 MHz                                                                   | PCI operating at 66 MHz                | Green  | ON               | <input type="checkbox"/> |
| PCI LED: 33 MHz                                                                   | PCI operating at 33 MHz                | Green  | OFF              | <input type="checkbox"/> |
| PCI LED: Host                                                                     | PCI operating as host                  | Green  | ON               | <input type="checkbox"/> |
| CPU Power LED: Reset                                                              | IXP465 system is in reset              | Green  | OFF              | <input type="checkbox"/> |
| CPU Power LED: 3.3V                                                               | +3.3V power is applied to IXP465       | Green  | ON               | <input type="checkbox"/> |
| CPU Power LED: 2.5V                                                               | +2.5V power is applied to IXP465       | Green  | ON               | <input type="checkbox"/> |
| CPU Power LED: COREV                                                              | +1.3V/+1.4V power is applied to IXP465 | Green  | ON               | <input type="checkbox"/> |
| GPIO LEDs:<br>GPIO 0 - GPIO 15                                                    | GPIO[15:0] driven low                  | Green  | ON               | <input type="checkbox"/> |
| GPIO LEDs: Power LED                                                              | +2.5V power is on                      | Green  | ON               | <input type="checkbox"/> |
| FLASH STATUS                                                                      | Flash device is being programmed       | Yellow | OFF              | <input type="checkbox"/> |
| † Board silkscreen text reads "+1.5V" however, core voltage is actually 1.3/1.4V. |                                        |        |                  |                          |

Figure 6. Intel® IXDP465 Development Platform LED Locations



## 9.0 Preparing the Platform for Initial Use

After unpacking the board and before powering on the board, the IXDP465 development platform needs to be prepared for first time use.

To prepare the platform, follow these steps:

1. Verify that all default switch settings in [Table 3 on page 10](#) are checked off.
2. Verify that all default jumper settings in [Table 4 on page 12](#), [Table 5 on page 15](#), and [Table 6 on page 17](#) are checked off.
3. Confirm that either one of two boot options is selected, controlled by jumper(s) JP127 (A24) and JP128 (A23) as shown in [Figure 3 on page 14](#).
  - For RedBoot, install both JP127 and JP128.
  - For VxWorks, install JP127 only.
4. Install the Intel® PRO/100+ Adapter into PCI slot 0. Connect the straight Ethernet cable provided with the IXDP465 development platform and connect to a hub.

**Note:** An alternative option is to use a cross-over Ethernet cable between the Intel® PRO/100+ Adapter and the host system.

5. Connect the serial cable between COM1 on the host system:
  - to UART0 for Linux\* developers
  - to UART1 for VxWorks\* developers

[Table 8](#) shows the UART serial communication values.

**Table 8. UART Communications Configuration**

| Parameter       | Linux* Value | VxWorks* Value |
|-----------------|--------------|----------------|
| Port            | UART0        | UART1          |
| Bits per Second | 115,200      | 9,600          |
| Data Bits       | 8            | 8              |
| Parity          | None         | None           |
| Stop Bit        | 1            | 1              |
| Flow Control    | None         | None           |

## 10.0 Starting the Platform

To start the platform, follow these steps:

1. Verify that the power switch is in the OFF position on the Autec Power Systems\* power supply provided with the IXDP465 development platform.
2. The power module plugs into the baseboard through a standard ATX 20-pin power supply connector (P1). Connect the ATX power supply cable to ATX connector on the IXDP465 development platform.
3. Power on the board by flipping the black switch on the power supply.
4. Verify that all LED illuminations match the defaults settings listed in [Table 7 on page 19](#).

5. Verify the board booted properly by checking the LCD display
  - for RedBoot bootloader:
    - line 1 = RedBoot
    - line 2 = 0001
  - for VxWorks bootloader: see Figure 7.

**Figure 7. LCD Display for Wind River\* VxWorks\* Bootloader**



## 11.0 Operating the Platform

The software release notes are intended to guide the user through software installation and setup of the host computer, and can be found at the following Web site:

<http://www.intel.com/design/network/products/npfamily/ixp425swr1.htm>

*Note:* You must register and login to download Intel software.

In the “Software Available” section of the above Web site, first click Register/Login, then select the latest current software release; for example, “Intel® IXP400 Software v2.0”. Then click the link for the release notes; for example, “2.0 Release Notes”.

Developers should continue by following the instructions in the software release notes.

Refer to the *Intel® IXP465 Development Platform User’s Guide* for detailed instructions on using the IXP465 development platform, including how to update the IXP465 development platform’s flash memory.

## 12.0 Technical Support

If any of the contents are missing or if you have any questions, contact your local Intel representative.