LXD9785 PQFP Demo Board with FPGA for SS-SMII (Fiber)-to-MII Conversion

Development Kit Manual

January 2002

Order Number: 249323-003

Contents

Figures

Document #: 249323
Revision #: 003
Rev. Date: January 24, 2002

Tables

Revision History

Date	Revision	Page	Description
January 2002	003	All	Replaced LXT9785 with LXT9785/9785E globally
		16	Added new section 4.5 Expended Temperature Operation with the LXT9785HE.
March 2001	002	11	Replaced LXD9785 demo board graphic with A2 version.
		12	Quick Start Jumper Settings table: Added JP15 and JP16.
		13	Quick Start Switch Settings table: - Removed TxSLEW (S5-1:2) - Renumbered remaining switches - Replaced MDIX with Section and new configuration. - Removed “Auto-Negotiation, 10/” under Switch S8. - Changed Setting for S8-6 / CFG_1 from “1” to “0”.
		14	Global Configuration Settings (S5) table: - Removed TxSLEW (S5-1:2); renumbered remaining switches.
		14	Global Configuration Settings (S8) table: - Replaced MDIX with Section and new configuration - Removed “Auto-Negotiation, 10/” from table.
		19 - 35	Replaced A1 schematics with A2.
		36	Bill of Materials (edits throughout for A2 version).

1.0 General Description

The LXD9785 PQFP MII Demo Board is an eight-port 100 Mbps Fast Ethernet Media Access Unit (MAU) that provides a working platform for evaluation of the LXT9785/9785E Fast Ethernet Octal Transceiver. All eight network ports provide a fiber interface for a 100BASE-FX connection.

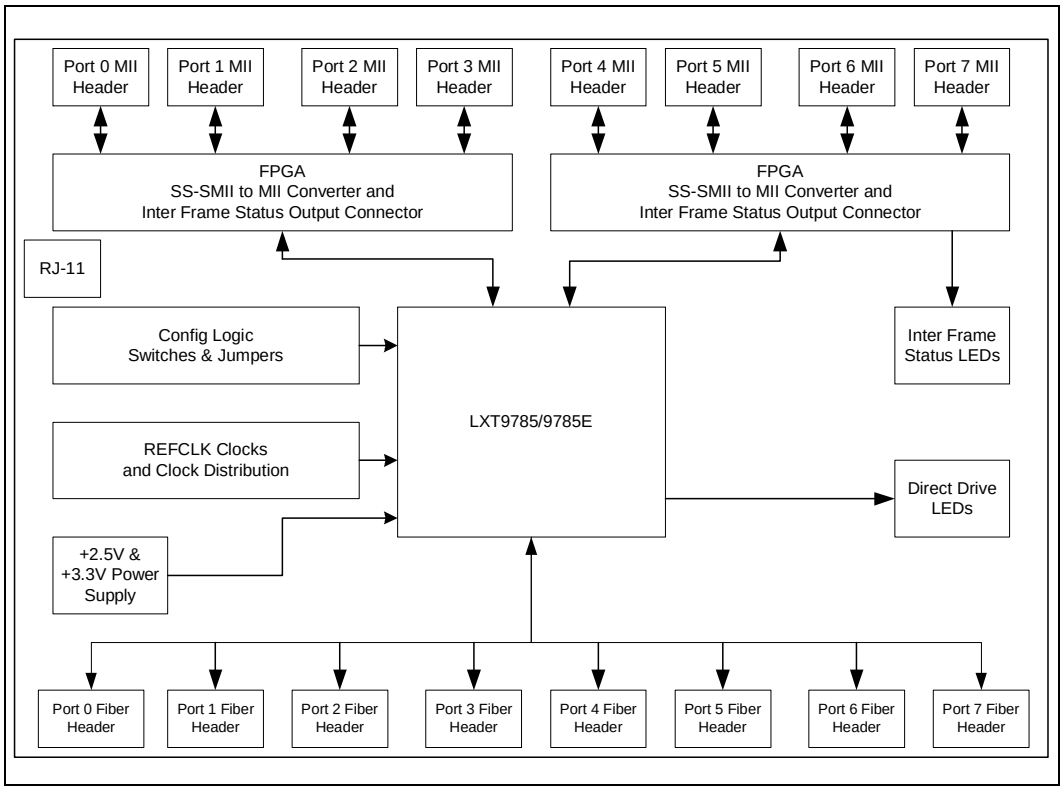
The Demo Board allows system designers to test 100 Mbps Fiber link performance and register functionality using a standard MII interface prior to board prototyping. Two FPGAs convert the eight fiber (SS-SMII) interfaces on the LXT9785/9785E to eight standard MII interfaces. This conversion simplifies evaluation of the LXT9785/9785E, rendering it compatible with existing MII test equipment.

The Demo Board requires three external power supply inputs supplied by 2.5V and 3.3V power supplies.

1.1 Features

- Eight independent IEEE 802.3-compliant 100BASE-FX ports.
- Quick setup, ease of use, and clear visibility of application settings for:
  - Complete system demonstration.
  - Individual circuit isolation.
- JTAG boundary scan.
- Two LED options for major functions:
  - Configuration LEDs which can be controlled through register 20 (*refer to the LXT9785/9785E Datasheet*).
  - Inter Frame Status LED output controlled by FPGAs.
- Configurable via MDIO port or hardware jumpers.

Figure 1. LXD9785 PQFP MII Demo Board



2.0 Introduction

2.1 Overview

This document describes typical hardware set-up procedures for the LXD9785 PQFP MII Demo Board. To begin immediate operation, a "Quick-Start Checklist" on page 12 supports 100BASE-FX operation.

Hardware switches and jumpers allow the designer access to all hardware configuration options. Each option is outlined in the "Optional Configurations" on page 14.

The Demo Board provides two sets of LED indicators: Direct Drive LEDs and Inter Frame Status per-port LEDs. The Direct Drive LEDs can be used to display speed, transmit and receive activities, collision condition, link status, duplex mode, and isolate condition. The Inter Frame Status LEDs can be used to display full-duplex or half-duplex, 10 Mbps or 100 Mbps, or link.

Board schematics and a Bill of Materials are located in the back of the document.

2.2 Equipment Requirements

The LXD9785 Demo Board is populated with all of the IC components needed for twisted-pair evaluation. However, the following additional equipment is also required:

- SmartBits Advanced Multi-port Performance Test Box
- PC with Smart Windows (version 6.51 or newer) installed.
- A 3.3V DC Power Supply.
- A 2.5V DC Power Supply.
- Eight MII Cables (male-to-male).
- Eight external NIC cards.
- Eight fiber cables.

2.3 Fiber Register Configuration

For a register setup via MDIO, proceed with the configuration of the device by setting Register Bit 16.0 to 1 for all ports (see Table 5).

2.4 Typical Setup

Figure 2 shows a typical test setup for standard operation of the LXD9785/9785E PQFP MII Demo Board. The Demo Board plugs into a SmartBits Advanced Multi-port Performance Test Box via eight standard 40-pin MII cables (not included on the board). Eight external NIC cards directly connect to the SmartBits test box and plug into the Demo Board through fiber-module connectors. Each port's operation speed is set globally via hardware or individually via the MDIO for evaluation of 100 Mbps capabilities using all eight ports.

Figure 2. Typical Test Setup

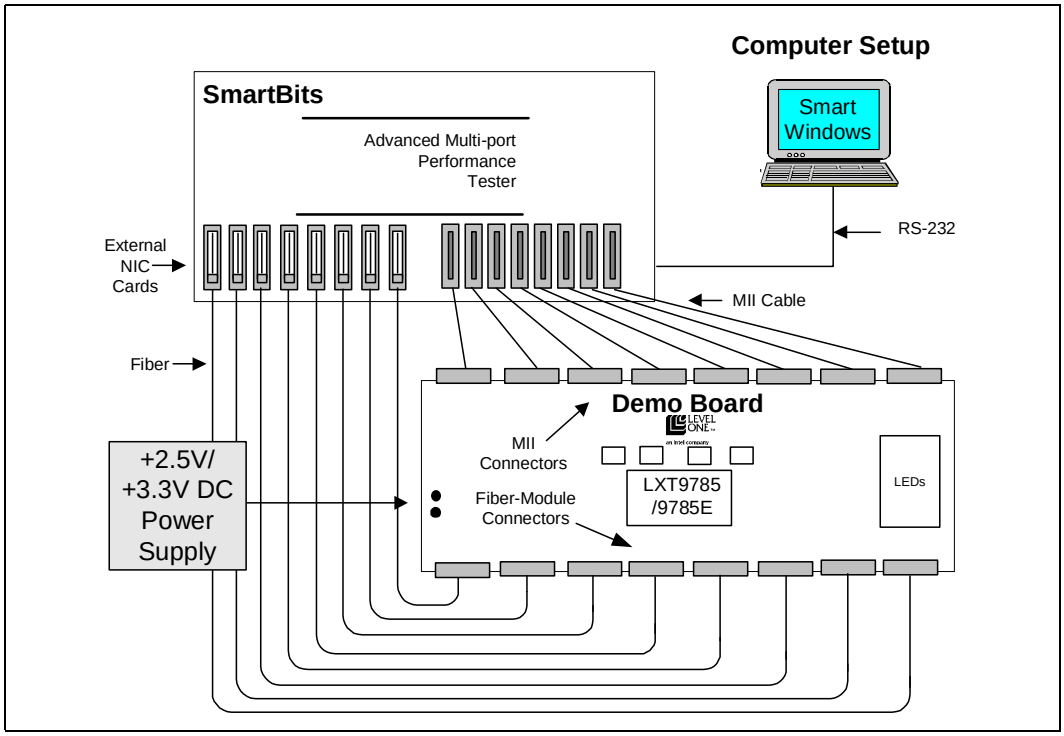
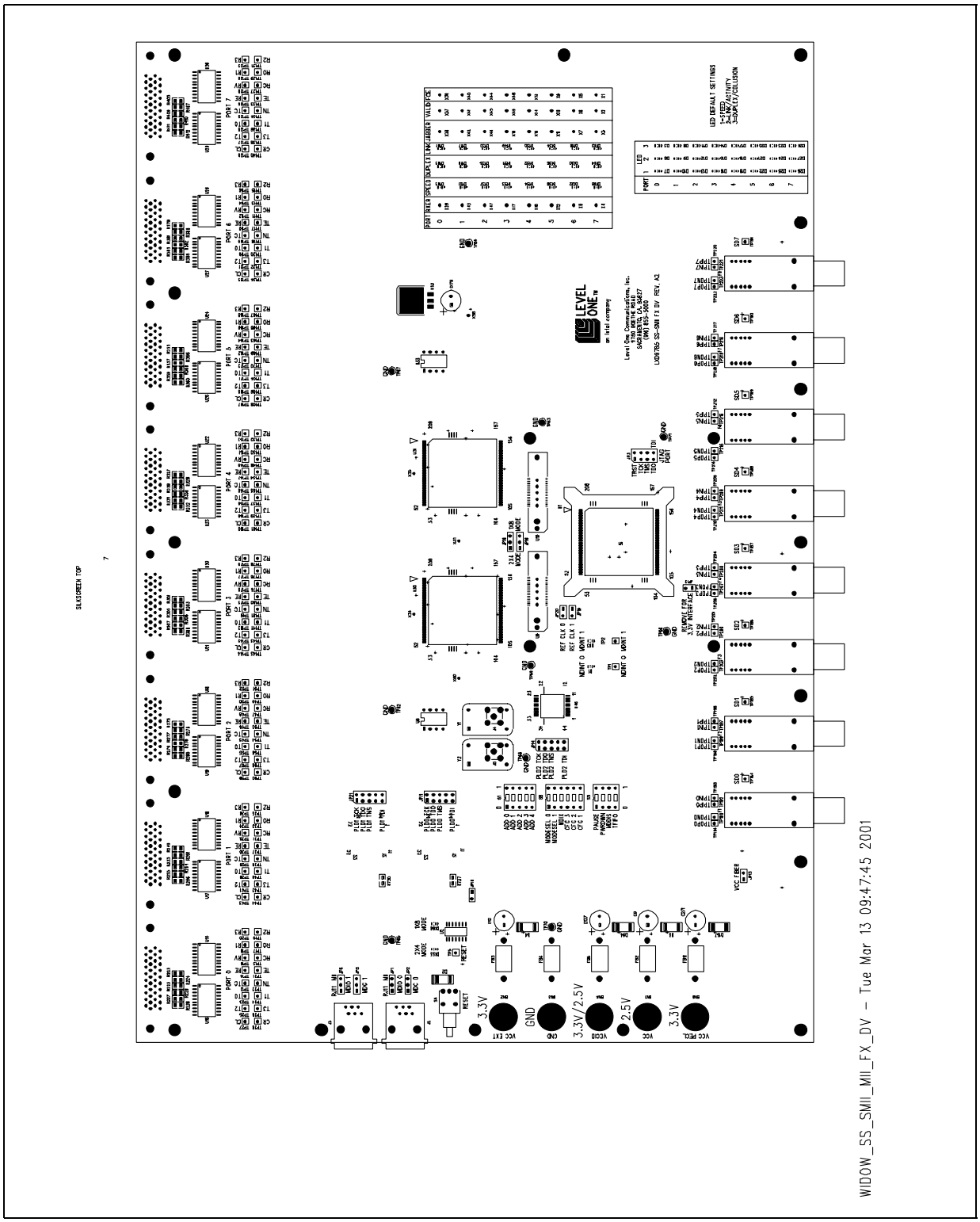


Figure 3. LXD9785/9785E SS-SMII Fiber Demo Board



3.0 Quick-Start Checklist

Use this quick-start procedure for easy setup of the LXD9785 PQFP MII Demo Board. This procedure sets all ports to the default condition (100 Mbps and full-duplex capabilities).

1. Set the jumpers in accordance with Table 1.
2. Set switches S1, S5, and S8 in accordance with Table 2.
3. Connect the eight Demo Board MII ports to the SmartBits test box via MII connector/cables. Male-to- male connectors are required to interface the SmartBits test box to the LXD9785 PQFP MII Demo Board and are available from Newark (.5m cable - Newark P/N 91F9746).
4. Connect the fiber ports to external NIC cards via fiber cables. Each NIC card plugs directly into the SmartBits test box.
5. Connect +2.5V DC power to VCC and a +3.3V DC power supply to VCCIO and VCC-EXT.
6. With the Demo Board appropriately configured, apply power to the LXD9785 PQFP MII Demo Board and press Reset switch S4.
7. Proceed with evaluation as desired.

Table 1. Quick-Start Jumper Settings

Jumper / Label	Setting	Configuration
JP1 / MDIO	Jumper Pins 2 & 3	Routes MDIO through Port 0 MII Connector.
JP2 / MDC	Jumper Pins 2 & 3	Routes MDC through Port 0 MII Connector.
JP12 / SD Interface	Open	Enables 3.3V SD Fiber interface.
JP13	Jumpered	Provides voltage to Fiber transceivers.
JP15	Jumper Pins 2 & 3	Enables 1x8 mode.
JP16	Jumper Pins 1 & 2	Enables 2x4 mode.

Table 2. Quick-Start Switch Settings

Switch / Label	Setting	Configuration
Switch S1		
S1-1 / ADD_0	0	Sets PHY MDIO base address to 00000.
S1-2 / ADD_1	0	
S1-3 / ADD_2	0	
S1-4 / ADD_3	0	
S1-5 / ADD_4	0	
Switch S5		
S5-1 / PAUSE	0	Disables Pause function.
S5-2 / PWRDWN	0	Disables Power-Down function.
S5-3 / MDDIS	0	Enables MDIO channel.
Switch S8		
S8-1 / ModeSel 0	0	Switch settings for SS-SMII mode.
S8-2 / ModeSel 1	1	
S8-3 /Section	0	Enables Section mode: 1x8 or 2x4.
S8-4 / CFG_3	1	Sets port configuration to 100 Mbps and Full-Duplex.
S8-5 / CFG_2	1	
S8-6 / CFG_1	0	

4.0 Optional Configurations

4.1 Global Operating Configurations

Switch S5 and S8 configure operating characteristics on all ports of the LXD9875 Demo Board. Each switch can be set manually by toggling the switch either to 1 or 0. Set switches S5 and S8 to the desired configuration according to Table 3 and Table 4 respectively.

Table 3. Global Configuration Settings (Switch S5)

Switch / Label	Description
S5-1 / PAUSE_0	Pause - Enable Pause capability on all ports. 1 = Pause enabled. 0 = Pause disabled.
S5-2 / PWRDWN	Power-Down - Enable global power-down mode. 1 = Power-Down enabled on all ports. 0 = Normal operation.
S5-3 / MDDIS	Management Disable - Disables MDIO Access. 1 = MDIO is disabled. (no read or write capability). 0 = MDIO is read/write capable (normal operation).

Global configuration settings for Switch S8 are displayed in Table 4.

Table 4. Global Configuration Settings (Switch S8)

Switch / Label	Description			
S8-1 / ModeSel 0	Settings for SS-SMII mode.	ModeSel1	ModeSel0	Mode
S8-2 / ModeSel 1		1	0	SS-SMII
S8-3 /Section	Enables Section mode: 1x8 or 2x4.			
S8-4 / CFG_3	Sets port configuration to 100 Mbps and Full-Duplex.			
S8-5 / CFG_2				
S8-6 / CFG_1				

4.2 MII Address Configurations

The ADDR <4:0> pins are used to configure the MII address by using the configuration settings for Switch S1, as seen in Table 5.

Table 5. PHY Address Configuration Settings (Switch S1)

Jumper / Label	Description
S1-1 / ADD_0	Address <4:0> - Sets base address. Each port adds its port number (starting with 0) to this address to determine its PHY address. Switch "0" sets address bit to 0. Switch "1" sets address bit to 10. Note: To make all ports accessible within the 0 - 31 PHY address range, DO NOT select a base address higher than 24. Port 0 = Base + 0 Port 1 = Base + 1 Port 2 = Base + 2 Port 3 = Base + 3 Port 4 = Base + 4 Port 5 = Base + 5 Port 6 = Base + 6 Port 7 = Base + 7
S1-2 / ADD_1	
S1-3 / ADD_2	
S1-4 / ADD_3	
S1-5 / ADD_4	

4.3 Alternate MDIO Routing Configuration

The MDIO and MDC signals may be routed either through the 40-pin connector for MII Port 0 (the standard configuration) or through an RJ-11 connector (J2), as shown in Table 6. In either configuration, the MII registers can be accessed for each port by setting the correct PHY address. *Refer to the LXT9785/9785E Data Sheet for specific register definitions and functions.* The standard configuration is to route MDIO through the Port 0 MII connector to the SmartBits Test Box by setting the pins for JP1 and JP2 to 2 & 3.

Note: MDIO sectionalization is not supported on this demo board.

Table 6. MDIO Routing (Port 0)

Desired Configuration	Jumper	Setting	Description
Route MDIO0 and MDC0 through MII	JP2	Jumper Pins 2 & 3	Routes MDC0 through Port 0 MII Connector.
	JP1	Jumper Pins 2 & 3	Routes MDIO0 through Port 0 MII Connector.
Route MDIO0 and MDC0 through RJ-11	JP2	Jumper Pins 1 & 2	Routes MDC0 through RJ-11 Connector J2.
	JP1	Jumper Pins 1 & 2	Routes MDIO0 through RJ-11 Connector J2.

4.4 JTAG Test Signals

The boundary scan test port is accessed via JP3 for board- level testing. The JTAG test signal descriptions are shown in Table 7. *The BSDL file for the LXT9785/9785E is available on the Intel web site at http://developer.intel.com/design/network/.*

Table 7. JTAG Test Signal Descriptions

Jumper	Pin#	Symbol	Description
JP3	1	TRST#	**Test Reset**. Input sourced by ATE
	3	TCK	**Test Clock.** Input sourced by ATE.
	5	TMS	**Test Mode Select**. Input sourced by ATE.
	7	TDO	**Test Data Output**. Output sourced by the PHY.
	8	TDI	**Test Data Input**. Input sourced by the ATE.
	2,4,6	GND	Connected to system ground.
JP11 / PLD0	JP11 is used for FPGA debug and is not designated for evaluation of the LXT9785/9785E device.		

4.5 Extended Temperature Operation with the LXT9785HE

The LXT9785HE provides reliable Ethernet transceiver functionality from -40^{o}C to +85^{o}C. Any LXD9785 demo board supporting a QFP package can support an LXT9785HE mounted and localized extended temperature applied to the LXT9785HE. The LXD9785 demo board components are commercial temperature grade.

5.0 LEDs

5.1 Direct Drive LEDs

The LXD9785 PQFP MII Demo Board provides three programmable LED drivers per port (D4 - D28). Each LED can display one of several available status conditions as selected by the LED Configuration Register (Address 20) shown in Table 8.

Table 8. Direct Drive LED Configuration Settings (Register 20)

LED Bits			Program Bits	Description
LED1	LED2	LED3		
15:12	11:8	7:4	0000	**Indicates 100 Mbps operation. (Default for LED1)**
			0001	Indicates transmit (Stretched).
			0010	**Indicates receive (stretched). (Default for LED3)**
			0011	Indicates collision (Stretched).
			0100	**Indicates active link (continuous). (Default for LED2)**
			0101	Indicates full-duplex.
			0110	Reserved.
			0111	Indicates transmit or receive activity.
			1000	Test Mode. Turn LED on (continuous).
			1001	Test Mode. Turn LED off (continuous).
			1010	Test Mode. Blink LED fast (continuous).
			1011	Test Mode. Blink LED slow (continuous).
			1100	Indicates link and receive status combined[1] (Stretched)[2].
			1101	Indicates link and activity status combined[1] (Stretched)[2].
			1110	Indicates duplex and collision status combined[3] (Stretched)[2].
			1111	Reserved.

1. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up. The secondary LED driver (receive, activity, or isolate) causes the LED to change state (blink).
2. Combined event LED settings are not affected by bit 20.1 (Pulse Stretch). These settings are stretched regardless of the value of 20.1.
3. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full-duplex. Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.

The programmable LEDs (LED_1, LED_2, and LED_3) are set in the default mode and are programmable via the MDIO pin. Register address 20 also provides optional LED pulse stretching up to 100 ms. Register bits 20.3:2 select one of three possible stretch times as shown in Table 9 on page 18.

Table 9. LED Pulse Stretch Settings (Register 20)

Bit	Name	Description	Type	Default
20.3:2	LEDFREQ	00 = Stretch LED events to 30 ms. 01 = Stretch LED events to 60 ms. 10 = Stretch LED events to 100 ms. 11 = Reserved.	R/W	00
20.1	PULSE-STRETCH	0 = Disable pulse stretching of all LEDs. 1 = Enable pulse stretching of all LEDs.	R/W	1

5.2 Inter Frame Status LEDs

By using the conversion FPGAs, the Inter Frame Status information for Speed status, Duplex status, and Link status are output to an LED circuit. The LEDs (D101 - D154) provide a continuous, real-time status for all eight ports. This feature is provided to assist the customer in evaluation of the Inter Frame Status operation.

6.0 Board Schematics

Figure 4. LXD9785 PQFP MII Demo Board Power (Fiber Board Revision A2)

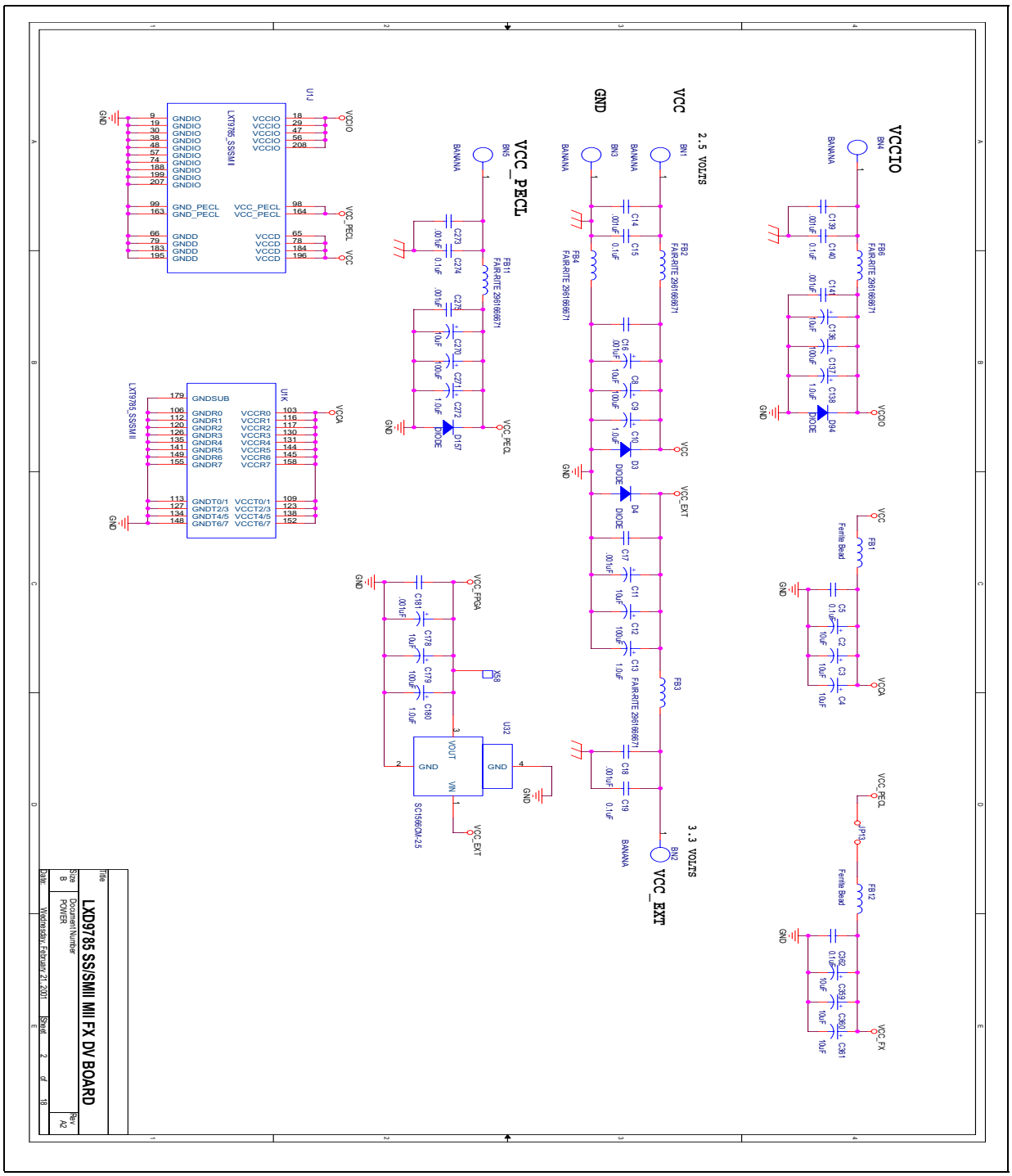


Figure 5. Control

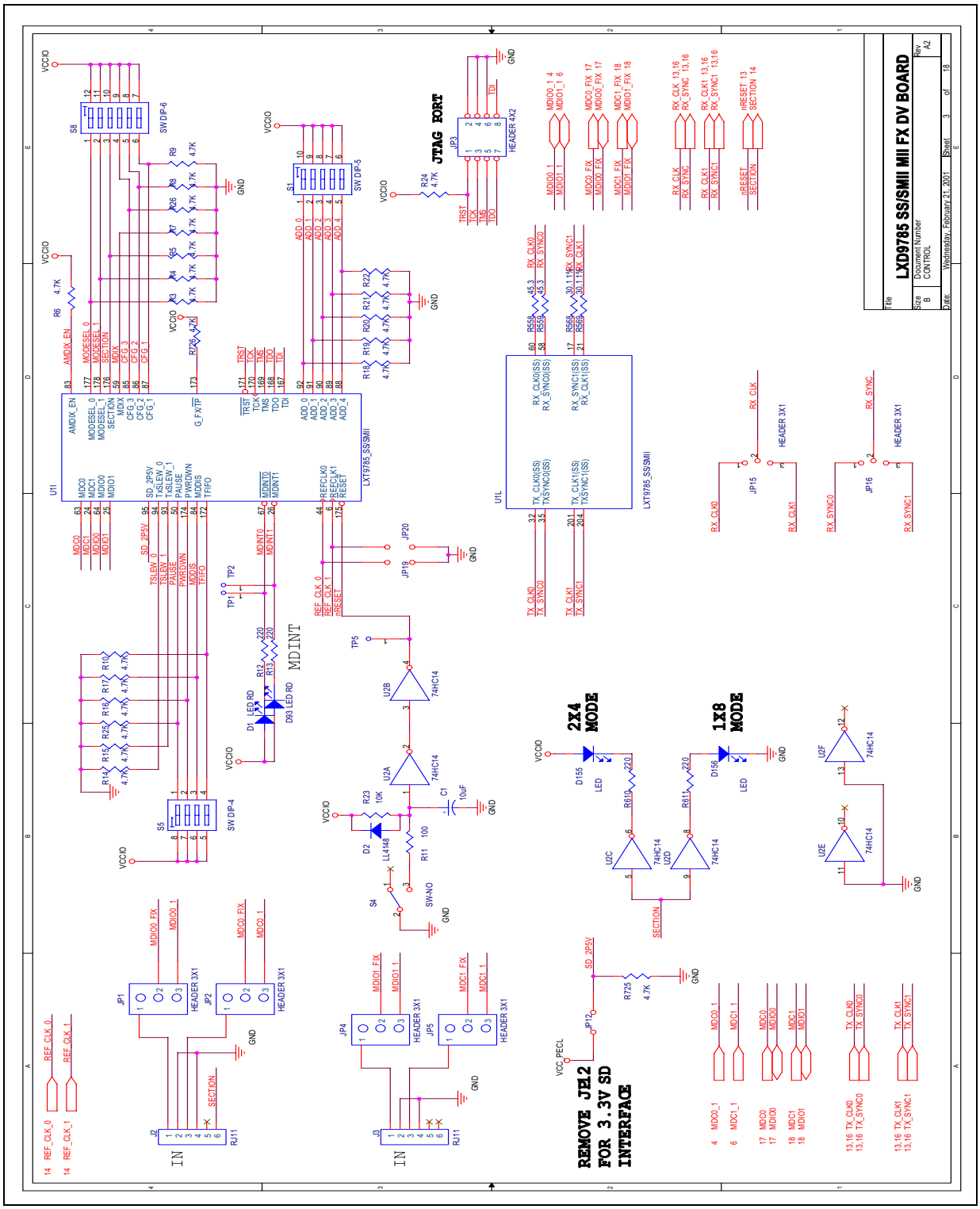


Figure 6. MII Ports 0 and 1

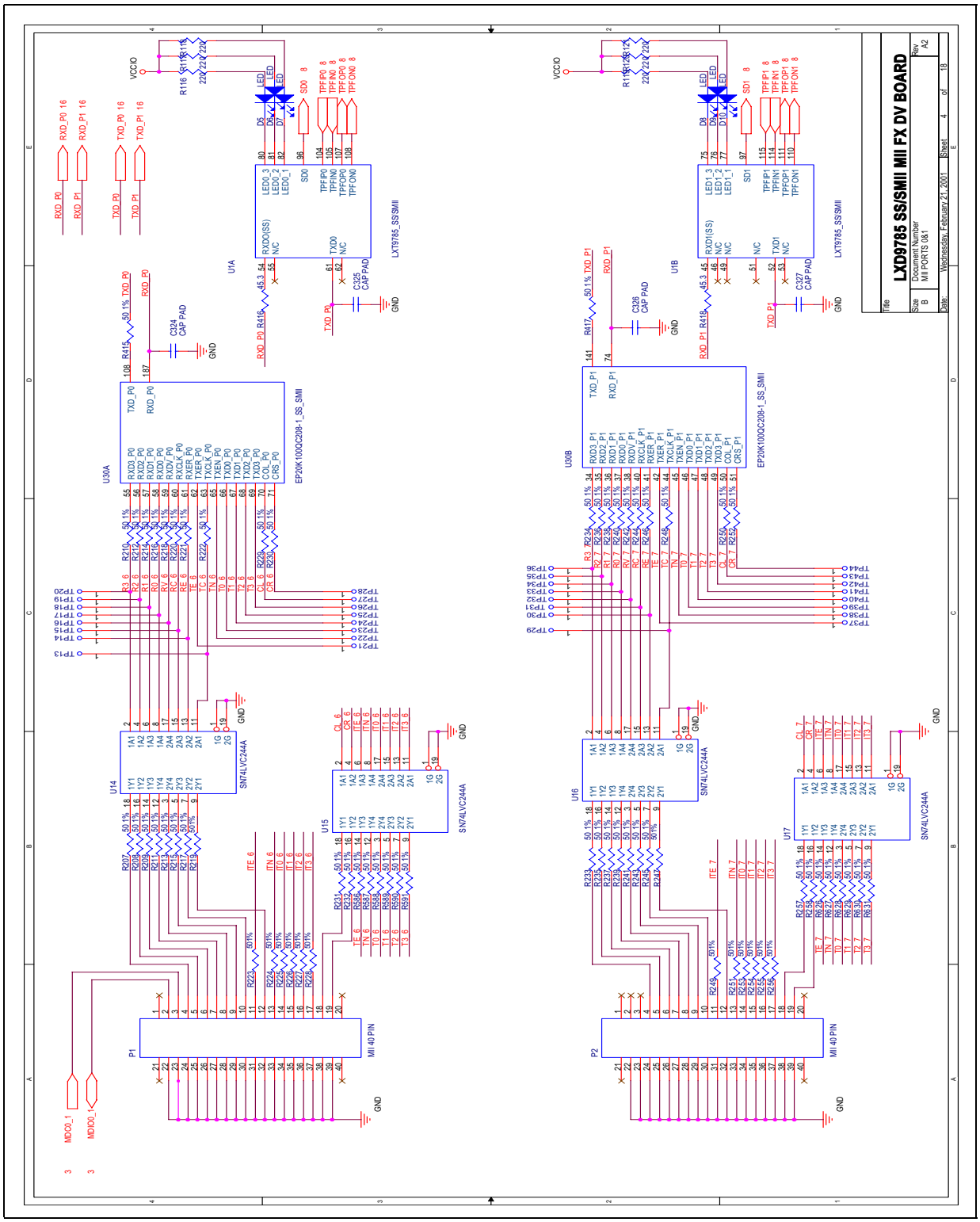


Figure 7. MII Ports 2 and 3

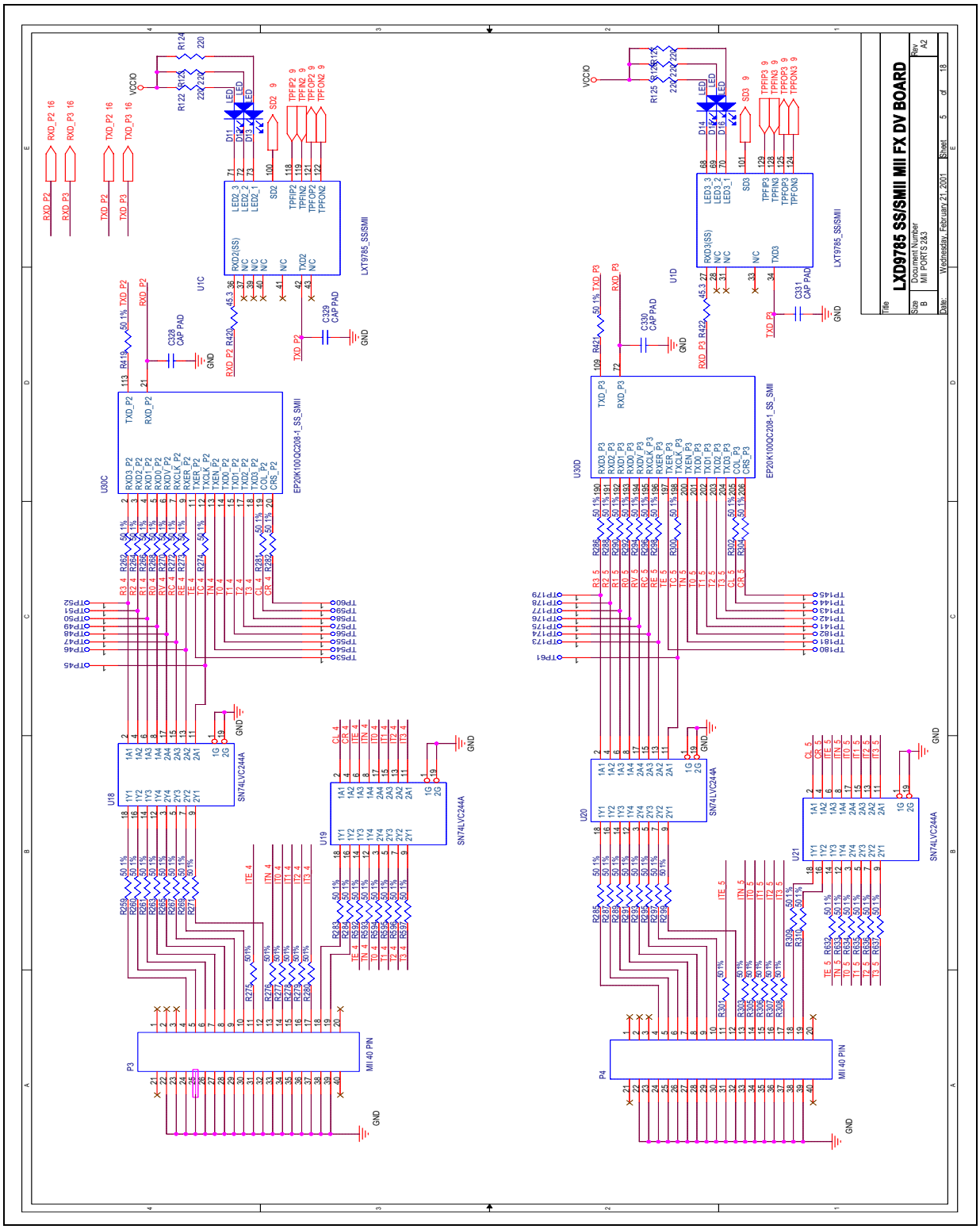


Figure 8. MII Ports 4 and 5

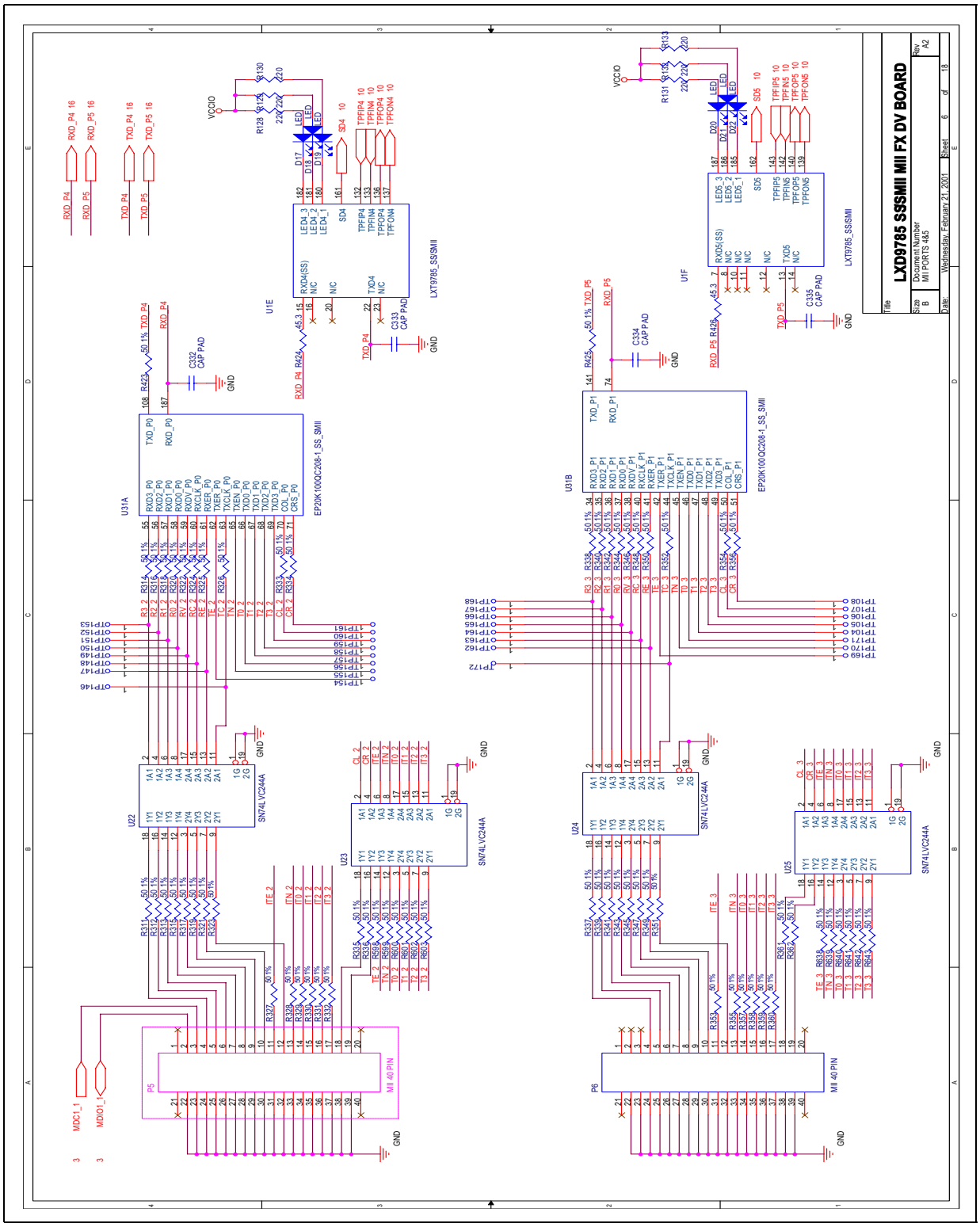


Figure 9. MII Ports 6 and 7

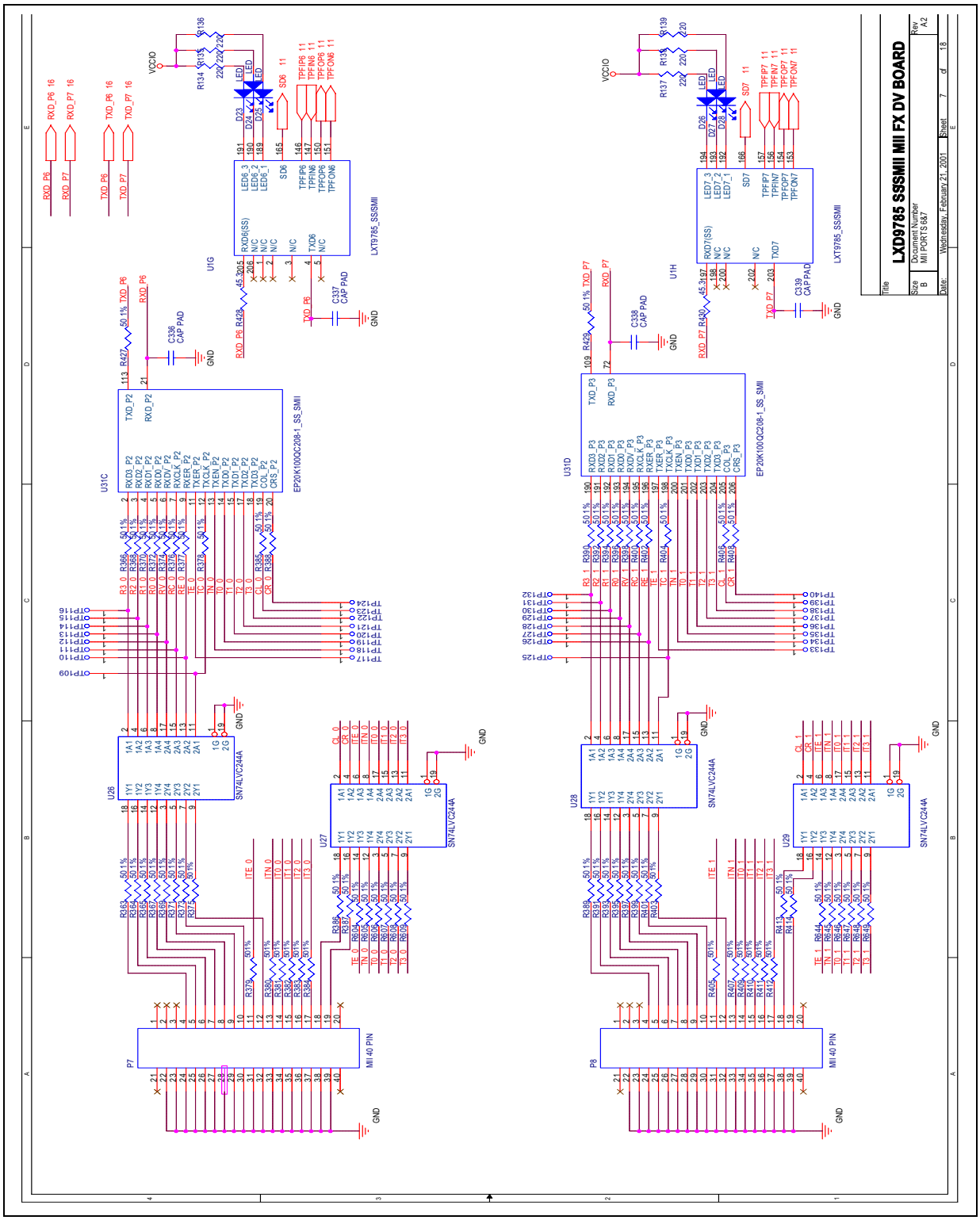


Figure 10. Fiber Ports 0 and 1

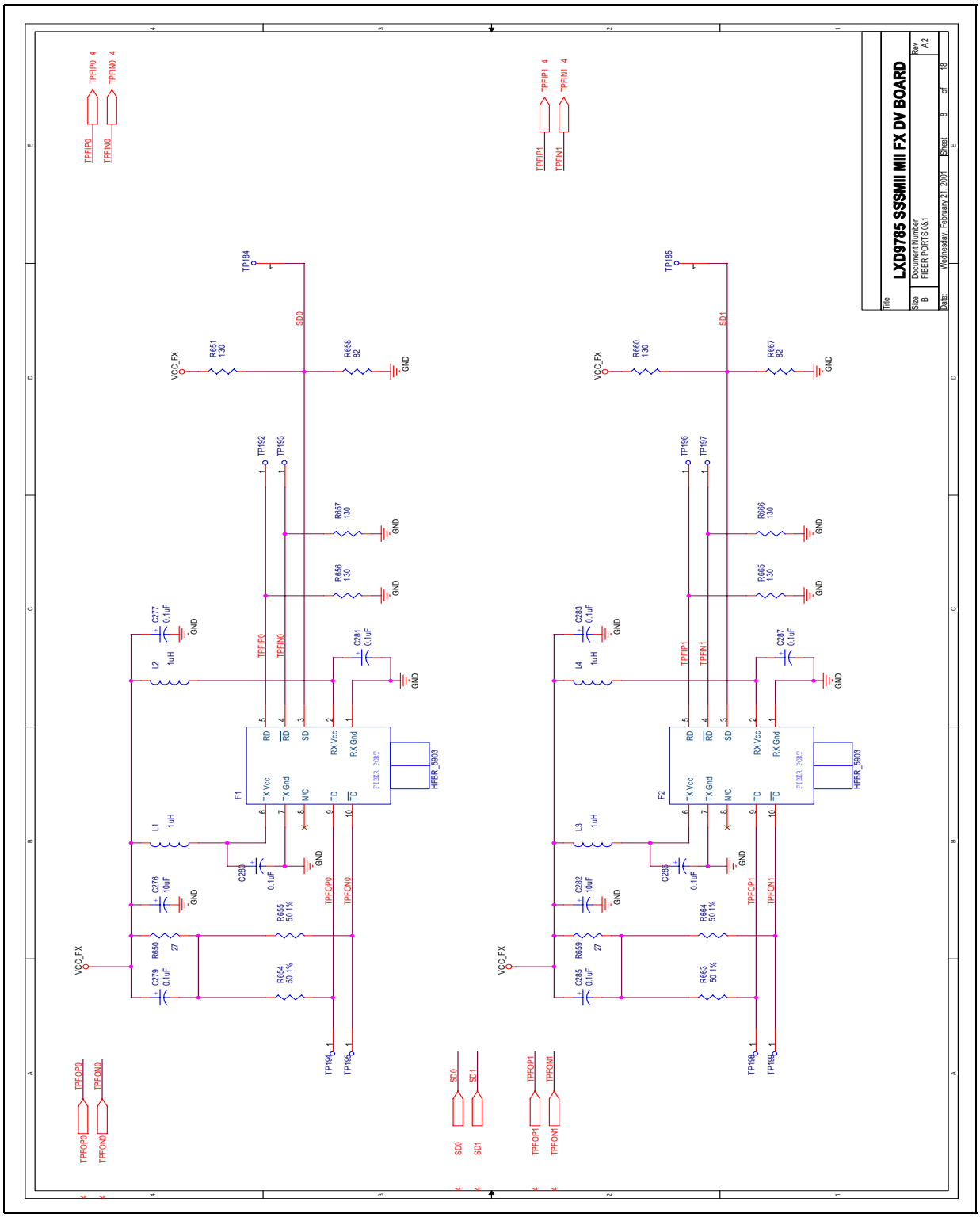


Figure 11. Fiber Ports 2 and 3

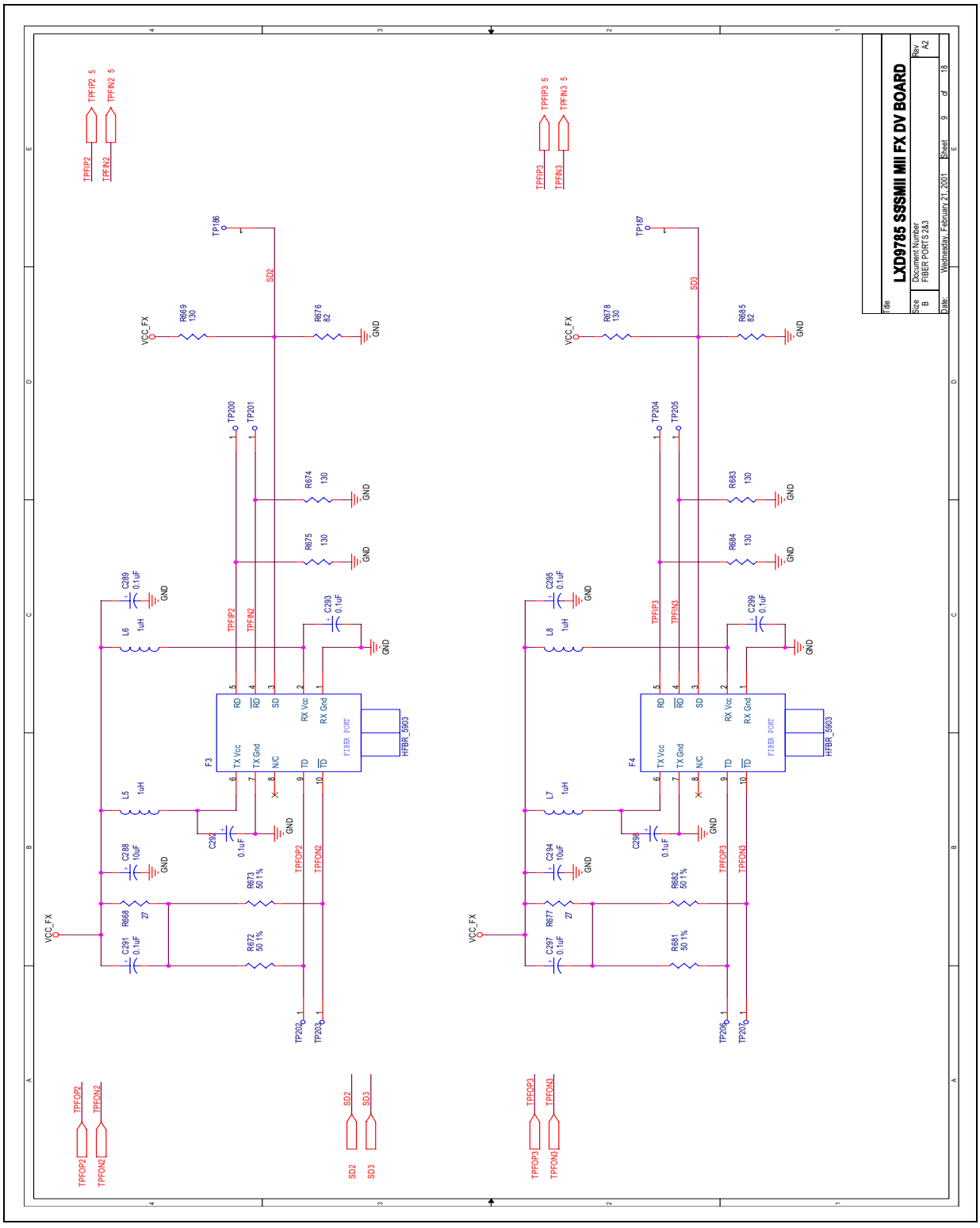


Figure 12. Fiber Ports 4 and 5

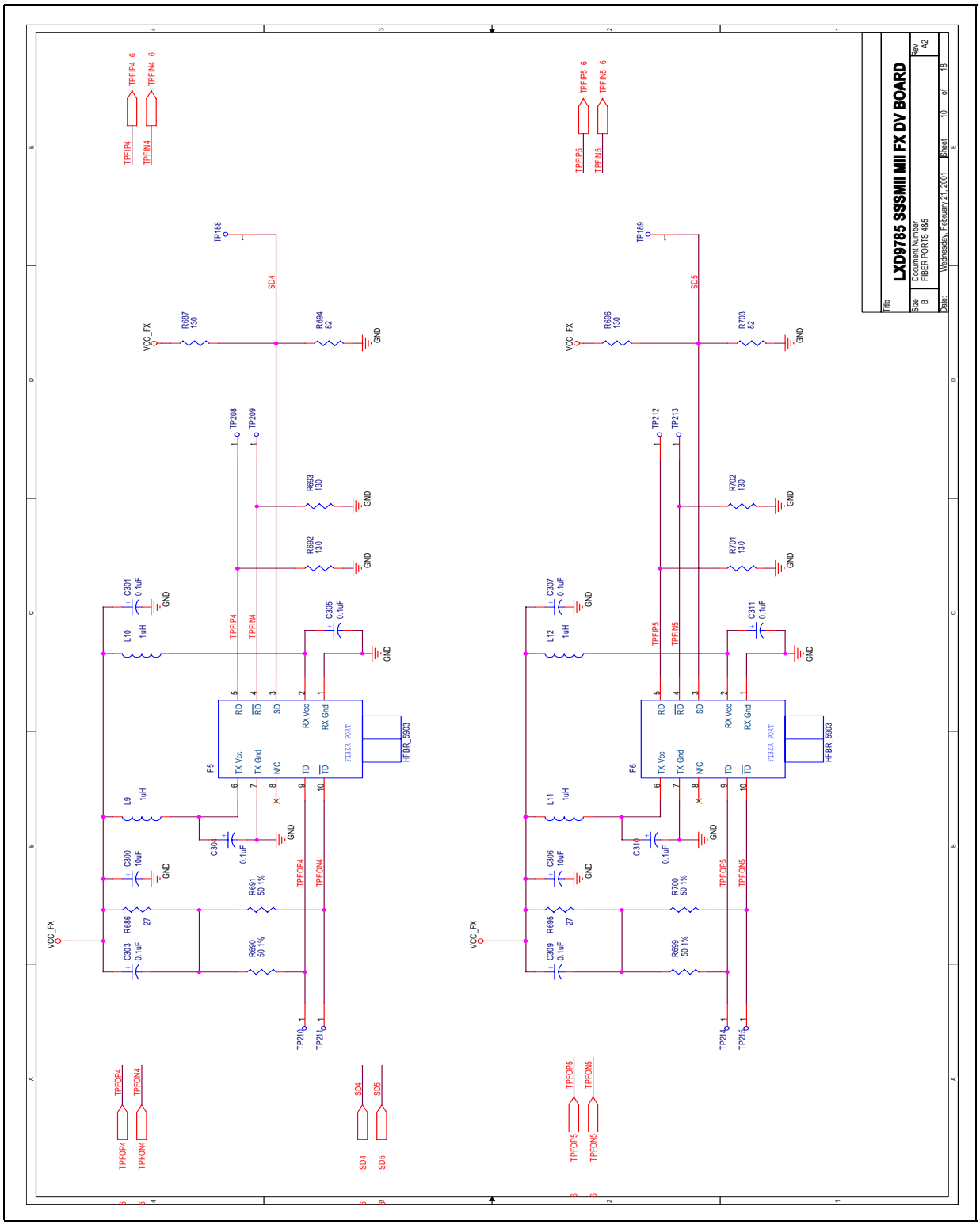


Figure 13. Fiber Ports 6 and 7

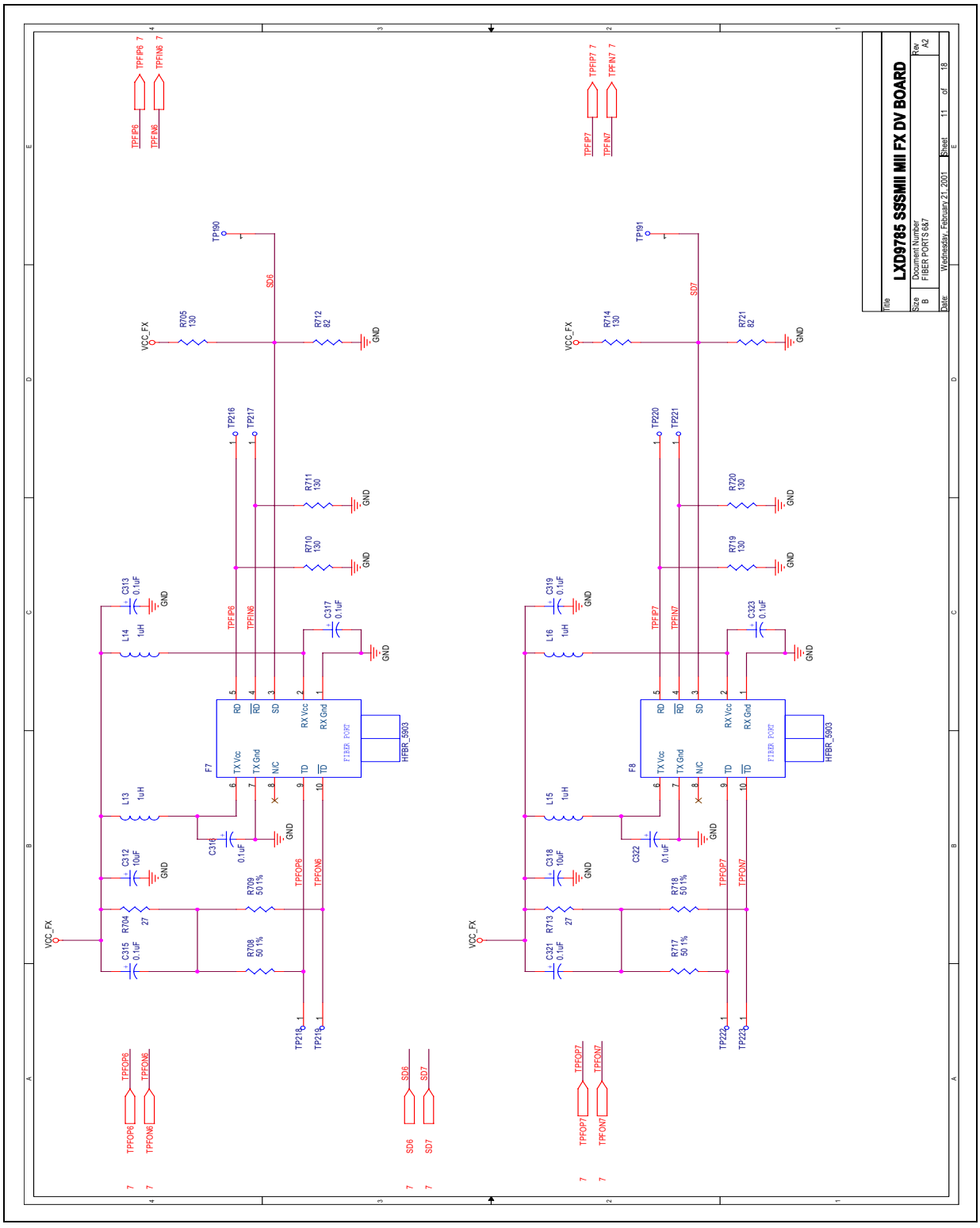


Figure 14. Caps

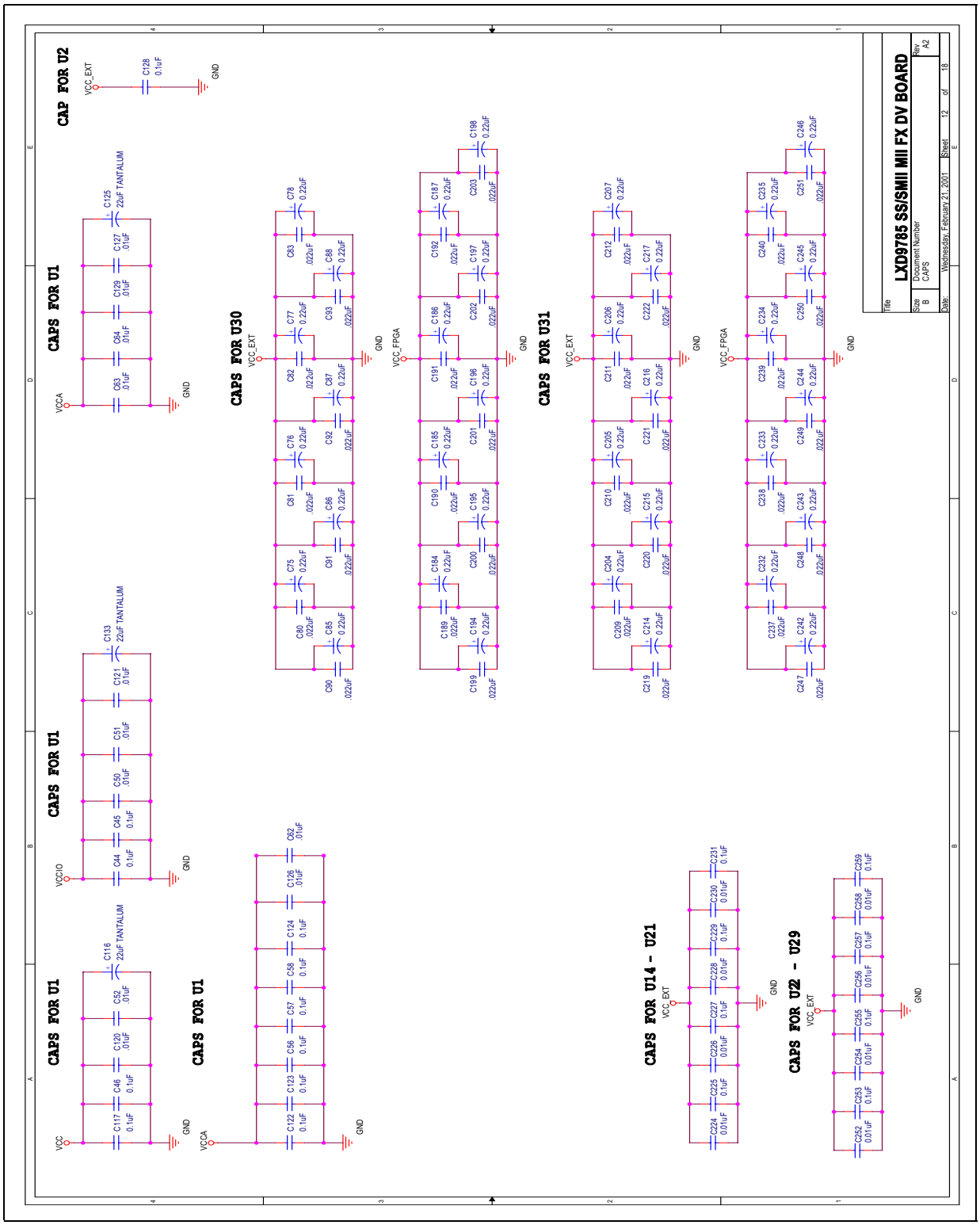


Figure 15. SS-SMII to MII ALTERA

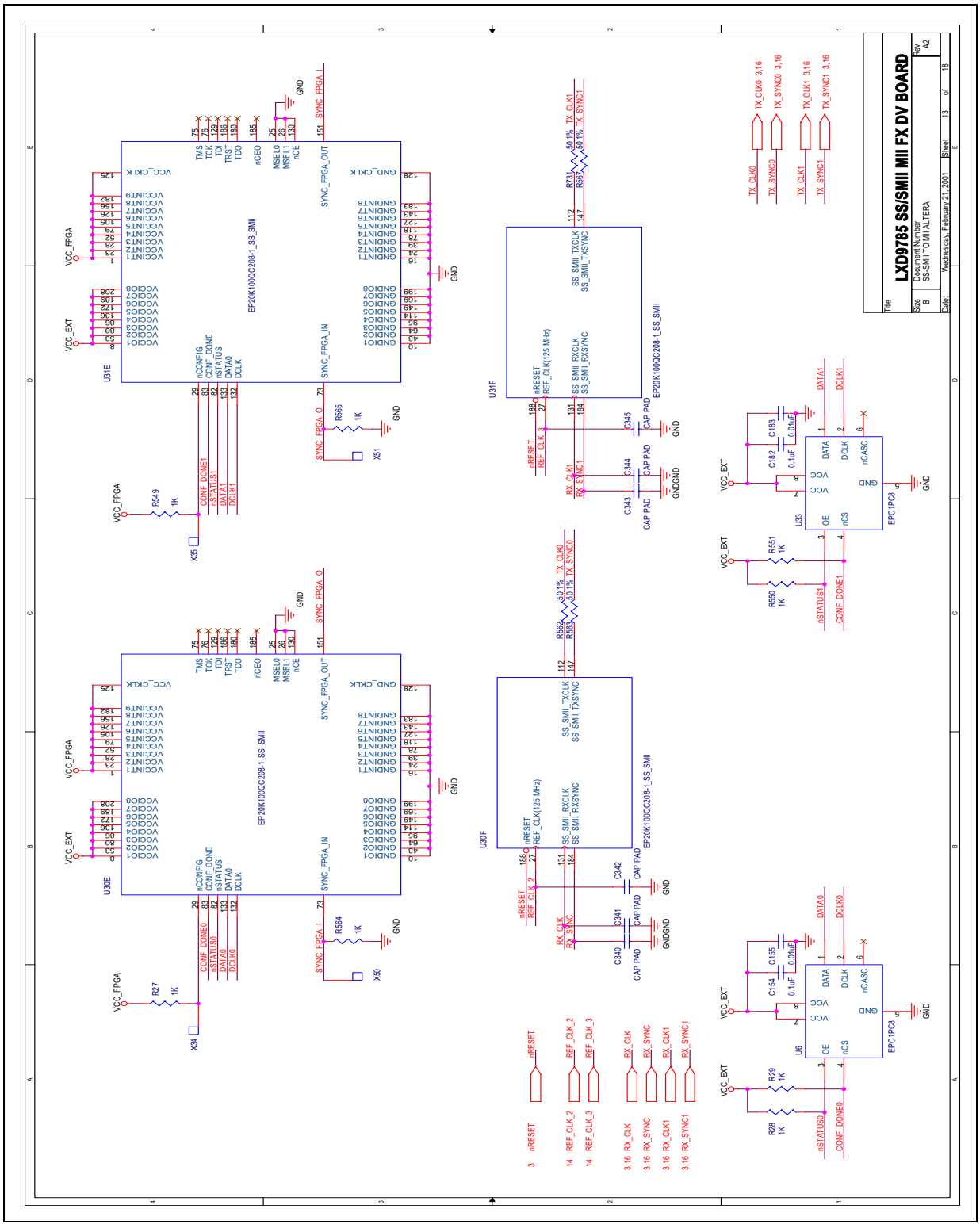


Figure 16. Clock Distribution

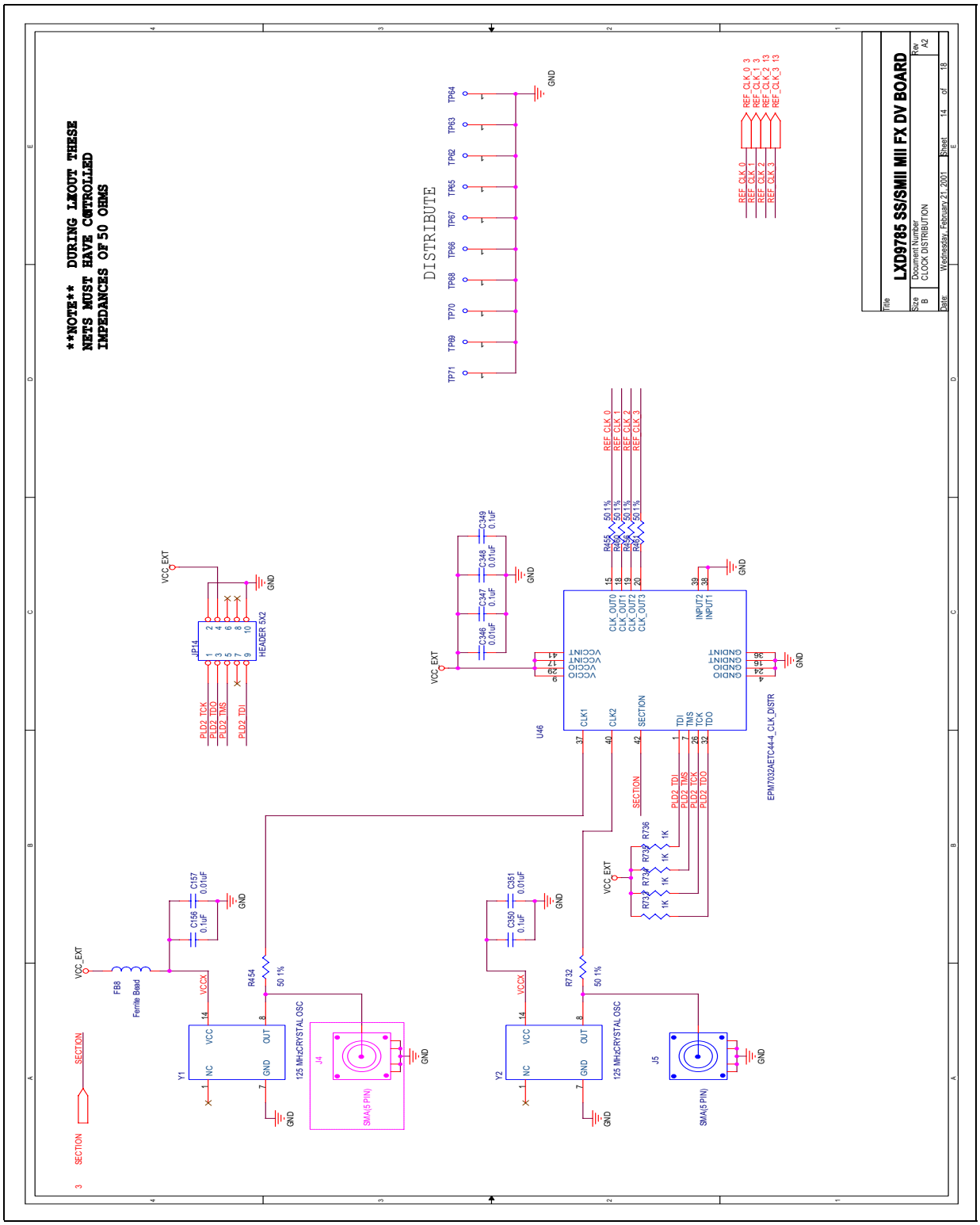


Figure 17. Inter-Frame Status LEDs

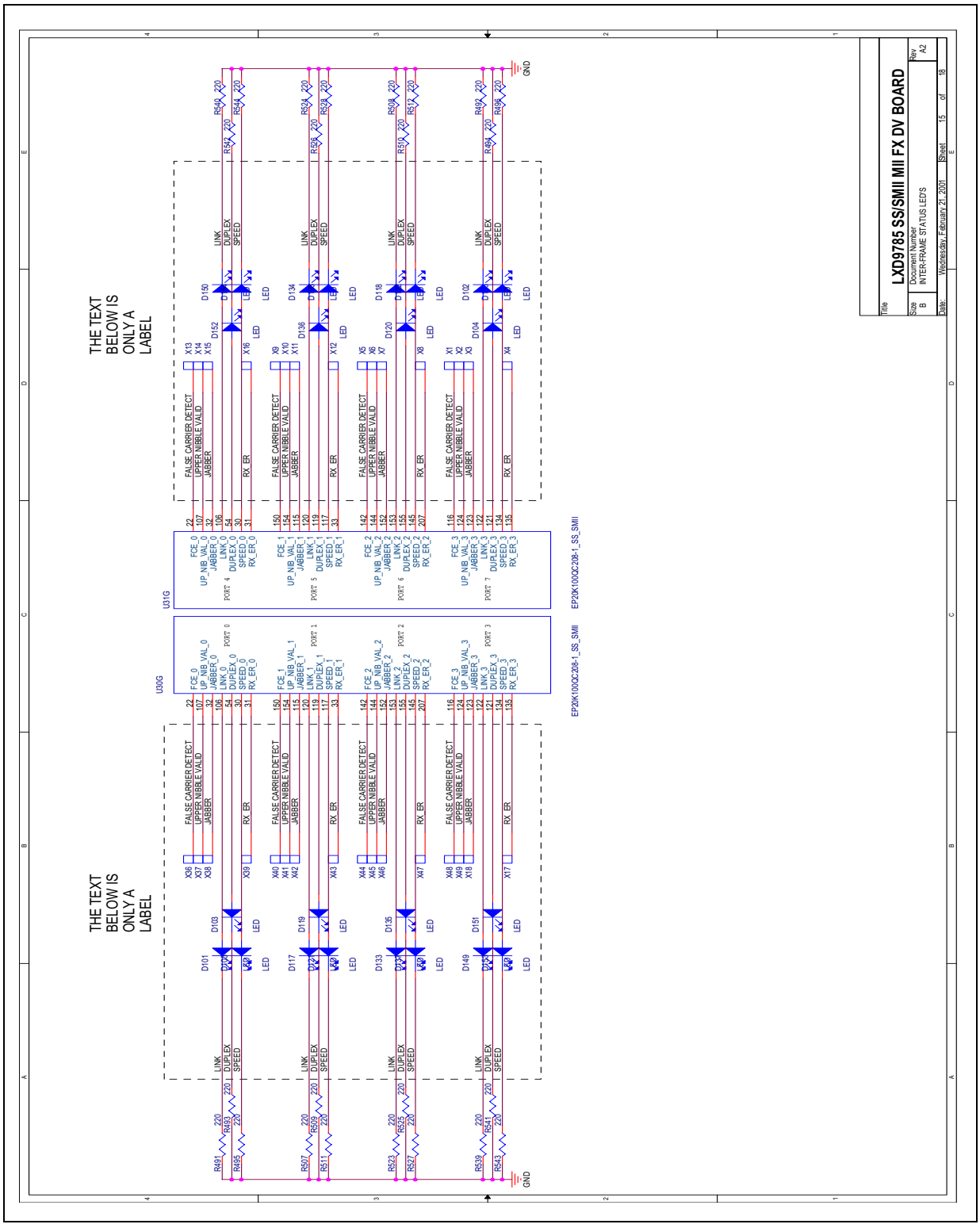


Figure 18. Logic Analyzer

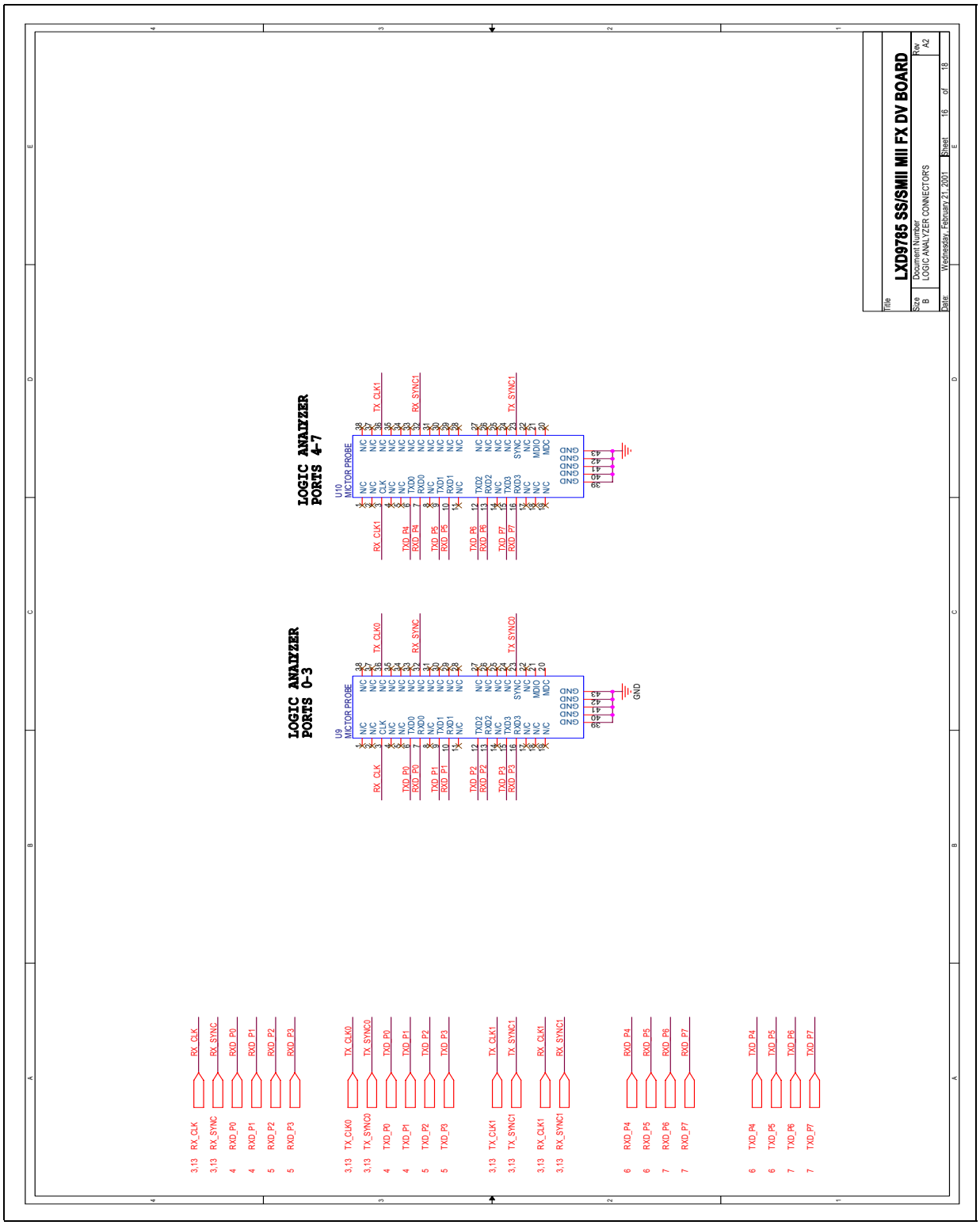


Figure 19. MDIO0 and MDC0 Fix

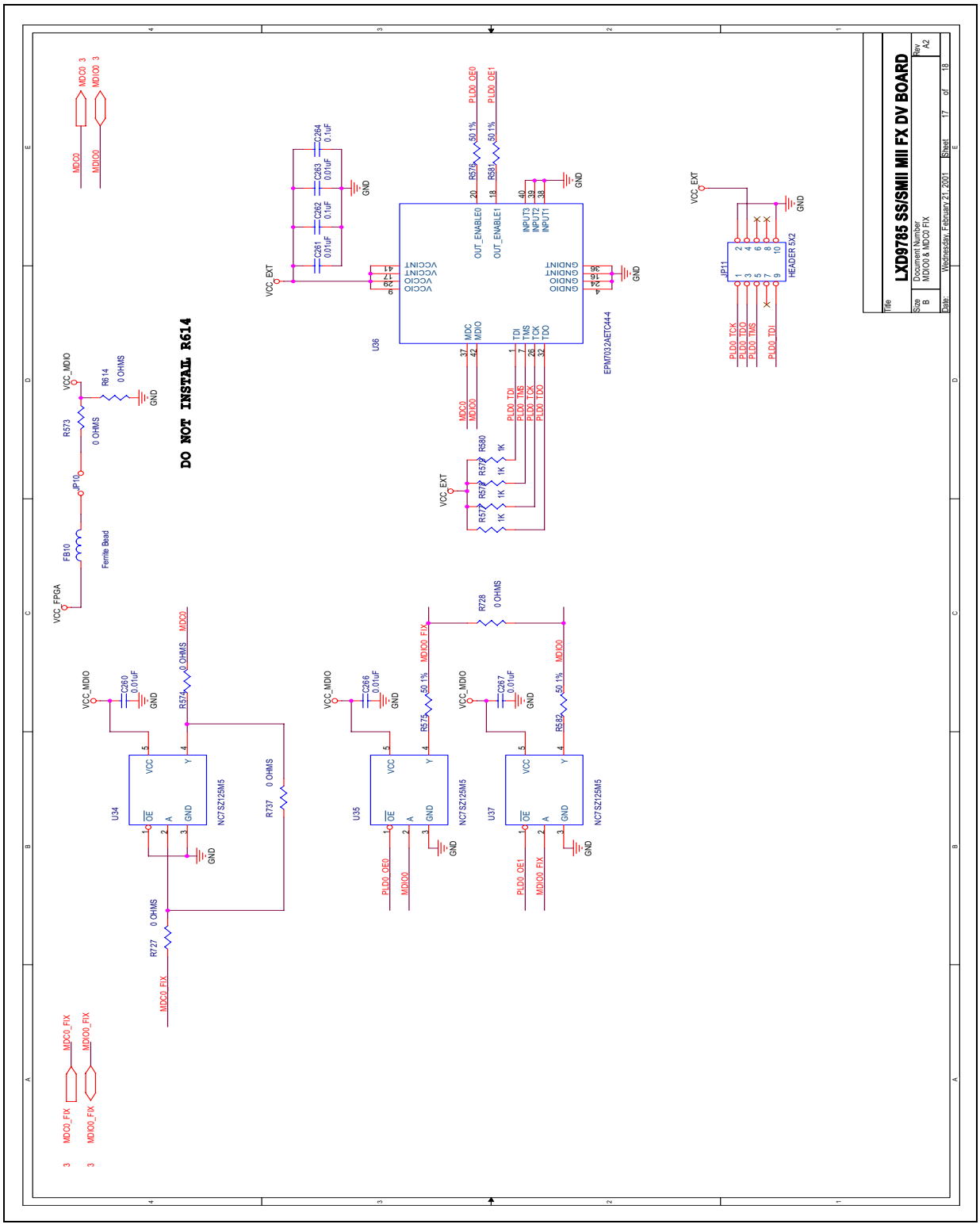
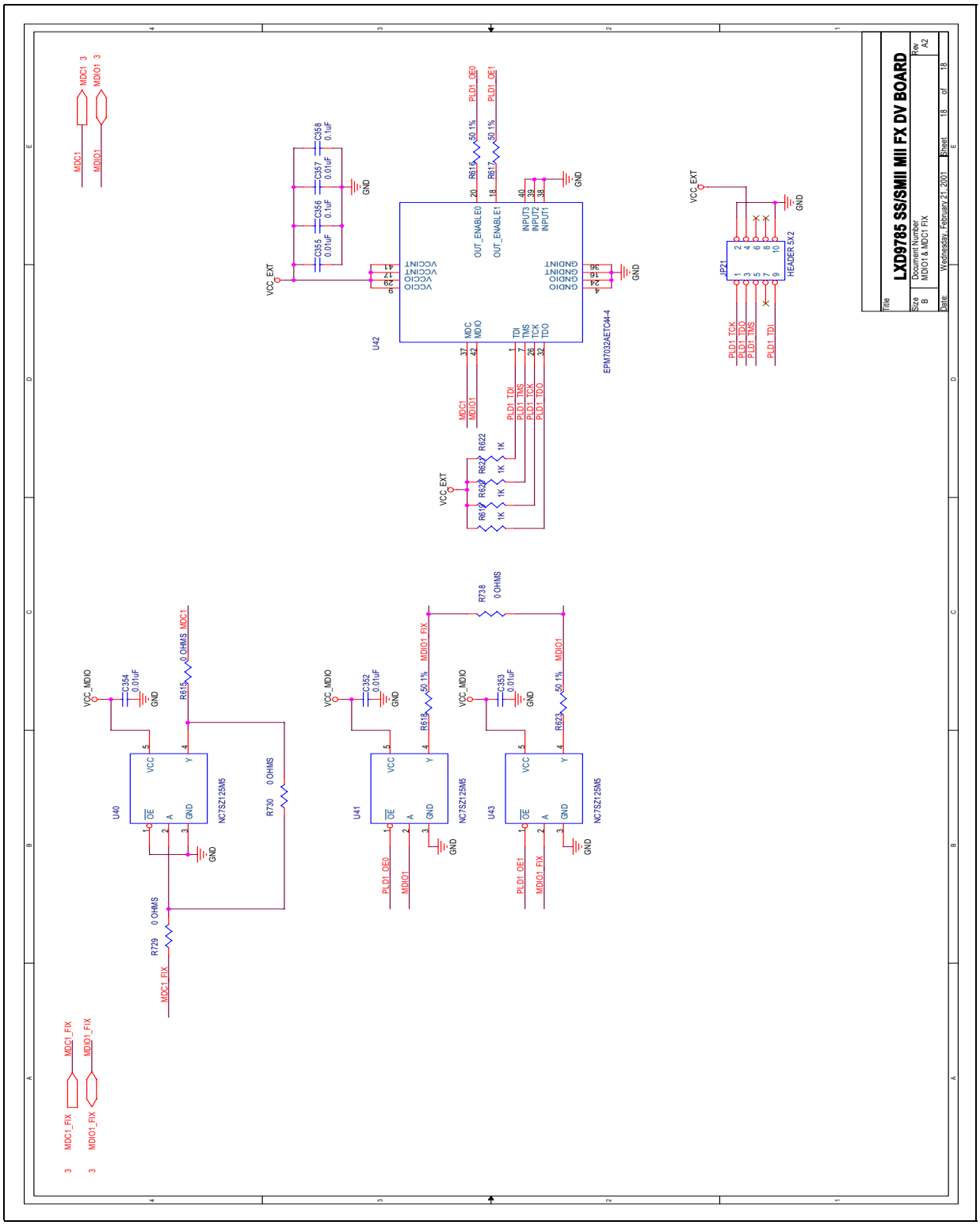


Figure 20. MDIO1 and MDC1 Fix



7.0 Bill of Materials

Table 10. LXD9785 Bill of Materials (Fiber - SS-SMII)

Reference Designator	Description	Manufacturer	Part Number
BN1-5	CONN BANANA NUT SILVER	EF JOHNSON	108-0740-001
C1-4, 8, 11, 136, 178, 270, 276, 282, 288, 294, 300, 306, 312, 318	CAP 10UF 20V TANT (CASEC)	PANASONIC	ECS-T1DC106R
C5, 15, 19, 44-46, 56, 57, 58, 117, 122-124, 128, 140, 154, 156, 182, 225, 227, 229, 231, 253, 255, 257, 259, 274, 277, 279-281, 283, 285-287, 289, 291-293, 295, 297-299, 301, 303-305, 307, 309-311, 313, 315-317, 319, 321-323, 347, 349, 350, 362, (DO NOT INSTALL C262, 264, 356, 358)	CAP 0.1UF 16V CER X7R (0805)	PANASONIC	ECJ-2VB1C104K
C9, 12, 137, 179, 271	CAP 100UF 16V MIN ELECT (TH)	PANASONIC	ECE-A1CKA101
C10, 13, 138, 180, 272	CAP 1.0UF 25V TANT (CASEA)	PANASONIC	ECS-T1EY105R
C14, 16-18, 139, 141, 181, 273, 275	CAP 0.001UF 50V 5% CER (0805)	PANASONIC	ECU-V1H102JCX
C50-52, 62-64, 120, 121, 126, 127, 129, 155, 157, 183, 224, 226, 228, 230, 252, 254, 256, 258, 346, 348, 351 (DO NOT INSTALL C260, 261, 263, 266, 267, 352-355, 357)	CAP 0.01UF 50V 10% CER (0805)	PANASONIC	ECU-V1H103KBG
C75-78, 85-88, 184-187, 194-198, 204-207, 214-217, 232-235, 242-246	CAP 0.22UF 35V TANT TE SERIES (CASEA)	PANASONIC	ECS-T1VY224R
C80-83, 90-93, 189-192, 199-203, 209-212, 219-222, 237-240, 247-251	CAP .022UF 50V CER (0805) SMD	PANASONIC	ECU-V1H223KBX
C116, 125, 133	CAP 22UF TANT (CASEC)	AVX	TAJC226M010R
D1, 93	LED RED SS TYPE LOW CUR SMD	PANASONIC	LNJ208R8ARA
D2	DIODE, LL4148 SMD ( )	DIODES, INC.	LL4148
D3, 4, 94, 157	TVS GULLWING 600W 5V UNI-DIR SMD	GENERAL SEMICONDUCTOR	SMBG5.0A
D5-28, 101-106, 117-122, 133-138, 149-156	LED, GREEN SS TYPE LOW CUR SMD	PANASONIC	LNJ308G8LRA
F1-8 (DO NOT INSTALL)	IC INTERFACE HFBR_5903 3.3V FIBER TRANSCEIVER ( )	HP	HFBR_5903 FIBER PORT
FB1, 5, 8 (DO NOT INSTALL FB10)	FBEAD REPL/ CT50ACC-322513T	CENTRAL TECHNOLOGY	CTCB1210-600-HC

Table 10. LXD9785 Bill of Materials (Fiber - SS-SMII) (Continued)

Reference Designator	Description	Manufacturer	Part Number
FB2-4, 6, 11	FERRITE BEAD	FAIR-RITE	2961666671
J2, 3	CONN MOD JACK 6-6 RJ11 UNSHIELDED BLOCK	CORCOM	RJ11-6L-B
J4, 5 (DO NOT INSTALL)	CONN SMA COAXIAL JACK	AMPHENOL	901-144
JP1, 2, 4, 5, 15, 16	HEADER 3X1	BERG	68000-240-3
JP3	HEADER 4X2	BERG	C9192-280-4
JP12, 19, 20 (DO NOT INSTALL JP10)	HEADER 2X1 (2 PIN)	BERG	68000-240-2
JP14 (DO NOT INSTALL JP11, 21)	HEADER 5X2	BERG	C9192-280-5
L1-16	INDUCTOR 1UH SMD (1206)	TDK#TDKMLF3216 A1R0KT	TDKMLF3216A1R0K T000
P1-8	CONN MII 40 PIN FEMALE	AMP	787171-4
R3-10, 14-22, 24-26, 725, 726	RES 4.75K 1/10W 1% (0805)	POPPY	POP 0805 4.75K OHM - 1%
R11	RES 100 OHM 1/ 10W 1% (0805) SMD	PANASONIC	ERJ-6ENF1000V
R12, 116-139, 491-496, 507-512, 523-528, 539-544	RES 221 OHM 1/ 10W 1% (0805) SMD	POPPY	POP 0805 221 OHM -1%
R23	RES 10K OHM 1/ 10W 1% (0805) SMD	PANASONIC	ERJ-6ENF1002V
R27-29, 549-551, 564, 565, 733-736 (DO NOT INSTALL R577-580, 619-622)	RES 1K OHM 1/ 10W 1% (0805) SMD	PANASONIC	ERA-67EB102V
R207-415, 417, 419, 421, 423, 425, 427, 429, 454-456, 460, 461, 562, 563, 567, 586-609, 626-649, 654, 655, 663, 664, 672, 673, 681, 682, 690, 691, 699, 700, 708, 709, 717, 718, 731, 732 (DO NOT INSTALL R575, 576, 581, 582, 616-618, 623)	RES 49.9 OHM 1/ 10W 1% (0805) SMD	POPPY	POP 0805 49.9 OHM -1%
R416, 418, 420, 422, 424, 426, 428, 430, 558, 559	RES 45.3 OHM 1/ 10W 1% (0805) SMD	PANASONIC	ERJ-6ENF45R3V
R568, 569	RES 30.1 OHM 1/ 10W 1% (0805) SMD	PANASONIC	ERJ-6ENF30R1V
R574, 615, 727-730, 737, 738 (DON'T INSTALL 573, 614)	RES 0 OHM 1/10W 5% (0805) SMD	PANASONIC	ERJ-6GEY0R00V
R650, 659, 668, 677, 686, 695, 704, 713	RES 27.4 OHM 1% 1/10W (0805) SMD	PANASONIC	ERJ-6ENF27R4V

Table 10. LXD9785 Bill of Materials (Fiber - SS-SMII) (Continued)

Reference Designator	Description	Manufacturer	Part Number
R651, 656, 657, 660, 665, 666, 669, 674, 675, 678, 683, 684, 687, 692, 693, 696, 701, 702, 705, 710, 711, 714, 719, 720	RES 130 OHM 1/ 10W 1% (0805) SMD	PANASONIC	ERJ-6ENF1300V
R658, 667, 676, 685, 694, 703, 712, 721	RES 82.5 OHM 1/ 10W 1% (0805)	PANASONIC	ERJ-6ENF82R5V
S1	SWITCH DIP 5 POS TOP SLIDE	C & K COMPONENTS	BD05
S4	SWITCH PB SPDT TINY RT-ANGLE	C & K COMPONENTS	TP12SH8AQE
S5	SWITCH DIP 4 POS TOP SLIDE	C & K COMPONENTS	BD04
S8	SWITCH DIP 6 POS TOP SLIDE	C & K COMPONENTS	BD06
TP1, 2, 5, 13-61, 104-182, 184-223	HEADER 1X1	BERG	68000-240-1
TP62-71	TESTPOINT COLOR CODED BLACK	KEYSTONE	5011
U1 (DO NOT INSTALL)	IC PHY LXT9785/ 9785E 208 PIN QFP (QFP208)	INTEL PART	LXT9785/9785E
SOCKET FOR U1	SOCKET 208 PIN 0.5MM PITCH SMT	YAMAICHI	IC149-208-061-S5
U2	IC LOGIC 74HC14 HEX INVERT TRIGGER 14 PIN SO	FAIRCHILD	MM74HC14M
U6, 33	IC MEM PROM EPC1 ALTERA 8 PIN DIP (DIP8)	ALTERA	EPC1PC8
SOCKET FOR U6, 33	SOCKET 8 PIN DIP GOLD	MILL -- MAX MANUFACTURING CORP	110-93-308-41-001
U9, 10	CONN 38 PIN MICTOR PLUG CONNECTOR ( )	AMP	2-767004-2
LATCH HOUSING FOR U9, 10	MISC LATCH HOUSING FOR MICTOR RECPT	PRECISION INTERCONNECT	105-1089-00
U14-29	IC LOGIC 74LVC244 LOW VOLTAGE BUFFER 20 PIN SOIC	TEXAS INSTRUMENTS	SN74LVC244ADW
U30, 31	IC FPGA 20K100 2.5V 208 PIN TQFP ( )	ALTERA	EP20K100QC208-1
U32	REG SC1566 2.5V 3A LOW DROPOUT 3 PIN TO-263	SEMTECH	SC1566CM-2.5

Table 10. LXD9785 Bill of Materials (Fiber - SS-SMII) (Continued)

Reference Designator	Description	Manufacturer	Part Number
(DO NOT INSTALL U34, 35, 37, 40, 41, 43)	IC LOGIC NC7SZ125 SINGLE TRISTATE BUFFER SOT23	FAIRCHILD SEMICONDUCTOR	NC7SZ125M5
U46 (DO NOT INSTALL U36, 42)	IC FPGA 7032A 3.3V PROGRAMMABLE PLD 44 PIN TQFP	ALTERA	EPM7032AETC44-4
Y1, 2 (DO NOT INSTALL)	OSC 125.000MHZ 25PPM 3.3V	SARONIX	SCS-LO-1067