Intel® IQ31244 Customer Reference Board

User's Manual

April 2004

Order Number: 252933-001

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Revision History

Date	Revision	Description
April 2004	001	Initial release

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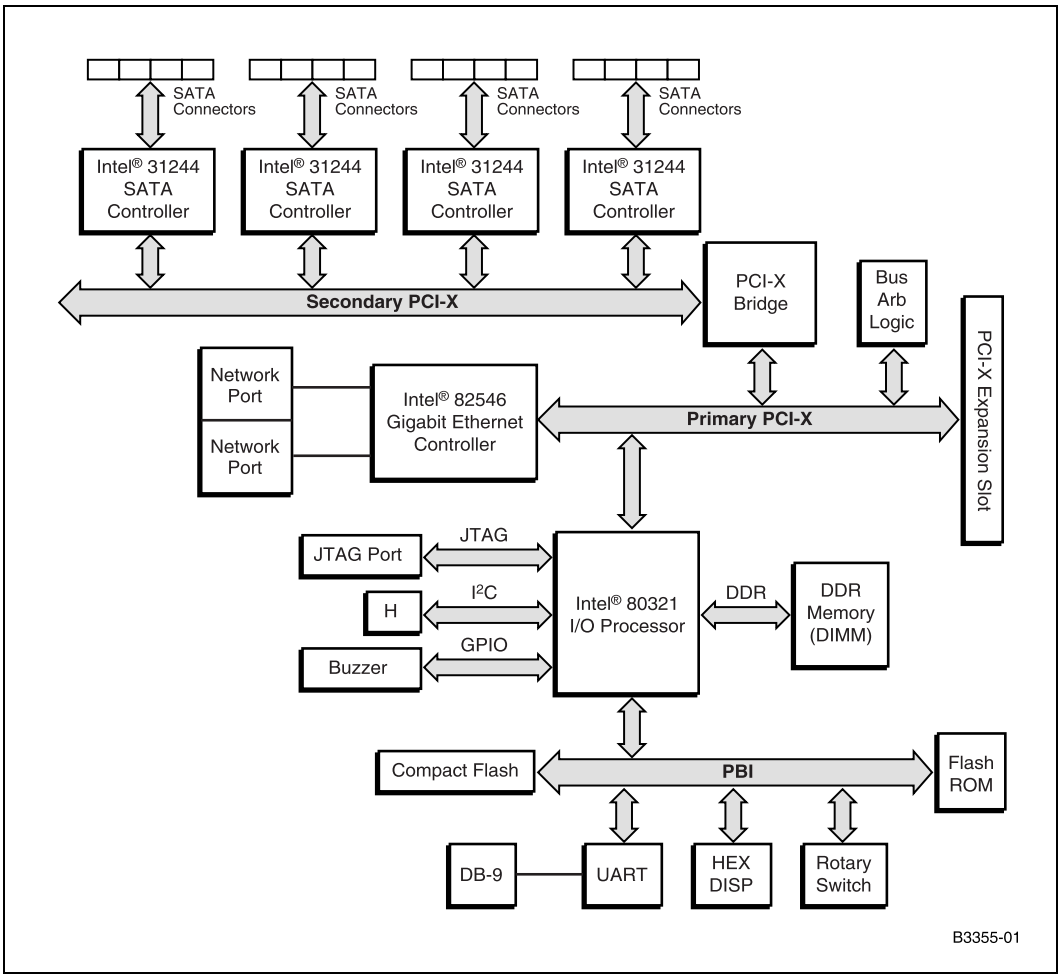
1.0 Introduction

The Intel® IQ31244 Customer Reference Board (hereafter called “IQ31244”) is a FlexATX motherboard based on the Intel® 80321 I/O Processor. The Intel® third-party part number for this motherboard is MB-701.

This platform is capable of operating at a maximum of 100 MHz PCI-X on both the secondary and primary PCI buses (refer to Figure 1). The IQ31244 features Intel® 31244 PCI-X to Serial ATA Controllers on the secondary side of an Intel® 31154 133 MHz PCI Bridge. The IQ31244 also includes an Intel® 82546 Dual-Port Gigabit Ethernet Controller, a 64-bit PCI-X expansion slot, and various features on the 80321 peripheral bus interface (PBI). The Intel® 31154 133 MHz PCI Bridge provides a PCI-X bridge, which allows direct peer-to-peer communication between the processor and the four 31244 PCI-X to Serial ATA Controllers on the secondary PCI-X 64-bit bus with frequency of 100 MHz. The IQ31244 provides sixteen Serial ATA connectors, since each Serial ATA has four SATA channels. The Intel® 82546EB Dual-Port Gigabit Ethernet Controller interface has two network ports. The Intel® 80321 I/O Processor also provides the DDR SDRAM memory controller. The IQ31244 processor peripheral bus interface operates at a frequency of 33 MHz frequency with flash ROM, CompactFlash*, UART, Hex Display LEDs, and rotary switch.

A block diagram of IQ31244 is shown in Figure 1.

Figure 1. Intel® IQ31244 Customer Reference Board Block Diagram



1.1 Features

The features of the IQ31244 are described in Table 1.

Table 1. Features and Descriptions

Feature	Description
Processor	• Intel® 80321 I/O Processor
Primary PCI	Options for the clock on 64-bit bus: • 100 MHz PCI-X • 66 MHz PCI-X • 66 MHz conventional PCI
Ethernet Ports	• Two RJ45 shielded magnetic LED gigabit connectors • Gigabit Ethernet debugging/download ports (using Intel® 82546EB Dual-Port Gigabit Ethernet Controller)
PCI Slot	• 64-bit PCI-X expansion connector
PCI-X Bridge	• Intel® 31154 133 MHz PCI Bridge
Secondary PCI	• 64-bit 100 MHz PCI-X bus • Four Intel® 31244 PCI-X to Serial ATA Controllers
Serial ATA	• Sixteen SATA connectors • Four Intel® 31244 PCI-X to Serial ATA Controllers
Flash ROM	• 8 MB Flash ROM 3.3 V—16-bit Flash
CompactFlash*	• 16-bit CompactFlash* PC Card Memory Mode
Form Factor	• FlexATX form factor in ATX chassis with 300 W power supply
General-Purpose I/O	• Eight GPIO pins
Hex Display	• Two 7-segment Hex LED displays
Rotary Switch	• Rotary/hex switch
RTC and NVRAM Supervisor	• Microprocessor power-on reset with watchdog timer and real-time clock
Buzzer	• 85 dB • Frequency 2300 Hz
JTAG Port	• ARM*-compliant JTAG 20-pin header
Memory	• PC 1600 Double Data Rate (DDR) SDRAM (100 MHz clock rate) • 256 MB 64-bit (expandable)
Onboard Power	• Board sources +3.3 V, +5 V, +12 V, and -12 V from ATX power supply. • Cores require +1.3 V, +1.5 V, and +2.5 V.
Power LED	• “Power On” (green) LED indicator
SATA LEDs	• 2-pin header for each SATA channel
Temperature Sensor	• 2-wire serial temperature sensor
Serial Port	• One serial console port (16C550-compatible)
Chassis	• ATX desktop enclosure with 300 W power supply

1.2 Electrical Specifications

The electrical specifications of the IQ31244 are given in Table 2.

Table 2. Intel® IQ31244 Customer Reference Board Power Requirements

Voltage	Current (Typical)	Current (Maximum)
+3.3 V	3.19 Amps	4.56 Amps
+5 V	1.6 mAmps	2.28 mAmps
+12 V	0.0 Amps	0.0 Amps
-12 V	0.0 Amps	0.0 Amps

Most ATX power-supply units (PSUs) regulate off the 5 V signal. When no devices are drawing from the 5 V supply, the ATX PSU does not supply 3.3 V correctly to the motherboard. To compensate for this, it is recommended that a load (for example, an SATA hard drive) be added on the 5 V rail from the PSU.

Note: The included 300 W power supply is sufficient to power up to four drives at one time. An additional power supply is required to provide power for more than four drives. To estimate the required power supply, estimate that each SATA drive draws approximately 2.8 A on the 12 V supply.

1.2.1 SATA Drive Enclosures

It is highly recommended that the SATA drives are housed in an enclosure to reduce the environmental noise that can affect performance. An example of a SATA four-drive enclosure is the DE400 model from Storcase*:

http://www.storcase.com/dataexpress/datasheet/dexpress_de400.pdf.

1.3 Environmental Specifications

Table 3. Environmental Specifications

Characteristic	Range
Operating temperatures	0–55 °C
Relative humidity (non-condensing)	0–95%
Storage temperatures	-55–125 °C

Note: A small amount of airflow is required to prevent the IQ31244 operating temperature from exceeding 55 °C. When the ATX chassis cover is removed, an external fan is required to provide adequate air flow within the chassis.

1.4 Physical Characteristics

Table 4 provides the physical characteristics of the IQ31244.

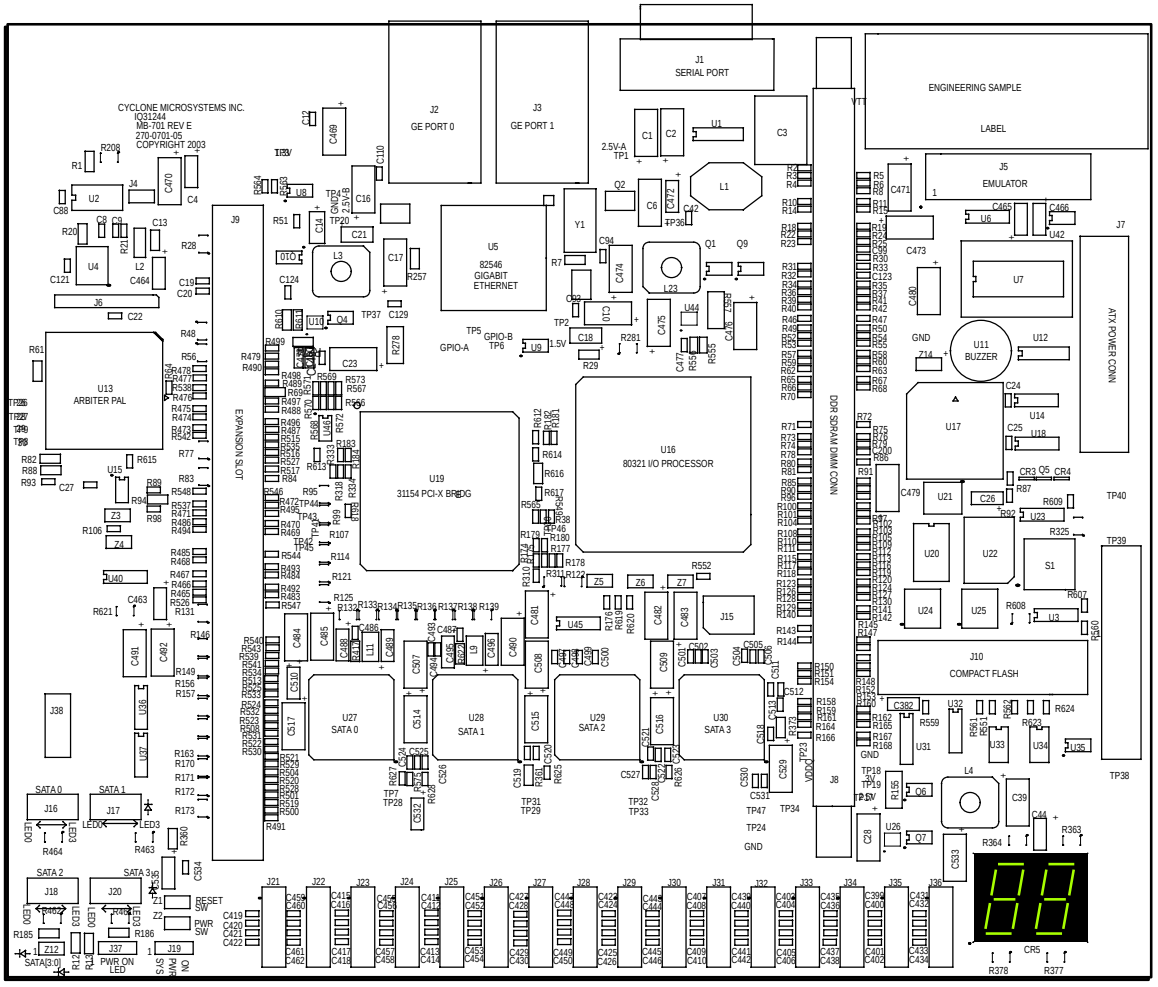
Table 4. Physical Characteristics

Characteristic	Description
Dimensions (width × height)	9.0" × 7.5" (228.6 mm × 190.5 mm)
Form factor	FlexATX
Expansion card slot	PCI expansion slot **NOTE:** Use only PCI-X expansion cards.
Power supply connector	ATX (Molex* 39-29-9202 or equivalent)

1.5 Physical Configuration

Figure 2 (not to scale) shows the location of jumpers, connectors, and ICs on the IQ31244 motherboard. Refer to this figure when component locations are referenced later in the manual.

Figure 2. Component Layout Diagram (not to scale)



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1.6 Reference Information

Table 5 provides a list of reference information for the components used in this platform.

Table 5. Documents and Manufacturers

Document	Manufacturer
• *Intel® IQ31244 PCI-X Motherboard with Serial ATA Controllers and Ethernet Controller User's Manual* (252933) • *Intel® 80321 I/O Processor Developer's Manual* (273517) • *Intel® 80321 I/O Processor Datasheet* (273518) • *Intel® 80321 I/O Processor Design Guide* (273520) • *Intel® 31154 133 MHz PCI Bridge Datasheet* (278821) • *Intel® 31154 133 MHz PCI Bridge Developer's Manual* (278848) • *Intel® 31154 133 MHz PCI Bridge Specification Update* (300826) • *Intel® 31244 PCI-X to Serial ATA Controller Datasheet* (273595) • *Intel® 31244 PCI-X to Serial ATA Controller Design Guide* (273651) • *Intel® 31244 PCI-X to Serial ATA Controller Developer's Manual* (273603) • *Intel® 82546EB Dual-Port Gigabit Ethernet Controller Specification Rev. 1.1* (document under disclosure) • *Intel StrataFlash® 28F640J3A Flash ROM Datasheet* (290667)	Intel Corporation Literature Sales PO Box 5937, Denver, CO 80217-9808 (800) 548-4725 http://www.intel.com
• Texas Instruments* TL16C550 UART • Texas Instruments* TL7702B	Texas Instruments Literature Response Center P.O. Box 809066, Dallas, TX 75380-9066 (800) 477-8924 http://www.ti.com
Serial ATA Specification, Revision 1.0	Serial ATA Working Group http:\\www.serialata.org
Microchip Technology* Serial EEPROM-93LC46	Microchip Technology http://www.microchip.com
STMicroelectronics* NVRAM Supervisor-M41ST85W	STMicroelectronics http://www.st.com
National Semiconductor* LM75 Digital Temperature Sensor	National Semiconductor Corp. 1111 West Bardin Road, Arlington, TX 760017 (800) 272-9959 http://www.national.com
• *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a • *PCI Local Bus Specification*, Revision 2.2	PCI Special Interest Group 5440 SW Westgage Dr. Suite #217, Portland, OR 97221 (800) 433-5177 (503) 222-6190 (fax) http://www.pcisig.com/specifications
• *ATX Specification*, version 2.1 • *FlexATX Addendum to microATX Specification*, version 1.0	FormFactors.org http://www.formfactors.org/formfactor.asp
CF+ and CompactFlash Specification*, Revision 1.4	CompactFlash* Association P.O. Box 51537, Palo Alto, CA 94303 (650) 843-1220 (650) 493-1871 (fax) http://www.compactflash.org email: infoflash@compactflash.org

2.0 PCI-X Interface

The IQ31244 contains two 64-bit PCI-X buses. The primary PCI bus, clocked at up to 100 MHz, interfaces with the Intel® 80321 I/O Processor, the Intel® 82546 Dual-Port Gigabit Ethernet Controller, the Intel® 31154 133 MHz PCI Bridge, and the PCI-X expansion slot.

Note: The PCI-X expansion slot must be used for PCI-X cards only.

The secondary PCI bus, clocked at 100 MHz, provides the interface between the Intel® 31154 133 MHz PCI Bridge and the four Intel® 31244 PCI-X to Serial ATA Controllers.

In addition, the two buses can communicate with each other by means of the Intel® FW31154 133 MHz PCI-X Bridge. The primary bus and secondary bus can operate at different speeds and modes independently of each other. Depending on the peripheral add-in card capability, the primary bus can operate at either conventional PCI, PCI-X 66 MHz, or PCI-X 100 MHz. The mode of the IQ31244 primary bus can also be set by jumpers Z3 and Z4, as shown in Table 6.

Table 6. Primary PCI Bus

Type of PCI	Speed	Z4	Z3
PCI-X 100	100 MHz	Open	Open
PCI-X 66	66 MHz	Open	Closed
Conventional PCI	66 MHz	Closed	Open

2.1 PAL Arbitration Circuit

The IQ31244 provides a Programmable Analog Logic (PAL) arbitration circuit on the primary PCI-X bus. A rotating priority arbitration scheme with a host and three agents is used. The priority rotates as shown in Table 7. The arbiter evaluates all requests and grants the bus to the highest-priority requesting device. On reset, the host is granted the bus, and agent 0 (PCI-X bridge) has the next-highest priority.

Table 7. Rotation Scheme of the PAL Arbitration Circuit

Priority	Description
Host	Intel® 80321 I/O Processor
0	Intel® 31154 133 MHz PCI Bridge
1	Expansion slot
2	Intel® 82546 Dual-Port Gigabit Ethernet Controller

When an agent is “skipped”, priority is not returned to that agent until the next passing cycle. This means that the agent is dropped from the highest priority to the lowest priority.

The arbiter has a time-out feature that functions as follows. Any PCI master which has requested the bus, but has not started an access within 16 clocks of receiving a grant, is assumed to be broken and the grant is rescinded.

When the PCI bus arbiter receives a request for the bus and there are currently no active transactions on the bus, the arbiter immediately grants ownership to the requester.

When two or more requests are active, the bus is granted to the requester with the higher priority. This approach ensures that all requesters are able to gain access to the bus in a reasonable time and that a high-bandwidth PCI adapter cannot starve all other requesters off the bus. This arbitration scheme conforms to the fairness doctrine described in the *PCI Bus Specification*, Revision 2.2.

The arbiter also implements bus parking. After a transaction is complete, if there are no requests for the bus, the arbiter parks the bus at the last owner. When that device wishes to begin another PCI transaction, it may do so without first requesting the bus. When another device requests the bus, the arbiter can immediately remove bus ownership from the idle device where it is parked. After reset or power-up the PCI bus is parked at the host.

Highest arbitration priority is given to the host immediately succeeding the bus owner, active or parked. Bus ownership is passed to the host with the next-highest priority and with an active bus request.

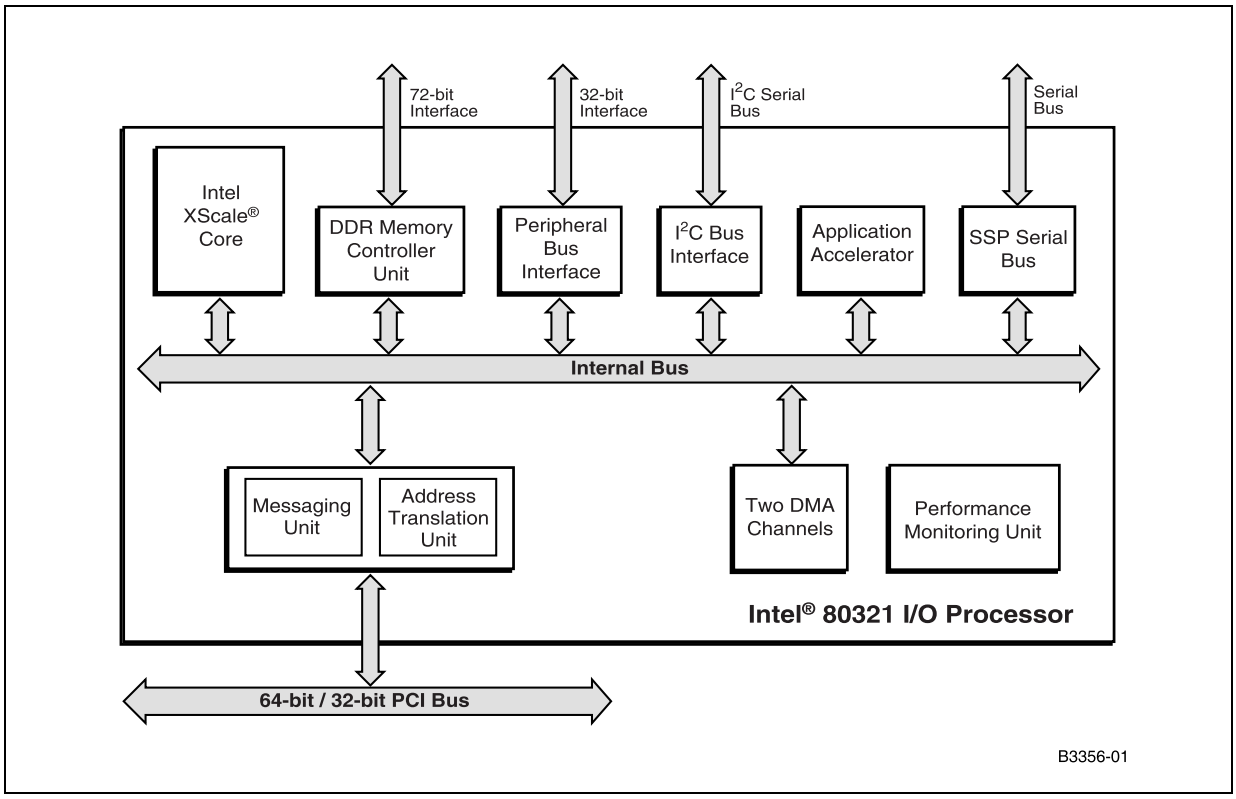
3.0 Intel® 80321 I/O Processor

The Intel® 80321 I/O Processor is based on the Intel XScale® micro-architecture core (compliant with ARM* architecture). The on-board 80321 processor supports 64-bit applications with operating frequency of up to 100 MHz. The processor operates in conventional PCI mode or in PCI-X mode as defined by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. The processor has the following features:

- Intel XScale® core
- PCI Local Memory Bus Address Translation Unit (ATU)
- Memory controller unit
- Peripheral Bus Interface (PBI)
- Application accelerator unit
- Two I^2C bus interface units
- Two DMA channels
- Performance monitoring unit
- Synchronous serial port unit
- Messaging unit
- Eight general-purpose I/O ports

The 80321 block diagram is shown in Figure 3.

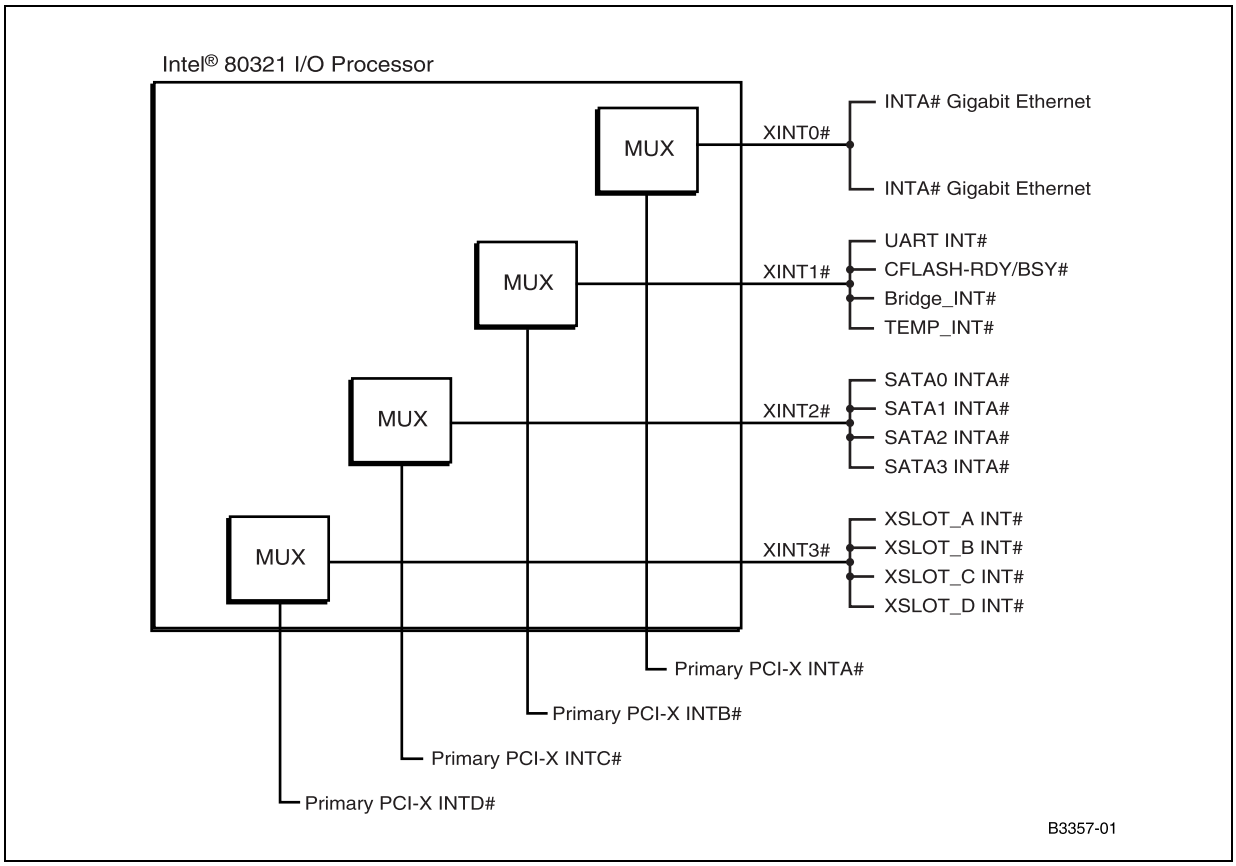
Figure 3. Intel® 80321 I/O Processor Block Diagram



3.1 Interrupts

The Intel® 80321 I/O Processor is built around an Intel XScale® core, which has four external interrupt lines designated XINT0# through XINT3#. In the 80321 processor, these interrupt lines are not directly connected to external interrupts, but pass through a layer of external interrupt routing logic. Figure 4 shows the interrupt connections on the processor.

Figure 4. Intel® 80321 I/O Processor Interrupt Connections



The external devices are AND-gated into designated interrupt signals. Therefore, the specific device that generates the interrupt cannot be detected. However, the eight GPIO pins of the Intel® 31154 133 MHz PCI Bridge are used to read interrupts from the specific device, as shown in Table 8.

Table 8. Intel® 31154 133 MHz PCI Bridge GPIO Pin Assignments

GPIO	Signal
7	SATA 3 Interrupt
6	SATA 2 Interrupt
5	SATA 1Interrupt
4	SATA 0 Interrupt
0	Expansion Slot INTB#

3.2 General-Purpose I/O Unit

The Intel® 80321 I/O Processor has eight general-purpose I/O GPIO[7:0] pins to control or monitor external devices in the I/O subsystem:

- The GPIO[0] and GPIO[1] signals are for CompactFlash* status.
- The GPIO[2] signal can be set to sound the buzzer. The buzzer can be disabled by adding a jumper onto Z14.
- The Flash ROM signal VPEN is assigned to GPIO[4] to allow software connection for code/data protection.
- The Flash ROM signal STS is assigned to GPIO[5] to allow interrupt input from the Flash ROM.
- The GPIO[6] and GPIO[7] signals are for the I^2C bus.

Table 9. GPIO Signal Definitions

GPIO	Signal
7	Port 0 SCL
6	Port 0 SDA
5	Port 1 SCL/Flash_VPEN
4	Port 1 SDA/Flash_STS
3	Watchdog Timer
2	Buzzer
1	Compact Flash Wait
0	Compact Flash Ready/Busy

3.3 I^2C Bus Units

The IQ31244 has two Inter-Integrated Circuit (I^2C) bus units. The first I^2C bus interfaces the Intel® 80321 I/O Processor with the other I^2C peripherals and microcontrollers for system management functions. Both buses allow the processor to serve as a master and slave device residing on the I^2C bus. The first I^2C has four components attached to the processor: the SDRAM EEPROM, the two temperature sensors, and the reset supervisor (with I^2C addresses as shown in Table 10). The second I^2C bus interface is through J15, a 4-pin header with pin 1 as SDA and pin 2 as SCL.

Table 10. I^2C Device Addresses

Designator	Device	Function	Address
J8	DDR SDRAM EEPROM DIMM	Memory configuration	1010 0000
U35	LM75	Temperature sensor	1001 000x
U8	LM75	Temperature sensor	1001 001x
U7	ST-M41ST85W	Reset supervisor	1101 000x

3.4 SDRAM EEPROM

The EEPROM located on the SDRAM module contains identification and configuration information. Start-up code must read this information on power-up and must properly configure the Intel XScale® processor to the SDRAM type.

3.5 Temperature Sensors

The National Semiconductor* LM75 temperature sensors have over-temperature trip points that trigger an interrupt when crossed. The sensors are placed on the board at U8 and U35. They share an interrupt line to the processor. Polling the two devices is required to determine which device triggered the interrupt. The sensors are placed in interrupt mode by the Breeze* initialization code (for more information, see the National Semiconductor website at http://www.national.com). The default over-temperature point is 80 °C. The sensors can be read for a temperature reading at any time. Reading after an interrupt clears the interrupt. The sensor does not interrupt again until the temperature drops below the hysteresis value (default is 75 °C) and rises again beyond the trip point. Consult the LM75 datasheet for more details on programming the temperature sensors.

3.6 Reset Supervisor

The STMicroelectronics* M41ST85W supervisor chip is connected to the Intel® 80321 I/O Processor through its I^2C bus interface. The supervisor controller uses a 512-bit, static CMOS SRAM organized as 64 words by 8 bits wide. This controller is driven by a 32.768 KHz clock. It features the time-of-day clock/calendar function, status/control of alarm, watchdog timer, and power-fail voltage monitoring (used by Ethernet LAN Power Good). The eight clock address locations contain the century, year, month, date, day, hour, minute, second, and tenths/hundredths of a second in 24-hour Binary Code Decimal (BCD) format. Corrections for 28-, 29- (leap year—valid until year 2100), 30- and 31-day months are made automatically.

The supervisor chip is supplied with a SNAPHAT package, which has a crystal and a battery for backup during power failures. The SNAPHAT comes in two battery sizes (48 or 120 mAh).

3.7 DDR SDRAM

The Intel® 80321 I/O Processor integrates a memory controller unit (MCU) to provide a direct interface between the processor and its local memory subsystem.The IQ31244 board is equipped with a 184-pin DIMM socket to accept a +2.5 V Double Data Rate (DDR) synchronous DRAM module with or without error correction code (ECC). This DDR SDRAM interface provides a direct connection to a reliable high-bandwidth memory subsystem. The socket accepts a 64- or 72-bit DDR SDRAM module with up to two 512 MByte banks for a maximum of 1 GByte. The SDRAM is accessible by the processor and the PCI bus by means of address translation by the memory management unit of the 80321.

3.7.1 Upgrading SDRAM

The IQ31244 board is equipped with unbuffered DDR SDRAM with ECC inserted in the 184-pin DIMM socket. The memory can be expanded by inserting a maximum-sized memory module of 1 Gbyte into the DIMM socket. The supported memory combinations are shown in Table 11.

Table 11. Supported SDRAM Configurations

Type	Size	Class	Total Memory Size
DDR 200	8M × 64 8M × 72	CL2	64 MBytes
		CL2 ECC	64 MBytes
	16M × 64 16M × 72	CL2	128 MBytes
		CL2 ECC	128 MBytes
	32M × 64	CL2	256 MBytes
	32M × 72	CL2 ECC	256 MBytes
	64M × 64	CL2	512 MBytes
	64M × 72	CL2 ECC	512 MBytes
	128M × 64	CL2	1 GByte
	128M × 72	CL2 ECC	1 GByte

3.7.2 Installation and Removal of Memory Modules

Installation and removal of DIMMs on the IQ31244 are simple procedures and require no special tools. Remove the adapter module from the motherboard before its memory configuration is changed. Take care to avoid static discharge while contacting the module or the motherboard. Wear a properly connected grounding strap while installing or removing memory modules on the IQ31244.

Align the key cut-outs of the module to the key pins of the DIMM socket. The memory module must be inserted vertically, and the latches on the socket must engage the mounting holes on the DIMM module. Be sure that the latches on both sides of the module are properly engaged.

4.0 Gigabit Ethernet Interface

The IQ31244 includes an Intel® 82546EB Dual-Port Gigabit Ethernet Controller on the primary PCI-X bus. Each port connector, J2 and J3, has a LINK indicator LED on the left side and a ACTIVITY indicator LED on the right side.

Table 12. Gigabit Ethernet Port Assignment

Pin	Symbol
1	T/R1ct
2	T/R1-
3	T/R1+
4	T/R2+
5	T/R2-
6	T/R2ct
7	T/R0ct
8	T/R0+
9	T/R0-
10	T/R3-
11	T/R3+
12	T/R3ct
13	LED1-
14	LED1+
15	LED2-
16	LED2+

4.1 Intel® 82546EB Dual-Port Gigabit Ethernet Controller

The Intel® 82546EB Dual-Port Gigabit Ethernet Controller is a single PCI device with two full Gigabit Ethernet MAC and PHY layer functions. It provides two standard IEEE 802.3 Ethernet interfaces with 1000Base-T, 100Base-TX, and 10Base-T applications. The controller manages dual MAC and PHY functions and directly interfaces with the PCI-X primary bus.

5.0 SATA Interface

On the IQ31244, the Intel® 31154 133 MHz PCI Bridge interfaces with four Intel® 31244 PCI-X to Serial ATA Controllers on the 64-bit data secondary PCI-X bus clocking at 100 MHz. The 31244 chip transmits and receives commands to one of the four Serial ATA channel with speeds of 1.5 Gb/s and 8b/10b encoded data. Each 31244 controller (U27–U30) has four channels. There is a total of sixteen SATA signal connectors (J21–J36) on the IQ31244 board. The IQ31244 is configured for Direct Port Access (DPA) mode to allow independent control of the SATA devices.

Table 13. SATA Port Assignment

SATA Controller	Port 0	Port 1	Port 2	Port 3	LED
U27	J24	J23	J22	J21	J16
U28	J28	J27	J26	J25	J17
U29	J32	J31	J30	J29	J18
U30	J36	J35	J34	J33	J20

Table 14. SATA Port Pin Assignment

Pin	Symbol
1	Ground
2	A+
3	A-
4	Ground
5	B-
6	B+
7	Ground

5.1 SATA JTAG Interface

The Intel® 31244 PCI-X to Serial ATA Controller JTAG interface is provided to assist on-board testing on one of the four 31244 devices. Table 15 shows the pin assignment of the 10-pin header for the JTAG (J38) on PCI-X to Serial ATA controller (U30).

Table 15. SATA JTAG Emulator Pin Assignment

Pin	Signal
1	TRST#
2	GND
3	TCK
4	GND
5	TMS
6	GND
7	TDI
8	GND
9	TDO
10	GND

5.2 Intel® 31244 PCI-X to Serial ATA Controller

Each of the 31244 chips transmits and receives commands to one of the four Serial ATA channels. Direct Port Access or DPA mode is hard-wired on each of the SATA controllers. DPA mode allows independent control of the SATA devices, allowing multiple disks to be accessed at the same time. Refer to the *Intel® 31244 PCI-X to Serial ATA Controller Developer's Manual* (273603) for more information.

Table 16. SATA Port Pin Assignment

Pin	Signal
1	Ground
2	A+
3	A–
4	Ground
5	B–
6	B+
7	Ground

5.3 Activity LEDs

The IQ31244 provides a group of four sets of headers for each SATA controller located on the bottom-left corner of the board. Each set of headers represents a cathode and anode of an LED for each port of the SATA controller. The SATA activity can be shown through a LED when it is connected to the headers. The activity of the SATA controller can displayed in two modes. In DPA mode, each port has its own LED signal. The group of headers (J16, J17, J18, and J20) are assigned to each SATA controller (U27, U28, U29, and U30). Z12 is the header for congregated SATA LED signals. Pin 1 is the cathode and pin 2 is the anode of the LED. The LED symbol is shown on the board.

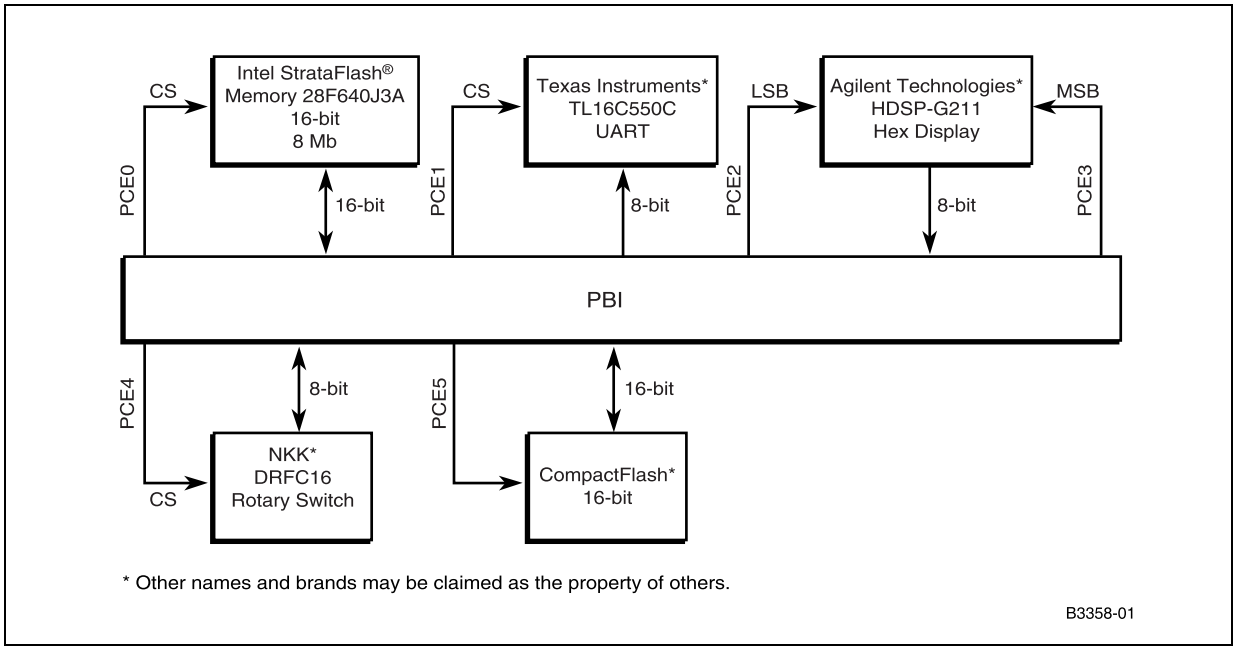
Table 17. SATA LED Header

Pin Cathode	Pin Anode	LED	Port
1	5	LED0	0
2	6	LED1	1
3	7	LED2	2
4	8	LED3	3

6.0 Peripheral Bus Interface Unit

The Peripheral Bus Interface (PBI) unit is a data-communication path to various components of the Intel® I/O processor hardware system that do not have PCI bus interfaces and do not optimally reside on the PCI bus. Since the peripheral bus has low bandwidth, the PBI incorporates a 1 KByte data queue to satisfy the 128 byte ADB requirement of the Intel® bus. The bus is selected to operate at 33 MHz. The PBI bus includes six chip enables. The PBI chip enables activate the appropriate peripheral device when the address falls within one of the six programmable address ranges. All six address ranges incorporate functionality that optimizes an interface for Flash Memory devices.

Figure 5. Peripheral Bus Interface Unit



6.1 Flash ROM

The IQ31244 provides 8 MBytes of sector-programmable Flash ROM for non-volatile code storage on the peripheral bus. The Flash ROM (designator U22) is an Intel® 28F640J3 type (or equivalent). On the IQ31244, the Flash ROM uses a 16-bit interface. The IQ31244 can be programmed using the JTAG emulator (J5).

6.2 CompactFlash*

The IQ31244 provides a vertical socket (J10) for a CompactFlash* Storage Card as additional flash memory storage. It is accessible by means of the 16-bit Peripheral Bus Interface (PBI). The CompactFlash Storage Card functions in PC Card ATA memory mode. For more details on the CompactFlash* functionality, refer to the CF+ section in the CompactFlash* specification, revision 1.4.

6.3 Console Serial Port

A single console serial port with a DB-9 line interface is included on the IQ31244. This port can be connected to a host system through the DB-9 connector from the rear I/O.

Table 18. Console Serial Port Connector

Pin	Signal	Description
1	N/C	Not used
2	RXD	Receive data
3	TXD	Transmit data
4	N/C	Not used
5	GND	Signal ground
6	N/C	Not used
7	RTS	Request to send
8	CTS	Clear to send
9	N/C	Not used

The serial port is based on a Texas Instruments* TL16C550 UART clocked at 1.843 Mhz. The device can be programmed to use this clock with the internal baud rate counters. The serial port can operate at speeds from 300 to 115,200 bps and can be operated in interrupt-driven or polled mode. For a detailed description of the registers and device operation, refer to the TL16C550 documentation (see Table 5, “Documents and Manufacturers” on page 13).

6.4 Rotary Switch

Table 19 describes the four-bit binary value generated by the rotary switch (S1).

Table 19. Read-Only Rotary Switch

Bit	Signal
0	A
1	B
2	C
3	D

6.5 JTAG Emulator Support

The IQ31244 provides a JTAG debugger interface at J5. This interface is compatible with the Wind River* visionPROBE*. The JTAG emulator interface connects primarily through the JTAG port of the Intel® 80321 I/O Processor and can assert a reset to the 80321. The JTAG emulator header definition (20-pin standard ARM* connector) is shown in Table 20.

Table 20. JTAG Emulator Pin Assignment

Signal	Pin	Pin	Signal
VTref	1	2	Vsupply
TRST#	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
GND	11	12	GND
TDO	13	14	GND
SRST#	15	16	GND
NC	17	18	GND
NC	19	20	GND

6.6 Hex Display

There are two seven-segment Hex LED displays (CR5). The two digits (MSB and LSB) utilize the peripheral bus, as shown in Figure 5, “Peripheral Bus Interface Unit” on page 26.

6.7 LEDs

The power-on LED can be plugged into J37 with pin 1 as the cathode and pin 3 as the anode.

7.0 ATX Power Connector

Table 21 shows the connector pinout for the main ATX power connector (J7). This header is implemented with a Molex* 39-29-9202 or equivalent. This power connector mates with a power supply connector, Molex 39-01-2200 or equivalent.

Table 21. ATX Power Connector (J1)

Pin	Signal
1	+3.3V
2	+3.3V
3	GND
4	+5V
5	GND
6	+5V
7	GND
8	PW-OK
9	5VSB
10	+12V
11	+3.3V
12	-12V
13	GND
14	PS-ON
15	GND
16	GND
17	GND
18	-5V
19	+5V
20	+5V

8.0 Jumpers

Table 22. Jumper Options

Designator	Type	Configure	Description
J4	2-pin post	Add shunt to enable	Enables spread-spectrum clocking on the primary PCI clocks.
J11, J12, J13, J14	3-pin post	Shunt on Pin 1 and pin 2 = DPA Mode Pin 2 and pin 3 = Master/Slave	SATA mode selection
J19	3-pin post	Shunt on Pin 1 and pin 2 = power by switch Pin 2 and pin 3 = auto power-on	System power by switch
J37	3-pin post	Pin 1 = Cathode Pin 3 = Anode	Power-on LED
J38	10-pin post	JTAG for U30 SATA controller	SATA controller JTAG
Z1	2-pin post	Chassis “RESET SW” cable	Power reset switch
Z2	2-pin post	Chassis “PWR SW” cable	Power switch
Z3	2-pin post	Open = 100 MHz Closed = 66 MHz	Primary clock
Z4	2-pin post	Open = PCI-X mode Closed = PCI mode	PCI-X mode
Z5	2-pin post	Add a shunt to the post	CompactFlash* to interrupt XINT1#
Z6	2-pin post	Add shunt to enable	PBI reset mode
Z7	2-pin post	Add shunt to enable	PBI retry mode
Z12	2-pin post	Add shunt to enable	Congregated LEDs
Z14	2-pin post	Add shunt to enable	Buzzer

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