Intel® 631xESB/632xESB I/O Controller Hub for Embedded Applications

Thermal and Mechanical Design Guidelines

February 2007

Order Number: 315263-001

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Revision History

Date	Revision	Description
February 2007	001	Initial public release.

1.0 Introduction

As the complexity of computer systems increases, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting, and/or passive heatsinks.

The goals of this document are to:

- Outline the thermal and mechanical operating limits and specifications for the Intel® 6321ESB I/O Controller Hub.
- Describe a reference thermal solution that meets the specification of Intel® 6321ESB I/O Controller Hub in Embedded applications.

Properly designed thermal solutions provide adequate cooling to maintain the Intel® 6321ESB I/O Controller Hub component die temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the Intel® 6321ESB I/O Controller Hub component die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the chipset. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

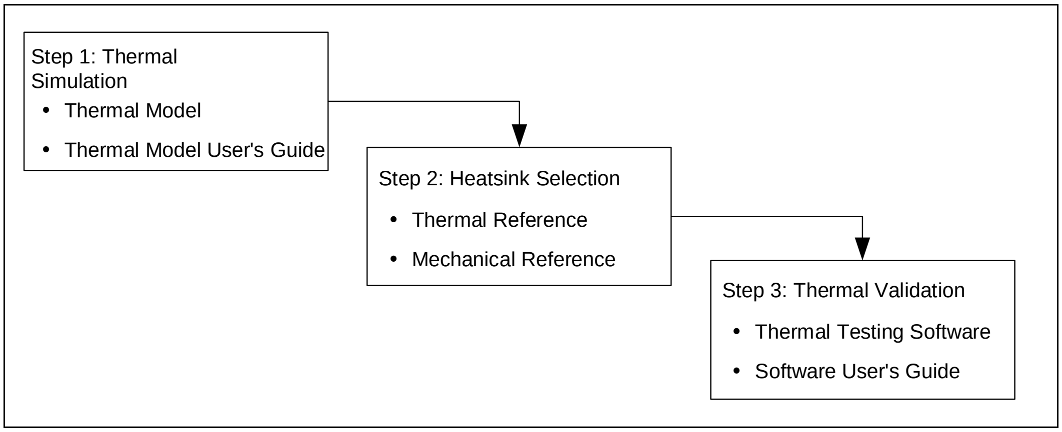
The simplest and most cost-effective method to improve the inherent system cooling characteristics is through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

This document addresses thermal design and specifications for the Intel® 6321ESB I/O Controller Hub component only. For thermal design information on other chipset components, refer to the respective component datasheet.

1.1 Design Flow

To develop a reliable, cost-effective thermal solution, several tools have been provided to the system designer. Figure 1 illustrates the design process implicit to this document and the tools appropriate for each step.

Figure 1. Thermal Design Process



1.2 Definition of Terms

Table 1. Definition of Terms

Term	Definition
BLT	Bond line thickness. Final settled thickness of the thermal interface material after installation of heatsink.
FCBGA	Flip Chip Ball Grid Array. A ball grid array packaging technology where the die is exposed on the package substrate.
Intel® 6321ESB I/O Controller Hub	The chipset component that integrates an Ultra ATA 100 controller, six Serial ATA host controller ports, one EHCI host controller supporting eight external USB 2.0 ports, LPC interface controller, flash BIOS interface controller, PCI/PCI-X interface controller, PCI Express interface, BMC controller, Azalia / AC'97 digital controller, integrated LAN controller, an ASF controller and a ESI for communication with the MCH.
LFM	Linear Feet Per Minute. A measure of airflow emitted from a forced convection device, such as an axial fan or blower.
MCH	Memory controller hub. The chipset component that contains the processor interface, the memory interface, and the South Bridge Interface.
Tcase-max	Maximum die temperature allowed. This temperature is measured at the geometric center of the top of the package die.
Tcase-min	Minimum die temperature allowed. This temperature is measured at the geometric center of the top of the package die.
TDP	Thermal Design Power. Thermal solutions should be designed to dissipate this target power level. TDP is not the maximum power that the chipset can dissipate.
Ψ_{CA}	Case-to-ambient thermal characterization parameter. A measure of the thermal solution thermal performance including the TIM using total package power. Defined as (TCASE – TLA) / Total Package Power. Note: Heat source must be specified when using Ψ calculations.
Ψ_{CS}	Case-to-Sink thermal characterization parameter. A measure of the thermal interface material performance using total package power. Defined as (TCASE - TSINK)/ Total Package Power. Note: Heat source must be specified when using Ψ calculations.
Ψ_{SA}	Sink-to-Ambient thermal characterization parameter. A measure of the heat sink performance using total package power. Defined as (TSINK - TLA)/Total Package Power. Note: Heat source must be specified when using Ψ calculations.

1.3 Reference Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents:

Table 2. Referenced Documents

Title	Location
Intel® 631xESB / 632xESB I/O Controller Hub Datasheet	http://www.intel.com/design/chipsets/datashts/313082.htm
Intel® 631xESB / 632xESB I/O Controller Hub Specification Update	http://www.intel.com/design/chipsets/specupdt/313075.htm
Intel® 631xESB/632xESB I/O Controller Hub Thermal/Mechanical Design Guide	Reference# 31307301
Intel® 6700PXH 64-bit PCI Hub/6702PXH 64-bit PCI Hub (PXH/PXH-V) Thermal Mechanical Design Guidelines	http://www.intel.com/design/chipsets/designex/302817.htm
Intel® 6700PXH 64-bit PCI Hub (PXH) Datasheet	http://www.intel.com/design/chipsets/datashts/302628.htm
BGA/OLGA Assembly Development Guide	
Various system thermal design suggestions	http://www.formfactors.org

1. Unless otherwise specified, these documents are available through your Intel field sales representative. Some documents may not be available at this time.

2.0 Packaging Technology

The Intel® 6321ESB I/O Controller Hub component uses a 40 mm x 40 mm, 10-layer FC-BGA3 package (see Figure 2 and Figure 3).

Figure 2. Intel® 6321ESB I/O Controller Hub Package Dimensions (Top View)

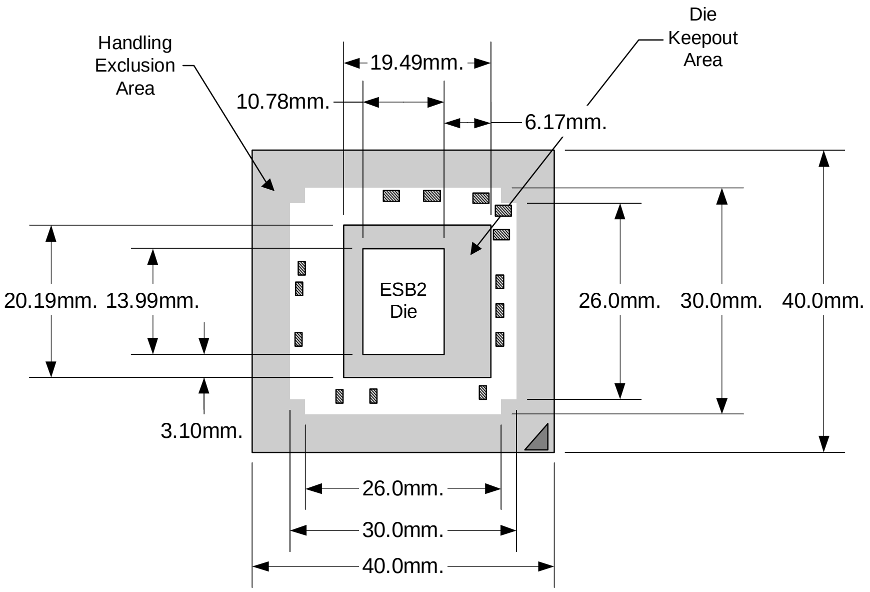
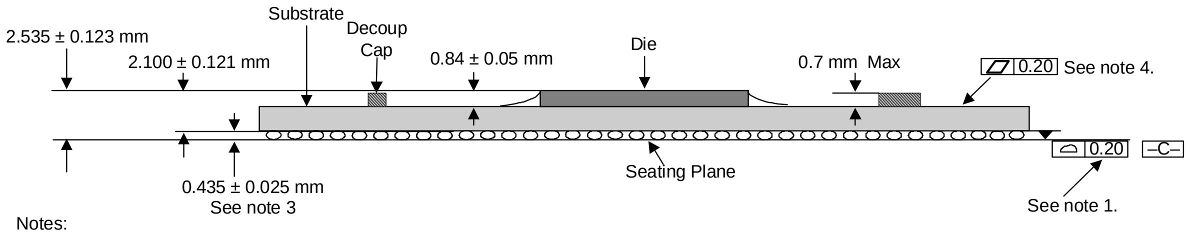
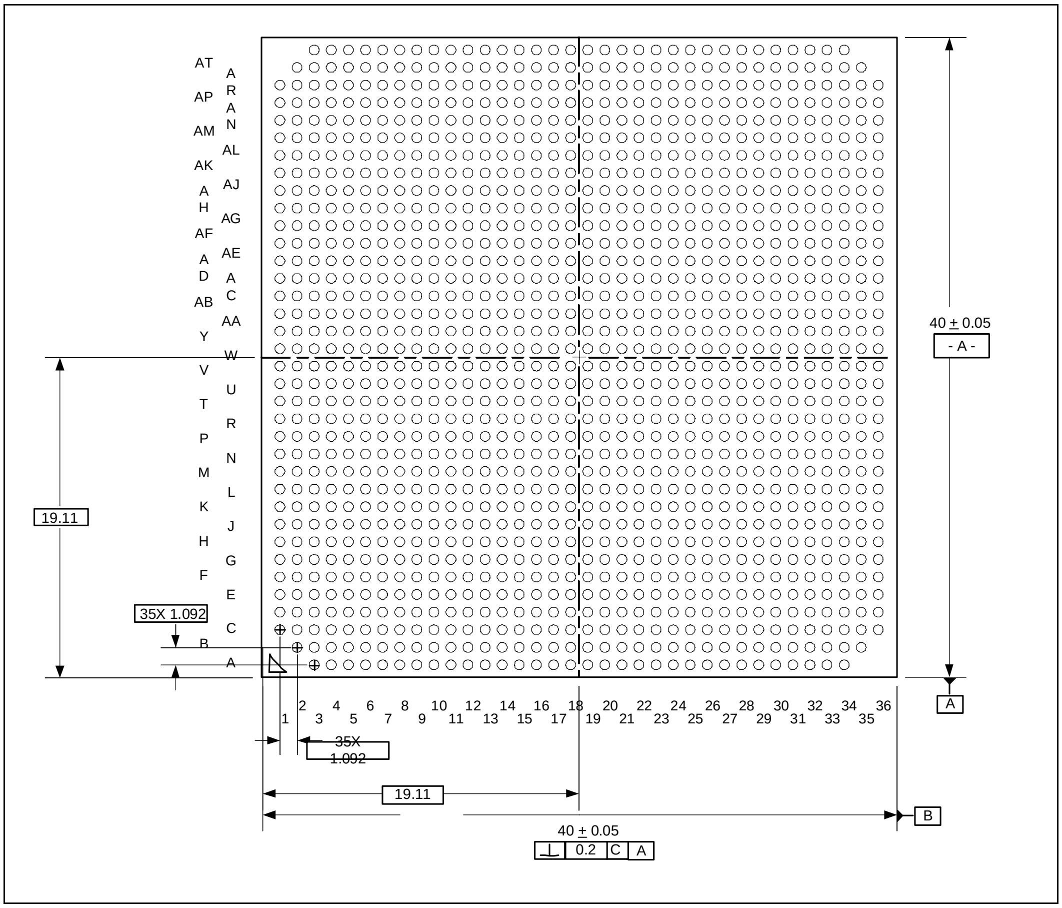


Figure 3. Intel® 6321ESB I/O Controller Hub Package Dimensions (Side View)



Notes:
1. Primary datum -C- and seating plan are defined by the spherical crowns of the solder balls (shown before motherboard attach)
2. All dimensions and tolerances conform to ANSI Y14.5M-1994
3. BGA has a pre-SMT height of 0.5mm and post-SMT height of 0.41-0.46mm
4. Shown before motherboard attach; FCBGA has a convex (dome shaped) orientation before reflow and is expected to have a slightly concave (bowl shaped) orientation after reflow

Figure 4. Intel® 6321ESB I/O Controller Hub Package Dimensions (Bottom View)



Notes:

1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M-1994.
3. Package Mechanical Requirements

The Intel® 6321ESB I/O Controller Hub package has an exposed bare die which is capable of sustaining a maximum static normal load of 15-lbf. The package is NOT capable of sustaining a dynamic or static compressive load applied to any edge of the bare die. These mechanical load limits must not be exceeded during heatsink installation, mechanical stress testing, standard shipping conditions and/or any other use condition.

Notes:

1. The heatsink attach solutions must not include continuous stress onto the chipset package with the exception of a uniform load to maintain the heatsink-to-package thermal interface.
2. These specifications apply to uniform compressive loading in a direction perpendicular to the bare die/ IHS top surface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only.

3.0 Thermal Specifications

3.1 Thermal Design Power (TDP)

Analysis indicates that real applications are unlikely to cause the Intel® 6321ESB I/O Controller Hub component to consume maximum power dissipation for sustained time periods. Therefore, in order to arrive at a more realistic power level for thermal design purposes, Intel characterizes power consumption based on known platform benchmark applications. The resulting power consumption is referred to as the Thermal Design Power (TDP). TDP is the target power level that the thermal solutions should be designed to. TDP is not the maximum power that the chipset can dissipate.

For TDP specifications, see Table 3. Flip chip ball grid array (FC-BGA) packages have poor heat transfer capability into the board and have minimal thermal capability without a thermal solution. Intel recommends that system designers plan for a heatsink when using the Intel® 6321ESB I/O Controller Hub component.

3.2 Die Case Temperature

To ensure proper operation and reliability of the Intel® 6321ESB I/O Controller Hub component, the die temperatures must be at or between the maximum/minimum operating temperature ranges as specified in Table 3. System and/or component level thermal solutions are required to maintain these temperature specifications. Refer to Chapter 6.0 for guidelines on accurately measuring package die temperatures.

Table 3. Intel® 6321ESB I/O Controller Hub Thermal Specifications

Parameter	Value	Notes
Tcase_max	105°C	
Tcase_min	5°C	
TDP	12.4W	

Note: These specifications are based on silicon characterization; however, they may be updated as further data becomes available.

4.0 Thermal Simulation

Intel provides thermal simulation models of the Intel® 6321ESB I/O Controller Hub component and associated user's guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated, system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool Flotherm* (version 5.1 or higher) by Flomerics, Inc*. These models are also available in IcePak* format. Contact your Intel field sales representative to order the thermal models and user's guides.

5.0 Thermal Solution Requirements

5.1 Characterizing the Thermal Solution Requirement

The idea of a "thermal characterization parameter" Ψ (the Greek letter psi), is a convenient way to characterize the performance needed for the thermal solution and to compare thermal solutions in identical situations (i.e., heating source, local ambient conditions, etc.). The thermal characterization parameter is calculated using total package power, whereas actual thermal resistance, θ (theta), is calculated using actual power dissipated between two points. Measuring actual power dissipated into the heat sink is difficult, since some of the power is dissipated via heat transfer into the package and board.

The case-to-local ambient thermal characterization parameter (Ψ_{CA}) is used as a measure of the thermal performance of the overall thermal solution. It is defined by Equation 1 and measured in units of °C/W.

Equation 1. Case-to-Local Ambient Thermal Characterization Parameter (Ψ_{CA})

$$\Psi_{CA} = \frac{T_{CASE} - T_{LA}}{TDP}$$

The case-to-local ambient thermal characterization parameter, Ψ_{CA}, is comprised of Ψ_{CS}, the thermal interface material (TIM) thermal characterization parameter, and of Ψ_{SA}, the sink-to-local ambient thermal characterization parameter:

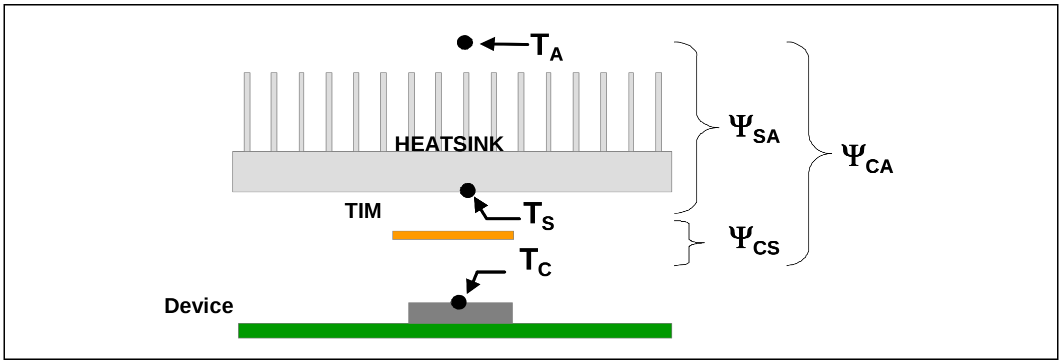
Equation 2. Case-to-Local Ambient Thermal Characterization Parameter (Ψ_{CA})

$$\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$$

Ψ_{CS} is strongly dependent on the thermal conductivity and thickness of the TIM between the heat sink and device package.

Ψ_{SA} is a measure of the thermal characterization parameter from the bottom of the heat sink to the local ambient air. Ψ_{SA} is dependent on the heat sink material, thermal conductivity, and geometry. It is also strongly dependent on the air velocity through the fins of the heat sink. Figure 5 illustrates the combination of the different thermal characterization parameters.

Figure 5. Processor Thermal Characterization Parameter Relationships



Example 1. Calculating the Required Thermal Performance

The cooling performance, Ψ_{CA}, is defined using the thermal characterization parameter previously described. The process to determine the required thermal performance to cool the device includes:

1. Define a target component temperature T_{CASE} and corresponding TDP.
2. Define a target local ambient temperature, T_{LA}.
3. Use Equation 1 and Equation 2 to determine the required thermal performance needed to cool the device.

The following provides an example of how you might determine the appropriate performance targets.

Assume:

- TDP = 12.4 W and T_{CASE} = 105° C
- Local processor ambient temperature, T_{LA} = 65° C.

Then the following could be calculated using Equation 1 for the given chipset configuration:

$$\Psi_{CA} = \frac{T_{CASE} - T_{LA}}{TDP} = \frac{105 - 65}{12.4} = 3.23° \frac{C}{W}$$

To determine the required heat sink performance, a heat sink solution provider would need to determine Ψ_{CS} performance for the selected TIM and mechanical load configuration. If the heat sink solution were designed to work with a TIM material performing at $\Psi_{CS} \leq 0.35$ °C/W, solving from Equation 2, the performance needed from the heat sink is:

$$\Psi_{SA} = \Psi_{CA} - \Psi_{CS} = 3.23 - 0.35 = 2.88°\frac{C}{W}$$

If the local ambient temperature is relaxed to 45° C, the same calculation can be carried out to determine the new case-to-ambient thermal resistance:

$$\Psi_{CA} = \frac{T_C - T_{LA}}{TDP} = \frac{105 - 45}{12.4} = 4.84°\frac{C}{W}$$

It is evident from the above calculations that a reduction in the local ambient temperature has a significant effect on the case-to-ambient thermal resistance requirement. This effect can contribute to a more reasonable thermal solution including reduced cost, heat sink size, heat sink weight, and a lower system airflow rate.

Table 4 summarizes the thermal budget required to adequately cool the Intel® 6321ESB I/O Controller Hub in one configuration using a TDP of 12.4 W. Further calculations would need to be performed for different TDPs. Since the results are based on air data at sea level, a correction factor would be required to estimate the thermal performance at other altitudes.

Table 4. Required Heat Sink Thermal Performance (Ψ_{CA})

Device	Ψ_{CA} (° C/W) at T_{LA} = 45° C	Ψ_{CA} (° C/W) at T_{LA} = 65° C
Intel® 6321ESB I/O Controller Hub @ 12.4 W	4.84	3.23

6.0 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the Intel® 6321ESB I/O Controller Hub die temperatures. Section 6.1 provides guidelines on how to accurately measure the Intel® 6321ESB ICH die temperatures. The flowchart in Figure 6 offers useful guidelines for thermal performance and evaluation.

6.1 Die Case Temperature Measurements

To ensure functionality and reliability, the Tcase of the Intel® 6321ESB ICH must be maintained at or between the maximum/minimum operating range of the temperature specification as noted in Table 3. The surface temperature at the geometric center of the die corresponds to Tcase. Measuring Tcase requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, and/or contact between the thermocouple cement and the heatsink base. For maximize measurement accuracy, only the 0° thermocouple attach approach is recommended.

6.1.1 Zero Degree Angle Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot from the centered hole to one edge of the heatsink. The slot should be parallel to the heatsink fins (see Figure 7).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. It is critical that the thermocouple bead makes contact with the die (see Figure 8).
6. Attach heatsink assembly to the MCH and route thermocouple wires out through the milled slot.

Figure 6. Thermal Solution Decision Flowchart

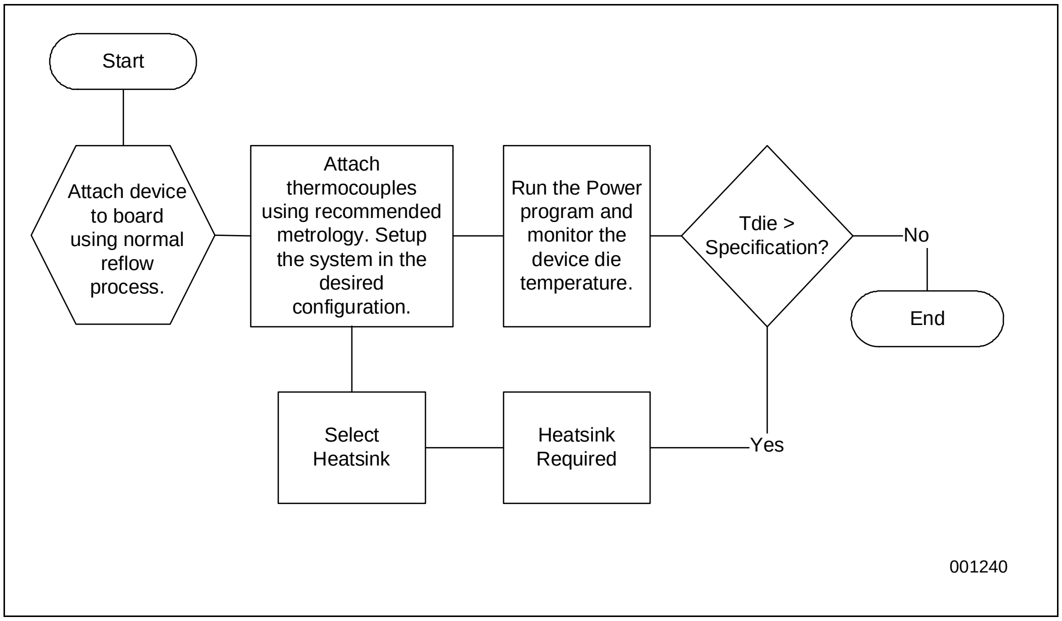
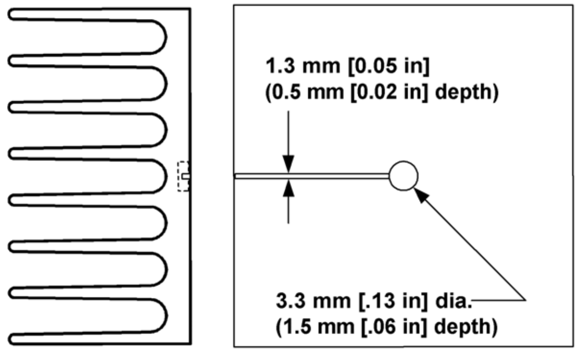
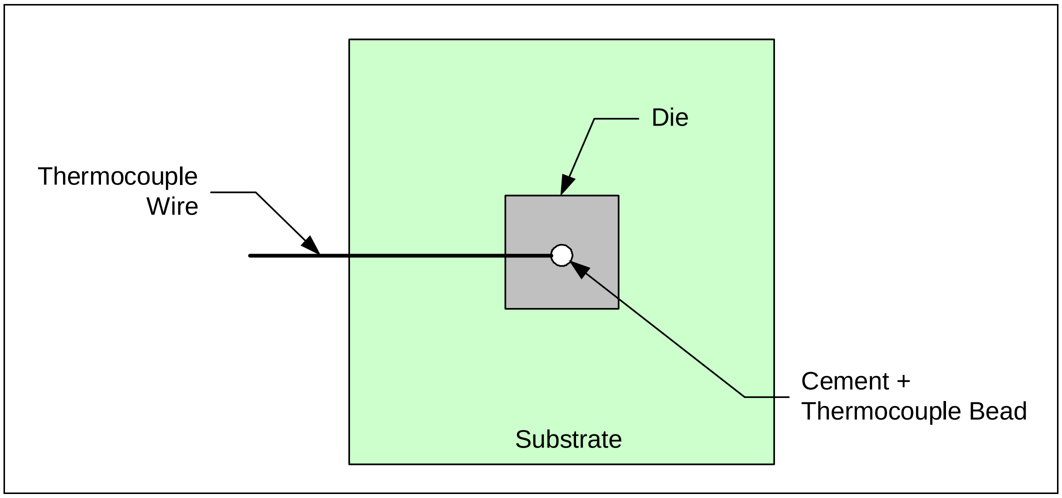


Figure 7. Zero Degree Angle Attach Heatsink Modifications



Note: Not to scale.

Figure 8. Zero Degree Angle Attach Methodology (Top View)



Note: Not to scale.

7.0 Reference Thermal Solution

Intel has developed one reference thermal solution to meet the cooling needs of the Intel® 6321ESB I/O Controller Hub component under operating environments and specifications defined in this document. This chapter describes the overall requirements for the Torsional Clip Heatsink reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need attached thermal solutions, depending on your specific system local-ambient operating conditions.

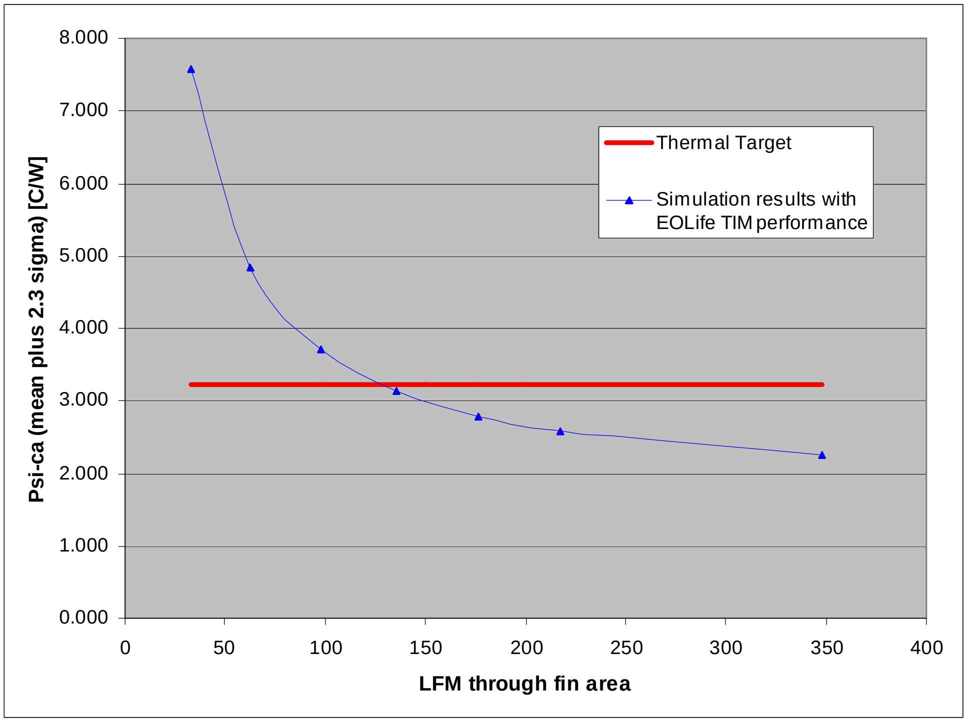
7.1 Operating Environment

The Intel® 6321ESB ICH reference thermal solution was designed assuming a maximum local-ambient temperature of 65°C. The minimum recommended airflow velocity through the cross section of the heatsink fins is 150 linear feet per minute (LFM). The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. These local-ambient conditions are based on a 55°C external-ambient temperature at sea level. (External-ambient refers to the environment external to the system.)

7.2 Heatsink Performance

Figure 9 depicts the measured thermal performance of the reference thermal solution versus approach air velocity. Since this data was measured at sea level, a correction factor would be required to estimate thermal performance at other altitudes.

Figure 9. Torsional Clip Heatsink Measured Thermal Performance Versus Approach Velocity and Target at 65C Local-Ambient

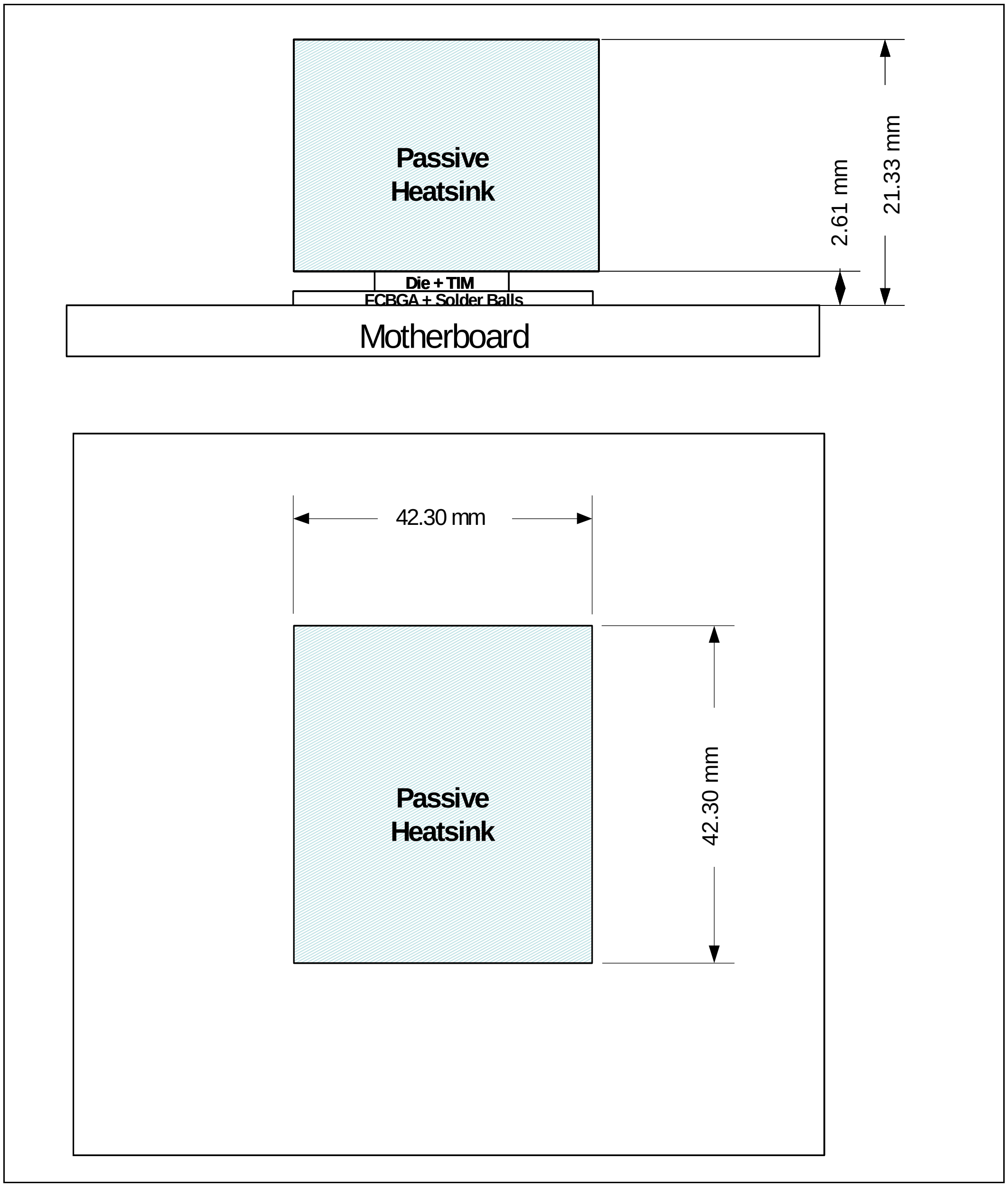


7.3 Mechanical Design Envelope

While each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the Intel® 6321ESB ICH thermal solution are shown in Figure 10.

When using heatsinks that extend beyond the Intel® 6321ESB I/O Controller Hub reference heatsink envelope shown in Figure 10, any motherboard components placed between the heatsink and motherboard cannot exceed 2.46 mm (0.10 in.) in height.

Figure 10. Torsional Clip Heatsink Volumetric Envelope for the Intel® 6321ESB I/O Controller Hub



7.4 Board-Level Components Keepout Dimensions

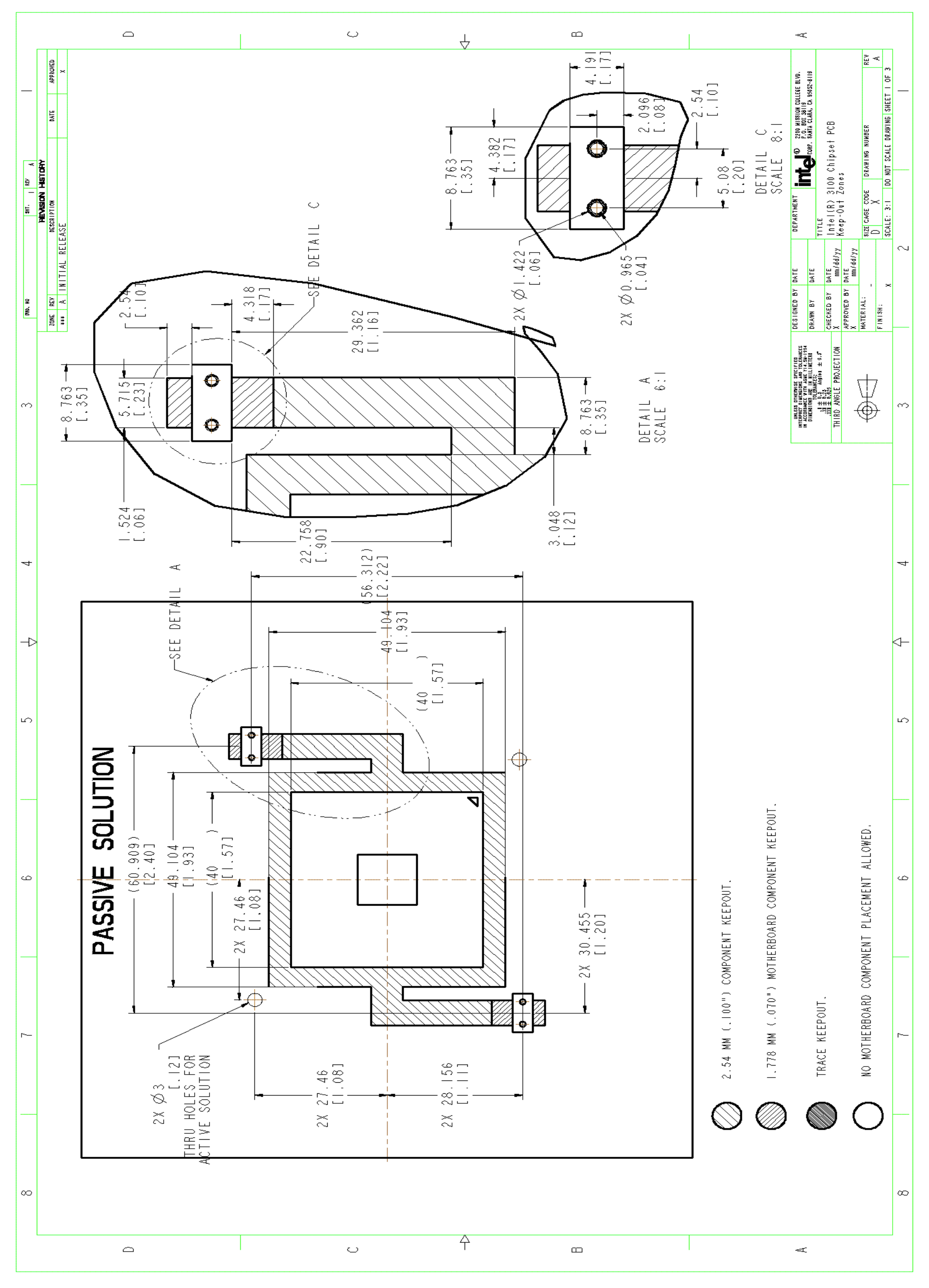
The location of holes pattern and keepout zones for the reference thermal solution are shown in Figure 11. This reference thermal solution has the same mounting hole pattern as that of the Intel® E7500/E7501/E7505 chipset.

7.5 Torsional Clip Heatsink Thermal Solution Assembly

The reference thermal solution for the Intel® 6321ESB ICH component is a passive heatsink with thermal interface. It is attached using a clip with each end hooked through an anchor soldered to the board. Figure 12 shows the reference thermal solution assembly and associated components. The torsional clip and the clip retention anchor are the same as the one used on the Intel® E7500/E7501/E7505 and 3100 chipset reference thermal solutions.

Full mechanical drawings of the thermal solution assembly and the heatsink clip are provided in Appendix B, "Mechanical Drawings". Appendix A, "Thermal Solution Component Suppliers" contains vendor information for each thermal solution component.

Figure 11. Torsional Clip Heatsink Board Component Keepout

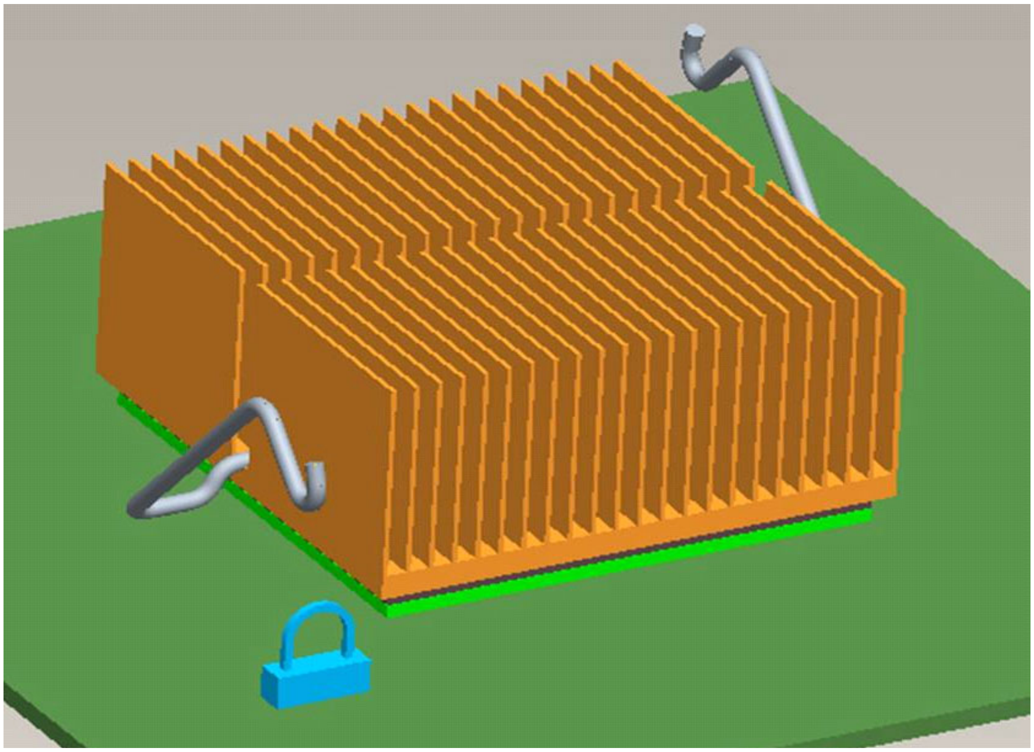


Note: Same Keepout zones as Intel ® 3100 Chipset

7.5.1 Heatsink Orientation

Since this solution is based on a unidirectional heatsink, mean airflow direction must be aligned with the direction of the heatsink fins.

Figure 12. Torsional Clip Heatsink Assembly



7.5.2 Mechanical Interface Material

There is no mechanical interface material associated with this reference solution.

7.5.3 Thermal Interface Material

A Thermal Interface Material (TIM) provides improved conductivity between the die and heatsink. The reference thermal solution uses Honeywell* PCM45F, 0.254 mm (0.010 in.) thick, 15 mm x 15 mm (0.59 in. x 0.59 in.) square.

Note: Unflowed or "dry" Honewell PCM-45F has a material thickness of 0.010 inch. The flowed or "wet" Honeywell PCM-45F has a material thickness of ~0.003 inch after it reaches its phase change temperature.

7.5.3.1 Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). BLT is the final settled thickness of the thermal interface material after installation of heatsink. The effect of pressure on the thermal resistance of the Honeywell PCM45 F TIM is shown in Table 5.

Intel provides both End of Line and End of Life TIM thermal resistance values of Honeywell PCM45F. End of Line and End of Life TIM thermal resistance values are obtained through measurement on a Test Vehicle similar to the Intel® 631xESB/632xESB I/O's physical attributes using an extruded aluminum heatsink. The End of Line value represents the TIM performance post heatsink assembly while the End of

Life value is the predicted TIM performance when the product and TIM reaches the end of its life. The heatsink clip provides enough pressure for the TIM to achieve End of Line thermal resistance of 0.345 °C x in^2/W and End of Life thermal resistance of 0.459°C in^2/W.

Table 5. Honeywell PCM45 F TIM Performance as a Function of Attach Pressure

Pressure on IHS(psi)	Thermal Resistance (°C × in^2) / W	
	End of Line End of Life	End of Line End of Life
2.18	0.391	0.551
4.35	0.345	0.459

Note: All measured at 50ºC.

7.5.4 Heatsink Clip

The reference solution uses a wire clip with hooked ends. The hooks attach to wire anchors to fasten the clip to the board. See Appendix B, “Mechanical Drawings” for a mechanical drawing of the clip.

7.5.5 Clip Retention Anchors

For Intel® 6321ESB I/O Controller Hub-based platforms that have very limited board space, a clip retention anchor has been developed to minimize the impact of clip retention on the board. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45° bent leads to increase the anchor attach reliability over time. See Appendix A, “Thermal Solution Component Suppliers” for the part number and supplier information.

8.0 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. Some general recommendations are shown in Table 6.

Table 6. Reliability Guidelines

Test (1)	Requirement	Pass/Fail Criteria (2)
Mechanical Shock	50 g, board level, 11 msec, 3 shocks/axis	Visual Check and Electrical Functional Test
Random Vibration	7.3 g, board level, 45 min/axis, 50 Hz to 2000 Hz	Visual Check and Electrical Functional Test
Temperature Life	85°C, 2000 hours total, checkpoints at 168, 500, 1000, and 2000 hours	Visual Check
Thermal Cycling	-5°C to +70°C, 500 cycles	Visual Check
Humidity	85% relative humidity, 55°C, 1000 hours	Visual Check

Notes:
1. It is recommended that the above tests be performed on a sample size of at least twelve assemblies from three lots of material.
2. Additional pass/fail criteria may be added at the discretion of the user.

§ §

Appendix A Thermal Solution Component Suppliers

A.1 Torsional Clip Heatsink Thermal Solution

Part	Intel Part Number	Supplier (Part Number)	Contact Information
AdvancedTCA* and Embedded Form Factor Heat Sink	N/A	ECB-00306-01-GP (Aluminum)	Wendy Lin 510-770-8566, x211 Wendy@coolermaster.com
Thermal Interface (PCM45F)	N/A	Honeywell* PCM45F	Paula Knoll 858-705-1274 paula.knoll@honeywell.com
Heatsink Attach Clip	A69230-001	CCI/ACK	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
Heat Sink Attach Clip	A69230-001	Foxconn*	Bob Hall (USA) 503-693-3509, x235 bhall@foxconn.com
Solder-Down Anchor	A13494-005	Foxconn (HB96030-DW)	Julia Jiang (USA) 408-919-6178 juliaj@foxconn.com

Note: The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.

Appendix B Mechanical Drawings

Table 7 lists the mechanical drawings included in this appendix.

Table 7. Mechanical Drawing List

Drawing Description	Figure Number
Torsional Clip Heatsink Assembly Drawing	Figure 13
Torsional Clip Heatsink Drawing	Figure 14
Heat Sink Foam Gasket Drawing	Figure 15
Torsional Clip Drawing	Figure 16

Figure 13. Torsional Clip Heatsink Assembly Drawing

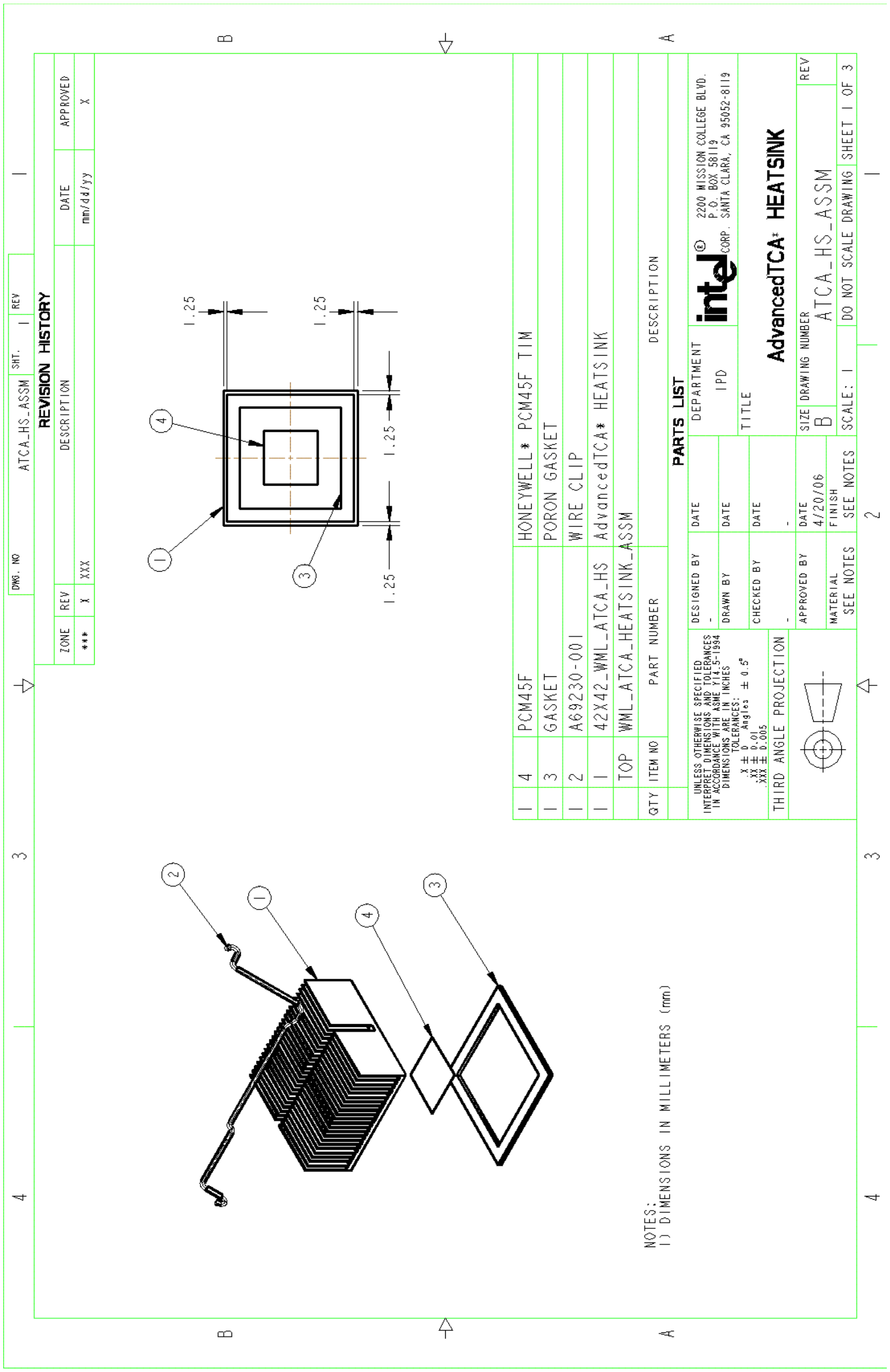


Figure 14. Torsional Clip Heatsink Drawing

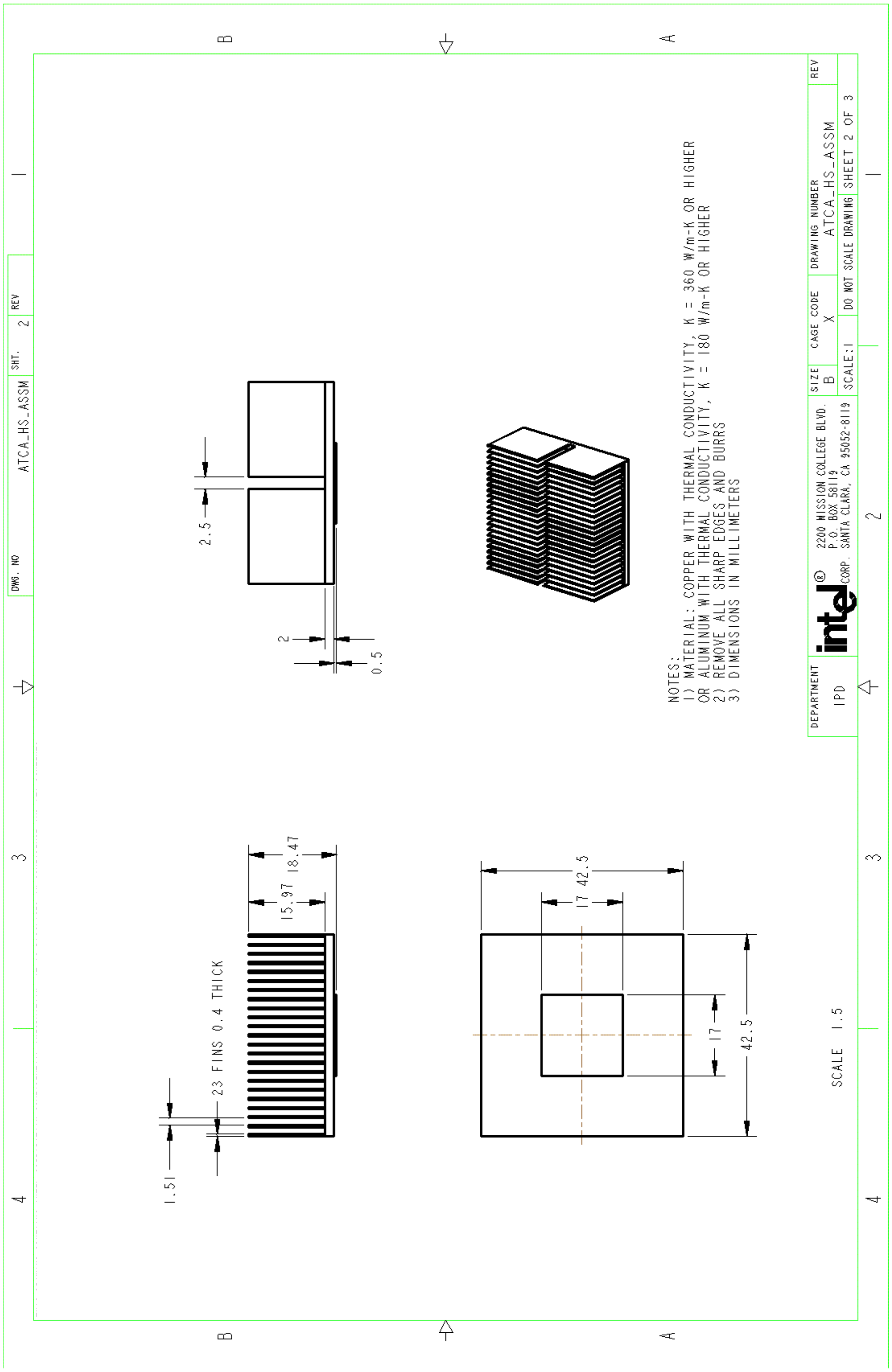


Figure 15. Heat Sink Foam Gasket Drawing

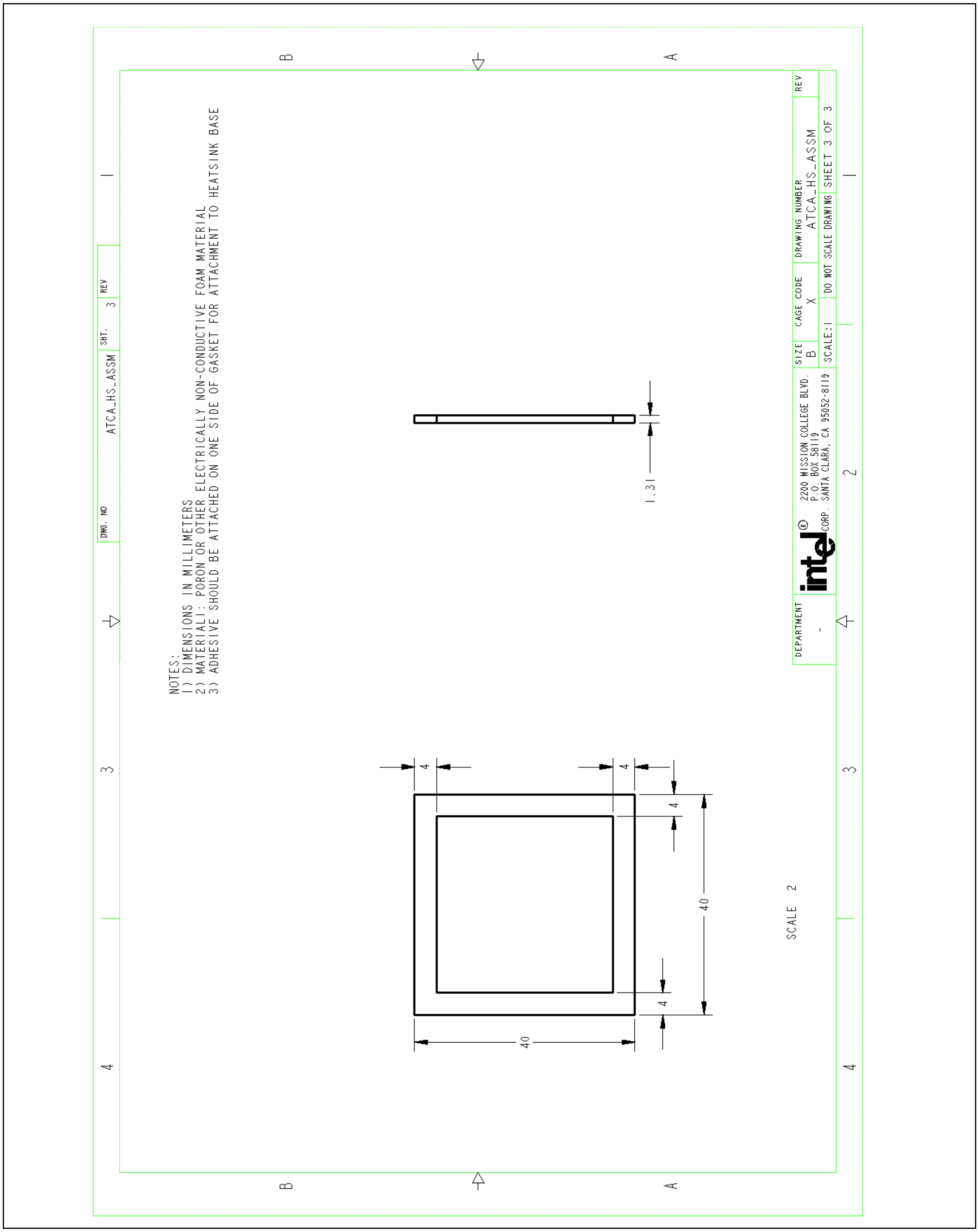
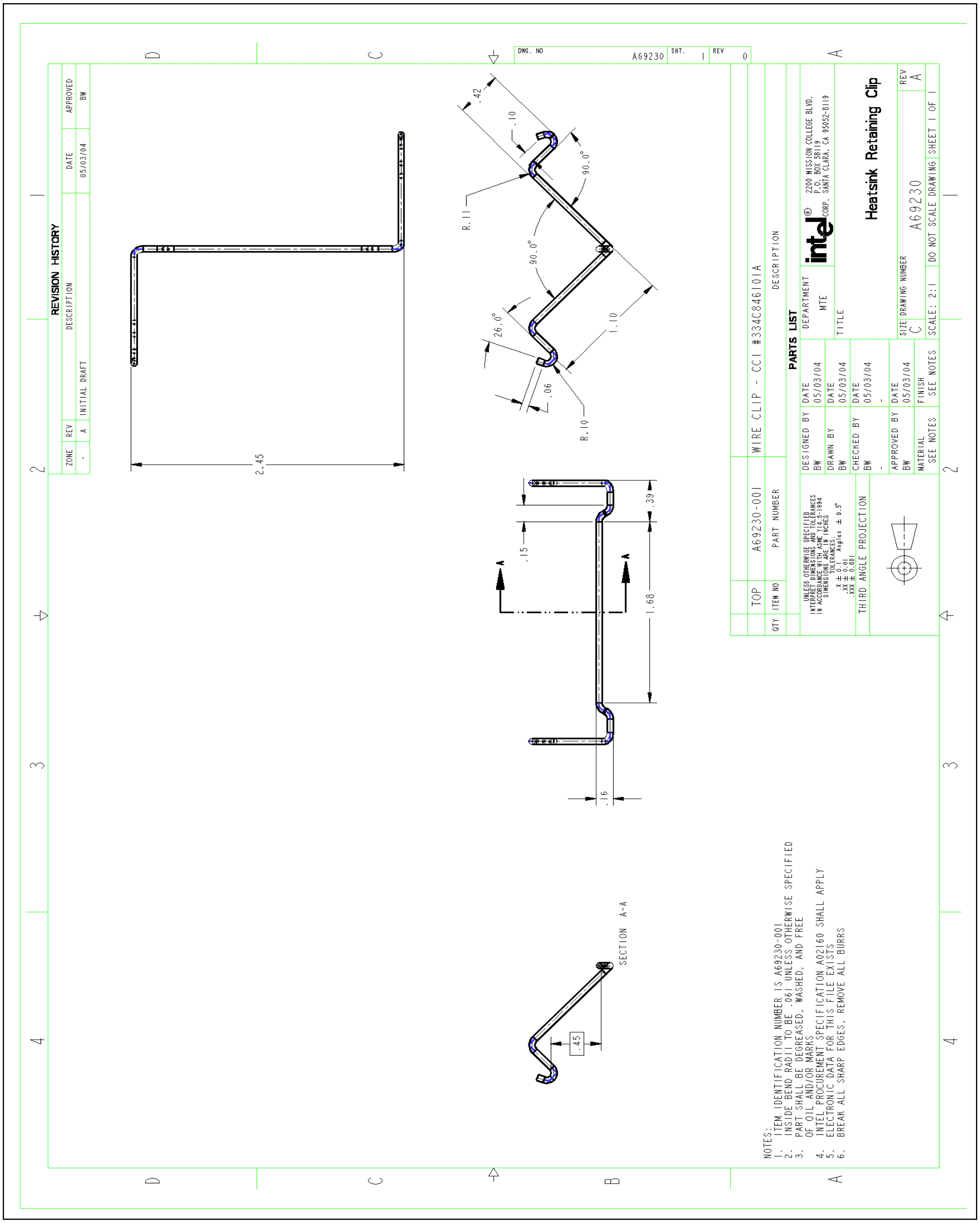


Figure 16. Torsional Clip Drawing



NOTES:
1. ITEM IDENTIFICATION NUMBER IS A69230-001
2. INSIDE BEND RADII TO BE .061 UNLESS OTHERWISE SPECIFIED
3. PART SHALL BE DEGREASED, WASHED, AND FREE OF OIL AND/OR MARKS
4. INTEL PROCUREMENT SPECIFICATION A02160 SHALL APPLY
5. ELECTRONIC DATA FOR THIS FILE EXISTS
6. BREAK ALL SHARP EDGES, REMOVE ALL BURRS