F²MC-16LX Family 16-bit Microcontroller Mounted with Dual-Operation Flash Memories **MB90890 Series**

A new F²MC-16LX CPU-driven microcontroller series is available with 64 K-byte dual-operation flash memories and a CAN controller integrated in a compact 48-pin package. This is the world first lineup of microcontrollers mounted with dual-operation flash memories.

Product Description

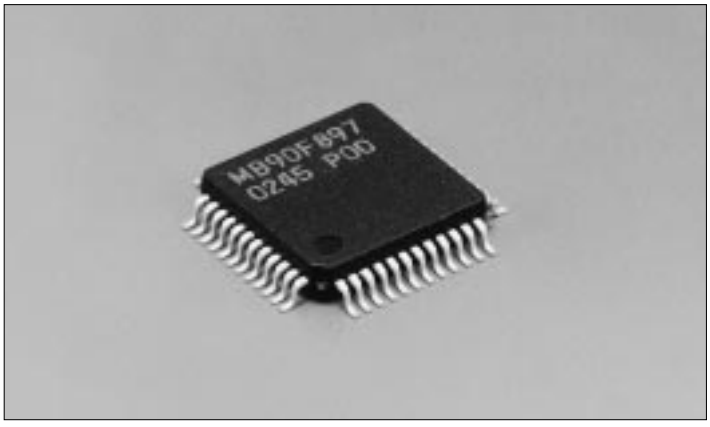
The new series provides the world first high-performance 16-bit CPU integrating dual-operation flash memories, together with a CAN controller, all within a LQFP-48 compact package.

CAN, Controller Area Network, is now the prevailing global standard for LAN systems installed in automobiles. The trend began in Europe, the first region in the world to adopt the CAN controller-mounted microcontrollers, and now FUJITSU is taking the lead in the industry by offering diversified lineups of CAN microcontrollers as solutions for the control of safety and amenity functions in automobiles. The Company has just succeeded in offering the world first microcontrollers mounted with flash memories that allow simultaneous execution of read/write operations. With this innovation, the flash memories applied conventionally for readout purposes to change programs can now be used to store various types of data during power interruptions.

This innovation offers several other advantages, as well. By eliminating the need for EEPROM and related component parts externally installed in the conventional designs, it substantially reduces cost. It also facilitates the new application of advanced controls for amenity, safety and communication, including learning and tracing of maintenance data with the use of large-density nonvolatile data memories.

The new series also offers an improved operating margin to

Photo 1 External View



pave the way towards packages that meet the higher standards of safety and reliability listed below.

- An extended range of operating voltages between 3.5V and 5.5V, ensuring enhanced reliability for system operation without possible voltage drops
- A 50% or greater increase in the margin for the circuit, from the typical 0.3VCC to less than 0.5VCC. This enables recognition of the 0 level of input voltages, opening up new possibilities for the realization of noise-resistant systems

Product Features

Configured with FUJITSU's original high-performance F²MC-16LX CPU

Minimum instruction execution time of 62.5ns (at 16MHz internal operation frequency)

System clock speed that can be increased by integral multiples with the internal PLL clock (enables increased internal operating frequency by an integral multiple of 1 to 4 times the base oscillator frequency)

Instruction set supporting C language and multitasking

Four available power-saving modes

- Sleep mode (CPU clock set OFF)
- Time-base timer mode
  (All timers but the time-base timer set OFF)
- Stop mode (Base oscillator set OFF)
- CPU intermittent operation mode
  (CPU operating clock repeatedly toggles ON and OFF based on preset values)

Resources

- I/O port: A maximum of 36 ports available (including four for higher-current outputs)
- 18-bit time-base counter/Watchdog timer/Clock timer: 1 channel
- 8/16-bit PPG timer: 8-bit×4-channel, or 16-bit×2-channel
- 16-bit reload timer: 2 channels
- 16-bit I/O timer
  16-bit free-running timer: 1 channel
  16-bit input capture (ICU): 4 channels
- UART: 2 channels
- DTP/external interruption circuit: 4 channels

Figure 1 Operation of Dual-Operation Flash Memory-Integrated Microcontroller Series MB90F897

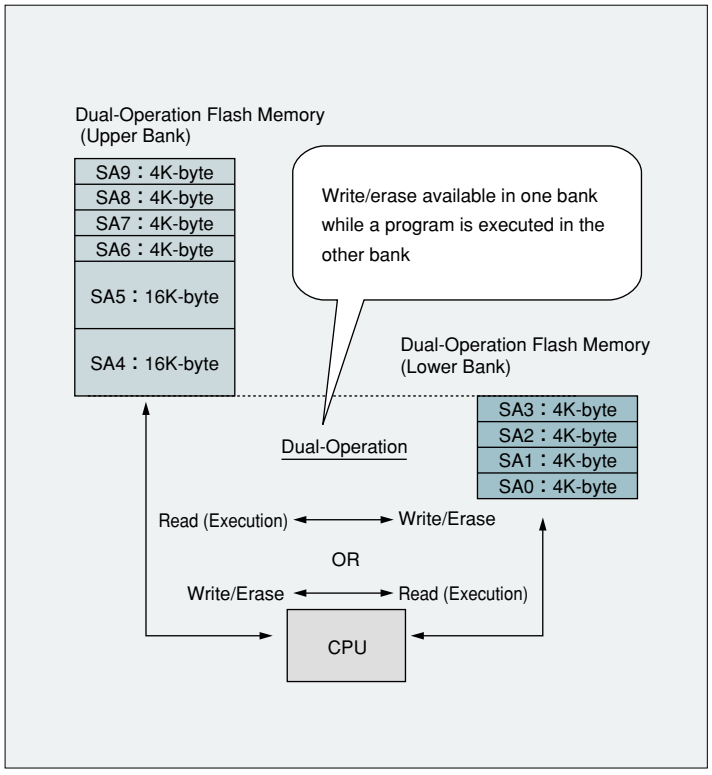
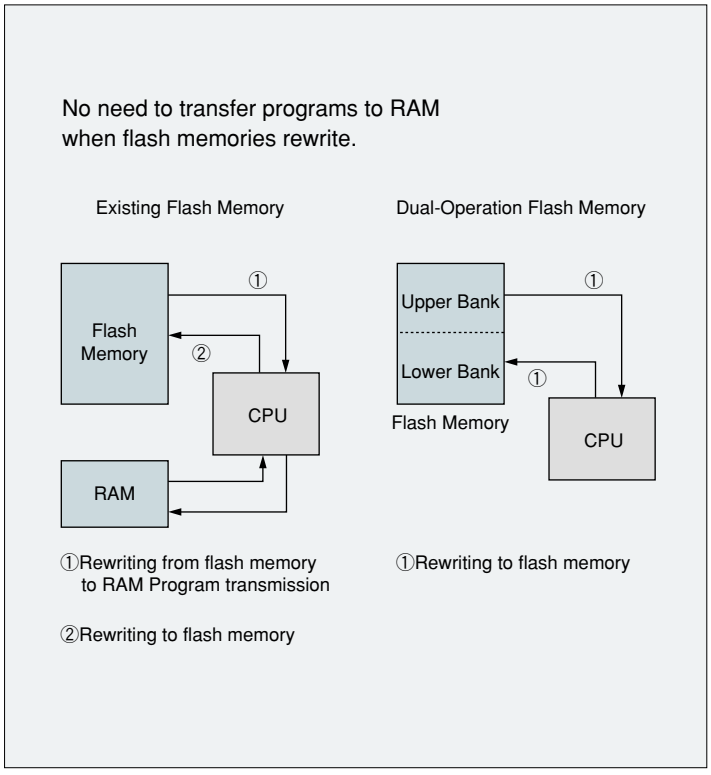


Figure 2 Operational Flow of CPU Rewrite by Flash Memory



- Delayed interruption generating module
- 8/10-bit A/D converter: 8 channels
- Address match detection function
- Input level changeable by software

■ **Package: FPT-48P-M26**

Features of Dual-Operation Flash Memory-Integrated Microcontrollers

Fig. 1 outlines the operation of MB90F897 series microcontrollers mounted with dual-operation flash memories. While the upper bank flash memory handles the execution of programs, the lower bank flash memory can be applied for write/erase operations (or vice versa). The new series also offers the following advantages for system control.

■ No need to download programs to RAM when flash memories self-rewrite to the CPU

Fig. 2 shows the operational flow for rewriting from flash memories to the CPU.

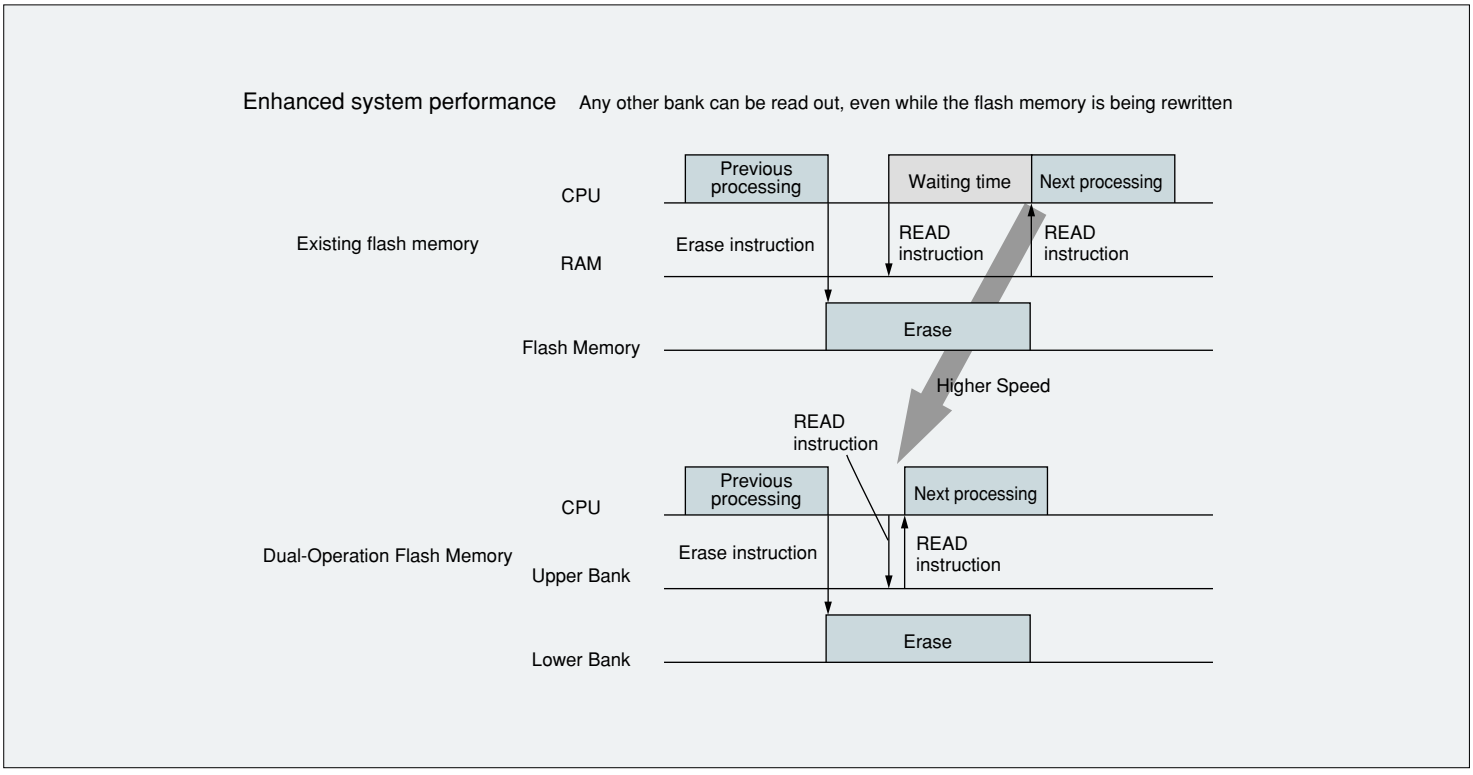
In conventional microcontrollers mounted with flash memories, programs have to be downloaded to RAM in order to initiate rewrites, as these devices disallow rewrite operations while programs are executed in the flash memories. FUJITSU's new microcontrollers integrated with dual-operation flash memory allow rewrites by executing programs on flash memory, thereby eliminating the need to transfer the programs to RAM. This obviates the need to make provisions against power failures during program execution on RAM, and cuts down the program download time as well.

■ Flash memory rewrites performed concurrently with system control

Fig. 3 illustrates the control sequence for rewriting the flash memory using interruption.

Conventionally, FUJITSU's flash memory-integrated microcontrollers have not been designed to allow interruptions while the RAM is executing a program. After the write/erase commands are issued, the software has to check the flag to identify whether or not the write/erase operation is completed. With the dual-operation flash

Figure 3 Control of Flash Memory Rewrite Based on Interruption



memory-integrated microcontrollers, the interruption can take place in response to any interruption factor generated after the write/erase is completed, thus enabling the processing of other programs after the write/erase command is issued. Write/erase operations for flash memories are smoothly and reliably executed while system control is in progress.

Fig. 4 provides the specifications for bank-to-bank transmission of the interruption vector.

The interruption vector is transmitted to the upper bank flash memory to rewrite the flash memory in the lower bank, and vice versa. Thus, interruption-based control is available for rewriting in either bank.

The software sector-protect function prevents erroneous writing/erasing of flash memory

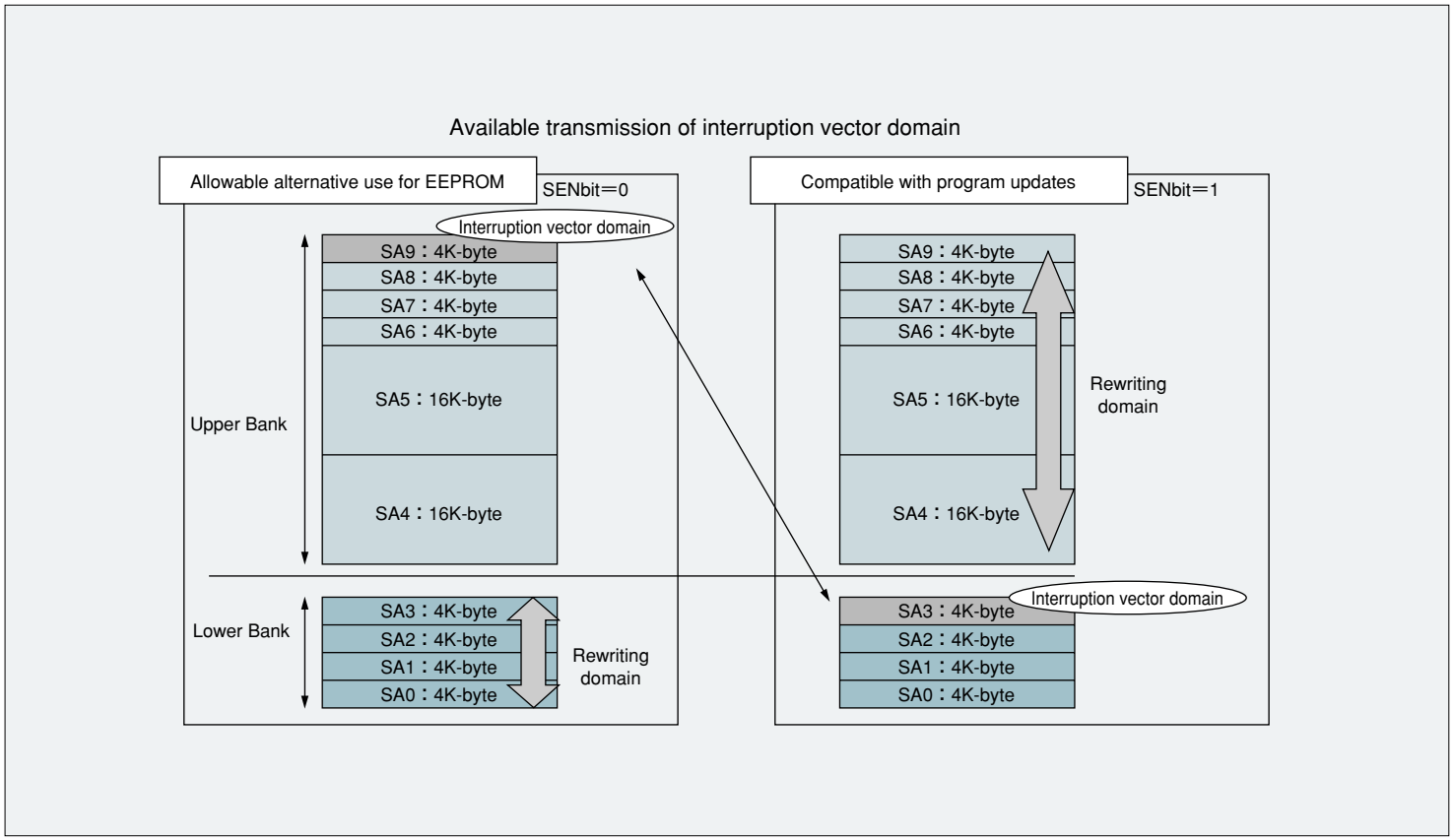
In the new series, settable sector-protect bits are assigned to protect individual sectors. An "0" setting in the bit sets the sector-protect function active, thereby protecting the target sector against attempts to perform write/erase operations. Once "0" is set, the "1" setting (to enable the write/erase) is disabled until any reset factor can be generated. This ensures that the flash memories are fully protected against write/erase attempts even in the case of program runaway.

Dual-operation flash memory-integrated microcontroller substitutes for an external EEPROM

Using the dual-operation flash memory-integrated microcontroller as a substitution for EEPROM offers the following benefits.

- Reduced system board mounting area
  The mounting area equivalent to an EEPROM footprint is reduced.
- Available EEPROM-like sector configuration
  Eight small-density (4K-byte) sectors are available, providing an easy-to-handle sector configuration for the data-rewrite area (Fig. 4).
- Faster write speed
  The targeted write time is 32μs/byte (typical), markedly faster than that with EEPROM.

Figure 4 Specifications for Bank-to-Bank Transmission of Interruption Vector



• Improved data reliability

Data can be written in the chip without external communication, eliminating concerns about data garble due to fluctuations in communications lines caused by external noise.

Table 1 provides a list of available packages in this series, **Fig. 5** is a block diagram, and **Fig. 6** shows pin assignments.

Development Environment

The new series is supported by SOFTUNE™ V3, a FUJITSU integrated software development environment. The SOFTUNE V3 application software is designed to simplify programming tasks to meet the diversified needs of program designers. The hardware is compatible with MB2140 Series, an emulator for the F²MC Family that permits real-time debugging.

Table 2 lists available development tools.

Typical Applications

The new series is a lineup of 16-bit commodity-grade microcontrollers tailor-engineered for applications that require high-speed real-time processing, data rewriting, or data storage to nonvolatile memory while executing programs on flash memories. Each device is incorporated in a compact 48-pin package suitable for system board installation within a limited mounting space. ✶

NOTES

* SOFTUNE is a trademark of FUJITSU LIMITED.

Figure 5 Block Diagram

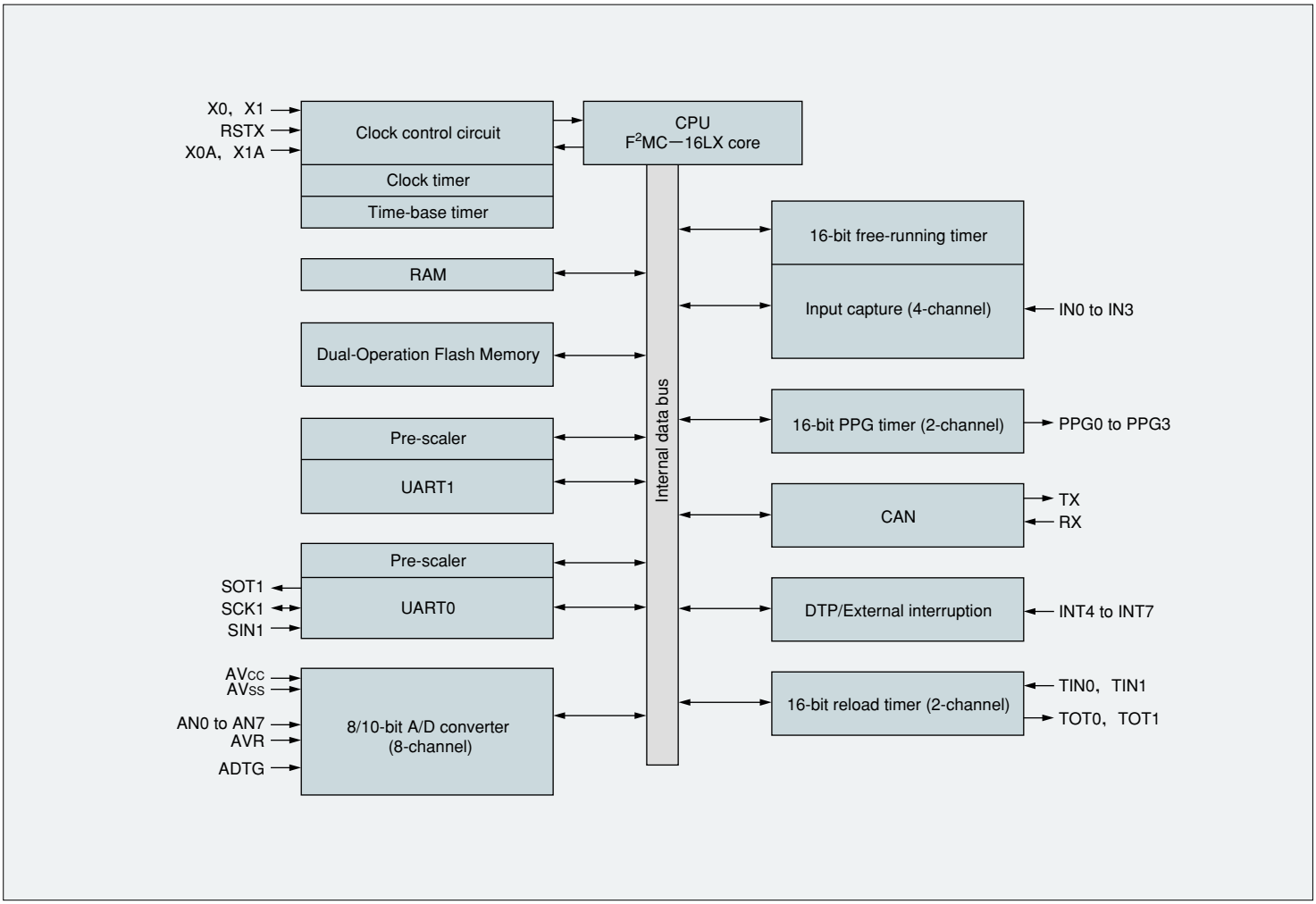


Table 1 Product Lineup

Item \ Model	MB90V495G	MB90F897/S
Type	Evaluation	Flash memory type
ROM density	Not installed	64K-byte
RAM density	6K-byte	2K-byte
CPU functions	Number of instructions：351 Maximum instruction execution time：62.5ns at an operating frequency of 4MHz (4 times the base oscillator frequency) Available addressing types：23 Allowable program patching：2 address pointers Maximum storage space：16M-byte	
Power-saving (Standby mode)	Sleep mode/Clock mode/Time-base timer mode/Stop mode/CPU intermittent mode	
I/O port	General-purpose I/O port (CMOS output)：34 (36*) Four of them intended for higher-current output ports	
Time-base timer	8-bit free-running counter Interruption interval：1.024ms, 4.096ms, 16.834ms, 131.072ms (at an oscillation clock frequency of 4MHz)	
Watchdog timer	Reset occurring interval：3.58ms, 14.33ms, 57.23ms, 458.75ms (at an oscillation clock frequency of 4MHz)	
16-bit I/O timer	16-bit free-running timer：1 channel Input capture：4 channels	
16-bit reload timer	Number of channels：2 Count clock interval：0.25 μs, 0.5 μs, 2.0 μs (Machine clock frequency 16MHz) Available external event counting	
Clock timer	15-bit free-running counter Interruption interval：31.25ms, 62.5ms, 12ms, 250ms, 500ms, 1.0ms, 2.0ms (at 8.192kHz sub clock)	
8/16-bit PPG timer	Number of channels：2-channel (Available in the 8-bit×4-channel configuration) PPG operation available in both the 8-bit×4-channel and 16-bit×2-channel configurations Allowable output of pulse waveform at any desired period and duty factor Count clock：62.5ns to 1μs (at a machine clock frequency of 16MHz)	
Delayed interruption generating module	Interruption generating module for task changing Used with the real-time OS	
DTP/External interruption	Number of channels：4 Rise edge/Fall edge activated in response to the input of "H" and "L" levels Available external interruption or extended intelligent I/O service (EI²OS)	
10-bit A/D converter	Number of channels：8 Resolution：Either 10-bit or 8-bit Conversion time：6.125μs (at a machine clock frequency of 16MHz, including the sampling time)	
UART（SCI）	Number of channels：2 With full duplex double buffers Transmission available in either state, synchronous or asynchronous to clock Also can be used as serial I/O Dedicated baud rate generator incorporated	
Process	CMOS	
Package	PGA256	LQFP-48
Operating voltage	4.5V to 5.5V	3.5V to 5.5V

*34 for MB90897：36 for MB90F897

Figure 6 Pin Assignments

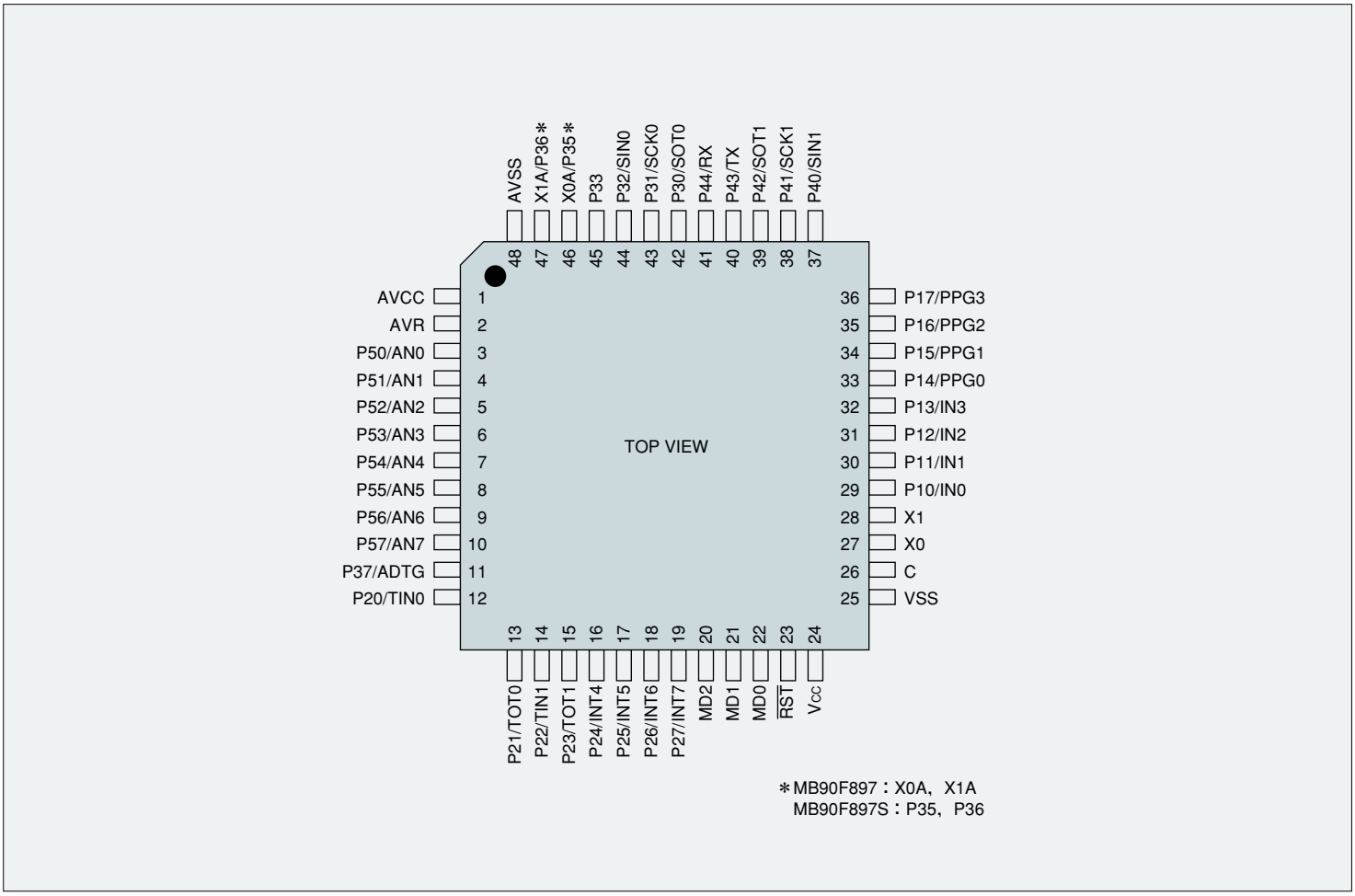


Table 2 Development Tools

Hardware	Main unit MB2141A
	Emulation pod MB2145-507
	Probe cable MB2132-466
Software	SOFTUNE V3 Workbench
	SOFTUNE V3 C Compiler
	SOFTUNE V3 Assembler
	SOFTUNE V3 C Analyzer
	SOFTUNE V3 C Checker