November 7, 2008

Errata Document for TrueTouch® CY8CTMG200, CY8CTST200

This document describes the errata for the TrueTouch® CY8CTMG200 and CY8CTST200. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's data sheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

CY8CTMG200 and CY8CTST200 Errata Summary

The following Errata items apply to the CY8CTMG200 and CY8CTST200 datasheets 001-47603 and 001-47602.

1. Latch-up susceptibility when maximum I/O sink current exceeded

- **PROBLEM DEFINITION**

  P1[3], P1[6], and P1[7] pins are susceptible to latch-up when the I/O sink current exceeds 25 mA per pin on these pins.

- **PARAMETERS AFFECTED**

  LU – Latch-up Current. Per JESD78A, the maximum allowable latch-up current per pin is 100 mA. Cypress internal specification is 200 mA latch-up current limit.

- **TRIGGER CONDITION(S)**

  Latch-up occurs when both of the following two conditions are met:

  A. The offending I/O is externally connected to a voltage higher than the I/O high state, causing a current to flow into the pin that exceeds 25 mA

  B. A Port1 I/O adjacent (P1[1], P1[4] and P1[5] respectively) to the offending I/O is connected to a voltage lower than the I/O low state, causing a signal that drops below Vss (signal undershoot), causing a current greater than 200 mA to flow out of the pin

- **SCOPE OF IMPACT**

  The trigger conditions outlined above exceed the maximum ratings specified in the CY8CTMG200 and CY8CTST200 datasheets 001-47603 and 001-47602.

- **WORKAROUND**

  Add a series resistor >300Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch-up limits.

- **FIX STATUS**

  This issue will be corrected in the next new silicon revision.

The following Errata item applies only to the **CY8CTMG200-48LTXI, CY8CTST200-48LTXI, and CY8CTMG200-00LTXI,** parts on the **001-47603 and 001-47602** Datasheets.

2. Does not meet USB 2.0 specification for D+ and D- rise/fall matching when supply voltage is under 3.3V

- **PROBLEM DEFINITION**

  Rising to falling rate matching of the USB D+ and D- lines has a corner case at lower supply voltages, such as those under 3.3V.

- **PARAMETERS AFFECTED**

  Rising to falling rate matching of the USB data lines.

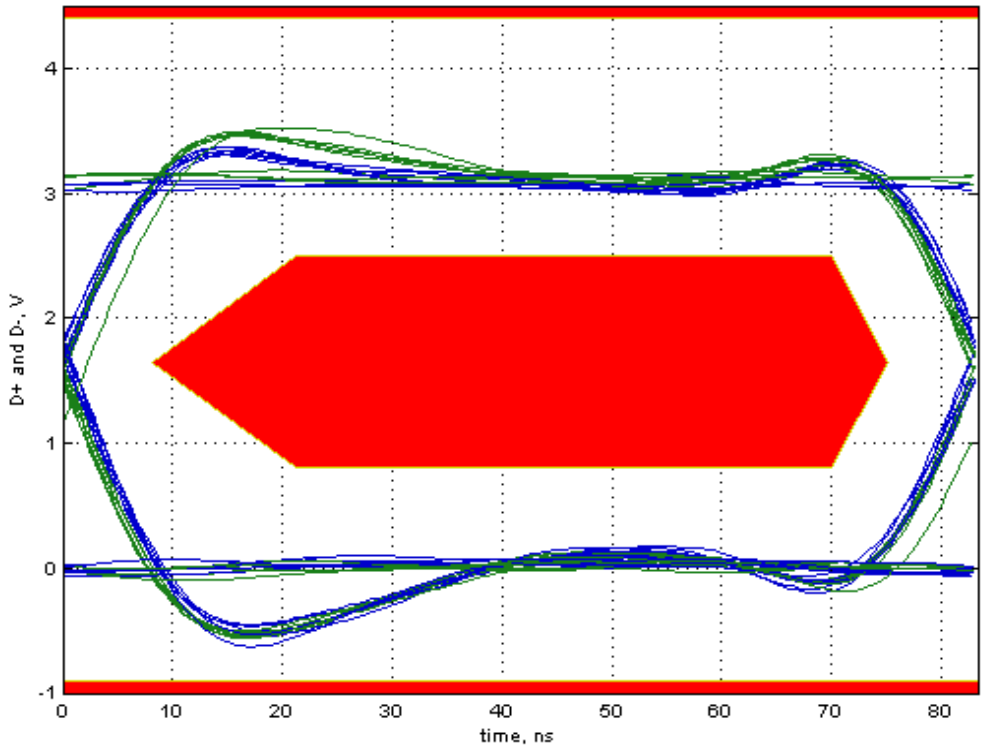
- **TRIGGER CONDITION(S)**

  Operating the VCC supply voltage at the low end of the chip's specification (under 3.3V) may cause a missmatch in the rising to falling rate.

- **SCOPE OF IMPACT**

  This condition does not affect USB communications but could cause corner case issues with USB lines' rise/fall matching specification. Signal integrity tests were run using the Cypress development kit for the part and excellent eye was observed with supply voltage of 3.15V.

Figure 1. Eye Diagram



- **WORKAROUND**

  Avoid the trigger condition by using lower tolerance voltage regulators.

- **FIX STATUS**

  This issue will be corrected in the next new silicon revision.

Document History Page

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	2603495	See ECN	DTB	First release.

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