PRELIMINARY

CY7C1330AV25
CY7C1332AV25

18-Mbit (512K x 36/1Mbit x 18) Pipelined Register-Register Late Write

Features

- **Fast clock speed: 250, 200 MHz**
- **Fast access time: 2.0, 2.25 ns**
- **Synchronous Pipelined Operation with Self-timed Late Write**
- **Internally synchronized registered outputs eliminate the need to control OE**
- **2.5V core supply voltage**
- **1.4–1.9V V_{DDQ} supply with V_{REF} of 0.68–0.95V**
  — Wide range HSTL I/O Levels
- **Single Differential HSTL clock Input K and $\overline{K}$**
- **Single $\overline{WE}$ (READ/WRITE) control pin**
- **Individual byte write ($\overline{BWS_{[a:d]}}$) control (may be tied LOW)**
- **Common I/O**
- **Asynchronous Output Enable Input**
- **Programmable Impedance Output Drivers**
- **JTAG boundary scan for BGA packaging version**
- **Available in a 119-ball BGA package (CY7C1330AV25 and CY7C1332AV25)**

Configuration

CY7C1330AV25 – 512K x 36

CY7C1332AV25 – 1M x 18

Functional Description

The CY7C1330AV25 and CY7C1332AV25 are high performance, Synchronous Pipelined SRAMs designed with late write operation. These SRAMs can achieve speeds up to 250 MHz. Each memory cell consists of six transistors.

Late write feature avoids an idle cycle required during the turnaround of the bus from a read to a write.

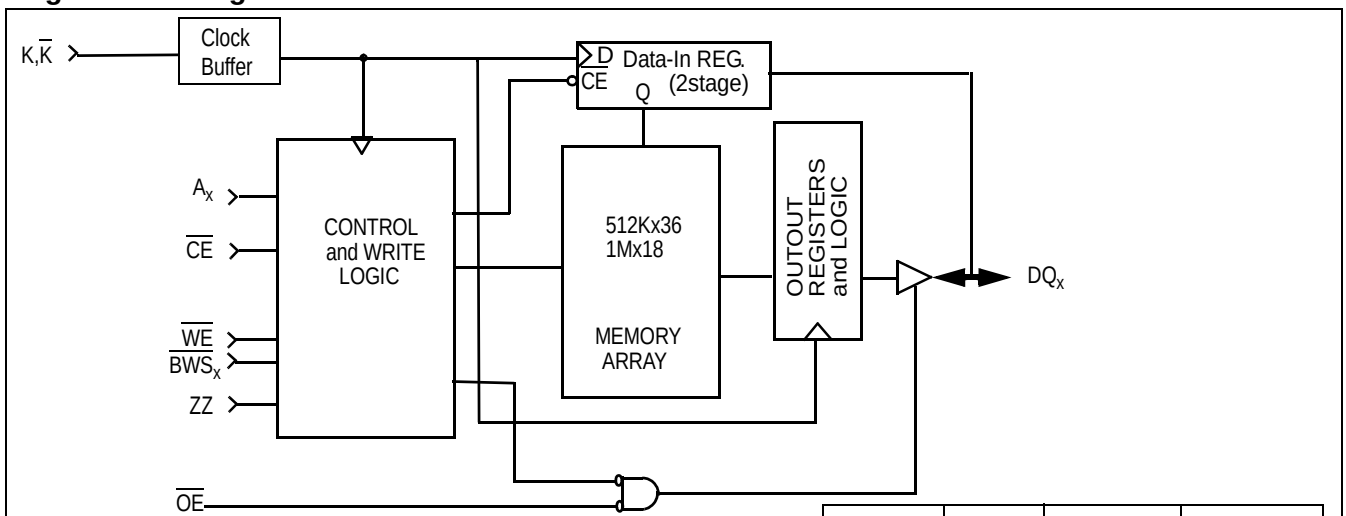
All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (K). The synchronous inputs include all addresses (A), all data inputs ($DQ_{[a:d]}$), Chip Enable ($\overline{CE}$), Byte Write Selects ($\overline{BWS_{[a:d]}}$), and read-write control ($\overline{WE}$). Read or Write Operations can be initiated with the chip enable pin ($\overline{CE}$). This signal allows the user to select/deselect the device when desired.

Power down feature is accomplished by pulling the Synchronous signal ZZ HIGH.

Output Enable ($\overline{OE}$) is an asynchronous input signal. $\overline{OE}$ can be used to disable the outputs at any given time.

Four pins are used to implement JTAG test capabilities. The JTAG circuitry is used to serially shift data to and from the device. JTAG inputs use LVTTL/LVCMOS levels to shift data during this testing mode of operation.

Logic Block Diagram



	A_X	DQ_X	$\overline{BWS_X}$
512Kx36	X = 18:0	X = a, b, c, d	X = a, b, c, d
1Mx18	X = 19:0	X = a, b	X = a, b

Selection Guide

	CY7C1330AV25-250 CY7C1332AV25-250	CY7C1330AV25-200 CY7C1332AV25- 200	Unit
Maximum Access Time	2.0	2.25	ns
Maximum Operating Current	600	550	mA
Maximum CMOS Standby Current	280	260	mA

Pin Configurations

119-Ball BGA (14 x 22 x 2.4 mm)

CY7C1330AV25 (512K x 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	A	A	NC	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_c	DQ_c	V_{SS}	ZQ	V_{SS}	DQ_b	DQ_b
E	DQ_c	DQ_c	V_{SS}	$\overline{CE}$	V_{SS}	DQ_b	DQ_b
F	V_{DDQ}	DQ_c	V_{SS}	$\overline{OE}$	V_{SS}	DQ_b	V_{DDQ}
G	DQ_c	DQ_c	$\overline{BWS_c}$	NC	$\overline{BWS_b}$	DQ_b	DQ_b
H	DQ_c	DQ_c	V_{SS}	NC	V_{SS}	DQ_b	DQ_b
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQ_d	DQ_d	V_{SS}	K	V_{SS}	DQ_a	DQ_a
L	DQ_d	DQ_d	$\overline{BWS_d}$	$\overline{K}$	$\overline{BWS_a}$	DQ_a	DQ_a
M	V_{DDQ}	DQ_d	V_{SS}	$\overline{WE}$	V_{SS}	DQ_a	V_{DDQ}
N	DQ_d	DQ_d	V_{SS}	A0	V_{SS}	DQ_a	DQ_a
P	DQ_d	DQ_d	V_{SS}	A1	V_{SS}	DQ_a	DQ_a
R	NC	A	M_1	V_{DD}	M_2	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1332AV25 (1M x 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	A	A	NC	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_b	NC	V_{SS}	ZQ	V_{SS}	DQ_a	NC
E	NC	DQ_b	V_{SS}	$\overline{CE}$	V_{SS}	NC	DQ_a
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_a	V_{DDQ}
G	NC	DQ_b	$\overline{BWS_b}$	NC	NC	NC	DQ_a
H	DQ_b	NC	V_{SS}	NC	V_{SS}	DQ_a	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQ_b	V_{SS}	K	V_{SS}	NC	DQ_a
L	DQ_b	NC	NC	$\overline{K}$	$\overline{BWS_a}$	DQ_a	NC
M	V_{DDQ}	DQ_b	V_{SS}	$\overline{WE}$	V_{SS}	NC	V_{DDQ}
N	DQ_b	NC	V_{SS}	A0	V_{SS}	DQ_a	NC
P	NC	DQ_b	V_{SS}	A1	V_{SS}	NC	DQ_a
R	NC	A	M_1	V_{DD}	M_2	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Definitions

Name	I/O Type	Description
A	Input-Synchronous	**Address Inputs used to select one of the address locations**. Sampled at the rising edge of the K.
$\overline{BWS_a}$ $\overline{BWS_b}$ $\overline{BWS_c}$ $\overline{BWS_d}$	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BWS_a}$ controls DQ_a, $\overline{BWS_b}$ controls DQ_b, $\overline{BWS_c}$ controls DQ_c, $\overline{BWS_d}$ controls DQ_d.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to initiate a write sequence and high to initiate a read sequence.
K,$\overline{K}$	Input-Differential Clock	**Clock Inputs**. Used to capture all synchronous inputs to the device.
$\overline{CE}$	Input-Synchronous	**Chip Enable Input, active LOW**. Sampled on the rising edge of CLK. Used to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
DQ_a DQ_b DQ_c DQ_d	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[x:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$. DQ a,b,c,d are 9 bits wide
M_1, M_2	Read Protocol Mode Pins	**Mode control pins, used to set the proper read protocol**. For specified device operation, M_1 must be connected to V_{SS}, and M_2 must be connected to V_{DD} or V_{DDQ}. These mode pins must be set at power-up and cannot be changed during device operation.
ZZ	Input-Asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved.
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternately, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**. For this device, the V_{DD} is 2.5V.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**. For this device, the V_{DDQ} is 1.5V.
V_{REF}	Input-Reference Voltage	**Reference Voltage Input**. Static input used to set the reference level for HSTL inputs and Outputs as well as AC measurement points.
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK.
TDI	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK.
TMS	Test Mode Select Synchronous	**This pin controls the Test Access Port state machine**. Sampled on the rising edge of TCK.
TCK	JTAG serial clock	**Serial clock to the JTAG circuit**.
NC	–	**No connects**.

Introduction

Functional Overview

The CY7C1330AV25 and CY7C1332AV25 are synchronous-pipelined Late Write SRAMs running at speeds up to 250 MHz. All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.0 ns (250-MHz device).

Accesses can be initiated by asserting Chip Enable ($\overline{CE}$) on the rising edge of the clock. The address presented to the device will be latched on this edge of the clock. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $BWS_{[d:a]}$ can be used to conduct individual byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed late write circuitry.

All operations (Reads, Writes, and Deselects) are pipelined.

Pipelined Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) Chip Enable ($\overline{CE}$) is asserted active and (2) the Write Enable input signal ($\overline{WE}$) is asserted HIGH. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 2.0 ns (250-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will tri-state following the next clock rise.

Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. The data outputs are provided from the data in registers rather than the memory array. This operation occurs on a byte to byte basis. If only one byte is written during a write operation and a read operation is performed on the same address; then a partial bypass read operation is performed since the new byte data will be from the datain registers while the remaining bytes are from the memory array.

Late Write Accesses

The Late Write feature allows for the write data to be presented one cycle later after the access is started. This feature eliminates one bus-turnaround cycle which is necessary when going from a read to a write in an ordinary pipelined Synchronous Burst SRAM.

Write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}$ is asserted active and (2) the write signal $\overline{WE}$ is asserted LOW. The address presented to A_x is loaded into the Address Register. The write signals are latched into the Control Logic block.

The data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal when a write is detected. This allows the external logic to present the data on DQ and DQP ($DQ_{[a:b]}$ for CY7C1332AV25 and $DQ_{[a:d]}$ for CY7C1330AV25). In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the Address Register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the Write operation is controlled by $\overline{BWS}$ ($\overline{BWS}_{[a:d]}$ for CY7C1330AV25 and $\overline{BWS}_{[a:b]}$ for CY7C1332AV25) signals. The CY7C1330AV25 and CY7C1332AV25 provide byte write capability that is described in the Write Cycle Description table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BWS}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1330AV25/CY7C1332AV25 is a common I/O device, data should not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ inputs. Doing so will tri-state the output drivers. As a safety precaution, DQ is automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Power-up/Power-down Supply Voltage Sequencing

The power-up and power-down supply voltage application recommendations are as follows:

Power-up: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, V_{IN}.

Power-down: V_{IN}, V_{REF}, V_{DDQ}, V_{DD}, V_{SS}.

V_{DDQ} can be applied/removed simultaneously with V_{DD} as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM, The allowable range of RQ to guarantee impedance matching with a tolerance of ±10% is between 175Ω and 350Ω, with V_{DDQ}=1.5V. The output impedance is adjusted every 1024 cycles to adjust for drifts in supply voltage and temperature.The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to V_{DD}.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation

guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Cycle Description Truth Table[1, 2, 3, 4, 5]

Operation	Address Used	$\overline{CE}$	$\overline{WE}$	$\overline{BWS_x}$	CLK	ZZ	Comments
Deselected	External	1	X	X	L-H	0	I/Os tri-state following next recognized clock.
Begin Read	External	0	1	X	L-H	0	Address latched. Data driven out on the next rising edge of the clock.
Begin Write	External	0	0	Valid	L-H	0	Address latched, data presented to the SRAM on the next rising edge of the clock.
Sleep Mode	-	X	X	X	X	1	Power down mode.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{IH}$		128	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{IH}$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq V_{IL}$	$2t_{CYC}$		ns

Write Cycle Descriptions[1, 2]

Function (CY7C1330AV25)	$\overline{WE}$	$\overline{BW_d}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	1	X	X	X	X
Write Byte 0 – DQ_a	0	1	1	1	0
Write Byte 1 – DQ_b	0	1	1	0	1
Write Bytes 1, 0	0	1	1	0	0
Write Byte 2 – DQ_c	0	1	0	1	1
Write Bytes 2, 0	0	1	0	1	0
Write Bytes 2, 1	0	1	0	0	1
Write Bytes 2, 1, 0	0	1	0	0	0
Write Byte 3 – DQ_d	0	0	1	1	1
Write Bytes 3, 0	0	0	1	1	0
Write Bytes 3, 1	0	0	1	0	1
Write Bytes 3, 1, 0	0	0	1	0	0
Write Bytes 3, 2	0	0	0	1	1
Write Bytes 3, 2, 0	0	0	0	1	0
Write Bytes 3, 2, 1	0	0	0	0	1
Write All Bytes	0	0	0	0	0
Abort Write All Bytes	0	1	1	1	1

Write Cycle Descriptions[1, 2]

Function (CY7C1332AV25)	$\overline{WE}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	1	X	X
Write Byte 0 – DQ_a	0	1	0
Write Byte 1 – DQ_b	0	0	1
Write All Bytes	0	0	0
Abort Write All Bytes	0	1	1

Notes:
1. X = “Don't Care,” 1 = Logic HIGH, 0 = Logic LOW. $\overline{BWS_X}$ = 0 signifies at least one Byte Write Select is active, $\overline{BWS_X}$ = Valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by $\overline{WE}$ and $\overline{BWS_X}$. See Write Cycle Description table for details.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal.
4. Device will power-up deselected and the I/Os in a tri-state condition, regardless of $\overline{OE}$.
5. $\overline{OE}$ assumed LOW.

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This port operates in accordance with IEEE Standard 1149.1-1900 but does not have the set of functions required for full 1149.1 compliance. The TAP operates using JEDEC standard 1.8V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Instruction codes). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is given during the “Update IR” state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

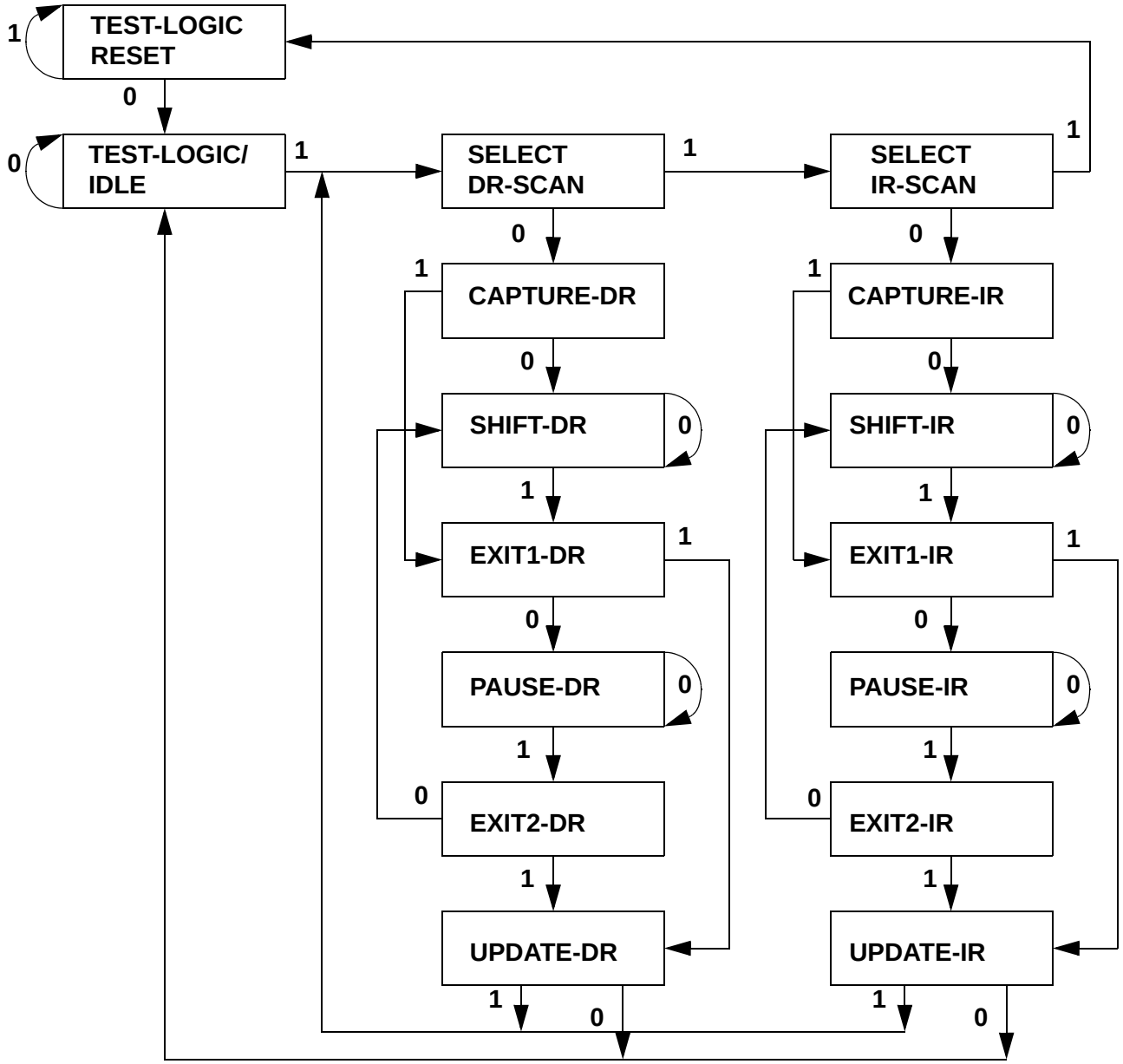
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

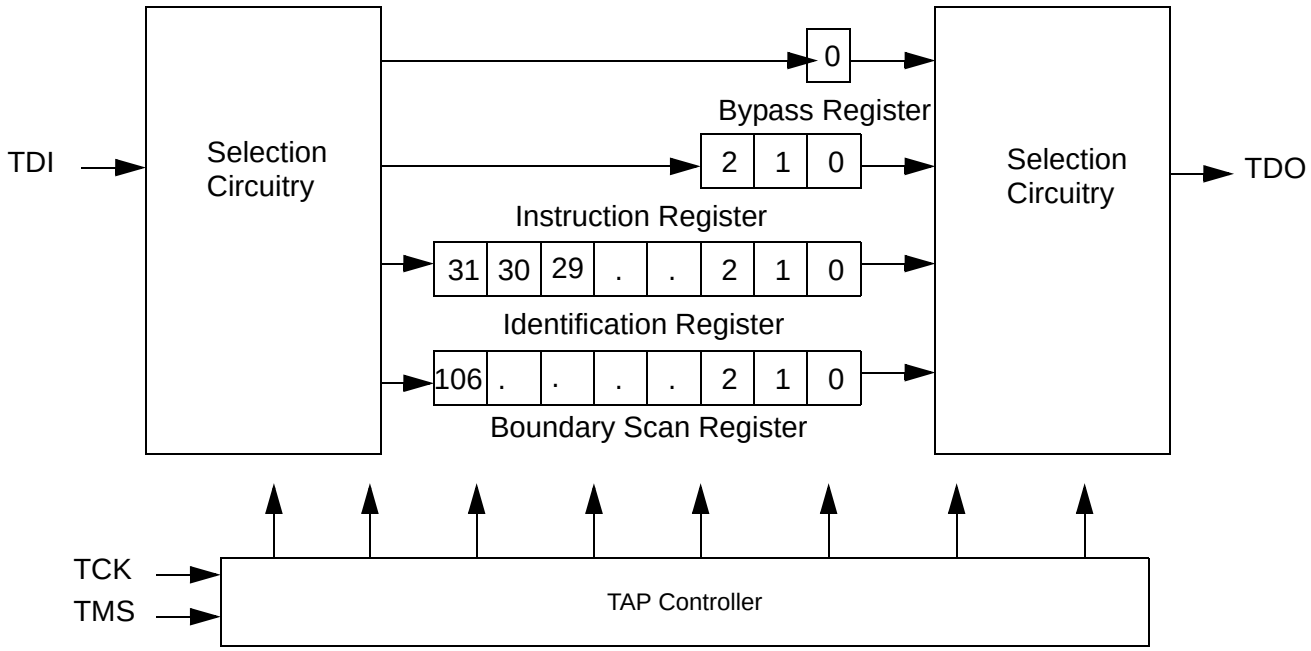
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram[6]



Note:
6. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[7, 8, 9]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA	1.7		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA		0.7	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
I_X	Input and Output Load Current	GND ≤ V_I ≤ V_{DD}	–5	5	µA

TAP AC Switching Characteristics Over the Operating Range [10, 11]

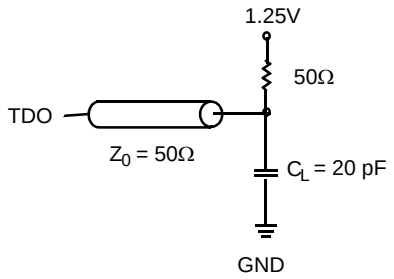
Parameter	Description	Min.	Max.	Unit
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH	20		ns
t_{TL}	TCK Clock LOW	20		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	5		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	5		ns
t_{CS}	Capture Set-up to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns

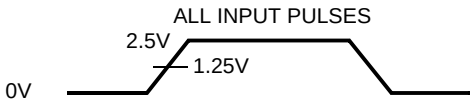
Notes:
7. Minimum voltage equals –2.0V for pulse durations of less than 20 ns.
8. Input waveform should have a slew rate of ≥ 1 V/ns.
9. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics Table.
10. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

TAP AC Switching Characteristics Over the Operating Range (continued)[10, 11]

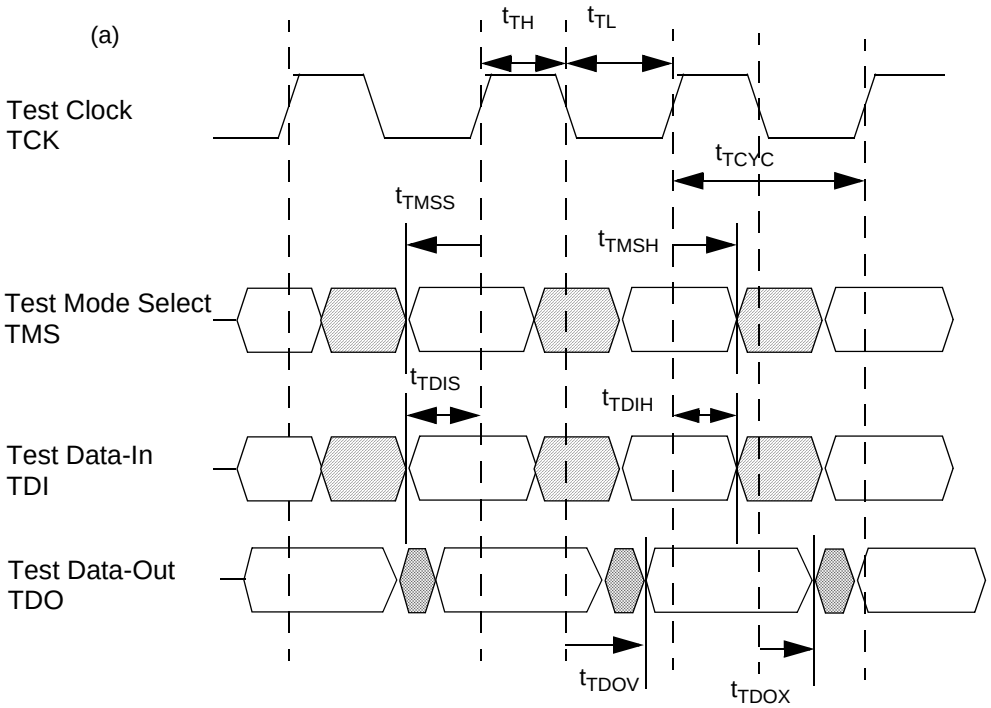
Parameter	Description	Min.	Max.	Unit
t_{CH}	Capture Hold after Clock Rise	5		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

TAP Timing and Test Conditions[11]





(a)



Identification Register Definitions

Instruction Field	Value		Description
	CY7C1330AV25	CY7C1332AV25	
Revision Number (31:29)	000	000	Version number.
Cypress Device ID (28:12)	01011110101100101	01011110101010101	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size—CY7C1330AV25	Bit Size—CY7C1332AV25
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	70	51

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order (1 Mbit x 18)

Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID
1	5R	18	7E	35	1H
2	6T	19	6D	36	3G
3	4P	20	6A	37	4D
4	6R	21	6C	38	4E
5	5T	22	5C	39	4G
6	7T	23	5A	40	4H
7	7P	24	6B	41	4M
8	6N	25	5B	42	2K
9	6L	26	3B	43	1L
10	7K	27	2B	44	2M
11	5L	28	3A	45	1N
12	4L	29	3C	46	2P
13	4K	30	2C	47	3T
14	4F	31	2A	48	2R
15	6H	32	1D	49	4N
16	7G	33	2E	50	2T
17	6F	34	2G	51	3R

Boundary Scan Order (512K x 36)

Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID
1	5R	25	6F	49	2H
2	4P	26	7E	50	1H
3	4T	27	6E	51	3G
4	6R	28	7D	52	4D
5	5T	29	6D	53	4E
6	7T	30	6A	54	4G
7	6P	31	6C	55	4H
8	7P	32	5C	56	4M
9	6N	33	5A	57	3L
10	7N	34	6B	58	1K
11	6M	35	5B	59	2K
12	6L	36	3B	60	1L
13	7L	37	2B	61	2L
14	6K	38	3A	62	2M
15	7K	39	3C	63	1N
16	5L	40	2C	64	2N
17	4L	41	2A	65	1P
18	4K	42	2D	66	2P
19	4F	43	1D	67	3T
20	5G	44	2E	68	2R
21	7H	45	1E	69	4N
22	6H	46	2F	70	3R
23	7G	47	2G		
24	6G	48	1G		

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°°C

Supply Voltage on V_{DD} Relative to GND..... –0.5V to +2.9V

Supply Voltage on V_{DDQ} Relative to GND ..... –0.5V to +V_{DD}

DC Voltage Applied to Outputs in High-Z State[7] ..... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage[7] ..... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 1500V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	2.37V to 2.63V	1.4V to 1.9V

Electrical Characteristics Over the Operating Range

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			2.37	2.63	V
V_{DDQ}	I/O Supply Voltage			1.4	1.9	V
V_{OH1}	Output HIGH Voltage[12]	Programmable Impedance Mode[14]		$V_{DDQ}/2$	V_{DD}	V
V_{OL1}	Output LOW Voltage[13]	Programmable Impedance Mode[14]		V_{SS}	$V_{DDQ}/2$	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –0.1 mA, Minimum Impedance Mode[15]		V_{DDQ} – 0.2	V_{DDQ}	V
V_{OL2}	Output LOW Voltage	I_{OL} = 0.1 mA, Minimum Impedance Mode[15]		V_{SS}	0.2	V
V_{OH3}	Output HIGH Voltage	I_{OH} = –6.0 mA, Minimum Impedance Mode[15]		V_{DDQ} – 0.4	V_{DDQ}	V
V_{OL3}	Output LOW Voltage	I_{OL} = 6.0 mA, Minimum Impedance Mode[15]		V_{SS}	0.4	V
V_{IH}	Input HIGH Voltage			V_{REF} + 0.1	V_{DDQ} + 0.3	V
V_{IL}	Input LOW Voltage[7]			–0.3	V_{REF} – 0.1	V
I_X	Input Leakage Current	GND ≤ V_I ≤ V_{DDQ}		–1	1	mA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–1	1	mA
V_{REF}	Input Reference Voltage	Typical value = 0.75V		0.68	0.95	V
V_{IN}–CLK	Clock Input Reference Voltage			–0.3	V_{DDQ} + 0.3	V
V_{DIF}–CLK	Clock Input Differential Voltage			0.1	V_{DDQ} + 0.3	V
V_{CM}–CLK	Clock Common Mode Voltage	Typical Value =0.75V		0.55	0.95	V
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	250 MHz		600	mA
			200 MHz		550	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	250 MHz		280	mA
			200 MHz		260	mA

AC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		V_{REF} + 0.2	–	V
V_{IL}	Input LOW Voltage		–	V_{REF} – 0.2	V

Notes:
12. I_{OH} = (V_{DDQ}/2)/(RQ/5)±15% for 175Ω ≤ RQ ≤ 350Ω.
13. I_{OL} = (V_{DDQ}/2)/(RQ/5)±15% for 175Ω ≤ RQ ≤ 350Ω.
14. Programmable Impedance Output Buffer Mode. The ZQ pin is connected to V_{SS} through RQ.
15. Minimum Impedance Output Buffer Mode: The ZQ pin is connected directly to V_{SS} or V_{DD}.
16. $T_{Power-up}$: Assumes a linear ramp from 0V to V_{DD} (min.) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

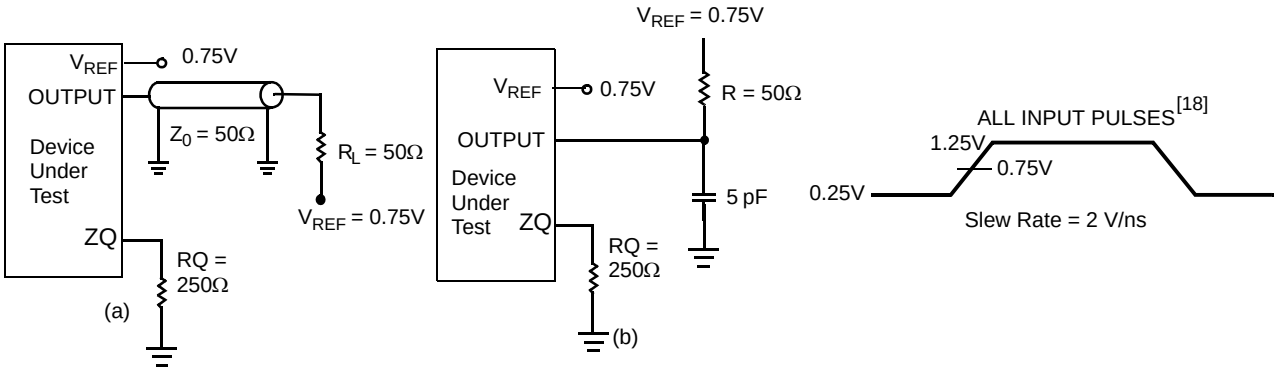
Capacitance[17]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 2.5V V_{DDQ} = 1.5V	5	pF
C_{CLK}	Clock Input Capacitance		6	pF
$C_{I/O}$	Input/Output Capacitance		7	pF

Thermal Resistance[17]

Parameter	Description	Test Conditions	BGA Typ.	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	19.7	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		6.0	°C/W

AC Test Loads and Waveforms



Notes:
17. Tested initially and after any design or process change that may affect these parameters.
18. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75V, V_{REF} = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads.

Switching Characteristics[18, 19, 20, 21]

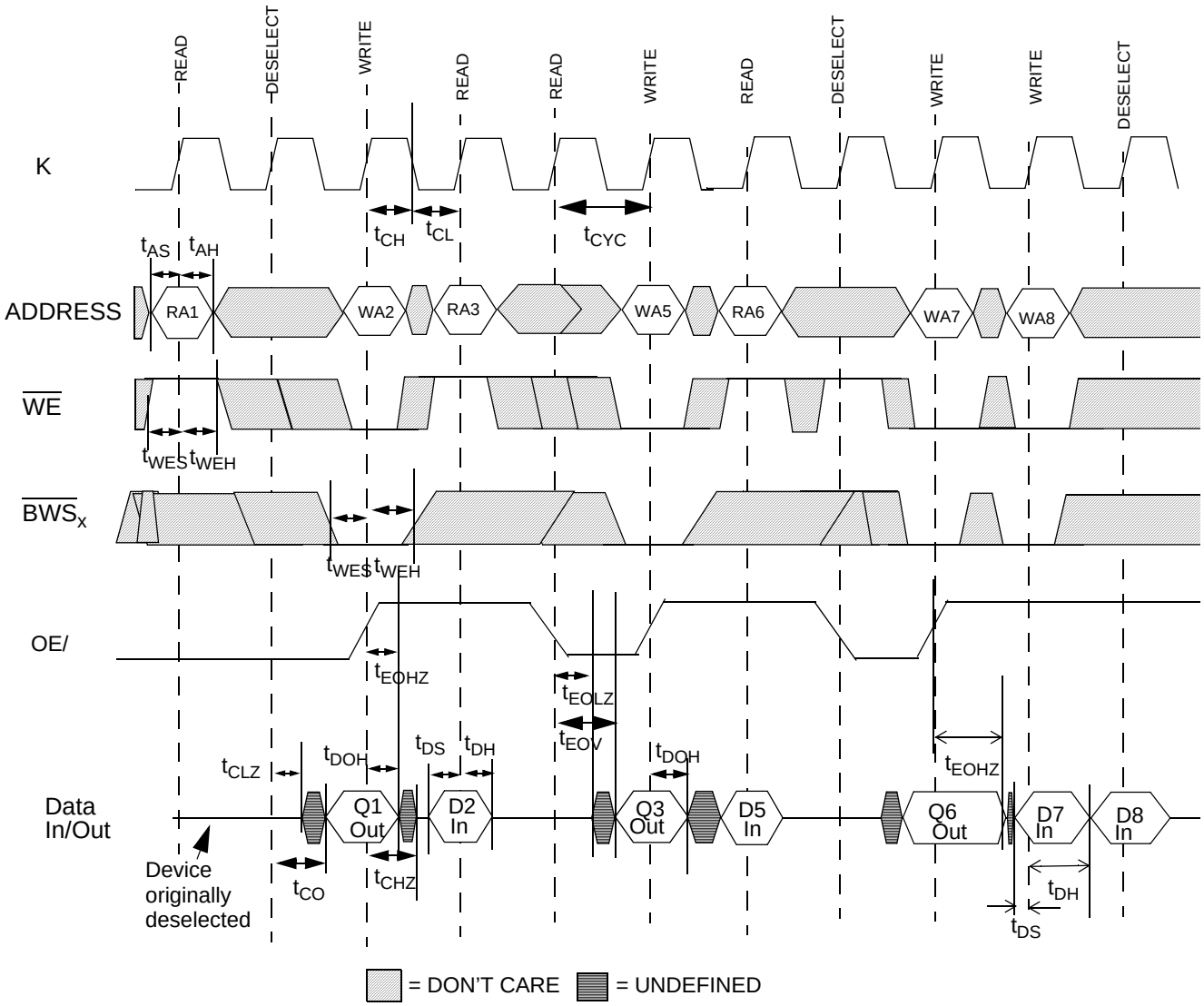
Parameter	Description	250		200		Unit
		Min.	Max.	Min.	Max.	
t_{Power}	V_{CC} (typical) to the First Access Read or Write[22]	1		1		ms
Clock						
t_{CYC}	Clock Cycle Time	4.0		5.0		ns
F_{MAX}	Maximum Operating Frequency		250		200	MHz
t_{CH}	Clock HIGH	1.5		1.5		ns
t_{CL}	Clock LOW	1.5		1.5		ns
Output Times						
t_{CO}	Data Output Valid After CLK Rise		2.0		2.25	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[17, 19, 21]		2.0		2.25	ns
t_{DOH}	Data Output Hold After CLK Rise	0.5		0.5		ns
t_{CHZ}	Clock to High-Z[17, 18, 19, 20, 21]		2.0		2.25	ns
t_{CLZ}	Clock to Low-Z[17, 18, 19, 20, 21]	0.5		0.5		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[18, 19, 21]		2.0		2.25	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[18, 19, 21]	0.5		0.5		ns
Set-Up Times						
t_{AS}	Address Set-Up Before CLK Rise	0.3		0.3		ns
t_{DS}	Data Input Set-Up Before CLK Rise	0.3		0.3		ns
t_{WES}	$\overline{WE}$, $\overline{BWS_X}$ Set-Up Before CLK Rise	0.3		0.3		ns
t_{CES}	Chip Select Set-Up	0.3		0.3		ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.6		0.6		ns
t_{DH}	Data Input Hold After CLK Rise	0.6		0.6		ns
t_{WEH}	$\overline{WE}$, $\overline{BW_X}$ Hold After CLK Rise	0.6		0.6		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.6		0.6		ns

Notes:

19. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 100 mV from steady-state voltage.
20. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
21. This parameter is sampled and not 100% tested.
22. This part has a voltage regulator that steps down the voltage internally; t_{Power} is the time power needs to be supplied above V_{DD} minimum initially before a read or write operation can be initiated.

Switching Waveforms

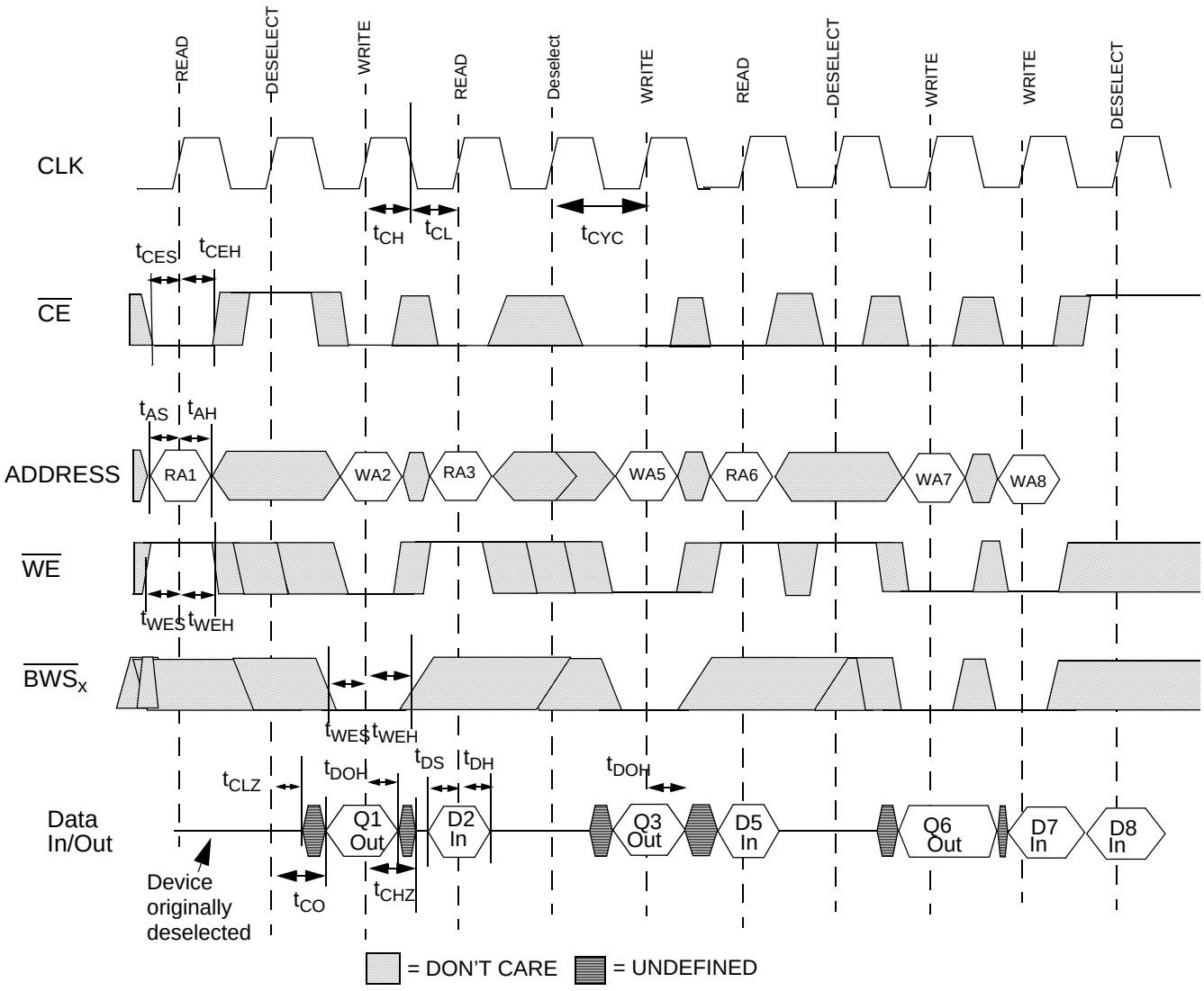
READ/WRITE/DESELECT Sequence ($\overline{OE}$ Controlled)[23, 24, 25, 26]



Notes:
23. The combination of $\overline{WE}$ and $\overline{BWS_x}$ (x = a, b, c, d for x36 and x = a, b for x18) define a write cycle (see Write Cycle Description table).
24. All chip enables need to be active in order to select the device. Any chip enable can deselect the device.
25. $\overline{RA}$x stands for Read Address X, WAx Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X.
26. $\overline{CE}$ held LOW.

Switching Waveforms (continued)

READ/WRITE/DESELECT Sequence ($\overline{CE}$ Controlled)



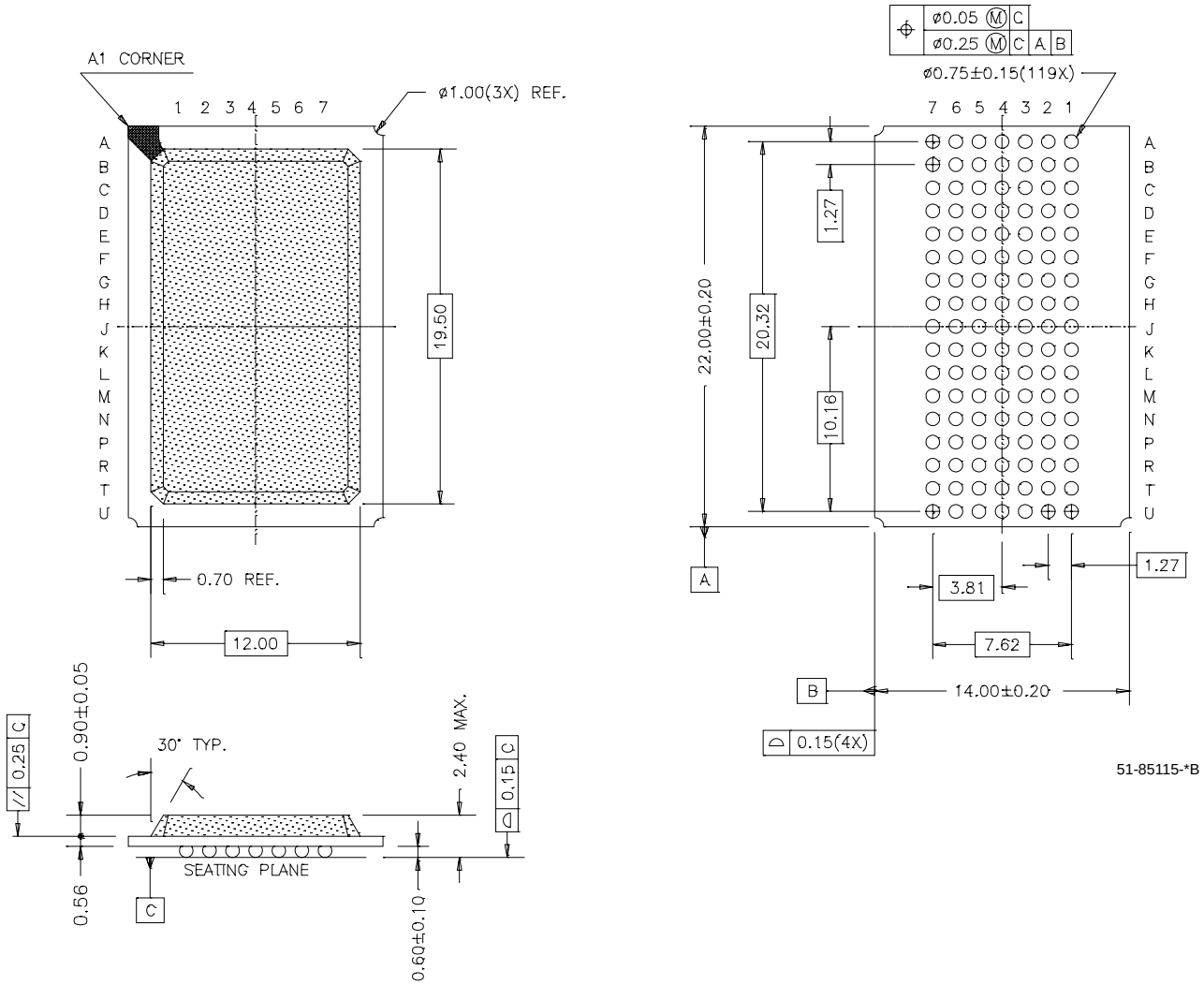
Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
250	CY7C1330AV25-250BGC CY7C1332AV25-250BGC	51-85115	119-ball Fine-Pitch Ball Grid Array (14 x 22 x 2.4 mm)	Commercial
	CY7C1330AV25-250BGXC CY7C1332AV25-250BGXC	51-85115	119-ball Fine-Pitch Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free	
200	CY7C1330AV25-200BGC CY7C1332AV25-200BGC	51-85115	119-ball Fine-Pitch Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1330AV25-200BGXC CY7C1332AV25-200BGXC	51-85115	119-ball Fine-Pitch Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free	

Package Diagram

119-ball PBGA (14 x 22 x 2.4 mm) (51-85115)



All product and company names mentioned in this document are trademarks of their respective holders.

Document History Page

Document Title: CY7C1330AV25/CY7C1332AV25 18-Mbit (512K x 36/1Mbit x 18) Pipelined Register-Register Late Write SRAM Document Number: 001-07844				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	469811	See ECN	NXR	New data sheet
*A	503690	See ECN	VKN	Minor change: Moved data sheet to web