EPSON

S1C33 Family Data Sheets

- S1C33 Family
- S1C33000 Core
- S1C33209
- S1C33T01
- S1C33L01
- S1C33S01
- S1C33221/222
- S1C33240
- S1C33210
- S1C33205/225/226/245
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- S1C33 Family Development Environment
- S1C33 Family Middleware and Firmware
- List of Hardware Resources used by Middleware
- S1C33 Family D/A Technology PCM15
- S1C33 Family S5U1C330R1S Middleware
- S1C33 Family S5U1C330M2S Middleware
- S1C33 Family S5U1C330V1S Middleware
- S1C33 Family S5U1C330M1S Middleware
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- S1C33 Family S5U1C330J1S Middleware
- S1C33 Family S5U1C330C1S Middleware
- S1C33 Family S5U1C330G1S Middleware
- S1C33 Family S5U1C330P1S Middleware
- S1C33 Family S5U1C330H1S Middleware
- S1C33 Family S5U1C330S2S Middleware
- S1C33 Family S5U1C330U1S Middleware
- S1C33 Family S5U1C330G3S Middleware
- S1C33 Family Demonstration and Evaluation Board
- S1C33 Family Tool Selection Guide

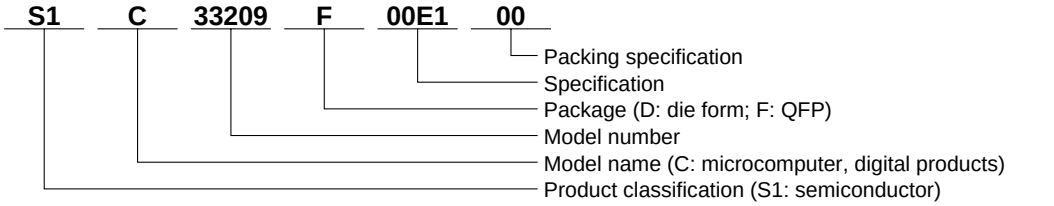
SEIKO EPSON CORPORATION

The information of the product number change

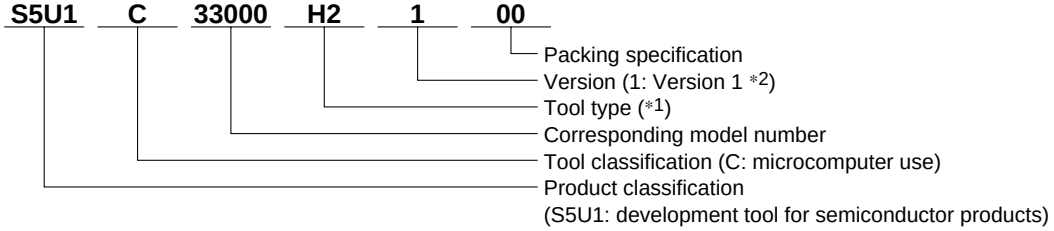
Starting April 1, 2001, the product number has been changed as listed below. Please use the new product number when you place an order. For further information, please contact Epson sales representative.

Configuration of product number

Devices



Development tools



*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)
*2: Actual versions are not written in the manuals.

Comparison table between new and previous number

S1C33 Family processors

Previous No.	New No.
E0C33A104	S1C33104
E0C33202	S1C33202
E0C33204	S1C33204
E0C33208	S1C33208
E0C33209	S1C33209
E0C332T01	S1C33T01
E0C332L01	S1C33L01
E0C332L02	S1C33L02
E0C332S08	S1C33S01
E0C332129	S1C33221
E0C33264	S1C33222
E0C332F128	S1C33240

Previous No.	New No.
CC33	S5U1C33000C
CF33	S5U1C330C1S
COSIM33	S5U1C330C2S
GRAPHIC33	S5U1C330G1S
HMM33	S5U1C330H1S
JPEG33	S5U1C330J1S
MON33	S5U1C330M2S
MELODY33	S5U1C330M1S
PEN33	S5U1C330P1S
ROS33	S5U1C330R1S
SOUND33	S5U1C330S1S
SMT33	S5U1C330S2S
TS33	S5U1C330T1S
USB33	S5U1C330U1S
VOX33	S5U1C330V1S
VRE33	S5U1C330V2S

Comparison table between new and previous number of development tools

Development tools for the S1C33 Family

Previous No.	New No.
ICE33	S5U1C33104H
EM33-4M	S5U1C33104E
PRC33001	S5U1C33104P1
POD33001	S5U1C33104P2
ICD33	S5U1C33000H
DMT33004	S5U1C33104D1
DMT33004PD	S5U1C33104D2
DMT33005	S5U1C33208D1
DMT33005PD	S5U1C33208D2
DMT33006LV	S5U1C33L01D1
DMT33006PDLV	S5U1C33L01D2
DMT33007	S5U1C33208D3
DMT33007PD	S5U1C33208D4
DMT33008LV	S5U1C33T01D1
DMT33008PDLV	S5U1C33T01D2
DMT332S08LV	S5U1C33S01D1
DMT332S08PDLV	S5U1C33S01D2
DMT33209LV	S5U1C33209D1
DMT33209PDLV	S5U1C33209D2
DMT332F128LV	S5U1C33240D1
DMT33MON	S5U1C330M1D1
DMT33MONLV	S5U1C330M2D1
DMT33AMP	S5U1C330A1D1
DMT33AMP2	S5U1C330A2D1
DMT33AMP3	S5U1C330A3D1
DMT33AMP4	S5U1C330A4D1
DMT33CF	S5U1C330C1D1
DMT33CPLD400KLV	S5U1C330C2D1

Previous No.	New No.
DMT33LIF	S5U1C330L1D1
DMT33SMT	S5U1C330S1D1
DMT33LCD26	S5U1C330L2D1
DMT33LCD37	S5U1C330L3D1
EPOD33001	S5U1C33208E1
EPOD33001LV	S5U1C33208E2
EPOD33208	S5U1C33208E3
EPOD33208LV	S5U1C33208E4
EPOD332L01LV	S5U1C33L01E1
EPOD332T01	S5U1C33T01E1
EPOD332T01LV	S5U1C33T01E2
EPOD33209	S5U1C33209E1
EPOD33209LV	S5U1C33209E2
EPOD332128	S5U1C33220E1
EPOD332128LV	S5U1C33220E2
EPOD332S08LV	S5U1C33S01E1
MEM33201	S5U1C33001M1
MEM33201LV	S5U1C33001M2
MEM33202	S5U1C33002M1
MEM33202LV	S5U1C33002M2
MEM33203	S5U1C33003M1
MEM33203LV	S5U1C33003M2
MEM33DIP42	S5U1C330D1M1
MEM33TSOP48	S5U1C330T1M1
EPOD176CABLE	S5U1C33T00E31
EPOD100CABLE	S5U1C33S00E31
EPOD33SRAM5V	S5U1C33000S
EPOD33SRAM3V	S5U1C33001S

EPSON

S1C33 Family

32-bit Single Chip Microcomputer

■ DESCRIPTION

The S1C33 Family microcomputer consists of a Seiko Epson original CMOS 32-bit RISC core, ROM, RAM, DMA, timers, SIO, PLL, A/D and other circuits. Featuring high-speed operation, low power consumption, reduced code size, and multiplication/accumulation function, this product may be used in a wide range of applications, from OA equipment to portable equipment. This product is also available as an ASIC or custom microcomputer.

■ S1C33000 CORE DESCRIPTION

Operating frequency	:	DC to 60MHz (differs depending on the S1C33xxx model)
Instruction set	:	16-bit fixed code size, 105 types of instructions Immediate and addressing mode extension with EXT instruction
Multiplication/accumulation function	:	MAC operation (16 bits × 16 bits + 64 bits → 64 bits) is executed in two cycles
Register set	:	Sixteen 32-bit general-purpose registers, Five 32-bit special registers
Memory space	:	28-bit (256MB) space

■ S1C33 FAMILY GENERAL-PURPOSE MICROCOMPUTER LIST

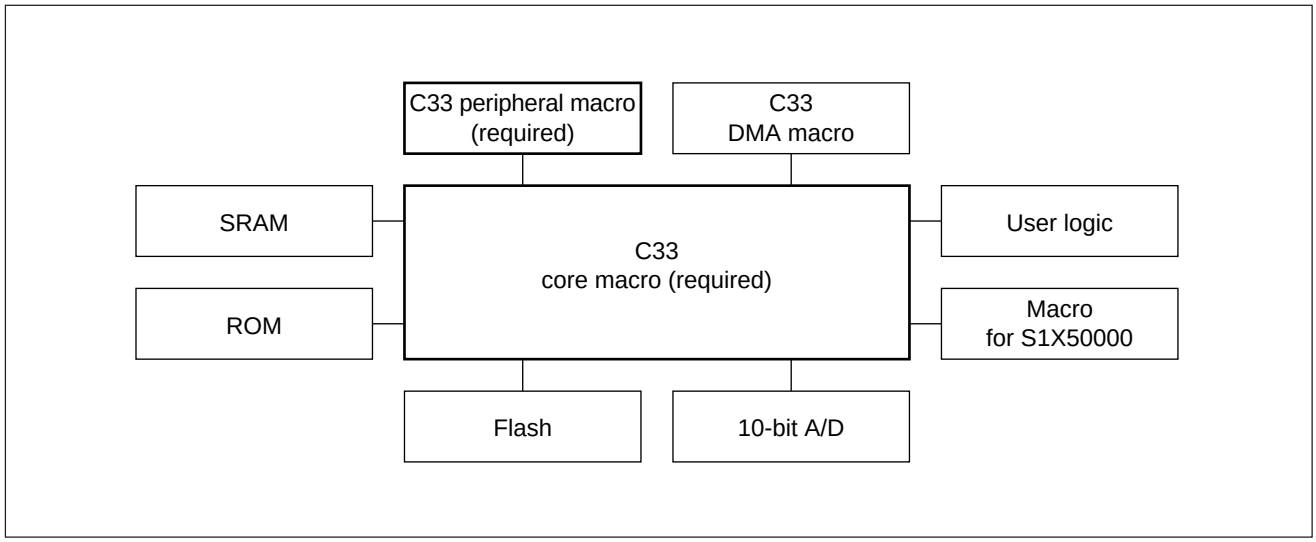
Model	PKG	Voltage(V)		Main clock	PLL	Sub	ROM	RAM	DMA(ch)		SIO	Timer(ch)		RTC	I/O(bit)		A/D	D/A	Others
		Core	I/O	max. frequency		clock	(KB)	(KB)	HS	I	(ch)	16bit	8bit		I	I/O	(ch)	(ch)	
S1C33209	QFP5-128 QFP15-128	1.8 ~3.6	1.8 ~5.5	60MHz(3.3V) 20MHz(2.0V)	x1, x2, x4 selectable	32.768kHz	–	8/4/2	4	128	4	6	6	○	13	29	8	–	–
S1C33L01	QFP18-176	1.8 ~3.6	1.8~5.5 (I/O, Bus) 3.0~5.5 (LCD I/F)	50MHz(3.3V) 20MHz(2.0V)		32.768kHz	128	8 + 40 (VRAM)	4	128	2	6	4	○	13	29	8	–	Built-in LCDC equivalent to S1D13705
S1C33T01	QFP18-176	1.8 ~3.6	1.8~5.5 (I/O, Bus)	60MHz(3.3V) 20MHz(2.0V)		32.768kHz	–	8	4	128	4 + I^2C x 2	10	6	○	13	69	8	–	–
S1C33221	QFP5-128	1.8 ~3.6	1.8 ~5.5	50MHz(3.3V) 20MHz(2.0V)		32.768kHz	128	8	4	128	4	6	6	○	13	29	8	–	–
S1C33222*							64												
S1C33S01	QFP15-100	1.8 ~3.6	Same as core	50MHz(3.3V) 20MHz(2.0V)		32.768kHz	–	8	–		2	6	4	○	–	29	–	–	–
S1C33240*	QFP5-128	2.7 ~3.6	2.7 ~5.5	40MHz(3.3V) 20MHz(Flash access: 0 wait)		32.768kHz	128 (Flash)	8	4	128	4	6	4	○	13	29	8	–	–
S1C33210	QFP15-128	2.7 ~3.6	Same as core	50MHz		32.768kHz	–	8	4	128	3	6	6	○	7	27	4	–	PDC I/F: 1ch PHS I/F: 1ch HDLC: 1ch
S1C33205*	QFP15-128	1.8 ~3.6	1.8 ~5.5	60MHz(3.3V) 20MHz(2.0V)		32.768kHz	–	8	4	128	4	6	6	○	13	29	8	–	–
S1C33225*				50MHz(3.3V) 20MHz(2.0V)			128												
S1C33226*							64												
S1C33245*		2.7 ~3.6	2.7 ~5.5	40MHz(3.3V) 20MHz(Flash access: 0 wait)			128 (Flash)												
S1C33L03*	QFP20-144	1.8 ~3.6	1.8 ~5.5	50MHz(3.3V) 20MHz(2.0V) LCDC: 25MHz(3.3V)		32.768kHz	–	8	4	128	4	6	6	○	13	29	8	–	–

*: Under development (This model is under development, therefore the contents of the above specifications may be revised at final.)

○: Available
– : None

■ S1C33 FAMILY CUSTOM MICROCOMPUTER

Available as a custom microcomputer incorporating S1C33 macros based on the S1X50000 series of Epson embedded arrays.



■ S1C33 FAMILY DEVELOPMENT ENVIRONMENT LIST

● Software Tools

Tool	Description
S5U1C33000C	C compiler package (running under Windows 95/98 and NT4.0) Includes C compiler to debugger and utilities. An evaluation version is also available.
S5U1C330M2S + S5U1C330M1D1 (5V) S5U1C330M2D1 (3.3V)	Debug monitor Enables the creation of an inexpensive debug environment using user resources (ROM 10KB, RAM 2.5KB, SIO 1ch.) to connect to the debugger.

● Basic Hardware Tool

Tool	Description
S5U1C33000H	In-circuit debugger for the S1C33 chip with on-chip ICE This is a reduced-pin connecting-type ICE requiring only 4 or 10 pins for connection.

● Hardware Expansion Tools

Tool	Description
S5U1C33209E1 (5V) S5U1C33209E2 (3.3V)	Emulation pod for the S1C33209 (with emulation memory board I/F) Note) With the capacity to emulate up to 256KB of internal ROM. (maximum 50MHz, 0 wait state)
S5U1C33L01E1 (3.3V)	Emulation pod for the S1C33L01 (with emulation memory board I/F) Note) Supports ROM development using the internal ROM emulation function. (maximum 50MHz, 0 wait state)
S5U1C33T01E1 (5V) S5U1C33T01E2 (3.3V)	Emulation pod for the S1C33T01 (with emulation memory board I/F) Note) With the capacity to emulate up to 256KB of internal ROM. (maximum 50MHz, 0 wait state)
S5U1C33221E1 (5V) S5U1C33221E2 (3.3V)	Emulation pod for the S1C33221 (with emulation memory board I/F) Note) With the capacity to emulate up to 256KB of internal ROM. (maximum 50MHz, 0 wait state)
S5U1C33240E1 (5V) S5U1C33240E2 (3.3V)	Emulation pod for the S1C33240 (with emulation memory board I/F)
S5U1C33S01E1 (3.3V)	Emulation pod for the S1C33S01 (with emulation memory board I/F) Note) With the capacity to emulate up to 256KB of internal ROM. (maximum 50MHz, 0 wait state)
S5U1C330D1M1 (5–3.3V)	ROM emulation I/F board The DIP socket for the target board ROM and the S5U1C33001Mx/S5U1C33002Mx are connected to emulate ROM. It supports ×16 type of 1M, 2M, 4M, 8M, and 16M-bit ROMs in 40 to 42-pin DIPs.
S5U1C33T1M1 (5–3.3V)	Flash emulation I/F board The S5U1C33001Mx/S5U1C33002Mx is connected to the 48-pin TSOP flash memory board pattern on the target board to emulate flash memory. It supports ×16 type of 4M, 8M, 16M, and 32M-bit flash memory in 48-pin TSOPs.
S5U1C33001M1 (5V) S5U1C33001M2 (3.3V)	2MB × 2 block emulation memory board (accessible with 1 wait state up to 33MHz) When two boards are cascaded, up to 2MB × 4 blocks can be emulated. Powerful break functions for a map break, six bus breaks and two area breaks can also be added to the S5U1C33000H (with S5U1C33xxxEx connected).
S5U1C33002M1 (5V) S5U1C33002M2 (3.3V)	1MB emulation memory board (accessible with 1 wait state, up to 33MHz) When two boards are cascaded, up to 1MB × 2 blocks can be emulated.
S5U1C33003M1 (5V) S5U1C33003M2 (3.3V)	2MB × 2 block emulation memory board (accessible with 1 wait state up to 33MHz) When two boards are cascaded, up to 2MB × 4 blocks can be emulated. This board has no flex10k for expanding break functions but other functions are the same as S5U1C33001Mx.

Note: High-speed SRAM for ROM emulation is a rental option.
S5U1C33001S (for 3.3V), S5U1C33000S (for 5V)

● Simulation and Emulation Tools

Tool	Description
S1C33 ASIC design kit	Contains a simulation model for C33-macro and provides a simulation environment required to create custom microcomputers. It is customized to suit the specifications of your custom microcomputer.
S5U1C330C2S	Containing a simulation model for the S1C33209 etc., it provides emulation environment with CPLD, and co-simulation environment via the debugger. Supports software development, also including provisions for external ASIC.

■ S1C33 FAMILY MIDDLEWARE AND FIRMWARE LIST

Classification	Trade name	Contents
Voice	S5U1C330V1S	Voice compression/expansion and voice processing
	S5U1C330G3S	Voice compression/expansion G72SA, G723.1A
	S5U1C330T1S	Simple text to speech
	S5U1C330V2S	Voice recognition
	S5U1C330H1S	High-performance Japanese voice recognition using phoneme model
Sound	S5U1C330M1S	PWM method simple melody output
	S5U1C330S1S	MIDI-like sound output based on WAVE sound source
Image	S5U1C330J1S	JPEG compression/expansion (high-speed version is under development)
	S5U1C330G1S	Graphics and GUI library
	S5U1C330P1S	Japanese handwritten character recognition
OS	S5U1C330R1S	µITRON3.0 compliant real-time OS
Debug tool	S5U1C330M2S	Debug monitor running on user board
	FLS33	On-board/on-chip flash memory erase/programming routine executable using a debugger (included with S5U1C33000C Ver.2.0 or later)
PC I/F	S5U1C330C1S	I/O firmware for compact flash memory Supports DOS file (FAT12/16)
	S5U1C330S2S	DOS file system supporting SmartMedia
	S5U1C330U1S	USB sample program

Evaluation versions are available for all of the above products. Various demonstration version software applications are also available for the demonstration board.

■ S1C33 FAMILY DEMONSTRATION/PROPTOTYPE BOARD LIST

Board name	IC supported	Input voltage Operating voltage	Operating frequency	S5U1C330M2S area	Flash	SRAM	I/F	Bus I/O output	Others
S5U1C33209D1	S1C33209	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–
S5U1C33L01D1 S5U1C33L01D2	S1C33L01	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1 S5U1C330LxD	Bus and I/O pin output	D2 is for S5U1C33L01E1 With 12V, 5 to 28V, -5 to -28V outputs for LCD
S5U1C33T01D1	S1C33T01	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–
S5U1C33S01D1	S1C33S01	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–
S5U1C33240D1	S1C33240	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–
S5U1C33210D1	S1C33210	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–

● Expansion Board

Board name	Power	Function
S5U1C330A3D1	5V	8–32kHz sampling audio input/output board Supports PCM15, stereo output, and S5U1C330M1S piezoelectric buzzer output.
S5U1C330A4D1	5V	Audio input/output board Contains low-cost transistor amplifier supporting PCM15.
S5U1C330L2D1	5V	LCD demonstration board with 2.6-inch DTFD panel (exclusive use for S5U1C33L01D1) Note)
S5U1C330L3D1	5V	LCD demonstration board with 3.7-inch DTFD panel (exclusive use for S5U1C33L01D1) Note)
S5U1C330C1D1	3.3V	Demonstration board for compact flash Connected with a bus connector.
S5U1C330L1D1	3.3 to 5V	I/F board for Agilent Technologies (former HP) 16500A Connected with a bus connector.
S5U1C330S1D1	3.3V	Memory card board for smart medium and S5U1C330S2S Connected with a bus connector.
S5U1C330U1D1	3.3V	Evaluation board for USB macro that can be implemented to ASIC
S5U1C330C2D1	3.3V	ASIC emulation board for Altera APEX20K 400 (400,000 gates) is installed in the socket (default). Interchaneable with 1000 (1,000,000 gates).

Note: A rental board only is available because the quantity is limited.

■ S1C33 STARTUP GUIDE

The following describes available materials and how to use them as references when you examine the type of S1C33 product to choose or when you actually start developing your application system.

1) Collection of S1C33 Family data sheets

First, take a look at the list shown previously to get an overall view of the S1C33 Family, including the types of microcomputers, development tools, middleware, and demonstration boards. For an outline description of each product, see the relevant part of this collection of data sheets. Each type of microcomputer and middleware is outlined in one to several pages.

2) Manuals

When you need detailed information about any microcomputer, development tool, middleware, or demonstration board, refer to the manual for that product. When manuals are needed, please contact Seiko Epson or a local Seiko Epson distributor. Manuals in PDF format are also included in the data CD described in (3) below.

The following lists the typical manuals that are needed first:

- S1C33000 Core CPU Manual
- S1C33 Family C Compiler Package Manual
- S1C33xxx Technical Manual (xxx denotes the microcomputer type which includes, for example, 209 or L01)
- S1C33 Family Application Note

In particular, S1C33 Family Application Note contains information on how to write CPU core and S1C33 programs, as well as S1C33 peripheral function programming, and information on basic circuit board and sound output features. Please be sure to read S1C33 Family Application Note before starting development.

3) S1C33 Family data CD

Obtain the "S1C33 Family data CD" from Seiko Epson.
The following are included. Refer to the necessary data.

- Manuals for all PDFs in the S1C33 Family (in English and Japanese)
- Bug reports (regarding the IC, tools, etc.)
- Circuit diagrams of all demonstration boards (PDF)
- Photographs of all hardware tools and demonstration boards
- Q & A (in Japanese only)
- Patches (e.g., function extensions and bug fixes) for the latest versions of development tools and middleware
- Middleware demonstration software (demonstration samples that can be run after downloading to the demonstration board)
- Evaluation versions of development tools
  Primary tools are included so that you can start development before purchasing tools.
- Evaluation versions of middleware
  Samples, execution files, and PC tools are included. Check this data to see what kinds of samples and tools are available. Note that because binary libraries are not included, you cannot use this data for development purposes using the make utility.

Before starting development, be sure to consult the bug reports for the microcomputer used. Also, because bug reports are updated and/or released from time to time, be sure to get the latest information from Seiko Epson. Bug reports are distributed in the file named "report*date*.exe" (e.g., report00_09_20.exe). When this file is executed, the data is expanded into "c:\s1c33\reprt" in the same form as the data CD.

4) Evaluation of development tools at start of development

Since the S1C33 Family has a wide range of hardware tools available, you may have difficulty choosing the appropriate product for your needs. For help, please refer to "S1C33 Tool Selection Guide", provided in this collection of data sheets, when choosing the desired tool.

Also, we recommend installing the evaluation versions of development tools from the S1C33 Family data CD to your computer following instructions from Chapter 2, "Installation", in the S1C33 Family C Compiler Package Manual, and run them according to Section 3.2, "Tutorial". This will help you get accustomed to the series of operations needed for a range of tools from the C compiler to the debugger. The debugger's simulator facility allows you to perform a series of processing functions—compiling, assembling, linking, and debugging—without using the ICE or target board.

Furthermore, looking over the S1C33 Family Application Note will prove helpful.

5) Middleware evaluation

The S1C33 middleware made by Seiko Epson has a demonstration version that can be run on the demonstration board for evaluation purposes. Install the demonstration software from the S1C33 Family data CD to your computer by executing the file. Prepare the necessary demonstration board or equivalent, and download the demonstration software to the demonstration board, following the instructions in the readme file. Note that the evaluation version of middleware is included in the data CD, although it cannot be used in actual development.

When using middleware, please also refer to "List of Hardware Resources used by Middleware" in this collection of data sheets. Although you need to read the respective manuals to obtain details on middleware, this list helps you get outline information on hardware resources used by each middleware. Resource assignments are important items to consider when designing your application board.

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EPSON

S1C33000 Core

32-bit Single Chip Microcomputer

- 32-bit RISC Core
- High-code-efficient Instruction Set
- Multiplication and Accumulation Instruction
- High-speed Operation and Low Current Consumption

■ DESCRIPTION

The S1C33000 is a 32-bit RISC-type core CPU for the S1C33 Family microprocessors. The S1C33 Family will be developed using this core as the main unit and implementing various peripheral circuits such as RAM, ROM, DMA, A/D and D/A converters. The S1C33000 core has a high-code efficient instruction set, MAC (multiplication and accumulation) instruction and features high-speed operation and low current consumption. It is suitable for a wide range of embedded applications such as portable equipment, OA and FA equipment, digital signal processing systems and various controllers.

■ FEATURES

- Processor type ..... Seiko Epson original 32-bit RISC core
- Operating frequency ..... DC to 60MHz (differs depending on the S1C33xxx model)
- Instruction set ..... 16-bit fixed code size
  105 types of instructions with high linearity
  Principle instructions can be executed in one cycle.
- Multiplication and accumulation instruction .... MAC instruction (16 bits × 16 bits + 64 bits → 64 bits)
  Executable in two cycles per operation
- Register set ..... Sixteen 32-bit general-purpose registers
  Five 32-bit special registers
- Memory space ..... 28-bit (256MB) space
  A linear space including code, data and I/O areas.
  The memory space is divided into 19 areas and they can be accessed with the select signals delivered from the core.
- Immediate data extension ..... Immediate data in the instruction codes can be extended up to 32 bits using the EXT instruction.
- Interrupts ..... Reset, NMI and 216 external interrupts
  Four software exceptions and two instruction execution exceptions
  The core fetches vectors in the trap table to branch processing.
- Reset ..... Cold reset (for resetting all conditions)
  Hot reset (resetting except for bus and port status)
  Trap table is selectable from internal or external memory when booting and is relocatable.
- Power down mode ..... HALT instruction (stops the core only.)
  SLP instruction (stops all the circuits.)
- Others ..... Little endian/Big endian format
  Harvard architecture

■ MEMORY MAP AND TRAP TABLE

Memory Map

			Area size
0xFFFFFFF	Area 18	External memory	64MB
	Area 17	External memory	64MB
	Area 16	External memory	32MB
	Area 15	External memory	32MB
	Area 14	External memory	16MB
	Area 13	External memory	16MB
	Area 12	External memory	8MB
0x1000000	Area 11	External memory	8MB
0x0C00000	Area 10	External memory	4MB
	Area 9	External memory	4MB
	Area 8	External memory	2MB
	Area 7	External memory	2MB
	Area 6	External I/O	1MB
	Area 5	External memory	1MB
0x0100000	Area 4	External memory	1MB
0x0080000	Area 3	On-chip ROM	512KB
0x0060000	Area 2	Reserved	128KB
0x0040000	Area 1	Internal I/O	128KB
0x0000000	Area 0	On-chip RAM	256KB

Trap Table

	Address offset
Reserved	1023
External maskable interrupt 215	929
:	
External maskable interrupt 0	64
Software exception 3	60
:	
Software exception 0	48
Reserved	32–44
NMI	28
Address error	24
Reserved	20
Zero division	16
Reserved	4–12
Reset	0

Trap table start address
When booting from built-in ROM: 0x0080000
When booting from external memory: 0x0C00000
The trap table can be relocated using the trap table base register TTBR (memory-mapped register) after resetting the CPU.
Vectors will be fetched from the trap table for booting and interrupts.

■ REGISTERS

General-purpose registers (16)

31	0
R15	
R14	
:	
R1	
R0	

Special registers (5)

31	0	
PC		Program counter
PSR		Processor status register
SP		Stack pointer
ALR		Arithmetic operation low register
AHR		Arithmetic operation high register

(AHR, ALR: Option for Multiplication & Accumulation, Multiplication, and Division)

■ INSTRUCTION SET

● Instruction Format and Operation

∗ The cycle lists the number of execution cycles assuming that the instructions are stored in the built-in ROM and access to the built-in RAM.
∗ Sample format: signX and immX = immediate data, %XX = register

Classification	Instruction	Sample format	Operation	Cycle
Relative branch	jp, jrgt, jrge, jrlt, jrle, jrugt, jruge, jrult, jrule, jreq, jrne, call	jp sing8	Branches to PC + (sign8 × 2)	1,2 (branch) or 3 (call)
Relative delayed branch	jp.d, jrgt.d, jrge.d, jrlt.d, jrle.d, jrugt.d, jruge.d, jrult.d, jrule.d, jreq.d, jrne.d, call.d	jp.d sing8	Branches to PC + (sign8 × 2) Executes the next instruction before branching.	1 or 2 (call)
Absolute branch	call, jp, call.d, jp.d	call %rb	Branches to the address indicated with %rb.	1 to 3
Special branch	ret, ret.d, int imm2, reti, brk, retb		Return, interrupt, etc.	3 to 10
Logic operation	and, or, xor, not	and %rd, %rs and %rd, sign6	%rd = %rd & %rs %rd = %rd & sign6	1

Arithmetic operation	add, sub	add %rd, %rs
		add %rd, imm6
		add %sp, imm12
			%rd = %rd + %rs
			%rd = %rd + imm6
			%sp = %sp + imm12
				1

Classification	Instruction	Sample format	Operation	Cycle
Comparison	cmp	cmp %rd, %rs cmp %rd, sign6	%rd - %rs (changes the flags only) %rd - sign6	1
Operation with carry	adc, sbc	adc %rd, %rs	%rd = %rd + %rs + carry flag	1
Multiplication	mlt.h, mlt.uh (16 bits) mlt.w, mlt.uw (32 bits)	mlt.h %rd, %rs	%alr = %rd × %rs (32 = 16 × 16) %ahr:%alr = %rd × %rs (64 = 32 × 32)	1 5
Division	div0s, div0u, div1, div2s, div3s		Division is performed according to a combination of these instructions.	1
Shift	srl, sll (logical shift) sra, sla (arithmetical shift) rr, rl (rotate)	srl %rd, imm4 srl %rd, %rs	%rd = %rd >> imm4 %rd = %rd >> %rs 0 to 8 shift count can be specified.	1
Memory data load	ld.b (signed 8-bit load) ld.ub (unsigned 8-bit load) ld.h (signed 16-bit load) ld.uh (unsigned 16-bit load) ld.w (32-bit load)	ld.w %rd, [%sp+imm6] ld.w [%sp+imm6], %rs ld.w %rd, [%rb] ld.w %rd, [%rb]+ ld.w [%rb], %rs ld.w [%rb]+, %rs	%rd = [%sp+imm6] (stack relative access) [%sp+imm6] = %rs %rd = [%rb] (register indirect access) %rd = [%rb], %rb = %rb + 4 (post inc.) [%rb] = %rs [%rb] = %rs, %rb = %rb + 4	1 or 2
Register data load	ld.w	ld.w %rd, %rs ld.w %rd, sign6 ld.w %rd, %ss ld.w %ss, %rs	Copy between registers Immediate data substitution Copy from a special register Copy to a special register	1
Conversion	ld.b, ld.ub, ld.h, ld.uh	ld.b %rd, %rs	Type conversion	1
Bit	btst, bset, bclr, bnot	btst [%rb], imm3	Bit test, set, clear and negation	3
System	nop, slp, hlt		No operation, clock stop	1
MAC	mac		Repeats <%ahr:%alr= [%r14] × [%r15] + %ahr:%alr> %r13 times.	2 × N + 4
Stack	pushn, popn	pushn %rs	Continuous push/pop from %r0 to %rs	1 × N
Scan	scan0, scan1	scan0 %rd, %rs	Gets the length of 0s or 1s within 8 bits from MSB.	1
Swap	swap, miror	swap %rd, %rs	Bit swap, mirror operation in 8-bit units	1
Extension	ext	ext imm13	Extends immediate data in the instruction.	1

● Immediate Extension with EXT Instruction

Examples)

Original instruction	Extension with one EXT	Extension with two EXTs
call sign8	ext imm13 call sign8 (= call sign21)	ext imm13 ext imm13 call sign8 (= call sign31)

Classification	Instruction	Original format	Extended operation with one EXT	Extended operation with two EXTs
Relative branch	jp,jrgt,jrge,jrlt jrle,jrugt,jruge,jrult,jrule, jreq,jrne,call and delayed instructions	jp sing8	jp sign21	jp sign31
3-operand operation	add, sub, and, or, xor, not, cmp	add %rd, %rs	add %rd, %rs, imm13 Operand extension	add %rd, %rs, imm26 Operand extension
Operation	add, sub, and, or, xor, not, cmp, ld.w	add %rd, imm6 /sign6	add %rd, imm19/sign19	add %rd, imm32
Stack load	ld.b, ld.ub, ld.h, ld.uh, ld.w	ld.w %rd, [%sp+imm6] ld.w [%sp+imm6], %rs	[%sp+imm19] Offset extension	[%sp+imm32] Offset extension
Absolute load	ld.b, ld.ub, ld.h, ld.uh, ld.w	ld.w %rd, [%rb] ld.w %rd, [%rb]+ ld.w [%rb], %rs ld.w [%rb]+, %rs	[%rb+imm13] Offset addition	[%rb+imm28] Offset addition
Bit	btst, bset, bclr, bnot	btst [%rb], imm3	[%rb+imm13] Offset addition	[%rb+imm26] Offset addition

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EPSON

S1C33209

32-bit Single Chip Microcomputer

- 32-bit S1C33000 RISC Core
- Multiply Accumulation
- Built-in 8K-byte RAM
- 10-bit ADC
- 4-ch. SIO
- High-speed DMA, Intelligent DMA

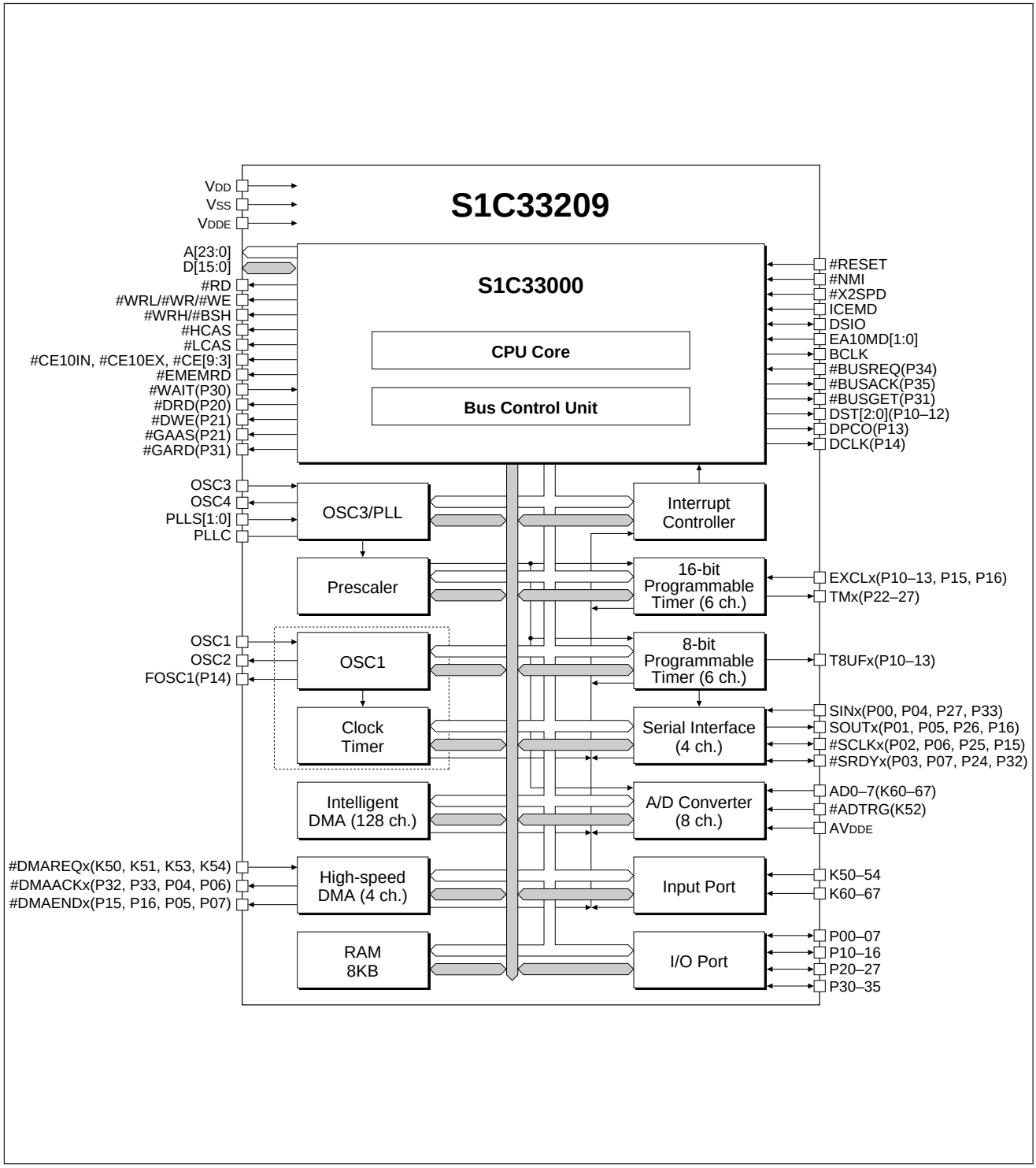
■ DESCRIPTION

The S1C33209 is a CMOS 32-bit microcomputer composed of a CMOS 32-bit RISC core, 8K-byte RAM, 4-channel SIO, A/D converter, timers, PLL and other circuits. The S1C33209 features high-speed operation and low current consumption. It is suitable for various portable equipment and multimedia control systems. The S1C33209 also provides a DSP function using the internal MAC (multiplication and accumulation) operation function with the A/D converter, this makes it possible to achieve speech recognition and voice synthesis systems.

■ FEATURES

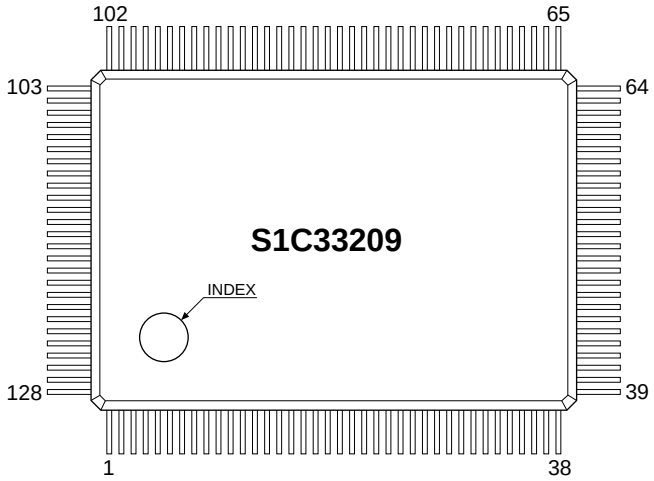
- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC core
- Main clock ..... 60MHz (Max., up to 15MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... 8,192 bytes
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 6 channels and 16 bits × 6 channels
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 4 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits
  I/O port : 29 bits
- Interrupt controller ..... External interrupts : 10 types
  Internal interrupts : 29 types
- External bus interface ..... 24-bit address bus, 16-bit data bus, 7 chip enable pins
  DRAM and burst ROM may be connected directly.
- Shipping form QFP5-128pin/QFP15-128pin
- Supply voltage ..... Core voltage : 1.8 to 3.6V
  I/O voltage : 1.8 to 5.5V
- Current consumption ..... SLEEP state : 10µA (3.3V, 32.768kHz, clock timer run state, Typ.)
  : 2.5µA (2.0V, 32.768kHz, clock timer run state, Typ.)
  RUN state : 65mA (3.3V, 50MHz Typ.)

■ BLOCK DIAGRAM



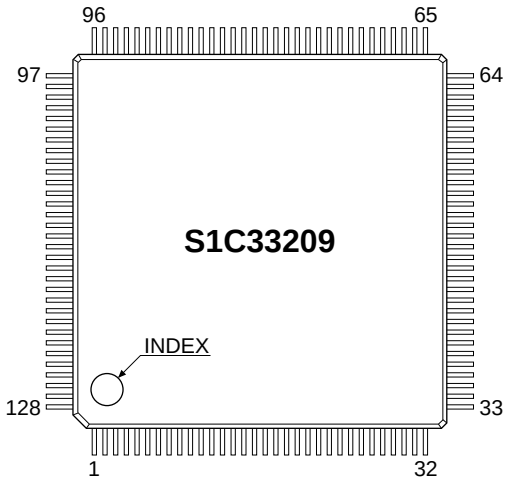
■ PIN LAYOUT

QFP5-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P24/TM2/#SRDY2	33	K65/AD5	65	#RESET	97	A16
2	VSS	34	K50/#DMAREQ0	66	#NMI	98	ICEMD
3	P25/TM3/#SCLK2	35	K64/AD4	67	A0/#BSL	99	A17
4	P26/TM4/SOUT2	36	K63/AD3	68	A1	100	A18
5	P15/EXCL4/#DMAEND0/#SCLK3	37	K62/AD2	69	P34/#BUSREQ/#CE6	101	A19
6	P27/TM5/SIN2	38	AVDDE	70	VSS	102	P04/SIN1/#DMAACK2
7	BCLK	39	K61/AD1	71	A2	103	P05/SOUT1/#DMAEND2
8	P00/SIN0	40	K60/AD0	72	A3	104	P06/#SCLK1/DMAACK3
9	P01/SOUT0	41	D6	73	A4	105	VSS
10	D15	42	VSS	74	A5	106	PLLC
11	VDD	43	D5	75	A6	107	VSS
12	P03/#SRDY0	44	D4	76	#CE10IN	108	PLLS1
13	D14	45	D3	77	VDD	109	PLLS0
14	P31/#BUSGET/#GARD	46	D2	78	#EMEMRD	110	P07/#SRDY1/#DMAEND3
15	D13	47	D1	79	A7	111	#X2SPD
16	P32/#DMAACK0/#SRDY3	48	D0	80	#HCAS	112	EA10MD0
17	D12	49	P35/#BUSACK	81	A8	113	EA10MD1
18	P33/#DMAACK1/SIN3	50	VDDE	82	#LCAS	114	VDD
19	D11	51	#CE9/#CE17/#CE17&18	83	A9	115	(No Connection)
20	K54/#DMAREQ3	52	OSC2	84	P16/EXCL5/#DMAEND1/SOUT3	116	OSC4
21	D10	53	#CE7/#RAS0/#CE13/#RAS2	85	A10	117	P20/#DRD
22	K53/#DMAREQ2	54	OSC1	86	A20	118	OSC3
23	D9	55	#CE6/#CE7&8	87	A11	119	P21/#DWE/#GAAS
24	K52/#ADTRG	56	#RD	88	A21	120	#CE3
25	VSS	57	VSS	89	A12	121	P22/TM0
26	K51/#DMAREQ1	58	#WRL/#WR/#WE	90	A22	122	P23/TM1
27	P02/#SCLK0	59	#WRH/#BSH	91	A13	123	DSIO
28	D8	60	#CE10EX/#CE9&10EX	92	A23	124	P10/EXCL0/T8UF0/DST0
29	D7	61	#CE8/#RAS1/#CE14/#RAS3	93	VSS	125	P11/EXCL1/T8UF1/DST1
30	VDDE	62	#CE5/#CE15/#CE15&16	94	A14	126	P12/EXCL2/T8UF2/DST2
31	K67/AD7	63	#CE4/#CE11/#CE11&12	95	A15	127	P13/EXCL3/T8UF3/DPCO
32	K66/AD6	64	P30/#WAIT/#CE4&5	96	VDDE	128	P14/FOSC1/DCLK

QFP15-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P26/TM4/SOUT2	33	K63/AD3	65	A1	97	A18
2	P15/EXCL4/#DMAEND0/#SCLK3	34	K62/AD2	66	P34/#BUSREQ/#CE6	98	A19
3	P27/TM5/SIN2	35	AVDDE	67	VSS	99	P04/SIN1/#DMAACK2
4	BCLK	36	K61/AD1	68	A2	100	P05/SOUT1/#DMAEND2
5	P00/SIN0	37	K60/AD0	69	A3	101	P06/#SCLK1/DMAACK3
6	P01/SOUT0	38	D6	70	A4	102	VSS
7	D15	39	VSS	71	A5	103	PLLC
8	VDD	40	D5	72	A6	104	VSS
9	P03/#SRDY0	41	D4	73	#CE10IN	105	PLLS1
10	D14	42	D3	74	VDD	106	PLLS0
11	P31/#BUSGET/#GARD	43	D2	75	#EMEMRD	107	P07/#SRDY1/#DMAEND3
12	D13	44	D1	76	A7	108	#X2SPD
13	P32/#DMAACK0/#SRDY3	45	D0	77	#HCAS	109	EA10MD0
14	D12	46	P35/#BUSACK	78	A8	110	EA10MD1
15	P33/#DMAACK1/SIN3	47	VDDE	79	#LCAS	111	VDD
16	D11	48	#CE9/#CE17/#CE17&18	80	A9	112	(No Connection)
17	K54/#DMAREQ3	49	OSC2	81	P16/EXCL5/#DMAEND1/SOUT3	113	OSC4
18	D10	50	#CE7/#RAS0/#CE13/#RAS2	82	A10	114	P20/#DRD
19	K53/#DMAREQ2	51	OSC1	83	A20	115	OSC3
20	D9	52	#CE6/#CE7&8	84	A11	116	P21/#DWE/#GAAS
21	K52/#ADTRG	53	#RD	85	A21	117	#CE3
22	VSS	54	VSS	86	A12	118	P22/TM0
23	K51/#DMAREQ1	55	#WRL/#WR/#WE	87	A22	119	P23/TM1
24	P02/#SCLK0	56	#WRH/#BSH	88	A13	120	DSIO
25	D8	57	#CE10EX/#CE9&10EX	89	A23	121	P10/EXCL0/T8UF0/DST0
26	D7	58	#CE8/#RAS1/#CE14/#RAS3	90	VSS	122	P11/EXCL1/T8UF1/DST1
27	VDDE	59	#CE5/#CE15/#CE15&16	91	A14	123	P12/EXCL2/T8UF2/DST2
28	K67/AD7	60	#CE4/#CE11/#CE11&12	92	A15	124	P13/EXCL3/T8UF3/DPCO
29	K66/AD6	61	P30/#WAIT/#CE4&5	93	VDDE	125	P14/FOSC1/DCLK
30	K65/AD5	62	#RESET	94	A16	126	P24/TM2/#SRDY2
31	K50/#DMAREQ0	63	#NMI	95	ICEMD	127	VSS
32	K64/AD4	64	A0/#BSL	96	A17	128	P25/TM3/#SCLK2

EPSON

S1C33T01

32-bit Single Chip Microcomputer

- High-speed 32-bit RISC Core
- Multiply Accumulation
- 8K-byte RAM Built-in
- 10-bit ADC
- 4-ch. SIO, 2-ch. I^2C
- High-speed DMA, Intelligent DMA

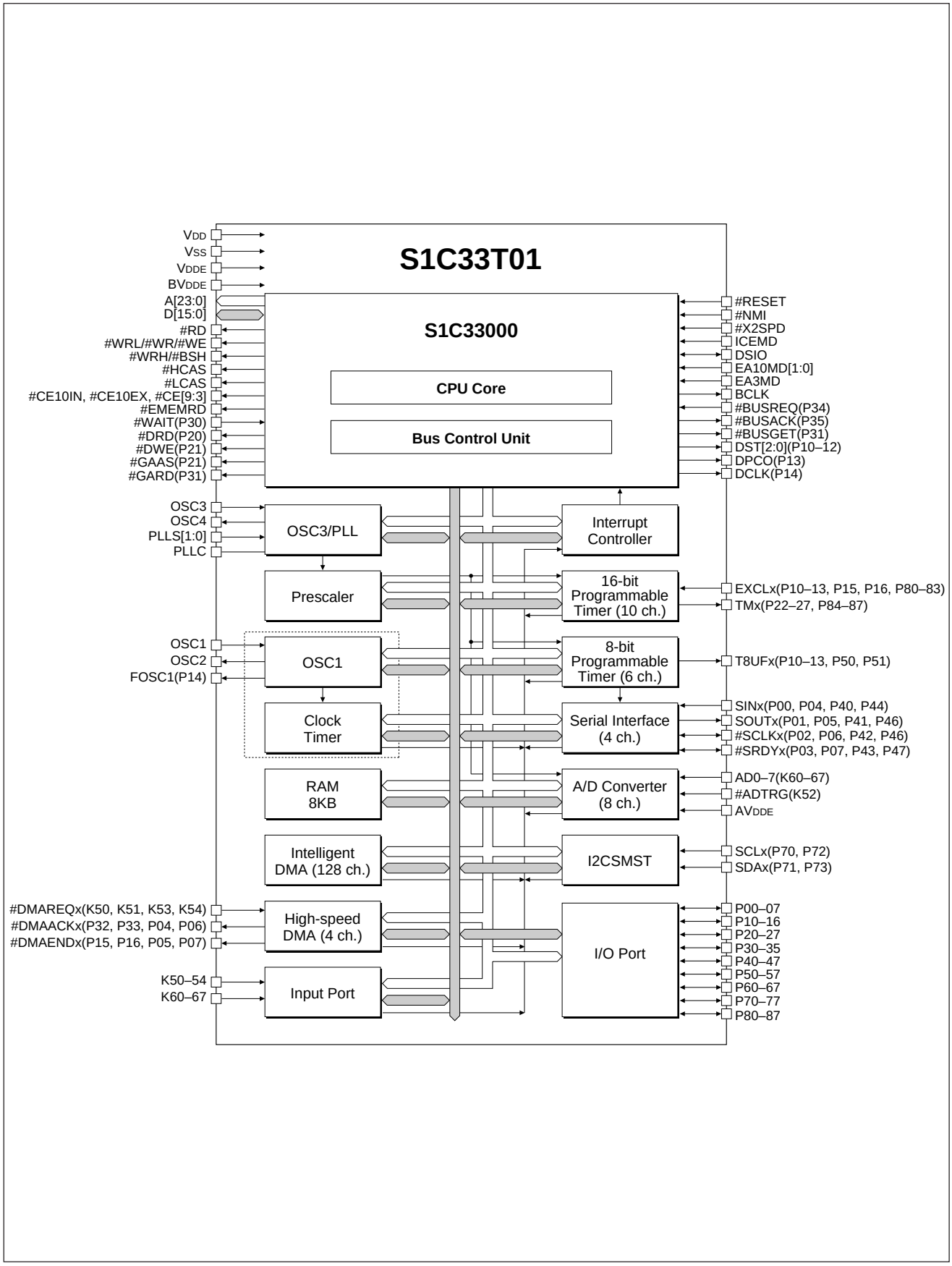
■ DESCRIPTION

The S1C33T01 is a CMOS 32-bit microcomputer composed of a CMOS 32-bit RISC core, 8K-byte RAM, DMA, 4-ch. SIO, 2-ch. I^2C, ADC, timers, PLL and oscillators. The S1C33T01 features high-speed operation and low current consumption. The S1C33T01 also provides a DSP function using the internal MAC (multiplication and accumulation) operation function with the A/D converter, this makes it possible to achieve speech recognition and voice synthesis systems.

■ FEATURES

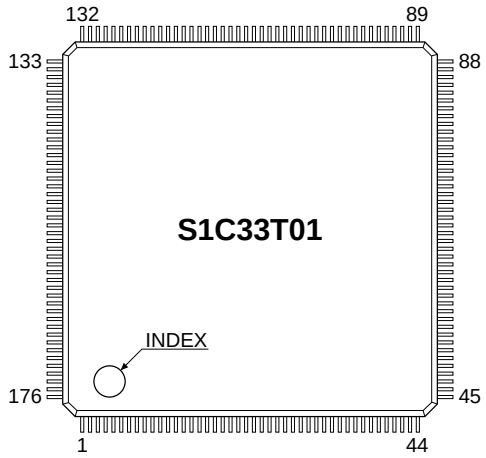
- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC core
- Main clock ..... 60MHz (Max., up to 15MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... 8,192 bytes
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 6 channels and 16 bits × 10 channels
- PWM timer ..... Realized with a 16-bit programmable timer
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 4 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
- I^2C bus ..... Single master type, 2 channels (option)
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits
  I/O port : 69 bits
- Interrupt controller ..... External interrupts : 18 types
  Internal interrupts : 69 types
- External bus interface ..... 24-bit address bus, 16-bit data bus, 7 chip enable pins
  DRAM and burst ROM may be connected directly.
- Shipping form QFP18-176pin
- Supply voltage ..... Core voltage : 1.8 to 3.6V
  I/O voltage : 1.8 to 5.5V
- Current consumption ..... SLEEP state : 10µA (3.3V, 32.768kHz, clock timer run state, Typ.)
  : 2.5µA (2.0V, 32.768kHz, clock timer run state, Typ.)
  RUN state : 65mA (3.3V, 50MHz Typ.)

■ BLOCK DIAGRAM



■ PIN LAYOUT

QFP18-176pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	#X2SPD	45	P35/#BUSACK	89	A16	133	P71/SDA0
2	EA10MD1	46	P34/#BUSREQ/#CE6	90	A17	134	P70/SCL0
3	EA10MD0	47	P31/#BUSGET/#GARD	91	A18	135	#NMI
4	EA3MD	48	P30/#WAIT/#CE4&5	92	A19	136	PLLS1
5	P47/#SRDY3	49	P21/#DWE/#GAAS	93	A20	137	PLLS0
6	P46/#SCLK3	50	P20/#DRD	94	A21	138	#RESET
7	P45/SOUT3	51	#CE9/#CE17	95	A22	139	PLLC
8	P44/SIN3	52	#CE8/#RAS1/#CE14/#RAS3	96	A23	140	V_{SS}
9	V_{SS}	53	V_{SS}	97	BV_{DDE}	141	P67
10	P43/#SRDY2	54	#CE7/#RAS0/#CE13/#RAS2	98	D15	142	P66
11	P42/#SCLK2	55	#CE6	99	D14	143	P65
12	P41/SOUT2	56	#CE5/#CE15	100	D13	144	P64
13	P40/SIN2	57	#CE4/#CE11	101	D12	145	P63
14	P07/#SRDY1/#DMAEND3	58	BV_{DDE}	102	D11	146	P62
15	P06/#SCLK1/#DMAACK3	59	#CE3	103	D10	147	V_{DDE}
16	P05/SOUT1/#DMAEND2	60	#CE10IN	104	V_{SS}	148	P61
17	P04/SIN1/#DMAACK2	61	#CE10EX	105	D9	149	P60
18	V_{DDE}	62	BCLK	106	D8	150	P57
19	P03/#SRDY0	63	V_{SS}	107	D7	151	P56
20	P02/#SCLK0	64	#HCAS/#UWE	108	D6	152	P55
21	P01/SOUT0	65	#LCAS/#CAS	109	D5	153	P54
22	P00/SIN0	66	#WRH/#BSH/#UWE	110	V_{DD}	154	V_{SS}
23	P33/#DMAACK1	67	#WRL/#WR/#WE/#LWE	111	D4	155	OSC4
24	P32/#DMAACK0	68	V_{DD}	112	D3	156	OSC3
25	V_{SS}	69	#EMEMRD	113	D2	157	V_{DD}
26	K54/#DMAREQ3	70	#RD	114	D1	158	P53
27	K53/#DMAREQ2	71	A0/#BSL	115	D0	159	P52
28	K52/#ADTRG	72	A1	116	BV_{DDE}	160	P51/T8UF5
29	K51/#DMAREQ1	73	V_{SS}	117	P87/TM9	161	P50/T8UF4
30	K50/#DMAREQ0	74	A2	118	P86/TM8	162	P16/EXCL5/#DMAEND1
31	V_{DD}	75	A3	119	P85/TM7	163	P15/EXCL4/#DMAEND0
32	OSC2	76	A4	120	V_{DDE}	164	V_{SS}
33	OSC1	77	A5	121	P84/TM6	165	P14/FOSC1/DCLK
34	V_{SS}	78	BV_{DDE}	122	P83/EXCL9	166	P13/EXCL3/T8UF3/DPCO
35	ICEMD	79	A6	123	P82/EXCL8	167	P12/EXCL2/T8UF2/DST2
36	K67/AD7	80	A7	124	V_{SS}	168	P11/EXCL1/T8UF1/DST1
37	K66/AD6	81	A8	125	P81/EXCL7	169	P10/EXCL0/T8UF0/DST0
38	K65/AD5	82	A9	126	P80/EXCL6	170	DSIO
39	K64/AD4	83	A10	127	P77	171	P27/TM5
40	K63/AD3	84	A11	128	P76	172	P26/TM4
41	K62/AD2	85	A12	129	P75	173	P25/TM3
42	K61/AD1	86	A13	130	P74	174	P24/TM2
43	K60/AD0	87	A14	131	P73/SDA1	175	P23/TM1
44	AV_{DDE}	88	A15	132	P72/SCL1	176	P22/TM0

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EPSON

S1C33L01

32-bit Single Chip Microcomputer

- High-speed 32-bit RISC Core
- Multiply Accumulation
- Built-in LCD Controller
- 10-bit ADC
- Built-in ROM and RAM
- Twin-clock Oscillator

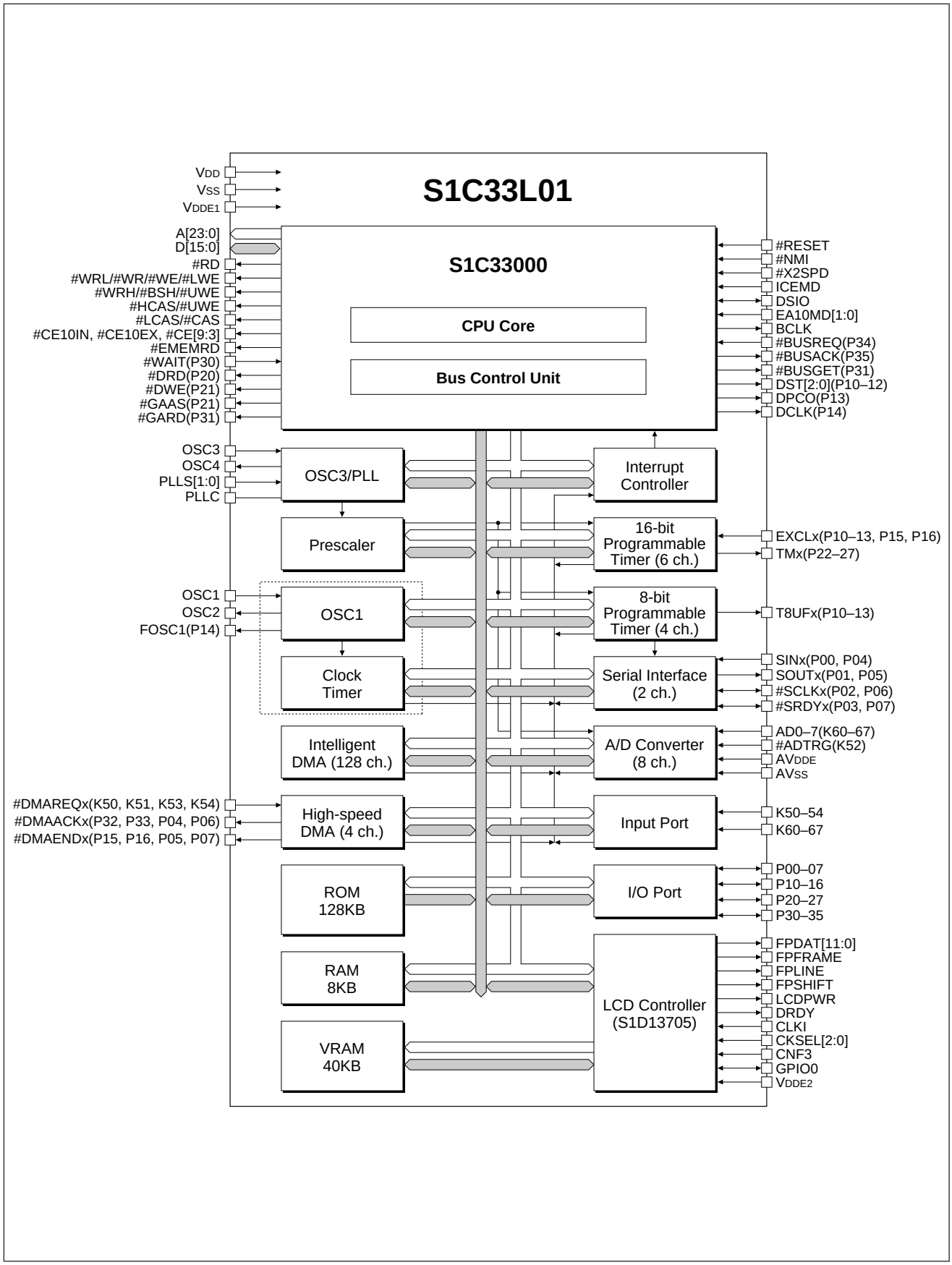
■ DESCRIPTION

The S1C33L01 is a CMOS 32-bit microcomputer composed of a CMOS 32-bit RISC core, ROM, RAM, DMA, timers, SIO, PLL, LCDC and other circuits. The S1C33L01 can be operated with high speed and spend little current. With the ADC, PWM and the MAC function, the S1C33L01 is suitable for voice applications and PDAs.

■ FEATURES

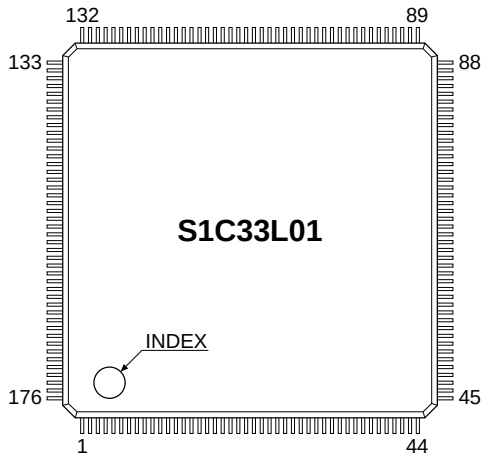
- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC core
- Main clock ..... 50MHz (Max., up to 12.5MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal ROM size ..... 128K bytes
- Internal RAM size ..... Data RAM : 8K bytes
  VRAM : 40K bytes
- LCD controller ..... S1D13705 equivalent
  4/8-bit monochrome/color LCD interface
  Active-matrix TFT/D-TFD interface
  1, 2 or 4 bits/pixel; 2, 4, or 16-level gray-scale display
  1, 2, 4 or 8 bits/pixel; 2, 4, 16 or 256 color display
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 4 channels and 16 bits × 6 channels
- PWM timer ..... Realized with a 16-bit programmable timer
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 2 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits
  I/O port : 29 bits
  Pins are shared with the inputs and outputs of built-in peripheral circuits.
- Interrupt controller ..... External interrupts : 6 types
  Internal interrupts : 29 types
- External bus interface ..... 24-bit address bus, 16-bit data bus, 7 chip enable pins
  DRAM and burst ROM may be connected directly.
- Shipping form ..... QFP18-176pin or chip
- Supply voltage ..... Core voltage : 1.8 to 3.6V
  I/O voltage : 1.8 to 5.5V
- Current consumption ..... SLEEP state : 10µA (3.3V, 32.768kHz, clock timer run state, Typ.)
  : 2.5µA (2.0V, 32.768kHz, clock timer run state, Typ.)
  RUN state : 60mA (3.3V, 50MHz Typ.)

■ BLOCK DIAGRAM



■ PIN LAYOUT

QFP18-176pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	A23	45	D2	89	N.C.	133	P21/#DWE/#GAAS
2	A22	46	D1	90	VSS	134	P20/#DRD
3	A21	47	D0	91	GPIO0	135	P16/EXCL5/#DMAEND1
4	A20	48	VSS	92	FPDAT11/GPIO4/INVERSE	136	P15/EXCL4/#DMAEND0
5	VDDE1	49	BCLK	93	FPDAT10/GPIO3	137	VDDE1
6	A19	50	#EMEMRD	94	FPDAT9/GPIO2	138	P14/FOSC1/DCLK
7	A18	51	#RD	95	VDDE2	139	P13/EXCL3/T8UF3/DPCO
8	A17	52	#WRL/#WR/#WE/#LWE	96	FPDAT8/GPIO1	140	P12/EXCL2/T8UF2/DST2
9	A16	53	#WRH/#BSH/#UWE	97	FPSHIFT	141	P11/EXCL1/T8UF1/DST1
10	A15	54	VDDE1	98	FPDAT7	142	P10/EXCL0/T8UF0/DST0
11	VSS	55	#CE10EX	99	FPDAT6	143	VSS
12	A14	56	#CE10IN	100	FPDAT5	144	P07/#SRDY1/#DMAEND3
13	A13	57	#CE3	101	VDD	145	P06/#SCLK1/DMAACK3
14	A12	58	VSS	102	FPDAT4	146	P05/SOUT1/#DMAEND2
15	A11	59	K67/AD7	103	FPDAT3	147	P04/SIN1/#DMAACK2
16	A10	60	K66/AD6	104	FPDAT2	148	VDD
17	VDD	61	K65/AD5	105	FPDAT1	149	OSC2
18	A9	62	AVDDE	106	VSS	150	OSC1
19	A8	63	K64/AD4	107	FPDAT0	151	VSS
20	A7	64	K63/AD3	108	FPLINE	152	P03/#SRDY0
21	A6	65	K62/AD2	109	FPFRAME	153	P02/#SCLK0
22	A5	66	AVSS	110	DRDY/MOD/FPSHIFT2	154	P01/SOUT0
23	VSS	67	K61/AD1	111	VDDE2	155	P00/SIN0
24	A4	68	K60/AD0	112	LCDPWR	156	CNF3
25	A3	69	K54/#DMAREQ3	113	N.C.	157	CKSEL2
26	A2	70	K53/#DMAREQ2	114	N.C.	158	CKSEL1
27	A1	71	K52/#ADTRG	115	N.C.	159	CKSEL0
28	A0/#BSL	72	VDD	116	N.C.	160	VDDE1
29	VDDE1	73	K51/#DMAREQ1	117	N.C.	161	CLKI
30	D15	74	K50/#DMAREQ0	118	VSS	162	ICEMD
31	D14	75	#LCAS/#CAS	119	P35/#BUSACK	163	VSS
32	D13	76	#HCAS/#UWE	120	P34/#BUSREQ/#CE6	164	OSC4
33	D12	77	#CE9/#CE17	121	P33/#DMAACK1	165	OSC3
34	D11	78	VSS	122	P32/#DMAACK0	166	EA10MD1
35	VSS	79	#CE8/#RAS1/#CE14/#RAS3	123	P31/#BUSGET/#GARD	167	EA10MD0
36	D10	80	#CE7/#RAS0/#CE13/#RAS2	124	P30/#WAIT/#CE4&5	168	#X2SPD
37	D9	81	#CE5/#CE15	125	VDD	169	VDD
38	D8	82	#CE4/#CE11	126	P27/TM5	170	PLLS1
39	D7	83	#CE6	127	P26/TM4	171	PLLS0
40	D6	84	VDDE1	128	P25/TM3	172	#NMI
41	VDD	85	N.C.	129	P24/TM2	173	VSS
42	D5	86	N.C.	130	P23/TM1	174	PLLC
43	D4	87	N.C.	131	VSS	175	#RESET
44	D3	88	N.C.	132	P22/TM0	176	DSIO

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S1C33S01

32-bit Single Chip Microcomputer

- High-speed 32-bit RISC Core
- Multiply Accumulation
- 8K-byte RAM Built-in
- 2-ch. SIO

■ DESCRIPTION

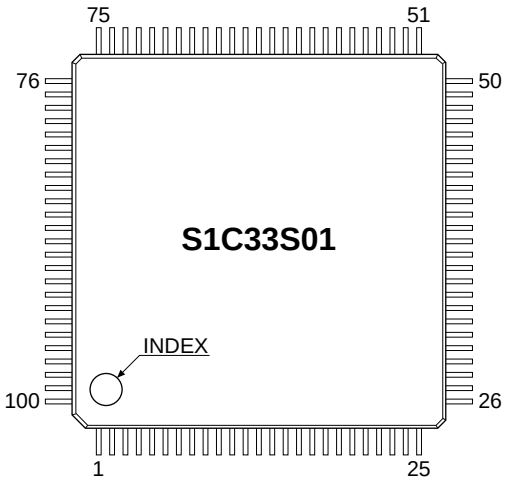
The S1C33S01 consists of the S1C33000 32-bit RISC type CPU as the core, a bus control unit, an interrupt controller, timers, serial interface circuits, 8K-byte RAM and other circuits. It also includes a high-speed oscillation circuit, PLL and low-speed oscillation circuit allowing high-speed operation and low-power operation with excellent clock functions. The S1C33S01 also provides a DSP function, by using the internal MAC (multiplication and accumulation) operation function, it makes it possible to design simply voice synthesis systems.

■ FEATURES

- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC core
- Main clock ..... 50MHz (Max., up to 12.5MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... 8,192 bytes
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 4 channels and 16 bits × 6 channels
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 2 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
- I/O port ..... I/O port : 29 bits
  Pins are shared with the inputs and outputs of built-in peripheral circuits.
- Interrupt controller ..... External interrupts : 8 types
  Internal interrupts : 23 types
- External bus interface ..... 24-bit address bus
  (High-order 4 bits are shared with the I/O ports)
  16-bit data bus
  6 chip enable pins
  (shared with the I/O ports)
  SRAM, DRAM and burst ROM may be connected directly.
- Shipping form QFP15-100pin
- Supply voltage ..... 1.8 to 3.6V (single power supply)
- Current consumption ..... SLEEP state : 10µA (3.3V, 32.768kHz, clock timer run state, Typ.)
  : 2.5µA (2.0V, 32.768kHz, clock timer run state, Typ.)
  RUN state : 49mA (3.3V, 60MHz Typ.)

■ PIN LAYOUT

QFP15-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	#WRL/#WR/#WE	26	A0/#BSL	51	A21/P34/#BUSREQ	76	P14/FOSC1/DCLK
2	#WRH/#BSH	27	A1	52	A22/P35/#BUSACK	77	P13/EXCL3/T8UF3/DPCO
3	#RD	28	A2	53	#CE9/P32	78	P12/EXCL2/T8UF2/DST2
4	#EMEMRD	29	A3	54	A23/P07/#SRDY1	79	P11/EXCL1/T8UF1/DST1
5	#LCAS	30	VDD	55	P06/#SCLK1	80	P10/EXCL0/T8UF0/DST0
6	#HCAS	31	A4	56	P05/SOUT1	81	PLLS0
7	VSS	32	A5	57	P04/SIN1	82	PLLS1
8	D0	33	A6	58	VSS	83	PLLC
9	D1	34	A7	59	OSC1	84	VSS
10	D2	35	VSS	60	OSC2	85	#X2SPD
11	D3	36	A8	61	VDD	86	OSC3
12	D4	37	A9	62	#RESET	87	OSC4
13	D5	38	A10	63	#NMI	88	ICEMD
14	VDD	39	A11	64	EA10MD0	89	#CE10EX
15	D6	40	VDD	65	EA10MD1	90	#CE10IN
16	D7	41	A12	66	VSS	91	VDD
17	D8	42	A13	67	#CE8/P31/#BUSGET/#GARD	92	BCLK
18	D9	43	A14	68	P30/#WAIT	93	#CE6/P20/#DRD
19	D10	44	A15	69	P03/#SRDY0	94	#CE7/P21/#DWE/#GAAS
20	D11	45	VSS	70	P02/#SCLK0	95	P22/TM0
21	VSS	46	A16	71	P01/SOUT0	96	P23/TM1
22	D12	47	A17	72	P00/SIN0	97	P24/TM2
23	D13	48	A18	73	#CE5/P16/EXCL5	98	P25/TM3
24	D14	49	A19	74	#CE4/P15/EXCL4	99	P26/TM4
25	D15	50	A20/P33	75	DSIO	100	P27/TM5

EPSON

S1C33221/222

32-bit Single Chip Microcomputer

Preliminary

- High-speed 32-bit RISC Core
- Multiply Accumulation
- 10-bit ADC
- Built-in RAM
- High-speed DMA, Intelligent DMA
- Twin-clock Oscillator

■ DESCRIPTION

The S1C33221/222 is a CMOS 32-bit microcomputer composed of a CMOS 32-bit RISC core, ROM, RAM, DMA, timers, SIO, PLL and other circuits. The S1C33221/222 can be operated with high speed and spend little current. With the ADC, PWM and the MAC function, the S1C33221/222 is suitable for voice applications, PDAs and OA products such as printers.

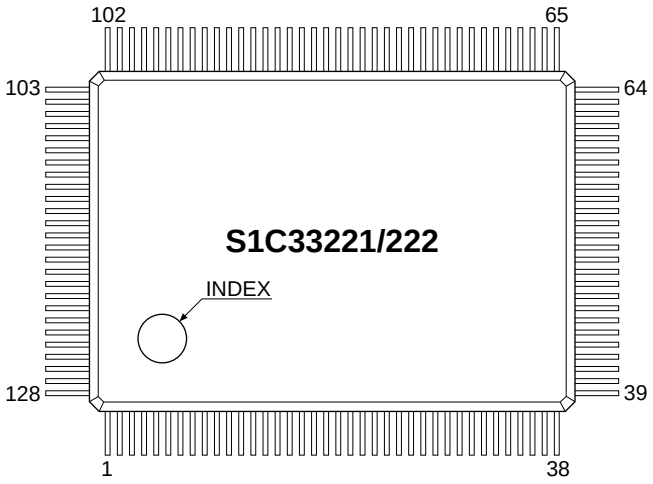
■ FEATURES

- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC core
- Main clock ..... 50MHz (Max., up to 12.5MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... 8,192 bytes
- Internal ROM size ..... 131,072 bytes (S1C33221), 65,536 bytes (S1C33222)
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 6 channels and 16 bits × 6 channels
- PWM timer ..... Realized with a 16-bit programmable timer
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 4 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits
  I/O port : 29 bits
  Pins are shared with the inputs and outputs of built-in peripheral circuits.
- Interrupt controller ..... External interrupts : 10 types
  Internal interrupts : 29 types
- External bus interface ..... 24-bit address bus, 16-bit data bus, 7 chip enable pins
  DRAM and burst ROM may be connected directly.
- Shipping form QFP5-128pin
- Supply voltage ..... Core voltage : 1.8 to 3.6V
  I/O voltage : 1.8 to 5.5V
- Current consumption ..... SLEEP state : 10µA (3.3V, 32.768kHz, clock timer run state, Typ.)
  : 2.5µA (2.0V, 32.768kHz, clock timer run state, Typ.)
  RUN state : 70mA (3.3V, 50MHz Typ.)

∗ This model is under development, therefore the contents of the above specifications may be revised at final.

■ PIN LAYOUT

QFP5-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P24/TM2	33	K65/AD5	65	#RESET	97	A16
2	VSS	34	K50/#DMAREQ0	66	#NMI	98	ICEMD
3	P25/TM3	35	K64/AD4	67	A0/#BSL	99	A17
4	P26/TM4	36	K63/AD3	68	A1	100	A18
5	P15/EXCL4/#DMAEND0	37	K62/AD2	69	P34/#BUSREQ/#CE6	101	A19
6	P27/TM5	38	AVDDE	70	VSS	102	P04/SIN1/#DMAACK2
7	BCLK	39	K61/AD1	71	A2	103	P05/SOUT1/#DMAEND2
8	P00/SIN0	40	K60/AD0	72	A3	104	P06/#SCLK1/DMAACK3
9	P01/SOUT0	41	D6	73	A4	105	VSS
10	D15	42	VSS	74	A5	106	PLLC
11	VDD	43	D5	75	A6	107	VSS
12	P03/#SRDY0	44	D4	76	#CE10IN	108	PLLS1
13	D14	45	D3	77	VDD	109	PLLS0
14	P31/#BUSGET/#GARD	46	D2	78	#EMEMRD	110	P07/#SRDY1/#DMAEND3
15	D13	47	D1	79	A7	111	#X2SPD
16	P32/#DMAACK0	48	D0	80	#HCAS	112	EA10MD0
17	D12	49	P35/#BUSACK	81	A8	113	EA10MD1
18	P33/#DMAACK1	50	VDDE	82	#LCAS	114	VDD
19	D11	51	#CE9/#CE17	83	A9	115	N.C.
20	K54/#DMAREQ3	52	OSC2	84	P16/EXCL5/#DMAEND1	116	OSC4
21	D10	53	#CE7/#RAS0/#CE13/#RAS2	85	A10	117	P20/#DRD
22	K53/#DMAREQ2	54	OSC1	86	A20	118	OSC3
23	D9	55	#CE6	87	A11	119	P21/#DWE/#GAAS
24	K52/#ADTRG	56	#RD	88	A21	120	#CE3
25	VSS	57	VSS	89	A12	121	P22/TM0
26	K51/#DMAREQ1	58	#WRL/#WR/#WE	90	A22	122	P23/TM1
27	P02/#SCLK0	59	#WRH/#BSH	91	A13	123	DSIO
28	D8	60	#CE10EX	92	A23	124	P10/EXCL0/T8UF0/DST0
29	D7	61	#CE8/#RAS1/#CE14/#RAS3	93	VSS	125	P11/EXCL1/T8UF1/DST1
30	VDDE	62	#CE5/#CE15	94	A14	126	P12/EXCL2/T8UF2/DST2
31	K67/AD7	63	#CE4/#CE11	95	A15	127	P13/EXCL3/T8UF3/DPCO
32	K66/AD6	64	P30/#WAIT/#CE4&5	96	VDDE	128	P14/FOSC1/DCLK

EPSON

S1C33240

32-bit Single Chip Microcomputer

Preliminary

- High-speed 32-bit RISC Core
- Multiply Accumulation
- 10-bit ADC
- Built-in RAM
- High-speed DMA, Intelligent DMA
- Twin-clock Oscillator
- Built-in Flash Memory

■ DESCRIPTION

The S1C33240 is a CMOS 32-bit microcomputer composed of a CMOS 32-bit RISC core, Flash, RAM, DMA, timers, SIO, PLL and other circuits. The S1C33240 can be operated with high speed and spend little current. With the ADC, PWM and the MAC function, the S1C33240 is suitable for voice applications, PDAs and OA products such as printers.

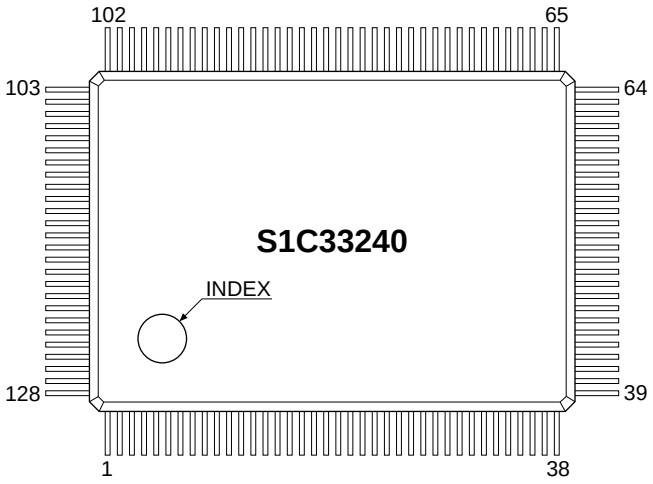
■ FEATURES

- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC core
- Main clock ..... 40MHz (Max., up to 10MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... 8,192 bytes
- Internal Flash memory size ..... 131,072 bytes (Accessible with 0 wait states for up to 20MHz)
  Can be erased and programmed using the S5U1C33000H and S5U1C33000C.
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 4 channels and 16 bits × 6 channels
- PWM timer ..... Realized with a 16-bit programmable timer
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 4 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits
  I/O port : 29 bits
  Pins are shared with the inputs and outputs of built-in peripheral circuits.
- Interrupt controller ..... External interrupts : 10 types
  Internal interrupts : 29 types
- External bus interface ..... 24-bit address bus, 16-bit data bus, 7 chip enable pins
  DRAM and burst ROM may be connected directly.
- Shipping form QFP5-128pin
- Supply voltage ..... Core voltage : 2.7 to 3.6V
  I/O voltage : 2.7 to 5.5V
- Current consumption ..... SLEEP state : 16µA (3.3V, 32.768kHz, clock timer run state, Typ.)
  RUN state : 65mA (3.3V, 40MHz Typ.)

∗ This model is under development, therefore the contents of the above specifications may be revised at final.

■ PIN LAYOUT

QFP5-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P24/TM2	33	K65/AD5	65	#RESET	97	A16
2	VSS	34	K50/#DMAREQ0	66	#NMI	98	ICEMD
3	P25/TM3	35	K64/AD4	67	A0/#BSL	99	A17
4	P26/TM4	36	K63/AD3	68	A1	100	A18
5	P15/EXCL4/#DMAEND0	37	K62/AD2	69	P34/#BUSREQ/#CE6	101	A19
6	P27/TM5	38	AVDDE	70	VSS	102	P04/SIN1/#DMAACK2
7	BCLK	39	K61/AD1	71	A2	103	P05/SOUT1/#DMAEND2
8	P00/SIN0	40	K60/AD0	72	A3	104	P06/#SCLK1/DMAACK3
9	P01/SOUT0	41	D6	73	A4	105	VSS
10	D15	42	VSS	74	A5	106	PLLC
11	VDD	43	D5	75	A6	107	VSS
12	P03/#SRDY0	44	D4	76	#CE10IN	108	PLLS1
13	D14	45	D3	77	VDD	109	PLLS0
14	P31/#BUSGET/#GARD	46	D2	78	#EMEMRD	110	P07/#SRDY1/#DMAEND3
15	D13	47	D1	79	A7	111	#X2SPD
16	P32/#DMAACK0	48	D0	80	#HCAS	112	EA10MD0
17	D12	49	P35/#BUSACK	81	A8	113	EA10MD1
18	P33/#DMAACK1	50	VDDE	82	#LCAS	114	VDD
19	D11	51	#CE9/#CE17	83	A9	115	EA10MD2
20	K54/#DMAREQ3	52	OSC2	84	P16/EXCL5/#DMAEND1	116	OSC4
21	D10	53	#CE7/#RAS0/#CE13/#RAS2	85	A10	117	P20/#DRD
22	K53/#DMAREQ2	54	OSC1	86	A20	118	OSC3
23	D9	55	#CE6	87	A11	119	P21/#DWE/#GAAS
24	K52/#ADTRG	56	#RD	88	A21	120	#CE3
25	VSS	57	VSS	89	A12	121	P22/TM0
26	K51/#DMAREQ1	58	#WRL/#WR/#WE	90	A22	122	P23/TM1
27	P02/#SCLK0	59	#WRH/#BSH	91	A13	123	DSIO
28	D8	60	#CE10EX	92	A23	124	P10/EXCL0/T8UF0/DST0
29	D7	61	#CE8/#RAS1/#CE14/#RAS3	93	VSS	125	P11/EXCL1/T8UF1/DST1
30	VDDE	62	#CE5/#CE15	94	A14	126	P12/EXCL2/T8UF2/DST2
31	K67/AD7	63	#CE4/#CE11	95	A15	127	P13/EXCL3/T8UF3/DPCO
32	K66/AD6	64	P30/#WAIT/#CE4&5	96	VDDE	128	P14/FOSC1/DCLK

EPSON

S1C33210 (Mobile Access Gateway IC)

32-bit Single Chip Microcomputer

- 32-bit RISC CPU
- HDLC Controller
- Three Serial I/O (SIO) Interfaces
- 8K Bytes of Built-in RAM
- Multiply-and-accumulate Instructions
- Built-in Analog-to-digital Converter
- High-speed DMA and Intelligent DMA
- Low Power Consumption
- PDC, PHS, and CdmaOne Interfaces*1

*1: These interfaces require the software modem module.

■ DESCRIPTION

The S1C33210 single-chip microcomputer consists of the S1C33000 CMOS 32-bit RISC CPU core plus an HDLC controller, three serial I/O (SIO) interfaces, 8K bytes of built-in RAM, a direct memory access (DMA) controller, timers, an analog-to-digital converter, and other components. The device features both high-speed operation and low power consumption. The HDLC controller, serial I/O (SIO) interfaces, and other components necessary for mobile access make this device ideal for data communications adapters, PDAs, and other portable information equipment. The multiply-and-accumulate instructions and analog-to-digital converter support voice recognition, voice synthesis, and other forms of digital signal processing for use in portable multimedia terminals.

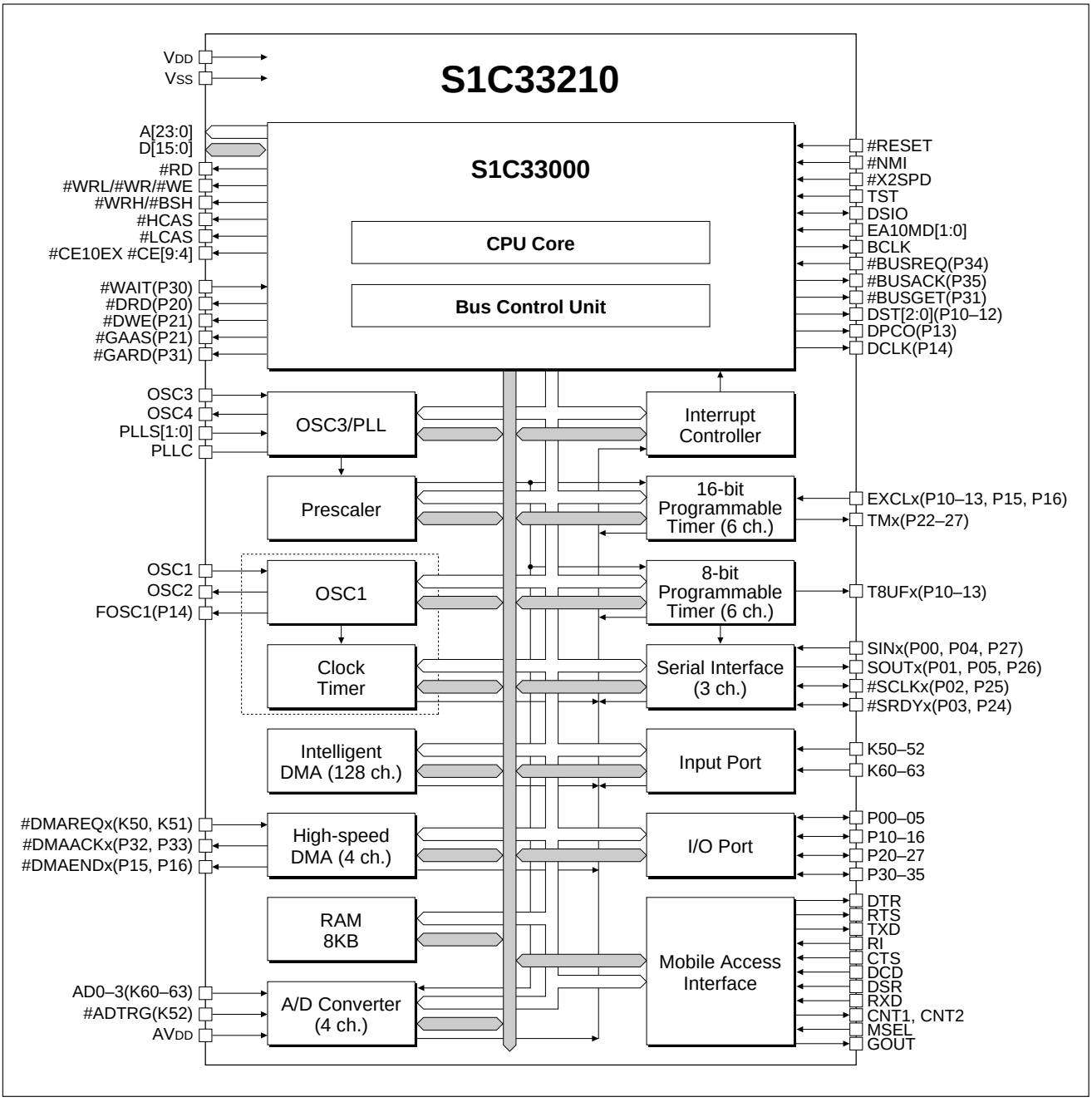
■ FEATURES

- CMOS LSI with 32-bit parallel processing ... S1C33000 RISC CPU
- Main clock ... 50MHz (Max., with built-in 4× phase-locked loop)
- Sub clock ... 32.768kHz (Typ.) crystal oscillator
- Instruction set ... 16-bit fixed-length arithmetic, highly orthogonal 105-member instruction set, multiply-and-accumulate (MAC) instructions that execute in two cycles
- Built-in RAM ... 8,192 bytes
- Clock timer ... 1 channel
- Programmable timers ... 8 bits × 6 channels and 16 bits × 6 channels
- PWM timer ... Application for 16-bit programmable timer
- Watchdog timer ... Application for 16-bit programmable timer
- PDC interface ... 1 channel
  Control interface represents application for serial I/O (SIO) interface.
- PHS interface ... 1 channel
  Control interface represents application for serial I/O (SIO) interface. Supports both 32 and 64 kbps.
  Built-in I.460 speed conversion.
- HDLC controller ... 1 channel
- Serial interfaces ... 3 channels
  Choice of clock synchronous or asynchronous operation. (ch0, ch2)
  (ch1 only supports asynchronous system.)
  Configurable as infrared (IrDA) interfaces.
- 10-bit analog-to-digital converter ... Cumulative comparison operation, 4 input channels.
- High-speed DMA ... 4 channels
- Intelligent DMA ... 128 channels
- General-purpose I/O ports ... Input port : 7 bits
  I/O port : 27 bits
  These pins double as I/O pins for the onboard peripherals.
- Interrupt controller ... External interrupts : 10 types
  Internal interrupts : 29 types
- External bus interfaces ... 24-bit address bus, 16-bit data bus, 7 chip enable outputs.
  Direct connection to DRAM and burst ROM.

S1C33210 (Mobile Access Gateway IC)

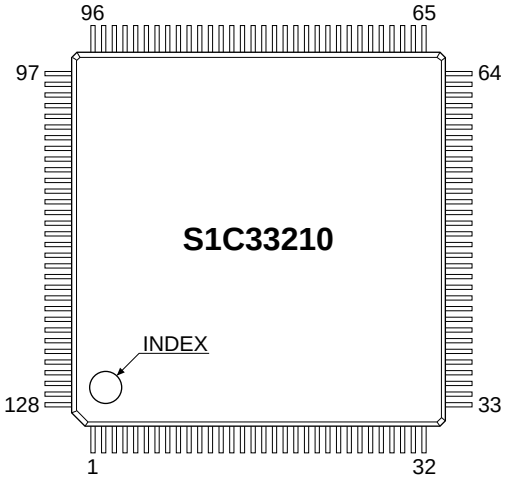
- Package QFP15-128pin
- Supply voltages ..... Internal operating voltage : 2.7 to 3.6V
  I/O levels : 2.7 to 3.6V
- Power consumption ..... In SLEEP mode : 4µW Typ.
  During normal operation : 230mW Typ. at 3.3V, 50MHz

■ BLOCK DIAGRAM



■ PIN LAYOUT

QFP15-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P26/TM4/SOUT2	33	K52/#ADTRG	65	A6	97	RI
2	P27/TM5/SIN2	34	#CE10EX/#CE9&10EX	66	A7	98	CNT2
3	VSS	35	#CE4/#CE11/#CE11&12	67	VSS	99	CNT1
4	BCLK	36	D7	68	P30/#WAIT/#CE4&5	100	TXD
5	P00/SIN0	37	D6	69	A8	101	CTS
6	P01/SOUT0	38	D5	70	A9	102	VSS
7	D15	39	VSS	71	#CE5/#CE15/#CE15&16	103	PLLC
8	VDD	40	D4	72	A10	104	SCANEN
9	P03/#SRDY0	41	D3	73	A20	105	PLLS1
10	D14	42	D2	74	VDD	106	PLLS0
11	P31/#BUSGET/#GARD	43	#RESET	75	A11	107	RXD
12	D13	44	#NMI	76	A21	108	DCD
13	P32/#DMAACK0	45	D1	77	P16/EXCL5/#DMAEND1	109	MSEL
14	D12	46	D0	78	A12	110	GOUT
15	P33/#DMAACK1	47	VDD	79	A22	111	VDD
16	D11	48	#CE9/#CE17/#CE17&18	80	TST	112	OSC3
17	P02/#SCLK0	49	#CE7/#RAS0/#CE13/#RAS2	81	A13	113	OSC4
18	D10	50	OSC2	82	A23	114	EA10MD0
19	K50/#DMAREQ0	51	OSC1	83	P04/SIN1/#DMAACK2	115	EA10MD1
20	#WRL/#WR/#WE	52	#CE6/#CE7&8	84	A14	116	#X2SPD
21	#WRH/#BSH	53	#CE8/#RAS1/#CE14/#RAS3	85	A15	117	P21/#DWE/#GAAS
22	VSS	54	VSS	86	P05/SOUT1/#DMAEND2	118	P22/TM0
23	K51/#DMAREQ1	55	A0/#BSL	87	A16	119	P23/TM1
24	#RD	56	A1	88	A17	120	DSIO
25	D9	57	A2	89	A18	121	P10/EXCL0/T8UF0/DST0
26	D8	58	A3	90	VSS	122	P11/EXCL1/T8UF1/DST1
27	VDD	59	P35/#BUSACK	91	A19	123	P12/EXCL2/T8UF2/DST2
28	K63/AD3	60	#HCAS	92	P20/#DRD	124	P13/EXCL3/T8UF3/DPC0
29	K62/AD2	61	#LCAS	93	VDD	125	P14/FOSC1/DCLK
30	AVDD	62	P34/#BUSREQ/#CE6	94	RTS	126	P24/TM2/#SRDY2
31	K61/AD1	63	A4	95	DTR	127	P25/TM3/#SCLK2
32	K60/AD0	64	A5	96	DSR	128	P15/EXCL4/#DMAEND0

■ PIN FUNCTION

● Pins for Power Supply System

Pin name	Pin No.	I/O	Pull-up	Function
V_{DD} x6	8, 27, 47, 74, 93, 111	–	–	Power supply pin (+)
V_{SS} x7	3, 22, 39, 54, 67, 90, 102	–	–	Power supply pin (-) GND
AV_{DD}	30	–	–	Analog system power supply (+); $AV_{DD} = V_{DD}$

● Pins for Clock Generator

Pin name	Pin No.	I/O	Pull-up	Function
OSC1	51	I	–	Low-speed (OSC1) oscillation input
OSC2	50	O	–	Low-speed (OSC1) oscillation output
OSC3	112	I	–	High-speed (OSC3) oscillation input
OSC4	113	O	–	High-speed (OSC3) oscillation output
PLLS[1:0]	105, 106	I	–	PLL set-up pins
PLLC	103	–	–	Capacitor connecting pin for PLL

● Pins for External Bus Interface Signals

Pin name	Pin No.	I/O	Pull-up	Function
A0/#BSL	55	O	–	Address bus (A0)/bus strobe (low byte) signal
A[23:1]	56–58, 63–66, 69, 70, 72, 75, 78, 81, 84, 85, 87–89, 91, 73, 76, 79, 82	O	–	Address bus (A1 to A23)
D[15:0]	7, 10, 12, 14, 16, 18, 25, 26, 36–38, 40–42, 45, 46	I/O	–	Data bus (D0 to D15)
#CE10EX/#CE9&10EX	34	O	–	Area 10 chip enable for external memory
#CE9/#CE17/#CE17&18	48	O	–	Chip enable (area 9, 17)
#CE8/#RAS1/#CE14/#RAS3	53	O	–	Chip enable (area 8, 14)/DRAM row strobe (Area 8, 14)
#CE7/#RAS0/#CE13/#RAS2	49	O	–	Chip enable (area 7, 13)/DRAM row strobe (Area 7, 13)
#CE6/#CE7&8	52	O	–	Area 6 chip enable
#CE5/#CE15/#CE15&16	71	O	–	Chip enable (area 5, 15)
#CE4/#CE11/#CE11&12	35	O	–	Chip enable (area 4, 11)
#RD	24	O	–	Read signal
#WRL/#WR/#WE	20	O	–	Write (low byte) signal/write signal/DRAM write signal
#WRH/#BSH	21	O	–	Write (high byte) signal/bus strobe (high byte) signal
#HCAS	60	O	–	DRAM column address strobe (high byte) signal
#LCAS	61	O	–	DRAM column address strobe (low byte) signal
BCLK	4	O	–	Bus clock output
P34/#BUSREQ/#CE6	62	I/O	–	I/O port/Bus release request input/Area 6 chip enable
P35/#BUSACK	59	I/O	–	I/O port/Bus release request acknowledge output
P30/#WAIT/#CE4&5	68	I/O	–	I/O port/Wait cycle request input/Area 4 and 5 chip enable
P20/#DRD	92	I/O	–	I/O port/DRAM read signal output for successive RAS mode
P21/#DWE/#GAAS	117	I/O	–	I/O port/DRAM write signal output for successive RAS mode/ Area address strobeoutput for GA
P31/#BUSGET/#GARD	11	I/O	–	I/O port/Bus status monitor signal output for bus release request/ Area read signal output GA
EA10MD1	115	I	Pull-up	Area 10 boot mode selection
EA10MD0	114	I	–	

● HSDMA Control Signal Pins

Pin name	Pin No.	I/O	Pull-up	Function
K50/#DMAREQ0	19	I	Pull-up	Input port/HSDMA Ch.0 request input
K51/#DMAREQ1	23	I	Pull-up	Input port/HSDMA Ch.1 request input
P32/#DMAACK0	13	I/O	–	I/O port/HSDMA Ch.0 acknowledge output
P33/#DMAACK1	15	I/O	–	I/O port/HSDMA Ch.1 acknowledge output
P04/SIN1/#DMAACK2	83	I/O	–	I/O port/Serial I/F Ch.1 data input/ HSDMA Ch.2 acknowledge output
P15/EXCL4/#DMAEND0	128	I/O	–	I/O port/16-bit timer 4 event counter input/ HSDMA Ch. 0 end-of-transfer signal output
P16/EXCL5/#DMAEND1	77	I/O	–	I/O port/16-bit timer 5 event counter input/ HSDMA Ch.1 end-of-transfer signal output
P05/SOUT1/#DMAEND2	86	I/O	–	I/O port/Serial I/F Ch.1data output/ HSDMA Ch.2 end-of-transfer signal output

● I/O Pins for Internal Peripheral Circuits

Pin name	Pin No.	I/O	Pull-up	Function
K52/#ADTRG	33	I	Pull-up	Input port/A/D converter trigger input
K60/AD0	32	I	–	Input port/A/D converter Ch.0 input
K61/AD1	31	I	–	Input port/A/D converter Ch.1 input
K62/AD2	29	I	–	Input port/A/D converter Ch.2 input
K63/AD3	28	I	–	Input port/A/D converter Ch.3 input
P00/SIN0	5	I/O	–	I/O port/Serial I/F Ch.0 data input
P01/SOUT0	6	I/O	–	I/O port/Serial I/F Ch.0 data output
P02/#SCLK0	17	I/O	–	I/O port/Serial I/F Ch.0 clock input/output
P03/#SRDY0	9	I/O	–	I/O port/Serial I/F Ch.0 ready signal output
P04/SIN1	83	I/O	–	I/O port/Serial I/F Ch.1 data input
P05/SOUT1	86	I/O	–	I/O port/Serial I/F Ch.1 data output
P10/EXCL0/T8UF0/DST0	121	I/O	–	I/O port/16-bit timer 0 event counter input/ 8-bit timer 0 output/DST0 signal output
P11/EXCL1/T8UF1/DST1	122	I/O	–	I/O port/16-bit timer 1 event counter input/ 8-bit timer 1 output/DST1 signal output
P12/EXCL2/T8UF2/DST2	123	I/O	–	I/O port/16-bit timer 2 event counter input/ 8-bit timer 2 output/DST2 signal output
P13/EXCL3/T8UF3/DPCO	124	I/O	–	I/O port/16-bit timer 3 event counter input/ 8-bit timer 3 output/DPCO signal output
P14/FOSC1/DCLK	125	I/O	–	I/O port/OSC1 clock output/DCLK signal output
P15/EXCL4/#DMAEND0	128	I/O	–	I/O port/16-bit timer 4 event counter input/ HSDMA Ch.0 end-of-transfer signal output
P16/EXCL5/#DMAEND1	77	I/O	–	I/O port/16-bit timer 5 event counter input/ HSDMA Ch.1 end-of-transfer signal output
P20/#DRD	92	I/O	–	I/O port/DRAM read signal output for successive RAS mode
P21/#DWE/#GAAS	117	I/O	–	I/O port/DRAM write signal output for successive RAS mode/ Area address strobe output for GA
P22/TM0	118	I/O	–	I/O port/16-bit timer 0 output
P23/TM1	119	I/O	–	I/O port/16-bit timer 1 output
P24/TM2/#SRDY2	126	I/O	–	I/O port/16-bit timer 2 output/Serial I/F Ch.2 ready signal I/O
P25/TM3/#SCLK2	127	I/O	–	I/O port/16-bit timer 3 output/Serial I/F Ch.2 clock I/O
P26/TM4/SOUT2	1	I/O	–	I/O port/16-bit timer 4 output/Serial I/F Ch.2 data output
P27/TM5/SIN2	2	I/O	–	I/O port/16-bit timer 5 output/Serial I/F Ch.2 data input
DTR	95	O	–	DTR output
RTS	94	O	–	RTS output
TXD	100	O	–	TXD output
RI	97	I	–	RI input
CTS	101	I	–	CTS input
DCD	108	I	–	DCD input
DSR	96	I	–	DSR input
RXD	107	I	–	RXD input
CNT1	99	O	–	Mobile control signal output 1
CNT2	98	O	–	Mobile control signal output 2
MSEL	109	I	Pull-up	Serial I/F Ch.3 operating setting input pin
GOUT	110	O	–	NMI request output

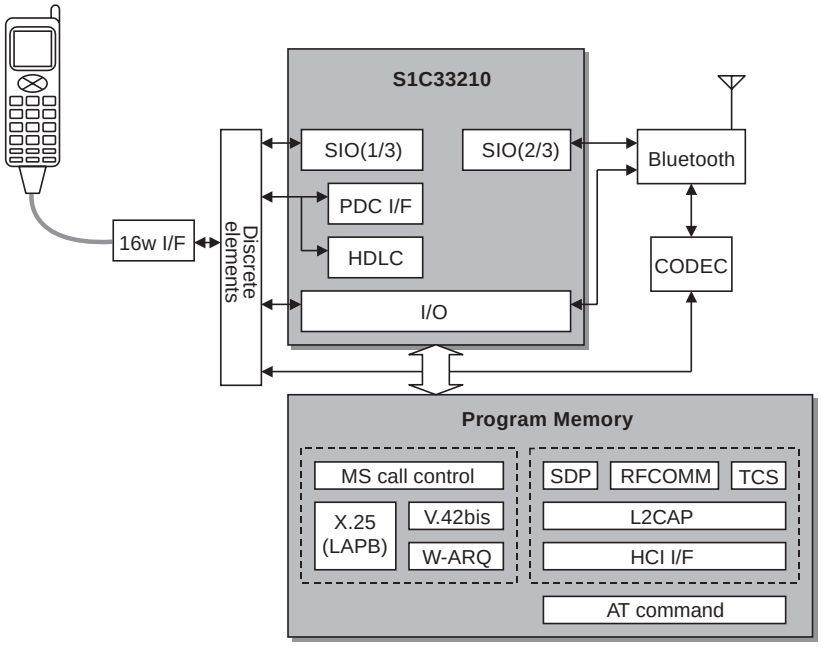
● Other Pins

Pin name	Pin No.	I/O	Pull-up	Function
TST	80	I	Pull-down	Test pin
DSIO	120	I/O	Pull-up	Serial I/O pin for debugging
#X2SPD	116	I	–	Clock doubling mode set-up pin
#NMI	44	I	Pull-up	NMI request input pin
#RESET	43	I	Pull-up	Initial reset input pin
SCANEN	104	I	Pull-down	

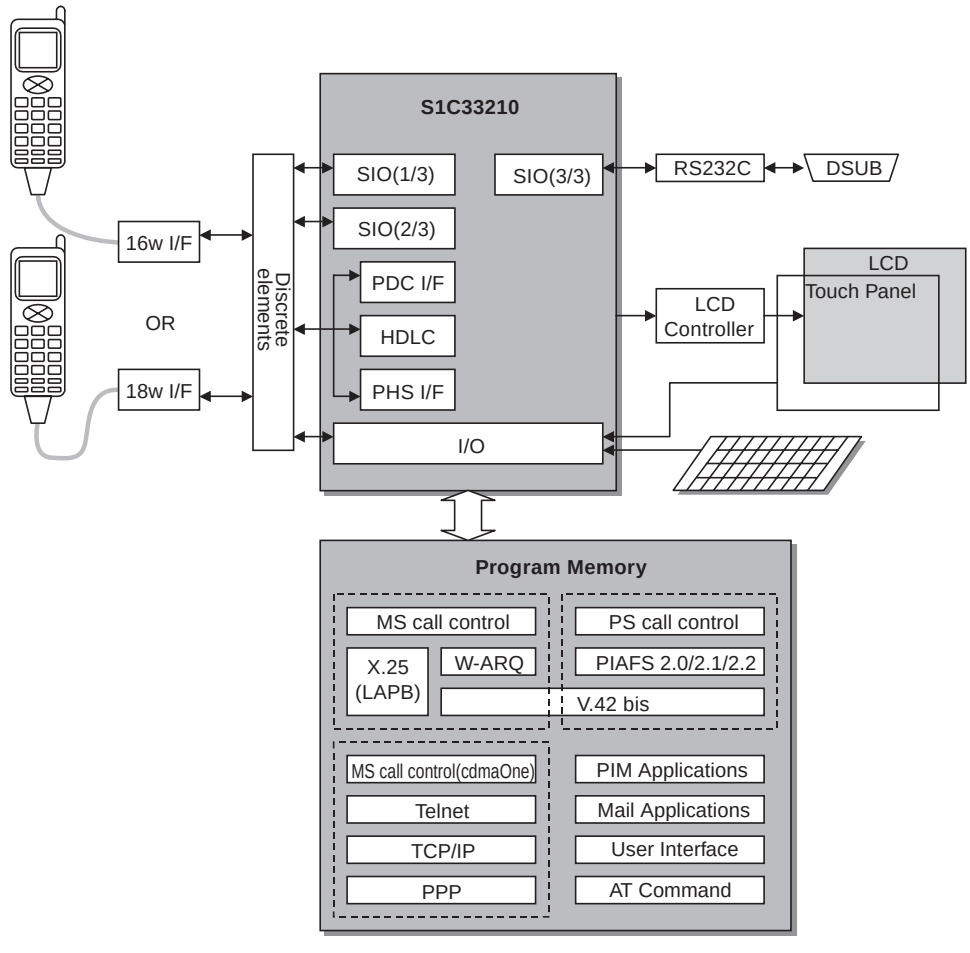
Note: "#" in the pin names indicates that the signal is low active.

■ APPLICATIONS

Bluetooth/PDC Adapter



PDA for PDC/PHS/cdmaOne



EPSON

S1C33205/225/226/245

32-bit Single Chip Microcomputer

Preliminary

- High-speed 32-bit RISC Core
- Built-in SDRAM Controller
- Multiply Accumulation
- 10-bit ADC
- Built-in 8K-byte RAM

■ DESCRIPTION

The S1C33205/225/226/245 is a CMOS 32-bit microcomputer composed of a CMOS 32-bit RISC core, RAM, DMA, timers, SIO, PLL and other circuits. Featuring high-speed operation, low current consumption, and including a SDRAM controller, this microcomputer allows direct connection of external SDRAM, making it ideal for use with PDAs and other portable devices. In addition, since the microcomputer incorporates an A/D converter and PWM and is capable of multiply-accumulate operations, digital signal processing such as speech synthesis processing can be accomplished with a single chip.

■ FEATURES

- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC core
- Main clock ..... 60MHz (Max., 15MHz external clock input: S1C33205)
  50MHz (Max., 12.5MHz external clock input: S1C33225/226/245)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... 8,192 bytes
- Internal ROM size ..... 128K bytes (S1C33225), 64K bytes (S1C33226)
- Internal Flash memory size ..... 128K bytes (S1C33245)
- SDRAM controller ..... Supports 1M × 16-bit to 16M × 16-bit SDRAMs
  Capable of access either in 8 or 16 bits
  Capable of burst reads and single writes
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 6 channels and 16 bits × 6 channels
- Watchdog timer ..... Realized with a 16-bit programmable timer
- PWM timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 4 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits
  I/O port : 29 bits
- Interrupt controller ..... External interrupts : 10 types
  Internal interrupts : 29 types
- External bus interface ..... 24-bit address bus, 16-bit data bus, 7 chip enable pins
  DRAM, SDRAM and burst ROM may be connected directly.
- Shipping form QFP15-128pin
- Supply voltage ..... Core voltage : 1.8 to 3.6V
  I/O voltage : 1.8 to 5.5V
- Current consumption ..... SLEEP state : TBD (3.3V, 32.768kHz, clock timer run state, Typ.)
  RUN state : TBD (3.3V, 50MHz Typ.)

∗ This model is under development, therefore the contents of the above specifications may be revised at final.

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EPSON

S1C33L03

32-bit Single Chip Microcomputer

Preliminary

- High-speed 32-bit RISC Core
- Built-in LCD Controller
- Built-in SDRAM Controller
- Multiply Accumulation
- 10-bit ADC
- Built-in 8K-byte RAM

■ DESCRIPTION

The S1C33L03 is a CMOS 32-bit microcomputer composed of a CMOS 32-bit RISC core, RAM, DMA, timers, SIO, PLL, LCD controller, SDRAM controller and other circuits. The S1C33L03 can be operated with high speed and spend little current. With the ADC, PWM and the MAC function, the S1C33L03 is suitable for voice applications and PDAs.

■ FEATURES

- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC core
- Main clock ..... 50MHz (Max., up to 12.5MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... 8,192 bytes
- LCD controller ..... DMA type
  4/8-bit monochrome LCD interface
  1, 2 or 4 bits/pixel; 2, 4, or 16-level gray-scale display
- SDRAM controller ..... Supports 1M × 16-bit to 16M × 16-bit SDRAMs
  Capable of access either in 8 or 16 bits
  Capable of burst reads and single writes
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 6 channels and 16 bits × 6 channels
- Watchdog timer ..... Realized with a 16-bit programmable timer
- PWM timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 4 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits
  I/O port : 29 bits
- Interrupt controller ..... External interrupts : 10 types
  Internal interrupts : 29 types
- External bus interface ..... 24-bit address bus, 16-bit data bus, 7 chip enable pins
  DRAM, SDRAM and burst ROM may be connected directly.
- Shipping form QFP20-144pin
- Supply voltage ..... Core voltage : TBD (1.8 to 3.6V)
  I/O voltage : TBD (1.8 to 5.5V)
- Current consumption ..... HALT state : TBD
  RUN state : TBD

∗ This model is under development, therefore the contents of the above specifications may be revised at final.

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EPSON

S1C33 Family Development Environment

Software tools

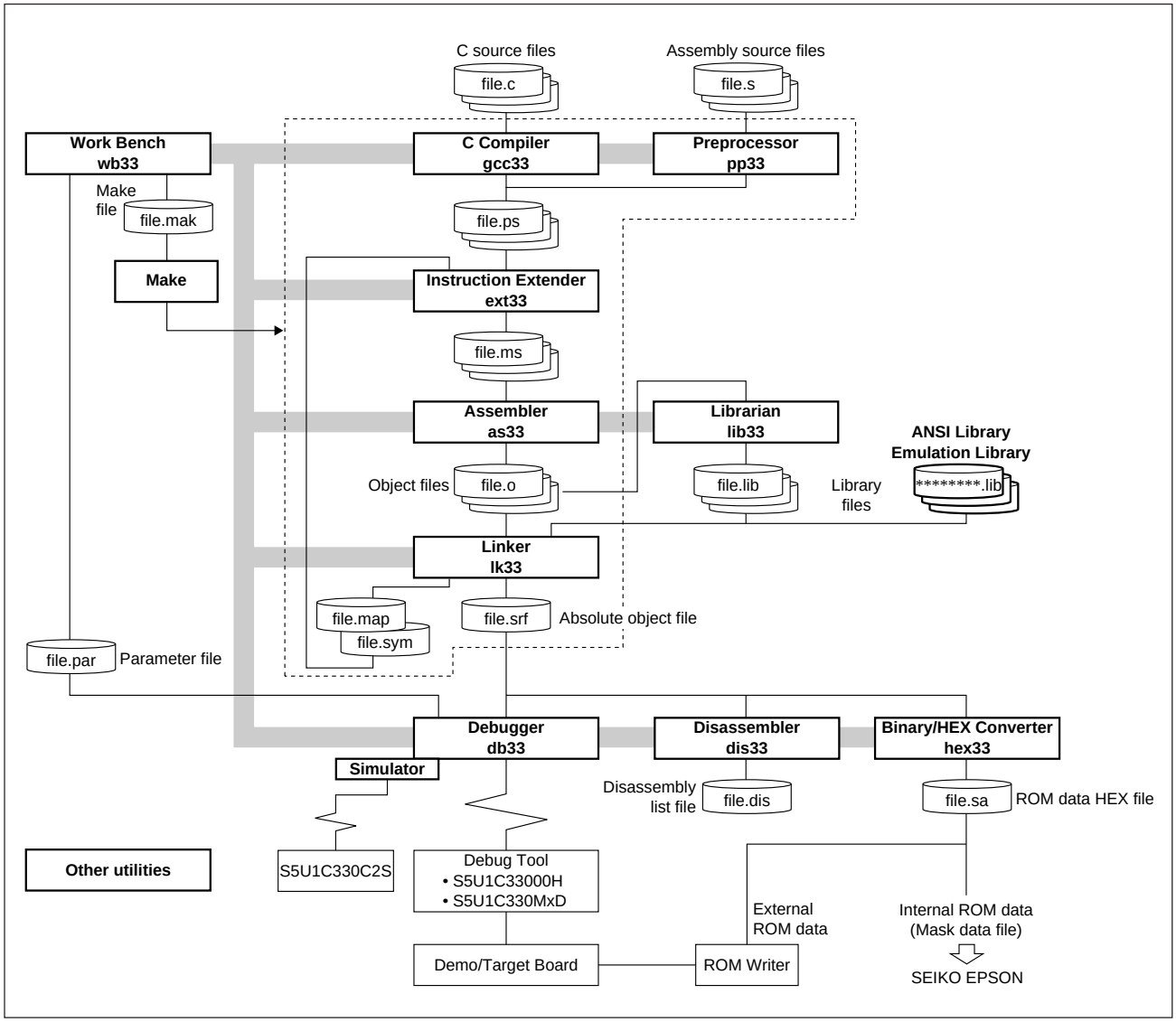
- C compiler with strong optimization capability
- Useful extended instructions based on the S1C33 instruction set
- C & assembler source level debugger capable of being connected to various types of debugging targets
- Supporting Windows 95/98/NT4.0 GUI

■ DESCRIPTION

The S1C33 Family development tools provide the following environment suitable for developing applications that use an S1C33 Family microcomputer:

- Software development in C language using the C compiler optimized for S1C33 architecture
  The C compiler has a strong optimization capability, it makes it possible to compile C source files with higher code efficiency
- Software development in assembly language using the extended instruction set
- Pleasant debugging environment using the debugger that supports C and assembly level debugging with GUI and the ICE which has various debugging functions

■ DEVELOPMENT FLOW



S1C33 Family Development Environment

■ FEATURES

● C Compiler
A C compiler optimized based on gcc 2.7.2 to meet the S1C33 architecture.
The C compiler and instruction extender realize high-code efficiency.

● Libraries
Supports ANSI C and floating-point emulation libraries.

● Preprocessor
Provides macro, #include, #define and #ifdef functions for assembly sources.

● Extended Instruction Set
An instruction set extended the S1C33 instructions into a form easy to use.
Mainly supports extension of immediate data and offset values into 32 bits, and 3-operand operations.
Supports simple assembler coding.

Principle extended instructions

Classification	Function	Instruction format	Instruction
Extended branch	Branches to entire address space	xjp LABEL	xjp, xcall, xjrgt, xjrge, ---, xjrne and the delayed branch instructions
Extended operation	3-operand operation with 32-bit immediate data	xadd reg, reg, 32-bit value	xadd, xsub, xand, xoor, xxor
Other extended operation	32-bit immediate data operation	xcmp reg, 32-bit value	xcmp, xnot
Extended immediate data substitution	32-bit immediate data substitution	xld.w reg, symbol+32-bit value	xld.w
Extended shift	Shift operation from 0 to 32 bits	xsrl reg, 0–32 and xsrl reg, reg	xsrl, xsll, xsra, ---, xrl
Extended stack relative load	Load and store from/to stack area	xld.w reg, [sp+32bit value]	xld.w, xld.ub, xld.b, xld.uh, xld.h
Extended absolute address load	Load and store from/to absolute addresses	xld.w reg, [symbol+32-bit value]	xld.w, xld.ub, xld.b, xld.uh, xld.h
Extended bit operation	Bit operation on absolute addresses	btst reg, [symbol+32-bit value]	btst, bset, bclr, bnot

● Instruction Extender
Expands the extended instructions into optimized form according to the information delivered from the linker.

● Assembler
Supports relocatable assembly and absolute assembly.

● Linker
Supports a free mapping function that allows software cashing.

● Debugger
A C and Assembly source level debugger.
Supports useful GUI such as seven multi-window and tool bar.
Supports software simulator (core and memory models).
S5U1C33000H, S5U1C330M2S, and S5U1C330C2S can be connected.

● Work Bench
A GUI tool that allows mouse-based control of software tools.

● Debug Monitor (S5U1C330M2S)
Allows on-board debugging with the ROM and RAM on the target board and a serial communication using S5U1C330MxD1.

Hardware tools

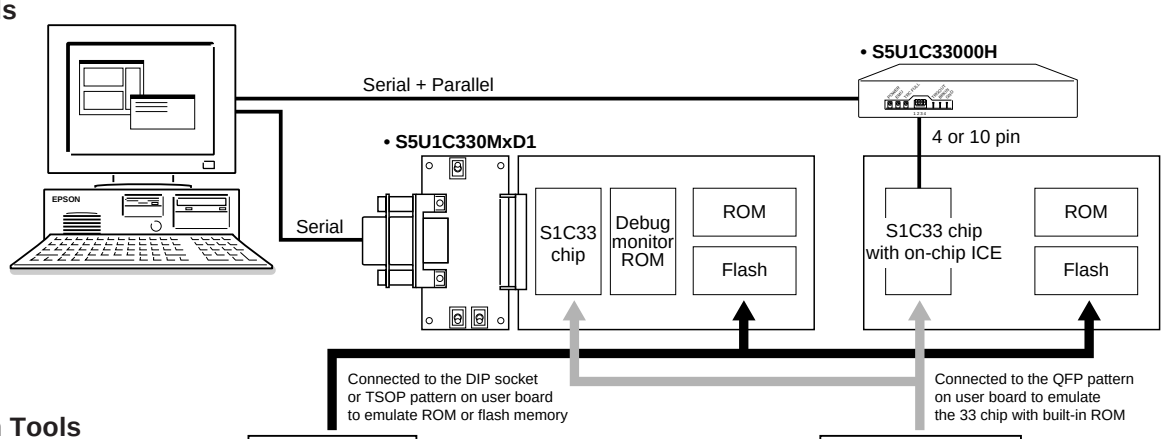
- Reduced-pin type (minimum 4-pin) ICE (S5U1C33000H) for the S1C33209 and later models with on-chip ICE
- Inexpensive debugging environment with the debug monitor S5U1C330M2S and S5U1C330MxD1 I/F board
- S5U1C33xxxEx tools for internal ROM emulation
- S5U1C33xxxMx tools for external memory emulation and enhanced break function

■ DESCRIPTION

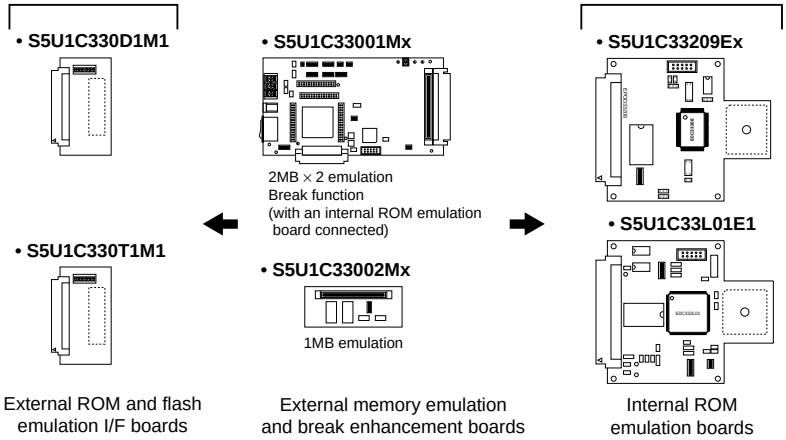
- For the S1C33209 and later models containing on-chip ICE function, development environment with reduced-pin type ICE which can be connected to the terget board with 4 pins (minimum) or 10 pins (standard) is provided. PC trace is supported when connected with 10 pins.
- S5U1C33000H may also be used for ASIC microcomputers with built-in S1C33 macro.
- S5U1C330M2S & S5U1C330MxD1 allows configuration of an inexpensive debug environment by placing the debug monitor S5U1C330M2S on user ROM and connecting it to the debugger through one serial I/F channel and the S5U1C330MxD1 I/F board. (May be used with the S1C33209 and later)
- Capable of emulating the internal ROMs of S1C33209 or later (maximum 50MHz, 0 wait states), S5U1C33xxxEx tools support program development for the internal ROM.
- Capable of emulating external ROM and flash memory, S5U1C33xxxMx tools support program development for external ROM.
- S5U1C33001Mx provides S5U1C33000H with a superior break function comparable to that of the full-function ICE.
- Supports on-board flash erase/programming operation in all debug environments (S5U1C33000H and S5U1C330M2S & S5U1C330MxD1).

■ SYSTEM DIAGRAM

● Basic Tools



● Expansion Tools



■ S1C33 FAMILY DEVELOPMENT ENVIRONMENT LIST

● Software Tools

Tool	Description
S5U1C33000H	In-circuit debugger for the S1C33 chip with on-chip ICE This is a reduced-pin connecting-type ICE requiring only 4 or 10 pins for connection.
S5U1C330M2S + S5U1C330M1D1 (5V) S5U1C330M2D1 (3.3V)	Debug monitor Enables the creation of an inexpensive debug environment using user resources (ROM 10KB, RAM 2.5KB, SIO 1ch.) to connect to the debugger.

● Hardware Expansion Tools

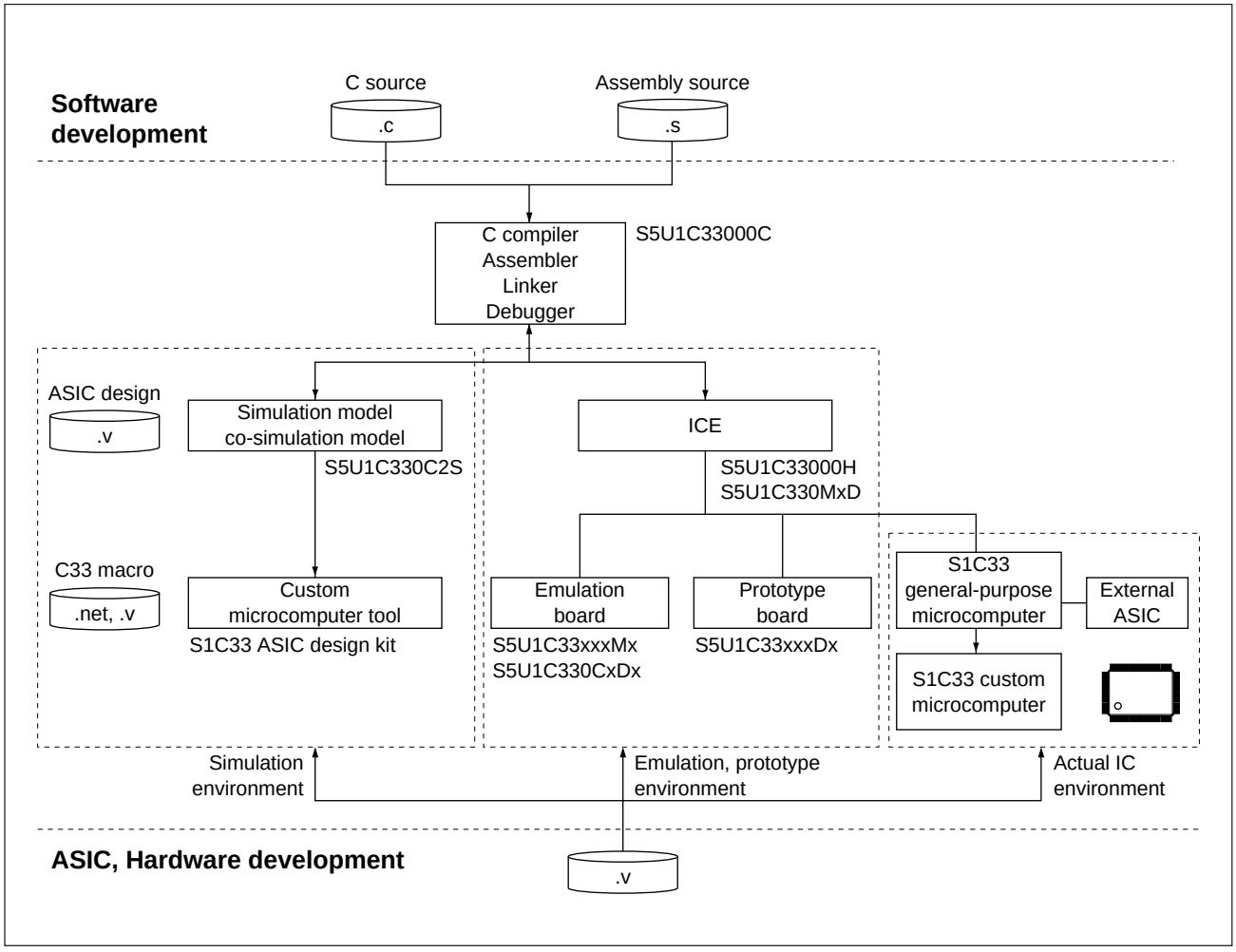
Tool	Description
S5U1C33209E1 (5V) S5U1C33209E2 (3.3V)	Emulation pod for the S1C33209 (with emulation memory board I/F) Note) With the capacity to emulate up to 256KB of internal ROM. (maximum 50MHz, 0 wait state)
S5U1C33L01E1 (3.3V)	Emulation pod for the S1C33L01 (with emulation memory board I/F) Note) Supports ROM development using the internal ROM emulation function. (maximum 50MHz, 0 wait state)
S5U1C33T01E1 (5V) S5U1C33T01E2 (3.3V)	Emulation pod for the S1C33T01 (with emulation memory board I/F) Note) With the capacity to emulate up to 256KB of internal ROM. (maximum 50MHz, 0 wait state)
S5U1C33221E1 (5V) S5U1C33221E2 (3.3V)	Emulation pod for the S1C33221 (with emulation memory board I/F) Note) With the capacity to emulate up to 256KB of internal ROM. (maximum 50MHz, 0 wait state)
S5U1C33240E1 (5V) S5U1C33240E2 (3.3V)	Emulation pod for the S1C33240 (with emulation memory board I/F)
S5U1C33S01E1 (3.3V)	Emulation pod for the S1C33S01 (with emulation memory board I/F) Note) With the capacity to emulate up to 256KB of internal ROM. (maximum 50MHz, 0 wait state)
S5U1C330D1M1 (5–3.3V)	ROM emulation I/F board The DIP socket for the target board ROM and the S5U1C33001Mx/S5U1C33002Mx are connected to emulate ROM. It supports ×16 type of 1M, 2M, 4M, 8M, and 16M-bit ROMs in 40 to 42-pin DIPs.
S5U1C33T1M1 (5–3.3V)	Flash emulation I/F board The S5U1C33001Mx/S5U1C33002Mx is connected to the 48-pin TSOP flash memory board pattern on the target board to emulate flash memory. It supports ×16 type of 4M, 8M, 16M, and 32M-bit flash memory in 48-pin TSOPs.
S5U1C33001M1 (5V) S5U1C33001M2 (3.3V)	2MB × 2 block emulation memory board (accessible with 1 wait state up to 33MHz) When two boards are cascaded, up to 2MB × 4 blocks can be emulated. Powerful break functions for a map break, six bus breaks and two area breaks can also be added to the S5U1C33000H (with S5U1C33xxxEx connected).
S5U1C33002M1 (5V) S5U1C33002M2 (3.3V)	1MB emulation memory board (accessible with 1 wait state, up to 33MHz) When two boards are cascaded, up to 1MB × 2 blocks can be emulated.
S5U1C33003M1 (5V) S5U1C33003M2 (3.3V)	2MB × 2 block emulation memory board (accessible with 1 wait state up to 33MHz) When two boards are cascaded, up to 2MB × 4 blocks can be emulated. This board has no flex10k for expanding break functions but other functions are the same as S5U1C33001Mx.

Note: High-speed SRAM for ROM emulation is a rental option.
S5U1C33001S (for 3.3V), S5U1C33000S (for 5V)

Simulation & emulation tools

■ DESCRIPTION

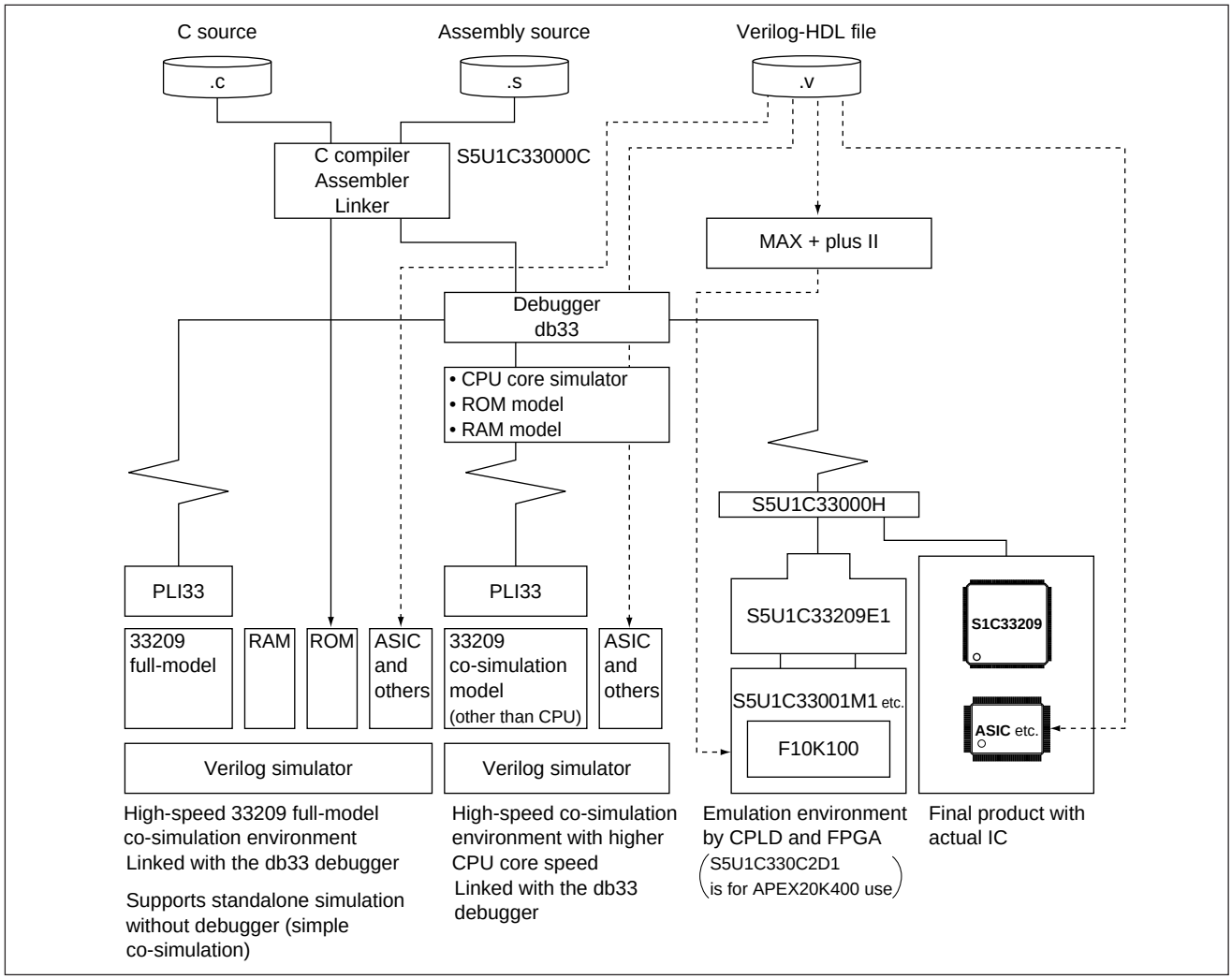
The S1C33 Family offers a total system development environment that allows you to develop software, external ASICs, or ASIC-incorporating custom microcomputers by means of simulation, emulation, prototype boards, or actual IC. This is accomplished by seamless linkage to ordinary software development tools of the ASIC development environment where you perform simulation or emulation.



System development environment

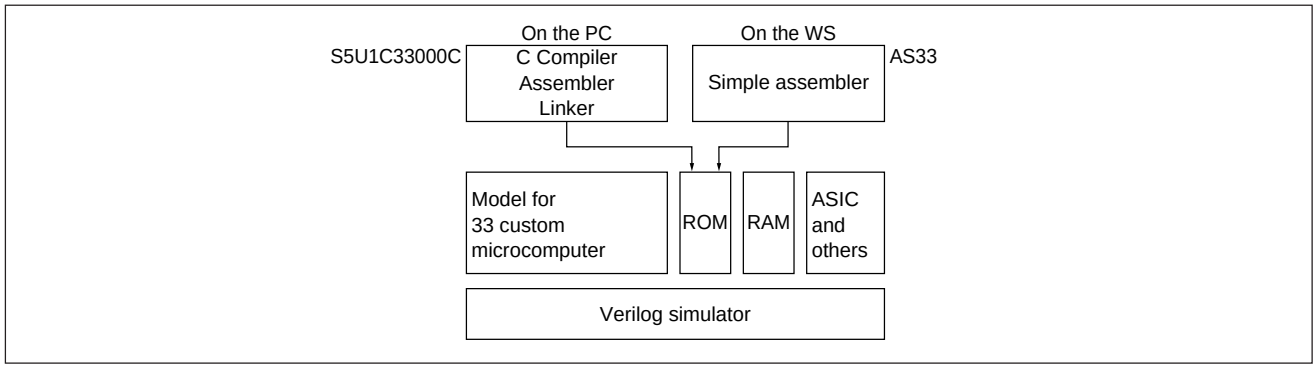
■ S5U1C330C2S

This tool provides co-simulation, and emulation environments for your C source code, assembler source code, or HDL source code written in Verilog HDL language. The separately available Verilog simulator (Verilog-XL, ModelSim), MAX + plusII, Quartus (Altera Corporation), S5U1C33001Mx, and S5U330C2D1 are required.



■ S1C33 ASIC DESIGN KIT

Development environment for custom microcomputers. This tool provides a simulation environment aiming for sign-off of ASIC microcomputers. It is customized before shipment to suit the specifications of your custom microcomputer.

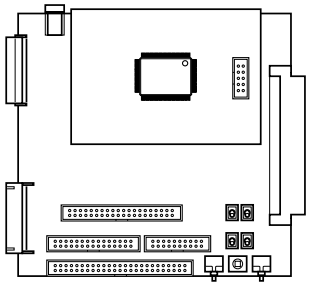


■ PROTOTYPE TOOLS

Centered around S5U1C33xxxDx, these tools provide a development environment in which a prototype can be evaluated beforehand. A wide selection of function-adding sub-boards helps support a combination of various prototypes.

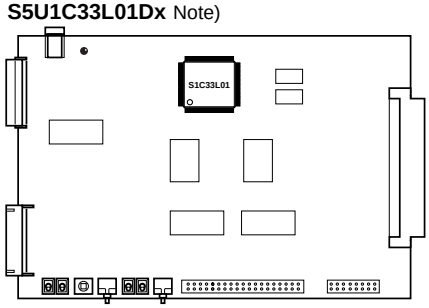
Main boards with an S1C33 chip

S5U1C33209Dx



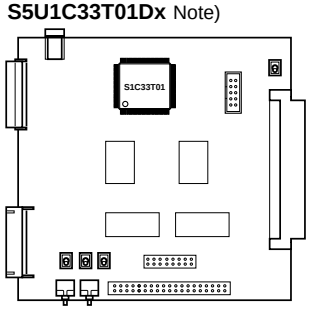
For S1C33209

S5U1C33L01Dx Note)



For S1C33L01

S5U1C33T01Dx Note)



For S1C33T01

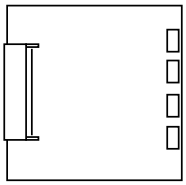
Note: Because the mounted microcomputer has upper compatibility, this tool can also be used for S1C33209 development.

The board contains the following two types of memory:
- Flash memory 1MB × 2
- SRAM 1MB

A 20MHz high-speed clock is available.

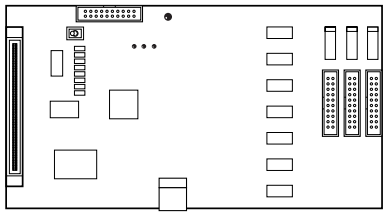
Function-adding sub-boards

S5U1C330AxD1



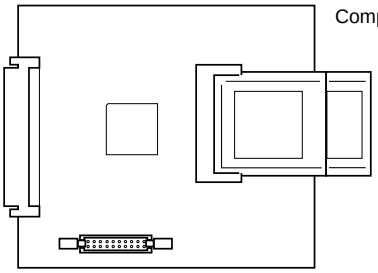
Audio board

S5U1C330U1D1



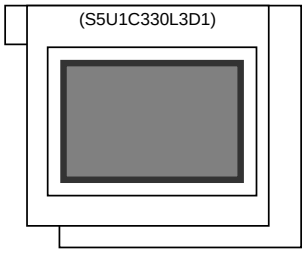
USB board

S5U1C330C1D1



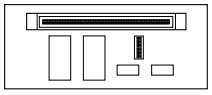
Compact flash board

S5U1C330L2D1, S5U1C330L3D1



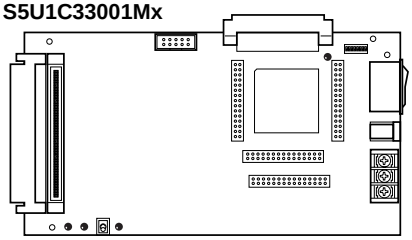
LCD display board (connected to S5U1C33L01Dx only)

S5U1C33002Mx



With 1MB SRAM
Together, two boards provide a maximum memory of 2MB

S5U1C33001Mx



With 4MB SRAM
Supports external ASIC emulation by CPLD

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■ S1C33 FAMILY MIDDLEWARE AND FIRMWARE LIST

Classification	Trade name	Contents (included technology) and sample program operation boards	Model supported
Voice	S5U1C330V1S	Voice compression/expansion and voice processing (VSX, ADPCM, VOX, VSC, PPC)	S1C332xx
		S5U1C33209D1 + S5U1C330A3D1	
	S5U1C330G3S	Voice compression/expansion (G729 Annex-A) Voice expansion (G723.1 Annex-A)	S1C33xxx
		S5U1C33209D1 + S5U1C330A3D1	
	S5U1C330T1S	Simple text to speech (VSX, VSX2)	S1C332xx
		S5U1C33209D1 + S5U1C330A3D12	
	S5U1C330V2S	Voice recognition	S1C332xx
		S5U1C33209D1 + S5U1C330A3D1	
	S5U1C330H1S	Voice recognition using phoneme model (Japanese only)	S1C332xx
		S5U1C33209D1 + S5U1C330A3D1	
Sound	S5U1C330M1S	PWM method simple melody output	S1C332xx
		S5U1C33209D1 + S5U1C330A3D1	
	S5U1C330S1S	MIDI-like sound output based on WAVE sound source (PCM15)	S1C332xx
		S5U1C33209D1 + S5U1C330A3D1	
Image	S5U1C330J1S	JPEG compression/expansion	S1C332xx
		S5U1C33209D1	
	S5U1C330G1S	Graphics and GUI library	S1C33L01
		S5U1C33L01D1 + S5U1C330L2D1/S5U1C330L3D1	
OS	S5U1C330R1S	µITRON3.0 compliant real-time OS	S1C332xx
		All S5U1C33xxxDx boards	
Others	S5U1C330M2S	Debug monitor running on user board	S1C332xx
		All S5U1C33xxxDx boards	
	FLS33	On-board/on-chip flash memory erase/programming routine executable using a debugger (included with S5U1C33000C Ver.2.0 or later)	S1C332xx
		All S5U1C33xxxDx boards	
	S5U1C330P1S	Handwritten character recognition	S1C332xx
		DMT33003 (made by EHK)	
PC I/F	S5U1C330C1S	I/O firmware for compact flash memory, supports DOS file	S1C332xx
		S5U1C33L01D1 + S5U1C330C1D1	
	S5U1C330S2S	I/O firmware for SmartMedia, supports DOS file	S1C332xx
		S5U1C33L01D1 + S5U1C330S1D1	
	S5U1C330U1S	USB sample program	S1C33xxx
		S5U1C33209D1 + S5U1C330U1D1	

■ VOICE COMPRESSION/EXPANSION AND VOICE PROCESSING TECHNOLOGY LIST

Technology name	Contents	Compression rate	Application package
VSX	Technology for performing timebase and silent compression based on ADPCM Supports a sampling rate of 8kHz	About 1/7	S5U1C330V1S S5U1C330T1S
VSX2	An upgraded version of VSX supporting sampling rates of 11.025 to 22.05kHz	About 1/7	S5U1C330T1S
ADPCM	High-speed version of ADPCM technology with the same sound quality as G726 Supports sampling rates of 8 to 22.05kHz	About 1/3	S5U1C330V1S
VOX	Technology for realizing high voice compression rates using voice synthesis technology Supports a sampling rate of 8kHz	About 1/10	S5U1C330V1S
VSC	Technology for changing the speed and pitch of voice by a factor of 1/2 to 2	–	S5U1C330V1S
PPCM	Capable of packing 10-bit PCM data without changing the original sound, using the packed PCM method Supports sampling rates of 8 to 22.05kHz	About 3/4	S5U1C330V1S
PCM15	High-precision 15-bit D/A technology using hybrid PWM, also capable of stereo Supports sampling rates of 16 to 48kHz	–	Evaluation tool in data CD
G729	G729 Annex-A Supports a sampling rate of 8kHz	About 1/10	S5U1C330G3S
G723	G723.1 Annex-A Supports a sampling rate of 8kHz	About 1/10	S5U1C330G3S

■ DEMONSTRATION SOFTWARE LIST

File name	Contents and demonstration boards
dm5s8jVx.exe	S5U1C330V1S Japanese, S5U1C330S1S, S5U1C330M1S, S5U1C330V2S, S5U1C330T1S Japanese (All for 10 bits, 8kHz output)
	S5U1C33209D1 + S5U1C330A3D1
dm5s8eVx.exe	S5U1C330V1S English, S5U1C330S1S, S5U1C330M1S, S5U1C330V2S (All for 10 bits, 8kHz output)
	S5U1C33209D1 + S5U1C330A3D1
dm5s16Vx.exe	VSX2 (10 bits, 16kHz),VSX2 (10 bits, 22kHz), text to speech (10 bits, 16kHz) (All contents in Japanese)
	S5U1C33209D1 + S5U1C330A3D1
dm7s22Vx.exe	MIDI-like sound output (15 bits, 22kHz, stereo), 2ch melody differential outputs
	S5U1C33209D1 + S5U1C330A3D1
dm7s32Vx.exe	PCM15 guitar sound (15 bits, 32kHz, mono)
	S5U1C33209D1 + S5U1C330A3D1
dm7s3bVx.exe	PCM15 beatmania (15 bits, 32kHz, mono)
	S5U1C33209D1 + S5U1C330A3D1
dm7s3cVx.exe	MIDI-like sound output (15 bits, 32kHz stereo, mono)
	S5U1C33209D1 + S5U1C330A3D1
dm6g26Vx.exe	LCD display demonstration for S5U1C330L2D1 panel
	S5U1C33L01D1 + S5U1C330L2D1
dm6g37Vx.exe	LCD display demonstration for S5U1C330L3D1 panel
	S5U1C33L01D1 + S5U1C330L3D1
dm6guiVx.exe	Graphics, GUI
	S5U1C33L01D1 + S5U1C330L2D1, S5U1C33L01D1 + S5U1C330L3D1
dm6cfVx.exe	Compact flash
	S5U1C33L01D1 + S5U1C330C1D1
dm6cmbVx.exe	Middleware demo collection (S5U1C330J1S, S5U1C330C1S, S5U1C330G1S, S5U1C330R1S, PCM15)
	S5U1C33L01D1 + S5U1C330A3D1 + S5U1C330C1D1 + S5U1C330L2D1
dm3pnVx.exe	Handwritten character recognition
	DMT33003 (made by EHK) + ROM writer
dm3smVx.exe	SmartMedia
	S5U1C33L01D1 + S5U1C330S1D1
dm7hmmVx.exe	Voice recognition using phoneme model
	S5U1C33209D1 + S5U1C330A3D1
dm7s4Vx.exe	G729, G723 playback
	S5U1C33209D1 + S5U1C330A3D1
dm7s5Vx.exe	G729 recording/playback
	S5U1C33209D2 + S5U1C33209E2 + S5U1C330A3D1 + S5U1C33000H1

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List of Hardware Resources used by Middleware

The following lists the default hardware resources used by each middleware. The resources to be used may be changed by modifying the source program opened to the user. Refer to each middleware manual for details.

■ S5U1C330V1S, S5U1C330G3S

- 16-bit timer 0 ..... A/D conversion trigger generation
- 16-bit timer 1 ..... 10-bit PWM output
- 16-bit timer 5 ..... PWM trigger generation
- A/D converter 0 ..... Voice input
- P23 ..... 10-bit PWM output
- K60 ..... Voice input

■ S5U1C330T1S

- 16-bit timer 0 ..... A/D conversion trigger generation (VSX2 voice input)
- 16-bit timer 1 ..... 10-bit PWM output
- 16-bit timer 5 ..... PWM trigger generation
- A/D converter 0 ..... Voice input (VSX2 voice input)
- P23 ..... 10-bit PWM output
- K60 ..... Voice input

■ S5U1C330V2S

- 16-bit timer 0 ..... A/D conversion trigger generation
- A/D converter 0 ..... Voice input
- K60 ..... Voice input

■ S5U1C330M1S

For single channel output

- 16-bit timers 0, 1, 2 and 3, and one related port

For 3-channel simultaneous output

- 16-bit timers 0, 1 and 2, and the related ports

For direct driving a piezoelectric buzzer

- 16-bit timers 0, 1, 2 and 3, and the related ports

List of Hardware Resources used by Middleware

■ S5U1C330S1S

For 15-bit stereo output

- 16-bit timer 1 ..... 9-bit PWM output, L channel
- 16-bit timer 2 ..... 9-bit PWM output, R channel
- 16-bit timer 3 ..... 6-bit PWM output, L channel
- 16-bit timer 4 ..... 6-bit PWM output, R channel
- 16-bit timer 5 ..... Sampling trigger generation
- P23 ..... 9-bit PWM output, L channel
- P24 ..... 9-bit PWM output, R channel
- P25 ..... 6-bit PWM output, L channel
- P26 ..... 6-bit PWM output, R channel

For 15-bit mono output

- 16-bit timer 1 ..... 9-bit PWM output
- 16-bit timer 3 ..... 6-bit PWM output
- 16-bit timer 5 ..... Sampling trigger generation
- P23 ..... 9-bit PWM output
- P25 ..... 6-bit PWM output

For 10-bit mono output

- 16-bit timer 1 ..... 10-bit PWM output
- 16-bit timer 5 ..... Sampling trigger generation
- P23 ..... 10-bit PWM output

■ S5U1C330J1S

No peripheral circuit is used.

■ S5U1C330G1S

- 16-bit timer 3 ..... GUI key sampling

■ S5U1C330R1S

- One 16-bit timer or 8-bit timer channel ..... System clock

■ S5U1C330M2S

- One serial interface channel and the related port

■ FLS33

No peripheral circuit is used.

■ S5U1C330C1S

- K62 ..... Port input interrupt 2
- P32 ..... Port input interrupt 6
- P33 ..... Port input interrupt 7

■ S5U1C330U1S

- P7 ..... XINT
- K51 ..... DMAREQ1
- P33 ..... DMAACK1
- One high-speed DMA channel ..... for DMA transfer

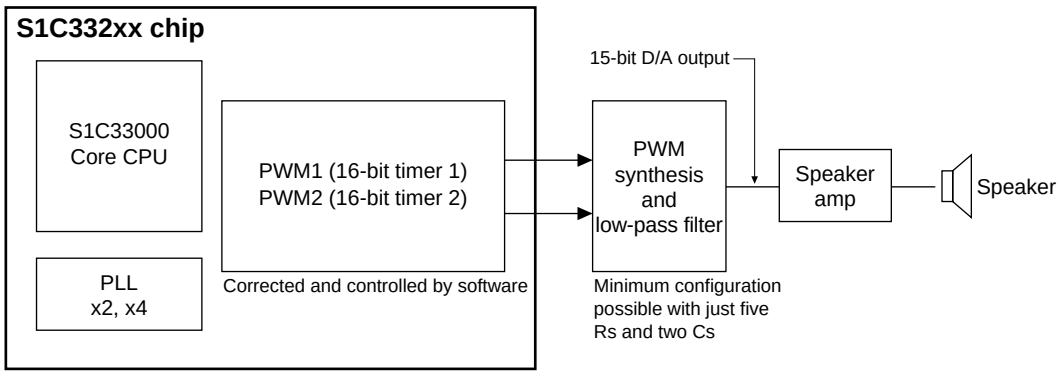
S1C33 Family D/A Technology PCM15

- High-precision D/A technology for the S1C332xx series
- Maximum 15 bits of precision in voice band using hybrid PWM technology; may be output in sampling frequencies up to 48kHz
- Able to realize CD-quality sound using only a microcomputer and several RC components

■ FEATURES

- Seiko Epson's original hybrid PWM technology allows the product to support a maximum 15 bits of precision and 8kHz to 48kHz sampling frequencies, enabling CD-quality sound at extremely low cost.
- The hybrid PWM technology is comprised of the following three PWM technologies:
  1. Fine-PWM technology
     Control of PWM in units of half-clock cycles allows production of vouice/music output with a maximum 10 bits of precision on even a single channel.
  2. Dual PWM technology
     Synthesizing two channels of the above fine PWM allows it so produce voice/music output with a maximum 15 bits of precision.
  3. Software-adjusted PWM technology
     By correcting PWM output through software processing, it realizes 0.01% accurate high-precision linearity error.
- Support will be provided for a wide range of products, from uncompressed PCM data to sound reproduction and voice expansion middleware to be released in the near future.
- Able to accommodate stereo output.
- May be used in all microcomputers, from the S1C332xx series to ASIC microcomputers built on 33 macros.
- Ideally suited for data banks with music functions, PDAs, electronic stationery, electronic toys, and mobile audio equipment.

■ HARDWARE CONFIGURATION



Refer to the "S1C33 Family Application Note", for details.

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EPSON

S1C33 Family S5U1C330R1S Middleware

Realtime OS middleware

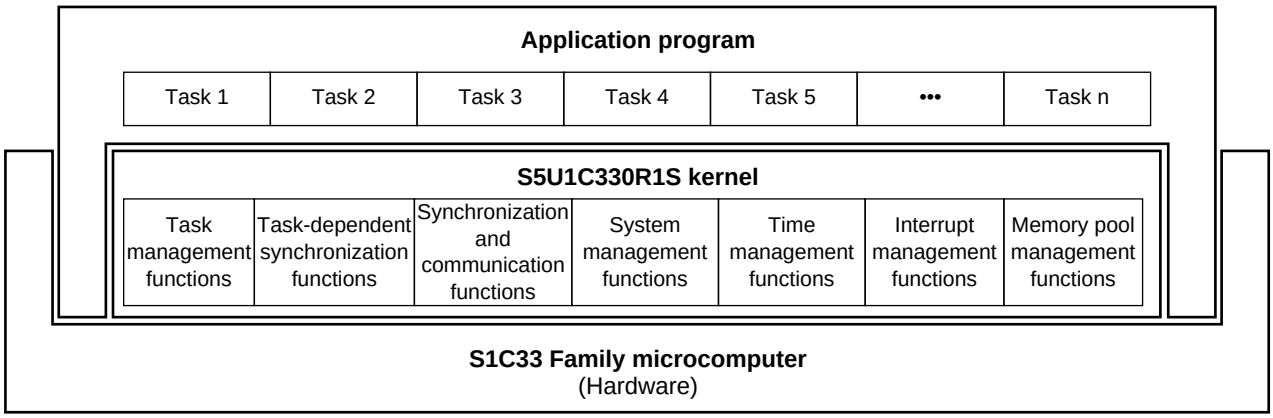
- Realtime OS for S1C33 Family
- Suport µITRON 3.0
- Optimize for S1C33 Family

■ DESCRIPTION

- The S5U1C330R1S is a realtime operating system for the S1C33 Family of single-chip microcomputers. Complies with µITRON3.0 specifications.
- Compact and high-speed kernel optimized for use in the S1C33 Family.
- The S5U1C330R1S is released with a CD-ROM including all source code, library and sample programs. So you can customize the S5U1C330R1S for your system.
- Multiple tasks can share a common stack area (when not processed in parallel). You can minimize the amount of RAM used in your system by your application.
- Using S5U1C330R1S in your design enables you to quickly and efficiently develop embedded applications for printers, PDAs, FA products and various types of control equipment.

■ FEATURES

● System Diagram



● Memory Requirements and Speed

Kernel size*1: ROM: 9.8K bytes
RAM: 2.4K bytes
Dispatch time*2: 13.6 µs (CPU: 40MHz, Bus: 20MHz)

∗1 Number of tasks = 8, number of priority levels = 8, number of event flags = 8, number of semaphore = 8, number of mailboxes = 8, number of message buffers = 8, number of variable-size memory pools = 8, number of fixed-size memory pools = 8, number of cyclic handlers = 8 and number of alarm handlers = 8

∗2 Tasks of the same priority were switched over by a rot_rdq system call.

These are standard values for a guide and will vary according to the user's system environment and the make condition. The net value should be evaluated on the actual system.

● **System Call List**

Classification	System call	Function
Task management	**dis_dsp( )**	Disable Dispatch
	ena_dsp( )	Enable Dispatch
	sta_tsk( )	Start Task
	ext_tsk( )	Exit Issuing Task
	ter_tsk( )	Terminate Other Task
	chg_pri( )	Change Task Priority
	rot_rdq( )	Rotate Tasks on the Ready Queue
	rel_wai( )	Release Wait of Other Task
	get_tid( )	Get Task Identifier
	exd_tsk( )	Exit and Delete Task
	ref_tsk( )	Reference Task Status
Task-dependent synchronization	**slp_tsk( )**	Sleep Task
	tslp_tsk( )	Sleep Task with Time-out
	wup_tsk( )	Wake Up Other Task
	sus_tsk( )	Suspend Other Task
	rsm_tsk( )	Resume Suspended Task
	can_wup( )	Cancel Wake Up Request
Synchronization and communication	**wai_sem( )**	Wait on Semaphore
	preq_sem( )	Poll and Request Semaphore
	twai_sem( )	Wait on Semaphore with Timeout
	sig_sem( )	Signal Semaphore
	ref_sem( )	Reference Semaphore Status
	rcv_msg( )	Receive Message from Mailbox
	prcv_msg( )	Poll and Receive Message from Mailbox
	trcv_msg( )	Receive Message from Mailbox with Timeout
	snd_msg( )	Send Messages to Mailbox
	ref_mbx( )	Reference Mailbox Status
	wai_flg( )	Wait Event Flag
	pol_flg( )	Poll Event Flag
	twai_flg( )	Wait Event Flag with Timeout
	set_flg( )	Set Event Flag
	clr_flg( )	Clear Event Flag
	ref_flg( )	Reference Event Flag Status
Extended synchronization and communication	**snd_mbf( )**	Send Messages to Message Buffer
	psnd_mbf( )	Poll and Send Messages to Message Buffer
	tsnd_mbf( )	Send Messages to Message Buffer with Timeout
	rcv_mbf( )	Receive Messages from Message Buffer
	prcv_mbf( )	Poll and Receive Messages from Message Buffer
	trcv_mbf( )	Receive Messages from Message Buffer with Timeout
	ref_mbf( )	Reference Message Buffer Status
System management	**get_ver( )**	Get Version Information
	ref_sys( )	Reference System Status
Time management	**set_tim( )**	Set System Clock
	get_tim( )	Get System Clock
	dly_tsk( )	Delay Task
	def_cyc( )	Define Cyclic Handler
	act_cyc( )	Activate Cyclic Handler
	def_alm( )	Define Alarm Handler
	ref_cyc( )	Reference Cyclic Handler Status
	ref_alm( )	Reference Alarm Handler Status
	ret_tmr( )	Return from Cyclic/Alarm Handler
Interrupt management	**loc_cpu( )**	Lock CPU
	unl_cpu( )	Unlock CPU
	ret_int( )	Return from Interrupt Handler
Memory pool management	**get_blk( )**	Get Variable-size Memory Block
	pget_blk( )	Poll and Get Variable-size Memory Block
	tget_blk( )	Get Variable-size Memory Block with Timeout
	rel_blk( )	Release Variable-size Memory Block
	get_blf( )	Get Fixed-size Memory Block
	pget_blf( )	Poll and Get Fixed-size Memory Block
	tget_blf( )	Get Fixed-size Memory Block with Timeout
	rel_blf( )	Release Fixed-size Memory Block
	ref_mpl( )	Reference Variable-size Memory Pool Status
	ref_mpf( )	Reference Fixed-size Memory Pool Status
Implementation-dependent functions	**ent_int( )**	Initialize Interrupt Handler Value
	vcre_tsk( )	Create Task
	vcre_mbf( )	Create Message Buffer
	vcre_mpl( )	Create Variable-size Memory Pool
	vcre_mpf( )	Create Fixed-size Memory Pool
	sys_clk( )	System Clock
	vchg_semcnt( )	Change Semaphore Count Value
	vchk_timer( )	Check Time Management Function

EPSON

S1C33 Family S5U1C330M2S Middleware

Debug monitor

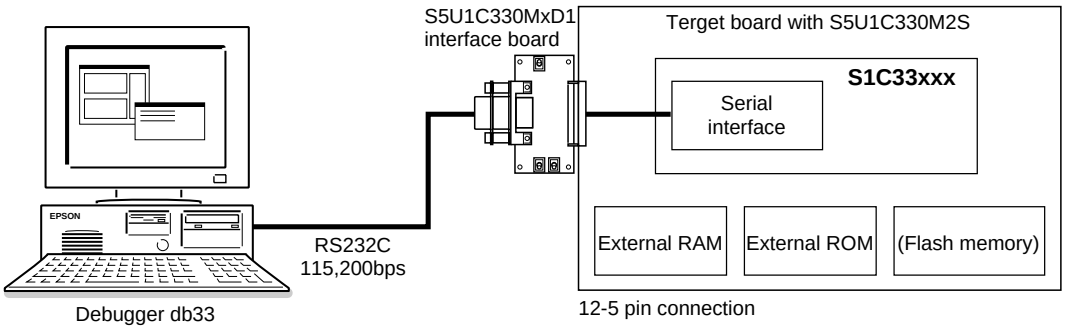
- Debug monitor for the S1C33 Family
- Runs on the target board providing a low-cost debug environment
- Controlled with the debugger in a PC through the S5U1C330MxD1 I/F board

■ FEATURES

- S5U1C330M2S is the debug monitor program for the S1C33 Family.
- Works on the user board by linking with the user program.
- Approx. 10KB ROM, approx. 2.5KB RAM and 1 ch of SIO are required for S5U1C330M2S operation. No interrupt resource is used.
- The debug monitor on the target board is controlled by the db33 debugger in the PC connected via the S5U1C330MxD1 board with the RS232C cable. S5U1C330M1D1 for 5V system and S5U1C330M2D1 for 3.3V system are available. They support 115,200bps data transfer, and are connected to the user board with 12 pins (standard) or 5 pins (minimum).
- S5U1C330M2S supports basic debug functions such as program downloading to RAM and Flash memory, memory dump, register read/write, stepping, program running, and PC break function.
- The S5U1C330M2S middleware including all source codes is provided with a CD-ROM. Simple I/F method of S5U1C330M2S allows easy implementation with the user program.
- The debugging environment does not need the ICE. The S5U1C330M2S debugging environment can be implemented to the final product.

■ DESCRIPTION

● Hardware System



● Software System

User software	Application			
S5U1C330M2S library	**S5U1C330M2S library** Start with m_mon_start (init functions)			RS232C Initialize, Read/Write
Hardware	S1C33 chip	ROM 10KB	RAM 2.5KB	SIO–S5U1C330MxD1

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EPSON

S1C33 Family S5U1C330V1S Middleware

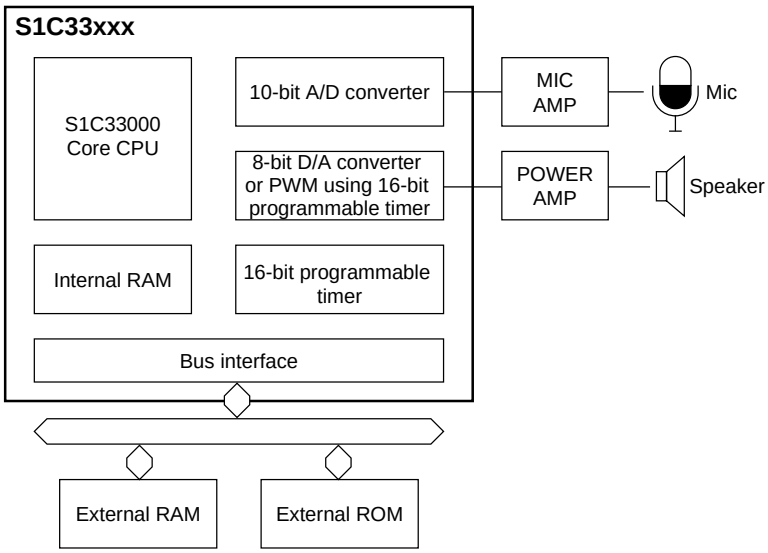
Voice compression and decompression middleware

- Voice compression and decompression middleware for the S1C33 Family
- Voice compression, decompression, and speed and pitch change supported
- Real-time execution in an S1C33 chip

■ FEATURES

- Voice middleware for the S1C33 Family is provided in the form of a linkable library in a CD-ROM.
- Compression, decompression, a speaking part with D/A (PWM) and a listening part with A/D are included in the library.
- Seiko Epson exclusive voice compression technologies VOX and VSX provide voice compression and de-compression with a high compression ratio. (In the case of VOX, an 8MHz sampled voice can be compressed to 8kbps standard to max 2kbps and various compression ratios can be selected.)
- With voice processing technology VSC, the voice speed can be changed from x2 to x1/4, and the voice pitch can be changed from x2 (high) to x1/3 (low).
- Supports PCM and ADPCM (40kbps, 32kbps, 24kbps, 16kbps).
- Suitable for voice memos, data banks with voice, PDA with voice, digital stationery with voice and digital toys with voice.

■ HARDWARE CONFIGURATION



■ MEMORY REQUIREMENTS AND SPEED

● Memory Requirements (byte)

	Internal RAM (0 wait)	ROM
VSX:	5.3K	17K
ADPCM:	4.5K	16K
VOX:	5.8K	13K

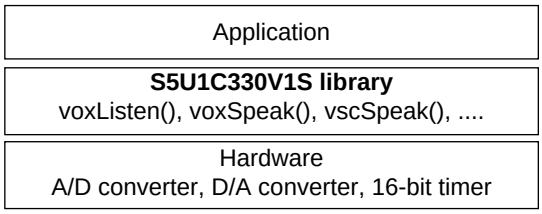
● Speed (CPU occupancy during 20MHz operation)

	Playback	Recording
VSX:	26%	55%
ADPCM:	50%	63%
VOX:	22%	85%

■ SOFTWARE CONFIGURATION

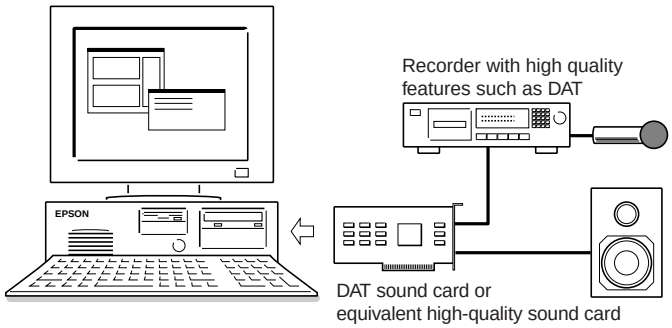
● S5U1C330V1S Library

Libraries with voice subroutines that are called from the user's application.

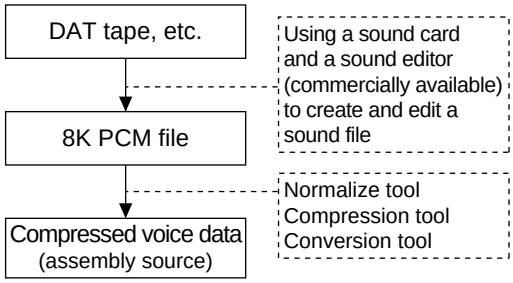


● S5U1C330V1S Data Creation Tool

This tool creates compressed voice ROM data for replay only.
It can be used with Windows95/NT4.0, or higher versions.

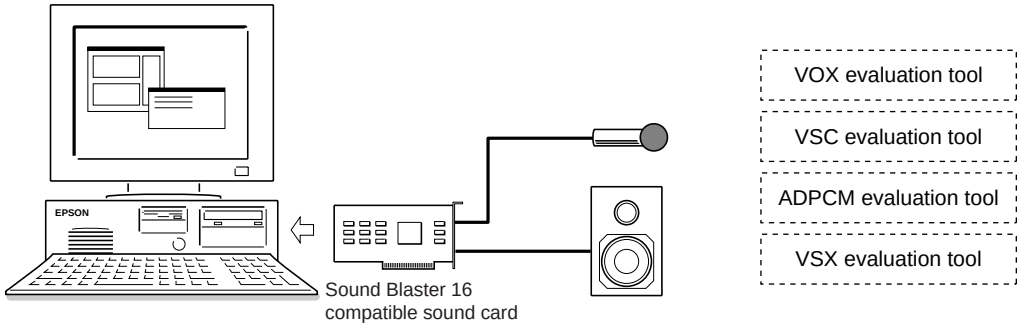


Flow in PC (Example)



● S5U1C330V1S Evaluation Tool

This is an evaluation tool for VOX and VSC technology using a sound board on a PC.
It can be used with Windows95/NT4.0, or higher versions.



∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330M1S Middleware

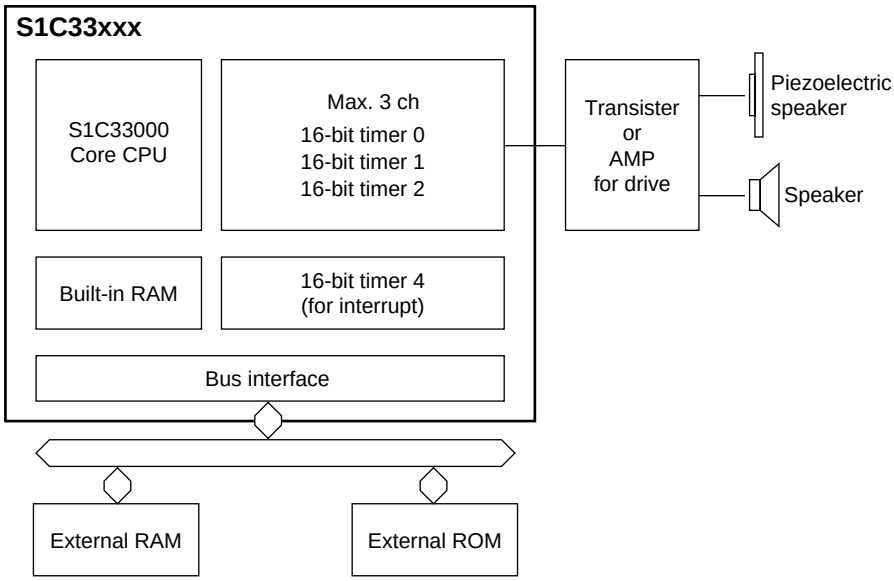
Melody playing middleware

- Melody playing middleware for the S1C33 Family
- Supports simple PWM method similar to general melody ICs
- Max. 3-channel simultaneous outputs
- Supports in an S1C33 chip

■ FEATURES

- Middleware for the S1C33 Family is provided as a linkable library.
- Melody is output with 60Hz to 4kHz PWM waveforms using 16-bit timers.
- Melody tools allow input of music and evaluation of melody output on the PC.
- Compact data and library size (melody data: 2 bytes per note, library: 1.5K bytes) that needs only a small ROM area.
- Suitable for data banks, PDAs, toys with a melody function.

■ HARDWARE CONFIGURATION



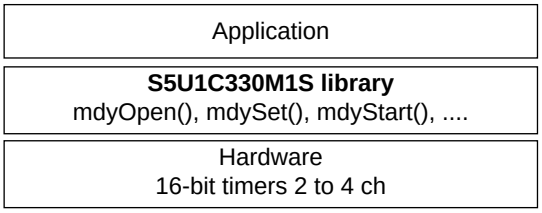
■ RESOURCE

ROM size : Melody library = approx. 1.5K bytes, Melody data = approx. 2 bytes per note
RAM size : Approx. 150 bytes
Timer : 16-bit timer 4 is used for generating an interrupt
Melody output : One 16-bit timer is used for each output channel

■ SOFTWARE CONFIGURATION

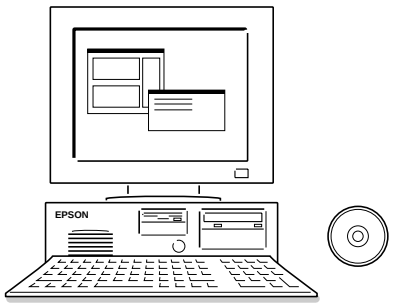
● S5U1C330M1S Library

Libraries with melody subroutines that are called from the user's application.

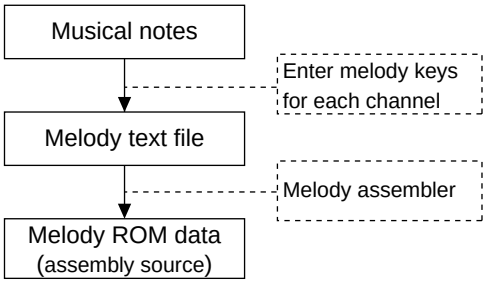


● **S5U1C330M1S Data Creation Tool**

This tool creates melody ROM data.
It can be used with Windows 95/98/NT4.0, or higher versions.

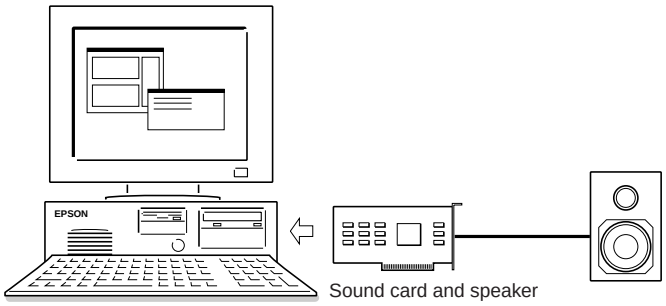


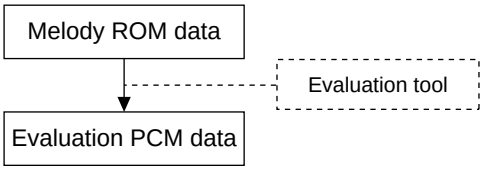
Flow in PC (Example)



● **S5U1C330M1S Evaluation Tool**

This tool is for evaluating melody data on a PC.
It can be used with Windows 95/98/NT4.0, or higher versions.





∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330S1S Middleware

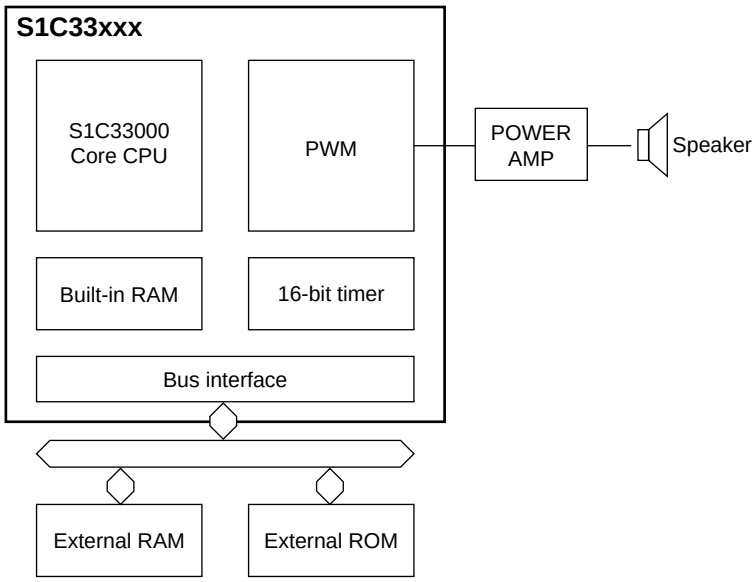
Sound playing middleware

- Sound playing middleware for the S1C33 Family
- Supports musical instruments with the WAVE table method
- 50 ch (monaural, 8kHz sampling)/40MHz playable in real time

■ FEATURES

- Middleware for the S1C33 Family is provided as a linkable library.
- Produces 15-bit stereo sound at a sampling frequency of 8 to 32kHz.
- Sound tools allow input of music and evaluation of sound output on the PC. Also available is a converter for converting MIDI files to S5U1C330S1S sound files.
- Compact data and library size (sound data: 3 bytes per note, instrument data: 4K to 8K bytes (8kHz sampling) per instrument) that needs only a small ROM area.
- Suitable for data banks, PDAs, toys with a sound function.

■ HARDWARE CONFIGURATION



■ RESOURCE

ROM size	:	Sound library = approx. 3K bytes, instrument = 4K to 8K bytes (8kHz sampling), sound data = approx. 3 bytes per note
RAM size	:	Approx. 3K bytes for library use, and 80 bytes for each play channel.
Timer	:	16-bit timer 5 is used for generating an interrupt
Sound outputs (PWM)	:	Uses 16-bit timers 1 through 4 (for 15-bit stereo output).

■ INSTRUMENTS SUPPORTED

Supports the 20 types of musical instruments given below as a standard feature. You also can create musical instrument data and register it as a new entry to S5U1C330S1S.

Non-percussion instruments (12 types)

Piano, Harpsichord, Celesta, Organ, Guitar, Bass, Electric Guitar, Violin, Trumpet, Clarinet, Piccolo, Flute

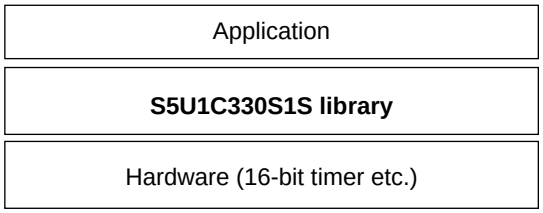
Percussion instruments (8 types)

Bass Drum, Side Stick, Snare, Tom, Crash Cymbal1, Hi-Hat, Bongo, Triangle

■ SOFTWARE CONFIGURATION

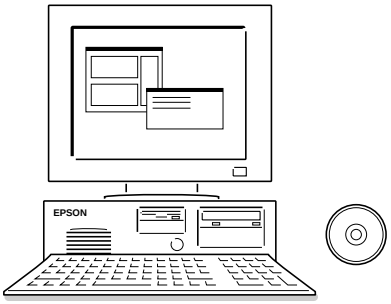
● S5U1C330S1S Library

Libraries with sound subroutines that are called from the user's application.

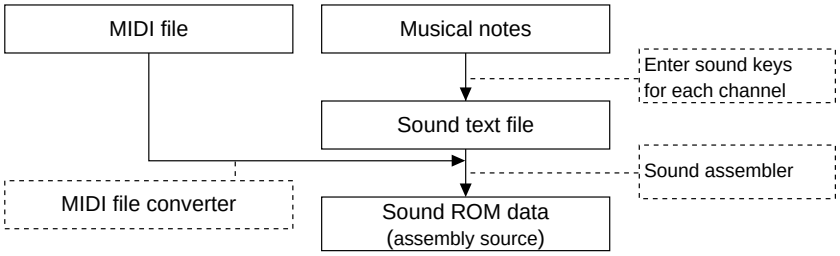


● S5U1C330S1S Data Creation Tool

This tool creates sound ROM data.
It can be used with Windows 95/98/NT4.0, or higher versions.

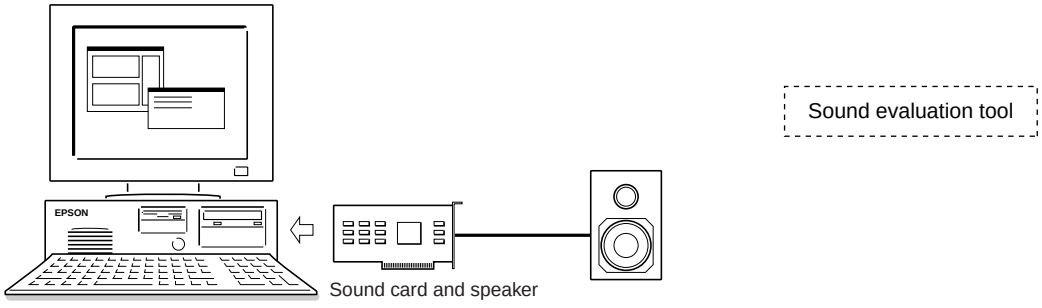


Flow in PC (Example)



● S5U1C330S1S Evaluation Tool

This tool is for evaluating sound data on a PC.
It can be used with Windows 95/98/NT4.0, or higher versions.



∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330T1S Middleware

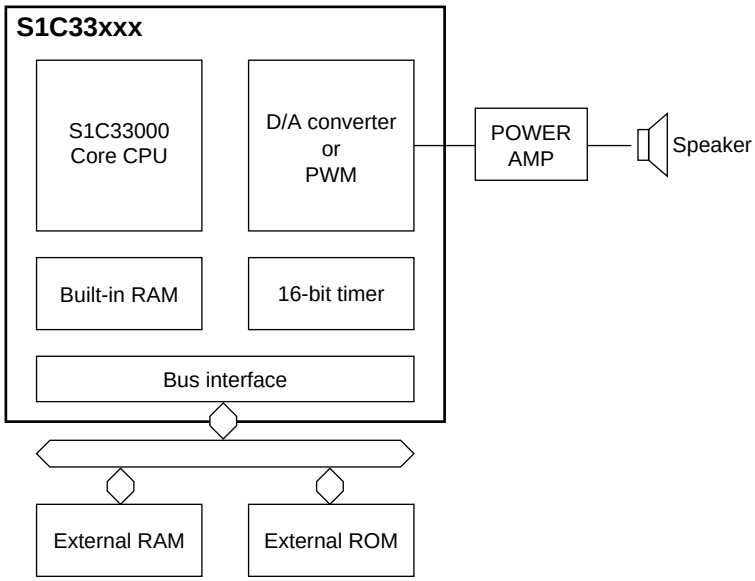
Text to speech middleware

- Text to speech middleware for the S1C33 Family
- Generates more natural speech by adjusting parameters for each phoneme
- Comes with VSX2, a high sampling rate version of VSX

■ FEATURES

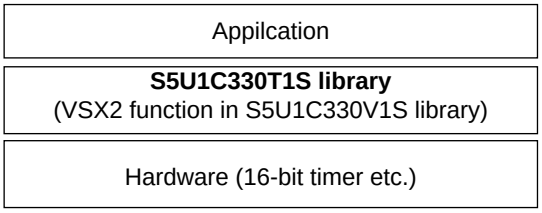
- The text-to-speech middleware for the S1C33 Family, this generates speech from Japanese text using phoneme data compressed by VSX (8kHz) or VSX2 (11.025 to 22.05kHz). Available in linkable library form.
- Speech can also be generated from your original registered words, with support for other languages aside from Japanese.
- A VSX2 speech compression/expansion technology supporting sampling rates of 11.025kHz, 16kHz, and 22.05kHz has just been introduced.
- The sound volume, pitch, length, and silent length between phonemes can be individually adjusted for each phoneme, for a more natural speech quality closer to actual speech.
- Running on a PC, the S5U1C330T1S tools allow you to adjust output parameters as well as evaluate sound quality before final production.
- The standard Japanese language phoneme data can be stored in approximately 100KB of memory (for a sampling frequency of 16kHz).
- The library program is about 15KB in size.
- Ideally suited for vending machines, PDA, electronic toys, and electronic stationery.

■ HARDWARE CONFIGURATION



■ SOFTWARE CONFIGURATION

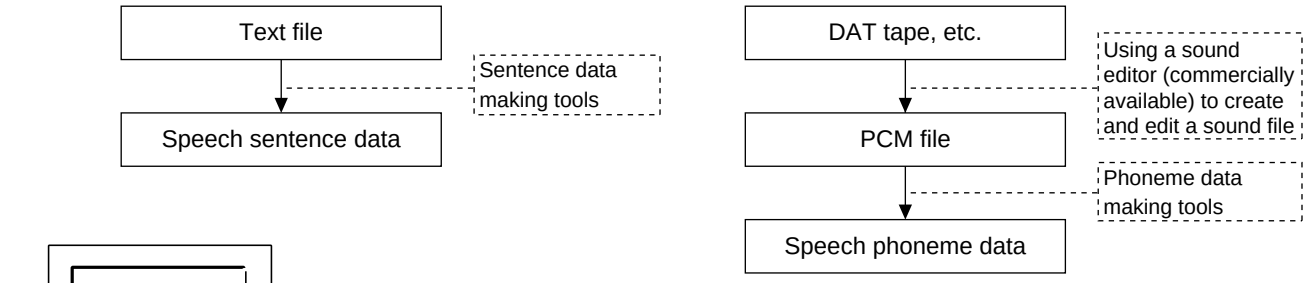
● **S5U1C330T1S Library**

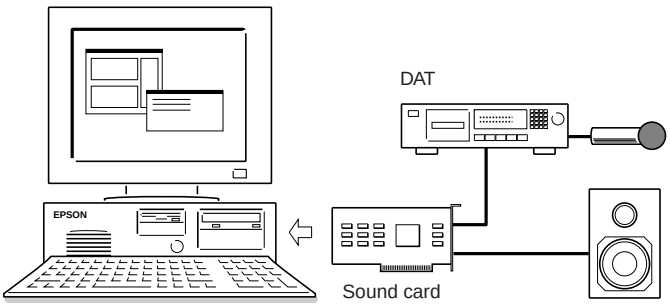


● **S5U1C330T1S Data Creation Tool**

This tool creates sentence data and phoneme (word) data.
It can be used with Windows 95/98/NT4.0, or higher versions.

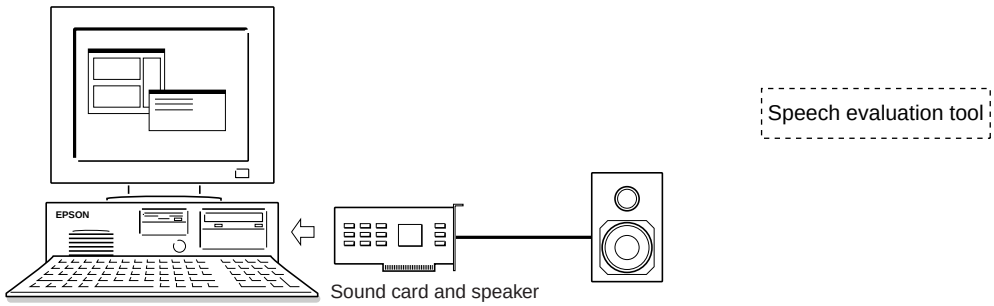
Flow in PC (Example)





● **S5U1C330T1S Evaluation Tool**

This is a GUI tool used to evaluate speech generated by S5U1C330T1S, using a PC sound board.
It can be used with Windows 95/98/NT4.0, or higher versions.



∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330V2S Middleware

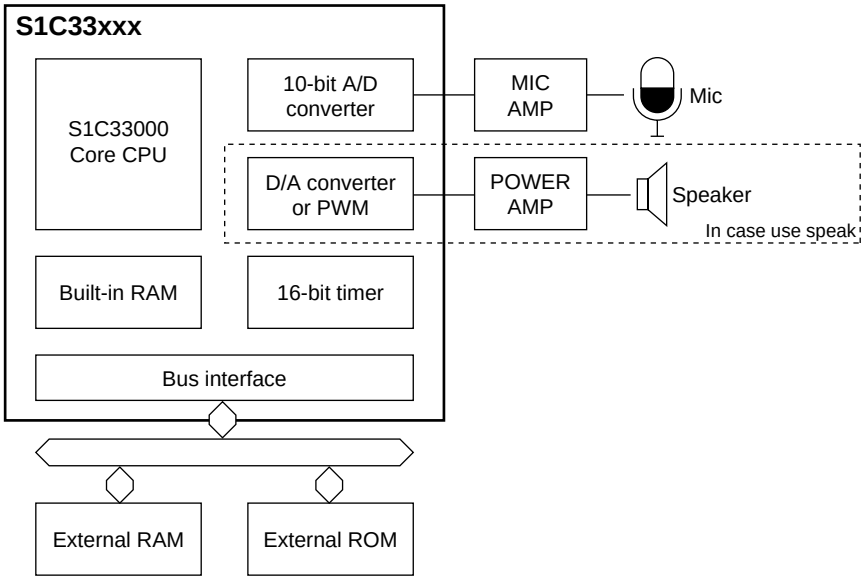
Voice recognition engine middleware

- Speech recognition middleware for the S1C33 Family
- Real-time execution in an S1C33 chip
- PC tools for making speech recognition ROM data

■ FEATURES

- Speech recognition middleware for the S1C33 Family is provided in the form of a linkable library.
- The speech recognition engine and a listening routines using an A/D converter are included in the library. Data decompression and speaking routines with a D/A converter or PWM can be implemented using the S5U1C330V1S library.
- Using the Seiko Epson exclusive isolated word recognition technology, 20 to 100 words can be recognized in real-time.
- 2 types of recognition methods are available; Speaker Independent Recognition for which data is created on a PC, and Speaker Dependent Recognition that allows direct word-registration on products.
- PC tools for evaluating the speech recognition engine are provided.
- Evaluation boards (S5U1C33209D1, S5U1C330A3D1, S5U1C330M1D1) are provided.
- Suitable for PDAs, digital stationeries and digital toys.

■ HARDWARE CONFIGURATION

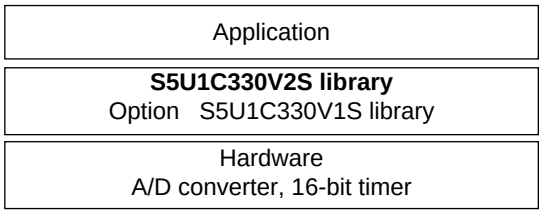


■ MEMORY REQUIREMENTS AND SPEED

- RAM ..... 5K bytes
- ROM
  Program ..... 27K bytes
  Dictionary data for recognition (Cepstrum) ..... 1,280 bytes/second
  Dictionary data for recognition (VQCode) ..... 128 bytes/second
- Recognition speed
  20MHz operation, recognition dictionary: 30 words ..... 0.54 seconds
  (Approximately 0.7 seconds for single dictionary entries such as "Good morning" or "Good afternoon")

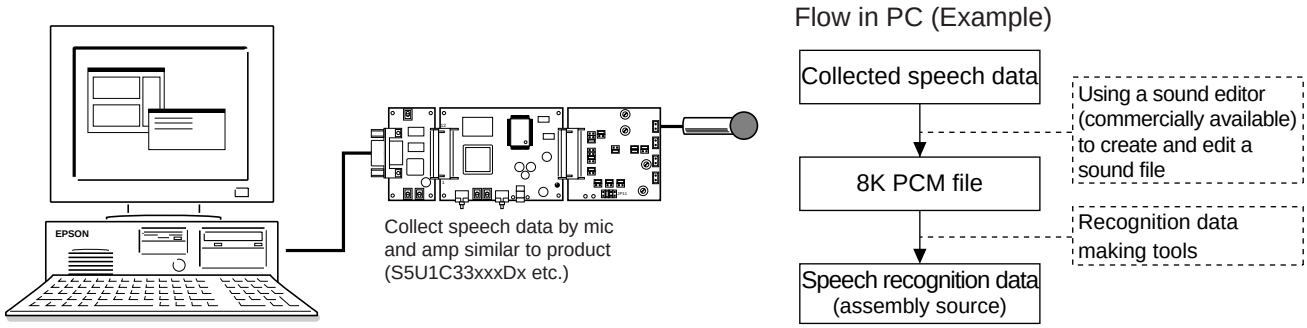
■ SOFTWARE CONFIGURATION

● S5U1C330V2S Library



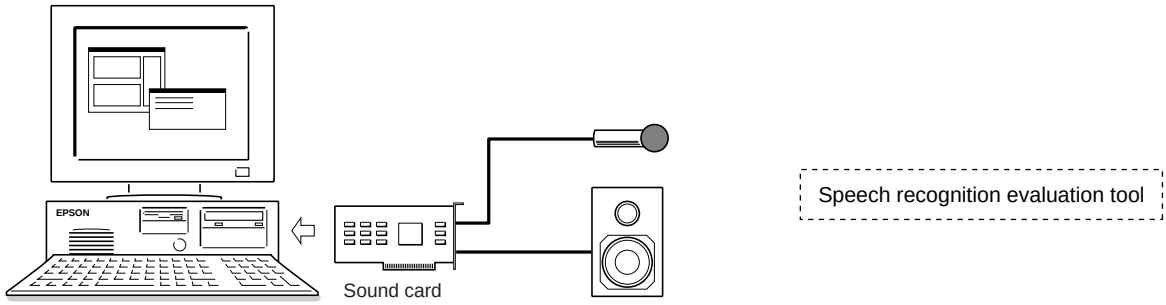
● S5U1C330V2S Data Creation Tool

This tool creates speech recognition ROM data. It can be used with Windows95/98/NT4.0, or higher versions.



● S5U1C330V2S Evaluation Tool

This is an evaluation tool for the S5U1C330V2S recognition engine using the sound board on a PC. It can be used with Windows95/98/NT4.0, or higher versions with GUI.



∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330J1S Middleware

Image compression and decompression middleware

- JPEG image compression and decompression middleware for the S1C33 Family
- Monochrome, RGB, YUV image-processing function supported
- PC tools to convert a JPEG compressed image into ROM data

■ FEATURES

- Image middleware for the S1C33 Family is provided in the form of a linkable library in a CD-ROM.
- This middleware conforms to JPEG baseline and is compatible with a great deal of JPEG data.
- Compress and decompress the image of B/W, grayscale, RGB color and YUV color.
- Compression ratios including <YCbCr> 4:4:4, 4:2:2 and 4:1:1 can be selected and reduction-expanded function can be used.
- PC tools for creating compressed JPEG image ROM data and evaluating image quality are provided.
- S5U1C330J1S does not use any interrupt or peripheral functions.
- Suitable for applications that capture and display image data such as digital cameras, PDA, digital stationery and digital toys.

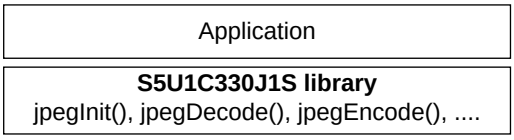
■ MEMORY REQUIREMENTS AND SPEED

- RAM ..... 36K bytes (for an image 320 pixels wide)
- ROM ..... 25K bytes
- Compression and decompression speed .... approx. 2 seconds
  (20MHz operation, 320 × 240 pixels)

■ SOFTWARE CONFIGURATION

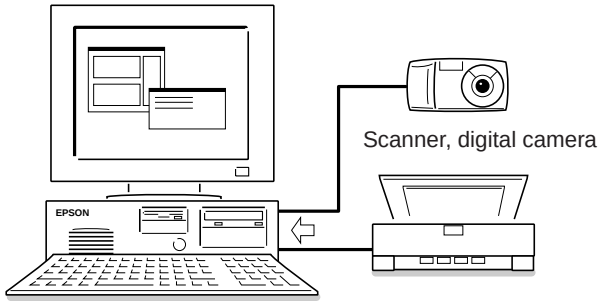
● S5U1C330J1S Library

Library including subroutines that are called from the user's application.
Compression and decompression are possible in an S1C33 chip.

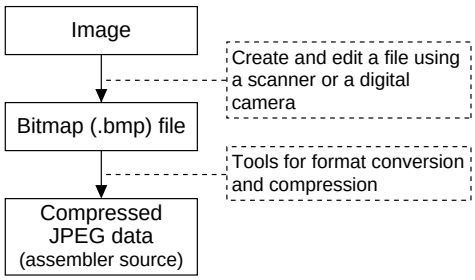


● S5U1C330J1S Data Creation Tool

This tool creates compressed JPEG image ROM data for display only.
It can be used with Windows95/98/NT4.0, or higher versions.

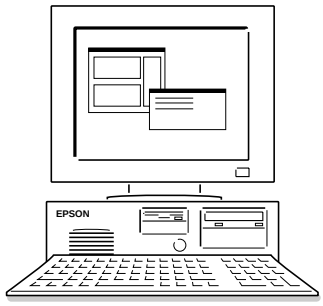


Flow in PC (Example)



● **S5U1C330J1S Evaluation Tool**

This tool is for evaluating JPEG compression and decompression quality on a PC.
With a PC, using GUI tools, the quality of image files when the compression ratio is changed can be evaluated.
It can be used with Windows95/98/NT4.0, or higher versions.



JPEG evaluation tool

∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330C1S Middleware

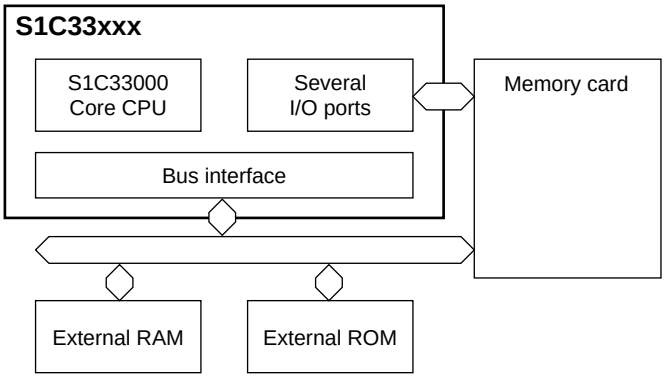
Compact FLASH middleware

- Compact FLASH middleware for the S1C33 Family
- Supports FAT file system (compatible with MS-DOS Ver.6.x)

■ FEATURES

- This is a middleware for the S1C33 Family, available in linkable library form.
- Uses True IDE mode to interface with memory cards.
- ATA FLASH card device driver allow use of compact FLASH or ATA FLASH cards.
- FAT file system driver enables MS-DOS Ver.6.x compatible file exchange. FAT format drivers for compact FLASH and ATA FLASH are also available.
- Ideally suited for use in digital cameras, PDAs, and electronic pocketbooks.

■ HARDWARE CONFIGURATION



■ REQUIRED RESOURCES

ROM space: approx. 30K bytes
RAM space: approx. 4K bytes

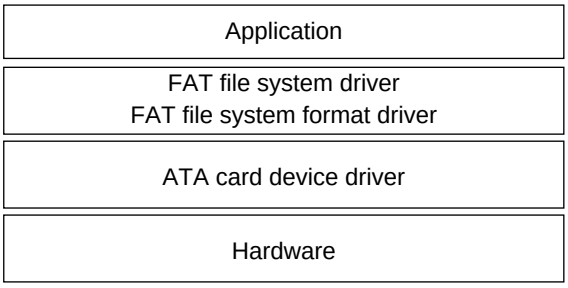
The following ports are used for controlling memory card.

K62 – INTRQ
P4 – CD1
P5 – CD2

■ RECOMMENDED CARDS

MELCO	8MB compact FLASH	RCF-C 8MB
MELCO	48MB compact FLASH	RCF-C 48MB
HAGIWARE	8MB compact FLASH	HPC-CF08X
I/O DATA	10MB compact FLASH	PCCF-10MS
EPSON	45MB compact FLASH	SECF-A45

■ SOFTWARE CONFIGURATION



● **ATA Card Device Driver**
Use of the compact FLASH and ATA FLASH cards require an ATA card device driver.

● **FAT File System Device Driver (supports FAT12 and FAT16)**
Permits MS-DOS Ver.6.x compatible file exchange (8 character file names, with three extension characters).
Support for Japanese file names.
API is standard ANSI-like (e.g., fopen() and fred()).

● **FAT File System Format Driver**
This driver initializes the FAT file system to make it usable in compact FLASH or ATA FLASH.

● **FAT File System Processing Speed (reference data)**
Measurement conditions:
CPU clock: 40MHz, Bus clock: 20MHz,
ATA register, ROM: wait 1, RAM: wait 0
A 1-MB file is read or 512-byte data is written 2,048 times.

MELCO 8MB compact FLASH RCF-C
Format..... 0.11s
1MB file read 12.02s
1MB file write 15.63s

EPSON 45MB compact FLASH SECF-A45
Format..... 0.59s
1MB file read 20.18s
1MB file write 28.38s

∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330G1S Middleware

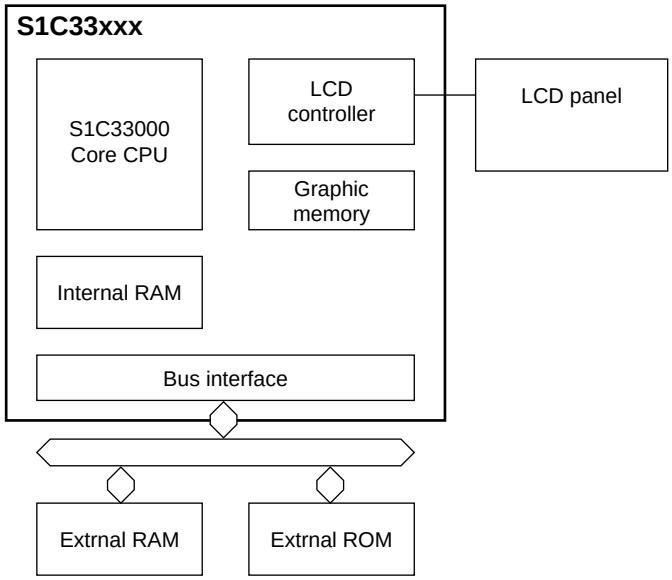
Graphic library

- Graphics library for the S1C33 Family
- Supports various grayscales, from 1, 2, 4, or 8bpp colors to monochrome
- Comes with the user interface resources necessary for GUI implementation

■ FEATURES

- This is a graphics library for the S1C33 Family provided in linkable library form. User interface resources required for GUI implementation are also available.
- Supports various grayscales from 1, 2, 4, or 8bpp colors to monochrome.
- Optimized for use with the S1C33 Family; library is fast and compact.
- Allows for advance evaluation using an emulation library running on a PC.
- Ideally suited for applications making use of LCD panels, including PDAs, electronic toys, and electronic stationery.

■ HARDWARE CONFIGURATION

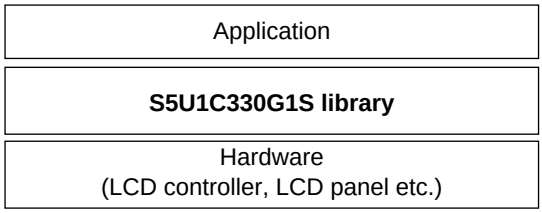


■ MEMORY REQUIREMENTS

Object	Code (ROM)	BSS (RAM)	Stack
GPC related function (gpc33.lib)	15K bytes	500 bytes	170 bytes
GUI related function (gpcgui.o, gpcevent.o)	4.2K bytes	23K bytes *1	250 bytes
1-byte font (gpcfont1.o in gpc33.lib)	3K bytes	–	–
2-byte font (gpcfont2.o in gpc33.lib)	164K bytes	–	–
Display driver (gpcdrv.o in gpc33.lib)	1K bytes	16 bytes	–

*1: If pop-up window is not used, BSS (RAM) of the GUI system takes about 3K bytes.

■ SOFTWARE CONFIGURATION



■ PRIMARY USER INTERFACE RESOURCES

Resorce	Description
Form window	Standard window
Pop-up window	Used to display alert information
Text window	Displays text.
Command button	Command execution button
Check box	Square box - checked when selected
Radio button	Round button that can be selected from a group of buttons

■ PRIMARY GRAPHIC FUNCTIONS

Function	Description
gpcDrawPoint	Draws a point.
gpcDrawLine	Draws a line.
gpcDrawRect	Draws a rectangle.
gpcFillRect	Fills a rectangle.
gpcInvrertRect	Reverses a displayed area.
gpcDrawEllipse	Draws an ellipse.
gpcFillEllipse	Fills an ellipse.
gpcDrawCircle	Draws a circle.
gpcFillCircle	Fills a circle.
gpcDrawArc	Draws an arc.
gpcDrawText	Outputs text.
gpcPutImage	Outputs an image.
gpcGetImage	Captures an image.

* This middleware is only available with the IC (S1C33 Family).
  This specification may change without notice.

EPSON

S1C33 Family S5U1C330P1S Middleware

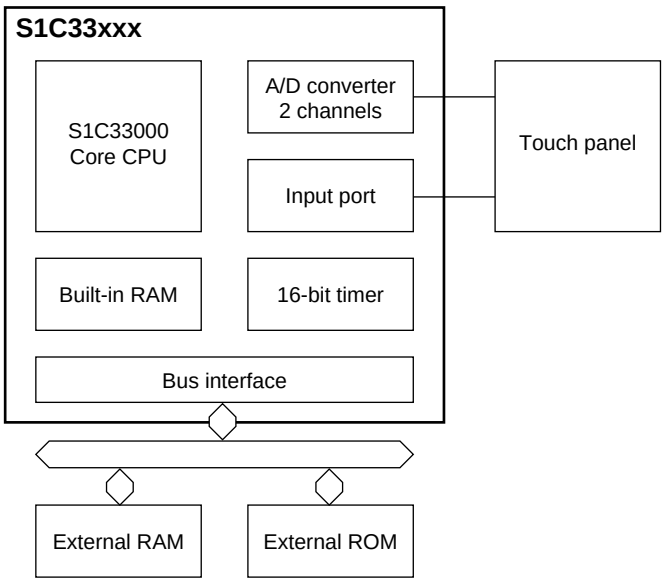
Pen writing recognition middleware

- Handwritten character recognition middleware for the S1C33 Family
- Handwritten character recognition level 1 supports a "printed style of writing"
- Handwritten character recognition level 2 supports a "simplified form of writing"

■ FEATURES

- Handwritten character recognition middleware for the S1C33 Family is provided in the form of a linkable library.
- Useful for handwritten character recognition in both Japanese and English.
- Handwritten character recognition level 1 supports the "printed style of writing", allowing for fast and memory-efficient character recognition.
- Handwritten character recognition level 2 supports the "simplified form of writing", providing a higher recognition rate than in level 1.
- Suitable for PDAs, personal organizers and digital stationeries.

■ HARDWARE CONFIGURATION



■ REQUIRED RESOURCES

- For the DMT33003 board made by EHK, this middleware uses one interrupt input port, two channels of A/D converters, and one channel of 16-bit timer.

  ＊ The two channels of A/D converters are used to acquire the x and y coordinates of the character written on the touch-panel. The 16-bit timer is used to set an interval time at which to acquire the coordinates.

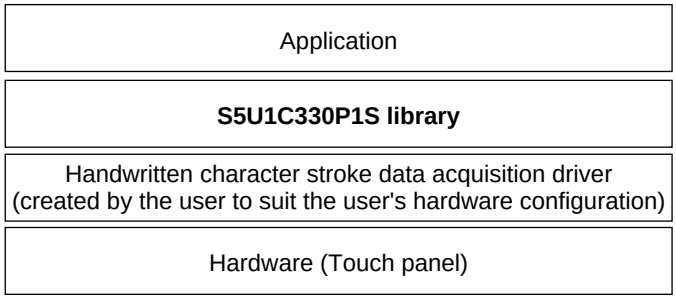
- Memory requirements

  RAM ..... approx. 140KB

  ROM Library (program) ..... approx. 70KB
  Dictionary data for Level 1 recognition (English and Japanese) ..... approx. 200KB
  Dictionary data for Level 2 recognition (English) ..... approx. 240KB
  Dictionary data for Level 2 recognition (Japanese) ..... approx. 1500KB

■ SOFTWARE CONFIGURATION

- The driver necessary to acquire the character stroke data must be created by the user in conformity with the user's hardware configuration.



  ∗ The sample sources of the handwritten character stroke data acquisition driver for the DMT33003 board made by EHK are in the public domain.

- Japanese Handwritten character recognition results are produced in shift JIS code and displayed as they are.
- For English handwritten character recognition, the recognition results in shift JIS code are converted into ASCII code using ASCII code conversion functions.
- Character strings written laterally can be recognized using character extracting functions.

∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330H1S Middleware

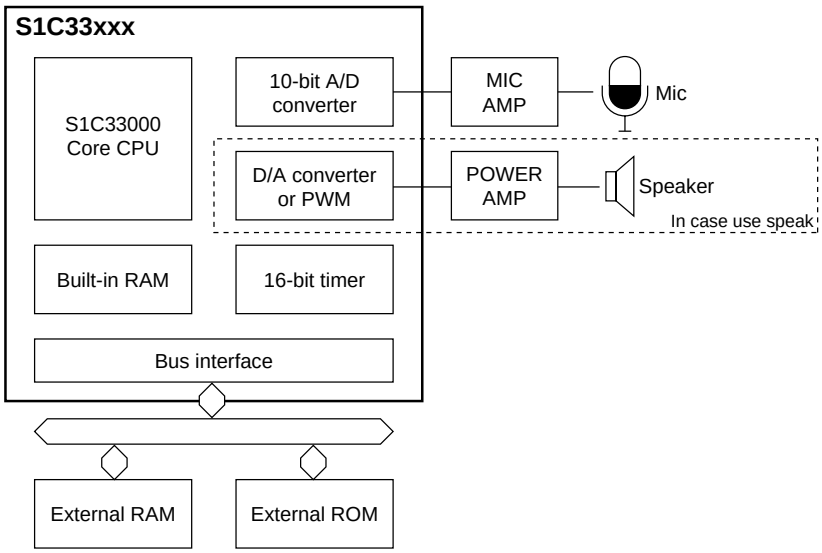
Voice recognition by phoneme model

- Japanese speech recognition middleware for the S1C33 Family
- Real-time execution in an S1C33 chip
- Phoneme model supported

■ FEATURES

- Speech recognition middleware for the S1C33 Family is provided in the form of a linkable library.
- The speech recognition engine and a listening routines using an A/D converter are included in the library. Speaking routines with a D/A converter or PWM can be implemented.
- Using the Seiko Epson exclusive phoneme model recognition technology, about 100 words can be recognized in real-time.
- Capable of selecting between two kinds of probability data for phonemes 33 and 85, according to the recognition rate and memory used.
- Supports Japanese for recognition.
- Voice recognition data can be created simply by just writing words to be recognized in text format.
- PC tools for evaluating the speech recognition engine are provided.
- Evaluation boards are provided.
- Suitable for PDAs, digital stationeries and digital toys.

■ HARDWARE CONFIGURATION

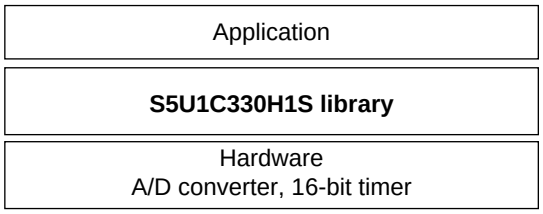


■ MEMORY REQUIREMENTS AND SPEED

- RAM ..... approx. 5K bytes
- ROM
  Library (Program) ..... approx. 55K bytes
  Recognition dictionary ..... Four bytes per vowel, 8 bytes per consonant
  Probability data for phoneme 33 ..... approx. 200K bytes
  Probability data for phoneme 85 ..... approx. 523K bytes
- Recognition speed
  40MHz operation, recognition dictionary: 50 words ..... 1 to 1.4 seconds
  (The dictionary is configured with 5 to 10 phonemes per single entry such as "Good morning" or "Good afternoon.")

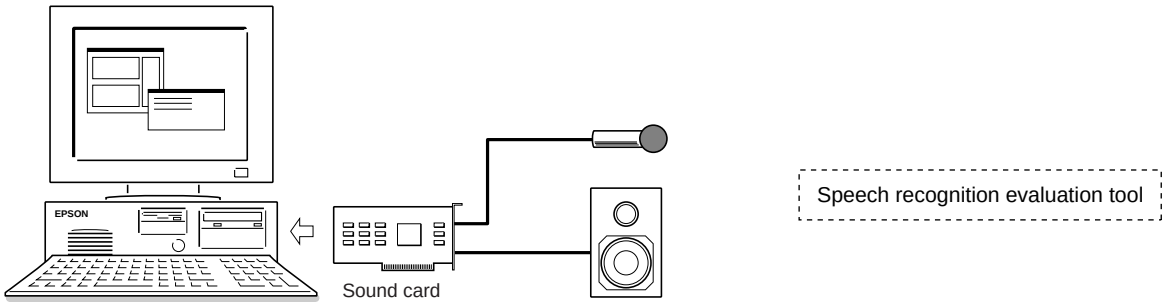
■ SOFTWARE CONFIGURATION

● S5U1C330H1S Library



● S5U1C330H1S Evaluation Tool

This is an evaluation tool for the S5U1C330H1S recognition engine using the sound board on a PC.



∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330S2S Middleware

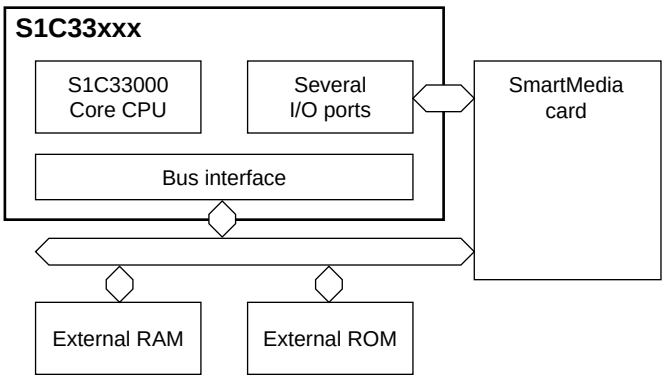
SmartMedia middleware

- SmartMedia middleware for the S1C33 Family
- Supports FAT file system (compatible with MS-DOS Ver.6.x)

■ FEATURES

- This is a middleware for the S1C33 Family, available in linkable library form.
- Conforms to the SmartMedia specifications of the SSFDC Forum.
- FAT file system driver enables MS-DOS Ver.6.x compatible file exchange. FAT format driver for SmartMedia is also available.
- Ideally suited for use in digital cameras, PDAs, and electronic pocketbooks.

■ HARDWARE CONFIGURATION



■ REQUIRED RESOURCES

ROM space: approx. 30K bytes
RAM space: approx. 18K bytes

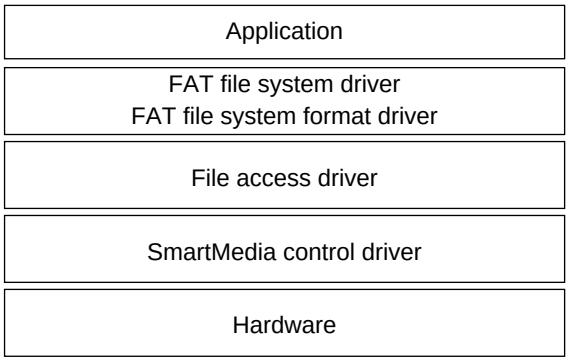
The following ports are used for controlling SmartMedia
P30 – Card Enable
P31 – Address Latch Enable
P32 – Command Latch Enable
P33 – Write Protect
P34 – Ready/Busy
P35 – Write Protect Seal
K62 – Card Detect

■ SUPPORTED MEMORY CARDS

SmartMedia card (4MB to 64MB)

■ SOFTWARE CONFIGURATION

● **SmartMedia Library**



∗ To allow modification of the SmartMedia control and file access drivers (some part) to suit the customer hardware environment, the source is left partly open to users.

● **File Access Driver, SmartMedia Control Driver**
Runs according to SmartMedia (4MB to 64MB).

● **FAT File System Device Driver (supports FAT12 and FAT16)**
Permits MS-DOS Ver.6.x compatible file exchange (8 character file names, with three extension characters).
Support for Japanese file names.
API is standard ANSI-like (e.g., fopen() and fred()).

● **FAT File System Format Driver**
This driver initializes the FAT file system to make it usable in SmartMedia.

∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330U1S Middleware

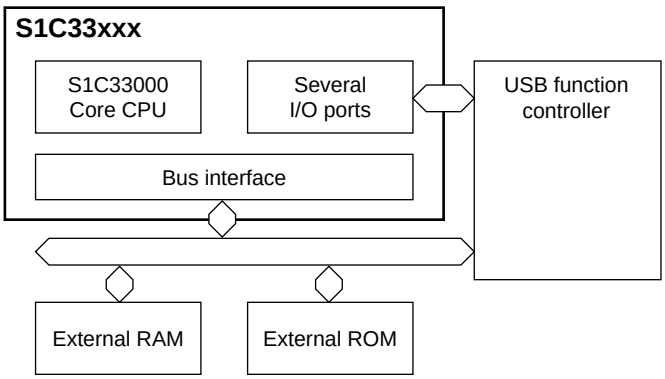
USB sample program

- USB sample program for the S1C33 Family
- Supports bulk transfer and interrupt transfer

■ FEATURES

- Sample programs for the S1C33 Family, with all source code.
- Includes a USB mouse program using Interrupt transfer.
- Includes a program-loader program using Bulk transfer.
  Also included are a device driver (Windows 98/2000 version) and application program for Bulk transfer.
- May be used to develop USB equipment using the S1C Family.

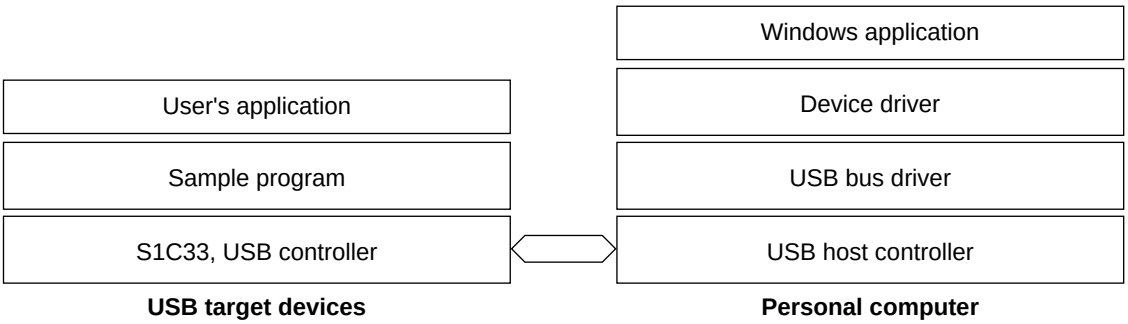
■ HARDWARE CONFIGURATION



■ REQUIRED RESOURCES

ROM space: approx. 6K bytes
RAM space: approx. 0.5K bytes
I/O port: K50 – Mouse move up
K51 – Mouse move left, DMAREQ1
K52 – Mouse move down
K53 – Mouse move right
K54 – Mouse left button
K67 – Mouse right button
P7 – XINT
P33 – DMAACK1
High-speed DMA: Ch1

■ SOFTWARE CONFIGURATION



- This program includes all source code.
- The supported USB function controllers are the FLAC075 and SPC7200.
- The USB function controllers comply with the USB1.1 specifications.
- The S1C33's high-speed DMA performs data transfers via the USB function controller's port interface for high-speed data transfers.
- Includes a Windows application and WDM driver for a head start on software development for USB target equipment.

∗ This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

EPSON

S1C33 Family S5U1C330G3S Middleware

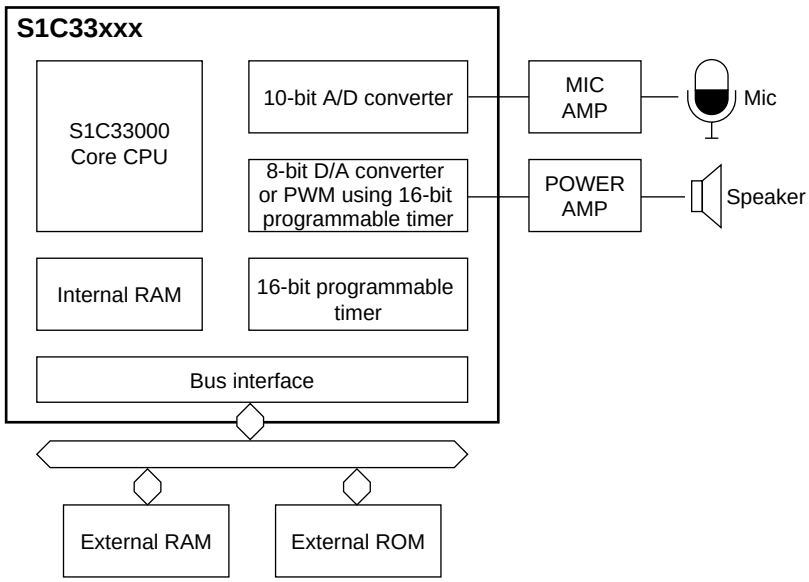
G729, G723.1 real time codec middleware

- G72x real time codec middleware for the S1C33 Family
- Real-time execution in an S1C33 chip
- Voice compression technologies G729, G723.1 supported

■ FEATURES

- G72x real time codec middleware for the S1C33 Family is provided in the form of a linkable library.
- Uses voice compression technologies G729 Annex-A and G723.1 Annex-A (decompression only) to compress and decompress voice data. The following compression rates are supported (based on 8-kHz sampling):
  G729 ..... 8kbps
  G723.1 ..... 6.3kbps/5.3kbps
- Suitable for voice memos, data banks with voice, PDA with voice, digital stationery with voice and digital toys with voice.

■ HARDWARE CONFIGURATION



■ MEMORY REQUIREMENTS AND SPEED

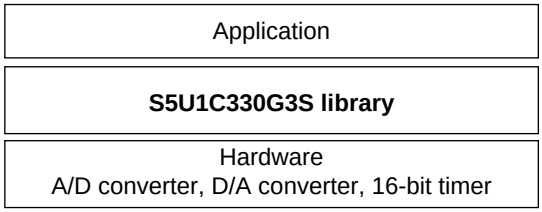
● **Memory Requirements (byte)**

	Internal RAM	External RAM	ROM
G729 compression/decompression:	7.5K	4.7K	38.4K
G729 decompression only:	7.5K	3.0K	20.0K
G723.1 decompression only:	7.3K	2.5K	33.0K

● **Speed (CPU occupancy)**

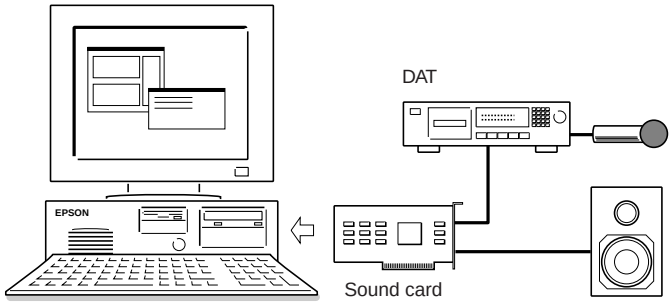
G729 compression (50MHz): 97% (measurement results when ROM and RAM are accessed with no wait states)
G729 decompression (40MHz): 75%
G723.1 decompression (40MHz): 40%

■ SOFTWARE CONFIGURATION

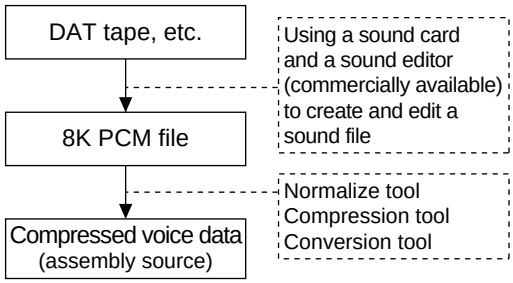


● S5U1C330G3S Data Creation Tool

This tool creates compressed voice ROM data for replay only.
It can be used with Windows95/NT4.0, or higher versions.



Flow in PC (Example)



∗ G729 and G723.1 require license fees.
This middleware is only available with the IC (S1C33 Family).
This specification may change without notice.

S1C33 Family Demonstration and Evaluation Board

■ FEATURES

- S5U1C33xxxDx is the evaluation board for the S1C33xxx. It contains 1MB Flash memory × 2, 1MB RAM, 20MHz and 32kHz oscillators.
- The onboard 1MB Flash memory includes the S5U1C330M2S debug monitor. It provides debugging functions, such as downloading a program to the RAM or Flash memory, running, stepping, setting breaks, with the S5U1C330MxD1 board and the db33 debugger on the PC. The demonstration boards support stand alone running by the program written in the Flash memory.
- The S5U1C330A3D1, S5U1C330LxD1, S5U1C330C1D1 and other expansion boards provide an environment for demonstration and evaluating the voice, graphic, comppact FLASH and other middlewares.
- S5U1C33xxxD2 (S1C33xxx QFP socket type) with S5U1C33xxxEx provide an internal ROM emulation function allowing evaluation and development of programs for ROM built-in models.

■ S1C33 FAMILY DEMO BOARD LIST

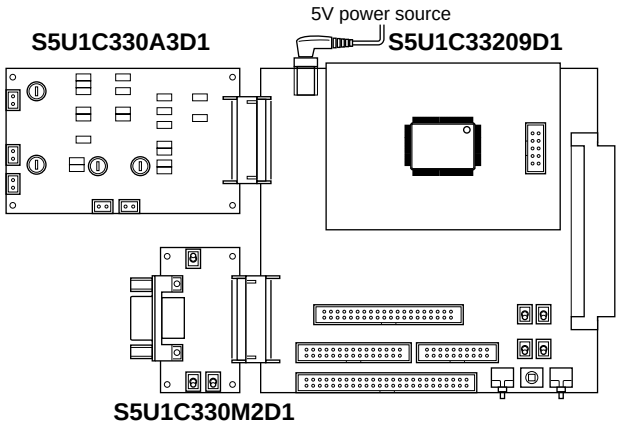
Board name	IC supported	Input voltage Operating voltage	Operating frequency	S5U1C330M2S area	Flash	SRAM	I/F	Bus I/O output	Others
S5U1C33209D1	S1C33209	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–
S5U1C33L01D1 S5U1C33L01D2	S1C33L01	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1 S5U1C330LxD	Bus and I/O pin output	D2 is for S5U1C33L01E1 With 12V, 5 to 28V, -5 to -28V outputs for LCD
S5U1C33T01D1	S1C33T01	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–
S5U1C33S01D1	S1C33S01	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–
S5U1C33240D1	S1C33240	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–
S5U1C33210D1	S1C33210	5V input 3.3V operation	40MHz 32kHz	Flash 1MB	1MB	1MB	S5U1C330M2D1 S5U1C330AxD1	Bus and I/O pin output	–

● Expansion Board

Board name	Power	Function
S5U1C330A3D1	5V	8–32kHz sampling audio input/output board Supports PCM15, stereo output, and S5U1C330M1S piezoelectric buzzer output.
S5U1C330A4D1	5V	Audio input/output board Contains low-cost transistor amplifier supporting PCM15.
S5U1C330L2D1	5V	LCD demonstration board with 2.6-inch DTFD panel (exclusive use for S5U1C33L01D1) Note)
S5U1C330L3D1	5V	LCD demonstration board with 3.7-inch DTFD panel (exclusive use for S5U1C33L01D1) Note)
S5U1C330C1D1	3.3V	Demonstration board for compact flash Connected with a bus connector.
S5U1C330L1D1	3.3 to 5V	I/F board for Agilent Technologies (former HP) 16500A Connected with a bus connector.
S5U1C330S1D1	3.3V	Memory card board for smart medium and S5U1C330S2S Connected with a bus connector.
S5U1C330U1D1	3.3V	Evaluation board for USB macro that can be implemented to ASIC
S5U1C330C2D1	3.3V	ASIC emulation board for Altera APEX20K 400 (400,000 gates) is installed in the socket (default). Interchaneable with 1000 (1,000,000 gates).

Note: A rental board only is available because the quantity is limited.

■ BOARD SYSTEM EXAMPLE (1) S5U1C33209D1 + S5U1C330A3D1



● Description

- Connecting the S5U1C330M2D1 and a PC allows on-board debugging of the user application, using a debugger (db33.exe) running on the PC.
- The S5U1C330A3D1 allows 8kHz to 32kHz-sampled voice/sound to be input or output to or from the board. S5U1C330A3D1 supports PCM15, stereo output, and S5U1C330M1S piezoelectric buzzer output.

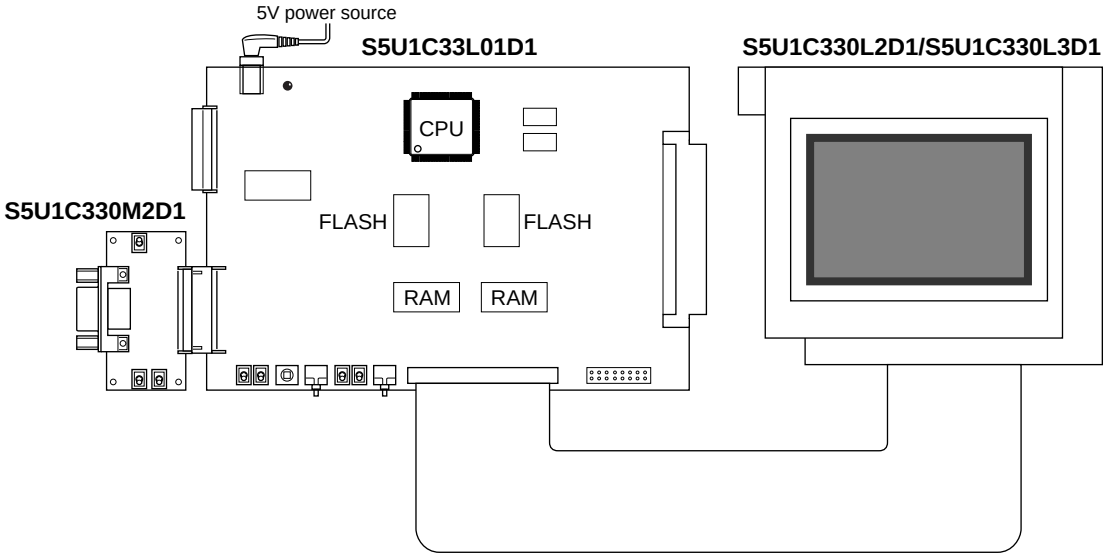
● Operational Demo Software

dm5s8jVx.exe (Voice demo 8kHz Japanese)
(S5U1C330V1S (Japanese), S5U1C330S1S, S5U1C330M1S, S5U1C330V2S, S5U1C330T1S)
dm5s8eVx.exe (Voice demo 8kHz English)
(S5U1C330V1S (English), S5U1C330S1S, S5U1C330M1S, S5U1C330V2S)
dm5s16Vx.exe (Voice demo 16kHz, 22kHz Japanese only)
(S5U1C330T1S (VSX2-16kHz, 22kHz), S5U1C330S1S-16kHz)
dm7s22Vx.exe (Sound demo 22kHz)
(S5U1C330S1S, 15 bits, 22kHz stereo, S5U1C330M1S 2ch differential outputs)
dm7s32Vx.exe (Sound demo 32kHz)
(PCM15, 32kHz monaural (guitar sound))
dm7s3bVx.exe (Sound demo 32kHz)
(PCM15, 32kHz monaural (beatmania))
dm7s3cVx.exe (Sound demo 32kHz)
(S5U1C330S1S, 15 bits, 32kHz stereo)

● Corresponding Middleware and Firmware Sample Software

S5U1C330V1S : Voice compression/expansion and voice processing
S5U1C330V2S : Voice recognition
S5U1C330T1S : Text to speech
S5U1C330M1S : PWM method simple sound output (1ch output, 2ch differential outputs)
S5U1C330S1S : Sound output based on WAVE sound source
S5U1C330M2S : Debug monitor running on user board
FLS33 : Flash memory programming routine

■ BOARD SYSTEM EXAMPLE (2) S5U1C33L01D1 + S5U1C330L2D1/S5U1C330L3D1



● **Description**

With the inclusion of the S5U1C330L2D1/S5U1C330L3D1, this example configuration allows demonstrations of LCD display capability using a 2.6-inch or 3.7-inch DTFD panel.

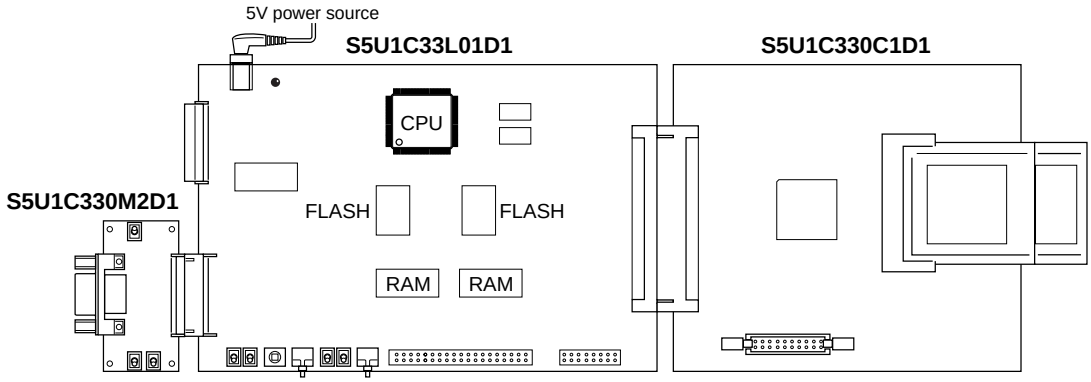
● **Operational Demo Software**

dm6g26Vx.exe (Display demonstration)–S5U1C33L01D1 + S5U1C330L2D1
dm6g37Vx.exe (Display demonstration)–S5U1C33L01D1 + S5U1C330L3D1
dm6guiVx.exe (S5U1C330G1S demonstration)–S5U1C33L01D1 + S5U1C330L2D1/S5U1C330L3D1

● **Corresponding Middleware and Firmware Sample Software**

S5U1C330J1S : JPEG compression/expansion
S5U1C330G1S : Graphics and GUI library
S5U1C330R1S : µITRON3.0 compliant real-time OS
S5U1C330M2S : Debug monitor running on user board (same as S5U1C33209Dx)
FLS33 : Flash memory programming routine (same as S5U1C33209Dx)

■ BOARD SYSTEM EXAMPLE (3) S5U1C33L01D1 + S5U1C330C1D1



● **Description**

With the inclusion of the S5U1C330C1D1, this example configuration allows demonstrations of compact flash. Use a bus connector to connect the S5U1C330C1D1.

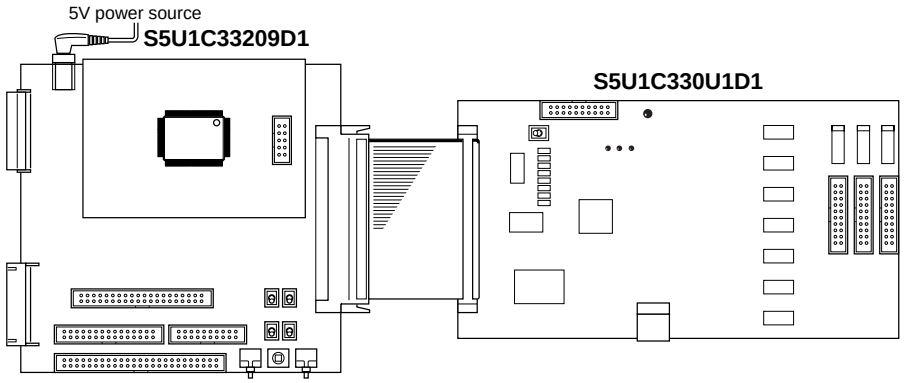
● **Operational Demo Software**

dm6cfVx.exe (S5U1C330C1S compact FLASH demonstration)–S5U1C33L01D1 + S5U1C330C1D1

● **Corresponding Middleware and Firmware Sample Software**

S5U1C330G1S : Graphics and GUI library
S5U1C330R1S : µITRON3.0 compliant real-time OS
S5U1C330M2S : Debug monitor running on user board (same as S5U1C33209Dx)
FLS33 : Flash memory programming routine (same as S5U1C33209Dx)
S5U1C33C1S : Compact FLASH library
(Supports up to the S5U1C33C1S12; not compatible with S5U1C33C1S21 and later)

■ BOARD SYSTEM EXAMPLE (4) S5U1C33209D1 + S5U1C330U1D1



● **Description**

With the inclusion of the S5U1C330U1D1, this example configuration allows demonstrations of USB sample program. Use a bus connector to connect the S5U1C330U1D1.

● **Operational Demo Software**

usbEVv10.exe

● **Corresponding Middleware and Firmware Sample Software**

S5U1C330U1S : USB sample program

S1C33 Family Tool Selection Guide

■ OVERVIEW

The S1C33 Family provides a varied lineup of development tools and evaluation boards to meet a broad range of situations and needs. The following is your guide to picking the ones best suited to your current project.
Note that the following applies only to S1C332xx devices. The S1C33104 uses a different set of tools.

■ CHOOSING BASIC TOOLS

Tool selection depends on such factors as the target device which includes program code and the type of emulation memory for built-in ROM and onboard ROM or flash. The steps for making your selections appear in alphabetical order.

(A) Obligatory tools

A-1 Compiler and in-circuit emulator

The following two items are always necessary.

S5U1C33000C	**S5U1C33000H**
C compiler package	Common in-circuit emulator

(B) Emulation memory tools for onboard program development

The following tools are available for downloading the program under development to the board.

B-1 Using Flash memory

B-1-1 Using FLS33 software (supplied with the S5U1C33000C)

FLS33 (CC33\utility), provides facilities for erasing Flash memory, downloading a program, and debugging it.

No additional items necessary

Note: For a list of the models supported by FLS33, see "■COMPATIBILITY LISTS".

B-1-2 Using S5U1C330T1M1 hardware

If the target device is in the standard 48-pin TSOP package, affix an S5U1C330T1M1 component to the foot pattern and add S5U1C33002Mx or S5U1C33001Mx components as appropriate (see Figure) to produce emulation memory for downloading and debugging programs.
One set is required for each target board being debugged.

S5U1C330T1M1	+	**S5U1C33002M1**	8M bits of emulation memory
S5U1C330T1M1	+	Two **S5U1C33002M1**s	16M bits of emulation memory
S5U1C330T1M1	+	**S5U1C33001M1**	32M bits of emulation memory

Note 1: The above is for models using a 5V bus. Substitute S5U1C33002M2 or S5U1C33001M2 if the bus operates at 3.3V.
Note 2: For the layout of the 48 pins, refer to the S5U1C330T1M1 manual.

B-1-3 Using S5U1C33xxxEx hardware

Substitute the appropriate S5U1C33xxxEx component for the S1C33 chip and add S5U1C33002Mx or S5U1C33001Mx components as appropriate (see Figure) to produce emulation memory for downloading and debugging programs. One set is required for each target board being debugged.

S5U1C33xxxEx	+	**S5U1C33002M1**	8M bits of emulation memory
S5U1C33xxxEx	+	Two **S5U1C33002M1**s	16M bits of emulation memory
S5U1C33xxxEx	+	**S5U1C33001M1**	32M bits of emulation memory
S5U1C33xxxEx	+	Two **S5U1C33001M1**s	64M bits of emulation memory

Note 1: The above is for models using a 5V bus. Substitute S5U1C33002M2 or S5U1C33001M2 if the bus operates at 3.3V.
Note 2: For further details on the S5U1C33xxxEx components, see "■COMPATIBILITY LISTS".

B-2 Using ROM

B-2-1 Using ROM in DIP or PLCC

If the target device is in a 40-pin DIP, 42-pin DIP, or 44-pin PLCC package, provide a ROM socket on the board and combine S5U1C330D1M1 with S5U1C33002Mx or S5U1C33001Mx as appropriate (See Figure) to produce emulation memory for downloading and debugging programs. One set is required for each target board being debugged.

DIP (40 or 42 pins)

S5U1C330D1M1	+	**S5U1C33002M1**	8M bits of emulation memory
S5U1C330D1M1	+	Two **S5U1C33002M1**s	16M bits of emulation memory
S5U1C330D1M1	+	**S5U1C33001M1**	32M bits of emulation memory

PLCC44

This package also requires a **Sunhayato27C4096** available separately.

Note: The above is for models using a 5V bus. Substitute S5U1C33002M2 or S5U1C33001M2 if the bus operates at 3.3V.

B-2-2 Using S5U1C33xxxEx hardware

This is the same as B-1-3, "Using S5U1C33xxxEx hardware".

B-3 Using nothing extra

If the program fits entirely in built-in ROM or runs in SRAM or DRAM on the board, there is no need for onboard emulation memory.

No additional items necessary

(C) Development tools for built-in ROM

C-1 Using FLS33 (supplied with the S5U1C33000C)

If the internal ROM is flash memory, use the FLS33 to erase and program the Flash memory, then debug the program.

Note: For a list of the models supported by FLS33, see "■COMPATIBILITY LISTS".

C-2 Using S5U1C33xxxEx

The built-in ROM is high-speed memory capable of operating with zero wait states at clock frequencies up to 50 MHz. When developing a program, use the S5U1C33xxxEx and S5U1C3300xS to produce emulation memory for debugging programs. One set is required for each target board being debugged.

S5U1C33xxxEx	+	**S5U1C33000S**	5V Bus
S5U1C33xxxEx	+	**S5U1C33001S**	3.3V Bus

Note 1: The S5U1C3300xS modules may be borrowed from Seiko Epson for a period of six months.
Note 2: For further details on the S5U1C33xxxEx components, see "■COMPATIBILITY LISTS".
Note 3: Tool (C) is used in conjunction with (A) and (B).

C-3 Built-in ROM not present or not used

No additional items necessary

■ OPTIONAL TOOLS

The following tools are available to complement the basic tools.

(G) ASIC development emulation support

There is a board using a CPLD for ASIC emulation.

G-1 Using Altera Flex10K100A

This Altera CPLD contains the equivalent of 100,000 gates. It is mounted on an S5U1C33001Mx component and connected to the target via an S5U1C33xxxEx component.
Note that the Altera PLD development tool MAX+PlusII and a download cable are also necessary.

S5U1C33xxxEx + **S5U1C33001M1** + **Altera MAX+PlusII**

G-2 Using Altera APEX20K400E

This Altera CPLD contains the equivalent of 400,000 gates. It is mounted on an S5U1C330C2D1 component and connected to the target via an S5U1C33xxxEx component.
Note that the Altera PLD development tool Quartus and a download cable are also necessary.

S5U1C33xxxEx + **S5U1C330C2D1** + **Altera Quartus**

Note 1: S5U1C33001M1 supports 5V bus. S5U1C33001M2 and S5U1C330C2D1 support 3.3V bus.
Note 2: For further details on the S5U1C33xxxEx components, see "■COMPATIBILITY LISTS".

(H) Enhancing break functions

The following tool, connected to the S1C33 external bus, provides addition break functions.

H-1 S5U1C33001Mx break functions

Combining S5U1C33000C Version 3 with the break functions inside the S5U1C33001Mx CPLD enhances the map break, bus break, and area break functions. The S5U1C33001Mx component is connected to the target via an S5U1C33xxxEx component.

S5U1C33xxxEx + **S5U1C33001M1**

Note 1: The above is for models using a 5V bus. Substitute S5U1C33001M2 if the bus operates at 3.3V.
Note 2: For further details on the S5U1C33xxxEx components, see "■COMPATIBILITY LISTS".

(I) S5U1C33xxxEx extension cables

These extension cables are for use with an S5U1C33xxxEx component.

I-1 176-pin cable

S5U1C33xxxEx — **S5U1C33T00E3** — S5U1C33T00T2 + Target board

I-2 100-pin cable

S5U1C33xxxEx — **S5U1C33S00E3** — S5U1C33S00T2 + Target board

Note: These cables are compatible with both 5V and 3.3V operation.

S1C33 Family Tool Selection Guide

■ ADVANTAGES AND DISADVANTAGES TO CERTAIN TOOLS

The approaches available each have their advantages and disadvantages.

(1) Onboard writes

B-1-1, using onboard resources only for everything, downloading the program to the onboard Flash memory, and using only the target board and S5U1C33000H, is perhaps the most trouble-free approach. The downside, however, is that it does not support software PC breaks. Only the two on-chip hardware PC breaks are available.

(2) Flash memory and ROM simulation

Next down on the trouble-free scale are the approaches accessing Flash memory or ROM with an S5U1C330T1M1 or S5U1C330D1M1 component. The only characteristics that change are the memory-related circuitry. Note that, if the memory capacity is available, an S5U1C33002Mx component is much easier to use than an S5U1C33001Mx because the latter features a much more complicated design.

(3) Using S5U1C33xxxEx hardware

Using an S5U1C33xxxEx component limits bus master functionality and greatly changes AC characteristics. Complicated settings also make this approach one to avoid whenever possible. Unfortunately, however, an S5U1C33xxxEx component is mandatory for developing built-in ROM. Access is also on the order of 8 ns slower with an S5U1C33xxxEx component. Using an extension cable (I) adds a further delay of 6 ns. Finally, note that the more tools added, the greater the susceptibility to noise.

■ CHOOSING AN EVALUATION BOARD

Before you build the actual target board and develop programs with these tools, an evaluation board or similar comes in handy for such purposes as evaluating the S1C33 microcomputer, learning how to use the tools, and developing a preliminary version by adding on a user board. The following are the things necessary for such evaluation environments.

(L) C compiler

Although it is better to use the product's C compiler, the evaluation version may be substituted. This package contains all the major components—compiler, assembler, and debugger, for example.

S5U1C33000C	or	**S5U1C33000C evaluation version**
Production version		ccEVvXX.exe from S1C33 data CD-ROM

(M) In-circuit emulator

Although S5U1C33000H is a better tool for the job, the S5U1C33xxxDx board includes a debugging monitor (S5U1C330M2S) that can used as a simple in-circuit emulator with S5U1C330MxD1. S5U1C330MxD1 can also download the demo software.

S5U1C33xxxDx and **S5U1C330M1D1**

Note: The above is for models using a 5V bus. Substitute S5U1C330M2D1 if the bus operates at 3.3V.

(N) Main S5U1C33xxxDx board

These boards contain an S1C33 microcomputer, Flash memory, and SRAM. Choose the one appropriate for your application.

N-1 Familiarizing yourself with the S1C33 Family

We recommend the S5U1C33209Dx here. It is a simple little board with an S1C33209.

S5U1C33209Dx

N-2 Evaluating built-in ROM speed

Three components are necessary: S5U1C33xxxD2, S5U1C33xxxEx, and S5U1C3300xS.

S1C33221 configuration	**S5U1C33209D2**	+	**S5U1C33209E1**	+	**S5U1C33000S**
S1C33L01 configuration	**S5U1C33L01D2**	+	**S5U1C33L01E1**	+	**S5U1C33001S**

Note 1: The S5U1C3300xS modules may be borrowed from Seiko Epson for a period of six months.
Note 2: Complicated settings make it advisable to avoid, whenever possible, using an S5U1C33xxxEx component.

N-3 Evaluating S1C33L01

For evaluating color panel

S5U1C33L01D1 (Contains S1C33L01) + **S5U1C330L2D1** 2.6-inch D-TFD panel
or
S5U1C330L3D1 3.7-inch D-TFD panel

Note 1: S5U1C330L2D1 and S5U1C330L3D1 are available on loan from Seiko Epson.

N-4 Testing S1C33T01 I/O functions

S5U1C33T01D1

Contains a S1C33T01 and provides full-pitch pin outputs for the I/O pins

N-5 Evaluating audio middleware

S5U1C33209D1 + **S5U1C330A3D1**

For use with S5U1C330V1S, S5U1C330V2S, S5U1C330T1S, S5U1C330M1S, and S5U1C330S1S

■ SAMPLE COMBINATIONS

Example 1:

S1C33209 device with no built-in ROM. Program development using onboard Flash memory.
An evaluation board for learning how to use the tools is also necessary.

Tool choices: A-1, B-1-1, C-1

S5U1C33000C , **S5U1C33000H**

Evaluation board choices: N-1, M

S5U1C33209Dx , **S5U1C330MxD1**

Example 2:

S1C33209 device without built-in ROM. Program development using DIP ROM (8M bits, 5 V).
An evaluation board for learning how to use the tools is also necessary.

Tool choices: A-1, B-2-1, C-1

S5U1C33000C , **S5U1C33000H** , **S5U1C330D1M1** , **S5U1C33002M1**

Example 3:

S1C33L01 device with built-in ROM. Program development using onboard Flash memory.
An evaluation board for learning how to use the tools is also necessary.

Tool choices: A-1, B-1-1, C-2

S5U1C33000C , **S5U1C33000H** , **S5U1C33L01E1**

Evaluation board choices: N-3, M

S5U1C33L01D1 , **S5U1C330M2D1**

■ COMPATIBILITY LISTS

(1) S5U1C33xxxEx support (as of December 1, 2000)

Microcomputer	S5U1C33xxxEx to use
S1C33209	S5U1C33209E1 (5V), S5U1C33209E2 (3.3V)
S1C33L01	S5U1C33L01E1 (3.3V)
S1C33T01	S5U1C33T01E1 (5V), S5U1C33T01E2 (3.3V)
S1C33S01	S5U1C33S01E1 (3.3V)
S1C33240	S5U1C33240E1 (5V), S5U1C33240E2 (3.3V)
S1C33221	S5U1C33221E1 (5V), S5U1C33221E2 (3.3V)

(2) FLS33 support (as of July 1, 2001) (Version 2.3)

Manufacturer	Model number	Voltage, Memory size	
FUJITSU, AMD	29F200, 29F400, 29F800	5V	2, 4, 8M bits
	29LV200, 29LV400, 29LV800, 29LV160	3.3V	2, 4, 8, 16M bits
	29DX32X	3.3V	32M bits
	MB84VD22194EE	3.3V	32M bits
	MBM29DL163TD	3.3V	16M bits
SHARP	LH28F800SUT	5V	8M bits
MITSUBISHI	M5M29GB160BVP, M5M29GT320VP	3.3V	16, 32M bits
ST	M29F102BB	5V	1M bits
	M29W800AT	3.3V	8M bits
SST	SST39LF200, SST39VF200, SST39LF160, SST39VF160	3.3V	2, 16M bits
SANYO	LE28F1101T	5V	2M bits
INTEL	DA28F320J5	5V	32M bits
EPSON	SPC7281, S1C33240	3.3V	512K bits, 1M bits

For further details, run the self-expanding archive CC33\utility\fls33\fls33vXX.exe and open the readme file.

S1C33 Family Data Sheets

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