EPC® - 2

Hardware Reference

RadiSys® Corporation

15025 S.W. Koll Parkway

Beaverton OR 97006

Phone: 800-950-0044

In Oregon: (503) 646-1850

07-0013-06 October 1992

Hardware Warranty

RadiSys Corporation ("RadiSys") warrants the EPC system and component modules to the original purchaser for two years from the product's shipping date. If an EPC product fails to operate in compliance with its specification during this period, RadiSys will, at its option, repair or replace the product at no charge. The customer is, however, responsible for shipping the product; RadiSys assumes no responsibility for the product until it is received. This warranty does not cover repair of products that have been damaged by abuse, accident, disaster, misuse, or incorrect installation.

RadiSys' limited warranty covers products only as delivered. User modification, such as the addition of memory arrays or other devices, may void the warranty, and if the product is damaged during installation of the modifications, this warranty does not cover repair or replacement.

This warranty in no way warrants suitability of the product for any specific application.

IN NO EVENT WILL RADISYS BE LIABLE FOR ANY DAMAGES, INCLUDING LOST PROFITS, LOST SAVINGS, OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE PRODUCT EVEN IF RADISYS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, OR FOR ANY CLAIM BY ANY PARTY OTHER THAN THE PURCHASER.

THE ABOVE WARRANTY IS IN LIEU OF ANY AND ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED OR STATUTORY, INCLUDING THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR USE, TITLE AND NONINFRINGEMENT. Repair or replacement as provided above shall be the Purchaser's sole and exclusive remedy and RadiSys' exclusive liability for any breach of warranty.

Contents

EPC-2 HARDWARE REFERENCE

December 1989

NOTES

1. Getting Started

This manual contains all the information you need to install and use the EPC-2 VXIbus embedded computer. Additional user's and programmer's manuals discuss the use of the EPConnect software package normally provided with EPC-2.

This manual describes not only the EPC-2 but also an additional version referred to here as the .i.EPC-2x; ("EPC-2 with EXM extension"). The two products differ in the following ways:

1. EPC-2x allows the use of one plug-in EXM module. For instance, the product .i.EPC-2e; is an EPC-2x containing an .i.EXM-10; Ethernet controller.
2. EPC-2 contains two built-in .i.serial port;s; EPC-2x contains one.
3. EPC-2 has a standard DB-25 parallel .i.printer port;; EPC-2x uses a special miniature connector and an adapter cable.
4. EPC-2 allows the use of an add-on .i.EPC-2AM; module.
5. EPC-2x has one additional BIOS .i.setup screen;.

This manual describes both the EPC-2 and EPC-2x. Unless otherwise noted, the term "EPC-2" hereafter in this manual will denote both. For products based on the EPC-2x, the EXM module is described in an accompanying manual. For instance, for the EPC-2e, the EXM-10 Hardware Reference accompanies this manual.

Please note that a revision of the EPC-2 (and EPC-2x) occurred in late November 1990. This manual applies to both the revision and the earlier model; where there are differences, the manual first explains the newer EPC-2 and then explains the differences in the older model. The simplest way to distinguish between the two versions is to inspect the back panel between the P1 and P2 VXIbus connectors. If there is a cutout in the panel exposing several jumper blocks, the EPC-2 is the revised model.

The differences between the revised and previous model are summarized below.

1. The .i.revised model; allows access to .i.jumpers; through the top, bottom, and back panels; the older model required removal of the side panels to access the jumpers.
2. The revised model supports optional use of .i.flat-panel display;s.
3. The revised model contains an .i.IDE; (integrated device electronics) hard disk instead of a SCSI disk. (A SCSI drive can still be obtained in the revised model on special order.)
4. The .i.battery; in the revised model is field replaceable.
5. The BIOS .i.setup screen; is different.
6. The revised EPC-2e contains an .i.EXM-10; Ethernet controller instead of .i.EXM-1;.

1¾ « [> “ Ÿ Ÿ £ ¤ ¤ MANUAL.STY
POSTSCRP¥ @ £0Ð┐Cx┘┌ Ÿ ¢ µ┌EPC-2 HARDWARE REFERENCE

Hidden: Indexed on 11/6/89. Also removed detail on VGA controller and EXP-MS. Don't forget to hide hidden text before hyphenating and printing

2. Installation

Before installing your EPC-2, you should unpack and inspect it for shipping damage.

* do not remove a cover from the module unless you are in a static-free environment. the epc-2, like most other electronic devices, is susceptible to esd damage. esd damage is not always immediately obvious, in that it can cause a partial breakdown in semiconductor devices that might not immediately result in a failure.
* make sure that the installation process described here is also performed in a static-free environment.
* the epc-2 contains a delicate hard disk. please handle it with care. avoid jarring the unit while it is in operation, and do not use excessive force when inserting and removing the epc-2 in a vxibus card cage.

Before installing the EPC-2 in a VXIbus chassis, you need to decide whether the EPC-2 is to be the .i.slot 0; .i.system controller;. Every VXIbus system needs a module that performs the system controller functions, including the standard VMEbus system controller functions (generation of the 16 MHz .i.SYSCLK; signal, arbitration of the bus, detection of .i.bus timeout; conditions, and initiation of the interrupt-acknowledge daisy chain), and the VXIbus slot-0 functions (generation of the 10 MHz ECL .i.CLK10; signals and control of the .i.MODID; module identification function).

To configure the EPC-2 as the slot-0 controller or not, there are two things you need to do:

ù Set jumpers within the unit.
ù Set the SLOT 0 FUNCTIONS field in the BIOS setup screen.

The EPC-2 is originally shipped to be the slot-0 controller. Since this is the typical use of the EPC-2, you can usually avoid dealing with the configuration steps described in this section.

Slot 0 / Non Slot 0 Configuration

The EPC-2 is shipped configured as a VXI .i.slot 0 controller;. If this is your intended use of the EPC-2 (which will usually be the case), you may skip this section.

To change the configuration of the EPC-2, there are four .i.jumpers; that need to be set. To locate the jumpers, you first need to determine the revision level of your EPC-2. If you see accessible jumpers through cutouts in the back, top, and bottom panels, you have the revised version. Otherwise, you have an older version.

To change the configuration of a revised-version EPC-2, follow the figure below. Three jumpers in the back panel and one jumper in the bottom panel need to be set. The three jumpers control the routing of the .i.CLK10;+ and CLK10- signals and the single jumper controls connection of the .i.MODID; line to pull-up and pull-down resistors.

.G.EPC2CJUM.EPS;3";3.52";Postscript

Note that there are only two valid combinations of setting the four jumpers. Also, the pictures depict the jumpers as seen when holding the unit horizontally such that the side nearest the floppy disk drive (right side) is up. The set of jumpers associated with .i.flat-panel display;s is discussed later.

To configure the EPC-2 as the slot-0 controller, you need to:

1. Set the jumpers as shown in the previous diagram.
2. Install the EPC-2 in slots 0 and 1 of your VXIbus chassis.

3. When you first power-on your system, invoke the BIOS .i.setup screen; and change the SLOT 0 FUNCTIONS to INTERNAL CLOCK or EXTERNAL CLOCK (the latter being the case if you have an external 10 MHz clock source connected to the EPC-2 front panel).

The setup screen is invoked by pressing the CTRL+ALT+ESC keys simultaneously. You can do this at the operating-system prompt or when the power-on selftest screen is cleared after rebooting.

To configure the EPC-2 as not the slot-0 controller, you need to:

1. Set the jumpers as shown in the previous diagram.
2. Install the EPC-2 in other than slot 0 of your VXIbus chassis.
3. When you first power-on your system, invoke the BIOS .i.setup screen; and change the SLOT 0 FUNCTIONS to NONE.

The setup screen is invoked by pressing the CTRL+ALT+ESC keys simultaneously. You can do this at the operating-system prompt or when the power-on selftest screen is cleared after rebooting.

Older Models

To change the configuration of the earlier version of the EPC-2, open the right cover and set the unit on a static-free surface with the front panel to the left. There are four .i.jumpers; that need to be set.

.G.EPC2JUMP.EPS;2.75";1.435";Postscript

To change the jumpers, you will need to use needle-nose pliers. Make sure that you and the pliers are grounded to avoid ESD damage.

After changing the jumpers, follow the procedure above. Note that some earlier EPC-2s allow invocation of the .i.setup screen; only immediately after the fixed-disk message appears near the bottom of the initial screen after booting.

Troubleshooting the Configuration Jumpers

There are several readily apparent consequences of incorrectly configuring the EPC-2. For an EPC-2 physically present in .i.slot 0; in the VXIbus system:

1. If the .i.resource manager; running on the slot 0 controller reports a system configuration differing widely from the actual configuration (e.g., reports no devices found or reports devices in empty slots), the .i.MODID jumper; (the single jumper) is probably set incorrectly.
2. If the EPC-2's power-on selftest reports a VXI failure, the .i.CLK10 jumpers; could be set incorrectly or the setup parameter SLOT 0 FUNCTIONS could be incorrect (i.e., set to NONE, or set to EXTERNAL when there is no external clock source connected).
3. If the CLK10+ and CLK10- signals are not being driven on the backplane, any of the problems mentioned in the previous point could be the cause.

For an EPC-2 physically present in other than slot 0 in the VXIbus system:

1. If the resource manager could not detect the presence of the EPC-2, the MODID jumper is set incorrectly.
2. If the EPC-2's power-on selftest reports a VXI failure, the .i.CLK10 jumpers; could be set incorrectly.
3. If multiple masters seem to be using the .i.data transfer bus; concurrently, or if the 16 MHz .i.SYSCLK; signal on the backplane is out of spec, the EPC-2's setup parameter SLOT 0 FUNCTIONS could be incorrect (i.e., set to other than NONE).
4. If the CLK10+ and CLK10- signals on the backplane are out of spec, the .i.CLK10 jumpers; in the EPC-2 may be set incorrectly.
4. .i.No SYSCLK error;If the EPC-2's power-on selftest reports "TESTING VME INTERFACE - NO SYSCLK," the slot 0 controller is not generating the 16 MHz .i.SYSCLK; signal.

EPC-2 Insertion

The EPC-2 is inserted in a VXIbus card cage in the following way:

1. Make sure that power to your VXI system is off. The modules are not designed to be inserted or removed from live backplanes.

2. Align the EPC-2 to two adjacent top and bottom card guides in the VXI chassis.
3. Slide the EPC-2 module into the chassis. Use firm pressure on the handles to mate the module with the backplane connectors.
4. Tighten the screws in the top and bottom of the front panel to ensure proper connector mating and prevent loosening of the module via vibration.

Note that the EPC-2 has a .i.front-panel key; adhering to the VXIbus specification that prevents its insertion next to certain other types of modules. These keys prevent problems associated with incompatible signal levels on the VXI daisy-chained .i.local bus;. Although the EPC-2 does not use the local bus, its ability to be a slot-0 controller means that it uses what would otherwise be "leftside" local bus lines for TTL .i.MODID; lines. Therefore the key prevents the EPC-2 from being installed to the immediate right of a module keyed for a "rightside" ECL, analog, or sensor local bus.

EXM Module Insertion (EPC-2x only)

The EPC-2x typically has one EXM installed in the front-panel slot (e.g., the .i.EPC-2e; contains an .i.EXM-1; or .i.EXM-10; Ethernet controller). If the EXM needs to be removed or replaced, loosen the two thumbscrews on the EXM and gently pull it out of its rear connector. To insert an EXM, slide the EXM into place in the card guides, push firmly on the EXM front panel to insert its rear connector, and tighten the thumb screws on the EXM's face plate.

Not all EXM types are compatible with the EPC-2x. You should not attempt to use a different type of EXM than that originally provided with your EPC-2x without first consulting with the supplier of your EPC-2x.

* make sure that power to your vxi system is off. exms are not designed to be inserted or removed from live systems.
* when inserting an exm, avoid touching the circuit board, and make sure the environment is static-free.

VXI Backplane Jumpers

.i.backplane jumpers;.i.daisy chain;.i.VME jumpers;.i.interrupt acknowledge;The VXIbus contains several daisy-chained control signals. Almost all VXIbus back-planes contain .i.jumpers; or DIP switches for these control signals to allow systems to operate with empty slots. Failing to install these jumpers properly is a common source of problems in building a new VXIbus system.

There are five jumpers per VXI slot, one for each of the four bus-grant arbitration levels and one for the interrupt-acknowledge daisy chain. Depending on the backplane manufacturer, the jumpers or DIP switches may be on the rear pins of the J1 connector, or may be alongside it on the front or rear side of the backplane. Based on what is in the VXI slot, install or remove the backplane jumpers as follows:

VXI slot content	IACK and bus-grant backplane jumpers
Empty slot	Install
EPC-2 left slot	Remove
EPC-2 right slot	Install
Other VXI modules	Remove
VME module	Consult manufacturer's literature

Connecting Peripherals to the EPC-2

The final step of installation is connecting peripherals, typically a video display and keyboard, but also perhaps a mouse, modem, printer, etc. Unless otherwise noted, all connectors are compatible with those found on IBM-compatible desktop PCs. Detailed pin assignments are described in Chapter 6.

Monitor

.i.VGA connector;A .i.monitor; is connected via the 15-pin D connector on the EPC-2 front panel. The graphics controller in the EPC-2 is .i.VGA; with analog color signals, meaning that old-style .i.EGA;, .i.CGA;, and monochrome monitors cannot be used. VGA monitors may be color or .i.gray-scale;; a parameter in the BIOS setup screen allows you to specify which type is being used. If using a

.i.multiscan monitor;, make sure to set the monitor's switch to analog (not TTL).
.i.monitor cables;Monitors that can be used are VGA-compatible monitors (i.e., those compatible with the IBM PS/2 and with PC VGA add-in cards) and multiscan (multifrequency or "multisync") monitors. If you cannot mate your monitor to the EPC-2 because you have a cable with a 9-pin connector, either (1) you have a TTL monitor that is not compatible with VGA or (2) you have a multisync monitor (which are usually shipped with 9- and 15-pin cables or adapters) and are using the wrong cable.
To ensure a reliable connection, the monitor's cable should be screwed into the EPC-2's connector.
Connecting a monitor is not absolutely necessary; its presence or absence does not affect the operation of the system. Also, the monitor can usually be safely connected and/or disconnected during operation.
The EPC-2 VGA controller supports some video modes beyond the standard IBM .i.VGA modes;, most importantly the 800 ´ 600 ´ 16-color mode. Use of this mode requires a .i.multiscan monitor;, as well as special software drivers. If .i.Windows 3.0; was purchased with your EPC-2, a special driver for this higher-resolution mode is provided on a separate diskette. Follow the installation instructions in the "readme" file on this diskette.
Flat-Panel Display
Use of certain VGA .i.flat-panel display;s requires access to more than the standard VGA signals, in particular to some signals provided on the .i.auxiliary video extension; or ".i.feature connector;" in the IBM PS/2. Installation of the three flat-panel .i.jumpers; as shown in the diagram earlier in this chapter brings three additional signals out to three normally unconnected pins on the 15-pin .i.VGA connector;. Two of these signals are the two low-order digital color signals, which are of use to flat panels supporting four shades of gray. The third is the logical AND of the dot clock and the alternate blanking signal. These three specific signals allow use of the .i.Fujitsu FPF8060;HRUK .i.plasma display;. Other flat-panel displays may or may not work with the EPC-2, depending on what video signals they require.
Note that gaining access to these signals requires construction of a custom cable; for more details, see Chapter 6.
.i.monitor problemsUse of a flat-panel display may require a special software driver; for instance Fujitsu distributes an .i.MS-DOS; driver with their FPF8060 display. For such displays that require software drivers, the EPC-2's BIOS selftest screen may appear garbled or may not appear at all, because it is displayed before the BIOS has booted the operating system.
Keyboard
The front panel contains a standard 5-pin PC/AT keyboard connector.
.i.keyboard errors;If the BIOS produces the message "KEYBOARD ERROR OR NO KEYBOARD PRESENT" at time of power-on or reset, either no keyboard is present, the keyboard cable is not firmly connected, a key was pressed, or the keyboard is not a PC/AT compatible keyboard.
If you wish to operate your system without a keyboard, you must start with a keyboard and invoke the BIOS .i.setup screen; to change the .i.configuration errors; field to "ignore .i.keyboard errors;." The system can then be booted with or without a keyboard.
Serial Ports
The front panel contains one or two DB-9 serial-port connectors. They are identical to the .i.serial port;s labelled .i.COM1; and .i.COM2; in the PC/AT and compatibles. They may be used for connecting a mouse, modem, serial printer, .i.RS-232; link, etc. On the EPC-2x, only one serial port - COM1 - exists.
The software drivers for most types of mouse detect the presence of the .i.mouse; dynamically, so it usually doesn't matter to which port the mouse is

connected. A common mistake is connecting the mouse too late (e.g., Microsoft Windows looks for a mouse when .i.Windows; is first invoked, so plugging a mouse in after Windows has been started has no effect).

Some PCs and PC peripherals contain DB-25 serial connectors instead of DB-9 connectors. Adapters converting from one to the other are readily available.

Parallel Printer Port

The .i.parallel port; on the front panel is compatible with the corresponding .i.LPT1; connector on IBM PCs and compatibles. Typically it is used to connect printers and software .i.security keys;..i.Printer port; A BIOS setup screen parameter lets you configure it in "normal" mode (electrically identical to the normal PC printer port) or in "input" mode (for use by parallel input devices, such as .i.scanner;s).

On the EPC-2 (not EPC-2x) the connector is a standard DB-25 connector. On the EPC-2x, the connector is a miniature 20-contact connector, compatible with a 3M 10320 plug or equivalent. The EPC-2x is supplied with an adapter cable that converts this to a standard DB-25 connector.

GPIB Port

The .i.GPIB port; is a standard shielded IEEE-488 receptacle.

External Clock Input

The EPC-2 provides the option, when it is configured as the slot-0 controller, of deriving the ECL .i.CLK10; signal from an internal oscillator or from a 10 MHz .i.external clock; source. An SMB connector is provided on the front panel. Its input impedance is 50 ohms. The external clock signal must have TTL levels. A function on the BIOS setup screen enables this external input.

3. Operation

This chapter contains information about user operation of the EPC-2.

System Reset

There are several ways for the operator to perform a system reset: pressing the reset switch on the front panel, simultaneously pressing the CTRL+ALT+DEL keys on the keyboard, invoking the BIOS setup program and following its instructions for reset, and power-off/power-on.

The reset switch performs a hardware reset of the EPC-2 and invokes the BIOS initialization routine, which performs a selftest of the hardware, initializes the EPC-2 hardware, locates the disk drives, and tries to boot an operating system.

If a keyboard is attached, pressing the CTRL+ALT+DEL keys causes a trap to the BIOS for a software-controlled reset. It is similar to pressing the reset switch, except no initial hardware reset occurs and only a subset of the selftest is performed. Unlike the reset switch, CTRL+ALT+DEL sometimes has no effect. The reason is that it is handled by software, and if the EPC-2 is currently "hung" somewhere in the operating system or application program in a state where interrupts are disabled, or if software has taken control of the keyboard interrupt, the CTRL+ALT+DEL sequence has no way of interrupting the software.

Removing and reapplying power to the EPC-2 also causes a hardware reset.

* **DISK DEVICES THAT AUTOMATICALLY PARK THEIR HEADS HAVE BEEN KNOWN TO FAIL OCCASIONALLY IF POWER IS REAPPLIED TOO QUICKLY. AFTER REMOVING POWER, WAIT 10 SECONDS OR MORE BEFORE REAPPLYING POWER.**

Generating VXIbus SYSRESET

When power is applied, the EPC-2 drives the VXIbus SYSRESET signal for at least the minimum time required by the VXIbus specification. Resetting the EPC-2 via the reset

switch or keyboard does *not* cause the EPC-2 to assert SYSRESET. The EPC-2 contains, however, a software-controllable register bit to allow software to assert SYSRESET.

Responding to VXIbus SYSRESET

A software-controllable register bit in the EPC-2 controls whether or not a hardware reset of the EPC-2 occurs when the VXIbus SYSRESET signal is asserted.

Front Panel Indicators

The EPC-2 contains the following three LEDs:

Run — This green LED should flicker during BIOS initialization and be lit thereafter. It denotes that the 386 is performing a DRAM access. If the LED is off, the most probable causes are (1) a "hung" condition has occurred in the operating-system or application software and (2) a VXIbus access is being attempted but the EPC-2 has not received a bus-grant signal. In the latter case, the usual reasons are an error in setting the jumpers on the VXIbus backplane, not being fully seated in the backplane, or a failure in the slot-0 system controller module.

Fail — This red LED can light only if the EPC-2 is configured as the VXIbus system controller. If lit, it indicates that some module is driving the VXIbus SYSFAIL line.

Test — This software-controllable yellow LED is used by the BIOS. It is lit whenever the BIOS is performing a hardware selftest, and is extinguished if and when the selftest is successful. It is possible for application software to use this LED for other purposes.

BIOS Screen Display

Whenever the EPC-2 is reset, information is displayed on the attached monitor showing the status of the BIOS selftest and the amount of memory found. If everything proceeds normally, the screen image should appear approximately as shown in the following figure.

```
386 Modular BIOS     Copyright Award Software
Copyright 1988-1989 RadiSys Corporation BIOS

TESTING INTERRUPT CONTROLLER #1  . . . . . . . . . . . OK
TESTING INTERRUPT CONTROLLER #2  . . . . . . . . . . . OK
TESTING CMOS BATTERY   . . . . . . . . . . . . . . . . OK
TESTING CMOS CHECKSUM  . . . . . . . . . . . . . . . . OK
TESTING VME INTERFACE  . . . . . . . . . . . . . . . . OK
TESTING VXI INTERFACE  . . . . . . . . . . . . . . . . OK
SIZING SYSTEM MEMORY   . . . . . . . . . . . . 640K FOUND
TESTING SYSTEM MEMORY  . . . . . . . . . . . . 640K    OK
CHECKING UNEXPECTED INTERRUPTS AND STUCK NMI . . . . . OK
TESTING PROTECTED MODE . . . . . . . . . . . . . . . . OK
SIZING EXPANSION MEMORY  . . . . . . . . . .  1024K FOUND
TESTING MEMORY IN PROTECTED MODE . . . . . .  1664K FOUND
TESTING PROCESSOR EXCEPTION INTERRUPTS . . . . . . . . OK
TESTING SERIAL PORT #1 . . . . . . . . . . . . . . . . OK
TESTING SERIAL PORT #2 . . . . . . . . . . . . . . . . OK
TESTING PARALLEL PORT  . . . . . . . . . . . . . . . . OK
TESTING IEEE 488 INTERFACE . . . . . . . . . . . . . . OK
```

If you are using a flat-panel display that requires loadable software drivers, this selftest screen may appear as garbled or not at all. If you are using a SCSI disk drive, the bottom of the screen will contain several messages from the SCSI BIOS.

For a 4 MB EPC-2 system, expect to see "3072K FOUND" for expansion memory. For an 8 MB EPC-2 system, expect to see "7168K FOUND" for expansion memory. For 16 MB, you should see "15360K FOUND."

Error messages that you might encounter during the execution of the BIOS initialization are:

KEYBOARD ERROR OR NO KEYBOARD PRESENT

This occurs if no keyboard is connected, if the keyboard is damaged or is not a PC/AT keyboard, or if keys are pressed during the BIOS selftest.

SCSI DISK FAILED

This occurs if the BIOS is expecting to find a bootable disk drive configured as SCSI drive 0, but the drive is not present or has failed.

ERROR ENCOUNTERED INITIALIZING HARD DRIVE

ERROR INITIALIZING HARD DISK CONTROLLER

This occurs if the BIOS is expecting to find a bootable AT (IDE) disk drive, but the drive is not present or has failed. Ensure that the EPC-2 is firmly seated in the back-plane and that both 5V and 12V are available to the EPC-2.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Invoke the BIOS setup function as described in the next section and ensure that floppy drive A is described as 1.44 MB and drive B is described as NONE. Then reset the system.

EXM CONFIGURATION ERROR (EPC-2x only)

This error indicates that configuration information in the EPC-2's nonvolatile CMOS RAM does not match the configuration of the actual EXM module in the EPC-2. You may hit any key to continue the initialization sequence, but you should not run any software that uses the EXMs until you correct the problem. To correct the problem, invoke the EXM setup screen as described in the next section.

BIOS Setup Screen

The EPC-2's BIOS contains a setup function to display and alter the system configuration. Some of this information is maintained in the EPC-2's nonvolatile CMOS RAM and is used by the BIOS to initialize the EPC-2 hardware. The remainder of the information is maintained in a nonvolatile control register.

To invoke the setup function in a "booted" system, press simultaneously the CTRL+ALT+ESC keys. This may be done during system operation in most, but not all circumstances. Some programs that take control of the keyboard at a low level, such as Windows 3.0, cause this key sequence to be interpreted differently, or not at all. It should always work, however, when the standard operating system prompt is shown on the screen. The setup function can be invoked prior to system booting by pressing CTRL+ALT+ESC immediately after the initial selftest screen is cleared. (In older

models of the EPC-2, the setup screen can only be invoked immediately after the SCSI Fixed Disk message appears near the bottom of the initial selftest screen appears.)

The main setup screen and two secondary ones will be similar to the following.

```
EPC-2 Setup Screen
20 MHz 386, 4 MBytes memory, no 387 present

Date (mm/dd/yy)              12/02/90
Time (hh:mm:ss)              09:34:56
Configuration Errors         Halt on all errors

Diskette Drive A             1.4M 3.5 inch
Diskette Drive B             None
Fixed Disk Drive C     AT
Fixed Disk Drive D     None

Bus Priority                 Pri 3
Bus Release Mechanism        RONR
Bus Arbitration              Priority
Slot 0 Functions             Internal clock

Parallel Port Mode           Normal (Printer)
VGA Monitor                  Color
```

```
Fixed Disk Menu

Fixed Disk Drive C: AT
  Type  36  252 MBytes:  1024 Cyls,   8 Heads,   63 Sectors
          Landing Zone: 1023        Precompensation: None

Fixed Disk Drive D: None
```

The EPC-2x has the following additional setup screen.

```
EXM Setup Screen

          ID OB1 OB2
Slot 0    FF  00  00
     1    FF  00  00
     2    FF  00  00
     3    FF  00  00
     4    FF  00  00
     5    FF  00  00
```

Some earlier models of the EPC-2 do not have the separate fixed disk menu; the disk options are on the initial setup screen.

Use the up and down cursor (arrow) keys to move from field to field. For most fields, once you are positioned at the field, pressing the left and right cursor (arrow) keys will rotate through the available choices. Once the screen has been changed to appear as you

desire, press the F10 function key, then the F5 function key, to save the changes in nonvolatile RAM and reboot. Press ESC to ignore any changes and exit.

The fields are explained below.

DATE and TIME

You change these values by moving the highlight to them and typing in the format shown.

CONFIGURATION ERRORS

This field gives you several choices about the situations under which the BIOS should wait for user input if a configuration error is found. The selections are (1) halt on all errors, (2) ignore all errors, (3) ignore keyboard errors (allows operation without a keyboard), (4) ignore disk errors, and (5) ignore keyboard and disk errors.

DISKETTE DRIVE

This field gives you several choices about the type of floppy disk drives installed as the A and B drives. Since the EPC-2 has a single 3.5" 1.44 MB floppy disk drive, the only correct setting of these parameters is that shown above.

FIXED DISK DRIVE

This field shows the type of disk selected from the fixed disk menu. To see the detailed characteristics of the device or to change the device, use the F3 function key to go to the fixed disk menu. If you have a SCSI disk, there are no options to select other than SCSI. (If you select SCSI for drive C, select SCSI also for nonexistent drive D.) If you have an IDE disk (the default on the revised EPC-2), use disk type AT. A label on the side of your EPC-2 should identify the specific drive installed. You can scroll through a set of numbered types; for each the physical configuration is displayed. It is possible to use a BIOS drive type that specifies a drive larger than the actual hard drive, which ensures access to the entire actual hard drive. When doing so, you must use the disk partitioning facilities provided by the operating system (e.g., FDISK) to tell the operating system to use only the amount of actual disk space available on the drive.

Although many different drive types may be used, the following are suggested.

Drive	Drive C definition	For DOS and OS/2	For Unix
SCSI	SCSI	Use FDISK; specify entire disk	Not supported
40 MB	At type 17	Use FDISK; specify entire disk	Not supported

100 MB	AT type 33	Use FDISK; specify 115 MB maximum for all partitions	Specify a maximum of 13950 tracks total for all partitions
200 MB	AT type 36	Use FDISK; specify 200 MB maximum for all partitions	Specify a maximum of 6550 tracks total for all partitions
50 MB	AT type 12	Use FDISK; specify entire disk	Automatic
110 MB	AT type 40	Use FDISK; specify entire disk	Automatic
240 MB	AT type 39	Use FDISK; specify entire disk	Automatic
400 MB	AT type 41	Use FDISK; specify entire disk	Automatic

BUS PRIORITY

This field allows you to select among the four VXIbus priority levels. This is the level at which the EPC-2 will contend for the bus when it performs a VXIbus access.

BUS RELEASE METHOD

This field allows you to toggle between two bus release modes: ROR (release on request) and RONR (request on no request, also known as the VXI fair-requester mode). ROR results in slightly better EPC-2 performance when accessing the VXIbus; RONR directs the EPC-2 to not "park" on the bus and thus slightly improves the access time of other VXIbus masters to the bus.

BUS ARBITRATION

This field toggles between the two arbitration algorithms provided by the EPC-2 when it is configured as the slot-0 system controller: priority arbitration and round-robin arbitration.

SLOT 0 FUNCTIONS

When the EPC-2 is configured as the slot-0 controller, this field allows you to specify INTERNAL CLOCK, meaning that an internal oscillator will generate the 10 MHz CLK10 signals, or EXTERNAL CLOCK, meaning that you are providing a front-panel 10 MHz clock input from which the EPC-2 should derive the CLK10 signals.

When the EPC-2 is configured as not a slot-0 controller (via the jumper settings described in Chapter 2), this field must be set to NONE.

PARALLEL PORT MODE

The printer port can be configured in two modes. NORMAL (PRINTER) mode configures the port identically to the configuration in most PCs. INPUT ONLY (SCANNER) configures it for parallel input devices.

VGA MONITOR

VGA monitors are color or gray-scale devices. Use this option to configure the EPC-2 to match your device.

EXM Configuration (EPC-2x only)

A separate setup screen, which is displayed by pressing the specified function key, contains information about the configuration of the EXM device. The EPC-2x's non-volatile RAM holds identification and configuration information for an EXM modules. The EPC-2x can hold only a single EXM module, which is EXM slot 0 (not to be confused with VXI slot 0). EXMs are shipped with a configuration program that allows you to specify EXM configurations in a symbolic high-level way. In addition, the BIOS displays the configuration information in low-level hexadecimal format and allows you to change it.

The first column (ID) is the unique ID expected for an EXM in that slot. FF denotes none. Other EXMs have unique IDs; for instance the ID of the EXM-1 Ethernet controller is FE and that of the EXM-10 Ethernet controller is F5. The next two columns are the EXM configuration bytes. The interpretation of the low-order bit of byte 1 is common for all EXMs: 1 denotes EXM enabled and 0 EXM disabled. The remaining bits in the configuration bytes are dependent on the specific EXM and are defined in the EXM manuals.

Normally the EPC-2x is shipped with an EXM installed and configured correctly. If for some reason you need to configure the EXM, use the EXM setup screen, not the standalone EXM configuration program. Follow the instructions in the specific EXM manual, considering the following additional restrictions due to the EPC-2 design:

1. If an interrupt is needed, use only IRQ3.
2. Do not use any DMA channels.
3. Do not select I/O addresses that conflict with those in the EPC-2. A complete list appears in Chapter 4. For instance, I/O addresses in the 300-377 range can be used.
4. If the EXM needs to use memory addresses, they must be in the 0D000-0DFFF range.

For instance, with an EXM-1, the suggested value for OB1 is 01h (Ethernet protocol) or 03h (802.3 protocol). With an EXM-10, the suggested value for OB1 is 01h (thin Ethernet cable) or 03h (thick Ethernet cable). For EXM-4, the suggested value for OB1 is 3Bh.

Disk Formatting

The hard disk in the EPC-2 is shipped from the factory low-level formatted with the proper interleave factor. Depending on the context in which you ordered the EPC-2, the disk is either bootable (containing an operating system and other software pre-installed) or empty and not high-level formatted.

If you wish to install a different operating system, including a version of MS-DOS earlier than version 4.0, you will probably need to first reformat the disk. Follow the instructions in your operating system manual. For instance, to install MS-DOS 3.3, you will need to run the MS-DOS 4.0 FDISK program to delete the partition and then boot the system from the MS-DOS 3.3 floppy diskette and use the FDISK and SELECT programs.

When installing DOS from floppy diskettes, be careful not to intermix Microsoft's version of DOS (MS-DOS) with IBM's version (PC-DOS). This can cause problems because the hidden files referenced by the boot block have different names in each. If you are installing MS-DOS, install it using original MS-DOS diskettes or diskettes formatted on an MS-DOS system. If you are installing PC-DOS, install it using original PC-DOS diskettes or diskettes formatted on a PC-DOS system.

Floppy Disk Formatting

Floppy diskettes can be formatted with the standard DOS or OS/2 format command, such as

```
format a:
```

which will format the diskette in drive A as a 1.44 MB nonsystem diskette. A frequent mistake is using this command to format a 720 KB diskette. To format a 720 KB diskette, use the command

```
format a: /N:9 /T:80
```

Low-level IDE (AT) Disk Formatting

For low-level formatting of an IDE hard drive, a disk utility must be used, such as DOSUTILS from Ontrack Computer Systems, Inc., QAPlus from DiagSoft, Inc., AMIDIAG from American Megatrends Inc., or SuperSoft Service Diagnostics from SuperSoft Inc.

Low-level SCSI Disk Formatting

In rare circumstances you might wish to do a low-level format and reinitialization of the SCSI drive. To do so, enter the BIOS setup function, and then press the indicated function key to enter the SCSI setup function.

You are now ready to do a low-level format of the disk, by pressing F1 and following the subsequent instructions. Do not split the drive into multiple volumes even if you see a warning that the volume is too large for DOS. If you are asked for drive parameters, they depend on the type of disk installed in your EPC-2. Some representative drives are specified in the following table. If your EPC-2 has another type of SCSI drive, call customer service for assistance.

Parameter 0	CP340	CP3040	CP3010
Cylinders	788	513	761
Heads	4	4	8
Sectors/track	26	40	40
Verify	yes	yes	yes
Interleave	4 (16 MHz) 3 (20 MHz)	1	1

When done, exit to the BIOS setup function and press F10 and then F5 to reboot. The new drive is now ready for high-level formatting.

CP-3040/CP-30100 Note: The CP-3040 actually has 1026 cylinders and 2 heads, and the CP-30100 has 1522 cylinders and 4 heads. The numbers in the table should be used, however, to circumvent the disk BIOS's limitation of 1023 cylinders.

4. Programming Interface

This chapter describes the EPC-2 as seen by a program. Wherever possible, users should avoid direct use of most of these facilities. Hardware features in common with standard PCs should be accessed by standard BIOS calls. Hardware unique to EPC-2, such as the VXIbus interface should be accessed through the .i.EPConnect; .i.Bus Manager;, an easy-to-use, high-level interface that frees you from most machine-dependent considerations.

Memory Map

.i.memory map;The 232 byte physical address space seen by the 386 is mapped as follows:

Range		Content
00000000	0009FFFF	DRAM (first 640 KB)
000A0000	000BFFFF	Video RAM
000C0000	000CFFFF	Write-protected DRAM containing VGA video BIOS
000D0000	000DFFFF	In EPC-2, mapped to interface of optional EPC-2AM module. In EPC-2x, mapped to the EXMbus
000E0000	000EFFFF	Mappable window onto VXI data transfer bus
000F0000	000FFFFF	Write-protected DRAM containing BIOS
00100000	00FEFFFF	Extended memory DRAM
00FF0000	00FFFFFF	Mapped to BIOS ROM for PC compatibility
02000000	FEFFFFFF	Mapped to VXIbus data-transfer bus .i.A32; space
FF000000	FFFFFFFF	386 upper ROM area

I/O Map
.i.I/O space map;The following defines the I/O addresses decoded by the EPC-2.
It does not define addresses that might be decoded by EXMs in the EPC-2x.

Port	Functional group	Usage
00	DMA	Channel 0 address
01		Channel 0 count
02		Channel 1 address
03		Channel 1 count
04		Channel 2 address
05		Channel 2 count
06		Channel 3 address
07		Channel 3 count
08		Command/status
09		DMA request
0A		Command register (R)
		Single-bit DMA req mask(W)
0B		Mode
0C		Set byte pointer (R)
		Clear byte pointer (W)
0D		Temporary register (R)
		Master clear (W)
0E		Clear mode reg counter (R)
		Clear all DMA req mask(W)
0F		All DMA request mask
20	Interrupt controller 1	Port 0
21		Port 1
22	82C301/304	Configuration
23		Configuration
40	Timer	Counter 0
41		Counter 1
42		Counter 2
43		Control (W)
60	Keyboard controller	Data I/O register
61	NMI status	NMI status
64	Keyboard controller	Command/status register
70	Real-time clock	RTC index reg / NMI enable
71		RTC data register
		0 seconds
		1 seconds alarm
		2 minutes
		3 minutes alarm
		4 hours
		5 hours alarm
		6 day of week
		7 date of month
		8 month

```
Port  Functional group  Usage

            9     year
            A     status A
            B     status B
            C     status C
            D     status D
            E     RAM
            ...
            3F    RAM

81    DMA   Channel 2 page register
82          Channel 3 page register
83          Channel 1 page register
87          Channel 0 page register
89          Channel 6 page register
8A          Channel 7 page register
8B          Channel 5 page register
8F          Refresh page register

96    EXM Configuration EXMID driver (EPC-2x) (W)

A0    Interrupt controller 2  Port 0
A1          Port 1

C0    DMA   Channel 4 address
C2          Channel 4 count
C4          Channel 5 address
C6          Channel 5 count
C8          Channel 6 address
CA          Channel 6 count
CC          Channel 7 address
CE          Channel 7 count
D0          Command/status
D2          DMA request
D4          Command register (R)
            Single-bit DMA req mask(W)
D6          Mode
D8          Set byte pointer (R)
            Clear byte pointer (W)
DA          Temporary register (R)
            Master clear (W)
DC          Clear mode reg counter (R)
            Clear all DMA req mask (W)
DE          All DMA request mask
F0    Coprocessor Clear coprocessor busy
F1          Reset coprocessor

1F0   IDE controller    Data register
1F1         Error / write precompensation
1F2         Sector count
1F3         Sector number
1F4         Cylinder low register
1F5         Cylinder high register
1F6         SDH register
1F7         Status/command register
```

2B0	SCSI controller	Current data (R) Output data (W)

Port	Functional group	Usage
2B1		Initiator command
2B2		Mode
2B3		Target command
2B4		Bus status (R) Select enable (W)
2B5		Bus and status register (R) Start DMA send (W)
2B6		Input data (R) Start DMA target receive (W)
2B7		Reset parity/interrupts (R) Start DMA initiator recv (W)
2B8	IEEE 488 Controller	Data-in / Byte-out
2B9		Interrupt status/mask 1
2BA		Interrupt status/mask 2
2BB		Serial poll status/mode
2BC		Address status/mode
2BD		Command pass-through / Auxiliary mode
2BE		Address 0
2BF		Address 1 / End of string
2F8	COM2 serial port	Receiver/transmitter buffer Baud rate divisor latch (LSB)
2F9		Interrupt enable register Baud rate divisor latch (MSB)
2FA		Interrupt ID register
2FB		Line control register
2FC		Modem control register
2FD		Line status register
2FE		Modem status register
378	LPT1 parallel port	Printer data register
379		Printer status register
37A		Printer control register
3B4	Video controller	CRT index register (mono)
3B5		CRT ctlr data reg (mono)
	0	Horizontal total register
	1	Horiz display enable end
	2	Start horiz blanking
	3	End horizontal blanking
	4	Start horiz retrace pulse
	5	End horizontal retrace
	6	Vertical total register
	7	Overflow
	8	Preset row scan
	9	Max scan line/others
	A	Cursor start
	B	Cursor end
	C	Start address high
	D	Start address low
	E	Cursor location high
	F	Cursor location low
	10	Vertical retrace start

```
11    Vertical retrace end
12    Vert display enable end
```

```
Port  Functional group  Usage

            13    Offset
            14    Underline location
            15    Start vertical blank
            16    End vertical blank
            17    CRTC mode control
            18    Line compare
3B8         Mode control reg (mono) (W)
3B9         Preset light pen (mono) (W)
3BA         Input status reg 0 (mono) (R)
            Feature control (mono) (W)
3BB         Clear light pen (mono) (W)
3BF         Hercules register
3C0         Attribute index register
            Attribute data register (W)
3C1         Attribute data register (R)
            0X    Palette registers
            10    Attribute mode control
            11    Overscan control
            12    Color plane enable
            13    Horizontal PEL panning
            14    Color select
3C2         Misc output register (W)
            Input status register 0 (R)
3C3         Video subsystem enable reg
3C4         Sequencer index register
3C5         Sequencer data register
            0     Reset register
            1     Clocking mode register
            2     Map mask register
            3     Character map select reg
            4     Memory mode register
3CA         Feature control register (R)
3CC         Misc output register (R)
3CE         Graphics controller index reg
3CF         Graphics data register
            0     Set/reset
            1     Enable set/reset
            2     Color compare
            3     Data rotate
            4     Read map select
            5     Graphics mode
            6     Miscellaneous
            7     Color don't care
            8     Bit mask
            9     Address offset A (PR0A)
            A     Address offset B (PR0B)
            B     Memory size (PR1)
            C     Video select (PR2)
            D     CRT control (PR3)
            E     Video control (PR4)
            F     Lock/status (PR5)
3D4         CRT index register (color)
3D5         CRT controller data (color)
            0     Horizontal total
            1     Horiz display enable end
```

2 Start horizontal blanking

```
Port  Functional group  Usage

            3     End horizontal blanking
            4     Start horiz retrace pulse
            5     End horizontal retrace
            6     Vertical total register
            7     Overflow
            8     Preset row scan
            9     Max scan line/others
            A     Cursor start
            B     Cursor end
            C     Start address high
            D     Start address low
            E     Cursor location high
            F     Cursor location low
            10    Vertical retrace start
            11    Vertical retrace end
            12    Vert display enable end
            13    Offset
            14    Underline location
            15    Start vertical blank
            16    End vertical blank
            17    CRTC mode control
            18    Line compare
3D8         Mode control reg (color) (W)
3D9         Color select register (W)
3DA         Input status reg 0 (color) (R)
            Feature control (color) (W)
3DB         Clear light pen (color) (W)
3DC         Preset light pen (color) (W)
3DE         AT&T / M24 (W)

3F2   Floppy disk controller  Operations
3F4         Command
3F5         Data
3F7         Control, also IDE drive
            address register

3F8   COM1 serial port  Receiver/transmitter buffer
            Baud rate divisor latch (LSB)
3F9         Interrupt enable register
            Baud rate divisor latch (MSB)
3FA         Interrupt ID register
3FB         Line control register
3FC         Modem control register
3FD         Line status register
3FE         Modem status register

8100  Memory mapping    Mapping register
8102        Mapping register
8104        Mapping register
8106        Mapping register
8108        Mapping register
810A        Mapping register
810C        Mapping register
810E        Mapping register
8110        Mapping register
```

8112	Mapping register
8114	Mapping register

Port	Functional group	Usage
8116		Mapping register
8118		Mapping register
811A		Mapping register
811C		Mapping register
811E		Mapping register
8120		Reserved
8122		Reserved
8124		Reserved
8126		Reserved
8128		Reserved
812A		Reserved
812C		Reserved
812E		Reserved
8130	E page mapping	E0xxx mapping
8132		E4xxx mapping
8134		E8xxx mapping
8136		ECxxx mapping
8138	Memory mapping	Mapping register
813A		Mapping register
813C		Mapping register
813E		Mapping register
8140	VXI Registers	ID low
8141		ID high
8142		Device type low
8143		Device type high
8144		Status/control low
8145		Status/control high
8146		Slave offset low
8147		Slave offset high
8148		Protocol/Signal low
8149		Protocol/Signal high
814A		Response low
814B		Response high
814C		Message high low
814D		Message high high
814E		Message low low
814F		Message low high
8150	VXI/VME Control Regs	VME map WA31-24
8151		VME modifier
8152		VME interrupt state
8153		VME interrupt enable
8154		VME event state
8155		VME event enable
8156		TTL trigger sample
8158		MODID/Interrupter
8159		MODID upper
815A		TTL trigger drive
815B		ECL trigger
815C		ULA
815D		Module status/control
815E		Signal FIFO (lower)
815F		Signal FIFO (upper)

Registers Specific to EPC-2
Registers in the I/O space that are specific to the EPC-2 are defined below.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I/O port
1	1	1	1	1	1	1	EXMI	

96
.i.EXMID Driver Register;

81xx
.i.Memory Mapping Registers;

VMEbus Address bits 21-14

8130/
2/4/6
.i.VME A21-14 Address Registers;

1	1	1	0	1	1	0	0

8140
.i.ID Register;, lower

1	0	0	1	1	1	1	1

8141
ID Register, upper

1	1	1	1	1	1	1	1

8142
.i.Device Type Register;, lower

0	1	1	1	0	0	0	S

8143
Device Type Register, upper

SRIE	POSR	SYSC	1	READY	PASS	NOSF	RSTP

8144
.i.Status/Control Register;, lower

SLE	MODID	SYSR	1	1	1	1	1

8145
Status/Control Register, upper

8146
.i.Slave Offset Register;, lower

0	0	0	1	1	SLAVE BASE

8147
Slave Offset Register, upper

1 1 1 1 1 1 1 1

8148
.i.signal register;.i.Protocol/Signal Register;, lower

0 0 0 1 1 0 1 1

8149
Protocol/Signal Register, upper

LOCK 1 ABMH SIG MLCK WRCP FSIG LSIG

814A
.i.Response Register;, lower

0 1 DOR DIR ERR RRDY WRDY 1

814B
Response Register, upper

814C
.i.Message High Register;, lower

814D
Message High Register, upper

814E
.i.Message Low Register;, lower

814F
Message Low Register, upper

VMEbus Address bits 31-24

8150
.i.VME A31-24 Address Register;

VME WA23-22 BORD IACK AM5 AM4 AM2 AM1

8151
.i.VME Modifier Register;

IRQ7 IRQ6 IRQ5 IRQ4 IRQ3 IRQ2 IRQ1 MSGR

8152

.i.VME Interrupt State Register;

IRQ7 IRQ6 IRQ5 IRQ4 IRQ3 IRQ2 IRQ1 MSGR

8153
.i.VME Interrupt Enable Register;

1 1 1 SIGR WDT ACFA BERR SYSF

8154
.i.VME Event State Register;

DSOR VWR 1 SIGR WDT ACFA BERR SYSF

8155
.i.VME Event Enable Register;

TTS7 TTS6 TTS5 TTS4 TTS3 TTS2 TTS1 TTS0

8156
.i.TTL Trigger Sample Register;

MO04 MO03 MO02 MO01 MO00 INTERRUPT-OUT

8158
.i.MODID / Interrupt Generator Register;

MO12 MO11 MO10 MO09 MO08 MO07 MO06 MO05

8159
.i.MODID Upper Register;

TTD7 TTD6 TTD5 TTD4 TTD3 TTD2 TTD1 TTD0

815A
.i.TTL Trigger Drive Register;

ES1 ES0 ED1 ED0 1 SBER 1 BSAM

815B
.i.ECL Trigger / Miscellaneous Register;

815C
.i.Unique Logical Address Register;

1 IST POSW BTOE WDTR FWDT 1 1

815D
.i.Module Status/Control Register;

815E
.i.Signal Register FIFO;, lower

815F
Signal Register FIFO, upper
Certain of these registers, and a few additional registers, are also mapped into the VXIbus A16 address space as 16-bit registers. These registers begin at a base related to the EPC-2's logical address. This base is given by

11uu uuuu uu00 0000

where uuuuuuuu is the EPC-2's .i.unique logical address; (.i.ULA;). The EPC-2 is a VXI .i.DC device; (.i.dynamic configuration;), meaning that after a system reset, its ULA is FFh, and it only responds to A16 accesses at the resultant base FFC0h and beyond if the MODID line is asserted. Once the EPC-2 is assigned a ULA, uuuuuuuu becomes this new ULA (whose value appears in the ULA register). The mapping of registers in the A16 space is shown below. For registers that are also accessible from within the EPC-2 via an I/O address, the I/O address is given in parentheses.

Offset	Upper byte	Lower byte
0	ID (8141)	ID (8140)
2	Device type (8143)	Device type (8142)
4	Status/control (8145)	Status/control (8144)
6	Slave offset (8147)	Slave offset (8146)
8	Protocol/signal (8149)	Protocol/signal (8148)
A	Response (814B)	Response (814A)
C	Message high (814D)	Message high (814C)
E	Message low (814F)	Message low (814E)
14	.i.Shared memory pointer; high	
16	Shared memory pointer low	
18	.i.Alternate response register;	

Where a bit position has been described by a 0 or 1, the bit is a ROM bit, and writing to it has no effect. Unless otherwise noted below, all registers and bit values are readable and writeable.

.i.EXMID Driver Register; (EPC-2x only)

1	1	1	1	1	1	1	EXMI

96
This write-only register is used to assert a -.i.EXMID signal; to the EXM slot. When EXMI=0, the ÄEXMID signal is asserted; when EXMI=1, it is not asserted.

.i.Memory Mapping Registers;

81xx
These registers are used by the EPC-2's BIOS to create the memory map described at the beginning of this chapter. Their function is not described in this manual.

.i.VME A21-14 Address Registers;

VMEbus Address bits 21-14

8130/
2/4/6
When an access is performed by the EPC-2 in its ".i.E page;" (address range 0E0000-0EFFFF), the access is mapped onto the VMEbus (VXI data transfer bus). The least-significant 14 of the VME address bits are provided directly (from the 386). The remaining 2 (for an A16 access), 10 (for an A24 access), or 18 (for an A32 access) bits must come from somewhere else. Eight of them come from

these registers. Bit 7 of this register is used as VME address bit 21, bit 6 as VME address bit 20, ..., and bit 0 as VME address bit 14.
Bits 14-15 of the 386's address select among these four registers. Thus the register at 8130 is associated with the address range 0E0000-0E3FFF, the one at 8132 with 0E4000-0E7FFF, and so on. The suggested usage is to maintain the two low-order bits of these registers as 00, 01, 10, and 11, respectively. This makes the E page one contiguous 64 KB window onto the VME/VXI data transfer bus.
.i.ID Register; (.i.VID;)

1	1	1	0	1	1	0	0

8140

1	0	0	1	1	1	1	1

8141
This register defines the EPC-2 as a .i.message-based device; that is mapped into the A16/A32 address spaces with the manufacturer being Radix MicroSystems (.i.manufacturer code; 4076).
Since the EPC-2 is a .i.DC device; (a device without a static ULA, but a ULA that can be assigned dynamically by the .i.resource manager;), an initial write into this register from the VXIbus assigns a ULA to the EPC-2.
.i.Device Type Register; (.i.VDT;)

1	1	1	1	1	1	1	1

8142

0	1	1	1	0	0	0	S

8143
This read-only register denotes that the EPC-2 responds to a 16 MB range in the .i.A32; space and has a .i.model code; of 255 (S=0) or 511 (S=1). S is controlled by the SLOT 0 FUNCTIONS parameter on the BIOS setup screen. S=0 (model code 255) means that the EPC-2 is configured as a slot-0 controller.
.i.Status/Control Register; (.i.VSC;)

SRIE	POSR	SYSC	1	READY	PASS	NOSF	RSTP

8144

SLE	MODID	SYSR	1	1	1	1	1

8145
This register contains VXI specified bits and EPC-2 device-dependent bits.
SLE .i.Slave enable;. If set (1), the EPC-2 will respond to certain A32 accesses from the VXI data-transfer bus.
.i.MODID; If clear (0), it denotes that the EPC-2's MODID pin is being asserted.
SYSR SYSRESET. The EPC-2 asserts the VXI .i.SYSRESET; line while this bit is 1. When using this bit, it is software's responsibility to ensure that the VXI/VME specified minimum assertion time of SYSRESET is met.
SRIE .i.SYSRESET input enable;. If set, assertion of VXI SYSRESET generates a reset of the EPC-2. One use of this bit is having software reset the VXI system (via bit SYSR) without resetting the EPC-2.
POSR This specifies the value of the low-order bit of the .i.nonvolatile option register;, a shift register in the EPC-2 also known as the .i.POS register;.
SYSC This is an indicator of whether the VXI .i.SYSCLK; signal is functioning. After SYSC is cleared by software, four SYSCLK rising edges will cause SYSC to be set.
READY This RAM bit, if set while PASS=1, denotes that the EPC-2 is ready to accept operational commands. In earlier versions of this manual, this bit was

named EXTE. Its implementation hasn't changed, but it was renamed to correspond to the renaming of the bit in revision 1.3 of the VXIbus specification.
PASS If set (1), the EPC-2 has completed its .i.selftest; successfully. If this bit is clear, the .i.Test LED; on the EPC-2 front panel is lit.
NOSF .i.SYSFAIL inhibit;. If set, the EPC-2 cannot assert the VXI SYSFAIL line.
RSTP Reset EPC. Setting this bit will .i.reset; the EPC-2.
.i.Slave Offset Register; (.i.VSO;)

8146

0	0	0	1	1	SLAVE BASE

8147

If SLE is set, the value in port 8147 defines the base address of the EPC-2's memory in the VXIbus A32 address space. This register can hold the values 18-1F, which correspond to the base addresses 18000000-1F000000.
The value in the lower part of this register (port 8146) is read-only from the VXIbus. See the definition of the VSH register for explanation.
.i.Protocol/Signal Register; (.i.VPR;)

1	1	1	1	1	1	1	1

8148

0	0	0	1	1	0	1	1

8149

The .i.protocol register; (the read value) defines the EPC-2 as being a .i.servant; and .i.commander;, having a .i.signal register;, being a bus master and an interrupter, providing the shared-memory protocol, and not providing .i.fast handshake mode;.
When written to from the VXIbus, this register is the .i.signal register;. The value written enters the signal FIFO (two deep) or returns a bus error (.i.BERR;) if the FIFO is already full.
.i.Response Register; (.i.VRE;)

LOCK	1	ABMH	SIG	MLCK	WRCP	FSIG	LSIG

814A

0	1	DOR	DIR	ERR	RRDY	WRDY	1

814B

This register contains some VXI-defined state bits associated with message handling, and several EPC-2 dependent bits.
DOR RAM bit available to software. Initialized to 0.
DIR RAM bit available to software. Initialized to 0.
ERR RAM bit available to software. Initialized to 1.
RRDY .i.Read ready;. A 1 denotes that the message registers contain outgoing data to be read by another device. RRDY is cleared when the .i.message low register; is read.
WRDY .i.Write ready;. If set, the message registers are armed for an incoming message. When a write occurs into the .i.message low register;message-low register, WRDY is cleared and the .i.MSGR interrupt; condition is asserted.
LOCK RAM bit available to software. Initialized to 1.
ABMH This EPC-2 specific bit is cleared when the .i.message high register; is read or written from the VXIbus. It serves as a .i.location monitor; for determining whether a message is 16 or 32 bits in length.
SIG If this EPC-2 specific bit is 0, the .i.signal register FIFO; is empty.

MLCK This EPC-2 specific bit is used for synchronization of messages from multiple senders, something not provided for in the VXI specification. If 1, the .i.message register; can be locked for the sending of a message. If 0, the message register has been .i.lock;ed.
WRCP This EPC-2 specific bit is a read-only copy of the WRDY bit.
FSIG Defined only when SIG=1, in which case FSIG is the number (0 or 1) of the register in the FIFO holding the earliest signal.
LSIG Defined only when SIG=1, in which case LSIG is the number (0 or 1) of the register in the FIFO holding the most recent signal.
FSIG and LSIG have no utility to software. They exist as read-only bits for tests of the EPC-2 during manufacture.
Message High Register (.i.VMH;)

814C

814D
.i.message high register;This register is an extension of the VML register for 32-bit .i.longword serial messages;. An access to this register in the A16 space on the VXIbus clears flag ABMH in the .i.response register;.
Message Low Register (.i.VML;)

814E

814F
.i.message low register;This register is typically used as an incoming message register for .i.word-serial messages;; the sender does D16 writes into it from the VXIbus.
Shared Memory Pointer Register (.i.VSH;,.i.VSL;)

14

16
.i.shared memory pointer;These registers form a 32-bit address register for the optional shared-memory protocol. The upper 16 bits (VSH) are not a physically distinct register; they are the same as the .i.VSO; register. Writing the upper 8 bits of VSH has no effect; writing the lower 8 bits of VSH changes the lower 8 bits of VSO (and vice versa).
.i.Alternate Response Register; (.i.VARE;)
 LOCK 1 ABMH SIG MLCK WRCP FSIG LSIG

18
 1 1 1 1 1 1 1 1

19
.i.alternate response register;The upper half of this register is 1111 1111 and the lower half is a read-only copy of the lower half of the .i.VRE; .i.response register;. This register is associated with multiple senders of messages to the EPC-2 and the MLCK bit; reading this register performs a test-and-set operation on MLCK if WRDY is set.
The protocol for synchronization of multiple senders of messages is as follows. A sender must first read VARE. If both WRDY and MLCK are set, the sender can

send the message; otherwise the sender must reread VARE until this condition is true. For 16-bit messages, the sender writes into .i.VML;. For 32-bit messages, the sender must write into .i.VMH; before writing into VML.
The bits RRDY, WRDY, ABMH, and MLCK in the .i.response register; are altered by hardware-detected conditions. A read from VML clears RRDY. A write into all or the lower 8 bits of VML clears WRDY. A read or write to all or the lower 8 bits of VMH clears ABMH. A read of VARE clears MLCK if WRDY is set.
.i.VME A31-24 Address Register; (.i.BWA;)
VMEbus Address bits 31-24

8150
This register is one of several that supply the VXIbus address bits when the EPC-2 makes an access in its ".i.E page;." This register supplies address bits A31-A24.
.i.VME Modifier Register; (.i.BWM;)
VME WA23-22 BORD IACK AM5 AM4 AM2 AM1

8151
.i.VMEbus address modifier;.i.address modifier;This register is also used when the EPC-2 makes an access through its .i.E page; to the VXIbus. Bits 7 and 6 provide VXI address bits A23 and A22, respectively. Bits 3-0 define the value placed on the associated VXI address-modifier lines. Register bits are not defined for the address-modifier AM3 and AM0 lines since, for all defined address-modifier values in the VMEbus specification, AM3 is 1 and AM0 is the inverse of AM1. Therefore these two bit values are generated by hardware.
BORD .i.byte ordering;Byte order. This bit controls the ordering of data bytes for D16 and D32 VXIbus accesses. If 0, the bytes are transmitted in .i.little endian; (Intel) order; if 1, byte-swapping hardware transmits the bytes in .i.big endian; (Motorola) order. Refer to a subsequent section in this chapter for more information on byte ordering.
IACK This bit, when set, is used to define the VXIbus access as an .i.interrupt acknowledge; cycle. The interrupt being acknowledged must be encoded by software as a value on address lines A1-A3.
.i.VME Interrupt State Register; (.i.BIS;)
IRQ7 IRQ6 IRQ5 IRQ4 IRQ3 IRQ2 IRQ1 MSGR

8152
This read-only register defines the state of the VXI and message interrupts.
IRQx If clear (0), the associated VXI interrupt line is asserted.
MSGR If clear (0), a .i.message interrupt; is being signalled. MSGR is clear if both of bits RRDY and WRDY in the .i.response register; are clear..i.MSGR interrupt;
.i.VME Interrupt Enable Register; (.i.BIE;)
IRQ7 IRQ6 IRQ5 IRQ4 IRQ3 IRQ2 IRQ1 MSGR

8153
This is a mask of the interrupt conditions in the interrupt state register. A 1 denotes that the corresponding interrupt is enabled. If any bit in this register is a 1 and the corresponding bit in the interrupt state register is a 0, the EPC-2 .i.IRQ10 interrupt; is asserted. Software may then examine the interrupt and event state registers to determine the cause.
.i.VME Event State Register; (.i.BES;)
1 1 1 SIGR WDT ACFA BERR SYSF

8154

Similar to the interrupt state register, this register defines additional conditions that may result in an .i.IRQ10 interrupt;. If the bit is 0, the condition is present.
SIGR .i.Signal register FIFO; is not empty.
WDT The EPC-2 .i.watchdog timer; period has expired.
ACFA VXIbus .i.ACFAIL; is asserted.
BERR An access from the EPC-2 to the VXIbus was terminated with a .i.BERR; (.i.bus error;).
SYSF VXIbus .i.SYSFAIL; is asserted.
.i.VME Event Enable Register; (.i.BEE;)
DSOR VWR 1 SIGR WDT ACFA BERR SYSF

8155
The low-order five bits are a mask of the interrupt conditions in the event state register. A 1 denotes that the corresponding event is enabled as an interrupt. If any bit in this register is a 1 and the corresponding bit in the event state register is a 0, the EPC-2 .i.IRQ10 interrupt; is asserted. Software may then examine the interrupt and event state registers to determine the cause.
The following two bits are read-only state bits:
DSOR Clear whenever either of the VXI DS0/DS1 .i.data strobes; is asserted. DSOR=0 thus indicates a data transfer in progress.
VWR When DSOR is 0, VWR=0 indicates that the data transfer is a write operation.
.i.TTL Trigger Sample Register; (.i.BTTS;)
TTS7 TTS6 TTS5 TTS4 TTS3 TTS2 TTS1 TTS0

8156
This read-only register contains the state of the eight TTL trigger lines on the VXI J2 backplane. A 1 denotes an asserted trigger. Note that this register does not necessarily match the value in the TTL drive register because of the open-collector nature of the trigger lines.
.i.MODID / Interrupt Generator Register; (.i.BMOL;)
MO04 MO03 MO02 MO01 MO00 INTERRUPT-OUT

8158
This register serves two purposes: an extension of the MODID bits in the BMOH register, and VXI .i.interrupt generation;.
If the three low-order bits are not 000, one of the seven VXI interrupt lines is asserted by the EPC-2. The line is the decoded value of these three bits (e.g., 001 denotes IRQ1, 111 denotes IRQ7). If and when an .i.interrupt acknowledge; cycle is sent to the EPC-2, the INTERRUPT-OUT bits are cleared. Software can also deassert an asserted interrupt by clearing these bits at any time. A reset of the EPC-2 or setting bit RSTP in the .i.VSC; register clears the INTERRUPT-OUT bits.
.i.MODID Upper Register; (.i.BMOH;)
MO12 MO11 MO10 MO09 MO08 MO07 MO06 MO05

8159
This register and BMOL drive and sample the LBUSA .i.local bus; signals on the VXI P2 connector. When the EPC-2 is installed in .i.slot 0;, these signals are the MODID signals on the VXI backplane. The bits named MO00-MO12 are associated with signals MODID00-MODID12.
When a write occurs to BMOH, the EPC-2 drives the MODID signals on the back-plane. A read of BMOH terminates the driving of the signals; the value returned from this "driver-terminating" read is not specified and should not be used. All other reads of BMOH and BMOL sample the MODID signals from the backplane. A

reset of the EPC-2 or setting bit RSTP in the .i.VSC; register terminates driving of the MODID lines.

.i.TTL Trigger Drive Register; (.i.BTTD;)

TTD7	TTD6	TTD5	TTD4	TTD3	TTD2	TTD1	TTD0

815A

This read/write register drives the VXI TTL trigger lines; a 1 bit causes the associated trigger line to be asserted. The actual change in state to the trigger lines is synchronized to the 10 MHz .i.CLK10; to support the VXI trigger .i.start/stop protocol;. Reading this register does not sample the triggers; it simply returns what was previously stored in this register. Sampling the trigger lines is performed with register .i.BTTS;.

A reset of the EPC-2 clears this register.

.i.ECL Trigger / Miscellaneous Register; (.i.BET;)

ES1	ES0	ED1	ED0	1	SBER	1	BSAM

815B

This read/write register contains the following bits:

ES Read-only bits that show the state of the ECL trigger lines on the backplane (1 meaning asserted).

ED A 1 asserts the corresponding ECL trigger.

SBER ".i.Sticky BERR;." This bit is cleared whenever an VXI data-transfer bus access by the EPC-2 is terminated by a .i.BERR;. By initially setting the bit and then performing a series of data transfers, software can determine if a bus error occurred. (Alternatively, software could examine the BERR bit in the .i.BES; register after each access, or enable the BERR event to generate an interrupt.)

BSAM This bit is 0 if a pipelined write is active from the EPC-2 onto the VXI data-transfer bus. It allows software to wait for the completion of a write (e.g., to determine when SBER can safely be examined after a series of writes).

.i.Unique Logical Address Register; (.i.BULA;)

815C

This register contains the EPC-2's .i.ULA;. Until a value is stored in this register, the EPC-2's register base in the A16 space is FFC0, and it responds only when its MODID is asserted. The ULA is changed by writing into this register or into the .i.ID register; (.i.BID;).

.i.Module Status/Control Register; (.i.MSC;)

1	IST	POSW	BTOE	WDTR	FWDT	1	1

815D

This register contains the following miscellaneous status and control bits:

IST This bit specifies whether a response .i.status/ID; or an event status/ID is used in an .i.interrupt acknowledge cycle;.

If IST is 0, the response format is used. In the 16-bit status/ID value returned, the upper 8 bits are the value of the upper 8 bits of the .i.BRE; .i.response register;, and the lower 8 bits are the EPC-2's .i.ULA;.

If IST is 1, the event format is used. The upper 8 bits of the status/ID value are the value of the upper 8 bits of the .i.VMH; .i.message high register;, and the lower 8 bits are the EPC-2's ULA. In this case software uses the VMH register for the event code, meaning that .i.longword serial messages; cannot be used at the same time.

POSW If set, writes to the .i.POS register; are enabled. (It is almost certainly a mistake to set this bit without having interrupts disabled.)

BTOE Enables the slot-0 .i.bus timeout; timer. This is used by the BIOS.

WDTR If 1, expiration of the .i.watchdog timer; generates a .i.reset; of the EPC-2. If 0, only the WDT event is signalled.
FWDT Fast .i.watchdog timer;. If clear, the period of the watchdog timer is about 6.7 seconds. If set, the period is about 210 ms.
A read of the MSC register also has a side effect of resetting the watchdog timer. Therefore, if you are using the watchdog timer, the intention is that you are required to read this register within the defined period of the timer to prevent its generating an interrupt.
.i.Signal Register FIFO; (.i.SRF;)

815E

815F
If the signal register FIFO is not empty, a read of these registers returns the oldest value in the FIFO. The value is removed from the FIFO upon reading of the "lower" byte (port 815E). If the FIFO is empty, the value returned is not specified.
Register State after Reset
A .i.hardware reset; of the EPC-2 (not a keyboard CTRL+ALT+DEL reset) clears all of the register bits to 0 (except those defined as a constant 1). The EPC-2's BIOS, however, initializes some of the registers based on information from the setup screen and elsewhere. The BIOS clears the .i.BIE; and .i.BEE; interrupt and event enable registers.
POS Register
The EPC-2 contains a .i.nonvolatile option register;, or .i.POS register;, containing information maintained by the BIOS. The information includes the .i.slot 0; enable, bus .i.arbitration priority;, .i.bus release mode;, .i.monitor type;, .i.arbitration mode;, DRAM size, .i.external clock; enable, and parallel port mode. Since the POS register is closely allied with correct operation of the BIOS, it is not user programmable; thus programming information is not provided in this manual.
VMEbus Accesses
Two C-language examples are given here for performing .i.VMEbus accesses; (accesses to the VXI .i.data transfer bus;) through the .i.E page;. The first performs a 16-bit read from the VMEbus A16 space. It requires setting the .i.address modifier;, relocating the A16 address into the E page (address range E0000-EFFFF), and then accessing the value pointed to by a C pointer variable.

```
#define WORD  unsigned short
#define LWORD unsigned long

WORD addr;   /* 16-bit A16 address */
WORD data;
WORD far * wptr;

outp(0x8130,0);  /* Set up E page as one contiguous region */
outp(0x8132,1);
outp(0x8134,2);
outp(0x8136,3);
outp(0x8151,0x0A);  /* Set address modifier to A16 supervisory access */
wptr = (WORD far *) (0xE0000000L + addr);
data = *wptr;       /* Read through window */
```

The next example does a byte write into the VMEbus .i.A32; space. Here the upper 16 bits of the VME address need to be stored in the appropriate registers.

```
LWORD addr;   /* 32-bit A32 address */
BYTE  data;
BYTE  far * wptr;


outp(0x8150,(WORD)(addr >> 24);           /* A31-A24 */
outp(0x8151,2 | (((addr << 8) >> 30) << 6));
  /* A23-A22 and address modifier for A32 supervisory data access */
outp(0x8130,(WORD)((addr << 10) >> 24);  /* A21-A14 */
wptr = (BYTE far *) (0xE0000000L + (addr & 0X00003FFFL));
*wptr = data;                            /* Write through window */
```

The success of the access can be checked either by enabling .i.BERR; as an interrupt or by looking at the BERR bit in the event state register after each access. Since writes are pipelined, software that looks at the BERR bit should first wait until the BSAM bit is set..i.pipelined write;.i.VMEbus write;

It is recommended that rather than performing accesses in this low-level hardware dependent form, the .i.Bus Manager; component of the EPConnect software package be used instead.

The following summarizes the source of the VMEbus address lines for accesses through the E page.

.i.A32;

```
31             24 23  22 21             14 13                          0
      From        From     From                   From
      port        port     port                 386 address
      8150        8151     8130/2/4/6            bits 13-0
```

.i.A24;

```
                  23  22 21             14 13                          0
From     From                    From
port     port                  386 address
8151     8130/2/4/6             bits 13-0
```

.i.A16;

```
                                    15 14 13                          0
From          From
port        386 address
813x         bits 13-0
```

Direct VMEbus Accesses

.i.data-transfer bus accesses;As described at the beginning of the chapter, an alternate way to perform .i.VMEbus accesses;, providing that one is in a 32-bit operating-system environment, is performing reads and writes at 386 addresses between 02000000h and FEFFFFFFh. These are directly mapped to the data-transfer bus with the same address, with an .i.address modifier; specifying .i.A32; supervisory data, and with .i.little endian; byte order..

Byte Ordering

.i.byte ordering;There are two fundamentally different ways of storing numerical values in byte locations in memory:

ù .i.Little endian;, characteristic of Intel microprocessors, where the least-significant data byte is stored in the lowest byte address

ù .i.Big endian;, characteristic of Motorola microprocessors and the VMEbus environment in general, where the most-significant data byte is stored in the lowest byte address.

To understand the difference and the potential problems, assume an Intel processor and a Motorola processor coexist in a shared memory environment. If the Motorola processor stored the 16-bit value 0102h in memory and the Intel processor fetched it, the Intel processor would interpret its numerical value as 0201h. If the Intel processor stored the 32-bit value 01020304h, the Motorola processor would fetch it as the number 04030201h.

The EPC-2 contains byte ordering hardware to allow programs to view VMEbus memory in either byte order. The order is selected by bit BORD in the .i.VME modifier register;.

When .i.little endian; is selected, bytes pass straight through from the 386's "byte lanes" to the VMEbus byte lanes (or vice versa on a read). That is, data lines 0-7 on the 386 connect to data lines 0-7 on the VMEbus (also called VME BYTE(0)), 8-15 to 8-15, 16-23 to 16-23, and 24-31 to 24-31.

When .i.big endian; is selected, the bytes are swapped between the 386 and VME. For a D16 access, 386 data lines 0-7 connect to data lines 8-15 on VME, and 386 data lines 8-15 connect to 0-7 on VME. For D32 accesses, the "outer two" and "inner two" bytes are swapped (i.e., 386 data lines 0-7 connect to VME data lines 24-31, 8-15 to 16-23, 16-23 to 8-15, and 24-31 to 0-7).

Byte swapping applies only to EPC-2 initiated (master) accesses; it does not apply to .i.slave; accesses (accesses from other VMEbus masters to the EPC-2's DRAM).

The EPConnect .i.Bus Manager; software provides functions for swapping byte ordering during memory-copy operations.

Read-Modify-Write Operations

.i.RMW cycle;Read-modify-write cycle;VXIbus RMW (read-modify-write) cycles can be performed through use of the 386's .i.LOCK instruction prefix; with certain instructions. All of these instructions perform a read followed by a write. When such a read occurs that is mapped to the VXIbus, the EPC-2 treats it as the start of a VXI RMW cycle. The next VME access from the 386 is treated as the write that terminates the RMW cycle. For this reason, RMW accesses that cross a 32-bit boundary will not behave as expected (because the 386 issues two read accesses).

Slave Accesses from the VMEbus

.i.slave;When SLE in the status/control register is set, the EPC-2 will respond to accesses in a 16 MB range of the A32 space. All types of VME accesses (reads, writes, and read-modify-writes of all lengths) are supported, except for .i.block transfer cycles;. The .i.address modifier; can specify supervisory, nonprivileged, program, or data.

When such an access is fielded by the EPC-2, the EPC-2's A24 or A32 base address is effectively subtracted from the VMEbus address value, and the result is treated, with several exceptions, as if the access came from the 386. The mapping of VXI slave-access addresses to addresses as seen by the 386 is shown in the following table.

VXI address range		Mapped to this local address in the EPC-2	
zz000000	zz09FFFF	00000000	0009FFFF
zz0A0000	zz0BFFFF	00100000	0011FFFF
zz0C0000	zz0CFFFF	000C0000	000CFFFF
zz0D0000	zz0EFFFF	00120000	0013FFFF
zz0F0000	zz0FFFFF	000F0000	000FFFFF
zz100000	zz13FFFF	hidden memory	
zz140000	zzFDFFFF	00140000	00FDFFFF

The .i.hidden memory; is DRAM in the EPC-2 that, because of the memory mapping, is accessible by VXI slave accesses but is not directly accessible from the 386. Also, note that slave accesses can reach two areas that are write-protected from the 386. These areas are not write-protected from slave accesses.

Self Accesses Across the VMEbus

.i.self accesses;Since the EPC-2's DRAM can be mapped into the VXI A32 address space, the EPC-2 can access its DRAM in an alternate way: by generating VXI accesses to the appropriate addresses. This can be of use in multiple-processor systems where some of the EPC-2's DRAM is used as shared global memory; it means

that the EPC-2 can access the global memory with the same addresses as used by other processors without needing to understand that the memory is actually on-board.

This ability is also useful in system checkout (i.e., checking operation of the backplane) and in giving an EPC-2 program the ability to view its memory in .i.big endian; format.

Read-Modify-Write Operations

.i.RMW cycle;Read-modify-write cycle;The EPC-2 provides synchronization integrity in its local DRAM between accesses from the 386 into the DRAM and RMW VXI accesses from other masters into the DRAM.

When a VXIbus slave read access occurs to the local DRAM, the EPC-2 watches the VXIbus data and address strobes to determine if the cycle is an RMW cycle. If it is, accesses by the 386 are held up until the terminating access of the RMW cycle occurs.

When the 386 performs a locked access (e.g., via an instruction using the .i.LOCK instruction prefix;) to the local DRAM, VXIbus read and RMW slave accesses are held up until the last locked access completes.

.i.self accesses;One more case of interest is when the EPC-2 performs a locked access that results in a self access. These function correctly (i.e., as if the access were not a self access), providing that operating-system tables (e.g., .i.page tables;) that are accessed by the 386 by implicit locked accesses are not mapped into VXI. This would only be a concern for user-written operating systems.

VXIbus Interrupt Acknowledgement

When it asserts an interrupt, the EPC-2 formulates a .i.status/ID; value that is transmitted on the bus as the response to a matching .i.interrupt acknowledge;ment cycle. The EPC-2 acts as a D16 interrupter. The lower eight bits of the status/ID value are the EPC-2's ULA, and the source for the upper eight bits is specified by the IST bit in the .i.MSC; .i.module status/control register;.

ID Register (VID)

1	1	1	0	1	1	0	0	8140
1	0	0	1	1	1	1	1	8141

This register defines the EPC-2 as a message-based device that is mapped into the A16/A32 address spaces with the manufacturer being RadiSys Corporation (manufacturer code 4076).

Since the EPC-2 is a DC device (a device without a static ULA, but a ULA that can be assigned dynamically by the resource manager), an initial write into this register from the VXIbus assigns a ULA to the EPC-2.

Device Type Register (VDT)

1	1	1	1	1	1	1	1	8142
0	1	1	1	0	0	0	S	8143

This read-only register denotes that the EPC-2 responds to a 16 MB range in the A32 space and has a model code of 255 (S=0) or 511 (S=1). S is controlled by the SLOT 0 FUNCTIONS parameter on the BIOS setup screen. S=0 (model code 255) means that the EPC-2 is configured as a slot-0 controller.

Status/Control Register (VSC)

SRIE	POSR	SYSC	1	READY	PASS	NOSF	RSTP	8144
SLE	MODID	SYSR	1	1	1	1	1	8145

This register contains VXI specified bits and EPC-2 device-dependent bits.

SLE Slave enable. If set (1), the EPC-2 will respond to certain A32 accesses from the VXI data-transfer bus.

MODID If clear (0), it denotes that the EPC-2's MODID pin is being asserted.

1¾ « È
Q a a d e e MANUAL.STY
POSTSCRPf @ £0Ð┐Cx┘┌b a c µ┌EPC-2 HARDWARE REFERENCE

Page ┌

5. Theory of Operation

This chapter specifies other information about the operation of the EPC-2 that might be useful to the system designer.

Processor, Coprocessor, Memory

The processor is an Intel 80386. The optional .i.coprocessor; is an 80387. The 387 is a factory-installed option.

The processor board contains eight SIMM sockets. The factory-installed .i.DRAM options; are 2, 4, 8, and 16 MB. The DRAM has byte-wide .i.parity;.

ROM and ROM Shadowing

EPC-2 contains a 27011 page-mode EPROM. The .i.EPROM; is mapped into the top of the processor's 32-bit address space, and also just below the 16 MB boundary for PC/AT compatibility. Alternate pages of the EPROM are accessed by using the page register in the EPROM chip. The EPROM contains the PC BIOS, VGA BIOS, SCSI disk BIOS, selftest program, and the setup screen program.

.i.ROM shadowing;For best possible performance, the BIOS initialization software copies the ROM contents into DRAM (called shadowing). DRAM at addresses 0Fxxxxh holds all but the VGA BIOS. DRAM at addresses 0Cxxxxh holds the VGA BIOS (beginning at 0C0000h). The BIOS write-protects these areas of memory.

GPIB Controller

The .i.GPIB controller; in the EPC-2 is fully software compatible with the National Instruments GPIB-PCII interface card. Because it is built into the EPC-2, its configuration is static. Specifically, it uses interrupt IRQ5, DMA channel 1, and I/O base address 2B8.

Battery

The .i.battery; powers the .i.CMOS RAM; and .i.TOD clock; when system power is not present. In older versions of the EPC-2, the battery is mounted on the circuit board and is not user replaceable. In newer versions, the battery is mounted on a velcro strip and connected to the circuit board via two wires to a four-pin keyed header. This battery may be replaced in the field using RadiSys part number 07-0018. Do this in a static-free environment and avoid touching the circuit board.

Interrupts and DMA Channels

.i.interrupt mapping;The assignment of interrupts is shown in the following table:

NMI	DRAM parity error, I/O channel check
IRQ0	timer
IRQ1	keyboard
IRQ3	.i.COM2; serial port
IRQ4	.i.COM1; serial port
IRQ5	.i.GPIB controller;
IRQ6	.i.floppy disk controller;
IRQ7	.i.LPT1; parallel port
IRQ8	clock
IRQ9	.i.VGA controller;
IRQ10	VXI interrupt/event
IRQ11	unassigned
IRQ12	.i.SCSI controller; (revised EPC-2) unassigned (older EPC-2s)
IRQ13	coprocessor
IRQ14	.i.IDE; disk (revised EPC-2) SCSI controller (older EPC-2s)

IRQ15 unassigned
The assignment of .i.DMA channels; is shown in the following table.

0	unassigned
1	.i.GPIB controller;
2	.i.floppy disk controller;
3	.i.SCSI controller;
5	unassigned
6	unassigned
7	unassigned

Watchdog Timer
EPC-2 contains a continually running timer having a period of either about 0.2 or 6.7 seconds (software selectable). The .i.watchdog timer; event is generated whenever the period expires. This event may be enabled as a source of the IRQ10 interrupt, or as a hardware .i.reset;. The timer is reset to its maximum value by an I/O read of the .i.module status/control register;.
EXMbus
This section applies to only the EPC-2x.
A subset of the .i.EXMbus;, an I/O expansion bus, is provided at the rear of a front-panel slot in the EPC-2x. .i.EXMID signal;The EXMbus is very similar to the .i.PC/AT I/O bus;. In addition, it contains a signal -EXMID used for dynamic recognition and configuration of EXMs. EXMs respond to one or more I/O addresses in the range 100h - 107h only when their Ä.i.EXMID signal; is asserted. EXMs are required to return a unique EXM-type identification byte in response to a read from I/O address 100h. The .i.EXMID driver register; provides the means to assert the ÄEXMID signal.
In the EPC-2x, only 8-bit transfers are supported across the EXMbus and only interrupt IRQ3 is available.
Further information on the EXMbus, its connectors, and standards for building EXMs is available upon request.
VXIbus Interface
.i.VMEbus interface;.i.P1 connector;.i.J1 connector;.i.P2 connector;.i.J2 connector;The EPC-2 module connects to the VXIbus J1 and J2 connectors in the left of the two slots occupied by the EPC-2.
On the P1 connector, the EPC-2 uses all of the defined VME/VXI lines except
SERCLK
SERDAT
+5V STDBY
On the P2 connector, the EPC-2 uses all of the defined VXIbus lines except
SUMBUS
LBUSC00-LBUSC11
RSV1,RSV2,RSV3
+24V,-24V
Slot 0 and System Controller Functions
When the EPC-2 is configured as the .i.slot 0 controller;, it performs the VXI slot-0 functions and the VME .i.system controller; functions.
The slot-0 functions consist of generation of the CLK10 signals and MODID support.
The VME system controller functions consist of serving as the .i.bus arbiter; (priority or round robin), driving the 16 MHz .i.SYSCLK; signal, starting the .i.IACK daisy chain;, and detecting and terminating .i.bus timeout;s. Once the EPC-2 sees either of the DS0 and DS1 lines asserted, a counter is started. If the counter expires before both DS0 and DS1 are deasserted, the EPC-2 asserts the VMEbus .i.BERR; signal until both data strobes are deasserted. The duration of the counter is approximately 100-120 microseconds.
Reset Behavior

Setting bit RSTP in the .i.VSC; .i.status/control register; puts the EPC-2 in the .i.soft reset state;. In this state the .i.RUN LED; is not illuminated, the screen is blank, and the .i.keyboard; and front-panel .i.reset switch; are inoperable. Only having another module clear RSTP or assert the VXI .i.SYSRESET; line, or doing a power off/on cycle (allowing 10 seconds or more in the off state to avoid damage to the disk drive) will remove the EPC-2 from this soft reset state.

Four conditions cause a full hardware reset of the EPC-2:

ù SYSRESET signal (when enabled in the .i.VSC; .i.status/control register;)
ù Front-panel reset switch
ù Expiration of the .i.watchdog timer; when bit WDTR in the .i.MSC; .i.module status/control register; is set
ù Power on

EPC-2AM Interface

The EPC-2AM is an optional one-slot adapter module that permits the addition of a standard .i.PCbus add-in card; to an EPC-2. The full complement of signals available in a standard 8-bit PC slot are not available, however. The signals available are listed below.

SD(0-7)
SA(0-19)
BALE
T/C
-IOR
-IOW
-SMEMR
-SMEMW
-IOCHK
IOCHRDY
REFRESH
CLK
OSC
-0WS
RESETDRV
AEN
IRQ3
IRQ4 (connected to EPC-2's IRQ7 in the revised
EPC-2 and IRQ12 in previous versions)
DRQ2 (connected to EPC-2's DRQ0)
-DACK2 (connected to EPC-2's -DACK0)
.i.DMA channels;The last three notes mean, for instance, that interrupt IRQ4 as seen by the PC card will actually be IRQ7 as seen by the EPC-2 software. The implication is that 8-bit PC cards that can be configured to use IRQ3 and no DMA channel will work without change, but use of the other interrupt or the DMA channel will probably require a change to the card's driver software.

Environmental and Electrical Specifications

.i.electromagnetic compatibility;.i.altitude;.i.humidity;.i.shock;.i.vibration.i.temperature;.i.operating temperature;.i.non-operating temperature;.i.cooling;.i.power consumption;The following represent an EPC-2 with 8 MB of memory and an 80387 coprocessor. They do not include the EXM module in an EPC-2x.

Characteristics	Specifications
Temperature	
Operating	5 to 55øC at point of entry of forced air
Non-operating	-40 to 60øC
Cooling	For 10øC rise, airflow of 2 liters per second against 0.014 mm H2O backpressure

Power
      +5V dc   8.4 A (max)
      +12V dc   0.7A (max, sustained)
            1.0A (for first 10 sec after power on, 40 MB or 100 MB drive)
            2.0A (for first 10 sec after power on, 200 MB drive)
      -12V dc   0.04 A (max)
      -5.2V dc   0.3A (max)
      -2V dc   0.12A (max)
Humidity   8 to 80%, non-condensing
Altitude
      Operating   3 km (10,000 ft)
      Non-operating   12 km (40,000 ft)
Shock
      Operating   Withstands 5 g's (1/2 sine), 11 ms duration
            without non-recoverable errors
      Non-operating   Withstands 70 g's (1/2 sine), 10 ms duration
Vibration
      Operating   Withstands 0.1" double amplitude, 5 to 27 Hz,
            0.5g's, 0-Pk, 28 to 500 Hz
      Nonoperating   Withstands 0.2" double amplitude, 5 to 62 Hz,
            4g's, 0-Pk, 63 to 500 Hz

6. Connectors

This chapter specifies the details of the connectors on the EPC-2. With one exception, the miniature parallel-port connector on the EPCÄ2x, all connectors are identical to the standard connectors on IBM PCs.

In the case of the EPC-2x, see the separate manual on the specific EXM for its connector definitions.

Pins are labelled from the point of view of looking into the front of the connector on the EPC-2.

.G.C:\MANUALS\DRAWINGS\COMCON.EPS;1.4";0.844";EPS

The DB-9 .i.COM1; and .i.COM2; .i.serial port; connectors are defined in the following table.

Pin	Signal	Pin	Signal
1	Carrier detect	6	Data set ready
2	Receive data	7	Request to send
3	Transmit data	8	Clear to send
4	Data terminal ready	9	Ring indicator
5	Signal ground		

.G.C:\MANUALS\DRAWINGS\LPTCONN.EPS;2.2";0.774";EPS

On the EPC-2 (not the EPC-2x) the DB-25 .i.LPT1; .i.parallel port; connector is defined as

Pin	Signal	Pin	Signal
1	Strobe	14	Auto line feed
2	DB0	15	Error
3	DB1	16	Initialize printer
4	DB2	17	Select in
5	DB3	18	Signal ground
6	DB4	19	Signal ground
7	DB5	20	Signal ground
8	DB6	21	Signal ground
9	DB7	22	Signal ground
10	Acknowledge	23	Signal ground
11	Busy	24	Signal ground
12	Paper end	25	Signal ground
13	Select		

.G.MINIPCON.EPS;1.2";0.631";EPS

On the EPC-2x, the .i.LPT1; .i.parallel port; connector is a miniature connector compatible with the 3M 10320 plug. The definition of this connector is shown below. Note that the .i.adapter cable; provided converts this connector into a standard DB-25 LPT1 connector as described above.

Pin	Signal	Pin	Signal
1	Strobe	14	Auto line feed
2	DB0	15	Error
3	DB1	16	Initialize printer
4	DB2	17	Select in
5	DB3	18	Signal ground
6	DB4	19	Signal ground
7	DB5	20	Signal ground
8	DB6		

9 DB7
10 Acknowledge
11 Busy
12 Paper end
13 Select

.G.C:\MANUALS\DRAWINGS\VGACONN.EPS;1.4";0.841";EPS
The DB-15 .i.monitor port; connector is defined as

Pin	Signal	Pin	Signal
1	Red	9	(key)
2	Green	10	Ground
3	Blue	11	P0 or unconnected
4	(not used)	12	P1 or unconnected
5	Ground	13	Horizontal sync
6	Ground	14	Vertical sync
7	Ground	15	F1 or unconnected
8	Ground		

.i.VGA connector;.i.flat-panel display;Three of the pins depend on whether the flat-panel .i.jumpers; are installed or not. If the three jumpers are not installed, pins 11, 12, and 15 are unconnected, as in a normal VGA connector. If the jumpers are installed, the three pins contain the following TTL output signals:
P0 Low-order bit (bit 0) of the digital video inputs to the EPC-2's .i.digital-to-analog converter; (.i.DAC;).
P1 Bit 1 of the digital video inputs to the EPC-2's DAC.
F1 Logical AND of DCLK and -BLANK, where DCLK is the .i.dot clock; to the DAC and -BLANK is the alternate blanking signal to the DAC. F1 is therefore a dot clock that is exactly 640 clocks per horizontal display line.
These three signals plus the horizontal and vertical sync signals needed for flat-panel displays are TTL outputs. F1 is driven from a 16V8 GAL and the other four are driven from a 74ALS244.
To use the .i.Fujitsu FPF8060;HRUK .i.plasma display;, a custom cable is needed making the following connections between the display and the EPC-2's VGA connector.
FPF8060HRUK

Plasma display		VGA connector	
Pin	Signal	Pin	Signal
1	VS	14	VS
3	HS	13	HS
4	GND	5	GND
15	D0	11	P0
16	GND	6	GND
17	D1	12	P1
18	GND	7	GND
19	DOTCLK	15	F1
20	GND	8	GND
21	BRIGHTNESS	to pin 25 on display (+5V)	

.i.monitor problems;If you are using a normal VGA .i.monitor;, you should not install the three flat-panel jumpers. Doing so could create fuzziness or synchronization problems with some types of VGA monitors.
.G.KB5CON.EPS;0.8";0.682";Postscript
The .i.keyboard connector; is defined as

Pin	Signal	Pin	Signal

1 Clock 4 ground
2 Data 5 +5V
3 not used

.G.GPIBCON.EPS;2";0.823";EPS

The GPIB port is a standard shielded IEEE-488 receptacle. The signals are shown below.

Pin	Signal	Pin	Signal
1	DIO1	13	DIO5
2	DIO2	14	DIO6
3	DIO3	15	DIO7
4	DIO4	16	DIO8
5	EOI	17	REN
6	DAV	18	GND
7	NRFD	19	GND
8	NDAC	20	GND
9	IFC	21	GND
10	SRQ	22	GND
11	ATN	23	GND
12	SHIELD	24	SIG GND

.G.EXTCKCON.EPS;0.3";0.3";EPS

An external 10 MHz clock can be supplied through a miniature SMB coax connector. The input impedance is 50 ohms. The signal must have TTL levels.

7. Error Messages

This chapter contains a summary of error and warning messages alphabetized by message text. These are messages generated by the BIOS and MS-DOS that may be related to your hardware configuration.

Bad partition table

.i.partition table;Your hard disk cannot be formatted because it has not yet been partitioned. Boot from a DOS floppy disk and run the FDISK program.

CMOS checksum invalid

Something in the nonvolatile .i.CMOS RAM; is incorrect. Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-2's .i.battery; has failed.

CMOS RAM error, check battery / run setup

Something in the nonvolatile CMOS RAM is incorrect. Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, first try reinitializing all CMOS RAM parameters. If the problem still occurs, the EPC-2's battery has failed.

.i.Disk boot failure;

No boot disk could be found. This could occur if your BIOS setup screen has all disks disabled, if your SCSI disk is disabled and no floppy diskette is inserted, if there is no operating system installed on the disk, or if the disk is inoperable.

Diskette drives or types mismatch error - run setup

.i.floppy diskette errors;The configuration information in the nonvolatile CMOS RAM does not match the floppy diskette installed in the system. Press CTRL+ALT+ESC to run the BIOS setup program. Drive A should be set to "1.4M" and drive B to NONE.

Error encountered initializing hard drive

Error initializing hard disk controller

.i.disk boot failure;.i.hard disk error;Either of these messages appears if the BIOS cannot boot from an AT (.i.IDE;) hard disk. Possible problems are that the BIOS setup information is incorrect, the disk is uninitialized, or the disk has failed.

Error: System requires a suitable video adapter

This is a Microsoft .i.Windows; error message. It can occur when software destroys DOS's unprotected information describing the video adapter. The problem can usually be corrected by entering the DOS command.i.mode command; mode co80

.i.EXM configuration error;

The EXM installed (or not installed) does not match the configuration information in the nonvolatile CMOS RAM. Hitting any key will allow you to continue, but doing so may cause problems later if software tries to use the EXM. To correct the problem, enter the setup program (via CTRL+ALT+ESC) to change the information on the setup screen and reboot.

General Failure error reading ...

.i.general failure;This almost always indicates the presence of an unformatted disk or diskette.

Invalid drive specification

You are trying to access a logical drive (e.g., A:, B:, ...) that is not known to the operating system.

Keyboard Error or no keyboard present

.i.keyboard errors;This message indicates that either (1) a .i.keyboard; is expected but none is present (check the integrity of the connector), (2) the

keyboard is not a valid PC/AT keyboard (e.g., it is a PC/XT-only keyboard), or (3) you pressed a key during the power-on selftest.

.i.Memory parity interrupt; at ...

This could be a software error (reading a nonexistent memory area) or a true hardware failure.

Non-system disk or disk error

.i.Non-system disk error;This is usually caused by an attempt to boot from a disk or diskette that is not formatted as a system disk. Most often it results when you reboot with a non-system diskette in the floppy drive, because the BIOS always attempts to boot from the floppy drive if a diskette is installed.

.i.Not ready error; reading drive ...

This is usually caused by not fully inserting a diskette into the floppy drive.

.i.Parity error; in segment ...

This could be a software error (reading a nonexistent memory area) or a true hardware failure.

.i.Real time clock error; - run setup

The battery-backed .i.TOD clock; is incorrect. Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-2's .i.battery; has failed.

8. Support and Service

If you have questions or problems, call 800-950-0044 between the hours of 8 AM and 5 PM Pacific time. Technical support is provided for users who purchased their system from RadiSys or a RadiSys sales representative; if you purchased your system elsewhere, you should contact that party for support.

Repair

Repair service under the standard warranty is provided to the original purchaser. Products returned for warranty repair that are found to be fully functional will be subject to a recertification fee. Typical turnaround time for repair and recertification is five working days (exclusive of shipping time).

Out-of-warranty service is subject to a service charge. After the damaged product is analyzed, the customer will be given a cost estimate and asked for authorization to proceed. All repairs are warranted for 90 days.

Shipping

Products requiring service may be returned to RadiSys, shipping prepaid, after issuance of a return materials authorization (RMA). Return authorization may be obtained by calling customer service (800-950-0044) with the product model, serial number, and problem description. Proper packaging, preferably the original shipping containers, should be used. Be sure to use anti-static and padded packaging, and to include a written description of the problem. The customer assumes all liability for loss or damage in transit in both directions. Unless otherwise agreed in advance, products will be returned to the customer with shipping and any repair charges due on delivery.

Ship the product needing service, freight prepaid, to:

Product Service Center
RadiSys Corporation
15025 S.W. Koll Parkway
Beaverton, OR 97006 USA

Other Services

Modifications to the warranty and repair services are available, including

- Overnight (express) shipment
- Quick-exchange programs (concurrent shipment of replacement and damaged unit)
- Extensions to the warranty period.

Index

1¾ « € - - -
0 1 1 MANUAL.STY POSTS
CRP2 @ £0Ð┐▯§┘┌. - / µ┌EPC-2 HARDWARE REFERENCE MANUAL
Page ┌
Page ┌
Ò

EPC - 2
Hardware Reference Manual

RadiSys Corporation
19545 NW Von Neumann Dr.
Beaverton OR 97006
Phone: 800-950-0044
In Oregon: (503) 690-1229

07-0013-02 December 1989

Hardware Warranty

RadiSys Corporation ("RadiSys") warrants the EPC system and component modules to the original purchaser for one year from the product's shipping date. If an EPC product fails to operate in compliance with its specification during this period, RadiSys will, at its option, repair or replace the product at no charge. The customer is, however, responsible for shipping the product; RadiSys assumes no responsibility for the product until it is received. This warranty does not cover repair of products that have been damaged by abuse, accident, disaster, misuse, or incorrect installation.

RadiSys' limited warranty covers products only as delivered. User modification, such as the addition of memory arrays or other devices, may void the warranty, and if the product is damaged during installation of the modifications, this warranty does not cover repair or replacement.

This warranty in no way warrants suitability of the product for any specific application.

IN NO EVENT WILL RADISYS BE LIABLE FOR ANY DAMAGES, INCLUDING LOST PROFITS, LOST SAVINGS, OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE PRODUCT EVEN IF RADISYS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, OR FOR ANY CLAIM BY ANY PARTY OTHER THAN THE PURCHASER.

THE ABOVE WARRANTY IS IN LIEU OF ANY AND ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED OR STATUTORY, INCLUDING THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR USE, TITLE AND NONINFRINGEMENT. Repair or replacement as provided above shall be the Purchaser's sole and exclusive remedy and RadiSys' exclusive liability for any breach of warranty.

Table of Contents

December 1989