AT91EB42
Evaluation Board

User Guide

Table of Contents

Section 1
Overview

1.1 Scope

The AT91EB42 Evaluation Board enables real-time code development and evaluation. It supports the AT91M42800.

This guide focuses on the AT91EB42 Evaluation Board as an evaluation and demonstration platform:

- Section 1 provides an overview.
- Section 2 describes how to set up the evaluation board.
- Section 3 details the on-board software.
- Section 4 contains a description of the circuit board.
- Section 5 and Section 6 are two appendices covering configuration straps and schematics, including pin connectors.

1.2 Deliverables

The evaluation board is delivered with a DB9 plug-to-DB9 socket straight-through serial cable to connect the target evaluation board to a PC. A bare power lead with a 2.1 mm jack on one end for connection to a bench power supply is also delivered.

The evaluation board is also delivered with a CD-ROM that contains an evaluation version of the software development toolkit and the documentation that outlines the AT91 microcontroller family.

The evaluation board is capable of supporting different kinds of debugging systems, using an ICE interface or the on-board Angel Debug Monitor. Refer to the AT91EB42 Getting Started Tutorial documents for recommendations on using the evaluation board in a full debug environment.

1.3 The AT91EB42 Evaluation Board

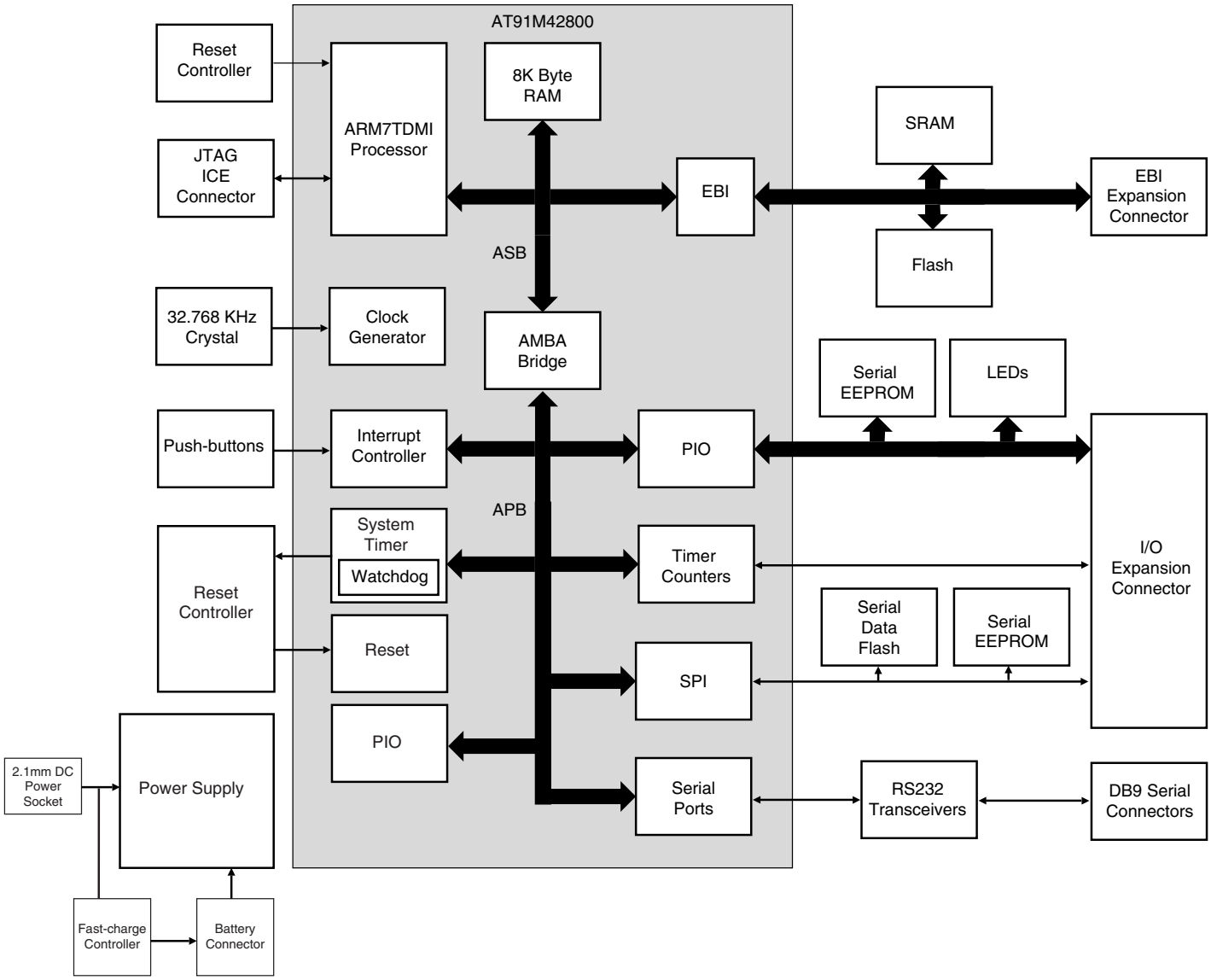
The board consists of an AT91M42800 together with several peripherals:

- Two serial ports
- Reset push button
- Four user-defined push buttons
- Eight LEDs
- a 256 KB 16-bit SRAM (upgradeable to 1M byte)
- a 2 MB 16-bit Flash (of which 1M byte is available for user software)
- a 4 MB Serial Data Flash
- a 64 KB Serial EEPROM
- a 32 KB SPI EEPROM

- 2 x 32-pin EBI expansion connectors
- 2 x 32-pin I/O expansion connectors
- 20-pin JTAG interface connector

If required, user-defined peripherals can also be added to the board. See Section 5 for details.

Figure 1-1. AT91EB42 Evaluation Board Block Diagram



Section 2

Setting Up the AT91EB42 Evaluation Board

2.1 Electrostatic Warning

The AT91EB42 Evaluation Board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

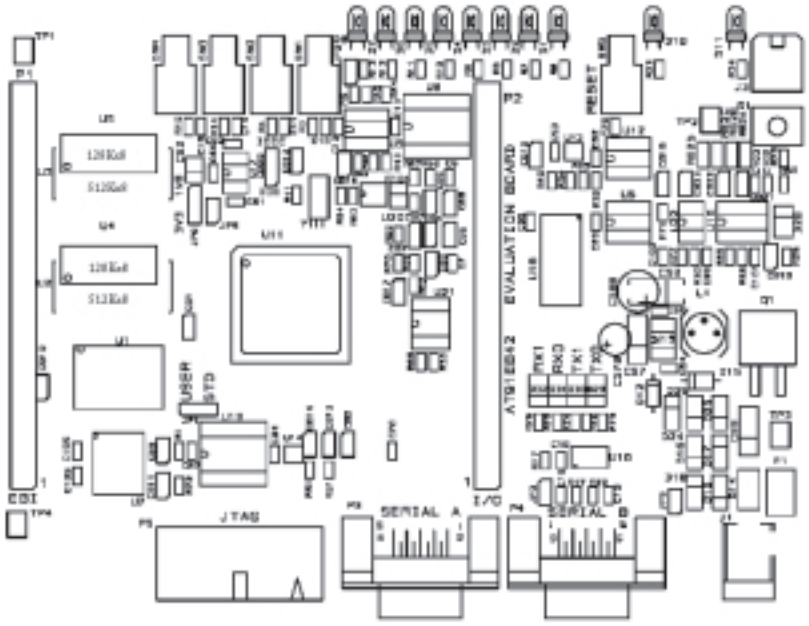
Requirements in order to set up the AT91EB42 Evaluation Board are:

- The AT91EB42 Evaluation Board itself
- The DC power supply capable of supplying 7.5V to 9V at 1A (not supplied)

2.3 Layout

Figure 2-1 shows the layout of the AT91EB42 Evaluation Board.

Figure 2-1. Layout of the AT91EB42 Evaluation Board



2.4 Jumper Settings

JP1 is used to boot standard or user programs. For standard operations, set it in the STD position.

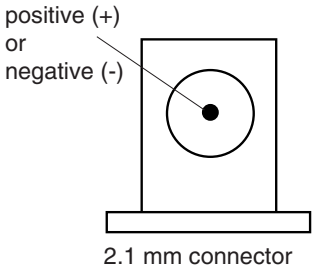
JP8 is used to select the core power supply of the AT91M42800: 3.3V or 1.8V. For operation at 1.8V, MCK frequency shall be limited to 17 MHz.

For more information about jumpers and other straps, see Section 5.

2.5 Powering Up the Board

DC power is supplied to the board via the 2.1 mm socket (J1) shown in Figure 2-2. The polarity of the power supply is not critical. The minimum voltage required is 7V.

Figure 2-2. 2.1 mm Socket



A battery power supply can be connected to the board via the J3 connector. A battery fast-charge controller is provided on-board to charge this battery.

The board has a voltage regulator providing +3.3V. The regulator allows the input voltage to range from 7V to 9V. When you switch the power on, the red LED marked POWER lights up. If it does not, switch off and check the power supply connections.

2.6 Measuring Current Consumption on the AT91M42800

The board is designed to generate the power for the AT91 product, and only the AT91 product, through the jumper JP5 (V_{DDIO}) and JP8 (V_{DDCORE}). This feature enables measurements to be made of the current consumption of the AT91 product.

See Section 5 for further details.

2.7 Testing the AT91EB42 Evaluation Board

To test the AT91EB42 Evaluation Board, perform the following steps:

1. Hold down the SW1 button and power-up the board, or generate a reset and wait for the light sequence on each LED to complete. All the LEDs light once and the LED D1 remains lit.
2. Release the SW1 button. The LEDs D1 to D7 light up one after the other. If any of the LEDs lights up twice, there is an error.

The LEDs represent the following components:

- D1 for the internal RAM
- D2 for the external RAM
- D3 for the external Flash
- D4 for the serial EEPROM
- D5 for the SPI DataFlash®
- D6 for the EEPROM
- D7 for the USART
- D8 is reserved

If a test is not carried out, the corresponding LED remains unlit and the test sequence restarts.

Section 3

The On-board Software

3.1 AT91EB42 Evaluation Board

The AT91EB42 Evaluation Board embeds an AT49BV1604 Flash memory device programmed with default software. Only the lowest 8 x 8 KB sectors are used. The remaining sectors are user definable, and can be programmed using one of the Flash downloader solutions offered in the AT91 library.

When delivered, the Flash memory device contains:

- the boot program
- the functional test software
- the SRAM downloader
- the Angel Debug Monitor
- a default user boot with a default application

The boot program, functional test software (FTS) and SRAM downloader are in sector 0 of the Flash. This sector is locked to prevent accidental erase, but it can be unlocked by applying 12V to the RESET pin.

3.2 Boot Software Program

The boot software program configures the AT91M42800, and thus controls the memory and other board components.

The boot software program is started at reset if JP1 is in the STD position. If JP1 is in the USER position, the AT91M42800 boots from address 0x01010000 in the Flash, which must have a user-defined boot.

The boot software program first initializes the EBI, then executes the REMAP procedure, and then checks the state of the buttons.

- When the button SW1 is pressed:

  All the LEDs light up together.

  The D1 LED remains lit until SW1 is released.

  The functional test software (FTS) is started.

- When the button SW2 is pressed:

  All the LEDs light up together.

  The D2 LED remains lit until SW2 is released.

  The SRAM downloader is activated.

- When SW3 or SW4 are pressed or no buttons are pressed:

  Branch at address 0x0100 2000.

  The Angel Debug Monitor starts from this address by recopying itself in external SRAM.

3.3 Programmed Default Memory Mapping

Table 3-1 defines the mapping defined by the boot program.

Table 3-1. Memory Map

Part Name	Start Address	End Address	Size	Device
U1	0x01000000	0x011FFFFF	2M Bytes	Flash AT49BV1604
U2-U3	0x02000000	0x02040000	256K Bytes	SRAM

The boot software program, FTS and SRAM downloader are in sectors 1 and 2 of the Flash device. Sectors 2 to 8 support the Angel Debug Monitor.

Sector 24 at address 0x0110 0000 must be programmed with a boot sequence to be debugged. This sector can be mapped at address 0x0100 0000 (or 0x0 after a reset) when the jumper JP1 is in the USER position.

3.4 SRAM Downloader

The SRAM downloader allows an application to be loaded in the SRAM at the address 0x02000000, then activated. It is started by the boot if the SW2 button is pressed at reset.

The procedure is as follows:

1. Connect the AT91EB42 Evaluation Board to the host PC serial “A” connection using the straight serial cable provided.
2. Power-on or press “RESET”, holding down the SW2 button at the same time. Wait for D2 to light up and then release SW2.
3. Start the BINCOM utility, available in the AT91 library, on the host computer:

   Select the port for communications (COM1 or COM2, depending on where you connected the serial cable on the host PC) and the baud rate for communications (115200 bds, 1 stop bit, no parity).

   Open the file to be downloaded and send it. Wait for the end of the transfer.
4. Press any button to end the download. The control is switched to the address 0x02000000.

3.5 Angel Monitor

The Angel monitor is located in the Flash from 0x01002000 up to 0x0100FFFF. The boot program starts it if no button is pressed at reset.

When Angel starts, it recopies itself in SRAM in order to run faster. The SRAM used by Angel is from 0x02020000 to 0x02040000, i.e., the highest half part of the SRAM.

The Angel on the AT91EB42 Evaluation Board can be upgraded regardless of the version programmed on it.

Note that if the debugger is started through ICE while the Angel monitor is on, the Advanced Interrupt Controller (AIC) and the USART channel are enabled.

3.6 Programmed Default Speed

As the speed of the AT91M42800 is programmable, the boot software program initializes the device to run as fast as possible, i.e., at 40 MHz. The boot software program and the functional test software are run at this speed. The SRAM downloader, after initialization of the USARTs, enters the processor in idle mode and activates the downloaded application at this speed. When Angel is started, it also runs at 40 MHz and the user should not modify this frequency without reprogramming the speed of the USARTs.

Section 4

Circuit Description

4.1 AT91M42800 Processor

Figure 6-1 on page 6-2 shows the AT91M42800. The footprint is for a 144-pin TQFP package.

Strap CB20 enables the user to choose between the standard ICE debug mode and the JTAG boundary scan mode of operation.

The operating mode is defined by the state of the JTAGSEL input detected at reset.

Jumper JP5 (see Figure 6-8 on page 6-9 in Section 6, “Appendix B – Schematics”) can be removed by the user to allow measurement of the current demand by the whole microcontroller (V_{DDIO} and V_{DDCORE}). Jumper JP8 can be removed to measure the core microcontroller consumption (V_{DDCORE}).

4.2 Expansion Connectors and JTAG Interface

The two expansion connectors, I/O expansion connector and EBI expansion connector, and the JTAG interface are described below.

The I/O and EBI expansion connectors’ pinout and position are compatible with the other evaluation boards (except the I/O expansion connector pinout and position of the EB40) so that users can connect their prototype daughter boards to any of these evaluation boards.

4.2.1 I/O Expansion Connector

The I/O expansion connector makes the general-purpose I/O (GPIO) lines, VCC3V3 and Ground, available to the user. Configuration straps CB2, CB3, CB4, CB11, CB13, CB14, CB15, CB17, CB18 and CB19 are used to select between the I/O lines being used by the evaluation board or by the user via the I/O expansion connector. The connector is not fitted at the factory; however, the user can fit any 32 x 2 connector on a 0.1" (2.54 mm) pitch.

4.2.2 EBI Expansion Connector

The schematic (Figure 6-4 on page 6-5 in Section 6, “Appendix B – Schematics”) also shows the bus expansion connector which, like the I/O expansion connector, is not fitted at the factory. The user can fit any 32 x 2 connector on a 0.1" (2.54 mm) pitch to gain access to the data, address, chip select, read/write, oscillator output and wait request pins. VCC3V3 and ground are also available on this connector.

Configuration strap CB1, when open, allows the user to connect the EBI expansion connector to the MPI expansion connector of an AT91EB63 evaluation board without any conflicts.

4.2.3 JTAG Interface

An ARM®-standard 20-pin box header (P5) is provided to enable connection of an ICE interface to the JTAG inputs on the AT91. This allows code to be developed on the board without using system resources such as memory and serial ports.

4.3 Memories

The schematic (Figure 6-3 on page 6-4 in Section 6, “Appendix B – Schematics”) shows one AT49BV1604 2 MB 16-bit Flash, one AT45DB321 4 MB serial DataFlash, one AT24C512 64 KB EEPROM, one AT25256 32 KB EEPROM and two 128K/512K x 8 SRAM devices.

Note: The AT91EB42 is fitted with two 128K x 8 SRAM devices.

A footprint is provided for the user to fit a multi-chip device memory that embeds Flash (1 MB) and SRAM (128 KB) in a single component in place of the Flash and SRAM devices (U7: M36W108AB from ST).

Strap JP1 shown on the schematic is used to select the part of 1 MB of the Flash to be accessed. This is to enable users to Flash download their application in the second part of the Flash and to boot on it.

4.4 Analog-to-digital Converter

A footprint is provided for the user to fit a 4-channel 10-bit ADC device (AD7817ARU from Analog Devices; see Figure 6-10 on page 6-11 in Section 6, “Appendix B – Schematics”). This device is interfaced to the AT91 microcontroller via the SPIA peripheral.

The voltage reference used is the 2.5V on-chip.

This device embeds a temperature sensor and is placed near the 32.768 KHz crystal quartz. Thus the user is able to take into account the frequency drift due to temperature evolution by a software program.

By default, two of the ADC channels are dedicated to supervise the board power supply voltage levels (channel 1 for the battery power supply, channel 2 for the standard power supply).

4.5 Power and Crystal Quartz

The AT91M42800 master clock is derived from a 32.768 KHz crystal quartz. The on-chip low-power oscillator together with two PLL-based frequency multipliers and the prescaler results in a programmable master clock between 500 Hz and 33 MHz.

Two sets of components for the PLL filters are fitted by default on the board (Figure 6-6 on page 6-7 in Section 6, "Appendix B - Schematics"). They are calculated to provide a 16.77 MHz (PLLA: multiplier factor of 512 and settling time of 600 µs) or a 33.55 MHz (PLLB: multiplier factor of 1024 and settling time of 4 ms) master clock frequency.

The voltage regulator provides 3.3V to the board and will light the red POWER LED (D11) when operating.

Power can be applied via the 2.1 mm connector to the regulator in either polarity because of the diode-rectifying circuit. Another regulator allows the user to power the AT91M42800 core with 3.3V or 1.8V by means of the JP8 jumper.

A battery power supply can be applied via the J3 connector. The type of battery and connections to be used are shown in the schematics (Figure 6-9 on page 6-10 in Section 6, "Appendix B - Schematics"). This type of battery will ensure the power supply of the board for approximately 30 minutes. A battery fast-charge controller is provided on-board to charge this battery. The number of series cells to be charged is set to 5, but can be changed via the CB21, CB22 and CB32 configuration straps. The maximum time allowed for fast-charging is set to 264 minutes.

4.6 Push Buttons, LEDs, Reset and Serial Interfaces

The IRQ0, TIOA0, PB6 and PB21 switches are debounced and buffered.

A supervisory circuit has been included in the design to detect and consequently reset the board when the 3.3V supply voltage drops below 3.0V. Note that this voltage can be changed depending on the board production series. The supervisory circuit also provides a debounced reset signal. This device can also generate the reset signal in case

of watchdog time-out as the pin NWDOVF of the AT91M42800 is connected to its input $\overline{MR}$.

The assertion of this reset signal will light up the red RESET LED (D10). By pressing the CLEAR RESET push button (S1), the LED can be turned off.

Another supervisory circuit initializes separately the microcontroller-embedded JTAG/ICE interface when the 3.3V supply voltage drops below 3.0V. Note that this voltage can be changed, depending on the board production series. These separated reset lines allow the user to reset the board without resetting the JTAG/ICE interface while debugging.

The schematic (Figure 6-5 on page 6-6 in Section 6, "Appendix B - Schematics") also shows eight general-purpose LEDs connected to port B PIO pins (PB8 to PB15).

Two 9-way D-type connectors (P3/4) are provided for serial port connection.

Serial port A (P3) is used primarily for host PC communication and is a DB9 female connector. TXD and RXD are swapped so that a straight-through cable can be used. CTS and RTS are connected together, as are DCD, DSR and DTR.

Serial port B (P4) is a DB9 male connector with TXD and RXD obeying the standard RS-232 pinout. Apart from TXD, RXD and ground, the other pins are not connected.

LEDs are connected to the TX and RX signals of both serial ports and show activity on these serial links.

A MAX3223 device (U10) and associated bulk storage capacitors provide RS-232 level conversion.

4.7 Layout Drawing

The layout diagram (Figure 6-1 on page 6-2 in Section 6, “Appendix B – Schematics”) shows an approximate floorplan for the board. This has been designed to give the lowest board area, while still providing access to all test points, jumpers and switches on the board.

The board is provided with four mounting holes, one at each corner, into which feet are attached. The board has two signal layers and two power planes.

Section 5

Appendix A – Configuration Straps

5.1 Configuration Straps (CB1 - 23, JP1 - 8)

By adding the I/O and EBI expansion connectors, users can connect their own peripherals to the evaluation board. These peripherals may require more I/O lines than available while the board is in its default state. Extra I/O lines can be made available by disabling some of the on-board peripherals or features. This is done using the configuration straps detailed below. Some of these straps present a default wire (notified by the default mention) that must be cut before soldering the strap.

CB1	On-board PB5/A23/CS4 Signal
Closed(1)	AT91 PB5/A23/CS4 signal is connected to the EBI expansion connector (P1-B21).
Open	AT91 PB5/A23/CS4 signal is not connected to the EBI expansion connector (P1-B21). This authorizes users to connect the EBI expansion connector of this board to the MPI expansion connector of an AT91EB63 Evaluation Board without conflict problems.

CB2, CB3, CB4	ADC Enabling
Closed(1)	ADC (U20) control lines enabled
Open	ADC (U20) control lines disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

CB5	Battery Power Supply Supervisory Enabling
Closed(1)	Battery power supply is supervised by the ADC (U20) channel 1 via a resistor bridge. The ratio is set to 0.3333 so that the battery voltage range can be supervised (5.5V to 6.2V).
Open	Battery power supply is not connected to the ADC (U20) channel 1. This authorizes users to connect the corresponding ADC channel to their own resources via the I/O expansion connector.

CB7	Standard Power Supply Supervisory Enabling
Closed[1]	Standard power supply is supervised by the ADC (U20) channel 2 via a resistor bridge. The ratio is set to 0.1485 so that the standard power supply can be supervised up to 15V.
Open	Standard power supply is not connected to the ADC (U20) channel 2. This authorizes users to connect the corresponding ADC channel to their own resources via the I/O expansion connector.

CB6, CB8	ADC Channels 3 and 4 Enabling
Closed [1]	ADC (U20) channels 3 and 4 are connected to ground.
Open	ADC (U20) channels 3 and 4 are not connected to ground. This authorizes users to connect the corresponding ADC channel to their own resources via the I/O expansion connector.

CB9	On-board Boot Chip Select
Closed [1]	AT91 NCS0 select signal is connected to the Flash memory.
Open	AT91 NCS0 select signal is not connected to the Flash memory. This authorizes users to connect the corresponding select signal to their own resources via the EBI expansion connector.

CB10	Flash Reset
Closed[1]	The on-board reset signal is connected to the Flash NRESET input.
Open	The on-board reset signal is not connected to the Flash NRESET input.

CB11	PB22 Ready/Busy MCM Memory Signal
Closed[1]	AT91 PB22 signal is connected to the multi-chip device memory (U7), Ready/Busy output pin
Open	AT91 PB22 signal is not connected to the multi-chip device memory (U7), Ready/Busy output pin. This authorizes users to connect the corresponding signal to their own resources via the I/O expansion connector

CB12	Boot Mode Strap Configuration
Open	BMS AT91 input pin is set for the microcontroller to boot on an external 16-bit memory at reset.
Closed[1]	BMS AT91 input pin is set for the microcontroller to boot on an external 8-bit memory at reset.

CB13, CB14	I^2C EEPROM Enabling
Closed[1]	EEPROM communication enabled
Open	EEPROM communication disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

CB15	Serial DataFlash Enabling
Closed(1)	AT91 NPCSA0 select signal is connected to the serial DataFlash memory.
Open	AT91 NPCSA0 select signal is not connected to the serial DataFlash memory. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

CB17	SPI EEPROM Enabling
Closed(1)	EEPROM communication enabled
Open	EEPROM communication disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

CB18	PB20 ADC Write Access Signal
Closed(1)	AT91 PB20 signal is used to control the RD/WR ADC (U20) input pin. Prior to a write access, position this PIO line in a low state. Position it in a high state prior to a read access.
Open	AT91 PB20 signal is not used to control the RD/WR ADC (U20) input pin. This authorizes users to connect the corresponding signal to their own resources via the I/O expansion connector.

CB19	PB18 End of Fast Charge Signal
Closed(1)	AT91 PB18 signal is connected to the battery charger (U16), NFASTCHG output pin.
Open	AT91 PB18 signal is not connected to the battery charger (U16), NFASTCHG output pin. This authorizes users to connect the corresponding signal to their own resources via the I/O expansion connector.

CB20	JTAGSEL
1-2(1)	AT91 standard ICE debug feature enabled
2-3	IEEE 1149.1 JTAG boundary scan feature enabled

CB21, CB22, CB23	Charger Device (U16): Programming the Battery Number of Cells		
Number of Cells	**CB21**	**CB22**	**CB23**
1	Open	Closed	Closed
2	Open	Open	Closed
4	Closed	Open	Closed
5(1)	Open	Closed	Open
6	Open	Open	Open
8	Closed	Open	Open

JP1	User or Standard Boot Selection
2-3	The first half part of the Flash memory is accessible at its base address.
1-2	The second half part of the Flash memory is accessible at its base address. This authorizes users to download their own application software in this part and to boot on it.

JP2	Push Button Enabling
Open	SW1-4 inputs to the AT91 are valid.
Closed	SW1-4 inputs to the AT91 are not valid. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

JP3	User or Standard Boot Selection
Open	The RS-232 transceivers are enabled.
Closed	The RS-232 transceivers are disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

JP8	Core Power Supply Selection
2-3	The AT91 core is powered by 3.3V power supply.
1-2	The AT91 core is powered by 1.8V power supply. In this case, the maximum frequency that can be used is 17 MHz.

Note: 1. Hardwired default position: To cancel this default configuration, cut the wire on the board.

5.2 Power Consumption Measurement Strap (JP5)

The JP5 strap enables connection of an ammeter to measure the AT91M42800 global consumption (V_{DDCORE} and V_{DDIO}) when V_{DDCORE} power supply is derived from V_{DDIO} (JP8 in 3V3 position). Core consumption can be measured by connecting another ammeter between JP8 1-2 or 2-3, depending on the power supply used to power the core.

The current measured on E11 is the total current required by the AT91M63200 on both V_{DDIO} and V_{DDPLL}. It is also the current consumed by the switching regulator VR1 that provides the 1.8V.

5.3 Ground Links (JP6)

The JP6 strap allows the user to connect the electrical and mechanical grounds.

5.4 Increasing Memory Size

The AT91EB42 Evaluation Board is supplied with two 128K x 8 byte SRAM memories. If, however, the user needs more than 256K bytes of memory, the devices can be replaced with two 512K x 8 3.3V 10/15 ns SRAMs, giving in total 1024K bytes.

Section 6

Appendix B – Schematics

6.1 Schematics

The following schematics are appended:

- Figure 6-1. PCB Layout
- Figure 6-2. AT91EB42 Blocks Overview
- Figure 6-3. EBI Memories
- Figure 6-4. I/O and EBI Expansion Connectors
- Figure 6-5. Push Buttons, LEDs and Serial Interface
- Figure 6-6. AT91M42800
- Figure 6-7. Reset and JTAG Interface
- Figure 6-8. Power Supply and Battery Charger
- Figure 6-9. Battery Type and Connection
- Figure 6-10. SPI Memories, I^2C Memories and SPI ADC

The pin connectors are indicated on the schematics:

- P1 = EBI Expansion Connector (Figure 6-4)
- P2 = I/O Expansion Connector (Figure 6-4)
- P3 = Serial A (Figure 6-5)
- P4 = Serial B (Figure 6-5)
- P5 = JTAG Interface (Figure 6-7)

Figure 6-1. PCB Layout

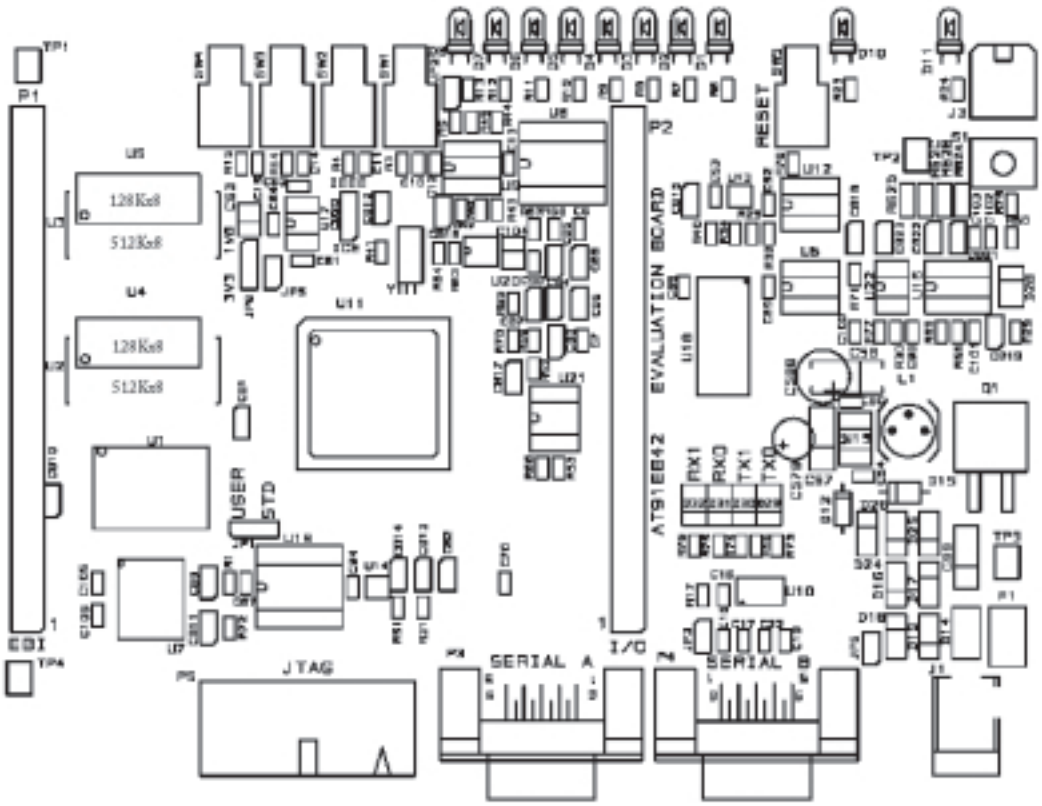


Figure 6-2. AT91EB42 Blocks Overview

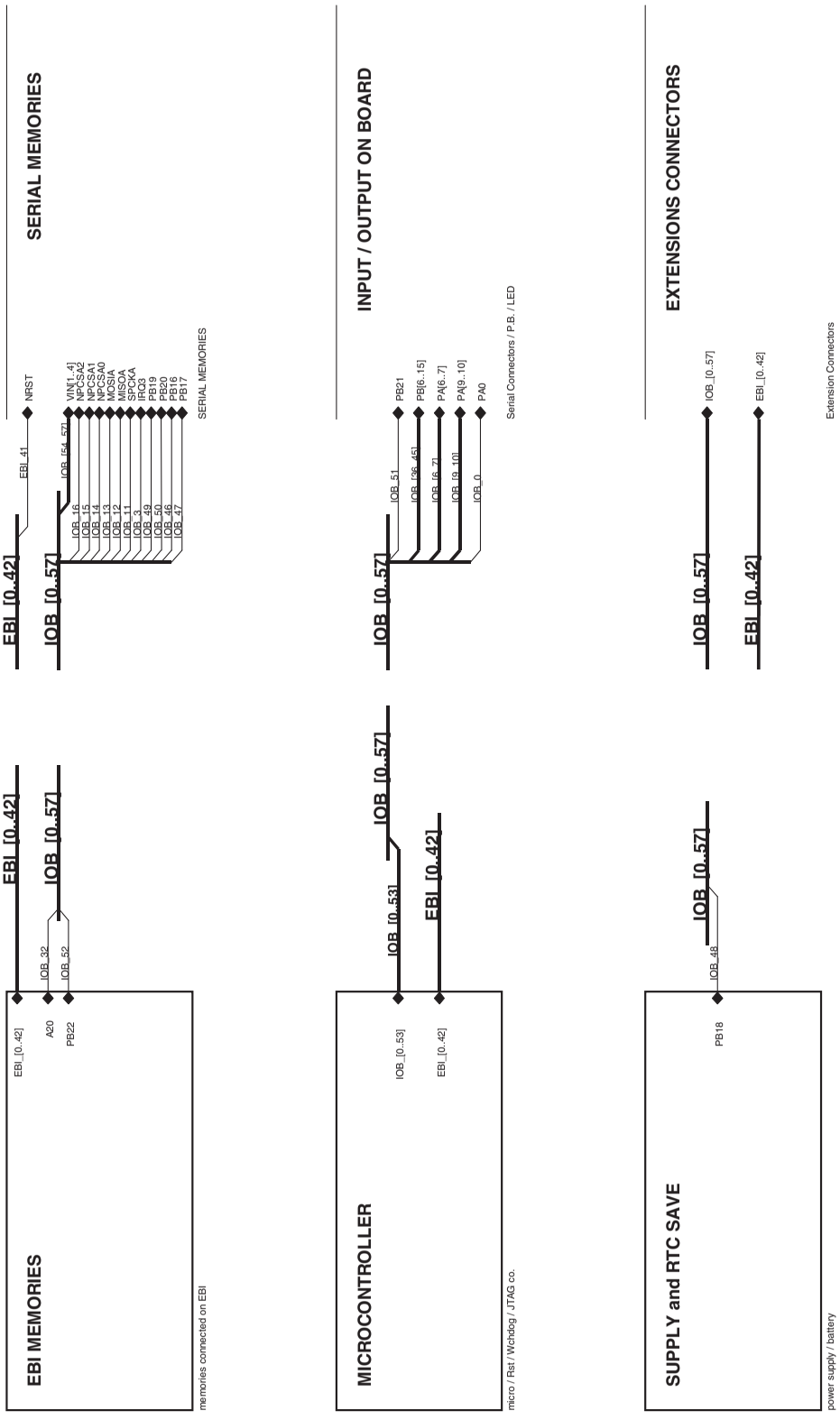


Figure 6-3. EBI Memories

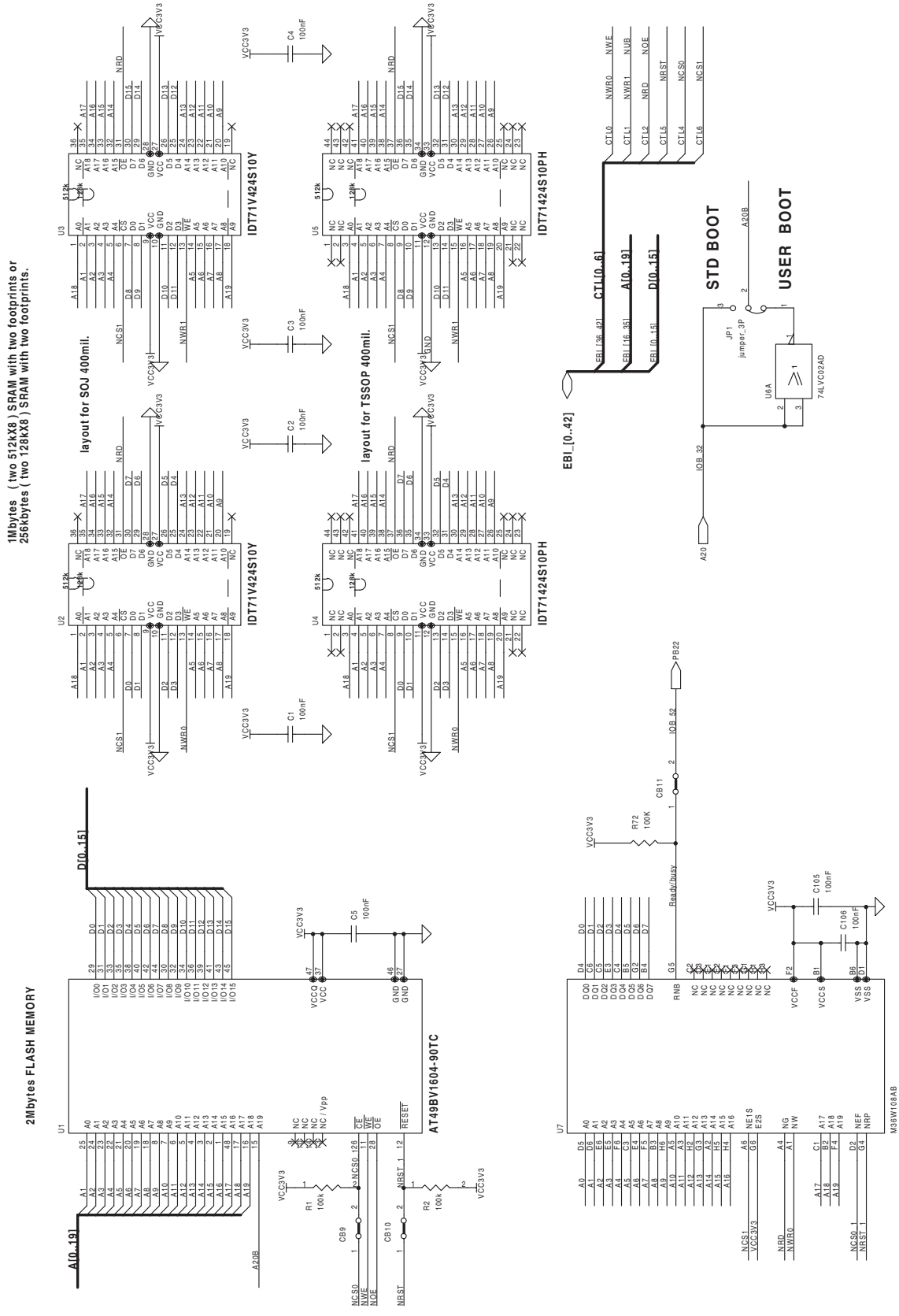


Figure 6-4. I/O and EBI Expansion Connectors

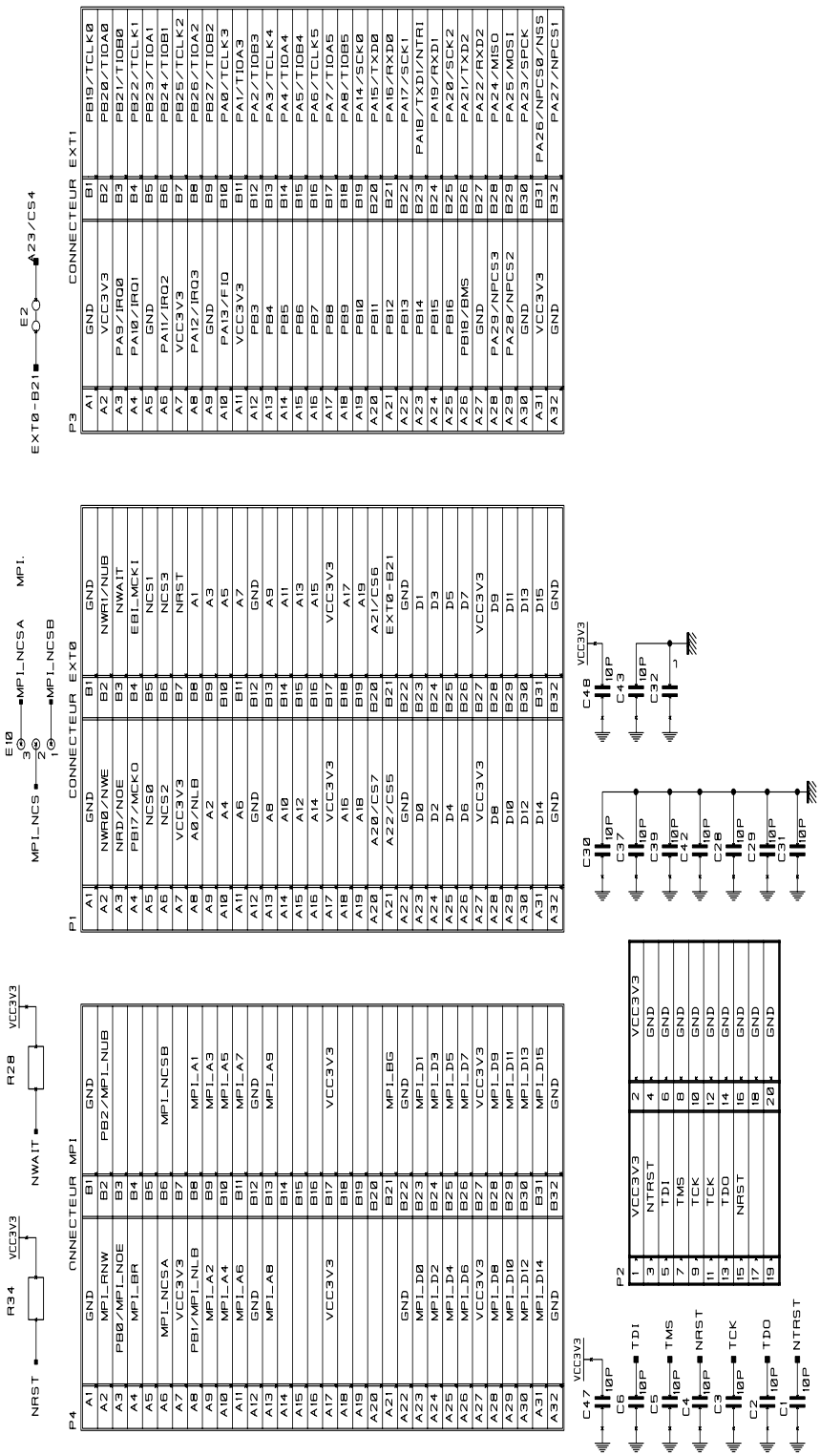


Figure 6-5. Push Buttons, LEDs and Serial Interface

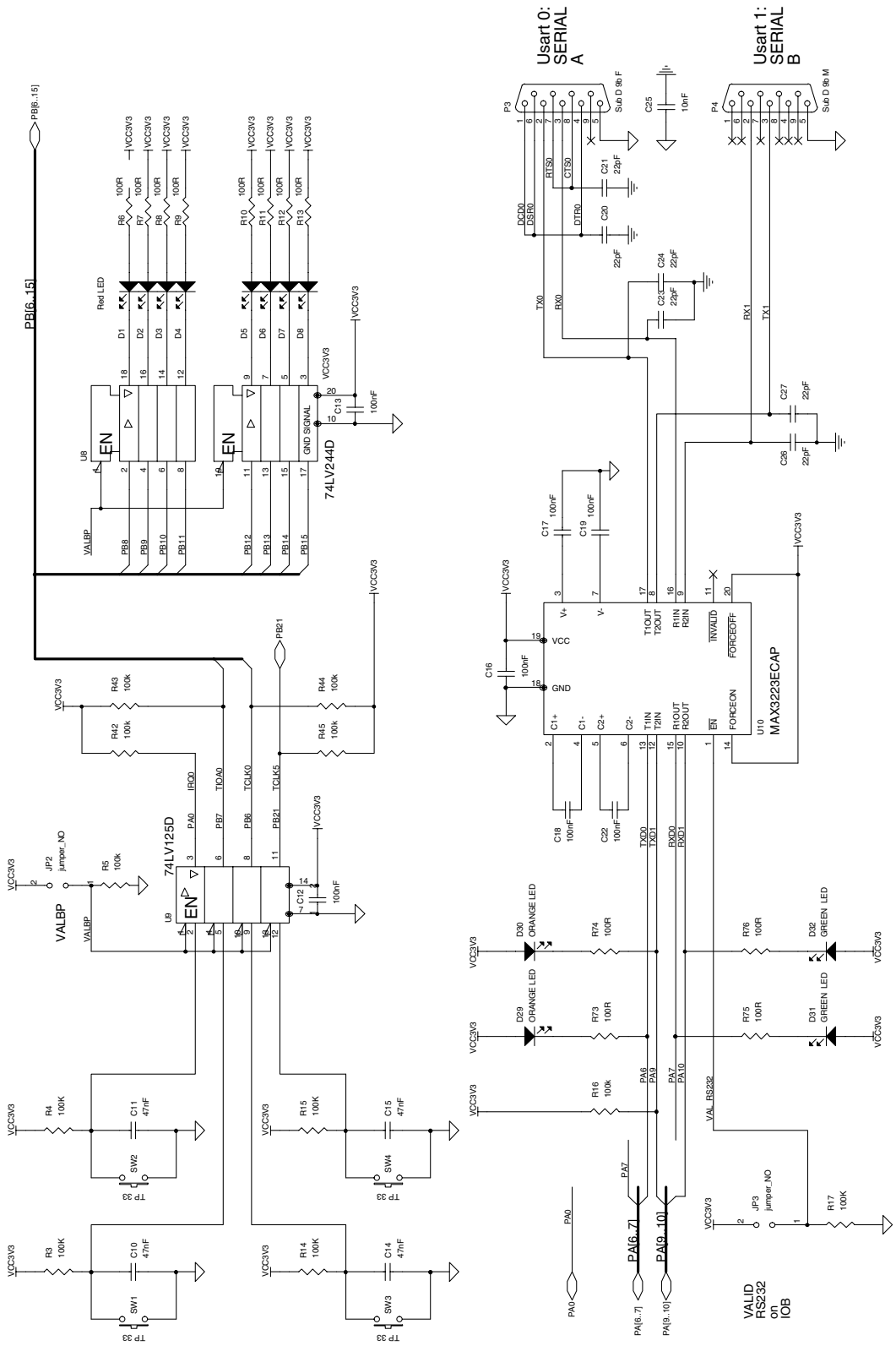


Figure 6-6. AT91M42800

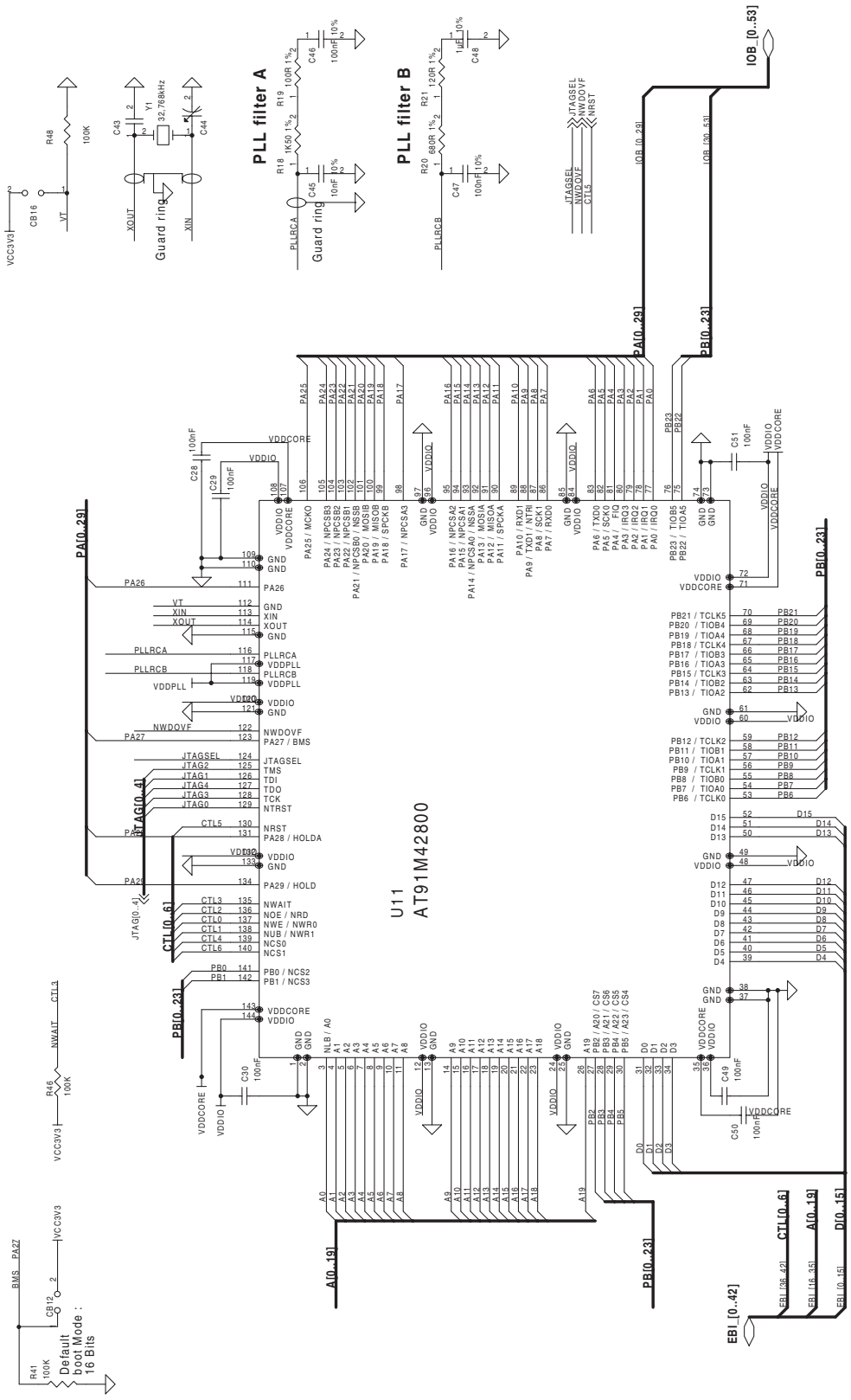


Figure 6-7. Reset and JTAG Interface

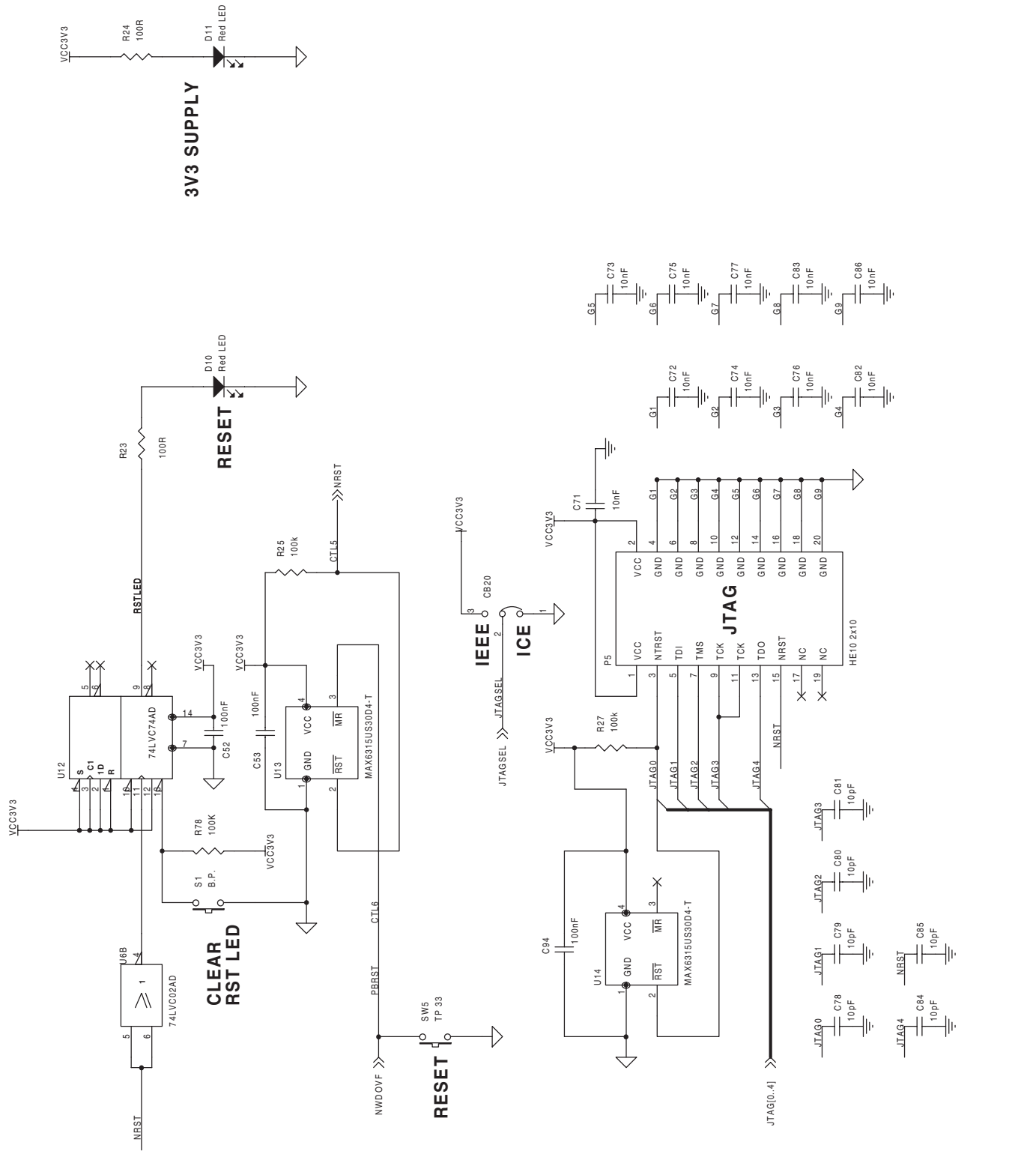


Figure 6-8. Power Supply and Battery Charger

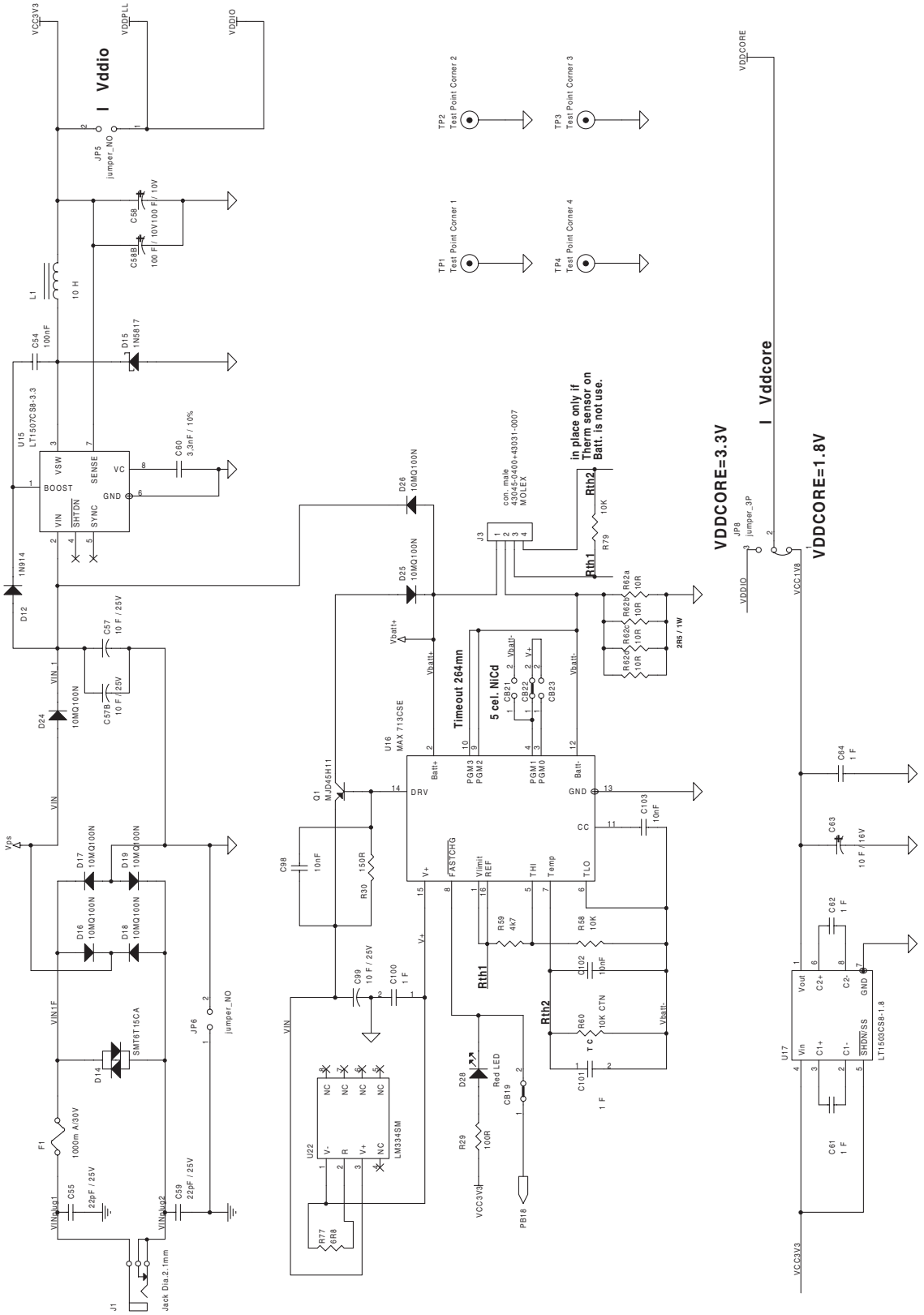


Figure 6-9. Battery Type and Connection

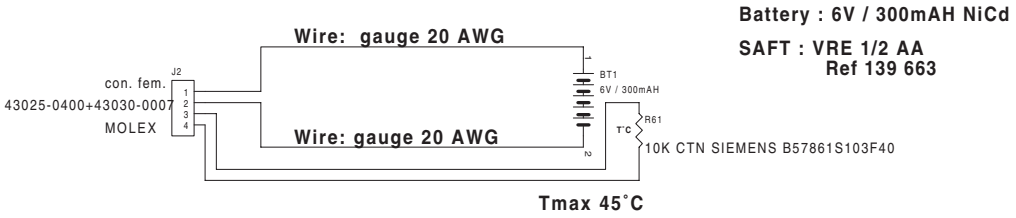
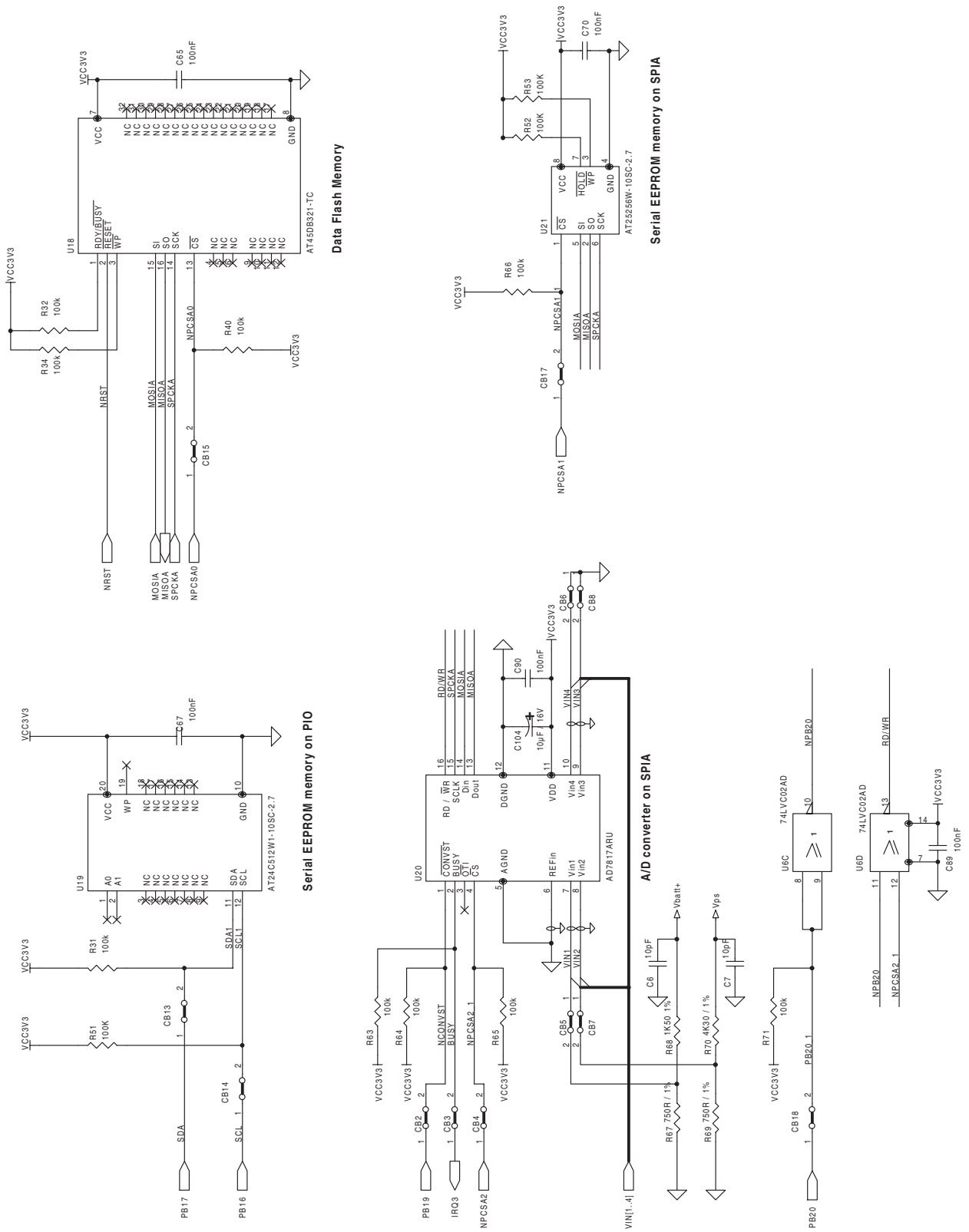


Figure 6-10. SPI Memories, I²C Memories and SPI ADC



Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

1708A–08/00/0M