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PS1000 User Guide

V1.2

Preliminary datasheet

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1. System Architecture

The PS1000 is an ASIC for the 1P3W (One-Phase, Three-Wire) Power Meter (Energy Meter) application. The PS1000 integrated all the function needs for energy meter application. The system architecture is shown in figure 1.

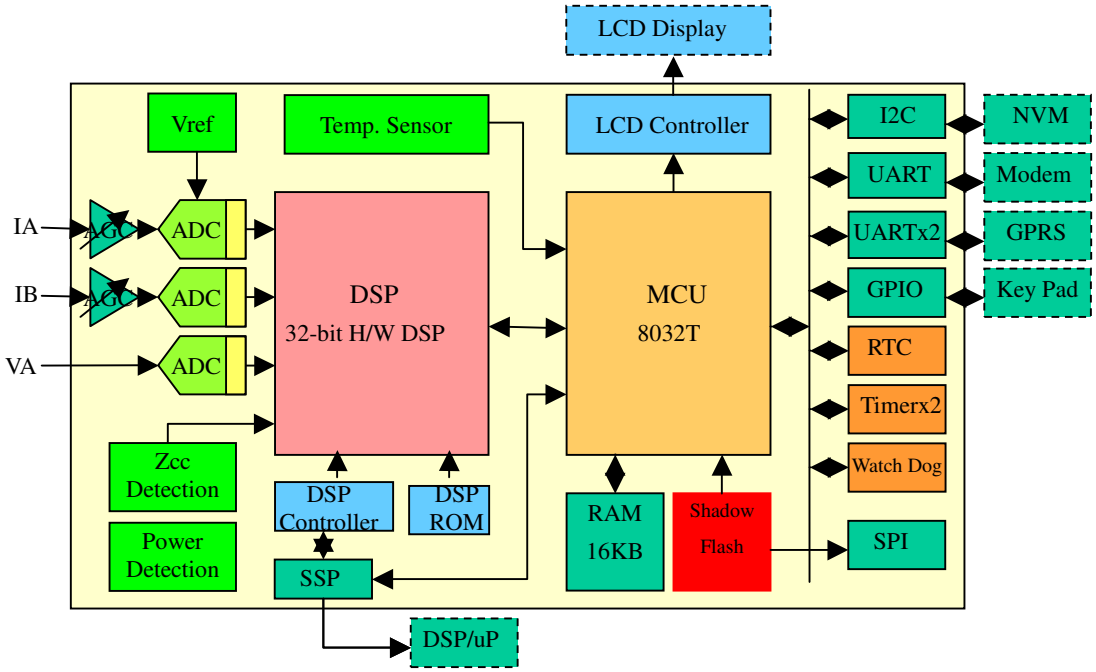


Figure 1. PS1000 System Architecture

PS1000 contains the following major subsystems

- 2 CH 16-bit ADC with AGC for current input(1x/2x/4x/8x)
- 1 CH 16-bit ADC for voltage input
- Built-in internal temperature sensor with 10-bit ADC
- Built-in 32-bit hardware DSP core (256x32 program space)
- 8032T high performance MCU
- 256B internal data memory space
- 16KB external data memory space
- 64KB program space
- Timer x 3 (including a Watch Dog Timer)
- UART x 3 (UART2/UART3 mapped to same timer)
- I2C interface
- TI DSP SSP interface
- SPI EEPROM interface
- 16 GPIO
- 40x4 LCD Controller/Driver
- 1/4 LCD Bias

The detail description for each block is described in each section.

PS1000 has several different package types. For the detail pin assignment, please reference the Section 14. The detail PIN description is shown in below.

Name	Type	Description
VCC3A	Power (3.3V)	3.3V Analog power supply
VCCIO	Power (3.3V)	3.3V I/O Power supply
VCCK	Power(2.5V)	2.5V Core power
VREG25	O	Regulator 2.5V output
VSSA	Ground	Analog Ground
GND	Ground	I/O, Digital Ground
VCCRTC	Power(2.5V)	RTC power supply (2.5V)
RTCXI	I	RTC crystal input (32.768K)
RTCXO	O	RTC crystal output
RTCGND	Ground	RTC Crystal ground
OSCVCC	Power(2.5V)	Crystal power supply (2.5V)
XTLI	I	System Crystal input (24MHz)

XTLO	O	System Crystal output
SCLK	I/O	SPI Clock input/output signal. The I/O selection depends on the SPI is in master or slave mode. In the master mode, the maximum clock rate is SYSCLK/4
SPICS	O	SPI CS control signal, active low
SO	O	SPI SO output
SI	I	SPI SI input
FSX	I/O	SSP transmit frame sync signal
DX	I/O	SSP transmit data signal
CLK	O	SSP CLK, the transmit and received clock. The maximum clock rate is SYSCLK/4
DR	O	SSP receive data signal
FSR	O	SSP receive frame sync signal
SCL	I/O	I2C clock
SDA	I/O	I2C Address/Data
VCM1	O	Current Phase A/B ADC reference output(VCC3A/2)
IBM	I	Phase B Current input(-)
IBP	I	Phase B Current input(+)
IAP	I	Phase A Current input(+)
IAM	I	Phase A Current input(-)
VAM	I	Voltage input(-)
VAP	I	Voltage input(+)
VCM2	O	Voltage ADC reference output(VCC3A/2)
VLCD	O	LCD bias power supply output
V1	I	LCD bias input 1
V2	I	LCD bias input 2
V3	I	LCD bias input 3
COM3~0	O	LCD COM output (maximum driving current 200uA)
SEG0~39	O	LCD Segment output (maximum driving current 20uA)
RST	I	Chip Reset, active high
EA	I	8051 MCU EA control signal 1: Internal ROM 0: External ROM
PSEN	I/O	8051 PSEN control pin
ALE	I/O	8051 ALE control signal
MODE2-0	I	Operation Mode selection 000 Normal Operation (1) 001 ICP Mode 010 External 51 Mode (1) 011 Normal Operation (2) 100 Memory Test Mode 101 External 51 Mode (2) 110 Analog Test Mode (Reserved) 111 Memory BIST Mode (Reserved)
P0.0	I/O	8051 P0 I/O port bit 0 (mapped to the AD0)
P0.1	I/O	8051 P0 I/O port bit 1 (mapped to the AD1)
P0.2	I/O	8051 P0 I/O port bit 2 (mapped to the AD2)
P0.3	I/O	8051 P0 I/O port bit 3 (mapped to the AD3)
P0.4	I/O	8051 P0 I/O port bit 4 (mapped to the AD4)
P0.5	I/O	8051 P0 I/O port bit 5 (mapped to the AD5)

P0.6	I/O	8051 P0 I/O port bit 6 (mapped to the AD6)
P0.7	I/O	8051 P0 I/O port bit 7 (mapped to the AD7)
P1.0(optional)	I/O	8051 P1 I/O port bit 0 (mapped to T2 interrupt input)
P1.1	I/O	8051 P1 I/O port bit 1 (mapped to T2EX interrupt input)
P1.2	I/O	8051 P1 I/O port bit 2 (mapped to RS-232 RxD1)
P1.3	I/O	8051 P1 I/O port bit 3 (mapped to RS-232 TxD1)
P1.4	I/O	8051 P1 I/O port bit 4 (mapped to RS-232 RxD2)
P1.5	I/O	8051 P1 I/O port bit 5 (mapped to RS-232 TxD2)
P1.6	I/O	8051 P1 I/O port bit 6 (mapped to ExtInt0 interrupt)
P1.7	I/O	8051 P1 I/O port bit 7 (mapped to ExtInt1 interrupt)
P2.0	I/O	8051 P2 I/O port bit 0 (mapped to the A8)
P2.1	I/O	8051 P2 I/O port bit 1 (mapped to the A9)
P2.2	I/O	8051 P2 I/O port bit 2 (mapped to the A10)
P2.3	I/O	8051 P2 I/O port bit 3 (mapped to the A11)
P2.4	I/O	8051 P2 I/O port bit 4 (mapped to the A12)
P2.5	I/O	8051 P2 I/O port bit 5 (mapped to the A13)
P2.6	I/O	8051 P2 I/O port bit 6 (mapped to the A14)
P2.7	I/O	8051 P2 I/O port bit 7 (mapped to the A15)
P3.0	I/O	8051 P3 I/O port bit 0 (mapped to RS-232 RxD0)
P3.1	I/O	8051 P3 I/O port bit 1 (mapped to RS-232 TxD2)
P3.2	I/O	8051 P3 I/O port bit 2 (mapped to INT0 interrupt input)
P3.3	I/O	8051 P3 I/O port bit 3 (mapped to INT1 interrupt input)
P3.4(optional)	I/O	8051 P3 I/O port bit 4 (mapped to T0 interrupt input)
P3.5(optional)	I/O	8051 P3 I/O port bit 5 (mapped to T1 interrupt input)
P3.6	I/O	8051 P3 I/O port bit 6 (mapped to memory WR_ control signal)
P3.7	I/O	8051 P3 I/O port bit 7 (mapped to memory RD_ control signal)

2. Mode Control

The PS1000 has several modes for different operation. The mode is controlled by the MODE and EA setting. Here is the configuration list.

Mode	EA	MCU	ROM	RAM	Notes
000	0	Internal	External Flash	XDATA+ I/O Memory	Normal Operation 1
000	1	Internal	Shadow RAM (Power On)	XDATA+ I/O Memory	Normal Operation 1
001	0	Internal	External Flash	Shadow RAM + I/O Memory	ICP Mode
001	1	Internal	Internal 2K ROM	Shadow RAM + I/O Memory	ICP Mode
010	x	External		Shadow RAM + I/O Memory	External 51 Mode 1
011	0	Internal	External Flash	XDATA+ I/O Memory	Normal Operation 2
011	1	Internal	Shadow RAM	XDATA+ I/O Memory	Normal Operation 2
100	x	External		Shadow + XData + I/O Memory	Memory Test Mode
101	x	External		I/O Memory	External 51 Mode 2
110	0	Non			Analog Test Mode 1
110	1	Non			Analog Test Mode 2
111	x	Non			Memory BIST

For the detail description for each mode, please reference the section 7 MCU.

3. Clock Setting

The operation frequency of some PS1000 internal function blocks, like the ADC, MCU, DSP and LCD can be adjusted depends on operation condition. It can be configured with some internal register. The next section will describe how to program these registers. When change these registers setting, please make sure that is matched with the system requirement.

3.1 MCU Clock Setting

The PS1000 can set the different MCU operation clock during the different operation condition. It also can help to save the power.

MCUCFG (0xFE29)							
B7	B6	B5	B4	B3	B2	B1	B0
PORTCFG	DSPTM[1:0]		DSPROM	MCUDIV[3:0]			

PORTCFG

0: P0/P2 normal operation

1: P0/P2 mapped to the P4/P5

DSPTM [1:0]

00: DSP normal operation

01: DSP Test Mode 1 (reserved)

10: DSP Test Mode 2 (reserved)

11: DSP Test Mode 3 (reserved)

DSPROM:

0: DSP Normal operation

1: Mapping DSPROM to the I/O memory space (0xF000 ~ 0xF3FF, 1KB)

MCUDIV: MCU clock Divider

MCUDIV[3:0]		22MHz	24MHz
0000	SCLK / 1	22.00	24.00
0001	SCLK / 2	11.00	12.00
0010	SCLK / 3	7.33	8.00
0011	SCLK / 4	5.50	6.00

0100	SCLK / 5	4.40	4.80
0101	SCLK / 6	3.67	4.00
0110	SCLK / 7	3.14	3.43
0111	SCLK / 8	2.75	3.00
1000	SCLK / 9	2.44	2.67
1001	SCLK / 10	2.20	2.40
1010	SCLK / 11	2.00	2.18
1011	SCLK / 12	1.83	2.00
1100	SCLK / 13	1.69	1.85
1101	SCLK / 14	1.57	1.71
1110	SCLK / 15	1.47	1.60
1111	SCLK / 16	1.38	1.50

3.2 ADC Clock Setting

The IA/IB/VA input ADC clock will be set as 1/2 system clock. For the ADC sampling rate, The PS1000 can set the different ADC sampling rate for different application. This setting is controlled by the ADCCFG register. The ADCCFG configuration is

ADCCFG (0xFE21)							
B7	B6	B5	B4	B3	B2	B1	B0
EN	ADCMODE		Half-Rate	ADCDIV			

ADC mode: ADC format selection

0x: Unsigned

10: Signed 2's complement

11: Signed 1's complement

Half-Rate

0: Normal ADC data rate

1: Half ADC data rate

ADCDIV: ADC sampling rate selection

		SYSCLK(24M)	SYSCLK(22M)
0000	ADC_CLK / 375	32.00K	29.33K
0001	ADC_CLK / 750	16.00K	14.67K
0010	ADC_CLK / 768	15.63K	14.32K
0011	ADC_CLK / 1536	7.81K	7.16K
0100	ADC_CLK / 1500	8.00K	7.33K
0101	ADC_CLK / 500	24.00K	22.00K
0110	ADC_CLK / 250	48.00K	44.00K

0111	ADC_CLK / 384	31.25K	28.65K
1000	ADC_CLK / 544	22.06K	20.22K
1001	ADC_CLK / 1088	11.03K	10.11K
1010	ADC_CLK / 512	23.44K	21.48K
1011	ADC_CLK / 1024	11.72K	10.74K
1100	ADC_CLK / 136	88.24K	80.88K
1101	ADC_CLK / 272	44.12K	40.44K
1110	ADC_CLK / 128	93.75K	85.94K
1111	ADC_CLK / 256	46.88K	42.97K

In the PS1000, it still has one ADC for temperature measurement. This ADC can be controlled by the SARCFG.

SARCFG (0xFE22)							
B7	B6	B5	B4	B3	B2	B1	B0
EN	x	x	SARDIV[4:0]				

EN: SAR ADC Enable or Disable

0: Disable SAR ADC

1: Enable SAR ADC

SARDIV [4:0]: SAR ADC selection. The clock range is 100K ~ 2MHz. The SAR ADC will output one ADC data every 13 SAR ADC clock

SARDIV[4:0]		SYSCLK(24M)	SYSCLK(22M)
00000	SYSCLK / 2	Not suggest	Not suggest
00001	SYSCLK / 4	Not suggest	Not suggest
00010	SYSCLK / 6	Not suggest	Not suggest
00011	SYSCLK / 8	Not suggest	Not suggest
00100	SYSCLK / 10	184.6	169.2
00101	SYSCLK / 12	153.8	141.0
00110	SYSCLK / 14	131.9	120.9
00111	SYSCLK / 16	115.4	105.8
01000	SYSCLK / 18	102.6	94.0
01001	SYSCLK / 20	92.3	84.6
01010	SYSCLK / 22	83.9	76.9
01011	SYSCLK / 24	76.9	70.5
01100	SYSCLK / 26	71.0	65.1
01101	SYSCLK / 28	65.9	60.4
01110	SYSCLK / 30	61.5	56.4
01111	SYSCLK / 32	57.7	52.9
10000	SYSCLK / 34	54.3	49.8
10001	SYSCLK / 36	51.3	47.0
10010	SYSCLK / 38	48.6	44.5

10011	SYSCLK / 40	46.2	42.3
10100	SYSCLK / 42	44.0	40.3
10101	SYSCLK / 44	42.0	38.5
10110	SYSCLK / 46	40.1	36.8
10111	SYSCLK / 48	38.5	35.3
11000	SYSCLK / 50	36.9	33.8
11001	SYSCLK / 52	35.5	32.5
11010	SYSCLK / 54	34.2	31.3
11011	SYSCLK / 56	33.0	30.2
11100	SYSCLK / 58	31.8	29.2
11101	SYSCLK / 60	30.8	28.2
11110	SYSCLK / 62	29.8	27.3
11111	SYSCLK / 64	28.8	26.4

3.3 DSP Clock Setting

The PS1000 can set the different DSP operation clock during the different operation condition. It also can help to save the power.

DSPCFG (0xFE25)							
B7	B6	B5	B4	B3	B2	B1	B0
EN	RDY	READ	SSPM	DSPDIV			

EN: DSP Enable or Disable
1: Enable DSP
0: Disable DSP

RDY: DSP ready flag
1: DSP data is ready; it must read by the MCU
0: DSP data is not ready or already read by MCU

READ: MCU Read data flag
MCU set this flag to clear the RDY flag, the “0” is clear. So, when DSP is operating the READ must set as ‘1’. When the MCU check the RDY is set to ‘1’, MCU must toggle READ flag (1-0-1) to clear the RDY flag.

SSPM: Specific the SSP interface is controlled by DSP or MCU.
1: SSP I/F is controlled by DSP
0: SSP I/F is controlled by MCU

DSPDIV: DSP clock Divider

DSPDIV[3:0]	DSPCLK	22MHz	24MHz

0000	SCLK / 1	22.00	24.00
0001	SCLK / 2	11.00	12.00
0010	SCLK / 3	7.33	8.00
0011	SCLK / 4	5.50	6.00
0100	SCLK / 5	4.40	4.80
0101	SCLK / 6	3.67	4.00
0110	SCLK / 7	3.14	3.43
0111	SCLK / 8	2.75	3.00
1000	SCLK / 9	2.44	2.67
1001	SCLK / 10	2.20	2.40
1010	SCLK / 11	2.00	2.18
1011	SCLK / 12	1.83	2.00
1100	SCLK / 13	1.69	1.85
1101	SCLK / 14	1.57	1.71
1110	SCLK / 15	1.47	1.60
1111	SCLK / 16	1.38	1.50

4. SFR Mapping

The PS1000 has some non-standard SFR configure register for some special blocks, like, SPI, I2C, SSP, ALU and extended interrupt controller.

The mapping of the PS1000 SFR is shown as follow. The red mark means these SFR were not the standard SFR.

F8H	IMR	IPR	ICR	IRR	ISR			
F0H	B							
E8H								
E0H	ACC	PDCON						
D8H	WDTCON							
D0H	PSW							
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		
C0H	SCON1	SBUF1	SCON2	SBUF2				
B8H	IP			SSPCFG1	SSPCFG2	SPICON	SPISTA	SPIDAT
B0H	P3		I2CCKH	I2CCKL	I2CCON	I2CSTA	I2CADR	I2CDAT
A8H	IE			SSPDXH	SSPDXL	SSPRXH	SSPRXL	SSPSTA
A0H	P2				Reserved	Reserved		
98H	SCON	SBUF	P5	ALU_OP	A0/R0	A1/R1	A2/R2	A3/R3
90H	P1		P4CON	P5CON	B0/R4	B1/R5	B2/R6	B3/R7
88H	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	P4
80H	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON

For the setting for each SFR control register, please reference the relative section. (For the standard SFR, please reference the 8051 data sheet.)

P4/P5							
B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P4 and P5 is the extended I/O space. It can map to the P0 and P2 I/O pin location. That is controlled by MCUCFG PORTCTRL. For the P4/P5, each bit can be set as input or output. It is controlled by the P4CON and P5CON. “1” is for input and “0” for the output.

P4CON/P5CON							
B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The other SFRs setting please reference the relative section. Here is quick

reference table

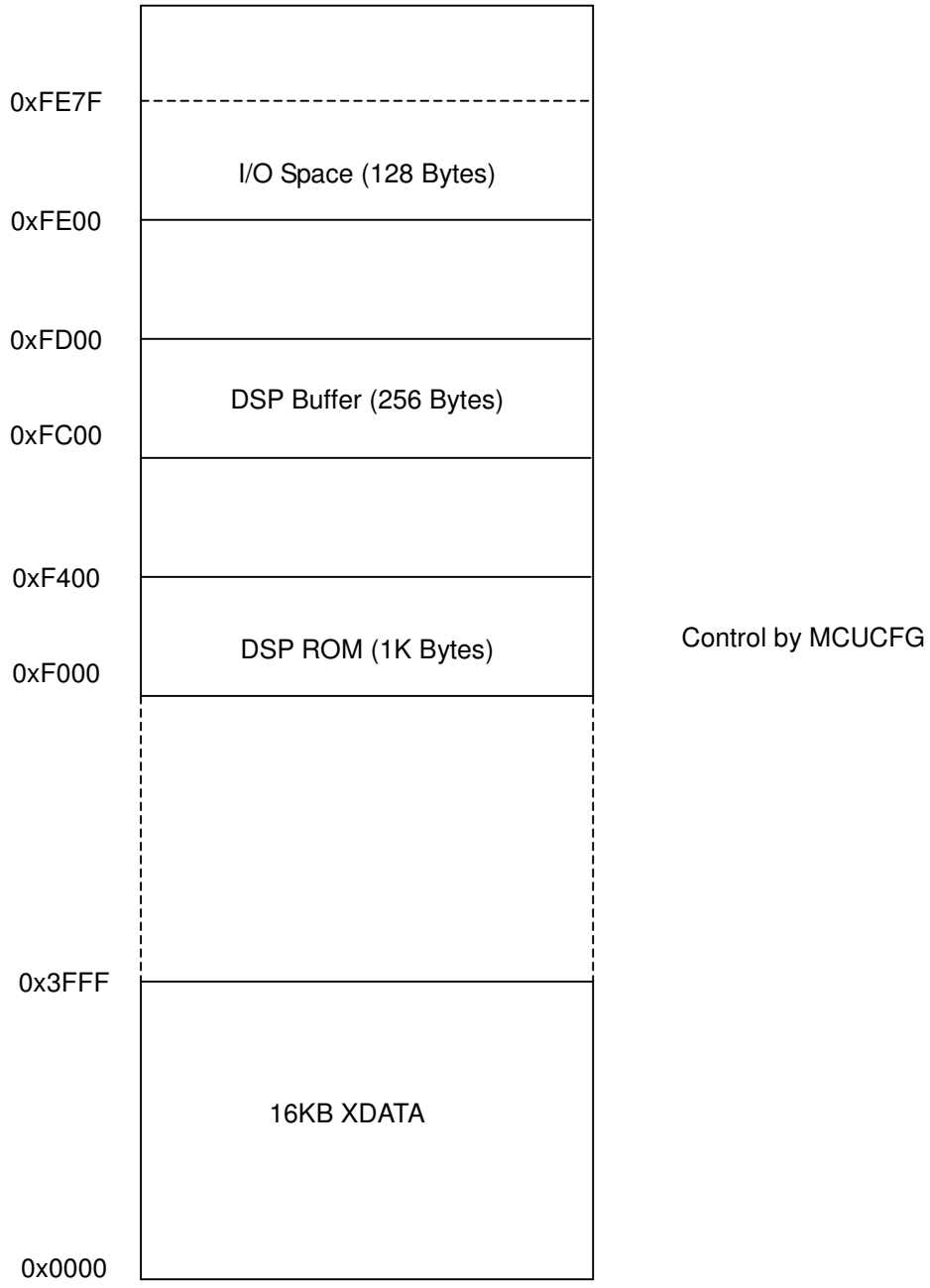
ALU	ALU_OP, A0, A1, A2, A3, B0, B1, B2, B3
I2C	I2CCKH, I2CCKL, I2CCON, I2CSTA, I2CADR, I2CDAT
SSP	SSPCON, SSPCFG
SPI	SPICON, SPISTA, SPIDAT
Interrupt	IMR, IPR, ICR, IRR

5. I/O Mapping

For the XDATA memory, address 0xF000 to 0xFFFF is mapping to the DSP and some special control register. The address 0xF000 ~ 0xF3FF(1KB) is mapped to DSPROM address. MCU can access this address by setting MCUCFG.DSPROM as '1'. When MCUCFG.DSPROM is setting as '0'. This address can not be access.

The address 0xFC00~0xFCFF (256 bytes) is mapped to the DSP data buffer and the 0xFE00~0xFE7F (128 bytes) is mapped to the I/O configuration. These use for store the DSP calculation data and system configuration registers. Detail description, please reference the relative section.

The memory mapping is shown as follow.


0xFE7F
I/O Space (128 Bytes)
0xFE00
0xFD00
DSP Buffer (256 Bytes)
0xFC00
0xF400
DSP ROM (1K Bytes)
0xF000
Control by MCUCFG
0x3FFF
16KB XDATA
0x0000

FE00h	ADCVA_L	FE10h	RTCYear	FE20h	AGCCFG	FE30h	UVTH_B0
FE01h	ADCVA_H	FE11h	RTCMonth	FE21h	ADCCFG	FE31h	UVTH_B1
FE02h	ADCIA_L	FE12h	RTCDay	FE22h	SARCFG	FE32h	UVTH_B2
FE03h	ADCIA_H	FE13h	RTCWeek	FE23h	SAGCFG	FE33h	UVTH_B3
FE04h	ADCIB_L	FE14h	RTCHour	FE24h	SWELLCFG	FE34h	UVTH_B4
FE05h	ADCIB_H	FE15h	RTCMinutes	FE25h	DSPCFG	FE35h	UVTH_B5
FE06h	Temp_L	FE16h	RTCSec	FE26h	LCDCFG	FE36h	SampleCnt_L
FE07h	Temp_H	FE17h		FE27h	LCDDIV	FE37h	SampleCnt_H
FE08h	AGCGain	FE18h	LoopCnt_L	FE28h	RTCCFG	FE38h	CONST
FE09h		FE19h	LoopCnt_H	FE29h	MCUCFG	FE39h	wRTCYear
FE0Ah		FE1Ah	DSPStatus	FE2Ah	OVTH _B0	FE3Ah	wRTCMonth
FE0Bh		FE1Bh		FE2Bh	OVTH _B1	FE3Bh	wRTCDay
FE0Ch		FE1Ch		FE2Ch	OVTH _B2	FE3Ch	RTCCFG2
FE0Dh		FE1Dh		FE2Dh	OVTH _B3	FE3Dh	wRTCHour
FE0Eh		FE1Eh		FE2Eh	OVTH _B4	FE3Eh	wRTCMinutes
FE0Fh		FE1Fh		FE2Fh	OVTH _B5	FE3Fh	wRTCSec

FE40h	LCDDAT0	FE50h	LCDDAT16	FE60h	AGCTH_L	FE60h	
FE41h	LCDDAT1	FE51h	LCDDAT17	FE61h	AGCTH_L	FE61h	
FE42h	LCDDAT2	FE52h	LCDDAT18	FE62h	AGCTH_L	FE62h	
FE43h	LCDDAT3	FE53h	LCDDAT19	FE63h	AGCTH_L	FE63h	
FE44h	LCDDAT4	FE54h	VAoffset_L	FE64h	AGCTH_L	FE34h	
FE45h	LCDDAT5	FE55h	VAoffset_H	FE65h	AGCTH_L	FE65h	
FE46h	LCDDAT6	FE56h		FE66h	AGCTH_H	FE66h	
FE47h	LCDDAT7	FE57h		FE67h	AGCTH_H	FE67h	
FE48h	LCDDAT8	FE58h	IAoffset_L	FE28h	AGCTH_H	FE68h	
FE49h	LCDDAT9	FE59h	IAoffset_H	FE29h	AGCTH_H	FE69h	
FE4Ah	LCDDAT10	FE5Ah	IBoffset_L	FE6Ah	AGCTH_H	FE6Ah	
FE4Bh	LCDDAT11	FE5Bh	IBoffset_H	FE6Bh	AGCTH_H	FE6Bh	
FE4Ch	LCDDAT12	FE5Ch	OffsetCFG_L	FE6Ch		FE6Ch	
FE4Dh	LCDDAT13	FE5Dh	OffsetCFG_H	FE2Dh		FE6Dh	
FE4Eh	LCDDAT14	FE5Eh		FE6Eh		FE6Eh	
FE4Fh	LCDDAT15	FE5Fh		FE6Fh		FE6Fh	

The description of each configuration register is shown as below

ADR	Name	Description	Notes
FE00h	ADCIA_L	IA channel ADC output (low byte)	Read only
FE01h	ADCIA_H	IA channel ADC output (high byte)	Read only
FE02h	ADCIB_L	IB channel ADC output (low byte)	Read only
FE03h	ADCIB_H	IB channel ADC output (high byte)	Read only
FE04h	ADCVA_L	VA channel ADC output (low byte)	Read only
FE05h	ADCVA_H	VA channel ADC output (high byte)	Read only
FE06h	Temp_L	Temperature sensor ADC output (low byte)	Read only
FE07h	Temp_H	Temperature sensor ADC output (high byte)	Read only
FE08h	AGCGain	IA/IB Auto Gain status	Read only

ADR	Name	Description	Notes
FE10h	RTCYear	RTC Year result 0 ~ 128 (2000 ~ 2128)	Read only

FE11h	RTCMonth	RTC Month result (1~12)	Read only
FE12h	RTCDay	RTC Day result (1~31)	Read only
FE13h	RTCWeek	RTC Weak result (1~7)	Read only
FE14h	RTCHour	RTC Hour result (0~23)	Read only
FE15h	RTCMinutes	RTC Minute result (0~59)	Read only
FE16h	RTCSec	RTC Second result (0~59)	Read only
FE18h	LoopCnt_L	DSP loop count (low byte)	Read only
FE19h	LoopCnt_H	DSP loop count (high byte)	Read only
FE1Ah	DSPStatus	DSP status register	Read only

ADR	Name	Description	Notes
FE20h	AGCCFG	AGC configuration register	Read/Write
FE21h	ADCCFG	I/V ADC configuration register	Read/Write
FE22h	SARCFG	Temperature ADC configuration register	Read/Write
FE23h	SAGCFG	Reserved	Read/Write
FE24h	SWELLCFG	Reserved	Read/Write
FE25h	DSPCFG	DSP configuration register	Read/Write
FE26h	LCDCFG	LCD configuration register	Read/Write
FE27h	LCDDIV	LCD control register	Read/Write
FE28h	RTCCFG	RTC configuration register	Read/Write
FE29h	MCUCFG	MCU configuration register	Read/Write
FE2Ah	OVTH_B0	Over voltage threshold setting byte 0 (LSB)	Read/Write
FE2Bh	OVTH_B1	Over voltage threshold setting byte 1	Read/Write
FE2Ch	OVTH_B2	Over voltage threshold setting byte 2	Read/Write
FE2Dh	OVTH_B3	Over voltage threshold setting byte 3	Read/Write
FE2Eh	OVTH_B4	Over voltage threshold setting byte 4	Read/Write
FE2Fh	OVTH_B5	Over voltage threshold setting byte 5 (MSB)	Read/Write
FE30h	UVTH_B0	Under voltage threshold setting byte 0 (LSB)	Read/Write
FE31h	UVTH_B1	Under voltage threshold setting byte 1	Read/Write
FE32h	UVTH_B2	Under voltage threshold setting byte 2	Read/Write
FE33h	UVTH_B3	Under voltage threshold setting byte 3	Read/Write
FE34h	UVTH_B4	Under voltage threshold setting byte 4	Read/Write
FE35h	UVTH_B5	Under voltage threshold setting byte 5 (MSB)	Read/Write
FE36h	SampleCnt_L	DSP integration period (low byte)	Read/Write
FE37h	SampleCnt_H	DSP integration period (high byte)	Read/Write
FE38h	CONST	DSP constant value	Read/Write
FE39h	wRTCYear	RTC Year setting	Read/Write
FE3Ah	wRTCMonth	RTC Month setting	Read/Write
FE3Bh	wRTCDay	RTC Day setting	Read/Write
FE3Ch	RTCCFG2	RTC Configuration register 2	Read/Write
FE3Dh	wRTCHour	RTC Hour setting	Read/Write
FE3Eh	wRTCMinutes	RTC Minute setting	Read/Write
FE3Fh	wRTCSec	RTC Second setting	Read/Write
FE40h	LCDDAT0	LCD SEG0/SEG1 display data buffer	Read/Write
FE41h	LCDDAT1	LCD SEG2/SEG3 display data buffer	Read/Write
FE42h	LCDDAT2	LCD SEG4/SEG5 display data buffer	Read/Write
FE43h	LCDDAT3	LCD SEG6/SEG7 display data buffer	Read/Write
FE44h	LCDDAT4	LCD SEG8/SEG9 display data buffer	Read/Write
FE45h	LCDDAT5	LCD SEG10/SEG11 display data buffer	Read/Write
FE46h	LCDDAT6	LCD SEG12/SEG13 display data buffer	Read/Write
FE47h	LCDDAT7	LCD SEG14/SEG15 display data buffer	Read/Write
FE48h	LCDDAT8	LCD SEG16/SEG17 display data buffer	Read/Write
FE49h	LCDDAT9	LCD SEG18/SEG19 display data buffer	Read/Write
FE4Ah	LCDDAT10	LCD SEG20/SEG21 display data buffer	Read/Write
FE4Bh	LCDDAT11	LCD SEG22/SEG23 display data buffer	Read/Write
FE4Ch	LCDDAT12	LCD SEG24/SEG25 display data buffer	Read/Write
FE4Dh	LCDDAT13	LCD SEG26/SEG27 display data buffer	Read/Write
FE4Eh	LCDDAT14	LCD SEG28/SEG29 display data buffer	Read/Write
FE4Fh	LCDDAT15	LCD SEG30/SEG31 display data buffer	Read/Write
FE50h	LCDDAT16	LCD SEG32/SEG33 display data buffer	Read/Write
FE51h	LCDDAT17	LCD SEG34/SEG35 display data buffer	Read/Write
FE52h	LCDDAT18	LCD SEG36/SEG37 display data buffer	Read/Write
FE53h	LCDDAT19	LCD SEG38/SEG39 display data buffer	Read/Write
FE54h	VAoffset_L	VA channel offset value (low byte)	Read/Write
FE55h	VAoffset_H	VA channel offset value (high byte)	Read/Write

FE58h	IAoffset_L	IA channel offset value (low byte)	Read/Write
FE59h	IAoffset_H	IA channel offset value (high byte)	Read/Write
FE5Ah	IBoffset_L	IB channel offset value (low byte)	Read/Write
FE5Bh	IBoffset_H	IB channel offset value (high byte)	Read/Write
FE5Ch	OffsetCFG_L	Offset Configuration register (low byte)	Read/Write
FE5Dh	OffsetCFG_H	Offset Configuration register (high byte)	Read/Write
FE60h	AGCTH_L	AGC threshold low setting byte 0 (LSB)	Read/Write
FE61h	AGCTH_L	AGC threshold low setting byte 1	Read/Write
FE62h	AGCTH_L	AGC threshold low setting byte 2	Read/Write
FE63h	AGCTH_L	AGC threshold low setting byte 3	Read/Write
FE64h	AGCTH_L	AGC threshold low setting byte 4	Read/Write
FE65h	AGCTH_L	AGC threshold low setting byte 5 (MSB)	Read/Write
FE66h	AGCTH_H	AGC threshold high setting byte 0 (LSB)	Read/Write
FE67h	AGCTH_H	AGC threshold high setting byte 1	Read/Write
FE28h	AGCTH_H	AGC threshold high setting byte 2	Read/Write
FE29h	AGCTH_H	AGC threshold high setting byte 3	Read/Write
FE6Ah	AGCTH_H	AGC threshold high setting byte 4	Read/Write
FE6Bh	AGCTH_H	AGC threshold high setting byte 5 (MSB)	Read/Write

6. DSP

The PS1000 has one special design 32-bit DSP for the Power calculation. For this DSP, it can perform and special program which define by the customer faster and lower power. The program for this DSP is shown below.

Here is the list for the DSP calculation

VA HPF	IA HPF	IB HPF
VA offset value	IA offset value	IB offset value
VA RMS value	IA RMS value	IB RMS value
PA value	PB value	
Over voltage count	Over voltage maximum value	
Under voltage count	Under voltage minimum value	

6.1 DSP Program

In the DSP, it had 64x32 memory space for DSP calculation. When the DSP finish the calculation base on the ADC sample number which specified by the sample count, the DSP will copy this memory data to the DSP output buffer (0xFC00 ~ 0xFCFF). The MCU can access this memory to get the DSP calculation result.

ADR				
0	Varms(H)	Varms(L)		
4	Iarms(H)	Iarms(L)	Ibrms(H)	Ibrms(L)
8	Pa(H)	Pa(L)	Pb(H)	Pb(L)
12				
16				
20	OVCnt	OVMax(H)	OVMax(L)	UVCnt
24	UVMin(H)	UVMin(L)		
28		VaOS		IaOS
32	IbOS			
36				
40				
44				
48				
52				
56	OVTH(L)	UVTH(H)	UVTH(L)	VAoffset
60		IAoffset	IBoffset	OffsetCFG

6.2 AGC

The DSP circuit has built-in one AGC control circuit. It can control the AGC at the front of IA/IB ADC input. The control range is 1X, 2X, 4X and 8X.

AGCCFG(0xFE20h)							
B7	B6	B5	B4	B3	B2	B1	B0
EN	MC	x	TM0	IBGain		IAGain	

EN: AGC Enable

0: Disable (Used DSP setting)

1: Enable (auto Control)

MC: Multi-Cycle Enable

0: Disable

1: Enable

TM0: ADC Test Mode Control

1: Bypass ADC Anti-Alias Filter for All ADC

IBGain: IB channel gain setting

00: 1X

01: 2X

10: 4X

11: 8X

IAGain: IA channel gain seting

00: 1X

01: 2X

10: 4X

11: 8X

For the auto gain control, it will depend on the integration result of IA and IB. the default value is 4X. When the IA/IB integration is over the 50% of full scale, the AGC will decrease the gain value as one level (8X – 4X – 2X – 1X). On the other hand, when the IA/IB integration value is under the 16% of full scale, AGC will increase the gain range as one level (1X – 2X – 4X – 8X). When the AGC reach to maximum gain range (8X), AGC will not increase the gain range again. Similarly, when AGC reach to minimum gain range (1X), AGC will not decrease the gain range again.

The MCU can disable the AGC function and control by MCU itself. The MCUCFG can set the AGCCFG.EN as 0. It will disable the AGC function and the gain will follow the value by AGCCFG.IAGain and AFGCFG.IBGain.

The MCU can get the current gain information form the AGCGain register. Here is the format of AGCGain.

AGCGain (FE08h)							
B7	B6	B5	B4	B3	B2	B1	B0
0	0	IAGain		0	0	IBGain	

The MCU can set the AGC threshold to control the AGC adjustment point. The threshold setting as

(MSB) (LSB)
AGCTH_L = {FE65h, FE64h, FE63h, FE62h, FE61h, FE60h}
AGCTH_H = {FE6Bh, FE6Ah, FE69h, FE68h, FE67h, FE66h}

6.3 DSP Status

The MCU can check the DSP status through the DSPStatus register.

DSPStatus (0xFE1A)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DSPRDY	STOP	TRIGCNT					

DSPRDY
0: DSP data is not ready
1: DSP data is ready, MCU need to read the DSP data and clear the DSPRDY flag

STOP
0: DSP is running
1: DSP is stop and wait for next ADC data

TRIGCNT: DSP Trig Count

7. MCU

The PS1000 has one high performance 8-bit 8051 MCU. This MCU has 64KB program space and 16KB data space. It also has 256B internal data space. The PS1000 MCU is fully compatible with general purpose 8051 MCU. Except the stand MCU, the PS1000 MCU still have some more special functional block for the performance and I/O enhancement.

For the standard MCU parts, please reference the 8051 user's manual. The following description only focus on the different parts.

7.1 32-bit ALU

PS1000 MCU had built-in one 32-bit ALU. This ALU can perform the 32 bits ADD, SUB, MUL, DIV, Shift and Rotate. It can make the 8051 more efficient for the 32 bits arithmetic operation. The ALU can control by the ALUOP SFR register. When the ALU is not used, the operand A and B in the SFR can play as internal register. The configuration of ALUOP is shown below

ALUOP(SFR 0x9B)							
B7	B6	B5	B4	B3	B2	B1	B0
EN	BUSY	MODE	CI	OPCODE			

EN: ALU operation control
1: ALU start operate
0: ALU Ready/operation

BUSY: ALU BUSY Flag
1: ALU Busy
0: ALU ready for next instruction

MODE: Operand A/B Mode control
0: A/B maps to ALU output C/D output when the SFR read
1: A/B does not map to ALU C/D output, it plays as register

CI: Carry input

OPCode: ALU operation Control

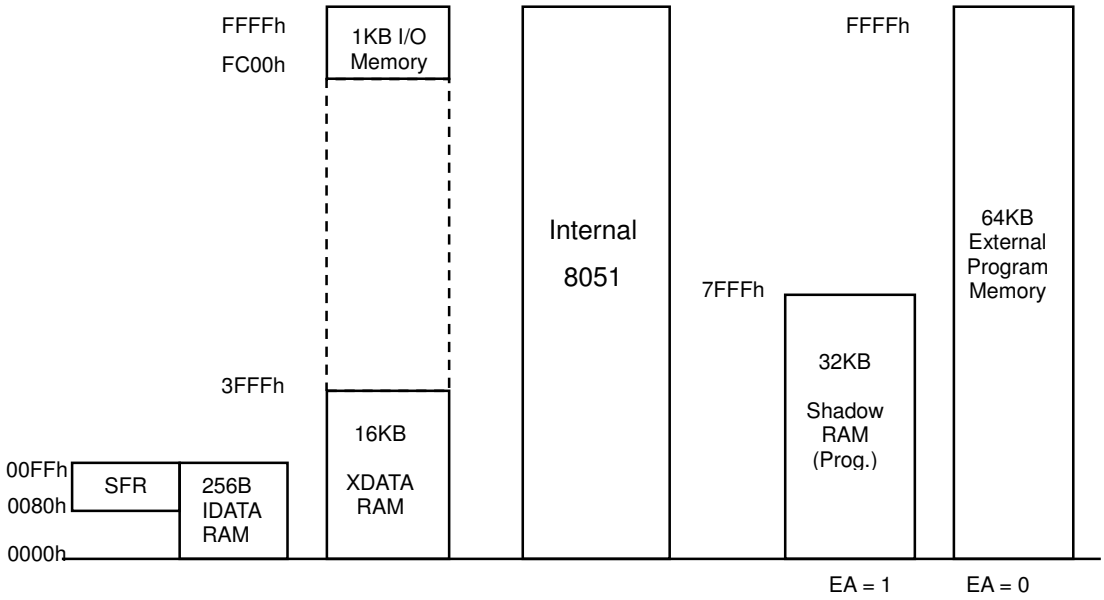
0000 16-bits MUL (unsigned) C = AL * BL
0001 16-bits MUL (signed) C = AL * BL
0010 32-bits MUL (unsigned) {D,C} = A * B
0011 32-bits MUL (signed) {D,C} = A * B
0100 C = C + D
0101 C = AH * AL, D = BH *BL (signed)
0110 32-bits DIV (unsigned) {C, D} = A / B
0111 32-bits DIV (unsigned)
1000 Shift Left
1001 Shift Left with Carry
1010 Shift Right
1011 Shift Right with Carry
1100 Rotate Left
1101
1110 Rotate Right
1111

When the MCU wants to use the ALU, it must set the operand A, B and OPCode fist. After all configurations are set, MCU toggle the EN bit to enable the ALU operation and wait for the BUSY return to zero. For every ALU operation, MCU needs to toggle the EN bit once.

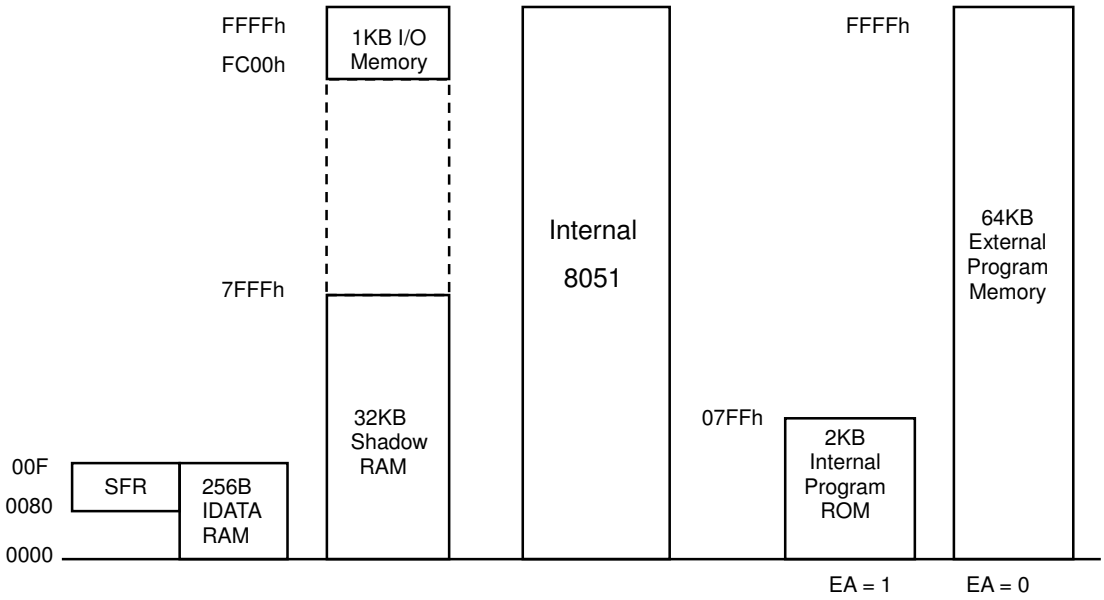
7.2 MODE Control

PS1000 has several operation modes; it can control by the MODE [2:0]. There are four major modes for the PS1000, normal operation mode, ICP (In-Circuit Programming) mode, external MCU mode and test mode. The memory space of each mode is shown as follow.

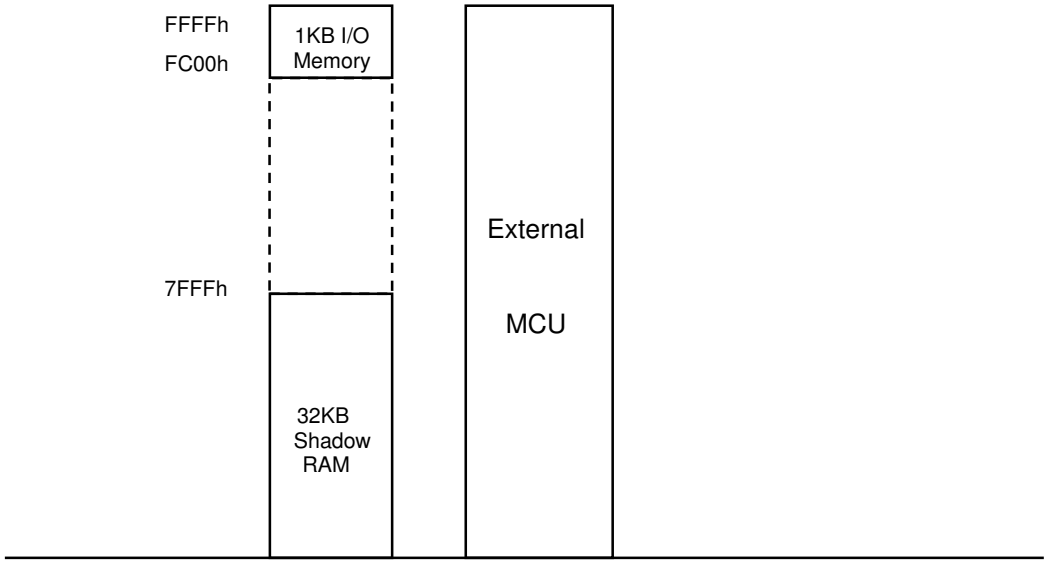
Normal Operation Mode



ICP Mode



External CPU Mode



The mode setting quick reference table is shown as below.

Mode	EA	MCU	ROM	RAM	Notes
000	0	Internal	External Flash	XDATA + I/O Memory	Normal Operation 1
000	1	Internal	Internal Flash	XDATA + I/O Memory	Normal Operation 1
001	0	Internal	External Flash	Flash + I/O Memory	ICP Mode
001	1	Internal	Internal ICP ROM	Flash + I/O Memory	ICP Mode
010	x	External		XDATA + I/O Memory	External 51 Mode 1
011	0	Internal	External Flash	XDATA+ I/O Memory	Factory Test Mode
011	1	Internal	Internal Flash	XDATA+ I/O Memory	Factory Test Mode
100	x	External		Internal Memory + I/O Memory	Memory Test Mode
101	x	External		I/O Memory	External 51 Mode 2
110	0	Non			Analog Test Mode1
110	1	Non			Analog Test Mode 2
111	x	Non			Memory BIST

Notes:

1. The “Normal Operation Mode” 1/2 is similar; the difference is “Normal Operation Mode 1” will trigger the power on sequence circuit.
2. The “External MCU Mode” 1/2 is similar; the difference is the XDATA memory space mapping.

For some other special MCU interface function please reference next several sections for the SPI, I2C and SSP I/O interface.

8. SPI

The PS1000 has one SPI interface which can be master or slave.

This SPI interface is controlled by the SPICTL/SPIDAT/SPISTA register. These registers are mapped at the SFR memory space. The setting for these register are

SPICTL(SFR 0xBD)							
B7	B6	B5	B4	B3	B2	B1	B0
EN	SS	MST	CPOL	CPHA	Baud Rate Selection		

EN SPI enable bit
1: enable the SPI interface
0: disable the SPI interface

SS SS disable bit
1: disable SS in both master and slave modes, no MODF interrupt request is generated.
0: enable SS in both master and slave modes

MST Serial peripheral master mode
1: configure the SPI as a master
0: configure the SPI as a slave

CPOL Clock polarity
1: SCK set to “1” in idle state
0: SCK set to “0” in idle state

CPHA Clock phase
1: have the data sampled when the SCK returns to idle state
0: have the data sampled when the SCK leaves the idle state

Baud Rate SPI clock selection

000	MCUCLK / 1
001	MCUCLK / 2
010	MCUCLK / 4
011	MCUCLK / 8
100	MCUCLK / 16
101	MCUCLK / 32
110	MCUCLK / 64
111	MCUCLK / 128

SPIDAT

SPIDAT(SFR 0xBF)							
B7	B6	B5	B4	B3	B2	B1	B0
D7	D6	D5	D4	D3	D2	D1	D0

SPISTA

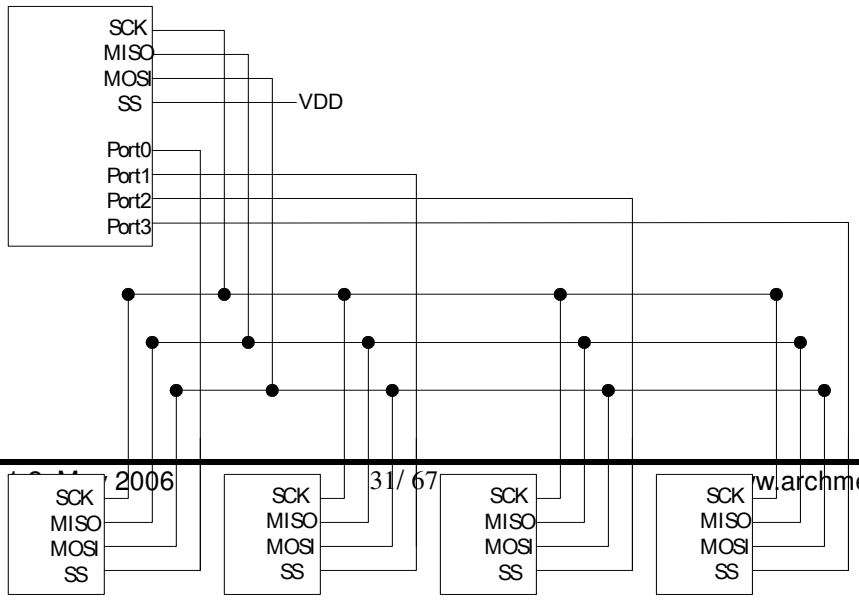
SPISTA(SFR 0xBE)							
B7	B6	B5	B4	B3	B2	B1	B0
SPIF	WCOL	MODF	x	x	x	x	x

SPIF SPI data transfer flag
1: the data transfer has been completed
0: data transfer is in progress or the status register has been read by controller

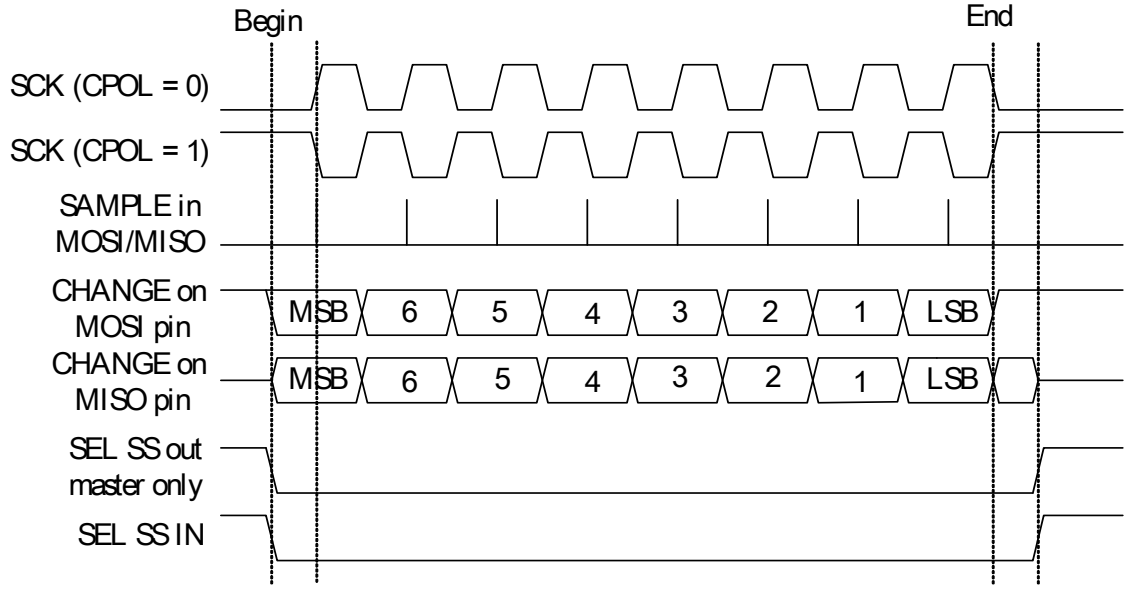
WCOL Write Collision Flag
1: a collision has been detected
0: no collision has occurred or the status register has been read by controller

MODF Mode Fault, it can only be cleared by disabling the SPI
1: the SS pin is at inappropriate logic level
0: the SS pin is at appropriate logic level

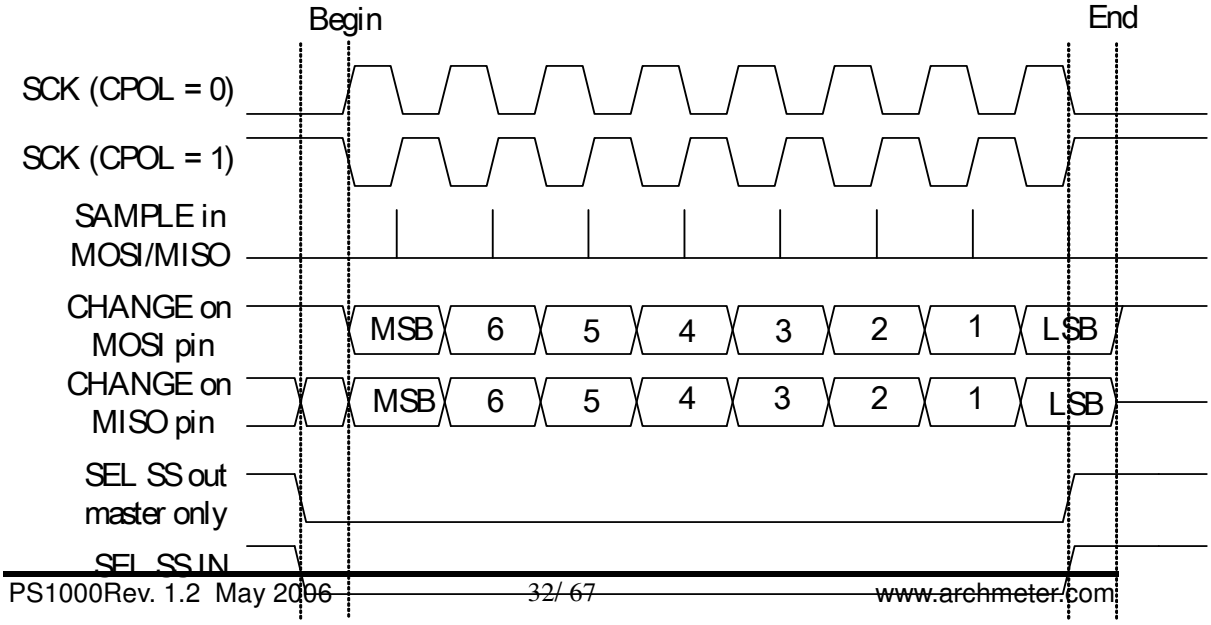
For the SPI interface, one master could connect with several slave devices. Here is the connection diagram. All slave devices share the SCK, MISO(SI) and MOSI(SO) bus. But for the SS control signal, each slave device must control individually.



For the SPI interface, it can select the different clock phase and polarity. Here is the timing diagram to show the different configuration.



CPHA=0



CPHA = 1

9. I²C

The PS1000 has one I²C interface. This I²C interface is controlled by the I2CCKH/I2CCKL/I2CCTL/I2CSTA/I2CDAT registers. These registers are mapped at the SFR memory space. The setting for these registers are

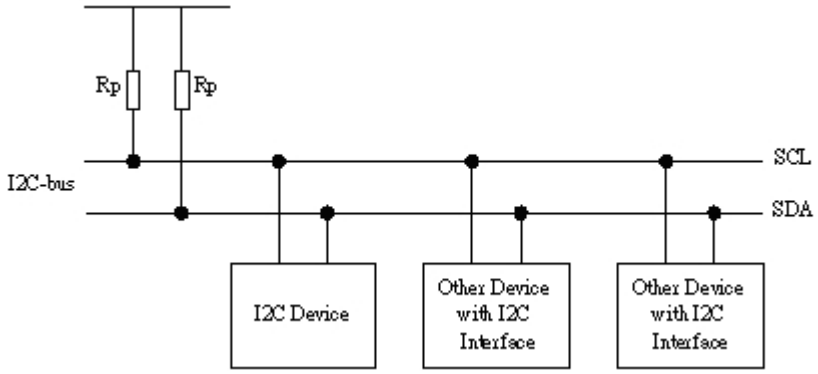
The I²C-bus uses two wires, serial clock (SCL) and serial data (SDA) to transfer information between devices connected to the bus, and has the following features:

- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes

A typical I²C-bus configuration is shown in below. Depending on the state of the direction bit (R/W), two types of data transfers are possible on the I²C-bus:

- Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
- Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows the data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the I²C-bus will not be released.

I²C-bus configuration



9.1 Registers

The micro-controller interfaces with the I^2C-bus through six Special Function Registers (SFRs): I^2CCKHR (I^2C SCL Duty Cycle Register High Byte), I2CCKLR (I^2C SCL Duty Cycle Register Low Byte), I2CCTLR (I^2C Control Register), I2CSTAR (I^2C Status Register), I2CADRR (I^2C Slave Address Register), and I2CDATR (I^2C Data Register).

I2CCKHR (I^2C SCL Duty Cycle Register High Byte)

I2CCKHR(SFR 0xB2) Reset value: 23h							
B7	B6	B5	B4	B3	B2	B1	B0
CKHR.7	CKHR.6	CKHR.5	CKHR.4	CKHR.3	CKHR.2	CKHR.1	CKHR.0

I2CCKLR (I^2C SCL Duty Cycle Register Low Byte)

I2CCKLR(SFR 0xB3) Reset value 23h							
B7	B6	B5	B4	B3	B2	B1	B0
CKLR.7	CKLR.6	CKLR.5	CKLR.4	CKLR.3	CKLR.2	CKLR.1	CKLR.0

The registers, I2CCKHR and I2CCKLR, define the data rate of the I^2C interface. I2CCKHR defines the number of the system clock for SCL = high, I2CCKLR defines the number of the system clock for SCL = low. The frequency of data transfer is determined by the following formula:

$$\text{Bit frequency} = f_{SYSTEM\_CLOCK} / (\text{I2CCKHR} + \text{I2CCKLR})$$

The values for I^2CCKHR and I2CCKLR do not have to be the same. Different duty cycle can be defined by setting these two registers. However, the value of the register must ensure that the data rate is in the I^2C data rate range of

0 – 400 KHz. Thus the values of I2CCKHR and I2CCKLR have some restrictions. Some relationship between the system clock, bit data rate, and values of registers are shown in table 1-1. Note that the values for both registers greater than three system clocks are recommended.

I^2C clock rates selection

I^2CCKHR + I^2CCKLR	Bit data rate (Kbit/sec) at f_{SYS_CLK}	
	5 MHz	25MHz
13	384	-
14	357	
20	250	
50	100	
70	71	357
100	50	250
200	25	75
500	10	50

I2CCTLR (I^2C Control Register)

I2CCTLR(SFR 0xB4) Reset value 00h							
B7	B6	B5	B4	B3	B2	B1	B0
I2CEN	STA	STO	INTR	AA	-	-	-

This register can be written or read. There are two bits affected by hardware: the INTR bit and STO bit. The INTR bit is set by hardware and the STO bit is cleared by hardware.

The STA bit is START flag. Setting this bit causes the I^2C interface to enter master mode and attempt transmitting a START condition or transmitting a repeated START condition when it is already in master mode.

The STO bit is STOP flag. Setting this bit causes the I^2C interface to transmit a STOP condition in master mode, or recovering from an error condition in slave mode.

If the STA and STO are both set, then a STOP condition is transmitted to the I^2C-bus if it is in master mode, and transmits a START condition afterwards. If it is in slave mode, an internal STOP condition will be generated, but it is not transmitted to the bus.

BIT	SYMBOL	FUNCTION

I2CCTLR7	I^2CEN	I2C enable bit 1 = enables the I2C interface 0 = disables the I2C interface
I2CCTLR6	STA	Start flag 1 = I^2C enters master mode and generates a START condition. When the I^2C interface is already in master mode and some data has been transmitted or received, it transmits a repeated START condition. 0 = no START condition or repeated START condition will be generated
I2CCTLR5	STO	STOP flag 1 = in master mode, a STOP condition is transmitted to the I^2C bus. When the bus detects the STOP condition, it will clear STO bit automatically. In slave mode, setting this bit can recover from an error condition. In this case, no STOP condition is transmitted to the bus. The hardware behaves as if a STOP condition has been received and it switches to "not addressed" Slave Receiver Mode. The STO flag is cleared by hardware automatically
I2CCTLR4	SI	I^2C interrupt flag 1 = one of the 25 possible I^2C states is entered, an interrupt is requested, it is cleared automatically when the I^2C status register is cleared
I2CCTLR3	AA	Assert acknowledge flag 1 = an acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line on the following situations: (1) The "own slave address" has been received. (2) The general call address has been received while the general call bit (GC) in I2ADR is set. (3) A data byte has been received while the I^2C interface is in the Master Receiver Mode. (4) A data byte has been received while the I^2C interface is in the addressed Slave Receiver Mode. 0 = an not acknowledge (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line on the following situations: (1) A data byte has been received while the I^2C interface is in the Master Receiver Mode. (2) A data byte has been received while the I^2C interface is in the Slave receiver Mode
I2CCTLR2-0	-	Reserved for future use

I2CSTAR (I^2C Status Register)

I2CSTAR(SFR 0xB5) Reset value 00h							
B7	B6	B5	B4	B3	B2	B1	B0
STAR.4	STAR.3	STAR.2	STAR.1	STAR.0	0	0	0

This register contains the status code of I^2C interface. The least three bits are always zero. There are 26 possible status codes. When the code is 00H, there is no relevant information available and SI bit is not set. All other 25 status codes correspond to defined I^2C states. When any of these statuses entered, the SI bit will be set. When the interrupt service routine completes, the firmware should clear this register, and the SI will be automatically cleared. The detailed description of the 26 status code is shown later in this documentation.

BIT	SYMBOL	FUNCTION
I2CSTAR7, 3	STA4, 0	I^2C the status code, the firmware should clear this register while interrupt service routine completes
I2CSTAR2, 0	-	These three bits are not used and always set to 0

I2CADRR (I^2C Slave Address Register)

Reset value 00h

I2CADRR(SFR 0xB6)							
B7	B6	B5	B4	B3	B2	B1	B0
ADRR.6	ADRR.5	ADRR.4	ADRR.3	ADRR.2	ADRR.1	ADRR.0	GCEN

I2CADRR register is readable and writable, and is only used when the I^2C interface is set to slave mode. In master mode, this register has no effect. The LSB of I2CADRR is general call bit. When this bit is set, the general call address (00H) is recognized.

BIT	SYMBOL	FUNCTION
I2CADRR7, 1	ADRR6, 0	7-bit own slave address When in master mode, the contents of this register has no effect.
I2CADRR0	GCEN	General call enable bit 1 = the general call address (00H) is recognized 0 = the general call address is ignored

I2CDATR (I^2C Data Register)

I2CDATR(SFR 0xB7) Reset value FFh							
B7	B6	B5	B4	B3	B2	B1	B0
DATR.7	DATR.6	DATR.5	DATR.4	DATR.3	DATR.2	DATR.1	DATR.0

I2CDATR register contains the data to be transmitted or the data received. The micro controller can read and write to this 8-bit register while it is not in the process of shifting a byte. Thus this register should only be accessed when the SI bit is set. Data in I2CDATR remains stable as long as the SI bit is set. Data in I2CDATR is always shifted from right to left: the first bit to be transmitted is the MSB(bit 7), and after a byte has been received, the first bit of received data is located at the MSB of I2CDATR.

9.2 Operation Modes

The I^2C device provides four operation modes: Master Transmitter Mode, Master Receiver Mode, Slave Transmitter Mode and Slave Receiver Mode.

9.2.1 Master Transmitter Mode

In this mode data is transmitted from master to slave. Before the master transmitter mode can be entered, I2CCTLR must be initialized as follows:

I^2CCTLR	7	6	5	4	3	2	1	0
	I2CEN	STA	STO	SI	AA	-	-	-
	1	0	0	0	0	-	-	-

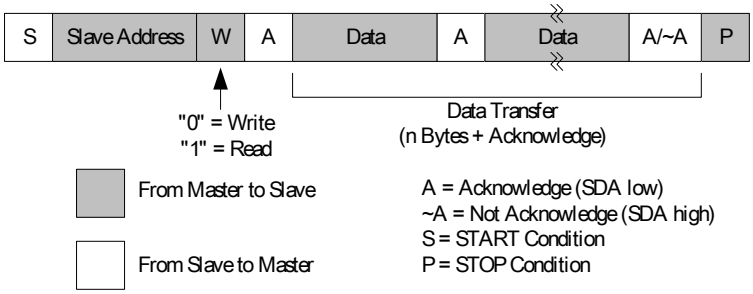
I2CEN must be set to 1 to enable the I^2C function. If the AA bit is 0, it will not acknowledge its own slave address or the general call address in the event of another device becoming master of the bus and it can not enter slave mode. STA, STO and SI bits must be cleared to 0.

The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case, the data direction bit (R/W) will be logic 0 indicating a write. Data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

The I^2C will enter Master Transmitter Mode by setting the STA bit. The I^2C logic will send the START condition as soon as the bus is free. After the START

condition is transmitted, the SI bit is set, and the status code in I^2C Status Register (I2CSTAR) should be 08h. This status code must be used to vector to an interrupt service routine where the user should load the slave address and data direction bit (SLA + W) to the I2C Data Register (I2CDATR). The I^2C Status Register (I2CSTAR) must be cleared by firmware, thus the SI bit is automatically cleared, before the data transfer can continue.

When the slave address and R/W bit have been transmitted and an acknowledgement bit has been received, the SI bit is set again. The appropriate action to be taken for each status codes is shown in Status Codes Table.

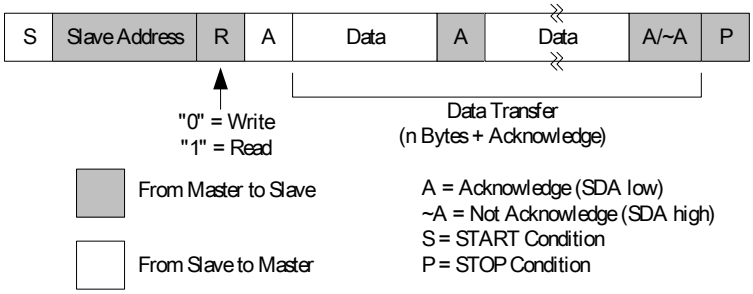


Format of master transmitter mode

9.2.2 Master Receiver Mode

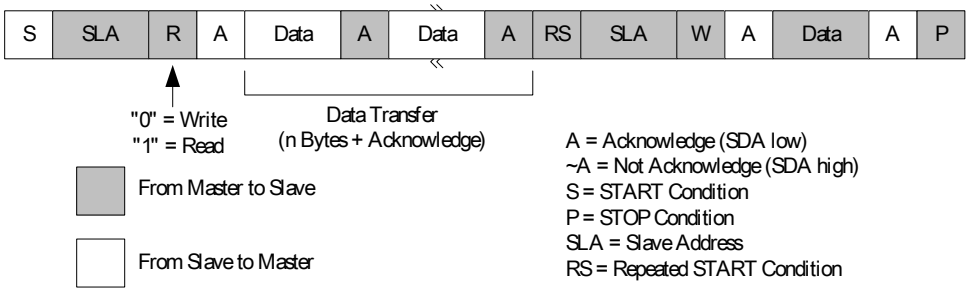
In the Master Receiver Mode, data is received from a slave transmitter. The transfer started in the same manner as in the Master Transmitter Mode. When the START condition has been transmitted, the interrupt service routine must load the slave address and the data direction bit to I^2C Data Register (I2CDATR). The I^2C Status Register (I2CSTAR) must be cleared by firmware, thus the SI bit is automatically cleared, before the data transfer can continue.

When the slave address and data direction bit have been transmitted and an acknowledge bit has been received, the SI bit is set, and the I^2C Status Register (I2CSTAR) will show the status code. The possible status codes are 40h or 48h.



Format of master receiver mode

After a repeated START condition, I^2C may switch to the Master Transmitter Mode.



A master receiver switches to master transmitter after sending restart

9.2.3 Slave Receiver Mode

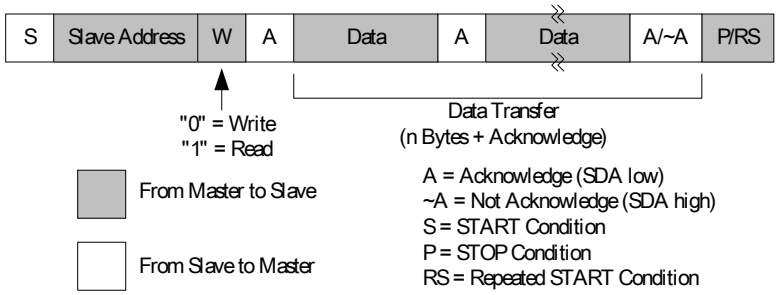
In the Slave Receiver Mode, data bytes are received from a master transmitter. To initialize the Slave Receiver Mode, the user should write the slave address to the Slave Address Register (I2CADRR) and the I^2C Control Register (I2CCTLR) should be configured as follows:

I^2CCTLR	7	6	5	4	3	2	1	0
	I^2CEN	STA	STO	SI	AA	-	-	-
	1	0	0	0	1	-	-	-

I2CEN must be set to 1 to enable I^2C function. AA bit must be set to 1 to acknowledge its own slave address. STA, STO and SI are cleared to 0.

After I2CADRR and I2CCTLR are initialized, the interface waits until it is addressed by its own address followed by the data direction bit which is 0 (W). If

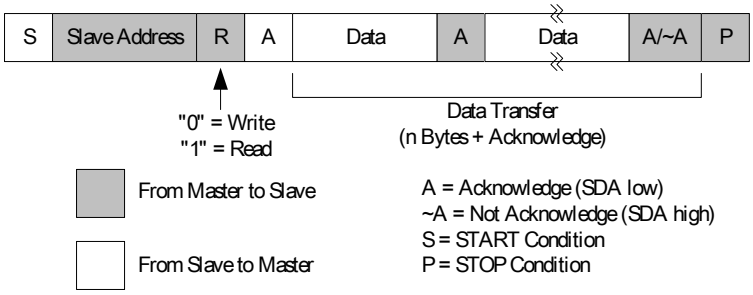
the direction bit is 1 (R), it will enter Slave Transmitter Mode. After the address and the direction bit have been received, the SI bit is set and a valid status code can be read from the I^2C Status Register (I2CSTAR).



Format of slave receiver mode

9.2.4 Slave Transmitter Mode

The first byte is received and handled as in the Slave Receiver Mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted via SDA while the serial clock is input through SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.



Format of slave transmitter mode

In a given application, I^2C may operate as a master and as a slave. In the slave mode, the I^2C hardware looks for its own slave address and the general call address. If one of these addresses is detected, an interrupt is requested. When the micro controller wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible slave action is not interrupted. If bus arbitration is lost in the master mode, I^2C switches to the slave mode immediately and can detect its own slave address in the same serial transfer.

9.3 Status Codes

In this section, the appropriate action to be taken for each status code is shown below.

Master Transmitter Mode

Status code (I2CSTAR)	Status of the I2C bus hardware	Application software response					Next action taken by I2C hardware
		to/from I2CDATR	to I2CCTLR				
			STA	STO	SI	AA	
08H	START condition has been transmitted	Load SLA+W	x	0	0	0	SLA+W will be transmitted
10H	Repeated START condition has been transmitted	Load SLA+W	x	0	0	0	SLA+W will be transmitted
		Load SLA+R	x	0	0	0	I2C will be switched to Master Receiver Mode
18H	SLA+W has been transmitted; ACK has been received	Load data byte	0	0	0	0	Data byte will be transmitted
		No I2CDATR action	1	0	0	0	Repeated START condition will be transmitted
		No I2CDATR action	0	1	0	0	STOP condition will be transmitted; STO flag will be reset
		No I2CDATR action	1	1	0	0	STOP condition followed by a START condition will be transmitted; STO flag will be reset
20H	SLA+W has been transmitted; NACK has been received	Load data byte	0	0	0	0	Data byte will be transmitted
		No I2CDATR action	1	0	0	0	Repeated START condition will be transmitted
		No I2CDATR action	0	1	0	0	STOP condition will be transmitted; STO flag will be reset
		No I2CDATR action	1	1	0	0	STOP condition followed by a START condition will be transmitted; STO flag will be reset
28H	Data byte in I2CDATR has been transmitted; ACK has been received	Load data byte	0	0	0	0	Data byte will be transmitted; ACK will be received
		No I2CDATR action	1	0	0	0	Repeated START condition will be transmitted
		No I2CDATR action	0	1	0	0	STOP condition will be transmitted; STO flag will be reset
		No I2CDATR action	1	1	0	0	STOP condition followed by a START condition will be transmitted; STO flag will be reset

30H	Data byte in I2C has been transmitted; NACK has been received	Load data byte	0	0	0	0	Data byte will be transmitted
		No I2CDATR action	1	0	0	0	Repeated START condition will be transmitted
		No I2CDATR action	0	1	0	0	STOP condition will be transmitted; STO flag will be reset
		No I2CDATR action	1	1	0	0	STOP condition followed by a START condition will be transmitted; STO flag will be reset
38H	Arbitration lost in SLA+(R/W) or data bytes	No I2CDATR action	0	0	0	x	I2C-bus will be released; not addressed slave will be entered
		No I2CDATR action	1	0	0	x	START condition will be transmitted when the bus becomes free

Master Receiver Mode

Status code (I2CSTAR)	Status of the I2C bus hardware	Application software response					Next action taken by I2C hardware
		to/from I2CDATR	to I2CCTLR				
			STA	STO	SI	AA	
08H	START condition has been transmitted	Load SLA+R	x	0	0	0	SLA+R will be transmitted
10H	Repeated START condition has been transmitted	Load SLA+R	x	0	0	0	SLA+R will be transmitted
		Load SLA+W	x	0	0	0	SLA+W will be transmitted; I2C will be switched to Master Transmitter Mode
38H	Arbitration lost in NACK bit	No I2CDATR action	0	0	0	x	I2C will be released; not addressed slave will be entered
		No I2CDATR action	1	0	0	x	START condition will be transmitted when the bus becomes free
40H	SLA+R has been transmitted; ACK has been received	No I2CDATR action	0	0	0	0	Data byte will be received; NACK will be returned
		No I2CDATR action	0	0	0	1	Data byte will be received; ACK will be returned
48H	SLA+R has been transmitted; NACK has been received	No I2CDATR action	1	0	0	0	Repeated START condition will be transmitted
		No I2CDATR action	0	1	0	0	STOP condition will be transmitted; STO flag will be reset
		No I2CDATR action	1	1	0	0	STOP condition followed by a START condition will be transmitted; STO flag will be reset
50H	Data byte has been received; ACK has been returned	Read data byte	0	0	0	0	Data byte will be received; NACK will be returned
		Read data byte	0	0	0	1	Data byte will be received; ACK will be returned
58H	Data byte has been received; NACK has been returned	Read data byte	1	0	0	0	Repeated START condition will be transmitted
		Read data byte	0	1	0	0	STOP condition will be transmitter; STO flag will be reset
		Read data byte	1	1	0	0	STOP condition followed by a START condition will be transmitted; STO flag will be reset

Slave Receiver Mode

Status code (I2CSTAR)	Status of the I2C bus hardware	Application software response					Next action taken by I2C hardware
		to/from I2CDATR	to I2CCTLR				
			STA	STO	SI	AA	
60H	Own SLA+W has been received, ACK has been returned	No I2CDATR action	x	0	0	0	Data byte will be received and NACK will be returned
		No I2CDATR action	x	0	0	1	Data byte will be received and ACK will be returned
68H	Arbitration lost in SLA+(R/W) as master, own SLA+W has been received, ACK returned	No I2CDATR action	x	0	0	0	Data byte will be received and NACK will be returned
		No I2CDATR action	x	0	0	1	Data byte will be received and ACK will be returned
70H	General call address has been received, ACK has been returned	No I2CDATR action	x	0	0	0	Data byte will be received and NACK will be returned
		No I2CDATR action	x	0	0	1	Data byte will be received and ACK will be returned
78H	Arbitration lost in SLA+(R/W) as master, general call address has been received, ACK has been returned	No I2CDATR action	x	0	0	0	Data byte will be received and NACK will be returned
		No I2CDATR action	x	0	0	1	Data byte will be received and ACK will be returned
80H	Previously addressed with own SLA address, data has been received, ACK has been returned	Read data byte	x	0	0	0	Data byte will be received and NACK will be returned
		Read data byte	x	0	0	1	Data byte will be received and ACK will be returned
88H	Previously address with own SLA address, data has been received, NACK has been returned	Read data byte	0	0	0	0	Switched to not addressed SLA mode, no recognition of own SLA or general address
		Read data byte	0	0	0	1	Switched to not address SLA mode, own SLA will be recognized, general call address will be recognized if GCEN = 1
		Read data byte	1	0	0	0	Switched to not address SLA mode, no recognition of own SLA or general address, a START condition will be transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to not addressed SLA mode, own slave address will be recognized, general call address will be recognized if GCEN = 1, a START condition will be transmitted when the bus becomes free
90H	Previously addressed with general call, data has been received, ACK has been returned	Read data byte	x	0	0	0	Data byte will be received ans NACK will be returned
		Read data byte	x	0	0	1	Data byte will be received and ACK will be returned

98H	Previously addressed with general call, data has been received, NACK has been returned	Read data byte	0	0	0	0	Switched to not addressed SLA mode, no recognition of own SLA or general call address
		Read data byte	0	0	0	1	Switched to not addressed SLA mode, own slave address will be recognized, general call address will be recognized if GCEN = 1
		Read data byte	1	0	0	0	Switched to not addressed SLA mode, no recognition of own SLA or general call address, a START condition will be transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to not addressed SLA mode, own slave address will be recognized, general call address will be recognized if GCEN = 1, a START condition will be transmitted when the bus becomes free
A0H	STOP condition or RESTART condition has been received while still addressed as slave	No I2CDATR action	0	0	0	0	Switched to not addressed SLA mode, no recognition of own SLA or general call address
		No I2CDATR action	0	0	0	1	Switched to not addressed SLA mode, own slave address will be recognized, general call address will be recognized if GCEN = 1
		No I2CDATR action	1	0	0	0	Switched to not addressed SLA mode, no recognition of own SLA or general call address, a START condition will be transmitted when the bus becomes free
		No I2CDATR action	1	0	0	1	Switched to not addressed SLA mode, own slave address will be recognized, general call address will be recognized if GCEN = 1, a START condition will be transmitted when the bus becomes free

Slave Transmitter Mode

Status code (I2CSTAR)	Status of the I2C bus hardware	Application software response					Next action taken by I2C hardware
		to/from I2CDATR	to I2CCTLR				
			STA	STO	SI	AA	
A8H	Own SLA+R has been received, ACK has been returned	Load data byte	x	0	0	0	Data byte will be transmitted
		Load data byte	x	0	0	1	Data byte will be transmitted
B0H	Arbitration lost in SLA+(R/W) as master, own SLA+R has been received, ACK has been returned	Load data byte	x	0	0	0	Data byte will be transmitted
		Load data byte	x	0	0	1	Data byte will be transmitted
B8H	Data byte in I2CDATR has been transmitted, ACK has been received	Load data byte	x	0	0	0	Data byte will be transmitted
		Load data byte	x	0	0	1	Data byte will be transmitted
C0H	Data byte in I2CDATR has been transmitted, NACK has been received	No I2CDATR action	0	0	0	0	Switched to not addressed SLA mode, no recognition of own SLA or general call address
		No I2CDATR action	0	0	0	1	Switched to not addressed SLA mode, own slave address will be recognized, general call address will be recognized if GCEN = 1
		No I2CDATR action	1	0	0	0	Switched to not addressed SLA mode, no recognition of own SLA or general call address, a START condition will be transmitted when the bus becomes free
		No I2CDATR action	1	0	0	1	Switched to not addressed SLA mode, own slave address will be recognized, general call address will be recognized if GCEN = 1, a START condition will be transmitted when the bus becomes free

10. SSP

The PS1000 has one SSP interface. This interface is compatible with TI serial peripheral interface specification.

This SSP interface is controlled by the SSPCFG / SSPCKL / SSPDXR / SSPRXR / SSPSTA registers. These registers are mapped at the SFR memory space. The setting for these register are

SSPCFG1 (SFR 0xBB)							
B7	B6	B5	B4	B3	B2	B1	B0
N/A	TXEN	RXEN	TXM	MCM	FSM	FO	DLB

TXEN: SSP TX I/F Enable

0: SSP TX I/F Disable (Default)

1: SSP TX I/F Enable

RXEN: B5 SSP RX I/F Enable

0: SSP RX I/F Disable (Default)

1: SSP RX I/F Enable

TXM : Frame Sync Mode (TXM)

0: FSX is External sync

1: FSX is internal sync

MCM: CLK Mode (MCM)

0: CLKX comes from External Clock (default)

1: CLKX comes from Internal Clock

FSM: Frame Sync Mode (FSM)

0: Continuous mode (default)

1: Burst Mode

FO: Data Length Control (FO)

0: 16 bits

1: 8 bits

DLB: Digital loop-back Control

0: Disable

1: Enable

SSPCFG2 (SFR 0xBC)							
B7	B6	B5	B4	B3	B2	B1	B0

CKEN	CLKDIV

CLKEN: Enable SSP clock divider

0: Disable, default MCUCLK/4 (same as N = 0)

1: Enable, MCUCLK/n

CLKDIV: SSP clock source divider

N: SSPCLK = MCUCLK / (2*(N+1))

SSPDXRL (SFR 0xAC)							
B7	B6	B5	B4	B3	B2	B1	B0
D7	D6	D5	D4	D3	D2	D1	D0

SSPDXRH (SFR 0xAB)							
B7	B6	B5	B4	B3	B2	B1	B0
D15	D14	D13	D12	D11	D10	D9	D8

SSPRXRL (SFR 0xAE)							
B7	B6	B5	B4	B3	B2	B1	B0
D7	D6	D5	D4	D3	D2	D1	D0

SSPRXRH (SFR 0xAD)							
B7	B6	B5	B4	B3	B2	B1	B0
D15	D14	D13	D12	D11	D10	D9	D8

SSPSTA (SFR 0xAF)							
B7	B6	B5	B4	B3	B2	B1	B0
XINT	XRDY	XEMP	XLoad	RINT	RRDY	RSRFULL	Read

XINT: Transmitter interrupt, only for few cycle

XRDY: '1' indicate the transmitter is ready for transmit.

XEMP: Transmit buffer is empty; it can load the new data to transmitter.

XLoad

RINT: Receiver interrupt, only for little cycle.

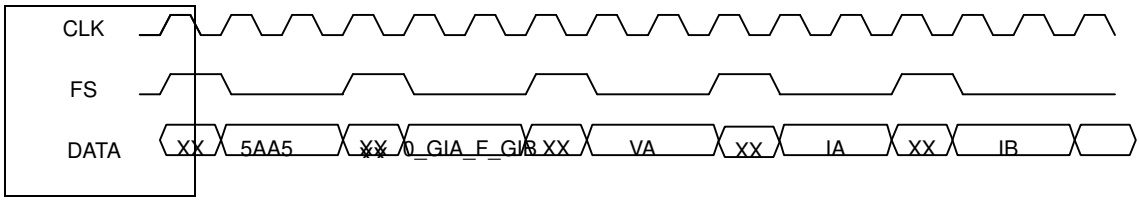
RRDY: '1' indicate the received data from SSP bus. The DRR register must be read immediately.

RSRFULL: 1' indicate the receiver buffer overrun.

Read: Set as '1' to indicate the DRR already read, this bit will auto clear when the RRDY will return to '0'

The SSP interface can control by DSP or MCU. It can select by the DSPCFG register (Bit5). When the SSP is controlled by the DSP, it only can be the TX mode. It will output the 3 channel ADC data and 2 current gain information.

The following diagram shows the SSP output waver under the DSP control mode.



11. RTC

The PS1000 has one RTC (Real-Time Clock) circuit. It can keep one clock count reference base one 32.768 KHz crystal.

This RTC circuit can make a different configuration base on the RTCCFG register.

RTCCFG (0xFE28)							
B7	B6	B5	B4	B3	B2	B1	B0
1	UPD	**RTCADJ[5:0]**					

UPD: RTC update

1: Update

0: no update (Default)

RTCADJ[5:0]: RTC Frequency Adjust (Hz), 2's complement

…

000010: RTCCLK = 32768 + 2Hz

000001: RTCCLK = 32768 + 1Hz

000000: RTCCLK = 32768Hz

111111: RTCCLK = 32768 - 1Hz

111110: RTCCLK = 32768 - 2Hz

…

The RTC circuit has one clock divider which can adjust the RTC clock rate used for RTC clock bias tuning. This divider must control very carefully to prevent the RTC clock error.

RTCCFG2(0xFE3C)							
B7	B6	B5	B4	B3	B2	B1	B0
RTCTM[2:0]			**x**	**RTCFADJ[3:0]**			

This register is used for configure the RTC test mode and fine adjust the RTC frequency.

RTCTM[2:0] RTC Test Mode control

Must always set as 000

RTCFADJ[3:0] RTC clock tuning fraction part (RTCAdj)

0000RTCAdj - 0/16Hz
0001RTCAdj - 1/16Hz
0010RTCAdj - 2/16Hz
0011 RTCAdj - 3/16Hz
0100RTCAdj - 4/16Hz
0101RTCAdj - 5/16Hz
0110 RTCAdj - 6/16Hz
0111 RTCAdj - 7/16Hz
1000RTCAdj - 8/16Hz
1001RTCAdj - 9/16Hz
1010RTCAdj - 10/16Hz
1011 RTCAdj - 11/16Hz
1100 RTCAdj - 12/16Hz
1101 RTCAdj - 13/16Hz
1110 RTCAdj - 14/16Hz
1111 RTCAdj - 15/16Hz

The RTC clock information can read from several RTC registers. These registers are RTCYear, RTCMonth, RTCDay, RTCWeek, RTCHour, RTCMinute and RTCSec. These registers will auto updated base one the RTC condition. The RTCYear value will be 0 to 255. It is represent as 2000 to 2255 DC.

RTCYear(0xFE10)							
B7	B6	B5	B4	B3	B2	B1	B0
Year (0 ~ 255)							

For the RTCMonth, the value will be 1 to 12. It is represent the Jan. to Dec.

RTCMonth(0xFE11)							
B7	B6	B5	B4	B3	B2	B1	B0
x	x	x	x	Month (1 ~ 12)			

For the RTCDay, the value will be 1 to 31. The last day will depends on the Year and Month.

wRTCDay(0xFE12)							
B7	B6	B5	B4	B3	B2	B1	B0
x	x	x	Day (1 ~ 31)				

For RTCWeek, the value will be 0 ~ 6. It is represent as Sunday to Saturday. The RTCWeek will not relative to which Year, Month and Day. It must set by user. The RTC circuit will keep the Week counting when the Day count is updated.

RTCWeek(0xFE13)							
B7	B6	B5	B4	B3	B2	B1	B0
x	x	x	x	x	Week (0~6)		

For RTCHour, the value will be 0 ~ 23.

RTCHour(0xFE14)							
B7	B6	B5	B4	B3	B2	B1	B0
x	x	x	Hour (0 ~ 23)				

For RTCMinute, the value will be 0 ~ 59.

RTCMinutes(0xFE15)							
B7	B6	B5	B4	B3	B2	B1	B0
x	x	Minute(0 ~ 59)					

For RTCSec, the value will be 0 ~ 59.

RTCSec(0xFE16)							
B7	B6	B5	B4	B3	B2	B1	B0
x	x	Second (0 ~ 59)					

In order to initialize the RTC value. It can set the initial RTC value in the RTC write registers (wRTCYear, wRTCMonth, wRTCDay, wRTCWeek, wRTCHour, wRTCMinutes and wRTCSec). The setting format is same as RTCYear, RTCMonth, RTCHour, RTCMinute and RTCSec except the RTCDay and RTCWeek. That is combine in one wRTCDay Register

wRTCDay(0xFE3B)							
B7	B6	B5	B4	B3	B2	B1	B0
Week (0~6)			Day (1 ~ 31)				

It is different as RTC information register. After setting the initial value into the RTC write register, it must trigger the RTC update flag (0 - 1 – 0). The RTC circuit will update the RTC information register base on the RTC write register when detect the RTC update flag is toggle.

12. LCD

The PS1000 has build-in one LCD driver. It can driver one 40x4 LCD panel. This LCD circuit is controlled by setting the LCDCFG and LCDDIV register.

LCDCFG(0xFE26)							
B7	B6	B5	B4	B3	B2	B1	B0
CTRL		MODE		SEG		COM	

CTRL: LCD IF Mode Control
- 00: LCD IF Disable (Default)
- 01: Test Mode
- 10: Blank Display
- 11: RAM Data Display

MODE: LCD Mode Control
- 00: Bias Mode
- 01: Static mode
- 1x: Not define

SEG: LCD Segment Control
- 00: 10 Segments On
- 01: 20 Segments On
- 10: 30 Segments On
- 11: 40 Segments On

COM: LCD COM Control
- 00: COM0 Static
- 01: COM0~COM1 (1/2 Duty)
- 10: COM0~COM2 (1/3 Duty)
- 11: COM0~COM3 (1/4 Duty)

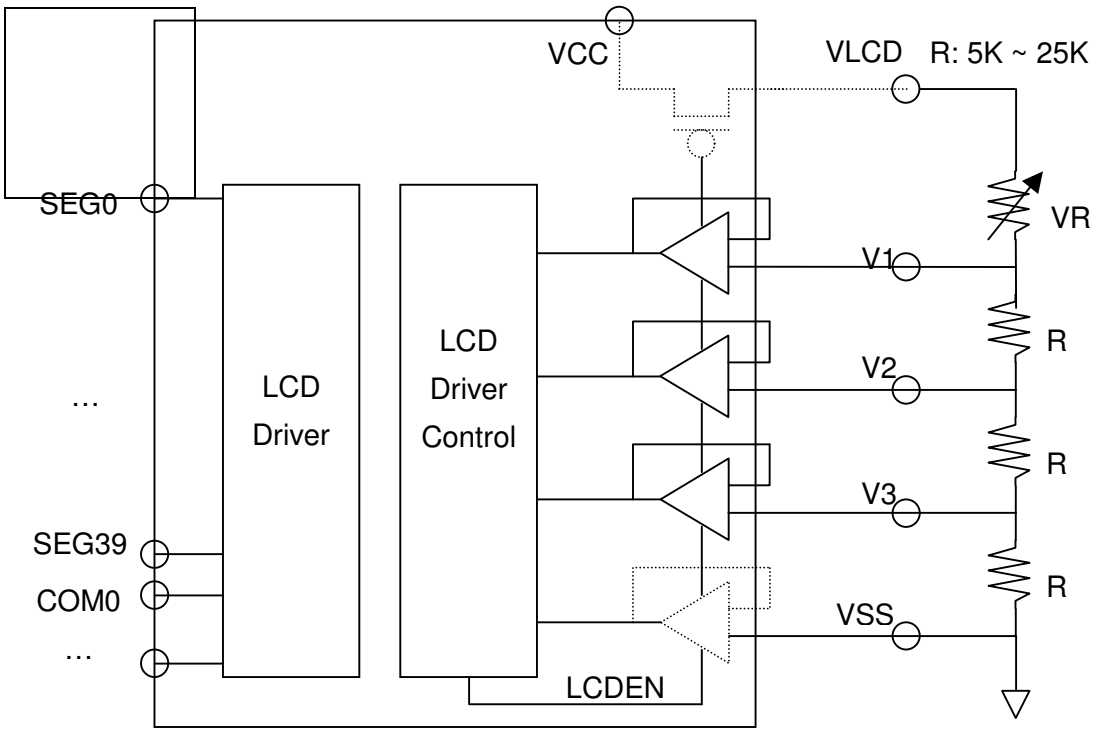
LCDDIV							
B7	B6	B5	B4	B3	B2	B1	B0
x	Divider						

Divider: LCD Frame frequency N

Frame Frequency 4*1024/ (duty*N)

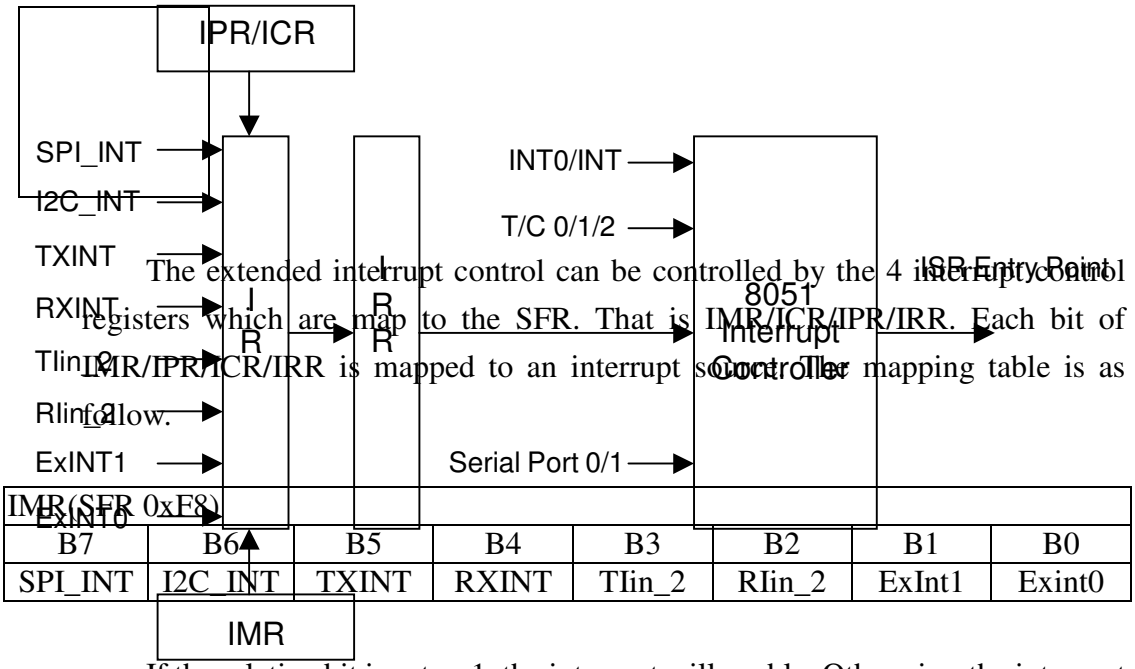
Segment Frequency 4*1024/N

User can set the LCD display data at the LCD buffer from LCD0 ~ LCD19. The LCD controller will automatic load the LCD0~LCD19 data and display on the LCD screen. The LCD controller also has one LCD bias circuit. It can generate the LCD bias for the COM and SEG driving. User can change the bias voltage for 1/2, 1/3 or 1/4 bias control. Here is the bias circuit block diagram.



13. Interrupt

The PS1000 has 8 extended interrupt input source for the SPI, I2C, SSP and I/O interface. The extended interrupt block diagram is shown as figure 2.



B7	B6	B5	B4	B3	B2	B1	B0
SPI_INT	I2C_INT	TXINT	RXINT	TIin_2	RIin_2	ExInt1	Exint0

The extended interrupt control can be controlled by the 4 interrupt control registers which are map to the SFR. That is IMR/ICR/IPR/IRR. Each bit of IMR/IPR/ICR/IRR is mapped to an interrupt source. The mapping table is as follow.

If the relative bit is set as 1, the interrupt will enable. Otherwise, the interrupt will disable. For each interrupt source, it can be level trigger or edge trigger. It is controlled by the ICR register. When the bit is set as 1, the relative interrupt source will be LEVEL trigger; otherwise, it will be EDGE trigger.

For each interrupt source, it also can set as high level or low level (rising edge or falling edge) trigger. It is controlled by the IPR. When the IPR is set as 1, the relative interrupt source is set as HIGH level (RISING edge) trigger, otherwise, it will set as LOW level (FALLING edge) trigger.

Whenever the interrupt is input, if the relative IMR is enabled, the IRR will be set as '1', it indicates the relative interrupt is inputted and switch the MCU program to the Interrupt Service Routine (ISR). The interrupt table is shown as following table. The extended interrupt ISR must base on the IRR register to decide what kind of task need to do and extended interrupt ISR also can decided the priority for these 8 extended interrupt source by the ISR.

Interrupt Type	Entry Point
External INT0	8‘b00000011 (8’h03)
Timer/Counter 0	8'b00001011 (8’h0B)
External INT1	8'b00010011 (8’h13)
Timer/Count 1	8'b00011011(8’h1B)
Serial Port2	8'b00100011 (8’h23)
Timer/Counter 2	8'b00101011 (8’h2B)
Extend INT	8'b00110011 (8’h33)
Serial Port 1	8'b00111011 (8’h3B)

14. Power Management

In PS1000, it design a lot of power management control method. Most of the functional block can turn-on/off individually. The MCU/DSP/ADC also can operate on a lot of different clock rate. It is programmable by setting the clock diver counter. It can make the power management more easily.

The following blocks have its own enable configuration setting.

Functional Block	Enable Setting	Operation Current(3.3V)	Operation Current (2.5V)
Fully Operation		26.17mA	32.95mA
DSP	DSPCFG[7]=0	1.32mA	
LCD	LCDCFG[7]=0	0.2mA	
RTC	RTCCFG[7]=0		7uA
AGC	AGCCFG[7]=0	0.1mA	
ADC	ADCCFG[7]=0	7.77mA	
Temperature Sensor	SARCFG[7]=0	0.6mA	
MCU	Power Down	2.33mA	3.73mA

For the MCU and DSP, when you change the different operation frequency, it also can help to save the power consumption or increase the MCU/DSP performance. Here is the reference table for MCU/DSP power consumption for different operation condition.

MCUDIV[3:0] DSPDIV[3:0]		Crystal (24MHz)	MCU Power Consumption(2.5V)	DSP Power Consumption(2.5V)
0000	SCLK / 1	24.00	**26.24mA**	**4.92mA**
0001	SCLK / 2	12.00	**11.57mA**	**2.34mA**
0010	SCLK / 3	8.00	**7.66mA**	**1.57mA**
0011	SCLK / 4	6.00	**5.62mA**	**1.19mA**
0100	SCLK / 5	4.80	**4.5mA**	**0.95mA**
0101	SCLK / 6	4.00	**3.81mA**	**0.8mA**
0110	SCLK / 7	3.43	N/A	N/A
0111	SCLK / 8	3.00	**2.8mA**	**0.6mA**
1000	SCLK / 9	2.67	N/A	N/A
1001	SCLK / 10	2.40	N/A	N/A
1010	SCLK / 11	2.18	N/A	N/A
1011	SCLK / 12	2.00	**1.81mA**	**0.39mA**
1100	SCLK / 13	1.85	N/A	N/A
1101	SCLK / 14	1.71	N/A	N/A
1110	SCLK / 15	1.60	N/A	N/A
1111	SCLK / 16	1.50	**1.42mA**	**0.29mA**

15. PIN Mapping

LQFP-128 Package

Left Side

Pin#	Name	Type	Description
1	P3.6	I/O	8051 P3 I/O port bit 6 (WR_)
2	P3.7	I/O	8051 P3 I/O port bit 7 (RD_)
3	VSSA	Ground	Analog Ground
4	VCM1	O	Reference output
5	IBM	I	IBM input
6	IBP	I	IBP input
7	IAP	I	IAP input
8	IAM	I	IAM input
9	VCC3A	Power (3.3V)	3.3V Analog Power supply
10	VAM	I	VAM input
11	VAP	I	VAP input
12	VCM2	O	Reference output
13	VSSA	Ground	Analog Ground
14	VCCA	Power (3,3V)	Analog Power Supply
15	RST	I	Chip Reset active
16	EA	I	8051 EA control signal
17	MODE0	I	Mode selection bit 0 (LSB)
18	MODE1	I	Mode selection bit 1
19	MODE2	I	Mode selection bit 2 (MSB)
20	VREG25	O	Regulator 2.5V output
21	VCC3A	Power (3.3V)	3.3V Analog Power supply
22	GNDIO/GNDK	Ground	Ground
23	VCC3A	Power (3.3V)	3.3V I/O Power supply
24	VLCD	O	LCD bias power supply output
25	V3	I	LCD bias input 3
26	V2	I	LCD bias input 2
27	V1	I	LCD bias input 1
28	COM0	O	LCD COM output
29	COM1	O	LCD COM output
30	COM2	O	LCD COM output
31	COM3	O	LCD COM output
32	SEG0	O	LCD segment output

Bottom Side

33	SEG1	O	LCD segment output
34	SEG2	O	LCD segment output
35	SEG3	O	LCD segment output
36	SEG4	O	LCD segment output
37	SEG5	O	LCD segment output
38	SEG6	O	LCD segment output
39	VCCK	Power(2.5V)	2.5V Core power
40	SEG7	O	LCD segment output
41	SEG8	O	LCD segment output
42	SEG9	O	LCD segment output
43	SEG10	O	LCD segment output
44	SEG11	O	LCD segment output
45	SEG12	O	LCD segment output
46	SEG13	O	LCD segment output
47	SEG14	O	LCD segment output
48	SEG15	O	LCD segment output
49	SEG16	O	LCD segment output
50	SEG17	O	LCD segment output
51	SEG18	O	LCD segment output
52	GND	Ground	Ground
53	SEG19	O	LCD segment output
54	SEG20	O	LCD segment output
55	SEG21	O	LCD segment output
56	SEG22	O	LCD segment output
57	SEG23	O	LCD segment output
58	SEG24	O	LCD segment output
59	SEG25	O	LCD segment output
60	SEG26	O	LCD segment output
61	SEG27	O	LCD segment output
62	SEG28	O	LCD segment output
63	VCCK	Power(2.5V)	2.5V Core power
64	SEG29	O	LCD segment output

Right Side

65	SEG30	O	LCD segment output
66	SEG31	O	LCD segment output
67	SEG32	O	LCD segment output
68	SEG33	O	LCD segment output
69	SEG34	O	LCD segment output
70	SEG35	O	LCD segment output
71	SEG36	O	LCD segment output
72	SEG37	O	LCD segment output
73	SEG38	O	LCD segment output
74	SEG39	O	LCD segment output
75	VCCIO	Power (3.3V)	3.3V I/O Power supply
76	VCCK	Power(2.5V)	2.5V Core power
77	SO	O	SPI SO signal
78	SCLK	O	SPI CLK signal
79	P0.0	I/O	8051 P0 I/O port0 bit 0
80	P0.1	I/O	8051 P0 I/O port0 bit 1
81	P0.2	I/O	8051 P0 I/O port0 bit 2
82	P0.3	I/O	8051 P0 I/O port0 bit 3
83	P0.4	I/O	8051 P0 I/O port0 bit 4
84	P0.5	I/O	8051 P0 I/O port0 bit 5
85	P0.6	I/O	8051 P0 I/O port0 bit 6
86	P0.7	I/O	8051 P0 I/O port0 bit 7
87	P1.0	I/O	8051 P1 I/O port1 bit 0
88	P1.1	I/O	8051 P1 I/O port1 bit 1
89	P1.2	I/O	8051 P1 I/O port1 bit 2(RxD1)
90	VCCRTC	Power(2.5V)	RTC power supply (2.5V)
91	RTCXI	I	RTC crystal input
92	RTCXO	O	RTC crystal output
93	RTCGND	Ground	RTC Crystal ground
94	XTLO	O	Crystal output
95	XTLI	I	Crystal input
96	VCCK	Power(2.5V)	Crystal power supply (2.5V)

Top Side

97	P1.3	I/O	8051 P1 I/O port1 bit 3(TxD1)
98	P1.4	I/O	8051 P1 I/O port1 bit 4(RxD2)
99	P1.5	I/O	8051 P1 I/O port1 bit 5(TxD2)
100	P1.6	I/O	8051 P1 I/O port2 bit 6
101	P1.7	I/O	8051 P1 I/O port2 bit 7
102	P2.0	I/O	8051 P2 I/O port2 bit 0
103	P2.1	I/O	8051 P2 I/O port2 bit 1
104	P2.2	I/O	8051 P2 I/O port2 bit 2
105	P2.3	I/O	8051 P2 I/O port2 bit 3
106	P2.4	I/O	8051 P2 I/O port2 bit 4
107	VCCIO	Power (3.3V)	3.3V I/O Power supply
108	P2.5	I/O	8051 P2 I/O port2 bit 5
109	SCL	I/O	I2C clock
110	SDA	I/O	I2C Address/Data
111	GNDIO/GNDK	Ground	Ground
112	P2.6	I/O	8051 P2 I/O port2 bit 6
113	SI	I	SPI SI input
114	P2.7	I/O	8051 P2 I/O port2 bit 7
115	P3.0	I/O	8051 P3 I/O port3 bit 0(RxD0)
116	P3.1	I/O	8051 P3 I/O port3 bit 1(TxD0)
117	P3.2	I/O	8051 P3 I/O port3 bit 2
118	PSEN(P3.4)	I/O	8051 PSEN control pin (opt for P3.4)
119	P3.3(P3.5)	I/O	8051 P3 I/O port bit 3(opt for P3.5)
120	ALE	I/O	8051 ALE control signal
121	SPICS	O	SPI CS control signal
122	VCCIO	Power (3.3V)	3.3V I/O Power supply
123	VCCK	Power(2.5V)	Crystal power supply (2.5V)
124	FSX	I/O	SSP FSX
125	DX	I/O	SSP DX
126	CLK	I/O	SSP CLK
127	DR	O	SSP DR
128	FSR	O	SSP FSR

Package Specification