ReadyBoard™ 800
Single Board Computer
Reference Manual

P/N 5001738B Revision B

Notice Page

NOTICE

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REVISION HISTORY

Revision	Reason for Change	Date
A, A	Initial Release	Oct/04
B, A	Board Revision/Updates	Dec/04
B, B	BIOS Updates/Changes	Feb/06

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Audience Assumptions

This reference manual is for the person who designs computer related equipment, including but not limited to hardware and software design and implementation of the same. Ampro Computers, Inc. assumes you are qualified in designing and implementing your hardware designs and its related software into your prototype computer equipment.

Contents

List of Figures

List of Tables

Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the ReadyBoard™ 800 single board computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- ReadyBoard 800 Specifications
- Environmental requirements
- Major integrated circuits (chips) and features implemented
- ReadyBoard 800 connector/pin numbers and definition
- BIOS Setup information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

Reference Material

The following list of reference materials may be helpful for you to complete your design successfully. Most of this reference material is also available on the Ampro web site in the Embedded Design Resource Center. The Embedded Design Resource Center was created for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience.

Specifications

- EPIC Specification Revision 1.0, March 22, 2004

  Web site: http://www.ampro.com/RP/EPIC_Specification_v1.0.pdf
- PC/104™ Specification Revision 2.5, November 2003
- PC/104-Plus™ Specification Revision 2.0, November 2003
- PCI-104™ Specification Revision 1.0, November 2003

  For latest revision of the PC/104, PC/104-Plus, and PCI-104 specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org
- PCI™ 2.3 Specifications

  For latest revision of the PCI specifications, contact the PCI Special Interest Group Office at:

  Web site: http://www.pcisig.com
- Compact Flash Specifications Revision 3.0, December 2004

  For the latest revision of the compact flash specifications, contact the Compact Flash association at:

  Web site: http://www.CompactFlash.org

Chip specifications used on the ReadyBoard 800:

- Intel Corporation and the Pentium® M 738, Celeron® M 373, or Celeron® M processors

  Web site: http://www.intel.com/design/mobile/datashts/302189.htm (30218908.pdf)

  Web site: http://www.intel.com/design/mobile/datashts/303110.htm (30311007.pdf)

  Web site: http://www.intel.com/design/intarch/datashts/30175301.pdf

- Intel Corporation and the chips, 82855GME and 82801DBM, used for the Northbridge/Video controller and Southbridge respectively.

  Web site: http://www.intel.com/design/chipsets/datashts/25261505.pdf

  Web site: http://www.intel.com/design/mobile/datashts/25233701.pdf

- Winbond Electronics, Corp. and the W83627HF chip used for the secondary I/O controller

  Web site: http://www.winbond-usa.com/products/winbond_products/pdfs/PCIC/627hf.pdf

- Intel Corporation and the 82551ER, used for the Ethernet controller.

  Web site: http://developer.intel.com/design/network/datashts/82551er_ds.htm (82551er_ds.pdf)

- Intel Corporation and the 82541GI, used for the Gigabit Ethernet controller.

  Web site: http://www.intel.com/design/network/datashts/82541gi_ei.pdf

NOTE	If you are unable to locate the datasheets using the links provided, go to the manufacturer's web site where you can perform a search using the chip datasheet number or name listed, including the extension, (htm for web page, pdf for files name, etc.

Related Ampro Products

The following items are directly related to successfully using the Ampro product you have just purchased or plan to purchase. Ampro highly recommends that you purchase and utilize a ReadyBoard 800 QuickStart Kit to do your project development.

ReadyBoard 800 Support Products

- ReadyBoard 800 QuickStart Kit (QSK)

  The QuickStart Kit includes the ReadyBoard 800, DDR SODIMM memory, a cable kit, documentation, and the ReadyBoard 800 Documentation and Support Software (Doc & SW) CD-ROM.

- ReadyBoard 800 Documentation and Support Software CD-ROM

  The ReadyBoard 800 Documentation and Software (Doc & SW) CD-ROM is provided with the ReadyBoard 800 QuickStart Kit. The CD-ROM includes all of the ReadyBoard 800 documentation, including this Reference Manual and the ReadyBoard 800 QuickStart Guide in PDF format, the software utilities, board support packages, and drivers for the unique devices used with Ampro supported operating systems.

- ReadyBox™ Family

  The ReadyBox family includes a series of enclosures with varying sizes that accept all of Ampro's ReadyBoard products. These ReadyBox enclosures allow you to install your ReadyBoard product with your preferred set of options for a rapidly deployable system for OEM production volumes. The ReadyBox family provides all of the standard PC style edge connectors of the ReadyBoard products, which are accessible on the front I/O panel, including three audio connectors, and a slot for a compact flash card. Depending on the enclosure, you may add PC-style connectors for two additional serial ports (4 total), two additional USB ports (4 total), and one parallel port connector. You can add up to tow PC/104, PC/104-Plus, or PCI-104 expansion boards to the ReadyBox ATX and 2U enclosures. The ReadyBox ATX is powered by an internal 150 W ATX power supply and the ReadyBox 1U and 2U are powered by a AC-DC converter or a customer-specific DC power supply. A mounting location is provided for the internal 2 ½" hard disk drive and the external mounting brackets and feet are provided as accessories.. Optional rack mounting hardware and an optional +12 VDC Brick power supply are provided for the ReadyBox 1U and 2U enclosures..

- ReadySystem™ Family

  The ReadySystem family is a series of high performance, low cost turnkey systems that come with a ReadyBoard 800 installed into a particular size ReadyBox enclosure with a specific size SODIMM, and a 2 ½" hard disk drive pre-loaded with one of Ampro's supported operating systems (Linux®, etc.). The ReadySystem provides all of the ReadyBoard's standard PC style connectors accessible on the front I/O panel, including three audio connectors and a slot for a compact flash card. Depending on the enclosure, you may add PC-style connectors for two additional serial ports (4 total), two additional USB ports (4 total), and one parallel port connector. You can install up to two PCI-104 or PC/104-Plus expansion boards into the ReadySystem ATX and 2U enclosures. A ReadySystem comes pre-tested and ready for application loading to provide customers with the fastest possible deployment of their embedded applications. Refer to the specific ReadySystem Users Guide on the web site, or on the ReadyBoard 800 Documentation and Support Software (Doc & SW) CD-ROM for more information.

Other ReadyBoard Products

- ReadyBoard™ 700 – This EPIC single board computer (SBC) is used for high volume embedded applications and provides designers with a low cost, low-power choice of high performance Intel® 933 MHz Low Voltage (LV) Pentium® III, 650 MHz LV Celeron®, or 400 MHz Ultra Low Voltage (ULV) Celeron® processors. In addition to the standard ReadyBoard features (4.5" x 6.5" form factor, PC-style connectors, PC/104-Plus, +5 volt only power, etc.), the ReadyBoard 700 supports two primary IDE drives, includes one compact flash socket on secondary IDE, eight GPIO pins, four RS-232 serial ports with the RS-485/RS-422 option for two ports, dual 10/100BaseT Ethernet interfaces, four USB v1.1 ports, IrDA, and AC'97 audio ports. It also supports up to 512 MB of SDRAM in an SODIMM socket, up to 32 MB UMA of AGP 4X video with built-in LVDS, CRT, and 36-bit TFT support, and Ampro embedded BIOS extensions, such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.

- ReadyBoard™ 710 – This EPIC single board computer (SBC) used for high volume embedded applications provides designers with a low cost, low-power alternative to the high cost of high performance processors. Through the use of advanced chipset technology with the Intel 650 MHz Low Voltage (LV) Celeron CPU, the ReadyBoard 710 provides DDR memory, USB 2.0 ports, Gigabit Ethernet. In addition to the standard ReadyBoard features (4.5" x 6.5" form factor, PC-style connectors, PCI-104, +5 volt only power, etc.), the ReadyBoard 710 supports two primary IDE drives, includes one compact flash socket on secondary IDE, eight GPIO pins, four RS-232 serial ports with the RS-485/RS-422 option for two ports, 10/100BaseT and 1000BaseT Gigabit Ethernet interfaces, four USB 2.0 ports, IrDA, and AC'97 audio solution. It also supports up to 1 GB of DDR SDRAM in an SODIMM socket, up to 64 MB UMA of AGP 8X equivalent video with built-in LVDS, CRT, and 24-bit TFT support, and Ampro embedded BIOS extensions, such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.

Other Ampro Products

- CoreModule™ Family – These complete embedded-PC subsystems on single PC/104 or PC/104-Plus form-factor (3.6"x3.8") modules feature 486, Celeron, and Celeron M CPUs. Each CoreModule includes a full complement of PC core logic functions, plus disk controllers, and serial and parallel ports. Most modules also include CRT and flat panel graphics controllers and/or an Ethernet interface. The CoreModules also come with built-in extras to meet the critical reliability requirements of embedded applications. These include onboard solid state disk compatibility, watchdog timer, smart power monitor, and Ampro embedded BIOS extensions.
- ETX Family – These high-performance, compact, rugged Computer-on-Module (COM) solutions use various x86 processors from Celeron to Pentium M CPUs in an ETX Revision 2.7 form factor to plug into your custom baseboard. Each ETX module provides standard peripherals, including dual Ultra/DMA 33/66/100 IDE, floppy drive interface, PCI bus, ISA bus, serial, parallel, PS/2 keyboard and mouse interfaces, 10/100BaseT Ethernet, USB ports, Video, and AC'97 audio. ETX modules support up to 512 MB (or more) of SODIMM DRAM. A 50% thicker PCB, Ampro embedded BIOS extensions, such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console, and optional –40°C to +85°C operation are available to meet your rugged application requirements.
- LittleBoard™ Family – These high-performance, highly integrated single-board computers use the EBX form factor (5.75"x8.00"), and are available with the Intel Pentium M, Celeron M, Pentium III, or Celeron processors. The EBX-compliant LittleBoard single-board computers offer functions equivalent to a complete laptop or desktop PC system, plus several expansion cards. Built-in extras to meet the critical requirements of embedded applications include onboard solid state disk capability, watchdog timer, smart power monitor, and Ampro embedded BIOS extensions.
- MightyBoard™ Family – These low-cost, high-performance single-board computers (SBC) use the Mini-ITX form factor (6.7" x 6.7") and are available with Intel Celeron M and Pentium M processors. MightyBoard products offer the equivalent functions of a complete laptop or desktop PC system, including DDR memory, high performance graphics, USB 2.0, Gigabit Ethernet, plus standard PCI expansion capability in one card slot. Ampro includes configuration control and embedded BIOS extensions such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.
- MiniModule™ Family – This extensive line of peripheral interface modules compliant with PC/104 and PC/104-Plus standards can be used with Ampro CoreModule, LittleBoard, and ReadyBoard single board computers to configure embedded system solutions. Ampro's highly reliable MiniModule products currently support USB 2.0, IEEE 1394 (Firewire), Ethernet, PC Card expansion, analog/data acquisition, additional RS-232/RS-485 serial ports, and general-purpose I/O (GPIO).

Chapter 2 Product Overview

This introduction presents general information about the EPIC Architecture and the ReadyBoard 800 single board computer (SBC). After reading this chapter you should understand:

- EPIC Architecture
- ReadyBoard 800 architecture
- ReadyBoard 800 features
- Major components
- Connectors
- Specifications

EPIC Architecture

In 2004, five companies collaborated to fill the void between the EBX size and the PC/104 size with a new industry standard form factor (115 mm x 165 mm, or 4.5" x 6.5") called "Embedded Platform for Industrial Computing™ (EPIC)." The EPIC standard principally defines physical size, mounting hole pattern, and power connector locations. It does not specify processor type or electrical characteristics. There are recommended connector placements for serial, parallel, Ethernet, graphics, and memory expansion. This embedded SBC standard ensures that embedded system OEMs can standardize their designs and that full featured embedded computing solutions can be designed into even more space constrained environments than ever before.

The EPIC standard boasts the same highly flexible and adaptable system expansion as EBX, allowing easy and modular addition of functions such as Firewire or wireless networking not usually contained in standard product offerings. The EBX system expansion is based on popular existing industry standards, PC/104™, PC/104-Plus™, and PCI-104™. PC/104 places the ISA bus on compact 3.6" x 3.8" modules with self-stacking capability. PC/104-Plus adds the power of a PCI bus to PC/104 while retaining the basic form factor, but PCI-104 expansion cards only provide the PCI Bus to the PC/104 form factor. Using PC/104 expansion cards, an EPIC board can be easily adapted to meet a variety of embedded applications. See Figures 2-1 and 2-2.

The EPIC standard also brings stability to the mid-sized embedded board market and offers OEMs assurance that a wide range of products will be available from multiple sources – now and in the future. The EPIC specification is freely available to all interested companies, and may be used without licenses or royalties. For further technical information on the EPIC standard, visit the web site at http://www.epic-sbc.org.

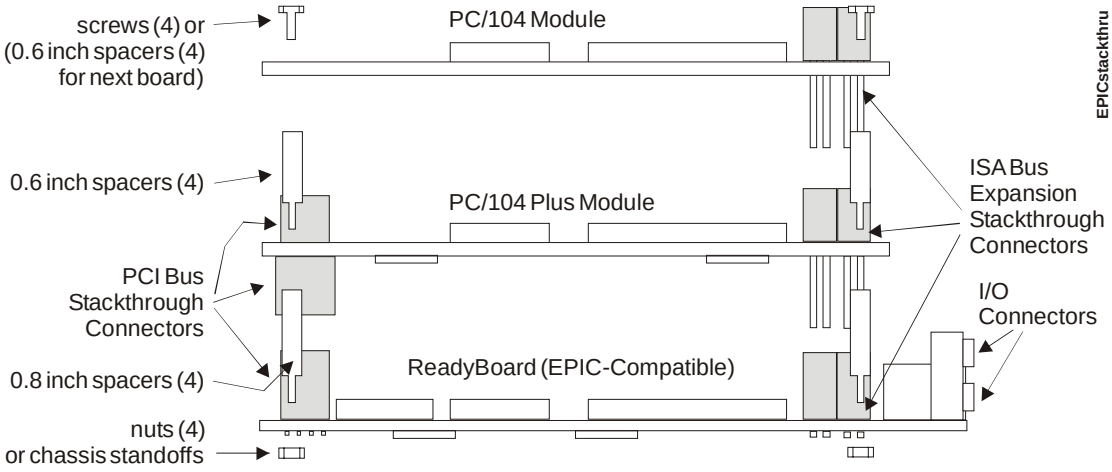


Figure 2-1. Typical ReadyBoard and PC/104 Module Stack

Product Description

The ReadyBoard 800 is a mid-sized, EPIC-compatible, affordable, high quality single-board system, which contains all the component subsystems of a PC/AT PCI motherboard plus the equivalent of up to 5 PCI expansion boards. The ReadyBoard 800 is based on one of the ultra high performance, high-integration Intel Pentium M or Celeron M processors. These processors with the matching chip set give designers a complete integration solution with a high performance embedded processor based on the EPIC form factor that conforms to the Revision 1.0 of the EPIC standard.

Each ReadyBoard 800 incorporates a Intel® 855GME chipset for the Memory Hub (Northbridge) and I/O Hub (Southbridge) controllers. This includes the Intel 82855GME memory hub, which controls graphics and memory interface and the Intel 82801DBM I/O Hub Controller for I/O functions. The Winbond Electronics Corp., Super I/O controller W83627HF, adds I/O functions. Together, the Intel and Winbond chips provide four serial ports, a floppy or EPP/ECP parallel port, four USB 2.0 ports, PS/2 keyboard and mouse interfaces, an Ultra/DMA 33/66 IDE controller supporting two IDE drives and one compact flash socket, AGP 4X graphics equivalent controller, which provides CRT and LVDS flat panel video interfaces for the most popular flat panels, and an audio AC'97 CODEC on the board. The ReadyBoard 800 also supports two independent Ethernet interfaces, 10/100BaseT and 1000BaseT, and up to 1 GB of ECC or non-ECC DDR RAM in a single 200-pin SODIMM socket.

The ReadyBoard 800 can be expanded through the PCI-104 expansion bus to accept the PCI-104 cards that offer compact, self-stacking, modular expandability for additional system functions. If required for an application, the PC/104 bus, an embedded system version of the signal set provided on a desktop PC's ISA bus is provided by the optional Ampro MiniModule ISA expansion board. The PC/104-Plus bus includes this signal set, and in addition, includes signals implementing a PCI bus, available on an additional 120-pin (4 rows of 30 pins) PCI expansion bus connector. The ISA bus operates at 8 MHz clock speed and the PCI bus operates at 33 MHz clock speed. See Figure 2-2.

Among the many embedded enhancements on the ReadyBoard 800 that ensure embedded system operation and application versatility are a watchdog timer, serial console support, battery-free boot, customizable splash screen, on-board high-density compact flash card, and Ampro BIOS extensions for OEM boot customization.

The ReadyBoard 800 is particularly well suited to embedded applications by meeting the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with Ampro MiniModules™ or other PCI-104 compliant expansion boards, or it can be used as powerful computing engine. The ReadyBoard 800 only requires a single +5V power supply.

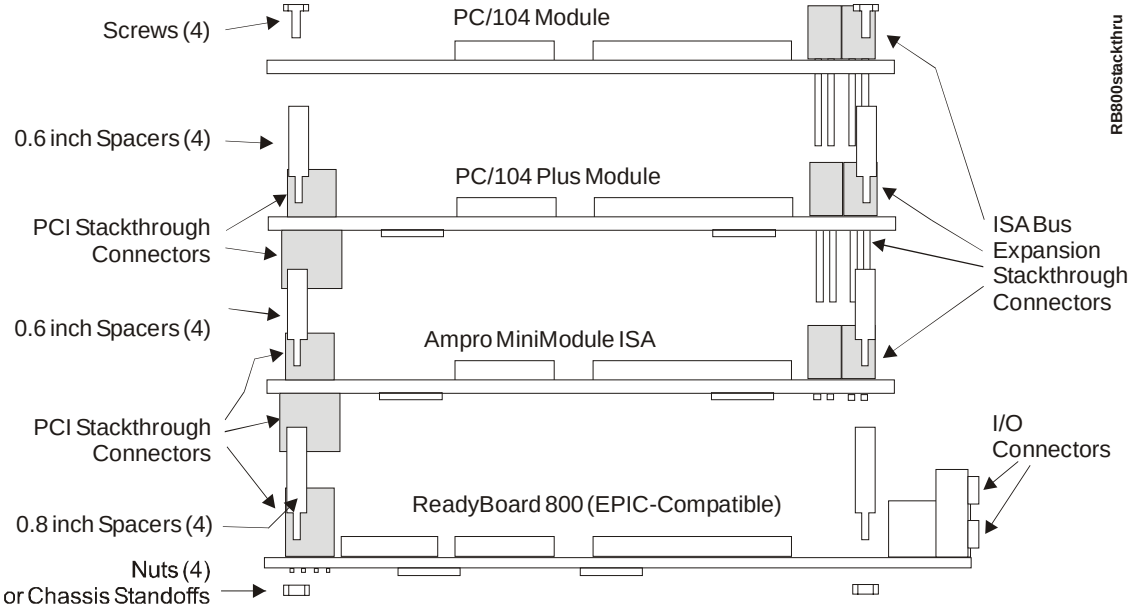


Figure 2-2. Stacking PC/104 Modules with a ReadyBoard 800

Board Features

- CPU features
  - Provides 1.4 GHz Low Voltage (LV) Intel Pentium M, 1.0 GHz Ultra Low Voltage (ULV) Celeron M, or 600 MHz Ultra Low Voltage (ULV) Celeron M processors
  - All processors support a Front Side Bus (FSB) of 400 MHz
- Memory
  - Provides a single standard 200-pin DDR SODIMM socket
  - Supports a single +2.5V DDR RAM SODIMM up to 1 GB
  - Supports PC2700 DDR 333 (166 MHz)
  - Provides 512 kB of flash memory
- PCI-104 Bus Interface
  - Supports PCI 2.3 standard
  - Supports PCI Bus speed of 33 MHz
  - Supports optional PC/104 standard (add-on MiniModule ISA expansion board)
  - Supports PC/104 standard at 8 MHz
- IDE Interfaces
  - Provides two enhanced IDE controllers
  - Supports two IDE drives on Primary IDE and one compact flash card on Secondary IDE
  - Supports dual bus master mode
  - Supports Ultra DMA 33/66/100 modes
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
  - Compact flash socket (Secondary IDE only)
    - Supports IDE compact flash card
    - Supports compact flash on secondary IDE bus with Master/Slave jumper
    - Supports bootable compact flash card
- Floppy/Parallel Interface
  - Shared floppy/parallel connector
  - Supports one floppy disk drive (1 standard 34-pin floppy drive)
  - Supports all standard PC/AT formats: 360 kB, 1.2 MB, 720 kB, 1.44 MB, 2.88 MB
  - Supports standard printer port
  - Supports IEEE standard 1284 protocols of EPP and ECP outputs
  - Bi-directional data lines
  - Supports 16 byte FIFO for ECP mode
- Serial Ports
  - Provides four buffered serial ports with full handshaking
  - Provides two DB9 connectors Serial 1 & 2 (COM1 & COM2)
  - Provides two serial ports Serial 3 & 4 (COM3 & COM4) through 20-pin header

- Provides 16550-equivalent controllers, each with a built-in 16-byte FIFO buffer
- Supports full modem capability on three of the four ports
- Supports RS-232 operation on all four ports
- Supports RS-485 or RS-422 operation on two ports, Serial 3 & 4 (COM3 & COM4)
- Supports programmable word length, stop bits, and parity
- Supports 16-bit programmable baud-rate generator

- USB Ports
  - Provides two root USB hubs
  - Provides four USB ports
  - Provides two standard USB connectors (USB 0 & 1) and one 10-pin header (USB 2 & 3)
  - Supports USB v2.0 and legacy v1.1 devices
  - Supports one USB floppy disk drive
  - Provides over-current shared fuses on board
- Audio interface
  - Supports AC'97 audio standard
  - Provides AC'97 CODEC
  - Provides non-amplified Stereo Line In/Out
  - Provides non-amplified MIC in (Mono)
- Ethernet Interfaces
  - Provides two fully independent Ethernet (RJ45) ports
  - Provides Intel's 82551ER and 825541GI (Gigabit) Ethernet controllers
  - Provides integrated LEDs on each port (Link/Activity and Speed)
  - Supports IEEE 802.3 10BaseT/100BaseTX compatible physical layer
  - Supports IEEE 802.3x 10BaseT/100BaseTX/1000BaseT compatible physical layer
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
  - Full-duplex mode supports transmit and receive frames simultaneously
  - Supports IEEE 802.3x Flow control in full duplex mode
  - Half-duplex mode supports enhance proprietary collision reduction mode
- Video Interfaces (CRT/LVDS)
  - Support CRT (1600 x 1200) with 64 MB UMA (Unified Memory Architecture)
  - Provides standard 15-pin VGA connector
  - Provides AGP 4X equivalent performance
  - Provides LVDS outputs (1 or 2 channels; four differential signal pairs; two 12-bit interleaved or one 24-bit non-interleaved) on 30-pin header
- Infrared Interface
  - Provides IrDA v1.1 signals on separate connector (J9)
  - Supports HPSIR and ASKIR infrared modes
  - Supports IR mode select from the Super I/O chip

- Keyboard/Mouse Interface
  - Provides PS/2 keyboard (shared with mouse) interface
  - Provides PS/2 mouse (shared with keyboard) interface
  - Provides shared over-current fuse
- Miscellaneous
  - Provides real-time clock (RTC) with replaceable battery
  - Supports battery-free boot
  - Supports external battery option
  - Provides Thermal and Voltage monitoring
  - Supports Serial Console
  - Provides General Purpose I/O (GPIO) capability
  - Supports USB Boot
  - Supports LAN Boot (PXE)
  - Supports watchdog timer (WDT)
  - Supports splash screen customization

Block Diagram

Figure 2-3 shows the functional components of the ReadyBoard 800.

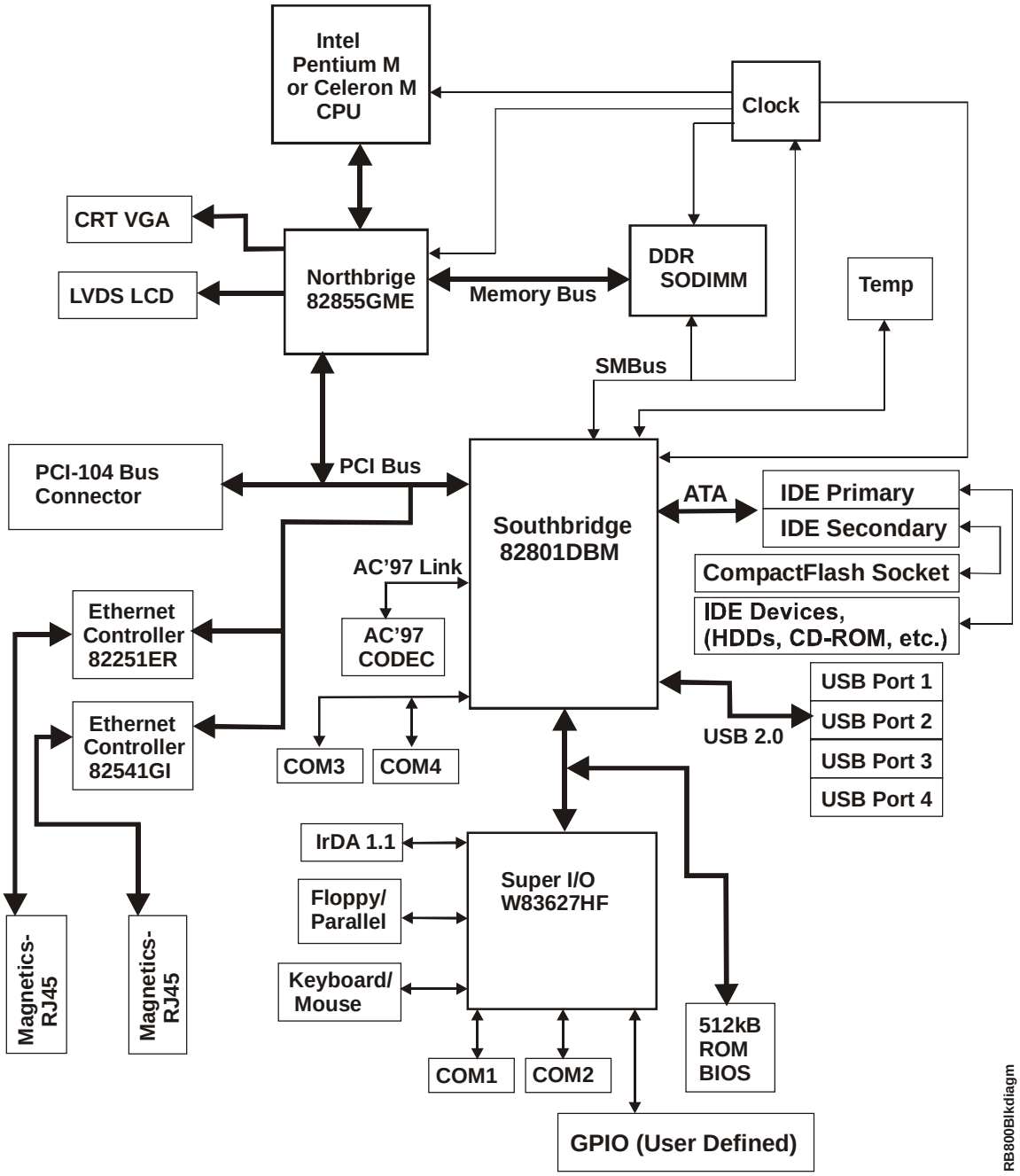


Figure 2-3. Functional Block Diagram

Major Integrated Circuits (ICs)

Table 2-1 lists the major integrated circuits (ICs or chips) on the ReadyBoard 800, including a brief description of each, and Figure 2-4 shows the location of the major chips.

Table 2-1. Major Integrated Circuit Description and Function

Chip Type	Mfg.	Model	Description	Function
CPUs (U5)	Intel	Pentium M Celeron M	LV 1.4 GHz, ULV 1.0 GHz, or ULV 600 MHz CPU's	Embedded CPU
Memory Hub (U7)	Intel	82855GME	Northbridge functions plus Video	Memory and Video
I/O Hub (U6)	Intel	82801DBM	Southbridge functions (provides some of standard I/O functions)	I/O Functions
Super I/O (U14)	Winbond Electronics, Corp.	W83627HF	Super I/O controller provides remaining standard I/O functions	I/O Functions
Ethernet Controllers (U12, U13)	Intel	82551ER 82541GI	Ethernet chips provide two independent 10/100BaseT and 1000/100/10BaseT based network channels	Ethernet Functions

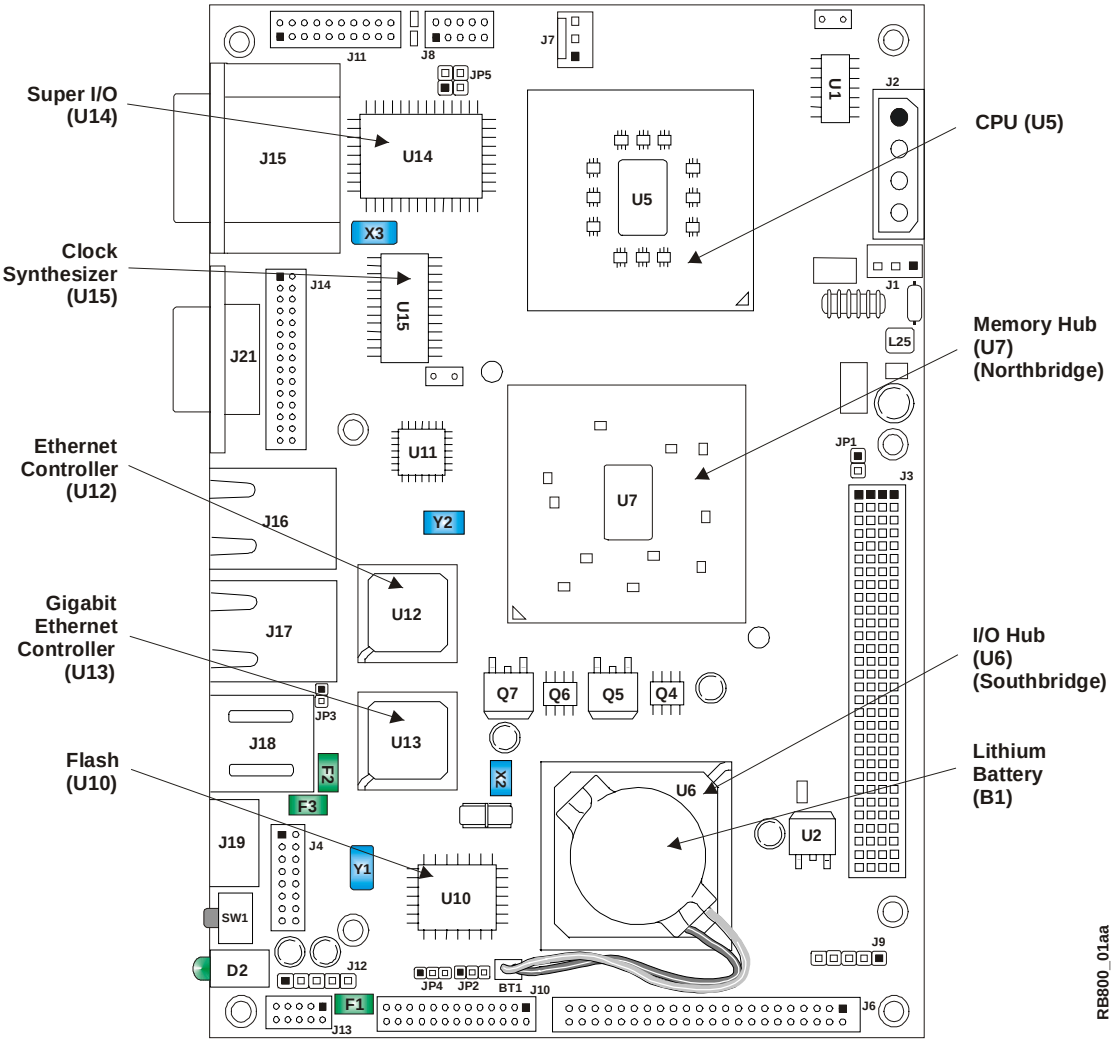


Figure 2-4. Component Location (Top view)

Connector Definitions

Table 2-2 describes the connectors shown in Figures 2-4 to 2-7. All I/O connectors use 0.1" pin spacing, where applicable, unless otherwise indicated.

Table 2-2. Connector Descriptions

Jack #	Signal/Device	Description
BTI	RTC battery (B1)	2-pin, 1.25 mm header for battery input
J1	Power On	3-pin, 2 mm header for Power On and +5V standby voltages
J2	Power In	4-pin, 5.08 mm connector for input power +5V, +12V, GND
J3	PCI-104	120-pin, 2 mm, connector for PCI bus
J4	Audio In/Out	16-pin, 2 mm connector for Line In L/R, Line Out L/R, Mic in
J5	Factory Only	Not loaded
J6	Primary IDE	44-pin, 2 mm connector for the primary IDE interface
J7	Fan connector	3-pin header provides +12v, tach, and ground to fan.
J8	GPIO	10-pin, 2 mm header for GPIO signals
J9	IrDA	5-pin header for IrDA signals
J10	Floppy/Parallel Port	26-pin, 2 mm connector for floppy/parallel port interface
J11	Serial B	20-pin, 2 mm connector for Serial ports 3 & 4 (COM3 & COM4)
J12	Utility	5-pin header for external Battery, Reset, Speaker
J13	USB 2 & 3	10-pin, 2 mm connector provides USB2 and USB3 output
J14	Video (LVDS)	30-pin, 2 mm connector for LVDS video display
J15A/B	Serial A	9-pin dual connectors for Serial ports 1 & 2 (COM1 & COM2, DB9)
J16	Ethernet 1 + LEDs	14-pin connector for 8-pin RJ45 and LEDs for Ethernet port 1
J17	Ethernet 2 + LEDs	14-pin connector for 8-pin RJ45 and LEDs for Ethernet port 2
J18A/B	USB 0 & 1	8-pin connector for two 4-pin interfaces provide USB0 and USB1
J19	Keyboard/Mouse	6-pin, 2 mm PS/2 Keyboard/Mouse connector (dual output cable)
J21	Video (CRT VGA)	15-pin connector for output to a CRT monitor
J22	SODIMM	200-pin socket for DDR SDRAM SODIMM
J23	Compact Flash	50-pin, 1.27 mm, socket accepts compact flash cards (Type I or II)

NOTE Ampro uses a connector/header numbering method in Chapter 3 to ease connector pin identification. For example, a 20-pin header with two rows of pins, using odd/even numbering, where pin-2 is directly across and adjacent to pin-1, is noted in this way; 20-pin, 2 rows, odd/even (1, 2). Alternately, a 20-pin connector using consecutive numbering, where pin-11 is directly across and adjacent to pin-1, is noted in this way; 20-pin, 2 rows, consecutive (1, 11). The second number in the parenthesis is always directly across from and adjacent to pin-1, with a few exceptions (PCI-104, PC/104, etc.). See Figure 2-5.

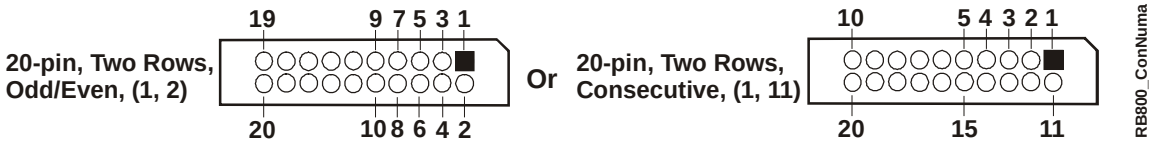


Figure 2-5. Connector Pin-Out Identifications

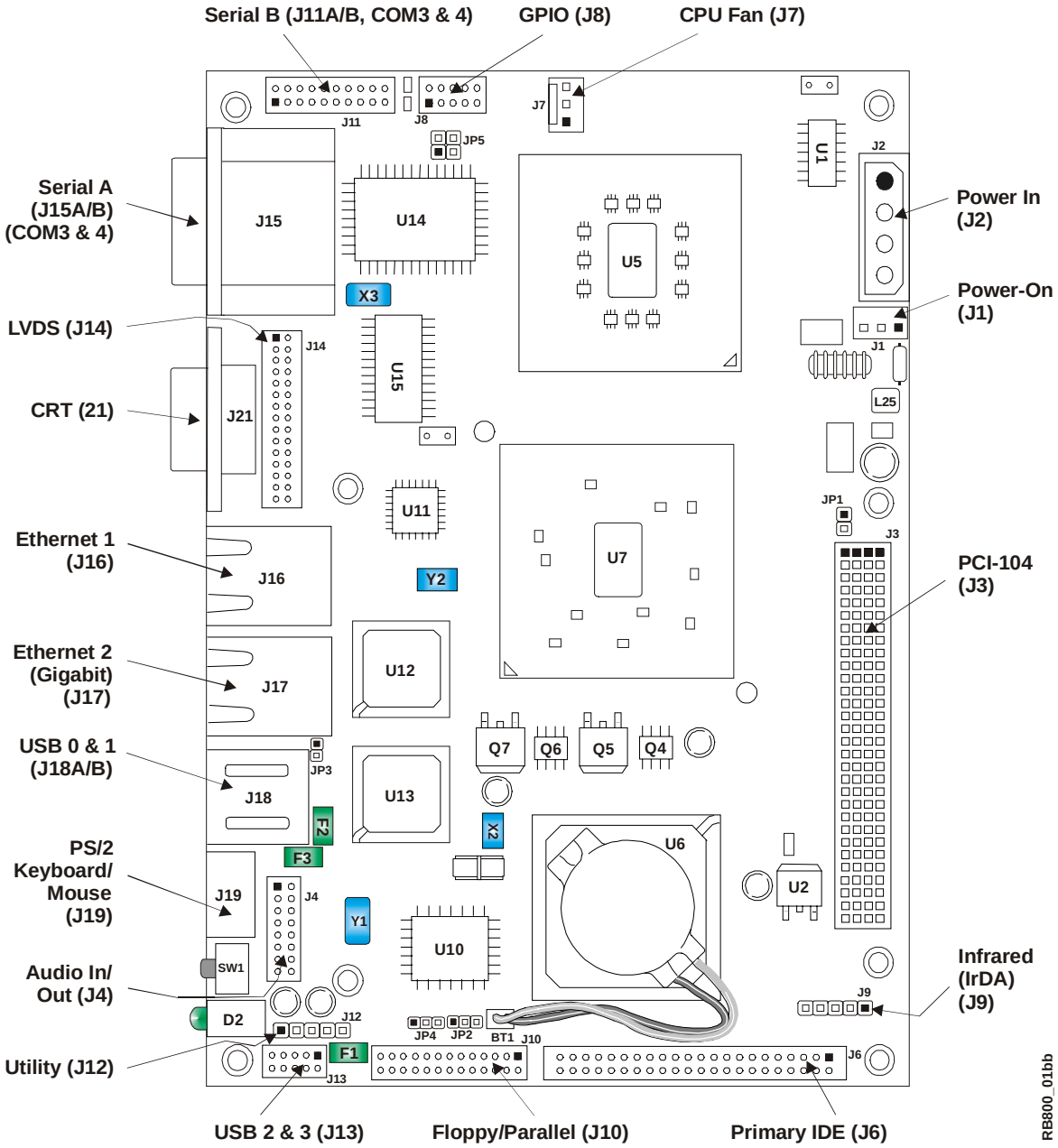


Figure 2-6. Connector Locations (Top view)

NOTE	Pin-1 is shown as a black pin (circle or square) in all connectors and jumpers in all illustrations. To comply with the PC/104, PC/104-Plus, or PCI-104 specifications, some pins in the connectors/headers are missing or have keys blocking the pins.

Jumper Definitions

Table 2-3 describes the jumpers shown in Figure 2-7. Refer to the Oops! Jumper for BIOS recovery.

Table 2-3. Jumper Settings

Jumper #	Installed/Enabled	Removed/Enabled
JP1 – ISA IRQ (SerialIRQ)	Enabled (pins 1-2) See Note ⊗	Disabled (removed) **Default**
JP2 – CMOS Normal/Clear	Normal (pins 1-2) **Default**	Clear (Resets CMOS, pins 2-3)
JP3 – CF Master/Slave	Master (pins 1-2)	Slave (removed) **Default**
JP4 – LCD Voltage Type	Enable +3.3V (pins 1-2) **Default**	Enable +5V (pins 2-3)
JP5 – COM3 RS485	Termination (pins 1-2)	No Termination (removed) **Default**
JP5 – COM4 RS485	Termination (pins 3-4)	No Termination (removed) **Default**

NOTE ⊗ The ISA interrupts are required on pin 31 (B1) of J3 on the PCI-104 connector, when using the MiniModule ISA board. Use the ISA IRQ jumper (JP1) to enable the ISA interrupts. For full PCI-104 compatibility the jumper should be removed (default setting). See Appendix B for more information.

Ethernet LED Definitions

Tables 2-4 and 2-5 provide the LED colors and definitions for the Ethernet ports, Port 1 (J16) and Port 2 (J17) located on the ReadyBoard 800. Refer to Figures 2-6 and 2-10.

Table 2-4. Ethernet Port 1 (J16) LED Indicators

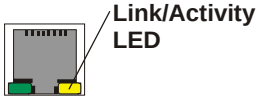
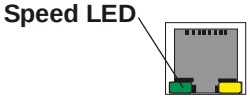
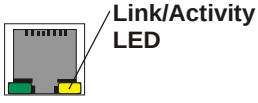
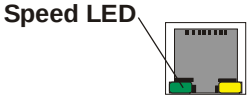
Indicator	Definition
	Link/Activity LED – This yellow LED is the activity/link indicator and provides the status of Ethernet port 1 (J16). • A steady On LED indicates a link is established. • A flashing LED indicates active data transfers.
	Speed LED – This green LED is the Speed indictor and indicates transmit or receive speed of Ethernet port 1 (J16). • A steady On LED indicates the port is at 100BaseT speed. • A steady Off LED indicates the port is at 10BaseT speed.

Table 2-5. Ethernet Port 2 (J17) LED Indicators

Indicator	Definition
	Link/Activity LED – This yellow LED is the activity/link indicator and provides the status of Ethernet port 2 (J17). • A steady On LED indicates a link is established. • A flashing LED indicates active data transfers.
	Speed LED – This green LED is the Speed indictor and indicates transmit or receive speed of Ethernet port 2 (J17). • A steady Off LED indicates the port is at 10 or 100BaseT speed. • A steady On LED indicates the port is at 1000BaseT speed.

Power/IDE LED Definitions

Table 2-6. Power/IDE Activity LED Indicators (D2)

LED #	Activity (On)	No Activity (Off)
LED stack (D2)	**Steady Green = Power On**	**Steady Off = Power Off**
LED stack (D2)	**Flashing Yellow = IDE activity** (IDE drive or compact flash)	**Steady Off = No IDE activity**

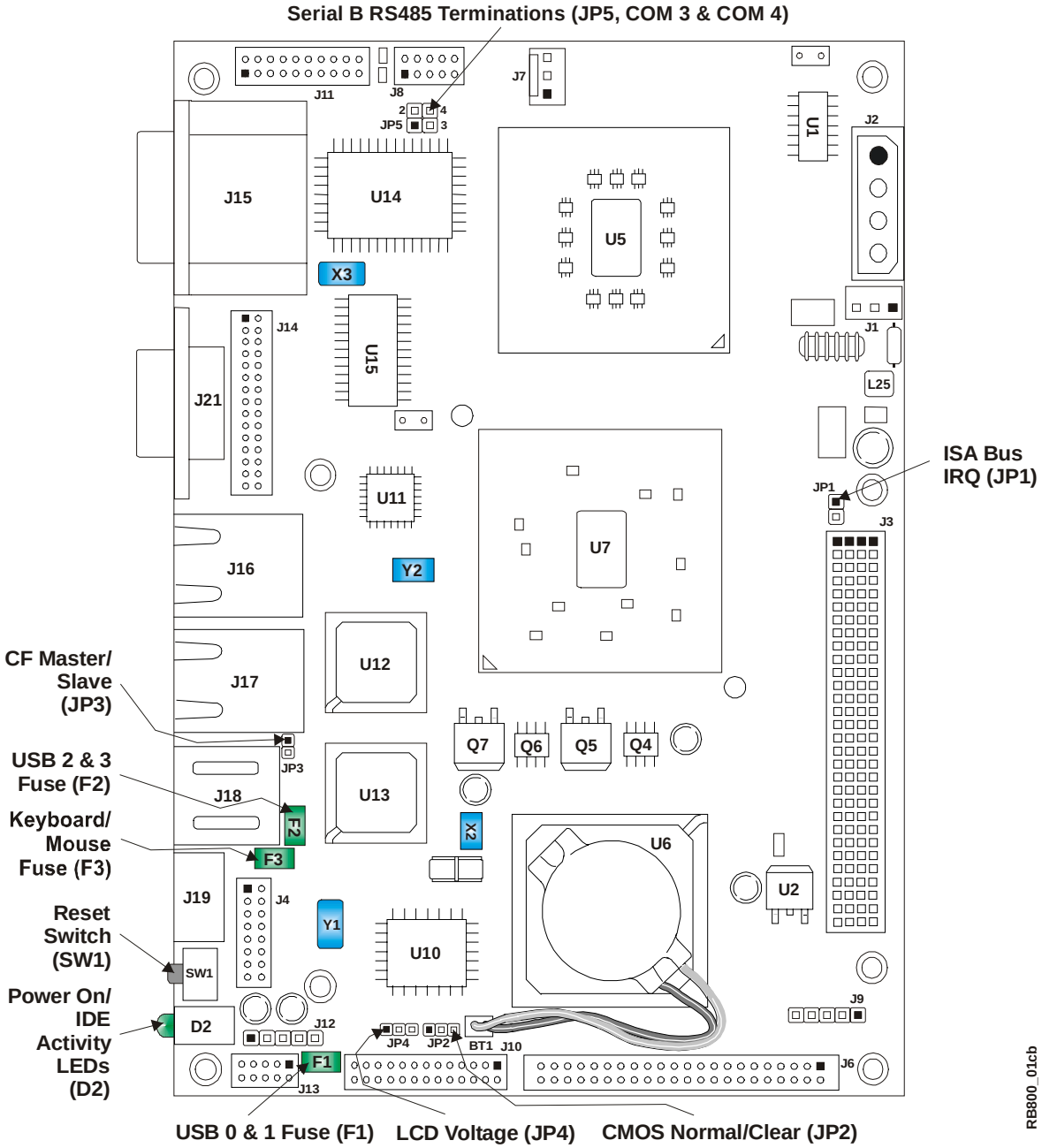


Figure 2-7. Jumper, Switch, Fuse, and LED Locations (Top view)

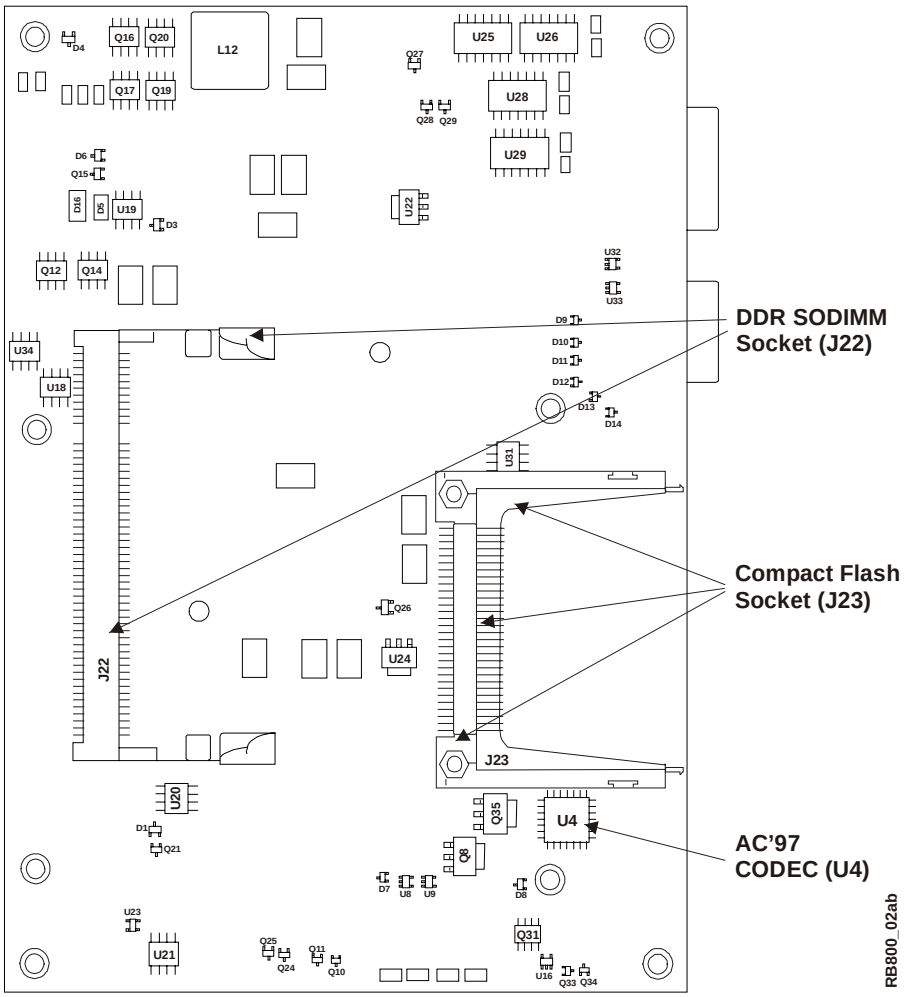


Figure 2-8. Connector and Component Locations (Bottom view)

Switch Definition

Table 2-7. Reset Switch (SW1)

Component	Description
Reset switch (SW1)	4-pin, momentary push button switch

Note: The reset switch (SW1) is located on the edge of the ReadyBoard 800. See Figures 2-7 and 2-10.

Additional Components

The fuses in Table 2-8 are shown in Figure 2-7.

Table 2-8. Additional Component Descriptions

Component	Description
Fuse (F1)	Auto-reset, 1.6 Amp shared fuse for USB 0 & USB 1
Fuse (F2)	Auto-reset, 1.6 Amp shared fuse for USB 2 & USB 3
Fuse (F3)	Auto-reset, 1.1 Amp shared fuse for Keyboard/Mouse protection

Specifications

Physical Specifications

Table 2-9 lists the physical dimensions of the board. Figures 2-9 and 2-10 give the mounting dimensions, including side views, and Figure 2-9 shows the pin-1 connector locations.

Table 2-9. Weight and Footprint Dimensions

Parameter	Dimensions
Weight	0.117 kg. (0.26 lb.)
Height (overall)	28.44 mm (1.12")
Width	115 mm (4.5")
Length	165 mm (6.5")
PCB Thickness	1.574 mm (0.062")

NOTE Overall height is measured from the upper board surface to the highest permanent component (at Serial A) on the upper board surface. This measurement does not include the heatsinks available for these boards. See Figure 2-10.

Power Specifications

Table 2-10 lists the ReadyBoard 800 power requirements.

Table 2-10. Power Supply Requirements

Parameter	600 MHz ULV Celeron M Characteristics	1.0 GHz ULV Celeron M Characteristics	1.4 GHz LV Pentium M Characteristics
Input Type	Regulated DC voltages	Regulated DC voltages	Regulated DC voltages
In-rush* Current	Typical 35.7A	Typical 24.4A	Typical 21.2A
BIT** Current	Typical 2.59A (12.95W)	Typical 3.6A (17.98W)	Typical 3.75A (18.75W)

Notes: *In-rush measured with video, 128 MB memory, and power connected. Typically, in-rush current reflects the short duration current spike associated with charging large on-board bulk capacitance during power supply start up. However, the listed in-rush current value is the result of placing a switch on the DC output of a fully 'ramped' power supply to give a worst-case current value, which is much higher than the standard method. This in-rush value should be regarded as a maximum design guideline, not a requisite value.

**The BIT (burn in test) is conducted with 128 MB DDR SODIMM, floppy, IDE HDD, USB HDD, USB CD-ROM, keyboard, mouse, serial loopbacks (4), USB compact flash reader and card (64 MB), USB Thumb drive, and active Ethernet channels (2) in a Windows™ 2000 OS environment.

Mechanical Specifications

Figures 2-9 and 2-10 show the top view and side views of the ReadyBoard 800 with the mechanical mounting dimensions.

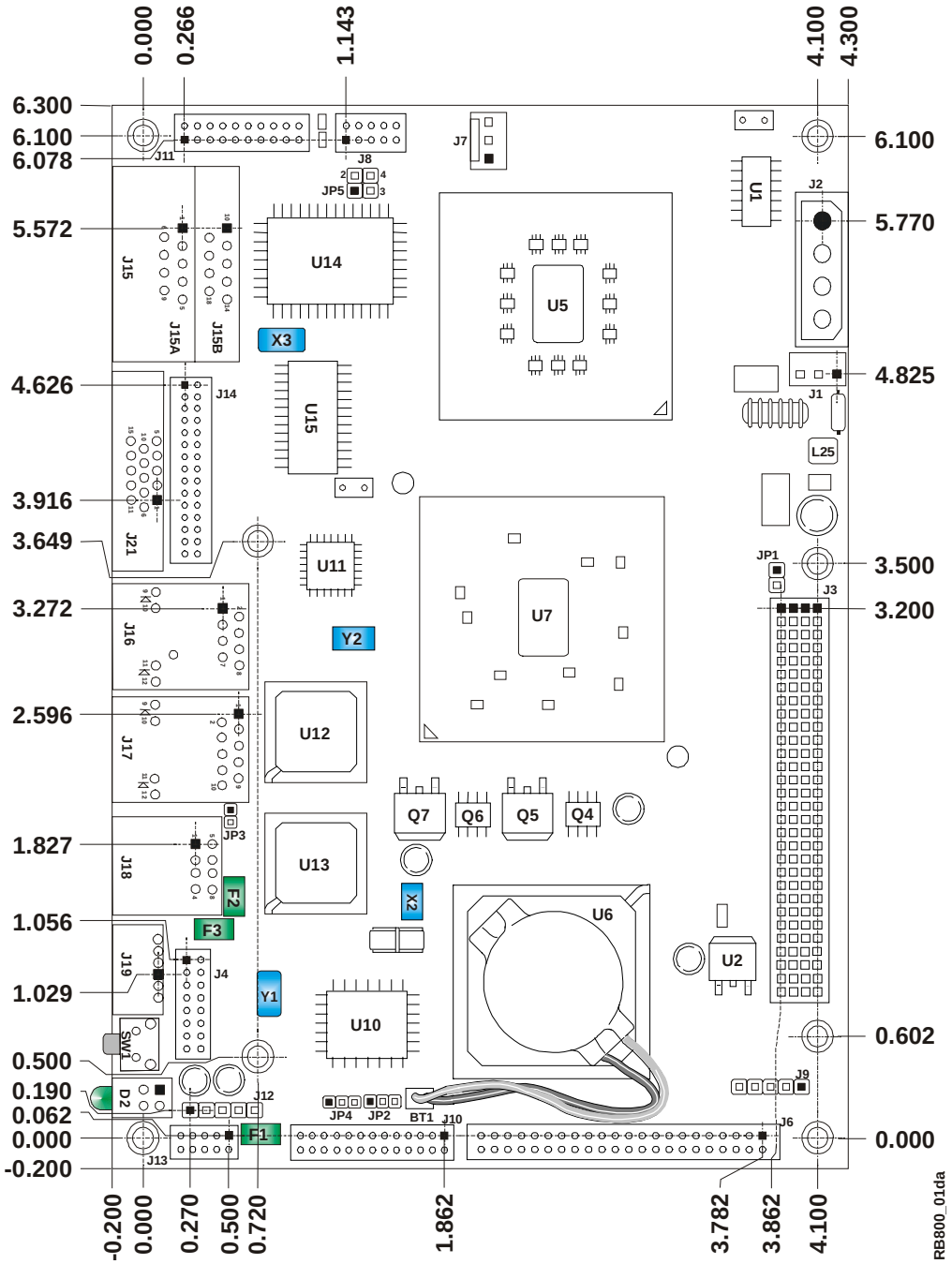


Figure 2-9. ReadyBoard 800 Dimensions (Top view)

NOTE	All dimensions are given in inches, unless otherwise specified.

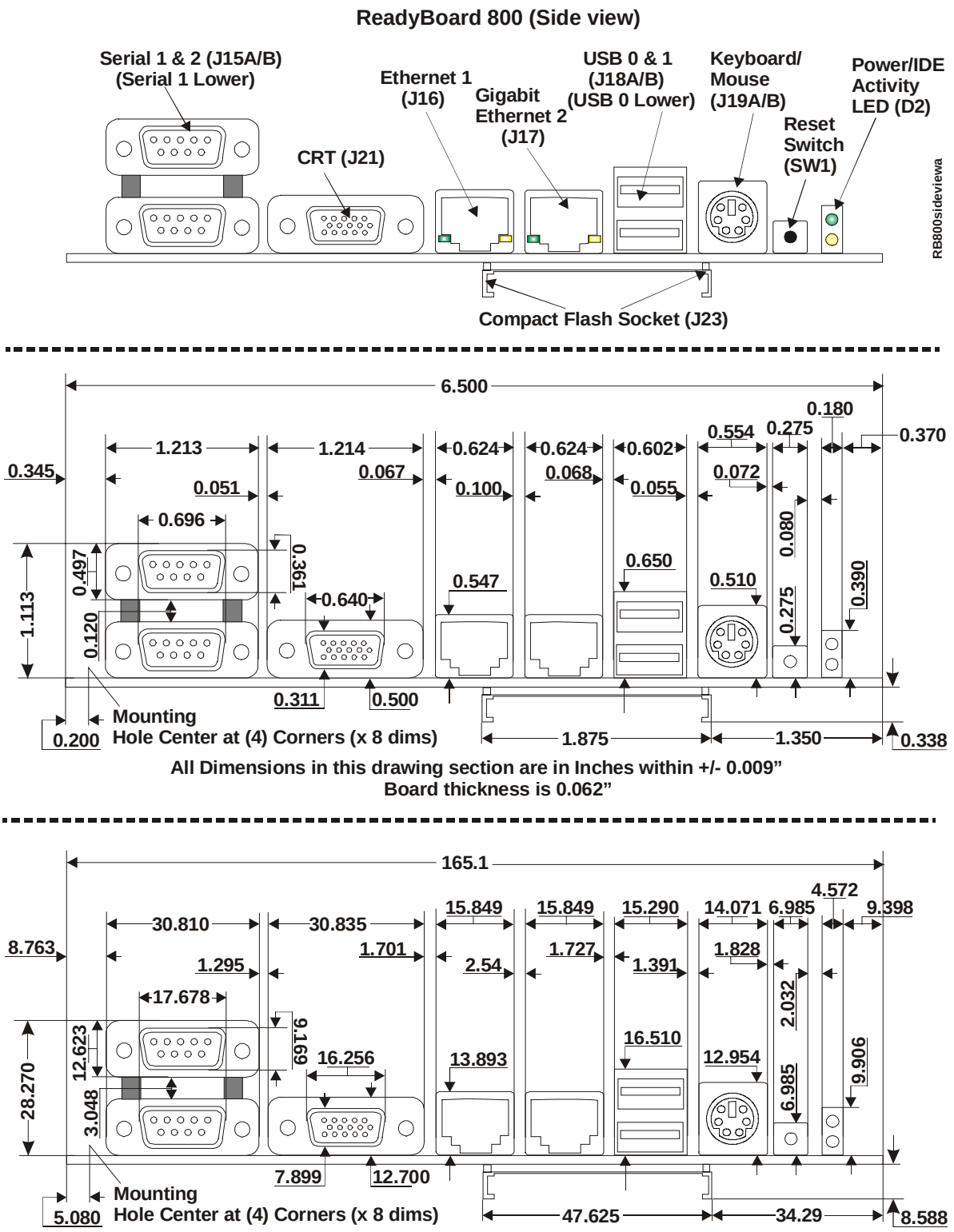


Figure 2-10. ReadyBoard 800 Panel Dimensions (Side view)

Environmental Specifications

Table 2-11 provides the most efficient operating and storage condition ranges required for this board.

Table 2-11. Environmental Requirements

	Processor	600 MHz ULV Celeron M Conditions	1.0 GHz ULV Celeron M Conditions	1.4 GHz LV Pentium M Conditions
Temperature	Operating	+0° to + 60° C (32° to + 140° F)	+0° to + 60° C (32° to + 140° F)	+0° to + 60° C (32° to + 140° F)
	Storage	–20° to +75° C (–4° to +167° F)	–20° to +75° C (–4° to +167° F)	–20° to +75° C (–4° to +167° F)
Humidity	Operating	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing
	Non-operating	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU, Northbridge, Southbridge, Secondary I/O, and voltage regulators are the sources of heat on the board. The ReadyBoard 800 is designed to operate at its maximum CPU speed of 600 MHz, 1.0 GHz, or 1.4 GHz. All processors and the Memory Hub (Northbridge) require a heatsink, but no fan.

Chapter 3 Hardware

Overview

This chapter discusses the chips and features of the connectors in the following order:

- CPU (U5)
- Memory (J22)
- PCI-104 (J3A, B, C, D)
- IDE Interfaces (J6)
- Compact Flash Socket (J23)
- Floppy/Parallel Interface (J10)
- Serial Interfaces (J11A/B, J15A/B)
- USB (J13A/B, J18A/B)
- Ethernet Interfaces (J16, J17)
- Audio Interface (J4)
- Video Interfaces (J14, J21)
- Miscellaneous
  - Utility Interfaces (J12)
  - Reset Switch (SW1)
  - Keyboard/Mouse (J19)
  - Infrared (IrDA) Port (J9)
  - Real Time Clock (RTC)
  - User GPIO signals (J8)
  - Temperature Monitoring
  - Serial Console
  - Watchdog timer
  - Power Interface (J1, J2)

NOTE	Ampro Computers, Inc. only supports the features/options tested and listed in this manual. The main integrated circuits (chips) used in the ReadyBoard 800 may provide more features or options than are listed for the ReadyBoard 800, but some of these chip features/options are not supported on the board and may not function as specified in the chip documentation.

CPU (U5)

The ReadyBoard 800 supports three Intel processor choices; high performance Low Voltage (LV) 1.4 GHz Pentium® M 738, Ultra Low Voltage (ULV) 1.0 GHz Celeron M 373, or an Ultra Low Voltage (ULV) 600 MHz Celeron® M processor.

Celeron M Processors

The Celeron M Ultra Low Voltage (ULV) processor (Banias core) at 600 MHz has 512 kB L2 Cache on board, with a 400 MHz FSB (front side bus). The 600 MHz Celeron M processor uses 130 nm architecture and requires a heatsink, but no fan.

The Celeron M 373 Ultra Low Voltage (ULV) processor (Dothan core) at 1.0 GHz has 512 kB L2 Cache on board, with a 400 MHz FSB (front side bus). The 1.0 GHz Celeron M 373 processor uses 90 nm architecture and requires a heatsink, but no fan.

Pentium M Processor

The Pentium M 738 Low Voltage (LV) processor (Dothan core) at 1.4 GHz has 2 MB L2 Cache on board with a 400 MHz FSB (front side bus). The 1.4 GHz Pentium M 738 processor uses 90 nm architecture and requires a heatsink, but no fan.

Memory

The ReadyBoard 800 memory consists of the following elements:

- DDR RAM SODIMM
- Flash memory

DDR RAM Memory (J22)

The ReadyBoard 800 supports a single 200-pin DDR SODIMM socket.

- SODIMM socket can support up to 1 GB of memory
- PC 2700 DDR 333 operating at 166 MHz (6 ns)
- +2.5V DDR RAM

NOTE	Ampro recommends using PC 2700 DDR 333 (166 MHz, 6 ns), +2.5V, 200-pin, DDR RAM SODIMM for maximum performance. The ReadyBoard 800 will operate acceptably with a PC 2100 DDR 266 (133 MHz, 7.5 ns) SODIMM.

Flash Memory (U10)

There is an 8-bit wide, 512 kB flash device used for system BIOS and it is connected to the LPC Bus. The BIOS is re-programmable and the supported features are detailed in Chapter 4, BIOS Setup.

Interrupt Channel Assignments

The channel interrupt assignments are listed in Table 3-1.

Table 3-1. Interrupt Channel Assignments (Typical)

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	D															
Keyboard		D														
Secondary Cascade			D													
COM1				O	D						O	O				
COM2				D	O						O	O				
COM3				O	O						O	D				
COM4				O	O						D	O				
Floppy							D									
Parallel						O		D								
RTC									D							
IDE Primary															D	O
IDE Secondary															O	D
Math Coprocessor														D		
PS/2 Mouse													D			
Sound Blaster						D		O		O	O					
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
PCI INTE	Automatically Assigned															
PCI INTF	Automatically Assigned															
PCI INTH	Automatically Assigned															
USB	Automatically Assigned															
VGA	Automatically Assigned															
Ethernet	Automatically Assigned															

Legend: D = Default, O = Optional Refer also to the IRQs listed in Chapter 4, BIOS Setup.

NOTE	The IRQs for the Ethernet, Video, and USB are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Memory Map

The following table provides the common PC/AT memory allocations. Memory below 000500h is used by the BIOS. Refer to Table 3-2.

Table 3-2. Memory Map

Base Address	Function
00000000h - 0009FFFFh	Conventional Memory
000A0000h - 000AFFFFh	Graphics Memory
000B0000h - 000B7FFFh	Mono Text Memory
000B8000h - 000BFFFFh	Color Text Memory
000C0000h - 000CFFFFh	Standard Video BIOS
000E0000h - 000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
00100000h - 04000000h	Extended Memory (If onboard VGA is enabled, then the amount of memory assigned is subtracted from extended memory)
FFF80000h - FFFFFFFFh	System Flash

I/O Address Map

Table 3-3 list the I/O address map.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
000-00F	Primary DMA Controller
020-021	Master interrupt Controller
040-043	Programmable Interrupt Timer (Clock/Timer)
060-06F	Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Registers
092	Fast A20 gate and CPU reset
094	Motherboard enable
102	Video subsystem register
0A0-0BF	Slave Interrupt Controller
0C0-0DF	Slave DMA Controller #2
0F0-0FF	Math Coprocessor
170-177	Secondary IDE Hard Disk Controller
1F0-1F8	Primary IDE Hard Disk Controller
201	Watchdog Timer (WDT)
278-27F	Parallel Printer
2E8-2FF	Serial Port 4 (COM4)
2F8-2FF	Serial Port 2 (COM2)
378-37F	Parallel port (Standard and EPP)
3C0-3DF	VGA
3E8-3EF	Serial Port 3 (COM3)
3F0-3F7	Floppy Disk Controller
3F8-3FF	Serial Port 1 (COM1)
778-77A	Parallel Port (ECP Extensions) (Port 378+400)
CF8-CFF	PCI bus Configuration Address and Data

PCI-104 Interface (J3)

The PCI-104 expansion interface uses a 120-pin (30x4) 2 mm connector. This connector carries all of the appropriate PCI signals operating at clock speeds up to 33 MHz. The I/O Hub (82801DBM), integrates a PCI arbiter that supports up to four devices with three external PCI masters. This interface header accepts stackable modules and is located on the top of the board.

Table 3-4 provides the PCI-104 pins/signals and descriptions for 120-pins, 4 individual rows, consecutive order (B1, A1, C1, D1), with 2 mm pin spacing.

Table 3-4. PCI-104 Pin/Signal Descriptions (J3)

Pin #	Signal	Input/ Output	Description
1 (A1)	Key/GND		Key - Ground
2 (A2)	VI/O		+5 volts – Reference voltage
3 (A3)	AD05	T/S	PCI Address and Data Bus Line 5 – These address and data signal lines (0-31) are multiplexed. A bus transaction consists of an address followed by one or more data cycles.
4 (A4)	C/BE0*	T/S	PCI Bus Command/Byte Enable 0 – This signal line is one of four signal lines. These signal lines are multiplexed, so that during the address cycle, the command is defined and during the data cycle, the byte enable is defined.
5 (A5)	GND		Ground
6 (A6)	AD11	T/S	PCI Address and Data Bus Line 11 – See Pin 3 for more information.
7 (A7)	AD14	T/S	PCI Address and Data Bus Line 14 – See Pin 3 for more information.
8 (A8)	+3.3V		+3.3 volts ±5%
9 (A9)	SERR*	O/D	System Error – This signal is for reporting address parity errors.
10 (A10)	GND		Ground
11 (A11)	STOP*	S/T/S	Stop – This signal indicates the current selected device is requesting the master to stop the current transaction
12 (A12)	+3.3V		+3.3 volts ±5%
13 (A13)	FRAME*	S/T/S	PCI Bus Frame access – This signal is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle
14 (A14)	GND		Ground
15 (A15)	AD18	T/S	PCI Address and Data Bus Line 18 – See Pin 3 for more information.
16 (A16)	AD21	T/S	PCI Address and Data Bus Line 21 – See Pin 3 for more information.
17 (A17)	+3.3V		+3.3 volts ±5%
18 (A18)	IDSEL0	In	Initialization Device Select 0 – This signal line is one of four signal lines and are used as the chip-select signals during configuration.
19 (A19)	AD24	T/S	PCI Address and Data Bus Line 24 – See Pin 3 for more information.
20 (A20)	GND		Ground

Pin #	Signal	Input/ Output	Description
21 (A21)	AD29	T/S	PCI Address and Data Bus Line 29 – See Pin 3 for more information.
22 (A22)	+5V		+5.0 volts ±5%
23 (A23)	REQ0*	T/S	Bus Request 0 – This signal line is one of three signal lines. These signals indicate the device desires use of the bus to the arbitrator.
24 (A24)	GND		Ground
25 (A25)	GNT1*	T/S	Grant 1 – This signal line is one of three grant lines and these indicate access has been granted to the requesting device (PCI Masters).
26 (A26)	+5V		+5.0 volts ±5%
27 (A27)	CLK2	In	PCI clock 2 – This signal line is one of four clock signal lines and these provide the timing outputs for four external PCI devices and the timing for all transactions on the PCI bus
28 (A28)	GND		Ground
29 (A29)	+12V		+12.0 volts ±5%
30 (A30)	NC		Not connected - Reserved
31 (B1)	SERIRQ		Serial IRQ – This signal line provides the serial IRQs for the MiniModule ISA expansion board if used. See Notes.
32 (B2)	AD02	T/S	PCI Address and Data Bus Line 2 – See Pin 3 for more information.
33 (B3)	GND		Ground
34 (B4)	AD07	T/S	PCI Address and Data Bus Line 7 – See Pin 3 for more information.
35 (B5)	AD09	T/S	PCI Address and Data Bus Line 9 – See Pin 3 for more information.
36 (B6)	VI/O		+5 volts – Reference voltage
37 (B7)	AD13	T/S	PCI Address and Data Bus Lines 13 – See Pin 3 for more information.
38 (B8)	C/BE1*	T/S	PCI Bus Command/Byte Enable 1 – See Pin 4 for more information.
39 (B9)	GND		Ground
40 (B10)	PERR*		Parity Error – This signal is for reporting data parity errors.
41 (B11)	+3.3V		+3.3 volts ±5%
42 (B12)	TRDY*	S/T/S	Target Ready – This signal indicates the selected device's ability to complete the current cycle of transaction. Both IRDY* and TRDY* must be asserted to terminate a data cycle
43 (B13)	GND		Ground
44 (B14)	AD16	T/S	PCI Address and Data Bus Line 16 – See Pin 3 for more information.
45 (B15)	+3.3V		+3.3 volts ±5%
46 (B16)	AD20	T/S	PCI Address and Data Bus Lines 20 – See Pin 3 for more information.
47 (B17)	AD23	T/S	PCI Address and Data Bus Line 23 – See Pin 3 for more information.
48 (B18)	GND		Ground

Pin #	Signal	Input/ Output	Description
49 (B19)	C/BE3*	T/S	PCI Bus Command/Byte Enable 3 – See Pin 4 for more information.
50 (B20)	AD26	T/S	PCI Address and Data Bus Line 26 – See Pin 3 for more information.
51 (B21)	+5V		+5.0 volts ±5%
52 (B22)	AD30	T/S	PCI Address and Data Bus Line 30 – See Pin 3 for more information.
53 (B23)	GND		Ground
54 (B24)	REQ2*	T/S	Bus Request 2 – This signal indicates a device desires use of the bus sent to the arbitrator. This request line is not available when the MiniModule ISA board is used. See Notes.
55 (B25)	VI/O		+5 volts – Reference voltage
56 (B26)	CLK0	In	PCI clock 0 – See Pin 27 for more information
57 (B27)	+5V		+5.0 volts ±5%
58 (B28)	INTD*	O/D	Interrupt D – This signal is used to request interrupts only for multi-function devices.
59 (B29)	INTA*	O/D	Interrupt A – This signal is used to request an interrupt.
60 (B30)	NC		Not connected (Reserved)
61 (C1)	+5V		+5.0 volts ±5%
62 (C2)	AD01	T/S	PCI Address and Data Bus Line 1 – See Pin 3 for more information.
63 (C3)	AD04	T/S	PCI Address and Data Bus Lines 4 – See Pin 3 for more information.
64 (C4)	GND		Ground
65 (C5)	AD08	T/S	PCI Address and Data Bus Line 8 – See Pin 3 for more information.
66 (C6)	AD10	T/S	PCI Address and Data Bus Line 10 – See Pin 3 for more information.
67 (C7)	GND		Ground
68 (C8)	AD15	T/S	PCI Address and Data Bus Line 15 – See Pin 3 for more information.
69 (C9)	NC		Not connected (SB0* – Snoop Backoff)
70 (C10)	+3.3V		+3.3 volts ±5%
71 (C11)	LOCK*	S/T/S	Lock – This signal indicates an operation that may require multiple transactions to complete
72 (C12)	GND		Ground
73 (C13)	IRDY*	S/T/S	Initiator Ready – This signal indicates the master's ability to complete the current data cycle of the transaction
74 (C14)	+3.3V		+3.3 volts ±5%
75 (C15)	AD17	T/S	PCI Address and Data Bus Line 17 – See Pin 3 for more information.
76 (C16)	GND		Ground

Pin #	Signal	Input/ Output	Description
77 (C17)	AD22	T/S	PCI Address and Data Bus Line 22 – See Pin 3 for more information.
78 (C18)	IDSEL1		Initialization Device Select 1 – See Pin 18 for more information
79 (C19)	VI/O		+5 volts – Reference voltage
80 (C20)	AD25	T/S	PCI Address and Data Bus Line 25 – See Pin 3 for more information.
81 (C21)	AD28	T/S	PCI Address and Data Bus Line 28 – See Pin 3 for more information.
82 (C22)	GND		Ground
83 (C23)	REQ1*	T/S	Bus Request 1 – See Pin 23 for more information.
84 (C24)	+5V		+5.0 volts ±5%
85 (C25)	GNT2*	T/S	Grant 2 – See Pin 25 for more information. This signal line is reserved for the MiniModule ISA expansion board. See Notes.
86 (C26)	GND		Ground
87 (C27)	CLK3	In	PCI clock 3 – See Pin 27 for more information
88 (C28)	+5V		+5.0 volts ±5%
89 (C29)	INTB*	O/D	Interrupt B – This signal is only used to request interrupts for multi-function devices.
90 (C30)	PME*		Power Management Event – This signal is used for power management events.
91 (D1)	AD0	T/S	PCI Address and Data Bus Line 0 – See Pin 3 for more information.
92 (D2)	+5V		+5.0 volts ±5%
93 (D3)	AD03	T/S	PCI Address and Data Bus Lines 3 – See Pin 3 for more information.
94 (D4)	AD06	T/S	PCI Address and Data Bus Lines 6 – See Pin 3 for more information.
95 (D5)	GND		Ground
96 (D6)	GND		Ground
97 (D7)	AD12	T/S	PCI Address and Data Bus Line 12 – See Pin 3 for more information.
98 (D8)	+3.3V		+3.3 volts ±5%
99 (D9)	PAR	T/S	PCI bus Parity bit – This signal is the even parity bit on AD[31:0] and C/BE[3:0]*
100 (D10)	NC		Not connected (SDONE – Snoop Done)
101 (D11)	GND		Ground
102 (D12)	DEVSEL*	S/T/S	Device Select – This signal is driven by the target device when its address is decoded.
103 (D13)	+3.3V		+3.3 volts ±5%
104 (D14)	C/BE2*		PCI Bus Command/Byte Enable 2 – See Pin 4 for more information.
105 (D15)	GND		Ground

Pin #	Signal	Input/ Output	Description
106 (D16)	AD19	T/S	PCI Address and Data Bus Line 19 – See Pin 3 for more information.
107 (D17)	+3.3V		+3.3 volts ±5%
108 (D18)	IDSEL2		Initialization Device Select 2 – See Pin 18 for more information.
109 (D19)	IDSEL3		Initialization Device Select 3 – See Pin 18 for more information.
110 (D20)	GND		Ground
111 (D21)	AD27	T/S	PCI Address and Data Bus Line 27 – See Pin 3 for more information.
112 (D22)	AD31	T/S	PCI Address and Data Bus Line 31 – See Pin 3 for more information.
113 (D23)	VI/O		+5 volts – Reference voltage
114 (D24)	GNT0*	T/S	Grant 0 – See Pin 25 for more information.
115 (D25)	GND		Ground
116 (D26)	CLK1	In	PCI clock 1 – See Pin 27 for more information
117 (D27)	GND		Ground
118 (D28)	RST*	In	PCI bus reset – This signal is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset
119 (D29)	INTC*	O/D	Interrupt C – This signal is used to request interrupts only for multi-function devices.
120 (D30)	GND		Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

The Input/Output signals in this table refer to the input/output signals listed in the PCI Local Bus Manual, Revision 2.3, Chapter 2, paragraph 2.1, Signal definitions. The following terms or acronyms are used in this table:

- In – Input is standard input only signal
- Out – Totem Pole output is a standard active driver
- T/S – Tri-State is a bi-directional input output pin
- S/T/S – Sustained Tri-State is an active low tri-state signal driven by one and only one agent at a time
- O/D – Open Drain allows multiple devices to share as a wire-OR.

NOTE One request signal (pin 54 or B24, REQ2) and one grant line (pin 85 or C25, GNT2) are not available to other cards/devices when the MiniModule ISA expansion board is used. These signal lines are reserved for the MiniModule ISA board, if jumper JP1 is enabled..

IDE Interface (J6)

The ReadyBoard 800 provides one primary IDE connector (J6) for two IDE devices and one compact flash socket (J23) for the secondary IDE controller.

The I/O Hub (Southbridge) EIDE interface logic supports the following features:

- Transfer rate up to 100 Mbps
- Increased reliability using Ultra DMA 33/66/100 transfer protocols
- Supports ATAPI and DVD compliant devices
- PIO IDE transfers as fast as 14 Mbps
- Single Bus Master EIDE
- Supports two IDE drives on primary interface and one compact flash card on the secondary IDE

Table 3-5 describes the primary IDE pins/ signals for the IDE 44-pin, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-5. Primary IDE Interface Pin/Signal Descriptions (J6)

Pin #	Signal	Description
1	RESET*	Reset – Low active hardware reset (RSTDRV inverted)
2	GND	Ground
3	PDD7	Primary Disk Data 7 – These signals (0 to 15) provide the disk data signals
4	PDD8	Primary Disk Data 8 – These signals (0 to 15) provide the disk data signals
5	PDD6	Primary Disk Data 6 – These signals (0 to 15) provide the disk data signals
6	PDD9	Primary Disk Data 9 – These signals (0 to 15) provide the disk data signals
7	PDD5	Primary Disk Data 5 – These signals (0 to 15) provide the disk data signals
8	PDD10	Primary Disk Data 10 – These signals (0 to 15) provide the disk data signals
9	PDD4	Primary Disk Data 4 – These signals (0 to 15) provide the disk data signals
10	PDD11	Primary Disk Data 11 – These signals (0 to 15) provide the disk data signals
11	PDD3	Primary Disk Data 3 – These signals (0 to 15) provide the disk data signals
12	PDD12	Primary Disk Data 12 – These signals (0 to 15) provide the disk data signals
13	PDD2	Primary Disk Data 2 – These signals (0 to 15) provide the disk data signals
14	PDD13	Primary Disk Data 13 – These signals (0 to 15) provide the disk data signals
15	PDD1	Primary Disk Data 1 – These signals (0 to 15) provide the disk data signals
16	PDD14	Primary Disk Data 14 – These signals (0 to 15) provide the disk data signals
17	PDD0	Primary Disk Data 0 – These signals (0 to 15) provide the disk data signals
18	PDD15	Primary Disk Data 15 – These signals (0 to 15) provide the disk data signals
19	GND	Ground
20	NC-Key	Not Connected - Key pin plug
21	PDDREQ	Primary Device DMA Channel Request – Used for DMA transfers between host and drive (direction of transfer controlled by DIOR* and DIOW*). Also used in an asynchronous mode with DMACK*. Drive asserts IDRQ0 when ready to transfer or receive data.
22	GND	Ground

Pin #	Signal	Description
23	PDIOW*	Primary Device I/O Read/Write Strobe – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
24	GND	Ground
25	PDIOR*	Primary I/O Read/Write Strobe – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
26	GND	Ground
27	PDIORDY	Primary I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
28	PDCEL	Primary Cable Select – Used to configure IDE drives as device 0 or device 1 using a special cable.
29	PDDACK*	Primary DMA Channel Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to DMARQ asserted.
30	GND	Ground
31	IRQ14	Interrupt Request 14 – Asserted by drive when it has pending interrupt (PIO transfer of data to or from the drive to the host).
32	NC	Not connected
33	PDA1	Primary IDE ATA Disk Address (0 to 2) – Used to indicate which byte in the ATA command block or control block is being accessed
34	PD33/66	UDMA 33/66 Sense – Senses which DMA mode to use for IDE devices.
35	PDA0	Primary IDE ATA Disk Address (0 to 2) – Used to indicate which byte in the ATA command block or control block is being accessed
36	PDA2	Primary IDE ATA Disk Address (0 to 2) – Used to indicate which byte in the ATA command block or control block is being accessed
37	PDCS1*	Primary Slave/Master Chip Select 1 – Used to select the host-accessible Command Block Register.
38	PDCS3*	Primary Slave/Master Chip Select 3 – Used to select the host-accessible Command Block Register.
39	IDE LED	IDE Activity – Indicates IDE drive activity to yellow IDE LED (D5) on card edge.
40	GND	Ground
41	+5V	+5 volts +/-5%
42	+5V	+5 volts +/-5%
43	GND	Ground
44	NC	Not connected

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Compact Flash Socket (J23)

The board contains a compact flash socket, which allows for the insertion of a compact flash card. The compact flash card acts as a standard IDE Drive and is connected to the Secondary IDE bus. If a compact flash card is installed, it is the only device using the secondary IDE bus. A Jumper is used to select the Master/Slave mode. Refer to Table 2-3, Jumper Settings for more information.

CAUTION	To prevent system hangs, ensure your compact flash card is compatible with UDMA 100 IDE hard disk drives. Consult the Hardware Release notes and your compact flash card vendor for UDMA 100 compatibility.

Table 3-6 provides the signals and descriptions for a standard compact flash socket, 50-pin, 2 rows, consecutive (1, 26) with 1.27 mm (0.050") pin spacing.

Table 3-6. Compact Flash Interface Pin/Signal Descriptions (J23)

Pin #	Signal	Description
1	GND	Ground
2	SDD3	Secondary Disk Data 3 – These signals (D0-D15) carry the Data, Commands, and Status between the host and the controller. D0 is the LSB of the even Byte of the Word. D8 is the LSB of the Odd Byte of the Word. All Task File operations occur in byte mode on the low order bus D0-D7, while all data transfers are 16 bit using D0-D15 to provide the disk data signals.
3	SDD4	Secondary Disk Data 4 – Refer to SDD3 on pin-2 for more information.
4	SDD5	Secondary Disk Data 5 – Refer to SDD3 on pin-2 for more information.
5	SDD6	Secondary Disk Data 6 – Refer to SDD3 on pin-2 for more information.
6	SDD7	Secondary Disk Data 7 – Refer to SDD3 on pin-2 for more information.
7	SDCS1*	Secondary Chip Select 1 – This signal, along with CE2*, select the card and indicate to the card when a byte or word operation is being performed. This signal accesses the even byte or odd byte of the word depending on A0 and CE2*.
8, 10	NC	Not connected
9	GND	Ground
11, 12	NC	Not connected
13	VCC	+5 volts +/-5%
14, 15	NC	Not connected
16, 17	NC	Not connected
18	SDA2	Secondary Address select 2 – One of three signals (0 – 2) used to select one of eight registers in the Task File. The host grounds all remaining address lines.
19	SDA1	Secondary Address select 1 – Refer to A2 on pin-18 for more information.
20	SDA0	Secondary Address select 0 – Refer to A2 on pin-18 for more information.
21	SDD0	Secondary Disk Data 0 – Refer to SDD3 on pin-2 for more information.
22	SDD1	Secondary Disk Data 1 – Refer to SDD3 on pin-2 for more information.
23	SDD2	Secondary Disk Data 2 – Refer to SDD3 on pin-2 for more information.
24	NC	Not connected (IOCS16*)
25, 26	CFD2, CFD1	Connected through 4.7k ohm resister to ground
27	SDD11	Secondary Disk Data 11 – Refer to SDD3 on pin-2 for more information.

Pin #	Signal	Description
28	SDD12	Secondary Disk Data 12 – Refer to SDD3 on pin-2 for more information.
29	SDD13	Secondary Disk Data 13 – Refer to SDD3 on pin-2 for more information.
30	SDD14	Secondary Disk Data 14 – Refer to SDD3 on pin-2 for more information.
31	SDD15	Secondary Disk Data 15 – Refer to SDD3 on pin-2 for more information.
32	SDCS3*	Secondary Slave/Master Chip Select – This signal, along with CE1*, selects the compact flash card and indicates to the card when a byte or word operation is being performed. This signal always accesses the odd byte of the word.
33, 40	NC	Not Connected (VS1*, VS2*)
34	SDIOR*	Secondary Device I/O Read/Write Strobe – This signal is generated by the host and gates the I/O data onto the bus from the CompactFlash card when the card is configured to use the I/O interface.
35	SDIOW*	Secondary Device I/O Read/Write Strobe – This signal is generated by the host and clocks the I/O data on the Card Data bus into the CompactFlash card controller registers when the card is configured to use the I/O interface. The clock occurs on the negative to positive edge of the signal (trailing edge).
36, 38	VCC	+5 volts +/-5%
37	IRQ15	Interrupt Request 15 – IRQ 15 is asserted by drive (CF) when it has a pending interrupt (PIO transfer of data to or from the drive to the host).
39	MASTER*	Master/Slave – This pin determines the Master or Slave configuration of the compact f lash by the jumper (JP3) setting. When this pin is grounded (jumper inserted), this device is configured as Master. When this pin is open (jumper removed), this device is configured as Slave (Default).
41	RstIDE-S*	Secondary IDE Reset – This input signal is the active low hardware reset from the host. If this pin goes high, it is used as the reset signal. This pin is driven high at power-up, causing a reset, and if left high will cause another reset.
42	SDIORDY	Secondary Device I/O-DMA Channel Ready – When negated, extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
43	NC	Not Connected (InpAck)
44	VCC	+5 volts +/-5%
45	IDE LED2	IDE Activity – Indicates CF activity to yellow IDE LED (D5) on board edge.
46	SD33-66	UDMA 33/66 Sense – Senses which DMA mode to use for the compact flash.
47	SDD8	Secondary Disk Data 8 – Refer to SDD3 on pin-2 for more information.
48	SDD9	Secondary Disk Data 9 – Refer to SDD3 on pin-2 for more information.
49	SDD10	Secondary Disk Data 10 – Refer to SDD3 on pin-2 for more information.
50	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Floppy/Parallel Interface (J10)

The Super I/O controller (W83627HF) provides the floppy controller and the parallel port controller. The floppy controller and the parallel port controller share the same output connector (J10) on the board and the device selection is made in the BIOS Setup Utility.

- Floppy Port Controller only supports one floppy drive, in the standard formats, such as 360 kB, 720 kB, 1.2 MB, 1.44 MB, or 2.88 MB drives.
- Parallel Port controller supports standard parallel, Bi-directional, ECP and EPP protocols.

NOTE	Due to the multiplexed nature of the signals for the floppy and parallel ports, you can only connect one of these devices at a time. Refer to Chapter 4, BIOS Setup later in this manual when selecting the floppy or parallel device in the BIOS Setup Utility. A reboot is necessary for the change of BIOS settings to take affect.

Table 3-7 describes the floppy/parallel port (J10) pin/signals with 26-pins, 2 rows, consecutive (1, 14) with 2 mm pin spacing.

Table 3-7. Floppy/Parallel Interface Pin/Signal Descriptions (J10)

Pin #	Signal	Description
1	Strobe*	Parallel Strobe* – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode.
2	PD0	Parallel Port Data 0 – This pin (0 to 7) provides parallel port data signals.
	INDEX*	Floppy Index – Detects head positioned over the beginning of a track.
3	PD1	Parallel Port Data 1 – This pin (0 to 7) provides parallel port data signals.
	TRK0*	Floppy Track 0 – Detects when head is positioned over track 0.
4	PD2	Parallel Port Data 2 – This pin (0 to 7) provides parallel port data signals.
	WPRT*	Floppy Write Protect – Senses if diskette is write protected.
5	PD3	Parallel Port Data 3 – This pin (0 to 7) provides parallel port data signals.
	RDATA*	Floppy Read Data – Raw serial bit stream from the drive for read operations.
6	PD4	Parallel Port Data 4 – This pin (0 to 7) provides parallel port data signals.
	DSKCHG*	Floppy Disk Change – Senses when drive door is open or the diskette has been changed since the last drive selection.
7	PD5	Parallel Port Data 5 – This pin (0 to 7) provides parallel port data signals.
8	PD6	Parallel Port Data 6 – This pin (0 to 7) provides parallel port data signals.
9	PD7	Parallel Port Data 7 – This pin (0 to 7) provides parallel port data signals.
10	ACK*	Parallel Acknowledge * – This is a status output signal from the printer. A Low State indicates it has received the data and is ready to accept new data.
	DS1*	Floppy Drive Select 1 – Select drive 1.
11	BUSY	Parallel Busy – This is a status output signal from the printer. A High State indicates the printer is not ready to accept data.
	MTR1*	Floppy Motor Control 1 – Select motor on drive 1.
12	PE	Parallel Paper End – This is a status output signal from the printer. A High State indicates it is out of paper.
	WDATA*	Floppy Write Data – Encoded data to the drive for write operations.

Pin #	Signal	Description
13	PTSLCT	Printer Select – This is a status output signal from the printer. A High State indicates it is selected and powered on.
	WGATE*	Floppy Write Enable – Drive signal to enable current flow in the write head.
14	AUTOFDX*	Parallel Auto Feed* – This is a request signal into the printer to automatically feed one line after each line is printed.
	DRVEN0*	Floppy Drive Density Select Bit 0
15	ERR*	Parallel Error – This is a status output signal from the printer. A Low State indicates an error condition on the printer.
	HDSEL*	Floppy Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
16	PINIT*	Printer Initialize* – This signal used to Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
	DIR*	Floppy Direction – Direction of head movement (0 = inward motion, 1 = outward motion).
17	SLCTIN	Parallel Select In – This output signal to the printer is used to select the printer. I/O pin in ECP/EPP mode.
	STEP*	Floppy Step – Low pulse for each track-to-track movement of the head.
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	NC	Not Connected

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Serial Interfaces (J15A/B, J11A/B)

The ReadyBoard supports 4 independent serial ports, using two separate chips. The Super I/O controller (W83627HF) provides Serial ports 1 and 2 through the Serial A DB9 connectors (J15A/B) and the Southbridge (82801DBM) provides serial ports 3 and 4 through Serial B connector (J11A/B). The four serial ports support the following features:

- Four individual 16550-compatible UARTs
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Four individual 16-bit FIFOs
- Serial A supports ports 1 and 2 using the Super I/O Controller
- Serial Port 1 (COM1) supports RS-232 and full modem support
- Serial Port 2 (COM2) supports RS-232, and full modem support
- Serial B supports ports 3 and 4 using the Southbridge
- Serial Port 3 (COM3) supports RS-232/RS-485/RS-422 and full modem support
- Serial Port 4 (COM4) supports RS-232/RS-485/RS-422 and modem support

NOTE	The RS-232/RS-485/RS-422 modes are selected in BIOS Setup under *BIOS and Hardware Settings* screen for Serial ports 3 (COM3) and 4 (COM4). However, the RS-232 mode is the default (Standard) for any serial port. RS-485 mode termination is selected with jumper JP5, pins 1-2 (COM3), and pins 3-4 (COM4), when the RS-485 mode is selected in BIOS Setup. Refer to Table 2-3 for more information.

To implement the two-wire RS485 mode on either serial port, you must tie the equivalent pins together for each port.

For example; on Serial Port 3, tie pin 3 (RX3-) to 5 (TX3-) and pin 4 (TX3+) to 6 (RX3+) at the Serial B interface connector (J11) as shown in Figure 3-1. As an alternate, tie pin 2 to 3 and pin 7 to 8 at the DB9 serial connector for Serial Port 3 as shown in Figure 3-1. Refer also to the following tables for the specific pins for the other ports and connectors. The RS-422 mode uses a four-wire interface and does not need any pins tied together, but you must select RS-485 in BIOS Setup.

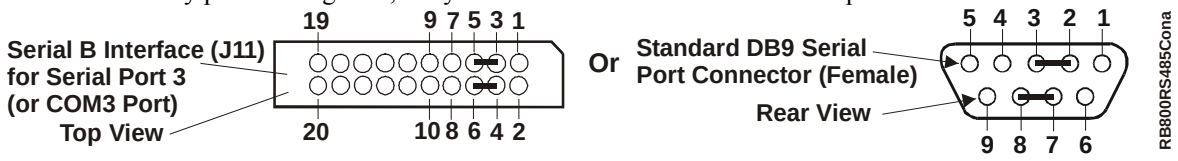


Figure 3-1. RS-485 Serial Port Implementation

Tables 3-8 and 3-9 list the pins and corresponding signals for the Serial A interface connector (J15A/B, Serial Ports 1 and 2) and Table 3-10 list the pins and corresponding signals for the Serial B interface connector (J11A/B, Serial Ports 3 and 4). Both serial A DB9 connectors use 9-pin consecutive (1, 6) and the Serial B connector uses 10-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing as shown in Figure 3-1.

Serial A Interface (J15A/B)

Table 3-8. Serial A (Serial 1) Interface Pin/Signal Descriptions (J15A)

Pin #	Signal	Description
1	DCD1*	Data Carrier Detect 1 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR1 as part of the DTR/DSR handshake.
2	RXD1	Receive Data 1 – Serial port 1 receive data in
3	TXD1	Transmit Data 1 – Serial port 1 transmit data out
4	DTR1*	Data Terminal Ready 1 – Indicates Serial port 1 is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
5	GND	Ground
6	DSR1*	Data Set Ready 1 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate.
7	RTS1*	Request To Send 1 – Indicates Serial port 1 is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.
8	CTS1*	Clear To Send 1 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
9	RI1*	Ring Indicator 1 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-9. Serial A (Serial 2) Interface Pin/Signal Descriptions (J15B)

Pin #	Signal	Description
1	DCD2*	Data Carrier Detect 2 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR2 as part of the DTR/DSR handshake.
2	RXD2	Receive Data 2 – Serial port 2 receive data in
3	TXD2	Transmit Data 2 – Serial port 2 transmit data out
4	DTR2*	Data Terminal Ready 2 – Indicates Serial port 2 is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
5	GND	Ground
6	DSR2*	Data Set Ready 2 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness.
7	RTS2*	Request To Send 2 – Indicates Serial port 2 is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
8	CTS2*	Clear To Send 2 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
9	RI2*	Ring Indicator 2 – Indicates external serial device is detecting a ring condition. Software initiates operation to answer and open the communications channel.

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Serial B Interface (J11A/B)

Table 3-10. Serial B Interface Pin/Signal Descriptions (J11A/B)

Pin #	Pin # DB9	Signal	Description
A1	1 (COM3)	DCD3*	Data Carrier Detect 3 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR3 as part of the DTR/DSR handshake.
A2	6	DSR3*	Data Set Ready 3 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR3 for overall readiness to communicate.
A3	2	RXD3 RX3-	Receive Data 3 – Serial port 3 receive data in. RX3- – If in RS485 or RS422 mode, this pin is Receive Data 3 -.
A4	7	RTS3* TX3+	Request To Send 3 – Indicates Serial port 3 is ready to transmit data. Used as hardware handshake with CTS3 for low level flow control. TX3+ – If in RS485 or RS422 mode, this pin is Transmit Data 3 +.
A5	3	TXD3 TX3-	Transmit Data 3 – Serial port 3 transmit data out. TX3- – If in RS485 or RS422 mode, this pin is Transmit Data 3 -.
A6	8	CTS3* RX3+	Clear To Send 3 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS3 for low level flow control. RX3+ – If in RS485 or RS422 mode, this pin is Receive Data 3 +.
A7	4	DTR3*	Data Terminal Ready 3 – Indicates Serial port 3 is powered, initialized, and ready. Used as hardware handshake with DSR3 for overall readiness to communicate.
A8	9	RI3*	Ring Indicator 3 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
A9	5	GND	Ground
A10	NC	NC	Not connected/Key
B11	1 (COM4)	DCD4*	Data Carrier Detect 4 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR4 as part of the DTR/DSR handshake.
B12	6	DSR4*	Data Set Ready 4 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR4 for overall readiness to communicate.
B13	2	RXD4 RX4-	Receive Data 4 – Serial port 4 receive data in. RX4- – If in RS485 or RS422 mode, this pin is Receive Data 4 -.
B14	7	RTS4* TX4+	Request To Send 4 – Indicates Serial port 4 is ready to transmit data. Used as hardware handshake with CTS4 for low level flow control. TX4+ – If in RS485 or RS422 mode, this pin is Transmit Data 4 +.
B15	3	TXD4 TX4-	Transmit Data 4 – Serial port 4 transmit data out. TX4- – If in RS485 or RS422 mode, this pin is Transmit Data 4 -.

Pin #	Pin # DB9	Signal	Description
B16	8	CTS4*	Clear To Send 4 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS4 for low level flow control.
		RX4+	RX4+ – If in RS485 or RS422 mode, this pin is Receive Data 4 +.
B17	4	DTR4*	Data Terminal Ready 4 – Indicates Serial port 4 is powered, initialized, and ready. Used as hardware handshake with DSR4 for overall readiness to communicate.
B18	9	NC	Not connected
B19	5	GND	Ground
B20	NC	NC	Not connected

Notes: The shaded area denotes power or ground. RS232 signals are listed first followed by RS485/RS422. The signals marked with * = Negative true logic.

USB Interfaces (J18A/B, J13A/B)

The I/O Hub (82801DBM) provides the USB solution for both legacy UHCI controllers and EHCI controller (USB 2.0) support. The Southbridge contains port-routing logic that determines which controller (UHCI or EHCI) handles the USB data signals. The PC-style (or Standard) connector (J18A/B) provides two of the four USB ports (USB0 and USB1). The other two USB ports share a single 10-pin header (J13A/B) on the board.

USB 2.0 Support

The Southbridge contains an Enhanced Host Controller Interface (EHCI) compliant host controller, which supports up to 4 high-speed USB 2.0 Specification compliant root ports. The higher speed USB 2.0 specification allows data transfers up to 480 Mbps using the same pins as the 4 Full-speed/Low-speed USB UHCI ports. The Southbridge port-routing logic determines which of the controllers (UHCI or the EHCI) processes the USB signals.

- One EHCI host controller for all four USB ports on connectors (J18A/B, and/or J13A/B)
- Supports USB v2.0 Specification
- Over-current fuses, located on the board, where USB0 and USB1 share a single fuse (F1) and USB2 and USB3 share a single fuse (F2). See Table 2-8.

Legacy USB Support

The Southbridge supports two USB Universal Host Controller Interfaces (UHCI) and each Host Controller includes a root hub with two separate USB ports each, for a total of 4 USB ports. The USB Legacy features implemented in the USB ports include the following:

- One root hub and two USB ports on connector (J18A/B)
- One root hub and two USB ports on connector (J13A/B)
- Supports USB v.1.1 and UHCI v.1.1 with integrated physical layer transceivers
- Supports improved arbitration latency for UHCI controllers
- UHCI controllers support Analog Front End (AFE) embedded cell instead of USB I/O buffers to allow for USB High-speed signaling rates
- Over-current fuses, located on the board, are used on all four USB ports

Primary USB0 and USB1 (J18A/B)

Table 3-11. USB 1 & 2 Interface Pin/Signal Descriptions (J18A/B)

Pin #	Signal	Description
1	+5V	+5V through a fuse (F1)
2	USBP0-	Universal Serial Bus Port 0 Data Negative
3	USBP0+	Universal Serial Bus Port 0 Data Positive
4	GND	Goes to ground thorough a choke
5	+5V	+5V through a fuse (F1)
6	USBP1-	Universal Serial Bus Port 1 Data Negative
7	USBP1+	Universal Serial Bus Port 1 Data Positive
8	GND	Goes to ground thorough a choke

Note: The shaded area denotes power or ground.

Secondary USB2 and USB3 (J13A/B)

Table 3-12 describes USB 2 & 3, J13A/B at 10-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-12. USB 2 & 3 Interface Pin/Signal Descriptions (J13A/B)

Pin #	Signal	Description
1, 2	+5V	+5V through a fuse (F2)
3	USBP2-	Universal Serial Bus Port 2 Data Negative
4	USBP3-	Universal Serial Bus Port 3 Data Negative
5	USBP2+	Universal Serial Bus Port 2 Data Positive
6	USBP3+	Universal Serial Bus Port 3 Data Positive
7, 8, 9, 10	GND	Goes to ground thorough a choke

Note: The shaded area denotes power or ground.

Ethernet Interfaces (J16, J17)

The Ethernet solution is provided by two Intel Ethernet controllers, Gigabit 82541GI (in GI, PI, or EI versions) and 82551ER for Port 2 and Port 1 respectively. Both controllers consist of a Media Access Controller (MAC) and a physical layer (PHY) combined into a single component solution.

Gigabit Ethernet Controller

The Intel® 82541GI Gigabit Ethernet Controller is 32-bit wide, PCI 2.3 compliant controller capable of transmitting and receiving data rates of 1000 Mbps, 100 Mbps, or 10 Mbps. The 82541GI's gigabit MAC design fully integrates the physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BaseT, 100BaseTX, and 10BaseT applications (802.3, 802.3u, and 802.3ab).

The 82541GI controller delivers high performance, PCI bus efficiency, with wide internal data paths to eliminate performance bottlenecks by efficiently handling large address and data words. The controller includes advanced interrupt handling features to limit PCI bus traffic and a PCI interface that maximizes the use of bursts for efficient bus usage. This controller caches up to 64 packet descriptors in a single burst with a large 64 kByte on-chip packet buffer to maintain superior performance with efficient PCI bandwidth use, as available PCI bandwidth changes. In addition, using hardware acceleration, the controller offloads tasks from the host controller, such as TCP/UDP/IP checksum calculations and TCP segmentation. The 82541GI Gigabit Ethernet controller supports or provides the following features:

- Low-latency transmit and receive queues to prevent waiting periods or buffer overflow
- Supports caches of 64 packet descriptors in a signal burst to provide efficient PCI bandwidth use
- Supports programmable host memory receive buffers (256 Bytes to 16 kBytes) and cache line sizes (16 to 256 Bytes)
- Supports wide optimized internal data paths for low latency data handling and superior DMA transfer rates
- Supports 64 kByte configurable Transmit and Receive FIFO buffers
- Supports simple programming model with descriptor ring transmit and receive management hardware
- Supports jumbo frames of 16 kByte transmit and receive packets
- Supports maximized system performance and throughput with interrupt reduction of transmit and receive operations
- Full duplex or half-duplex support at 10 Mbps, 100 Mbps, and 1000 Mbps
- Supports 1000BaseT 4-wire pairs and 10BaseT/100BaseT 2-wire pairs
- IEEE 802.3x 10BaseT/100BaseT/1000BaseT compatible physical layer to wire transformer
- IEEE 802.3ab Auto-Negotiation support, includes speed, duplex, and flow control
- IEEE 802.3ab PHY compliance and compatibility with Category-5 twisted pair cabling
- Implements latest DSP architecture with digital adaptive equalization, echo cancellation, and crosstalk cancellation to achieve high performance in noisy environments (high electrical/signal interference impairment)
- Supports transmit and receive IP, TCP, and UDP checksum offloading capabilities for lower CPU utilization
- Supports Transmit TCP segmentation and advanced packet filtering
- Supports system monitoring with industry standard consoles (SNMP and RMON statistic counters)
- Supports remote network management capabilities through DMI 2.0 and SNMP software (SDG 3.0, WfM 2.0, and PC2001 compliance)

- Supports a RJ-45 connector with magnetics integrated into connector
- Supports four-pair, 100 ohm, Category 5 UTP (Unshielded Twisted Pair) wiring

Tables 3-13 describes the pin-outs and signals of Gigabit Ethernet port, Ethernet Port 2.

Table 3-13. Ethernet Port 2 Pin/Signal Descriptions (J17)

Pin #	Signal	Description
1	MDI0+	Media Dependent Interface [0] – In MDI* configuration (1000BaseT), MDI[0]+/- corresponds to BI_DA+/-, and in MDI-X* configuration, MDI[0]+/- corresponds to BI_DB+/-. In MDI configuration (10BaseT or 100BaseT-TX), MDI[0]+/- is used for transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair.
2	MDI0-	
3	MDI1+	Media Dependent Interface [1] – In MDI configuration (1000BaseT), MDI[1]+/- corresponds to BI_DB+/-, and in MDI-X configuration, MDI[1]+/- corresponds to BI_DA+/-. In MDI configuration (10BaseT or 100BaseT-TX), MDI[1]+/- is used for transmit pair, and in MDI-X configuration, MDI[1]+/- is used for the receive pair.
6	MDI1-	
4	MDI2+	Media Dependent Interface [2] – In MDI configuration (1000BaseT), MDI[2]+/- corresponds to BI_DC+/-, and MDI-X configuration, MDI[2]+/- corresponds to BI_DD+/-. The 10BaseT or 100BaseT-TX are not used in this MDI pair.
5	MDI2-	
7	MDI3+	Media Dependent Interface [3] – In MDI configuration (1000BaseT), MDI[3]+/- corresponds to BI_DD+/-, and MDI-X configuration, MDI[3]+/- corresponds to BI_DC+/-. The 10BaseT or 100BaseT-TX are not used in this MDI pair.
8	MDI3-	
CT	CTap	Center Tap Ground – Goes to ground through 75 ohm resistor and 1.0 nF capacitor.
11	Speed	Speed LED – This signal line is shared with 1000BaseT and 100BaseT. The 10BaseT speed is indicated when no indication is seen for any activity.
12, 14	VCC3	LED Power – +3.3 volts for plus side of both LEDs
13	Link	Link/Activity LED – This signal indicates a Link is established or Activity is occurring over the port.
15, 16	GND	Shield Ground

Notes: The shaded area denotes power or ground. * MDI (medium dependent interface) is an Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a crossover cable. A medium dependent interface is also referred to as an MDI port or an uplink port. **MDI-X (or MDIX), short for medium dependent interface crossover (the "X" representing "crossover"), is an Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a crossover cable. MDIX is also referred to as an MDIX port.

10/100BaseT Ethernet Controller

Ethernet Port 1 uses an Intel 82551ER, 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the 82551ER to perform high-speed data transfers over the PCI bus. The 82551ER bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU.

- Backward software compatible to the 82559, 82558, and 82557
- Chained memory structure
- Full duplex or half-duplex support
- Full duplex support at 10 Mbps and 100 Mbps
- In half-duplex mode, performance is enhanced by a proprietary collision reduction mechanism.
- IEEE 802.3 10BaseT/100BaseT compatible physical layer to wire transformer
- Provides two LEDs for each port (speed, and link and activity are shared)
- Data transmission with minimum interframe spacing (IFS).
- IEEE 802.3u Auto-Negotiation support
- 3 kB transmit and 3 kB receive FIFOs (helps prevent data underflow and overflow)
- IEEE 802.3x 100BASE-TX flow control support
- Improved dynamic transmit chaining with multiple priorities transmit queues
- Supports a RJ-45 connector with magnetics integrated into the RJ-45 connector.

Tables 3-14 describes the pin-outs and signals of standard Ethernet port, Ethernet Port 1.

Table 3-14. Ethernet Port 1 Pin/Signal Descriptions (J16)

Pin #	Signal	Description
1	TX2+	Analog Twisted Pair Ethernet Transmit Differential Pair. These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair Cable (UTP). These signals interface directly with an isolation transformer.
2	TX2-	
3	RX2+	Analog Twisted Pair Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer.
6	RX2-	
4, 5, 7, 8	CT GND	Center Tap Ground – Center taps tied to ground through 75 ohm resistor and 1 nF capacitor.
9	ACT	Link/Activity signal indicates a Link is established or Activity is occurring
11	SPEED	Speed signal for 10BaseT or 100BaseT transfer rate
10, 12	+VCC	LED Power – +3.3 volts for plus side of both LEDs.

Note: The shaded area denotes power or ground.

Audio Interface (J4)

The audio solution on the ReadyBoard 800 is provided by the Southbridge (82801DBM) and the on-board Audio CODEC (ALC202A). These two chips use a digital interface to communicate between the two, which is defined by AC'97 and is revision 2.3 compliant. The input or output signals for the audio interface go through the 16-pin connector (J4) to an external cable and/or board, which has the respective audio connections. The PC Beep Speaker signal from the Southbridge is also fed to the on board Audio CODEC to provide a PC Beep signal for the stereo line out connections.

Audio CODEC (ALC202A) features

- AC'97 Rev 2.3 compliant
- 18-bit full duplex performance
- Variable sampling rate at 1 Hz resolution
- Stereo (Left and Right) Line In
- Stereo (Left and Right) Line Out
- Microphone (mono) in
- PC Beep speaker also fed to CODEC for signal to the Line Out (Left and Right) channels

Table 3-15 describes the Audio interface (J4) pin/signals on 16-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-15. Audio Interface Pin/Signal Descriptions (J4)

Pin #	Signal	Description
1, 3	NC	Not Connected
2, 4, 7, 8, 11, 12, 13, 14, 16	GND_AUD	Audio ground
5	LINEOUTL	Line Out signal left channel
6	LINEOUTR	Line Out signal right channel
9	LINE_IN_L	Line in signal left channel
10	LINE_IN_R	Line in signal right channel
15	MICIN	Microphone signal in

Note: The shaded area denotes power or ground.

Video Interfaces (J14, J21)

The Northbridge (82855GME) chip provides the graphics control and video signals to the traditional glass CRT monitors and the LVDS flat panel displays. The chip features are listed below:

- Supports 2D/3D graphics with extensive set of instructions including:
- 3D rendering and display
- BLT operations
- MPEG2 decode acceleration
- 3D overlay

CRT features:

- Provides an integrated 350 MHz, 24-bit RAMDAC to drive a progressive scan analog monitor and outputs to three 8-bit DACs provide the R, G, and B signals to the monitor.
- Supports resolutions up to 1600 x 1200 at 85 Hz refresh, or up to 2048x1536 at 75 Hz refresh
- Supports a maximum allowable video frame buffer size of 64 MB UMA (Unified Memory Architecture)
- Supports AGP 4X equivalent graphics performance

LVDS Flat Panel features:

- Supports an integrated dual channel LVDS flat panel interface
- Supports LVDS flat panel resolutions up to UXGA + (1600x1200)
- Supports a maximum pixel format of 18 bpp (with SSC supported frequency range from 35 MHz to 112 MHz (single channel/dual channel)
- Supports 1 or 2 channel LVDS outputs
- The 82855GME chip only supports the LVDS port on Pipe B of two pipelines
- Supports panel up-scaling (to fit a smaller source image onto a specific native panel size) as well as panning and centering

Table 3-16 describes the CRT pin/signals of a standard 15-pin video connector. Table 3-17 describes the LVDS pin/signals on 30-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

CRT Interface (J21)

Table 3-16. CRT Interface Pin/Signal Descriptions (J21)

Pin #	Signal	Description
1	RED	Red – This is the Red analog output signal to the CRT.
2	GREEN	Green – This is the Green analog output signal to the CRT.
3	BLUE	Blue – This is the Blue analog output signal to the CRT.
4	NC	Not connected
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	NC	Not connected
10	GND	Ground
11	NC	Not connected
12	DDDA	Display Data Channel Data – This signal line provides information to the CPU through the Northbridge about the monitor type, brand, and model. This is part of the Plug and Play standard developed by the VESA trade association.
13	HSYNC	Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT.
14	VSYNC	Vertical Sync – This signal is used for the digital vertical sync output to the CRT.
15	DDCLK	Display Data Channel Clock – This signal line provides the data clock signal to the CPU through the Northbridge from the monitor. This is part of the Plug and Play standard developed by the VESA trade association.

Note: The shaded area denotes power or ground.

LVDS Interface (J14)

Table 3-17. LVDS Interface Pin/Signal Descriptions (J14)

Pin #	Signal	Description	Line	Channel
1	+12V	+12V source		
2	VCC_LCD	+3.3V or +5V Depends on JP4 setting (+3.3V **Default**)		
3	GND	Ground	Gnd	
4	GND	Ground		
5	LVDSB_Clk+	Clock Positive Output	Clk	Channel 2
6	LVDSB_Clk-	Clock Negative Output		
7	LVDSB_Y3+	Data Positive Output	3	
8	LVDSB_Y3-	Data Negative Output		
9	LVDSB_Y2+	Data Positive Output	2	
10	LVDSB_Y2-	Data Negative Output		
11	LVDSB_Y1+	Data Positive Output	1	
12	LVDSB_Y1-	Data Negative Output		
13	LVDSB_Y0+	Data Positive Output	0	
14	LVDSB_Y0-	Data Negative Output		
15	LVD_BKLTCtl	Backlight Control		
16	LVD_EN	LCD enable		
17	LVDSA_Clk+	Data Positive Output	Clk	Channel 1
18	LVDSA_Clk	Data Negative Output		
19	LVDSA_Y3+	Data Positive Output	3	
20	LVDSA_Y3	Data Negative Output		
21	LVDSA_Y2+	Data Positive Output	2	
22	LVDSA_Y2	Data Negative Output		
23	LVDSA_Y1+	Data Positive Output	1	
24	LVDSA_Y1-	Data Negative Output		
25	LVDSA_Y0+	Data Positive Output	0	
26	LVDSA_Y0-	Data Negative Output		
27	LVDS_DDCPClk	Clock		
28	LVDS_DDCPData	Data		
29	LCD_BKLEN	Backlight Enable		
30	NC	Not connected		

Note: The shaded area denotes power or ground.

NOTE Pins 17-26 constitute 1st channel interface of two channels, or a single channel interface.

Pins 5-14 constitute 2nd channel interface of two channels.

Miscellaneous

Utility Interface (J12)

- Power-On – This control signal is provided externally through a switch by connecting ground to pin-1 on the Utility connector (J12).
- Reset Switch – This signal is provided externally through a switch by connecting ground to pin-3 on the Utility connector (J12). This signal line is shared with Reset Switch (SW1).
- PC Beep Speaker – The output signals from the Southbridge (82801DBM) and the Super I/O (W83627HF) are fed to pin-5 of the Utility connector (J12) through an OR circuit, and in conjunction with the +5V (pin-4), drives an external PC Beep speaker. The PC Beep speaker signal from the Southbridge is also fed to the on-board Audio CODEC to provide a PC Beep signal for the Line out connections.

Table 3-18. Utility Interface Pin/Signal Descriptions (J18)

Pin #	Signal	Description
1	PS_On	Power On input (connect between pins 1 & 2)
2	GND	Ground
3	RST_SW	Reset Switch input or output (connect between pins 3 & 2)
4	+5V	+5 Volts
5	Speaker	PC Beep Speaker + Output (connect between pins 5 & 4)

Note: The shaded area denotes power or ground.

Reset Switch (SW1)

The reset switch (SW1), located on the board edge, provides an internal reset signal (momentary ground) to the ReadyBoard 800. The reset switch (SW1) shares the reset line with pin-3 of the Utility interface (J12).

Keyboard/Mouse Interface (J19)

The PS/2 Keyboard and Mouse signal lines share the same mini-DIN connector (J19). A PS/2 Y-cable is used to connect to the PS/2 connector (J19), on the board edge.

NOTE	Each device has a specific connector on the Y-cable. The Super I/O senses when each device is connected and provides the appropriate signals.

Table 3-19. Keyboard/Mouse Interface Pin/Signal Descriptions (J19)

Pin #	Signal	Description
1	KB_Data	Keyboard data
2	MS_Data	Mouse Data
3	GND	Ground
4	+KBMS	Keyboard/Mouse Power (+ 5V +/- 5%)
5	KB_Clk	Keyboard Clock
6	MS_Clk	Mouse Clock
7, 8, 9	GND	Ground (Used for grounding the shield on the connector

Note: The shaded area denotes power or ground.

Infrared (IrDA) Port (J9)

The Infrared Data Association (IrDA) signals pass through a two-way communications header for an external IrDA device using infrared as the transmission medium. There are two basic infrared implementations provided; the Hewlett-Packard Serial Infrared (HPSIR) and the Amplitude Shift Keyed Infrared (ASKIR) methods. HPSIR is a serial implementation of infrared developed by Hewlett-Packard. The IrDA (HPSIR and ASKIR) signals share the same header as the IrDA model select signals. These signals are operating system (OS) and/or application dependent and will be configured and enable based on the user's application of these signals.

The HPSIR method allows serial communication at baud rates up to 115k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a single infrared pulse is sent at the beginning of the serial bit time. A one is sent when no infrared pulse is sent during the bit time.

The Amplitude Shift Keyed infrared (ASKIR) allows serial communication at baud rates up to 19.2 k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a 500 kHz waveform is sent for the duration of the serial bit time. A one is sent when no transmission is sent during the serial bit time.

Both of these methods require an understanding of the timing diagrams provided in the Super I/O controller (W83627HF) specifications available from the manufacture's web site and referenced earlier in this manual. For more information, refer to the Winbond W83627HF specifications and the Infrared Data Association web site at http://www.irda.org.

NOTE	For faster speeds and infrared applications not covered in this brief description, refer to the W83627HF chip specifications by Winbond Electronics Corp.

Table 3-20. Infrared Interface Pin/Signal Descriptions (J9)

Pin #	Signal	Description
1	+5V	+5V
2	IRTX	IR Transmit Data
3	IRSel	IR Mode Select
4	IRRX	IR Receive Data
5	GND	Ground

Note: The shaded area denotes power or ground.

Real Time Clock (RTC)

The ReadyBoard 800 contains a Real Time Clock (RTC). The CMOS RAM is backed up with a Lithium Battery. If the battery is not present, the BIOS has a battery-free boot option to complete the boot process.

Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event the BIOS settings you've selected prevent you from booting the system, but does not reset the CMOS or change the Time & Date in the BIOS. Refer to the CMOS Normal/Clear jumper (JP2) to reset the BIOS and change the Time & Date.

By using the Oops! jumper you can prevent the current BIOS settings in Flash memory from being loaded, forcing the use of the default BIOS settings. Connect the DTR pin to the RI pin on Serial port 1 (COM 1) prior to applying power to prevent the current BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and go into BIOS Setup. Change the desired BIOS settings, or select the default settings, and save the changes before rebooting the system.

To convert the Serial 1 interface to an Oops! jumper, short together the DTR (4) and RI (9) pins on the Serial Port 1 DB9 connector as shown in Figure 3-2.

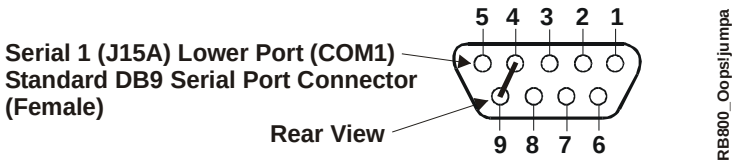


Figure 3-2. Oops! Jumper Connection

User GPIO Signals (J8)

The ReadyBoard 800 provides eight GPIO pins for custom use and the signals are routed to the J8 connector. Ampro has provided sample applications showing how to use the GPIO pins in the Miscellaneous Source Code Examples subdirectory, under the ReadyBoard 800 Software menu on the ReadyBoard 800 Doc & SW CD-ROM, *(CD-ROM\Software\Misc\GPIO)*.

For more information about the GPIO pin operation, refer to the datasheet specifications or Programming Manual for the Super I/O (W83627HF) controller at:

http://www.winbond-usa.com/products/winbond_products/pdfs/PCIC/627hf.pdf

Table 3-21 list the GPIO pin/signals on 10-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-21. User GPIO Signals Pin/Signal Descriptions (J8)

Pin #	Signal	Description
1	GND	Ground
2	+5V	+5 VDC
3	GPIO4	User defined
4	GPIO5	User defined
5	GPIO6	User defined
6	GPIO7	User defined
7	GPIO0	User defined
8	GPIO1	User defined
9	GPIO2	User defined
10	GPIO3	User defined

Note: The shaded area denotes power or ground.

Temperature Monitoring

The Super I/O controller (W83627HF) performs the temperature monitoring function and has inputs directly from two thermistors on the board. One thermistor is located near the CPU and the other thermistor is located near the I/O Hub (Southbridge).

NOTE	The ReadyBoard 800 requires a heatsink for all processors, but no fan.

Serial Console

The ReadyBoard 800 supports the serial console (or console redirection) feature. The serial console can be accessed by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Serial Console Setup

The serial console feature is implemented by connecting a standard null modem cable or a modified serial cable (or "Hot Cable") between one of the serial ports, such as Serial 1 (J15A), and the serial terminal or a PC with communications software. The BIOS Setup Utility controls the serial console settings on the ReadyBoard 800. Refer to Chapter 4, BIOS Setup to set the serial console option, using a serial terminal, or PC with communications software.

Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, certain pins must be shorted together at the Serial port connector or on the DB9 connector. For example, short the RTS (7) and RI (9) on the respective DB9 port connector as shown in Figure 3-3.

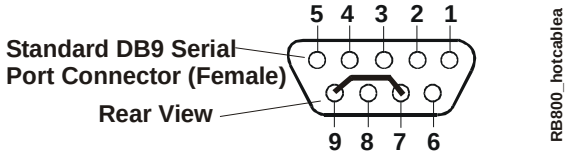


Figure 3-3. Hot Cable Jumper

Watchdog Timer (WDT)

The watchdog timer (WDT) restarts the system if a mishap occurs, ensuring proper start-up after the interruption. Possible problems include failure to boot properly, loss of control by the application software, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (watchdog timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT in the Advanced BIOS Features of BIOS Setup. Set the WDT for a time-out interval in seconds, between 2 and 255, in one second increments. Ensure you allow enough time for the operating system (OS) to boot. The OS or application must tickle (turnoff) the WDT before the timer expires. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some Ampro Board Support Packages provide an API interface to the WDT. The application must tickle (turnoff) the WDT before the timer expires or the system will be reset. The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

- Watchdog Code examples – Ampro has provided source code examples on the ReadyBoard 800 Doc & SW CD-ROM illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file in the Miscellaneous Source Code Examples subdirectory, under the ReadyBoard 800 Software menu on the ReadyBoard 800 Doc & SW CD-ROM.

Power Interfaces (J1, J2)

The ReadyBoard 800 uses various voltages onboard, but only one voltage is required externally (+5 volts) through the external connector, which uses a 4-pin header with 0.200" (5.08 mm) spacing. The optional +12V volts is also provided on the input connector, but is not used on the board except for LCD panel power and for PCI or optional ISA bus power. All other onboard voltages, including the CPU core voltages, are derived from the externally supplied +5 volts DC +/- 5%.

Power In Interface (J2)

Table 3-27 list the pin outs and signals for Power interface connector (J2).

Table 3-22. Power In Interface Pin/Signal Descriptions (J2)

Pin #	Signal	Description
1	+5V	+5.0 volts DC +/- 5%
2	GND	Ground
3	GND	Ground
4	+12V	This +12V is for PCI-104 bus power and LCD power only (optional).

Notes: The shaded area denotes power or ground. The +12V on the Power Interface connector (J2) is used for the LCD panel, PCI Bus, and optional ISA Bus power, but may also be supplied externally.

Power-On Interface (J1)

The signals on this connector allow the ATX power supply to be turned off (soft off) by the ReadyBoard. If you use a non-ATX power supply (lab supply or AT power supply) you must connect J1 pin-1 to +5V (pin-1 on J2) to enable the ReadyBoard 800 to power on completely. However, if you use a non-ATX power supply, then you won't have the soft off feature normally provided by ATX power supplies.

Table 3-23. Power-On Header Pin/Signal Descriptions (J1)

Pin #	Signal	Description
1	VCCSB	+5V suspend voltage (+5V, 100mA Standby) – This voltage is supplied from ATX power supply. This voltage is required for normal operation.
2	GND	Ground
3	PS_ON*	Power Supply On – This signal is sent to the ATX power supply by the ReadyBoard 800 to turn On the ATX power supply. This signal can also be used to turn Off the ATX power supply or go into a suspended or standby state.

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

NOTE	If the +5V suspend voltage is not present on the Power-On header (J1, pin-1) the ReadyBoard 800 will not completely power on. The board will have power (+5V), but it will not start the boot process and will never power up completely.

Optional CPU Fan (J7)

Table 3-24 lists the pins and signals of the optional CPU Fan and it has 3 pins, single row, with 0.100" pin spacing.

Table 3-24. Optional CPU Fan (J7)

Pin #	Signal	Description
1	Fan_Tach	Fan Tachometer – This signal indicates Fan speed.
2	+12V	+12.0 volts DC +/- 5%
3	GND	Ground

Note: The shaded area denotes power or ground.

Power and Sleep States

The following information only applies if an ATX power supply is used to provide power to the ReadyBoard 800. If a non-ATX power supply is used, then the ReadyBoard 800 is only controlled by the Power On/Off switch on the power supply and the various sleep states are not available. The sleep states are OS dependent and not available if your OS does not support power management based on the ACPI standard.

Power On Switch

The Power On switch turns the ReadyBoard 800 and its attached power supply to a fully On condition, if you are using an ATX power supply. Normally, if the operating system (OS) supports sleep states, the OS will turn Off the ReadyBoard and its power supply during the OS shut down process. If the OS supports sleep states, the Power On button typically, will also transition the ReadyBoard and its power supply between a fully Powered On state, various sleep states depending on the OS control setting, and a fully Powered Off state. If the OS does not support sleep states, then the Power On button only turns power On or Off to the ReadyBoard 800.

An OS supporting ACPI, typically allows the Power-On switch to be configured through a user interface. The Power-On switch for the ReadyBoard 800 is provided externally by connecting a momentary switch between pins-1 and -2 on the Utility connector (J12). The power on signal occurs when ground is placed on pin-1 of J12.

Sleep States (ACPI)

The ReadyBoard 800 supports the ACPI (Advanced Configuration and Power Interface) standard, which is a key component of certain Operating Systems' (OS's) power management. The supported features (sleep states) listed here are only available when an ACPI-compliant OS is used for the ReadyBoard, such as Windows 98/2000/ME/XP. The term "sleep" state refers to a low latency (reduced power consumption) state, which can be re-started (awakened) restoring full operation to the ReadyBoard 800.

In these various sleep states, the ReadyBoard 800 appears to be off, indicated by such things as no display on the attached monitor and no activity for the connected CD-ROM or hard drives. Normally, when a computer detects certain activity (i.e. power switch, mouse, keyboard, or certain types of LAN activity), it returns to a fully operational state.

NOTE	Currently, the Power-On switch is the only activity that will wake the ReadyBoard 800 from a powered down state, such as Standby (S1), Hibernate (S4) and Power Off (S5).

The ReadyBoard 800 supports at least four ACPI power states, depending on the operating system used and its ability to manage sleep states. Typically, the power on switch is used to wake up from a sleep state, or transition from one state to another, but this is dependent on the operating system.

- 1st state is normal Power On (S0).
  - To go to a fully powered on state, the ReadyBoard 800 must either be powered Off (S5), or in a sleep state (S1 or S4), and then the Power-On switch is pressed for less than 4 seconds (default).
  - The ReadyBoard 800 can transition from this state (S0) to the various states described below, depending on the power management capability of the OS and how it is programmed.
- 2nd state is a standby state (S1).

  In this state there are no internal operations taking placing, except for the internal RTC (real time clock) and the contents of RAM. This includes no activity for the CPU, CD-ROM, or hard disk drives. The ReadyBoard 800 appears to be off including the Power On LED.
  - Normally, to enter this sleep state, the ReadyBoard 800 must be fully powered on (S0) and the OS transitions the ReadyBoard into this standby state (S1) under user control.
  - To exit this sleep state, typically the Power-On switch is used to wake up the ReadyBoard 800 to restore full operation, including the Power On LED. Typically, pressing the Power-On switch for less than 4 seconds (default) will restore full operation.
- 3rd state is a hibernate or suspend-to-disk state (S4).

  In this state there are no internal operations taking placing, except for the internal RTC. This includes no activity for the CPU, CD-ROM, or hard disk drives. The ReadyBoard 800 appears to be off, including the Power On LED. Your system will take longer to wake-up in this sleep state, however, since your data is saved to the disk, it is more secure and should not be lost in the event of a power failure.
  - To enter a hibernate or suspend-to-disk state, the ReadyBoard 800 must be fully powered on and the OS transitions the ReadyBoard 800 into this sleep state (S4) under user control.
  - To exit this sleep state, typically pressing the Power-On switch for less than 4 seconds (default) will restore full operation.
- 4th state is the normal power Off or shutdown (S5).

  All activity stops except the internal clock, unless the power cord is removed from the power source.
  - To go to a fully powered down state, the ReadyBoard 800 must either be powered On, or in a sleep state, and then the Power-On switch is pressed for more than 4-to-6 seconds.
  - To go to a fully powered up state, press the Power-On switch for less than 4 seconds (default) and full operation is restored.

The OS may provide additional programming features to change the activation time for each state, and to shutdown or transition the ReadyBoard 800 at certain times, depending on the way the OS interface is programmed. Refer to the OS vender's documentation for power management under the ACPI standard.

NOTE	Some operating systems use the keyboard, mouse, Wake-on-Ring (serial port), and Wake-on-LAN (Ethernet port) as an activity to wake up the system from a sleep state. Currently, the ReadyBoard 800 only supports the Power On switch as the wake up activity.

Chapter 4 BIOS Setup Utility

Introduction

This chapter describes the BIOS Setup Utility menus and the various screens used for configuring the ReadyBoard 800. Some features in the Operating System or application software may require configuration in the BIOS Setup screens.

This section assumes the user is familiar with general BIOS Setup and does not attempt to describe the BIOS functions. Refer to the appropriate PC reference manuals for information about the onboard ROM-BIOS software interface. If Ampro has added to or modified the standard functions, these functions will be described.

Most of the ReadyBoard 800 options are controlled by BIOS Setup Utility. BIOS Setup is used to configure the board, modify the fields in the Setup screens, and save the results in the onboard configuration memory. Configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and the flash memory.

The Setup information is retrieved from configuration memory when the board is powered up or when it is rebooted. Changes made to the Setup parameters, with the exception of the time and date settings, do not take effect until the board is rebooted.

Setup is located in the ROM BIOS and can be accessed, while the board is in the Power-On Self Test (POST) state, just before starting the boot process. The screen displays a message indicating when you can press <Del> to enter the BIOS Setup Utility.

The ReadyBoard 800 BIOS Setup is used to configure items in the BIOS using the following menus:

- BIOS and Hardware Settings
- Reload Initial Settings
- Load Factory Default Settings
- Exit, Saving Changes
- Exit, Discarding Changes

Table 4-1 summarizes the list of BIOS menus and some of the features available for ReadyBoard 800. The BIOS Setup menu offers the menu choices listed above and the related topics and screens are described on the following pages.

Accessing BIOS Setup (VGA Display)

To access BIOS Setup using a VGA display for the ReadyBoard 800:

1. Turn on the VGA monitor and the power supply to the ReadyBoard 800.
2. Start Setup by pressing the [Del] key, when the following message appears on the boot screen.

```
Hit <Del> if you want to run SETUP
```

NOTE	If the setting for *Memory Test* is set to Fast, you may not see this prompt appear on screen if the monitor is too slow to display it on start up. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup.

3. Use the <Enter> key to select the screen menus listed in the opening BIOS screen. See Figure 4-1.
4. Follow the instructions at the bottom of each screen to navigate through the selections and modify any settings.

Accessing BIOS Setup (Serial Console)

Entering the BIOS Setup, in serial console mode, is very similar to the steps you use to enter BIOS Setup with a VGA display, except the actual keys you use.

1. Set the serial terminal, or the PC with communications software to the following settings:
   - 115k baud
   - 8 bits
   - One stop bit
   - No parity
   - No hardware handshake
2. Connect the serial terminal, or the PC with serial terminal emulation, to Serial Port 1 or Serial Port 2 of the ReadyBoard 800.
   - If the BIOS option, Serial Console is set to [Enable], use a standard null-modem serial cable.
   - If the BIOS option, Serial Console is set to [Hot Cable], use the modified serial cable described in Chapter 3, under Hot (Serial) Cable.
3. Turn on the serial terminal or the PC with serial terminal emulation and the power supply to the ReadyBoard 800.
4. Start Setup by pressing the Ctrl–c keys, when the following message appears on the boot screen.

```
Hit ^C if you want to run SETUP
```

5. Use the <Enter> key to select the screen menus listed in the opening BIOS screen. See Figure 4-1.

NOTE	The serial console port is not hardware protected, and is not listed in the COM table within BIOS Setup. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

Table 4-1. BIOS Setup Menus

BIOS Setup Menu	Item/Topic
BIOS and Hardware Settings	Date and Time Drive Assignment Boot Order Drive and Boot Options Keyboard & Mouse settings User Interface options Memory settings Power Management Advanced Features On-Board Features (Serial, Parallel, USB, Video, Audio, etc.) PCI Settings Plug and Play Options IRQs and DMA Settings
Reload Initial Settings	Resets the BIOS (CMOS) to the most recent settings
Load Factory Default Settings	Resets BIOS (CMOS) to factory settings
Exit, Saving Changes	Writes all changes to BIOS (CMOS) and exits
Exit, Discarding Changes	Closes BIOS without saving changes except time and date

BIOS Menus

BIOS Setup Opening Screen

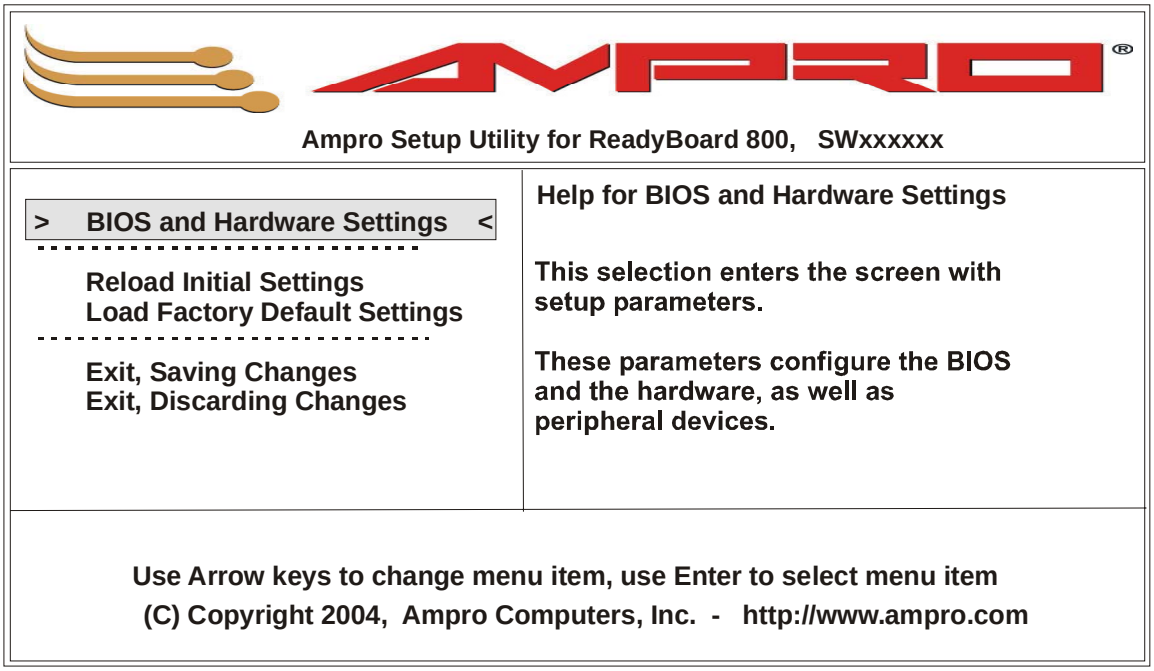


Figure 4-1. Opening BIOS Screen

NOTE	For the most current BIOS Information, refer to the Hardware Release Notes provided as hard copy in the shipping container.

NOTE	The default values or the typical settings are shown highlighted (**bold text**) in the list of options on the following pages. Refer to the bottom of the BIOS screens for navigation instructions and when making selections.

BIOS Configuration Screen

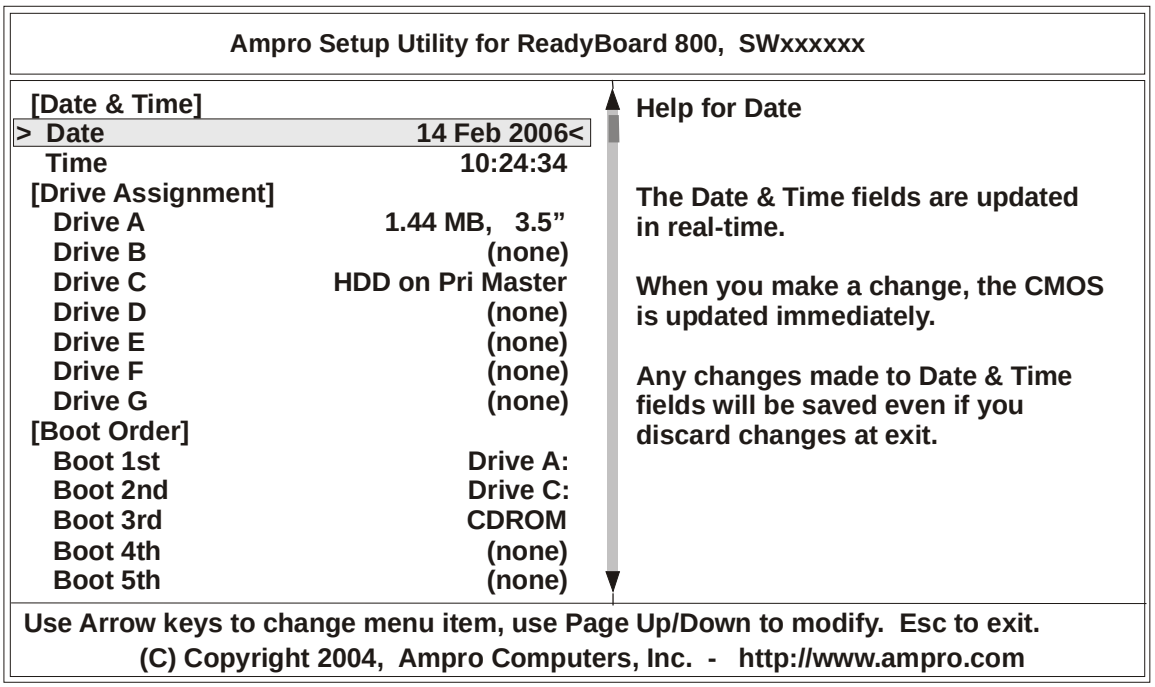


Figure 4-2. Modifying Setup Parameters Screen

- **Date & Time**
  - DATE (dd:mm:yyyy) – This requires the alpha-numeric entry of the day of the month, calendar month, and all 4 digits of the year, indicating the century plus year (14 Feb 2006).
  - Time (hh:mm:ss) – This requires 24 hour Clock setting in hours, minutes, and seconds

Drive Configurations and Boot Options

- **Drive Assignments**
  - Drive A – [none], [360 kB, 5.25"], [1.2 MB, 5.25"], [720 kB, 3.5"], [**1.44 MB, 3.5"],** [2.88 MB, 3.5"], or [USB Floppy]

NOTE	If USB Boot Support is [Disabled], the USB Floppy selections are invalid and Drive B must be set to [none]. See Table 4-2 Floppy Drive Setting.

  - Drive B – [**none**], [360 kB, 5.25"], [1.2 MB, 5.25"], [720 kB, 3.5"], [1.44 MB, 3.5"], [2.88 MB, 3.5"], or [USB Floppy]

NOTE	If a compact flash device is used in the system, it is always configured as [HDD/CF Sec Master or Slave] as Drive C or D.

  - Drive C – [none], [**HDD on Pri Master**], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]

NOTE	The BIOS does not support a break in the drive order, that is, Drive C can not be listed as [none] when the boot device is Drive D.

- Drive D – [**none**], [HDD on Pri Master], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]

Table 4-2. Floppy Drive BIOS Settings

# of Floppy Drive(s)	BIOS Settings
None	• Set Drives A and B to [None]
(1) Non-USB Floppy*	• Configure Drive A to floppy drive type (For example, [1.44 MB, 3.5"] • Set Drive B to [None]
(1) USB Floppy	• Set USB Boot Support to [Enable] • Set Drive A to [USB Floppy] • Set Drive B to [None]
(2) Floppy drives (1 USB Floppy and 1 non-USB Floppy drive*)	• Set USB Boot Support to [Enable] • Configure one drive (Drive A or B) to floppy drive type. (For example, [1.44 MB, 3.5"]) • Set one drive (Drive B or A) to [USB Floppy]

Note: *A standard 34-pin floppy cable has a twist in the cable wiring between the Floppy A and B connectors, where Floppy B has the straight through cable (non-twist) and is the middle connector. Due to the ReadyBoard 800's internal configuration and the cable supplied, there is only one physical connector available (the Floppy B connector, because the Floppy A connector is not provided).

NOTE Ampro does not recommend connecting a USB boot device to the ReadyBoard 800 through an external hub. Instead, connect the USB boot device directly to the ReadyBoard 800.

Any USB (block) device that emulates a hard disk drive can be used when [USB HDD] is set as the drive option. This includes various storage media types, such as USB hard disk drives, USB CD-ROMs, compact flash cards, and Flash or Thumb drives. Refer also to Boot Order settings, USB Boot Support under Advanced features, and USB (device enable) under On-Board Controllers for USB Drive boot order, USB Boot Enable, and the number of USB ports enabled, respectively.

- Drive E – [**none**], [HDD on Pri Master], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]
- Drive F – [**none**], [HDD on Pri Master], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]
- Drive G – [**none**], [HDD on Pri Master], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]

- **Boot Order**
  - Boot 1st – [none], [**Drive A**], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
  - Boot 2nd – [none], [Drive A], [Drive B], [**Drive C**], [Drive D], [CDROM], [Alarm], or [Reboot]

NOTE The [Alarm] option sounds beeps on the PC speaker and can be listed, like [Reboot], as the last boot device to indicate no bootable device was found.

Any of the drives can be listed as a boot drive.

- Boot 3rd – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
- Boot 4th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
- Boot 5th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
- Boot 6th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]

NOTE	The default Boot order is, A, C, CD-ROM, and the BIOS will start its search for a bootable device in drive A, then C, then CD-ROM. If no bootable device is found, the screen will display "No Bootable Device Available" and the boot process will stop, allowing you to select from: R – for Reboot, or S – for Setup. If you do not choose R or S, the boot process stops, until you intervene, unless you have selected [Reboot] as an option.

- **Drive and Boot Options**
  - Floppy over Parallel – [Disabled] or [**Enabled**]
    * If [Enabled], this option selects the Floppy Drive instead of the Parallel port on the shared connector.
    * If [Disabled], this option selects the Parallel port instead of the Floppy Drive on the shared connector.
  - Floppy Seek – [**Disabled**] or [Enabled]
  - Hard disk Seek – [**Disabled**] or [Enabled]
  - Floppy Swap – [**Disabled**] or [Enabled]
  - Boot Method – [**Boot Sector**] or [Windows CE]

    Boot Sector is the traditional method for booting the system. If [Windows CE] is selected, the BIOS attempts to load the NK.BIN file from the root directory of each boot device.
  - Primary IDE Cable – [Auto], [**40 Wire**], or [80 Wire]

    Setting these fields to [Auto], causes the BIOS to query the attached IDE device to determine the type of IDE cable used. If the BIOS detects [40 wire], or you select it, the BIOS will not use UDMA-66 or faster mode when sending signals to/from the IDE device.
  - Secondary IDE Cable – [Auto], [**40 Wire**], or [80 Wire]
  - Secondary Master ATA mode – [**LBA**], [Physical], or [Phoenix]

    This default option (LBA - Logical Block Address) could be used on any IDE device, including compact flash cards. However, this option specifically allows you to select between the existing formats used to format your compact flash card as the Secondary Master device.

NOTE	Always partition and format the compact flash on the ReadyBoard 800. The options listed here allow use any one of the three common geometries available for compact flash cards when configuring the file system for the ReadyBoard 800. The LBA (Logical Block Address) is set as the default method because it can handle larger drives and is the newest method available. The other common methods that may be encountered are Physical (below 512 MB) or Phoenix (physical above 512 MB).

  - Secondary Slave ATA mode – [**LBA**], [Physical], or [Phoenix]

    This default option (LBA - Logical Block Address) could be used on any IDE device, including compact flash cards. However, this option specifically allows you to select between the existing formats used to format your compact flash card as the Secondary Slave device.

User Interface Options

- **Keyboard and Mouse** (Configuration)
  - Numlock – [**Disabled**] or [Enabled]
  - Typematic – [Disabled] or [**Enabled**]

    These fields are used to set parameters for the keyboard.

    - Delay – [**250 ms**], [500 ms], [750 ms], or [1000 ms]

      This field determines how many milliseconds the keyboard controller waits before stating to repeat a key, if the key is held down on the keyboard.

    - Rate – [**30 cps**], [24 cps], [20 cps], [15 cps], [12 cps], [10 cps], [8 cps], or [6 cps]

      This field determines the rate, in characters per second, the keyboard controller will repeat a key, if the key is held down on the keyboard.

  - Initialize PS/2 Mouse – [Disabled] or [**Enabled**]
    * If this field is set to [Enabled], the BIOS will initialize the PS/2 mouse.
    * If the PS/2 mouse is [Disabled], then the BIOS will not initialize the PS/2 mouse, which may cause the mouse not to be recognized by the Operating System.
- User Interface
  - Show "Hit <Del>…" – [Disabled] or [**Enabled**]

    This field, if [Enabled], will place "Hit Del" on screen during the boot process, to indicate when you may press "Del" to enter the BIOS Setup menus.
  - F1 Error Wait – [**Disabled**] or [Enabled]
    * If this field is [Enabled], the BIOS will display an Error message indicating when an error has occurred during POST (power on self test) and wait for you to respond by hitting the F1 key.
    * If [Disabled] and an error occurs during POST, the BIOS will attempt to continue the boot process.
  - Config Box – [Disabled] or [**Enabled**]

    This field, if [Enabled], displays the Configuration Summary Box, which lists the configuration information for the system, at the completion of POST, but before the Operating System is loaded.
  - Splash Screen – [**Disabled**] or [Enabled]
    * If Splash Screen is [Enabled] it stays on screen, until the booted Operating System changes it, if the Config Box option is Disabled.
    * If Config Box option is [Enabled], the Splash Screen stays on screen until the Config Box is displayed.

      The Splash Screen is a graphical image displayed as the default (Ampro Splash Screen) or a user customized image on screen. Refer to the Splash Screen Customization topic later in this chapter for instructions on how to customize the splash screen.

Memory Control Options

- **Memory**
  - Memory Test – [**Fast**], [Standard], or [Exhaustive]
    - * If this field is set to [Fast], only basic memory tests are performed during POST to shorten POST time.
    - * If this field is set to [Standard], more than basic tests are performed, but POST time is increased.
    - * If this field is set to [Exhaustive], more rigorous tests are performed on memory, but this takes a significant amount of time for POST to complete.
  - Memory Hole – [**Disabled**], or [1MB]

    This field specifies the size of an optional memory hole, below 16 MB. Access to the memory addresses inside the memory hole region are forwarded to the PC/104 bus, where memory mapped PC/104 devices have access.
  - Shadow D000-D3FF – [**Disabled**] or [Enabled]

    These Shadow fields specify if BIOS option ROMs in the indicated segments should be shadowed to RAM. Shadowing option ROMs can potentially speed up the operation of the system. The indicated segments are only for option ROMs present on add-on PC/104 and PC/104-Plus cards.
  - Shadow D400-D7FF– [**Disabled**] or [Enabled]
  - Shadow D800-DBFF – [**Disabled**] or [Enabled]
  - Shadow DC00-DFFF – [**Disabled**] or [Enabled]

Power Management and Advanced User Options

- **Power Management**
  - ACPI – [Disabled] or [**Enabled**]
    - * If this field is set to [Enabled], the Advanced Configuration and Power Interface API is turned on and available for any Operating System that supports ACPI power states.
  - APM – [**Disabled**] or [Enabled]
    - * If this field is set to [Enabled], the Advanced Power Management API is turned on.

      This power management feature is an older standard and may not be as widely supported today as it once was. The current preference for power management control is ACPI.
- **Advanced features**
  - Post Memory Manager – [**Disabled**] or [Enabled]
    - * If this field is set to [Enabled], the Post Memory Manger API is turned on. The Post Memory Manger can be used by BIOS option ROMs to allocate memory in a well defined way.
  - CPU Serial Number – [Disabled] or [**Enabled**]
    - * If this field is set to [Enabled], the internal serial number in the Intel CPU is accessible by the Operating System and/or Applications that can make use of this information..
  - Watchdog Timeout (sec) – [select a number between 255 seconds and 1 second, in 1 second increments] or [**Disabled**]
    - * If this field is enabled by selecting a time interval (1 to 255 seconds), it will direct the watchdog timer to reset the system if it fails to boot the OS properly. Refer to the watchdog timer section in Chapter 3 for more information.

- Serial Console – [**Hot Cable**] or [Enabled]

  * If the [Hot Cable] option is selected, it only allows serial console (console redirection) operation when a Hot Cable is actually connected to Serial 1 or Serial 2 (COM 1 or 2). Use the modified serial cable described in Chapter 3, under Hot (Serial) Cable.

  * If the [Enabled] option is selected, it instructs the BIOS to operate in the serial console (console redirection) mode at all times with the serial port selected in the Serial Console > Port field listed below. Use a standard null-modem serial cable.

  * If a Hot Cable is connected to the other port (port not selected) the Hot Cable will override the settings in this field [Enabled] and the Serial Console > Port field.

- Port – [**3F8h**], [2F8h], [3E8h], or [2E8h]

  This field selects the COM (Serial) port address used for serial console (console redirection) when [Enabled] has been selected in Serial Console. Use a standard null-modem serial cable.

  * If you connect a Hot Cable to another port (port not selected) this action overrides this field setting and activates the connected port. Connecting a Hot Cable to one of the serial ports only allows console redirection when a Hot Cable is actually connected to Serial 1 or 2. Use the modified serial cable described in Chapter 3, under Hot (Serial) Cable.

- Auto Poweron – [Disabled] or [**Enabled**]

  This field selects the power-on state of the ReadyBoard 800 when power is applied initially to the board, or after a power loss to the power supply, and determines when the ReadyBoard 800 powers up. If you change this BIOS setting, it takes one complete power on/ off cycle before it takes effect.

  * If this field is set to [Enabled], the ReadyBoard 800 goes immediately to a complete power on state, enabling the boot process, as soon as power is applied to the board or power supply. This occurs without the use of the external Power-On switch connected to the Utility connector (J12), if the external battery is connected. Normally, this would only happen during the initial power on process or during the ReadyBoard 800's recovery after a power loss to the power supply.

NOTE	If the external battery is disconnected at BT1, then setting this feature to [Enabled] will not function as specified. You must use the external Power-On switch connected to the Utility connector (J12) to completely power on the board, if the external battery is disconnected or inoperable.

  * If this field is set to [Disabled], the ReadyBoard 800 goes to standby in all situations until you enable it with the external Power-On switch connected to the Utility connector (J12).

- SMM Support – [Disabled] or [**Enabled**]

  This field was created to disable all SMI (System Management Interrupt) activity. This feature should only be used in special cases and then only when SMI activity would degrade Realtime response.

  * If this field is set to [Enabled], the default setting, SMI functions are enabled allowing the Watchdog Timer, ACPI functions and the USB boot features to operate normally.

  * If this field is set to [Disabled], the Watchdog Timer, ACPI functions, and USB boot features will not operate.

CAUTION	Do not Disable the SMM Support feature, unless you are thoroughly convinced you need it. This feature is only used for special cases when all SMI activity needs to be halted, which will disable many features of your system, including the Watchdog Timer, ACPI functions, and USB boot features.

- USB Boot Support – [**Disabled**] or [Enabled]

  This field allows you to select a USB device as a boot device. Refer also to Drive Assignment settings, Boot Order settings, and USB (device enable) under On-Board Controllers for the USB Drive settings and the number of USB ports enabled, respectively.

  * If this field is set to [Disabled], none of the USB devices connected to the ReadyBoard 800 can be used as a boot device.
  * If this field is set to [Enabled], any of the bootable USB devices connected to the ReadyBoard 800 can be used as a boot device.

NOTE	Ampro does not recommend connecting a USB boot device to the ReadyBoard 800 through an external hub. Instead, connect the USB boot device directly to the ReadyBoard 800.

- LAN Boot – [**Disabled**] or [LAN 1]

  This field allows you to boot the system over the Ethernet 1 connection (LAN 1, J16). Refer to LAN Boot in Appendix C, *LAN Boot Feature* for more information.

  * If this field is set to [LAN 1], the ReadyBoard 800 will boot from Ethernet 1 (J16). If you enable LAN Boot for [LAN 1], you will need to reboot the system and go to PXE agent BIOS settings. Refer to Appendix C, for more information.

- **On-Board Serial Ports**

NOTE	Serial Ports 1 and 2 can not share the same IRQs, and the IRQs used for Serial Ports 1 and 2 can not be used for Serial Ports 3 and 4 and vice versa.

- Serial 1 – [Disabled], [**3F8h**], [2F8h], [3E8h], [2E8h], [260h], [3E0h], [2E0h], [220h], [228h], [238h], or [338h]

  This field specifies the base address used for Serial Port 1.

  - IRQ – [none], [1], [3], [**4**], [5], [6], [7], [9], [10], [11], [12], [14], or [15]

    This field specifies the IRQ used for Serial Port 1. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

- Serial 2 – [Disabled], [3F8h], [**2F8h**], [3E8h], [2E8h], [260h], [3E0h], [2E0h], [220h], [228h], [238h], or [338h]

  This field specifies the base address used for Serial Port 2.

  - IRQ – [none], [1], [**3**], [4], [5], [6], [7], [9], [10], [11], [12], [14], or [15]

    This field specifies the IRQ used for Serial Port 2. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

- Serial 3 – [Disabled], [3F8h], [2F8h], [**3E8h**], [2E8h], [260h], [3E0h], [2E0h], [220h], [228h], [238h], or [338h]

  This field specifies the base address used for Serial Port 3. If this field is set to [Disabled], then the port is not used, then no IRQ is assigned, making it available for other devices.

  - IRQ – [3], [4], [5], [9], [10], or [**11**]

    This field specifies the IRQ used for Serial Port 3.

  - Mode – [**RS-232**] or [RS-485]

    This field specifies the signal mode, RS232, or RS485, used for Serial Port 3. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

- Serial 4 – [Disabled], [3F8h], [2F8h], [3E8h], [**2E8h**], [260h], [3E0h], [2E0h], [220h], [228h], [238h], or [338h]

  This field specifies the base address used for Serial Port 4. If this field is set to [Disabled], then the port is not used, then no IRQ is assigned, making it available for other devices.

  - IRQ – [3], [4], [5], [9], [**10**], or [11]

    This field specifies the IRQ used for Serial Port 4.

  - Mode – [**RS-232**] or [RS-485]

    This field specifies the signal mode, RS232, or RS485, used for Serial Port 4. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

- **On-Board LPT Port**

  - LPT 1 – [Disabled], [**378h**], [278h], or [3BCh],

    This field specifies the base address used for the Parallel Port (LPT 1).

    - IRQ – [none], [1], [3], [4], [5], [6], [**7**], [9], [10], [11], [12], [14], or [15]

      This field specifies the IRQ used for the Parallel Port (LPT 1). If this field is set to [none], then no IRQ is assigned, making it available for other devices.

    - DMA – [**3**], [2], [1], or [0]

      This field specifies the DMA channel used for the Parallel Port (LPT 1). If the LPT 1 field is set to [Disabled], then no DMA channel is assigned, making it available for other devices.

    - Mode – [**Standard**], [SPP (bi-dir)], [EPP 1.9 + SPP], [EPP 1.7 + ECP], [EPP 1.9 + ECP], or [ECP]

      This field specifies the Mode used for Parallel Port (LPT 1).

- **On-Board GPIO Port**

  These three fields allow you to enable/disable the GPIO port and set the input and output values of each of the eight GPIO pins or bits on J8 during operation and initialization.

  - GPIO Port 0x300 – [**Disabled**] or [Enabled]

    * If this field is set to [Enabled], then all of the eight pins are available for customer utilization.

    * If this field is set to [Disabled], then none of the eight pins are available for customer use.

  - Port Mask (In = 0/Out = 1) – [**11110000**] or [Select 11111111 to 00000000]

    Select input or output bit direction settings from [11111111] to [00000000], where [**11110000**] is the default setting for all eight bits/pins.

  - Port Initialize Value – [Select 11111111 to 00000000] or [**00000000**]

    Select port initialization values from [11111111] to [00000000], where [**00000000**] is the default setting for all eight bits/pins.

- **On-Board Controllers**

  - Floppy – [Disabled] or [**Enabled**]

    * If this field is set to [Enabled], then the on-board Floppy controller is used.

  - Primary IDE – [Disabled] or [**Enabled**]

    * If this field is set to [Enabled], then the on-board Primary IDE controller is used.

  - Secondary IDE – [Disabled] or [**Enabled**]

    * If this field is set to [Enabled], then the on-board Secondary IDE controller is used.

- PS/2 Mouse – [Disabled] or [**Enabled**]
  - * If this field is set to [Enabled], then the on-board PS/2 Mouse controller is used and assigned an IRQ by the BIOS, typically IRQ 12.
  - * If this field is set to [Disabled], then the on-board PS/2 Mouse controller is not used and IRQ 12 is available for other devices.
- USB – [Disabled], [2 Ports] or [**4 Ports**]
  - * If this field is set to [4 Ports], both on-board USB controllers are used, each one supporting two USB ports.
  - * If this field is set to [2 Ports], the first on-board USB controller is used, supporting two USB ports, and the second on-board USB controller is disabled.
- Audio – [Disabled] or [**Enabled**]
  - * If this field is set to [Enabled], the on-board Audio controller is used.

Video and Flat Panel Options

- **On-Board Video**
  - Framebuffer Size – [Disabled], [1MB], [4MB], [8MB], [**16MB**], or [32MB]

    This field specifies the amount of system memory used for the on-board Video Framebuffer. The amount of memory used for the Framebuffer of the on-board Video controller is subtracted from the available system memory.

NOTE	If the Framebuffer Size field is set to [Disabled], then no video will be displayed on screen.

  - AGP Aperture Size – [64MB], [**128MB**], or [256MB]

    This field specifies the size of memory used for the AGP Aperture. The AGP Aperture Size indicates the amount of system memory that can be used for the 3D engine. The system memory is still available for the system use, unless an application actually uses the AGP Aperture memory.
  - Off-Board Primary – [**Disabled**] or [Enabled]

    This field specifies which video controller is initialized as the primary video controller. This includes the on-board (ReadyBoard 800) video controller and/or a second video controller (video card through PCI-104 bus), initialized as the primary and secondary, or primary video controller only.
    - * If this field is set to the default setting, [Disabled], the on-board video controller will always be initialized by the BIOS as the primary video controller. If a second video controller is present, the OS can initialize this video controller as the secondary video controller, allowing you to use two separate video controllers and displays.
    - * If this field is set to, [Enabled], the on-board video controller will not be initialized by the BIOS, allowing the OS to initialize an off board video controller as the primary controller. The on-board (ReadyBoard 800) video controller will not be recognized by the OS, and therefore, will never be initialized as the secondary controller.
  - Display – [**CRT**], [LCD], or [CRT + LCD]

    This field specifies the display type used.
    - * If [LCD] or [CRT + LCD] is selected, the panel type selection indicates the configuration the LCD panel attached. See the next field and Table 4-3.
    - * If the [CRT+LCD] is selected, the same video information is shown on both displays simultaneously.

- Panel Type – [**None**]

  Refer to Table 4-3 for the list of supported resolutions and flat panel types. Some LCD panels may require video BIOS modifications. It you think this is the case, or would like help in setting up your LCD panel, contact Ampro for assistance with the LCD panel adaptation.

Table 4-3. LCD Panel Type List

#	LCD Resolution	LCD Type
	None	**NA**
1	640 x 480 x 18 (bit)	LVDS
2	800 x 600 x 18 (bit)	LVDS
3	1024 x 768 x 24 (bit)	LVDS
4	1280 x 1024 x 18 (bit)	LVDS
5	1400 x 1050 x 18 (bit)	LVDS
6	1024 x 768 x 18 (bit)	LVDS
7	1600 x 1200 x 18 (bit)	LVDS

#	LCD Resolution	LCD Type
8		
9		
10		
11		
12		
13		
14		
15		

PCI, Plug n' Play, and Interrupt/DMA Assignments

- **PCI**
  - INTA IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
  - INTB IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]
  - INTC IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
  - INTD IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]
  - INTE IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
  - INTF IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
  - INTH IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]
- **Plug and Play**
  - PnP BIOS – [Disabled] or [**Enabled**]
    - If this field is set to [Enabled], the BIOS uses Plug and Play adapter initialization and assigns the resources, such as I/O addresses, IRQs, and DMA channels to Plug and Play compatible devices. The resources assigned by the BIOS are based on the settings of the IRQ and DMA channel assignments listed in the following fields.
    - If this field is set to [Disabled], the IRQs and DMA channels listed below will not be assigned to Plug and Play devices by the BIOS.
  - PnP OS – [Disabled] or [**Enabled**]
    - If this field is set to [Enabled], the BIOS makes the Plug and Play API available for Plug and Play Operating Systems. This allows the Plug and Play OS to get the Plug and Play information by calling the Plug and Play API.
  - Assign IRQ 1 – [**Disabled**] or [Enabled]
    - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
    - If another device in the system is using this IRQ, then this field should be set to [Disabled].
  - Assign IRQ 3 – [Disabled] or [**Enabled**] (Typically COM2)
    - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
    - If another device in the system is using this IRQ, then this field should be set to [Disabled].

- Assign IRQ 4 – [Disabled] or [**Enabled**] (Typically COM1)
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 5 – [Disabled] or [**Enabled**]
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 6 – [**Disabled**] or [Enabled] (Typically Floppy Disk)
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 7 – [Disabled] or [**Enabled**] (Typically LPT1)
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 9 – [Disabled] or [**Enabled**] (Typically unused)
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 10 – [Disabled] or [**Enabled**] (Typically unused)
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 11 – [Disabled] or [**Enabled**] (Typically ISA Bridge/Native IDE)
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 12 – [**Disabled**] or [Enabled] (Typically PS/2 Mouse)
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 14 – [**Disabled**] or [Enabled] (Typically Hard Disk)
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 15 – [**Disabled**] or [Enabled] (Typically Hard Disk)
  - * If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - * If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign DMA 0 – [**Disabled**] or [Enabled]
  - * If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - * If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 1 – [**Disabled**] or [Enabled]
  - * If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - * If another device in the system is using this DMA channel, then this field should be set to [Disabled].

- Assign DMA 2 – [**Disabled**] or [Enabled]
  - * If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - * If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 3 – [Disabled] or [**Enabled**]
  - * If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - * If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 5 – [Disabled] or [**Enabled]**
  - * If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - * If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 6 – [Disabled] or [**Enabled**]
  - * If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - * If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 7 – [Disabled] or [**Enabled**]
  - * If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - * If another device in the system is using this DMA channel, then this field should be set to [Disabled].

Splash Screen Customization

The ReadyBoard 800 BIOS supports a graphical splash screen, which can be customized by the user and displayed on screen when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image displayed on screen during the boot process and remain there, depending on the options selected in BIOS Setup, while the OS boots.

Splash Screen Image Requirements

The user's image may be customized with any bitmap software editing tool, but must be converted into an acceptable format with the tools (files and utilities) provided by Ampro. If the custom image is not converted with the tools provided, then the image will not display properly when this field is selected in BIOS Setup.

NOTE	Do not use other splash screen conversion tools, including tools from other Ampro products, as these will render an image that is not compatible with the ReadyBoard 800 BIOS.

The splash screen image supported by the ReadyBoard 800 BIOS should be:

- Bitmap image
- Exactly 640x480 pixels
- Exactly 16 colors
- A converted file size of not greater than 5 kbytes compressed (See example splash.rle file)

Converting the Splash Screen File

The following files are provided by Ampro on the ReadyBoard 800 Doc & SW CD-ROM and are required for converting a custom splash screen file. Refer to the CD-ROM for the utilities and an example of how to load a custom image in the CD-ROM\Software\Misc\Splash directory.

- splash.bmp
- convert.exe
- convert.idf
- resplash.com
- rb800.bin

The process of converting and loading a custom image onto the ReadyBoard 800 involves the following sequence of events:

- Prepare directory for conversion (create directory and copy the files into it)
- Obtain the ReadyBoard 800 BIOS binary
- Prepare the custom image file
- Convert the image to an acceptable BIOS format
- Merge the image with BIOS binary to create new BIOS binary
- Load the new BIOS binary onto the ReadyBoard 800

NOTE	You can use any Windows PC to convert the custom image, but your PC must have an internet browser to access, view, and make selections in the main menu of the ReadyBoard 800 Doc & SW CD-ROM. For example: Microsoft Internet Explorer 4.x, or greater, Netscape Navigator version 4.x, or greater, or the equivalent.

Use the following steps to convert and load your custom image onto the ReadyBoard 800.

1. Copy the files from the *CD-ROM\Software\Misc\Splash* directory on the CD-ROM to a new directory (conversion directory) on your PC.

   This new conversion directory is where you intend to do the conversion and save the file.

2. Ensure you remove the read-only attributes from all the files as part of the file copying process.

3. Copy the ReadyBoard 800 BIOS binary file (rb800.bin) to the new conversion directory on your PC where the other files and utilities are located.

   If this file is not on the ReadyBoard 800 Doc & SW CD-ROM, you will have to obtain it from Ampro.

NOTE	Ampro recommends keeping a copy of this original rb800.bin file, just in case you encounter problems with your new file or have difficulty updating the BIOS with the new image.

4. Prepare your custom image file with any Windows bitmap software editing tool.

   - For example, Corel Photo-Paint, Adobe Photoshop, or the Windows Paint program provided with Windows. You can insert a desired graphic image, logo, text, etc. into the file.
   - The custom image must be a bitmap image in .bmp format at 640x480 pixels and it must be 16 colors. The file should be about 150 bytes uncompressed. Refer to the example file splash.bmp.

5. Save your custom image file as splash.bmp at 640x480 pixels by 16 colors.

   - If your custom image file is not approximately 150 kbytes uncompressed in size it is probably not in the right format or is too complex to be used in the BIOS. You will have to edit it down in size until you have reached an acceptable file size. Refer to the example splash.bmp.
   - If you are doubtful about the conversion process, due to the file size, Ampro recommends making a copy of your new splash.bmp, so that you can edit it later if the conversion does not yield a small enough file. Otherwise, you may have to re-create your custom image before you can edit it down to an acceptable file size.

6. If your custom image file is not on the conversion PC, copy the new splash.bmp file to the conversion directory.

7. Run the following command from DOS, or a Windows DOS pop-up screen to convert your new splash.bmp file.

   ```
   C:\splash>convert convert.idf
   ```

   This conversion should yield a splash.rle file of approximately 5 kbytes in size or less, depending on the complexity of your image.

8. If the splash.rle file size is greater than 5 kbytes, go back to the unconverted image file and edit the file.

   You may reduce the file size of the converted image (splash.rle) by reducing the image's complexity.

9. Run the following command to merge the converted image with the BIOS binary file.

   ```
   C:\splash>resplash rb800.bin splash.rle rb800n.bin
   ```

   This creates a new BIOS named rb800n.bin, which has the new splash image. Rename the new BIOS file rb800n.bin to rb800.bin before using it to update the ReadyBoard 800.

10. Copy the files update.bat, aflash.exe, and the renamed rb800.bin to a DOS boot floppy.

11. Boot the ReadyBoard 800 from the floppy and run update.bat.

12. Cycle the power to the ReadyBoard 800 and enter BIOS Setup to enable the splash screen.

Appendix A Technical Support

Ampro Computers, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Requests for support through the Virtual Technician are given the highest priority, and usually will be addressed within one working day.

- Ampro Virtual Technician – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro web site at http://ampro.custhelp.com. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online before you can login to access this service.
- Personal Assistance – You may also request personal assistance by going to the "Ask a Question" area in the Virtual Technician. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request you can go to the "My Stuff" area and log in to check status, update your request, and access other features.
- Embedded Design Resource Center – This service is also free and available 24 hours a day at the Ampro web site at http://www.ampro.com. However, you must be registered online before you can login to access this service.

  The Embedded Design Resource Center was created as a resource for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience. This page contains links to White Papers, Specifications, and additional technical information.

Table A-1. Technical Support Contact Information

Method	Contact Information
Virtual Technician	http://ampro.custhelp.com
Web Site	http://www.ampro.com
Standard Mail	Ampro Computers, Incorporated 5215 Hellyer Avenue San Jose, CA 95138-1007, USA

Appendix B MiniModule ISA Board

Introduction

This Appendix describes the MiniModule ISA expansion board and how it is used with the ReadyBoard 800 to provide ISA bus signals to any PC/104 compatible expansion boards stacked onto the ReadyBoard 800. The MiniModule ISA expansion board mates to the ReadyBoard 800's PCI-104 connector (32-bit PCI bus) where it provides the necessary signals through a PCI-to-ISA bridge conversion for the PC/104 compatible expansion boards. The necessary Serial IRQs signals are provided through the PCI-104 connector at pin-31 (B-1).

What is PCI-104?

PCI-104 is the terminology used for the PCI-only (32-bit PCI bus) specification within the PC/104 product family. PCI-104 eliminates the need for the ISA bus (PC/104 and its 104-pin connector), retaining only the 120-pin connector for PCI and PC/104-Plus. The MiniModule ISA expansion board provides the ISA support through the PCI-104 connector and the PCI-to-ISA bridge located on the board.

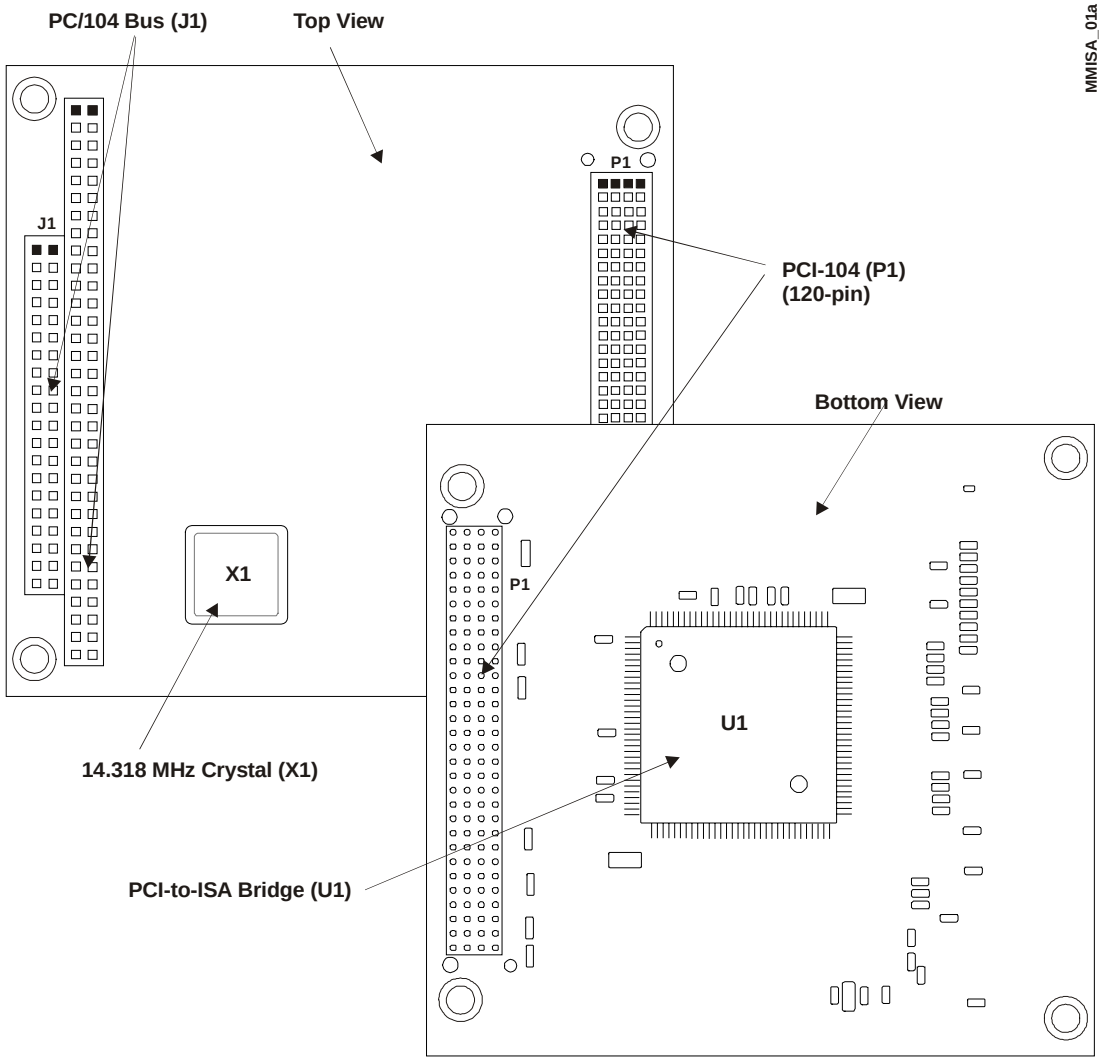


Figure B-1. MiniModule ISA Expansion Board (Top/Bottom view)

MiniModule ISA Expansion Board Features

- Supports PC/104 Bus and PC/104-Plus Bus expansion interfaces
- Supports ISA bus signals through PCI-104 connector
- Transparent to the Operating System
- Supports PC/104-Plus form factor 90 mm x 96 mm (3.6" x 3.8")

PCI-to-ISA Bridge Controller:

- PCI 2.3 compliant
- Transparent mode
- Full 24-bit ISA addressing
- 16-bit and 8-bit I/O and memory cycles
- Software transparent DMA
- ISA bus master supports (4) PC/104 cards
- Encodes all ISA IRQs

Specifications

Physical Specifications

Table B-1 lists the physical dimensions of the board. Figures B-2 and B-3 give the typical mounting order in side views.

Table B-1. MiniModule ISA Weight and Footprint Dimensions

Item	Dimension
Weight	0.027 kg. (0.06 lb.)
Height (overall)	11.07 mm (0.436")
Width	90 mm (3.6")
Length	96 mm (3.8")
Thickness	1.574 mm (0.062")

NOTE Overall height is measured from the upper board surface to the highest permanent component (PC/104 bus connector) on the upper board surface.

Power Requirements

The MiniModule ISA expansion board draws its power from the ReadyBoard 800 through the PCI-104 bus connector.

Environmental Specifications

Table B-2 provides the operating and storage condition ranges required for this expansion board.

Table B-2. MiniModule ISA Environmental Requirements

	Parameters	Conditions
Temperature	Operating	+0° to +60° C (32° to +140° F)
	Storage	–20° to +75° C (–4° to +167° F)
Humidity	Operating	5% to 95% relative humidity, non-condensing
	Non-operating	5% to 95% relative humidity, non-condensing

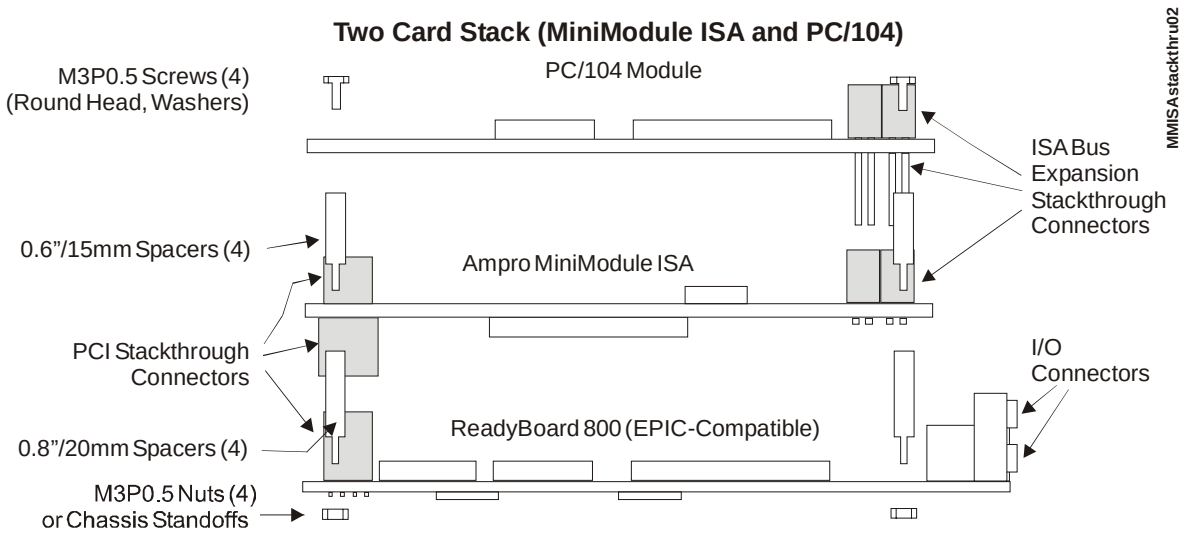


Figure B-2. MiniModule ISA Two Card Stack Order

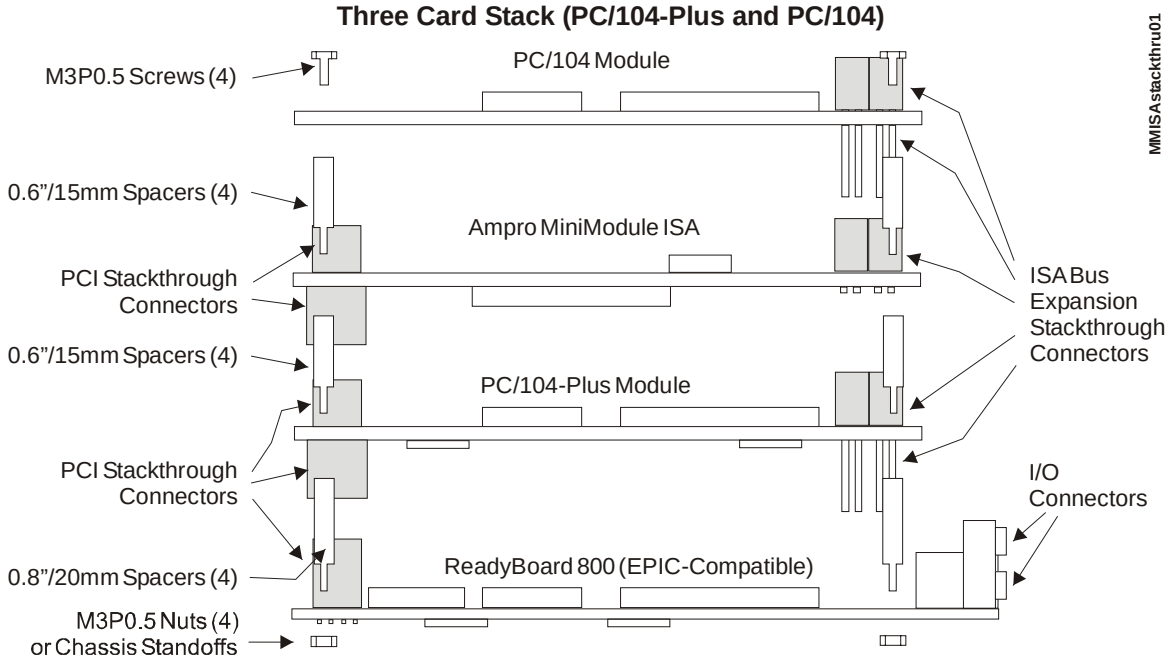


Figure B-3. MiniModule ISA Three Card Stack Order

PCI-104 Interface (P1)

The PCI-104 uses a 120-pin (30x4) 2 mm connector. This connector carries all of the appropriate PCI and ISA bus signals operating at clock speeds up to 33 MHz. This interface header accepts stackable modules and is located on both the top and bottom of the MiniModule ISA expansion board.

Table B-3 provides the signals and descriptions for the three dedicated signal lines reserved for the MiniModule ISA expansion board on the PCI-104 connector. For the complete PCI-104 pin-outs, refer to Table 3-4 earlier in the manual.

Table B-3. MiniModule ISA Dedicated PCI-104 Signal Lines (P1)

Pin #	Signal	Input/ Output	Description
31 (B1)	SERIRQ		Serial IRQ – This signal line provides the ISA IRQs to the PC/104 Bus if the MiniModule ISA expansion board is used.
54 (B24)	REQ2*	T/S	Bus Request 2 – This signal indicates this device desires use of the bus to the arbitrator. This request line is not available when the MiniModule ISA board is used. See Notes.
85 (C25)	GNT2*	T/S	Grant 2 – This signal line indicates access has been granted to the requesting device (PCI Masters). This signal line is reserved for the MiniModule ISA expansion board. See all Notes below.

Notes: The signals marked with * = Negative true logic.

The Input/Output column in this table refers to the input/output signals listed in the PCI Local Bus Manual, Revision 2.3, Chapter 2, paragraph 2.1, signal definitions. The following terms or acronyms are used in this table:

- T/S – Tri-State is a bi-directional input output pin

NOTE	One request signal (pin 54 or B24, REQ2) and one grant line (pin 85 or C25, GNT2) are not available to other cards/devices when the MiniModule ISA expansion board is used. These signal lines are reserved for the MiniModule ISA board, if jumper JP1 is Enabled.

PC/104 Interface (J1A, B, J1C, D)

The PC/104 Bus uses a 104-pin 0.10" header interface. This interface header will carry all of the appropriate PC/104 signals operating at clock speeds up to 8 MHz. This interface header accepts stackable modules and is located on the top of the MiniModule ISA expansion board.

Tables B-4 to B-7 describe the PC/104 pins/signals with 104-pins, 4 rows, consecutive numbering, (B1, A1, C0, D0), and 0.100" pin spacing.

Table B-4. PC/104 Interface Pin/Signal Descriptions (J1A)

Pin #	Signal	Description (J1 Row A)
1 (A1)	IOCHCHK*	I/O Channel Check – This is activated by ISA boards when requesting a non maskable interrupt (NMI) be sent to the system processor. It is driven active to indicate an uncorrectable error has been detected
2 (A2)	SD7	System Data 7 – This signal (0 to 19) provides a system data bit.
3 (A3)	SD6	System Data 6 – Refer to SD7, pin A2, for more information.
4 (A4)	SD5	System Data 5 – Refer to SD7, pin A2, for more information.
5 (A5)	SD4	System Data 4 – Refer to SD7, pin A2, for more information.
6 (A6)	SD3	System Data 3 – Refer to SD7, pin A2, for more information.
7 (A7)	SD2	System Data 2 – Refer to SD7, pin A2, for more information.
8 (A8)	SD1	System Data 1 – Refer to SD7, pin A2, for more information.
9 (A9)	SD0	System Data 0 – Refer to SD7, pin A2, for more information.
10 (A10)	IOCHRDY	I/O Channel Ready – This signal allows slower ISA boards to lengthen I/O or memory cycles by inserting wait states. This signal's normal state is active high (ready). ISA boards drive the signal inactive low (not ready) to insert wait states. Devices using this signal to insert wait states should drive it low immediately after detecting a valid address decode and an active read, or write command. The signal is released high when the device is ready to complete the cycle.
11 (A11)	AEN	Address Enable – This signal is used to degate the system processor and other devices from the bus during DMA transfers. When this signal is active, the system DMA controller has control of the address, data, and read/write signals. This signal should be included as part of ISA board select decodes to prevent incorrect board selects during DMA cycles.
12 (A12)	SA19	System Address 19 – This signal (0 to 19) provides a system address bit.
13 (A13)	SA18	System Address 18 – Refer to SA19, pin A12, for more information.
14 (A14)	SA17	System Address 17 – Refer to SA19, pin A12, for more information.
15 (A15)	SA16	System Address 16 – Refer to SA19, pin A12, for more information.
16 (A16)	SA15	System Address 15 – Refer to SA19, pin A12, for more information.
17 (A17)	SA14	System Address 14 – Refer to SA19, pin A12, for more information.
18 (A18)	SA13	System Address 13 – Refer to SA19, pin A12, for more information.
19 (A19)	SA12	System Address 12– Refer to SA19, pin A12, for more information.
20 (A20)	SA11	System Address 11 – Refer to SA19, pin A12, for more information.
21 (A21)	SA10	System Address 10 – Refer to SA19, pin A12, for more information.
22 (A22)	SA9	System Address 9 – Refer to SA19, pin A12, for more information.
23 (A23)	SA8	System Address 8 – Refer to SA19, pin A12, for more information.

Pin #	Signal	Description (J1 Row A)
24 (A24)	SA7	System Address 7 – Refer to SA19, pin A12, for more information.
25 (A25)	SA6	System Address 6 – Refer to SA19, pin A12, for more information.
26 (A26)	SA5	System Address 5 – Refer to SA19, pin A12, for more information.
27 (A27)	SA4	System Address 4 – Refer to SA19, pin A12, for more information.
28 (A28)	SA3	System Address 3 – Refer to SA19, pin A12, for more information.
29 (A29)	SA2	System Address 2 – Refer to SA19, pin A12, for more information.
30 (A30)	SA1	System Address 1 – Refer to SA19, pin A12, for more information.
31 (A31)	SA0	System Address 0 – Refer to SA19, pin A12, for more information.
32 (A32)	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table B-5. PC/104 Interface Pin/Signal Descriptions (J1B)

Pin #	Signal	Descriptions (J1 Row B)
33 (B1)	GND	Ground
34 (B2)	RESETDRV	Reset Drive – This signal is used to reset or initialize system logic on power up or subsequent system reset.
35 (B3)	+5V	+5V power +/- 10%
36 (B4)	IRQ9	Interrupt request 9 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
37 (B5)	-5V	Not connected (-5 volts)
38 (B6)	DRQ2	DMA Request 2 – Used by I/O resources to request DMA service, or to request ownership of the bus as a bus master device. Must be held high until associated DACK2 line is active.
39 (B7)	-12V	Not connected (-12 volts)
40 (B8)	ENDXFR*	Zero Wait State – This signal is driven low by a bus slave device to indicate it is capable of performing a bus cycle without inserting any additional wait states. To perform a 16-bit memory cycle without wait states, this signal is derived from an address decode.
41 (B9)	+12V	+12 Volts
42 (B10)	GND	Not connected (Key Pin)
43 (B11)	SMEMW*	System Memory Write – This signal is used by bus owner to request a memory device to store data currently on the data bus and only active for the lower 1 MB. Used for legacy compatibility with 8-bit cards.
44 (B12)	SMEMR*	System Memory Read – This signal is used by bus owner to request a memory device to drive data onto the data bus and only active for lower 1 MB. Used for legacy compatibility with 8-bit cards.
45 (B13)	IOW*	I/O Write – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to capture the write data on the data bus.
46 (B14)	IOR*	I/O Read – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to drive read data onto the data bus.
47 (B15)	DACK3*	DMA Acknowledge 3 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
48 (B16)	DRQ3	DMA Request 3 – Used by I/O resources to request DMA service. Must be held high until associated DACK3 line is active.

Pin #	Signal	Descriptions (J1 Row B)
49 (B17)	DACK1*	DMA Acknowledge 1 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
50 (B18)	DRQ1	DMA Request 1 – Used by I/O resources to request DMA service. Must be held high until associated DACK1 line is active.
51 (B19)	REFRESH*	Memory Refresh – This signal is driven low to indicate a memory refresh cycle is in progress. Memory is refreshed every 15.6 usec.
52 (B20)	SYSCLK	System Clock – This is a free running clock typically in the 8 MHz to 10 MHz range, although its exact frequency is not guaranteed.
53 (B21)	IRQ7	Interrupt Request 7 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
54 (B22)	IRQ6	Interrupt Request 6 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
55 (B23)	IRQ5	Interrupt Request 5 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
56 (B24)	IRQ4	Interrupt Request 4 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
57 (B25)	IRQ3	Interrupt Request 3 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
58 (B26)	DACK2*	DMA Acknowledge 2 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
59 (B27)	TC	Terminal Count – This signal is a pulse to indicate a terminal count has been reached on a DMA channel operation.
60 (B28)	BALE	Buffered Address Latch Enable – This signal is used to latch the LA23 to LA17 signals or decodes of these signals. Addresses are latched on the falling edge of BALE. It is forced high during DMA cycles. When used with AENx, it indicates a valid processor or DMA address.
61 (B29)	+5V	+5V power +/- 10%
62 (B30)	OSC	Oscillator – This clock signal operates at 14.3 MHz. This signal is not synchronous with the system clock (SYSCLK).
63 (B31)	GND	Ground
64 (B32)	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table B-6. PC/104 Interface Pin/Signal Descriptions (J1C)

Pin #	Signal	Descriptions (J1 Row C)
1 (C0)	GND	Ground
2 (C1)	SBHE*	System Byte High Enable – This signal is driven low to indicate a transfer of data on the high half of the data bus (D15 to D8).
3 (C2)	LA23	Lactchable Address 23 – This signal must be latched by the resource if the line is required for the entire data cycle.
4 (C3)	LA22	Lactchable Address 22 – Refer to LA23, pin C2, for more information.
5 (C4)	LA21	Lactchable Address 21 – Refer to LA23, pin C2, for more information.

Pin #	Signal	Descriptions (J1 Row C)
6 (C5)	LA20	Lactchable Address 20 – Refer to LA23, pin C2, for more information.
7 (C6)	LA19	Lactchable Address 19 – Refer to LA23, pin C2, for more information.
8 (C7)	LA18	Lactchable Address 18 – Refer to LA23, pin C2, for more information.
9 (C8)	LA17	Lactchable Address 17 – Refer to LA23, pin C2, for more information.
10 (C9)	MEMR*	Memory Read – This signal instructs a selected memory device to drive data onto the data bus. It is active on all memory read cycles.
11 (C10)	MEMW*	Memory Write – This signal instructs a selected memory device to store data currently on the data bus. It is active on all memory write cycles.
12 (C11)	SD8	System Data 8 – Refer to SD7, pin A2, for more information.
13 (C12)	SD9	System Data 9 – Refer to SD7, pin A2, for more information.
14 (C13)	SD10	System Data 10 – Refer to SD7, pin A2, for more information.
15 (C14)	SD11	System Data 11 – Refer to SD7, pin A2, for more information.
16 (C15)	SD12	System Data 12 – Refer to SD7, pin A2, for more information.
17 (C16)	SD13	System Data 13 – Refer to SD7, pin A2, for more information.
18 (C17)	SD14	System Data 14 – Refer to SD7, pin A2, for more information.
19 (C18)	SD15	System Data 15 – Refer to SD7, pin A2, for more information.
20 (C19)	GND	Key Pin

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table B-7. PC/104 Interface Pin/Signal Descriptions (J1D)

Pin #	Signal	Descriptions (J1 Row D)
21 (D0)	GND	Ground
22 (D1)	MEMCS16*	Memory Chip Select 16 – This is signal is driven low by a memory slave device to indicates it is cable of performing a 16-bit memory data transfer. This signal is driven from a decode of the LA23 to LA17 address lines.
23 (D2)	IOCS16*	I/O Chip Select 16 – This signal is driven low by an I/O slave device to indicate it is capable of performing a 16-bit I/O data transfer. This signal is driven from a decode of the SA15 to SA0 address lines.
24 (D3)	IRQ10	Interrupt Request 10 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
25 (D4)	IRQ11	Interrupt Request 11 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
26 (D5)	IRQ12	Interrupt Request 12 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
27 (D6)	IRQ15	Interrupt Request 15 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
28 (D7)	IRQ14	Interrupt Request 14 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
29 (D8)	DACK0*	DMA Acknowledge 0 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
30 (D9)	DRQ0	DMA Request 0 – Used by I/O resources to request DMA service. Must be held high until associated DACK0 line is active.

Pin #	Signal	Descriptions (J1 Row D)
31 (D10)	DACK5*	DMA Acknowledge 5 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
32 (D11)	DRQ5	DMA Request 5 – Used by I/O resources to request DMA service. Must be held high until associated DACK5 line is active.
33 (D12)	DACK6*	DMA Acknowledge 6 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
34 (D13)	DRQ6	DMA Request 6 – Used by I/O resources to request DMA service. Must be held high until associated DACK6 line is active.
35 (D14)	DACK7*	DMA Acknowledge 7 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
36 (D15)	DRQ7	DMA Request 7 – Used by I/O resources to request DMA service. Must be held high until associated DACK7 line is active.
37 (D16)	+5V	+5V Power +/- 10%
38 (D17)	MASTER*	Bus Master Assert – This signal is used by an ISA board along with a DRQ line to gain ownership of the ISA bus. Upon receiving a -DACK a device can pull -MASTER low which will allow it to control the system address, data, and control lines. After -MASTER is low, the device should wait one CLK period before driving the address and data lines, and two clock periods before issuing a read or write command.
39 (D18)	GND	Ground
40 (D19)	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Appendix C LAN Boot Feature

This Appendix describes the LAN Boot feature provided by the ReadyBoard 800, which can be enabled or disabled in the ReadyBoard 800 BIOS Setup Utility. The balance of this appendix briefly describes how to set up LAN Boot using the PXE boot agent BIOS settings.

Introduction

LAN Boot is supported by a single Ethernet port on the ReadyBoard 800, and is based on the Preboot Execution Environment (PXE), an open industry standard. PXE (pronounced *pixie*) was designed by Intel, along with other hardware and software vendors, as part of the Wired for Management (WfM) specification to improve management of desktop systems. This technology can also be applied to the embedded system market place. PXE turns the ReadyBoard 800 Ethernet port into boot device when connected over a network (LAN).

PXE boots the ReadyBoard 800 from the network (LAN) by transferring a *boot image file* from a server. This image file is typically the operating system for the ReadyBoard 800, or a pre-OS agent that can perform management tasks prior to loading the image file (OS). A management task could include scanning the hard drive for viruses before loading the image file.

PXE is not operating system-specific, so the image file can load any OS. The most common application of PXE (LAN Boot) is installing an OS on a brand new device (hard disk drive) that has no operating system, (or reinstalling it when the operating system has failed or critical files have been corrupted).

Using PXE prevents the user from having to manually install all of the required software on the storage media device, (typically a hard disk drive) including the OS, which might include a stack of installation CD-ROMs. Installing from the network is as simple as connecting the ReadyBoard 800 to the network and powering it on. The server can be set up to detect new devices and install software automatically, thereby greatly simplifying the management of small to large numbers of systems attached to a network.

If the hard disk drive should crash, the network can be set up to do a hardware diagnostic check, and once a software-related problem is detected, the server can re-install the defective software, or all the ReadyBoard 800 software from the server. Booting from the network also guarantees a *clean* boot, with no boot-time viruses or user-modified files. The boot files are stored on the PXE server, protected from infection and user-modification.

To effectively make use of the LAN Boot feature, you need a PXE boot agent for configuration and set up, as well as, a PXE server with PXE server components installed. Ampro has provided a third party PXE boot agent integrated into the ReadyBoard 800 BIOS, which allows you to select the LAN Boot feature. Once you change the BIOS settings to enable LAN Boot, you will need to exit BIOS Setup, saving your changes, and reboot the system to enter and set the PXE Boot Agent BIOS settings. Refer to *PXE Boot Agent BIOS Setup* on the next page for more setup and configuration information.

The PXE server includes specific PXE components, but Ampro does not provide the PXE server components or the PXE server. You will need to provide your own compatible PXE server and its related PXE components. The PXE server components include tools and utilities for such things as setting up the network-booting environment, setting up a pre-OS environment, booting remotely, managing the PXE client/server relationship, maintaining security, and utilities for building a boot image to be transferred over the network. The network must have a PXE server and TFTP (Trivial File Transfer Protocol) server. The PXE server is designed to work in conjunction with a Dynamic Host Configuration Protocol (DHCP) server. The PXE server can be shared with the DHCP server or installed on a different server. This makes it possible to add PXE to an existing network without affecting the existing DHCP server or configuration. The boot image file is transferred to the client using TFTP, and this file is then used to boot the client. Refer to these web sites for a more detailed technical description of how PXE works, go to, http://www.pxe.ca, or for more detailed information concerning PXE server tools, such as pre-OS agents, go to: http://www.pre-OS.com.

PXE Boot Agent BIOS Setup

This section describes the BIOS settings of the third party PXE Boot agent provided by Ampro and integrated into the ReadyBoard 800 firmware. The PXE Boot Agent's BIOS setup menu and screens are used when configuring the LAN boot feature in the ReadyBoard 800 BIOS.

The third party PXE Boot agent provided by Ampro supports multiple boot protocols and network environments such as traditional TCP/IP, NetWare, and RPL. It also includes support for all of the most used protocols including DHCP, BOOTP, RPL, NCP/IPX (802.2, 802.3, Ethernet II), and the Wired for Management (WfM) 2.0 specification for Preboot Execution Environment (PXE).

Accessing PXE Boot Agent BIOS Setup

To access PXE Boot Agent BIOS Setup when LAN Boot has been selected in the ReadyBoard 800 BIOS Setup screen, refer to this procedure:

1. Reboot the ReadyBoard 800 after selecting LAN 1 in BIOS Setup.

   The default setting for LAN boot is [Disabled].

2. Access the LAN Boot Setup by pressing the Ctrl +Alt + B keys, when the following message appears on the boot screen.

   ```
   Initializing MBA.  Press Ctrl + Alt + B to configure ..
   ```

3. Select from the menu options when the default screen appears as shown in Figure C-1.
4. Follow the instructions at the bottom of the screen to navigate through the selections and modify any settings.

NOTE	The default values are shown highlighted (**bold text**) in the list of options on the following pages. Refer to the bottom of the Setup screen for navigation instructions and when making selections.

PXE Boot Agent Setup Screen

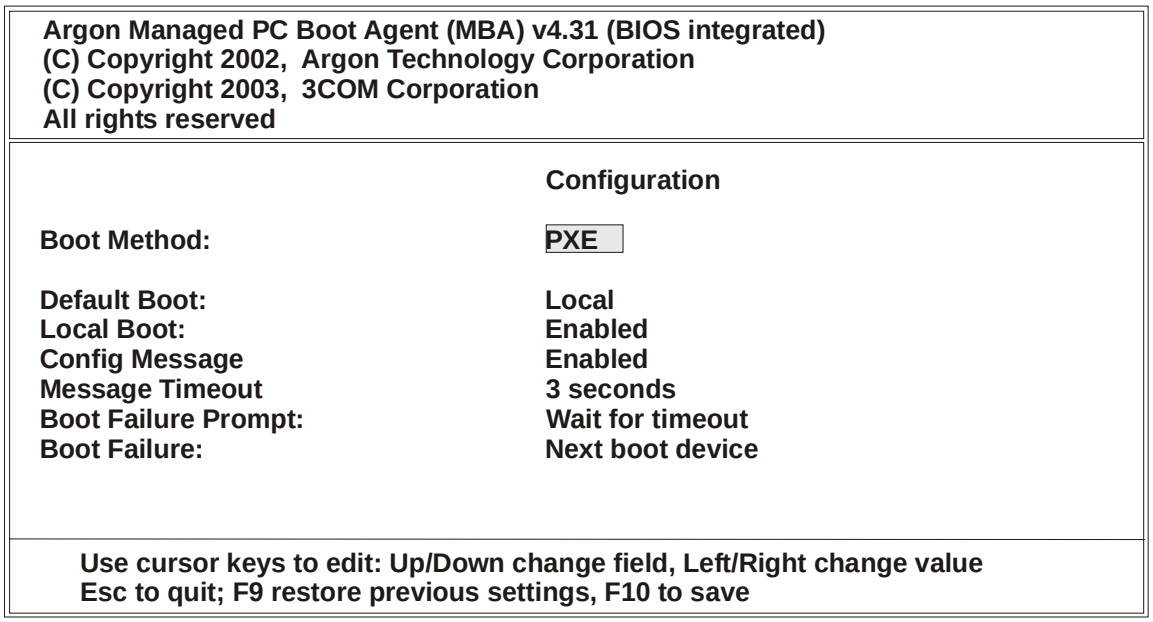


Figure C-1. PXE Agent Boot Setup Screen

- **PXE Configuration**
  - Boot Method: – [**PXE**], [TCP/IP], [NetWare], or [RPL]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

- **TCP/IP Configuration**
  - Boot Method: – [PXE], [**TCP/IP**], [NetWare], or [RPL]
  - Protocol: – [**DHCP**] or [BOOTP]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

- **NetWare Configuration**
  - Boot Method: – [PXE], [TCP/IP], [**NetWare**], or [RPL]
  - Protocol: – [802.2], [**802.3**], or [EthII]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

- **RPL Configuration**
  - Boot Method: – [PXE], [TCP/IP], [NetWare], or [**RPL**]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

Index