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S7-300 Automation System CPU Specifications: CPU 31xC and CPU 31x

Reference Manual

This manual is part of the documentation
package with the order number:
6ES7398-8FA10-8BA0

Edition 06/2003
A5E00105475-03

Safety Guidelines

This manual contains notices intended to ensure personal safety, as well as to protect the products and connected equipment against damage. These notices are highlighted by the symbols shown below and graded according to severity by the following texts:

Danger
indicates that death, severe personal injury or substantial property damage will result if proper precautions are not taken.

Warning
indicates that death, severe personal injury or substantial property damage can result if proper precautions are not taken.

Caution
indicates that minor personal injury can result if proper precautions are not taken.

Caution
indicates that property damage can result if proper precautions are not taken.

Notice
draws your attention to particularly important information on the product, handling the product, or to a particular part of the documentation.

Qualified Personnel

Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:

Warning
This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

This product can only function correctly and safely if it is transported, stored, set up, and installed correctly, and operated and maintained as recommended.

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A5E00105475-03

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Preface

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Purpose of this manual

This manual contains all the information you will need concerning the structure, communication functions, memory concept, cycle, response times and the specifications for the CPUs. You will then learn the points to consider when upgrading to one of the CPUs discussed in this manual.

Basic knowledge required

To understand this manual you need general knowledge of automation control engineering. You also require knowledge of the STEP 7 basic software. You may find it useful to read the *Programming with STEP 7 V5.1* manual first.

Scope of the Manual

This manual applies to the following CPUs with the following hardware and software versions:

CPU	Convention: In this manual, the CPUs are designated as follows:	Order No.	As of version	
			Firmware	Hardware
CPU 312C	CPU 31xC	6ES7312-5BD01-0AB0	V2.0.0	01
CPU 313C		6ES7313-5BE01-0AB0	V2.0.0	01
CPU 313C-2 PtP		6ES7313-6BE01-0AB0	V2.0.0	01
CPU 313C-2 DP		6ES7313-6CE01-0AB0	V2.0.0	01
CPU 314C-2 PtP		6ES7314-6BF01-0AB0	V2.0.0	01
CPU 314C-2 DP		6ES7314-6CF01-0AB0	V2.0.0	01
CPU 312	CPU 31x	6ES7312-1AD10-0AB0	V2.0.0	01
CPU 314		6ES7314-1AF10-0AB0	V2.0.0	01
CPU 315-2 DP		6ES7315-2AG10-0AB0	V2.0.0	01
CPU 317-2 DP		6ES7317-2AJ10-0AB0	V2.1.0	01

Note

This manual describes all modules available at the time of publication.

We reserve the right to enclose Product Information for new modules or new versions of modules containing up-to-date information.

Approvals

The SIMATIC S7-300 product series has the following approvals:

- Underwriters Laboratories, Inc.: UL 508 (Industrial Control Equipment)
- Canadian Standards Association: CSA C22.2 No. 142, (Process Control Equipment)
- Factory Mutual Research: Approval Standard Class Number 3611

CE mark

The SIMATIC S7-300 product series conforms to the requirements and safety specifications of following EU directives:

- EU directive 73/23/EWE "Low-voltage directive"
- EU directive 89/336/EEC "EMC directive“

C tick mark

The SIMATIC S7-300 product series is compliant with AS/NZS 2064 (Australia and New Zealand).

Standards

The SIMATIC S7-300 product series is compliant with the requirements and criteria for IEC 61131-2.

Its place in the world of documentation

This manual is part of the documentation package for the S7-300.

Reference Manual CPU Specifications: CPU 312 IFM to 318-2 DP You are reading this manual → CPU Specifications: CPU 31xC and CPU 31x	Description of the functions, structure and technical data of a CPU
Manual CPU 31xC: Technological Functions Examples	Description of the individual technological functions: - Positioning - Count - Point-to-point connection - Control The CD contains examples on the technological functions.
Installation Manual S7-300 Automation Sytems, Hardware and Installation: CPU 312 IFM - 318-2 DP S7-300 Automation Systems, Hardware and Installation: CPU 31xC und CPU 31x	Description of the configuration, installation, wiring and commissioning of a S7-300
Reference Manual S7-300 Programmable Controller Module Specifications	Function descriptions and technical data of signal modules, power supply modules and interface modules.
Instruction Lists CPU 312 IFM to 318-2 DP CPU 31xC, CPU 31x IM 151-7 CPU, BM 147-1 CPU, BM 147-2 CPU	List of stored instructions of the CPUs and their execution times. List of executable blocks (OBs/SFCs/SFBs) and their execution times.
Getting Started Getting Starteds take you through each commissioning step to a functioning application by using a concrete example. The following Getting Starteds are available to you:	- CPU 31x: Commissioning - CPU 31xC: Commissioning - CPU 314C: Positioning with Analog Output - CPU 314C: Positioning with Digital Output - CPU 31xC: Counting - CPU 31xC: Point-to-Point Connection - CPU 31xC: Controlling

Figure 1-1 Information environment of the S7-300

You will also require the following manual, in addition to this documentation package:

Reference Manual System Software for S7-300/400 System and Standard Functions Reference Manual part of the STEP 7 documentation package	Description of the SFCs, SFBs and OBS. You can also find the description in the STEP 7 Online Help.

Additional Figure 1-2 documentation

Recycling and Disposal

The ET200eco is recycleable due to its non-toxic materials. Please contact a company certified in the disposal of electronic scrap for environmentally safe recycling and disposal of your old device.

Further Support

If you have any technical questions, please get in touch with your Siemens representative or agent responsible.

http://www.siemens.com/automation/partner

Training Centers

Siemens offers a number of training courses to familiarize you with the SIMATIC S7 automation system. Please contact your regional training center or our central training center in D 90327 Nuremberg, Germany for details:

Telephone:	+49 (911) 895-3200.
Internet:	http://www.sitrain.com

SIMATIC Technical Support

In addition to your local dealer, you can also contact one of the three Support Centers:

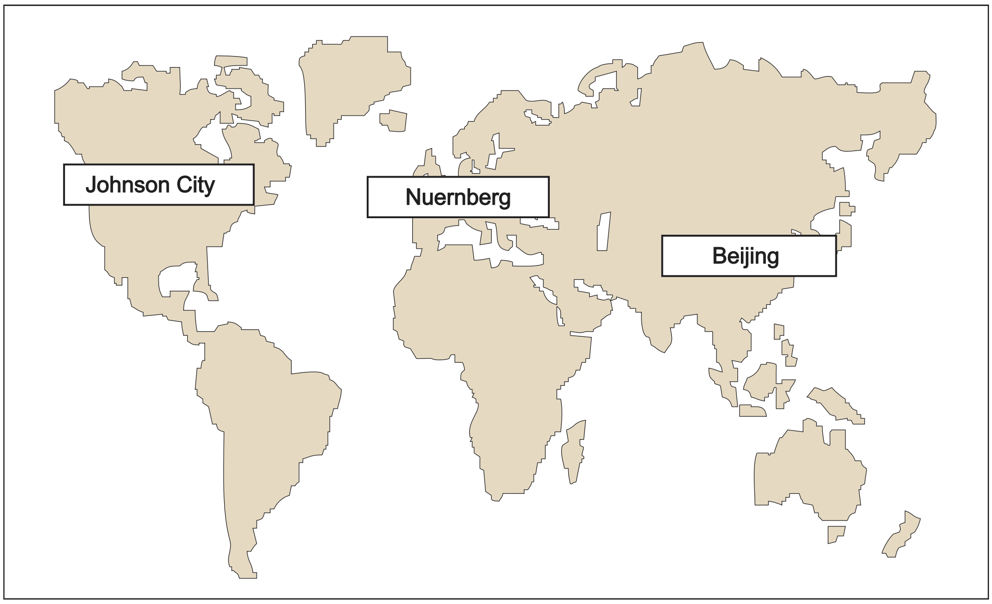

Figure 1-3 SIMATIC Technical Support

Worldwide (Nuremberg) **Technical Support** Local time: 0:00 to 24:00 / 365 days a year Phone: +49 (0) 180 5050 222 Fax: +49 (0) 180 5050 223 E-mail: adsupport@siemens.com GMT: +1:00		
Europe / Africa (Nuremberg) **Authorization** Local time: Mo.-Fr. 8:00 to 17:00 Phone: 49 (0) 180 5050-222 Fax: +49 (0) 180 5050-223 E-mail: adsupport@siemens.com GMT: +1:00	**America** (Johnson City) **Technical Support and Authorization** Local time: Mo.-Fr. 8:00 to 17:00 Phone: +1 (0) 770 740 3505 Fax: +1 (0) 770 740 3699 E-mail: isd-callcenter@sea.siemens.com GMT: –5:00	**Asia / Australia** (Beijing) **Technical Support and Authorization** Local time: Mo.-Fr. 8:00 to 17:00 Phone: +65 (0) 740-7000 Fax: +65 (0) 740-7001 E-mail: simatic.hotline@sea.siemens.com.sg GMT: +8:00
Technical Support and Authorization personnel generally speak both German and English.		

Service & Support on the Internet

In addition to our documentation, we offer our Know-how online on the internet at:

http://www.siemens.com/automation/service&support

where you will find the following:

- The newsletter, which constantly provides you with up-to-date information on your products.
- The right documents via our Search function in Service & Support.
- A forum, where users and experts from all over the world exchange their experiences.
- Your local representative for Automation & Drives via our representatives database.
- Information on field service, repairs, spare parts and more under "Services".

Guide to the S7-300 Documentation

2

In this Chapter

you will find a guide to the documentation for the S7-300.

Selecting and configuring

Table 2-1 Influence of the ambient conditions on the automation system (AS)

Information on ...	is available in ...
What provisions do I have to make for PLC installation space?	Chapter *Configuring; Mounting dimensions of modules,* and *Mounting; mounting the rail*, in the *Installation Manual*
How do environmental conditions influence the PLC?	*Appendix of the Installation Manual*

Table 2-2 Electrical isolation

Information on ...	is available in ...
Which modules can I use if electrical isolation is required between sensors/actuators?	Chapter *Configuring; Electrical assembly, protective measures and grounding, in the Installation Manual* Reference Manual *Module Data*
When is it required to isolate the potential of specific modules? How do I wire this?	Chapter *Configuring; Electrical assembly, protective measures and grounding, in the Installation Manual* Chapter *Wiring, in the Installation Manual*
Under which conditions do I have to separate stations galvanically? How do I wire this?	Chapter *Configuring; Configuring a subnet, in the Installation Manual* Chapter *Wiring, in the Installation Manual*

Table 2-3 Communication between sensors/actuators and the automation system

Information on ...	is available in ...
Which module is suitable for my sensor/actuator?	for CPU: in applicable *CPU Data* Reference Manual for signal modules: *Module Data* Reference Manual
How many sensors/actuators can I connect to the module?	for CPU: in applicable *CPU Data* Reference Manual for signal modules: *Module Data* Reference Manual
To connect my sensors/actuators to the PLC, how do I wire the front connector ?	Chapter *Wiring; Wiring front connectors, in the Installation Manual*
When do I need expansion devices (EG) and how do I connect them?	Chapter *Configuring, optional expansions and networking, in the Installation Manual*
How do I mount modules in module racks / on profile rails?	Chapter *Mounting; Mounting modules on a rail, in the Installation Manual*

Table 2-4 Use of centralized and decentralized peripherals

Information on ...	is available in ...
Which range of modules do I want to use?	for local I/O / expansion modules (EMs): *Module Data* Reference Manual for distributed I/O / PROFIBUS DP: Manual of the relevant I/O device, e.g. *Manual ET 200B*

Table 2-5 Configuration consisting of the central unit (CU) and expansion modules (EMs)

Information on ...	is available in ...
Which rack / rail is best suited to my application?	Chapter *Configuring, in the Installation Manual*
Which Interface Modules (IM) do I need to connect the EGs to the ZG?	Chapter *Configuring, Arranging modules on multiple module racks, in the Installation Manual*
What is the right power supply (PS) for my application?	Chapter *Configuring, in the Installation Manual*

Table 2-6 CPU performance

Information on ...	is available in ...
Which memory concept is best suited for my application?	in applicable *CPU Data* Reference Manual
How do I insert and remove Micro Memory Cards?	Chapter *Commissioning; Inserting/Removing the Micro Memory Card, in the Installation Manual*
Which CPU meets my requirements on performance ?	*Instruction list*; Reference Manual *CPU Data*
How fast is the response / processing time of the CPU?	in applicable *CPU Data* Reference Manual
Which technological functions are implemented?	*Technological functions* Manual
How can I use these technological functions?	*Technological functions* Manual

Table 2-7 Communication

Information on ...	is available in ...
Which principles do I have to take into account?	Manual *Communication with SIMATIC*
Which options and resources are available on the CPU ?	in applicable *CPU Data* Reference Manual
How do I optimize communication with the help of communication processors (CPs)?	the respective manual
Which type of communication network is best suited to my application?	Chapter *Configuring; Configuring a subnet, in the Installation Manual* Manual *Communication with SIMATIC*
How do I network the specific modules?	Chapter *Configuring* and *wiring, in the Installation Manual*

Table 2-8 Software

Information on ...	is available in ...
Which software do I require for my S7-300 system?	Chapter *Technical Specification*; applicable *CPU Data* Reference Manual

Table 2-9 Supplementary features

Information on ...	is available in ...
How do I realize operator control and monitoring? (Human Machine Interface)	for text-based display units: the relevant device manual for OPs: the relevant device manual for WinCC: the relevant device manual
How do I integrate modules for instrumentation and control?	for PCS 7: the respective device manual
What options are offered by redundant and fail-safe systems?	Manual *S7-400H - Redundant Systems*; Manual *Fail-safe Systems*

Structure and communication functions

3

3.1 Operator control and display elements

3.1.1 CPU 31xC: Operator control and display elements

Elements of CPU 31xC

The following illustration shows the operator control and display elements of a CPU 31xC.

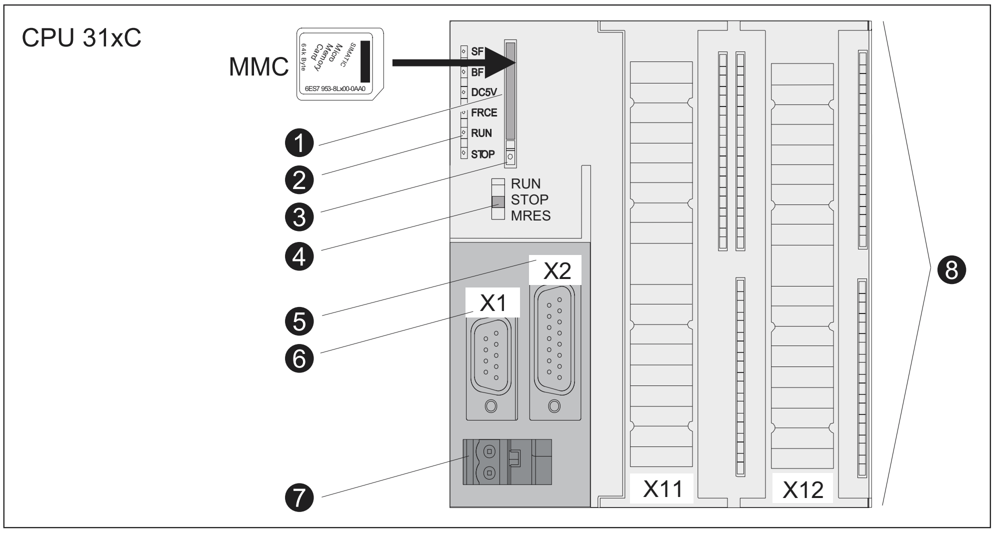

Figure 3-1 Elements and architecture of a CPU 31xC

The diagram illustrates under number	the following operator control / display element of your CPU
(1)	Slot for the Micro Memory Card (MMC)
(2)	Status and error displays
(3)	MMC ejector
(4)	Mode selector switch
(5)	Interface 2 X2 (PtP or DP)
(6)	Interface 1 X1 (MPI)
(7)	Power supply connection
(8)	Connection for the integrated inputs and outputs.

The next picture illustrates the integral digital and analog I/Os on a CPU 31xC with the front panels open.

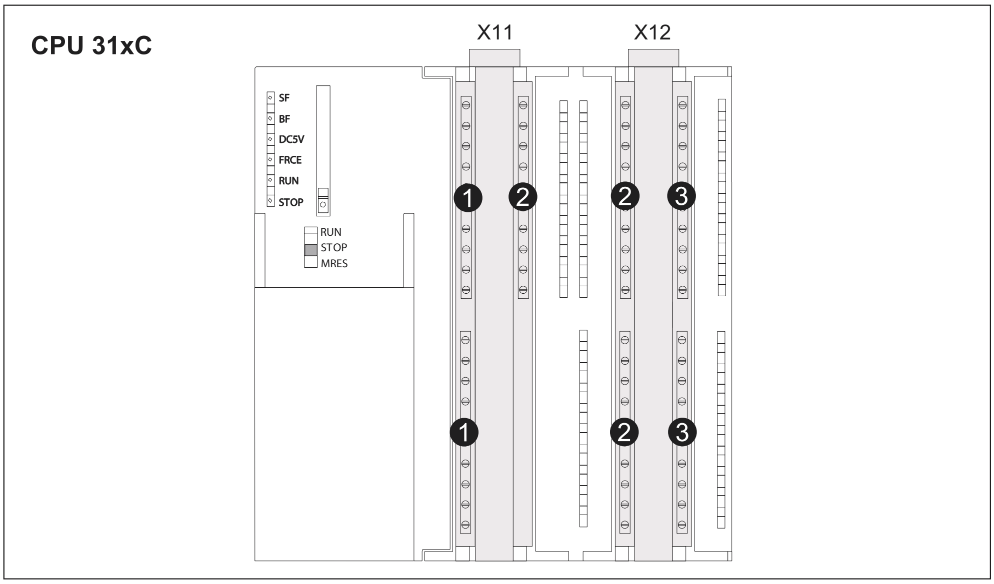

Figure 3-2 integrated I/Os on the CPU 31xC (e.g. a CPU 314C-2 PtP)

The diagram illustrates under number	The following integrated I/Os
(1)	Analog inputs and analog outputs
(2)	8 digital inputs
(3)	8 digital outputs

Differences between the CPUs

Table 3-1 Differences amongst the CPUs 31xC

Element	CPU 312C	CPU 313C	CPU 313C-2 DP	CPU 313C-2 PtP	CPU 314C-2 DP	CPU 314C-2 PtP
9-pin DP interface (X2)	–	–	X	–	X	–
15-pin PtP interface (X2)	–	–	–	X	–	X
Digital inputs	10	24	16	16	24	24
Digital outputs	6	16	16	16	16	16
Analog inputs	–	4 + 1	–	–	4 + 1	4 + 1
Analog outputs	–	2	–	–	2	2
Technological functions	2 counters	3 counters	3 counters	3 counters	4 counters 1 Channel for positioning	4 counters 1 Channel for positioning

Status and error displays

The CPU is equipped with following LED displays:

LED Name	With the LED color ...	the following CPU state is indicated:
SF	red	Hardware or software error
BF (only for CPUs with DP interface)	red	Bus error
5 VDC	green	5V power for CPU and S7-300 bus is OK
FRCE	yellow	Force job is active
RUN mode	green	CPU in RUN The LED blinks at startup with 2 Hz, in pause with 0.5 Hz.
STOP	yellow	CPU in STOP and PAUSE or startup The LED blinks for reset request with 0.5 Hz, during the reset with 2 Hz.

Using LEDs for diagnostics

Refer to the chapter *Testing functions, Diagnostics and Fault Elimination* in the *CPU 31xC and 31x Installation Manual*.

Slot for the SIMATIC Micro Memory Card (MMC)

A SIMATIC micro memory card (MMC) is used as the memory module. The MMC can be used as load memory and as portable storage medium.

Note

These CPUs do not have an integrated load memory, so an MMC MUST be inserted in order to use the CPU.

Mode Selector Switch

You can set the operating mode of the CPU with the mode selector switch. The mode selector switch is a three-position toggle switch.

Positions of the mode selector switch

The positions of the mode selector are explained in the order in which they appear on the CPU.

Table 3-2 Positions of the mode selector switch

Position	Description	Description
RUN mode	RUN mode	The CPU executes the user program.
STOP	STOP mode	The CPU does not scan user programs.
MRES	Memory reset	Mode selector switch position with momentary pushbutton function for CPU memory reset. Memory reset requires a specific sequence of operation (refer to the Installation Manual, Chapter *Commissioning*).

Power supply connector

Each CPU is equipped with a 2-pin power supply socket. When the CPU is supplied, the connector with screw terminals is already plugged into this socket.

Cross-reference

Further information on CPU operating modes is found in the *STEP 7 Online Help*.

For information on how to reset CPU memory using the mode selector switch, please refer to the Installation manual, Chapter *Commissioning*.

Details on error / diagnostics evaluation per LEDs are found in your Installation Guide, Chapter *Testing functions, Diagnostics and Fault Elimination*.

The *Memory concept* chapter contains information on using the MMCs and about the memory concept

3.1.2 CPU 31x: Operator control and display elements

Operator control and display elements of CPU 312, 314 and 315-2 DP

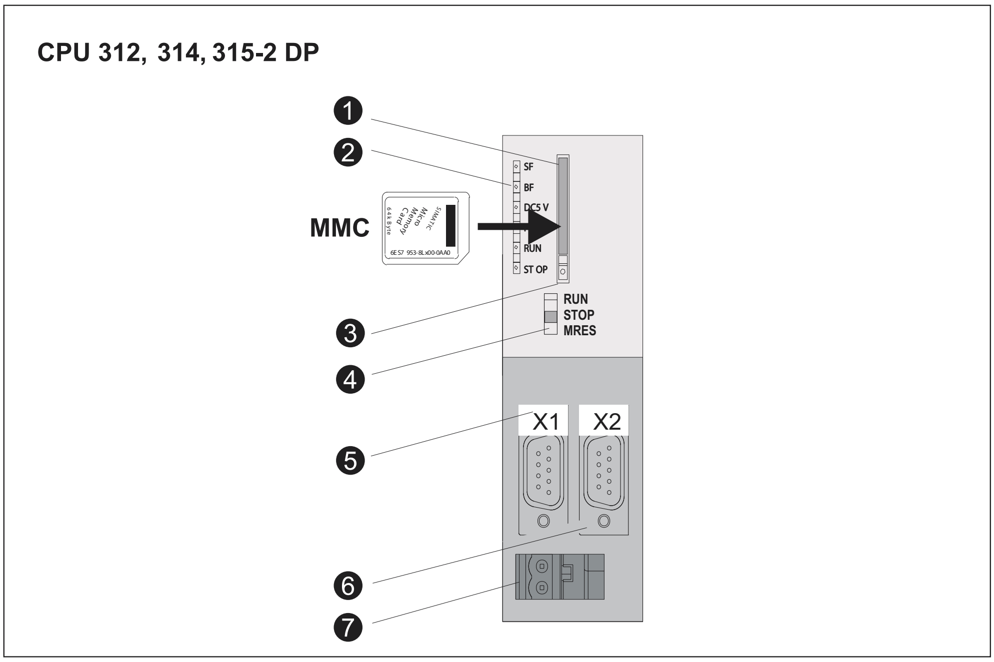

Figure 3-3 Operator control and display elements of CPU 312, 314 and 315-2 DP

The diagram illustrates under number	the following operator control / display element of your CPU
(1)	Slot for the Micro Memory Card (MMC)
(2)	Status and error displays
(3)	MMC ejector
(4)	Mode selector switch
(5)	Interface 1 X1 (MPI)
(6)	Interface 2 X2 (only for CPU 315-2 DP)
(7)	Power supply connection

Operator control and display elements of CPU 317-2 DP

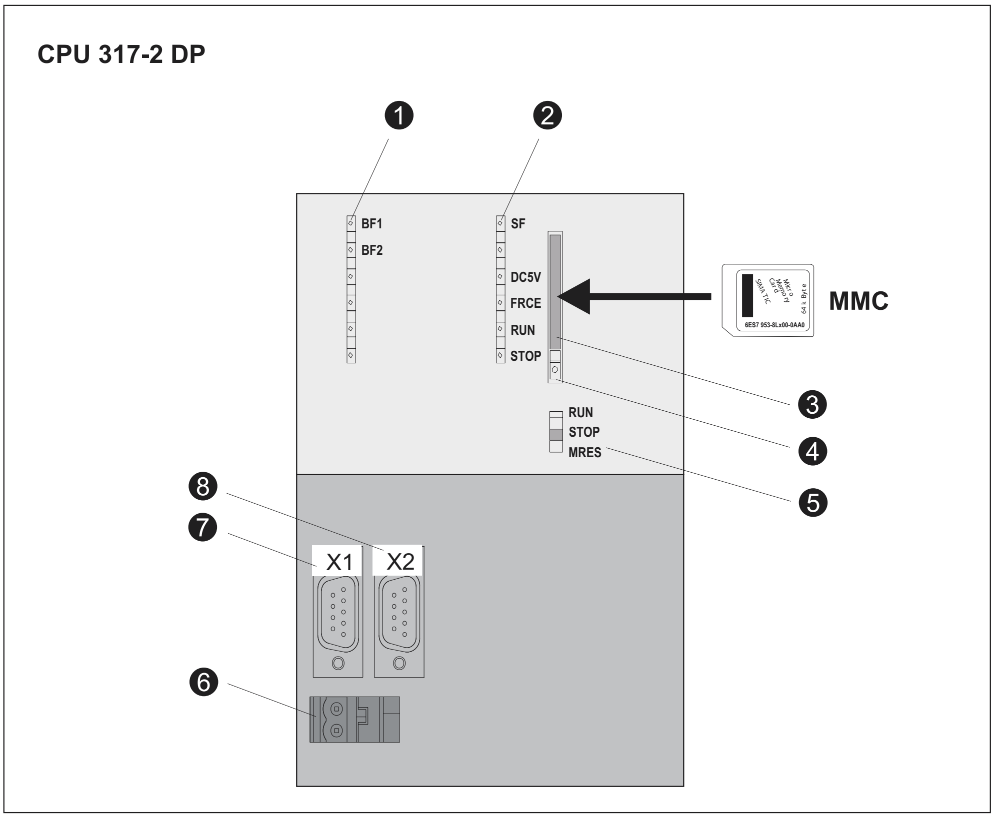

Figure 3-4 Operator control and display elements of CPU 317-2 DP

The diagram illustrates under number	the following operator control / display element of your CPU
(1)	Bus error
(2)	Status and error displays
(3)	Slot for the Micro Memory Card (MMC)
(4)	MMC ejector
(5)	Mode selector switch
(6)	Power supply connection
(7)	Interface 1 X1 (MPI/DP)
(8)	Interface 2 X2 (DP)

Differences between the CPUs

Table 3-3 Differences amongst the CPUs 31x

Element	CPU 312	CPU 314	CPU 315-2 DP	CPU 317-2 DP
The first interface of the CPU is a				
• MPI interface X1 (9-pin)	X	X	X	-
• MPI/DP interface X1 (9-pin)	-	-	-	X
The second interface of the CPU is a DP interface X2 (9-pin.)	-	-	X	X

Status and error displays

The CPU is equipped with following LED displays.

LED Name	With the LED color ...	the following CPU state is indicated:
SF	red	Hardware or software error
BF (CPU 315-2 DP only)	red	Bus error at DP interface (X2)
BF1 (CPU 317-2 DP only)	red	Bus error at interface 1 (X1)
BF2 (CPU 317-2 DP only)	red	Bus error at DP interface 2 (X2)
5 VDC	green	5V power for CPU and S7-300 bus is OK
FRCE	yellow	Force job is active
RUN mode	green	CPU in RUN The LED blinks at startup with 2 Hz, in pause with 0.5 Hz.
STOP	yellow	CPU in STOP and PAUSE or startup The LED blinks for reset request with 0.5 Hz, during the reset with 2 Hz.

Using LEDs for diagnostics

Refer to the chapter *Testing functions, Diagnostics and Fault Elimination* in the *CPU 31xC and 31x Installation Manual*.

Slot for the SIMATIC Micro Memory Card (MMC)

A SIMATIC micro memory card (MMC) is used as the memory module. The MMC can be used as load memory and as portable storage medium.

Note

These CPUs do not have an integrated load memory, so an MMC MUST be inserted in order to use the CPU.

Mode Selector Switch

You can set the operating mode of the CPU with the mode selector switch. The mode selector switch is a three-position toggle switch.

Positions of the mode selector switch

The positions of the mode selector are explained in the order in which they appear on the CPU.

Table 3-4 Positions of the mode selector switch

Position	Description	Description
RUN mode	RUN mode	The CPU executes the user program.
STOP	STOP mode	The CPU does not scan user programs.
MRES	Memory reset	Mode selector switch position with momentary pushbutton function for CPU memory reset. Memory reset requires a specific sequence of operation (refer to the Installation Manual, Chapter *Commissioning*).

Power supply connector

Each CPU is equipped with a 2-pin power supply socket. When the CPU is supplied, the connector with screw terminals is already plugged into this socket.

Further information

Further information on CPU operating modes is found in the *STEP 7 Online Help*.

For information on how to reset CPU memory using the mode selector switch, please refer to the Installation manual, Chapter *Commissioning*.

Details on error / diagnostics evaluation per LEDs are found in your Installation Guide, Chapter *Testing functions, Diagnostics and Fault Elimination*.

The *Memory concept* chapter contains information on using the MMCs and about the memory concept

3.2 SIMATIC Micro Memory Card (MMC)

The MMC as a memory module for the CPU

Your CPU uses a SIMATIC Micro Memory Card (MMC) as a memory module. You can use MMCs as load memory or as a portable storage medium.

Note

An MMC must be plugged in before you can use the CPU.

The following data is stored on MMC:

- User programs (all blocks)
- Archives and recipes
- Configuration data (STEP 7 projects)
- Data for an operating system update and backup

Note

On one MMC you can either store user and configuration data or the operating system.

Properties of an MMC

The MMC ensure maintenance-free and retentive operation of these CPUs. The chapter *Memory Concept* provides more details about retentive operation.

Caution

Data on a SIMATIC Micro Memory Card can be corrupted if you remove the card during write access. In this case you might have to insert the MMC memory in your PG to delete it, or you format the card in the CPU.

Never remove an MMC in RUN mode. Always remove when power is off or when the CPU is in STOP state and when no PG performs a write access the card. Disconnect the communication lines if you cannot safely exclude active write access functions from the PG (e.g. load/delete function block).

Plug-in SIMATIC Micro Memory Cards

The following memory modules are available:

Table 3-5 Available MMCs

Type	Order number	Required for a firmware update with ...
MMC 64k	6ES7 953–8LF00–0AA0	–
MMC 128k	6ES7 953–8LG00–0AA0	–
MMC 512k	6ES7 953–8LJ00–0AA0	–
MMC 2M	6ES7 953–8LL00–0AA0	CPUs without a DP interface
MMC 4M	6ES7 953–8LM00–0AA0	CPUs with a DP interface
MMC 8M	6ES7 953–8LP10–0AA0	–

MMC copy protection

Your MMC has an internal serial number that provides copy protection for the MMC at the user level. You can read this serial number via the SLL sublist $011C_H$ index 8 using SFC 51 "RDSYSST".

You can then program a STOP command, for example, in a copy-protected block if the expected and actual serial numbers of your MCC do not tally.

Further information can be found in the *SLL Sublist in the List of Operations* or the *System and Standard Functions* manual.

Maximum number of blocks that can be loaded in the MMC

The number of blocks that can be stored on the MMC depends on the capacity of the MMC being used. The maximum number of blocks that can be loaded is therefore limited by the capacity of your MMC (including blocks generated with the "CREATE DB“ SFC):

Table 3-6 Maximum number of loadable blocks on the MMC

Size of MMC	Maximum number of blocks that can be loaded
64 Kbyte	768
128 Kbyte	1024
512 Kbyte	Here the maximum number of blocks that can be loaded for the specific CPU is less than the number of blocks that can be stored on the MMC. Refer to *Specifications* of a specific CPU to determine the maximum number of blocks that can be loaded.
2 Mbyte	
4 Mbyte	
8 Mbyte	

Useful life of an MMC

The useful life of an MMC depends mainly on following criteria:

1. The number of delete or programming steps
2. external influences such as ambient temperature.

At ambient temperatures up to 60° C, a maximum of 100,000 delete/write operations can be performed on an MMC.

Caution

As a precaution against data loss, always make sure that the maximum number of delete/write operations is not exceeded.

Cross-reference

To learn how to reset or format an MMC, refer to the Commissioning chapter of the installation manual *S7-300 Hardware and Installation: CPU 31xC and CPU 31x.*

3.3 Interfaces

MPI interface

Availability: In all the CPUs described in this document.

The MPI (Multipoint Interface) represents the CPU's interface for PG/OP connections or for communication in an MPI subnet.

The typical (default) baud rate for all CPUs is 187.5 Kbps. You can also set the rate to 19.2 Kbps for communication with an S7-200. Other baud rates are only possible with CPU 317-2 DP (up to 12 Mbps).

The CPU broadcasts its bus parameter configuration via the MPI interface (e.g. the transmission rate). This allows a PG, for example, to acquire the correct parameters and automatically connect to an MPI subnet.

Note

In RUN mode you may only connect PGs to the MPI subnet.
Other stations (e.g.. OP, TP, ...) should not be connected to the MPI subnet while the PLC is in run mode. Otherwise, transferred data might be corrupted as a result interference or global data packages be lost.

PROFIBUS DP interface

Availability: CPU types with the "DP" in their name

The PROFIBUS-DP interface is mainly used to connect distributed I/O. PROFIBUS DP allows you to create large, extended subnets, for example.

The PROFIBUS DP interface can be configured as either master or slave, and offers a transmission speed of up to 12 Mbps.

The CPU sends its bus parameters (e.g. the baud rate) to the PROFIBUS DP interface (if it is used as the master). A programming device, for example, can then automatically retrieve the correct parameters and connect to a PROFIBUS subnet. In your configuration, you can disable this bus parameter broadcast.

CPU 317-2 DP has two DP interfaces: The first interface is an MPI/DP interface that you can reconfigure as a PROFIBUS interface in STEP 7.

Table 3-7 Possible interface operating modes for CPU 317-2 DP

MPI/DP interface (X1)	PROFIBUS DP interface (X2)
• MPI • DP master • DP slave 1)	• Not assigned • DP master • DP slave 1)

1) Excluded: DP slave at both interfaces simultaneously

Note

(For the DP interface in slave mode).

If you have disabled the Commissioning / Test mode check box in the DP interface properties in STEP 7, the baud rate you have set will be ignored, and the master's baud rate will be used automatically, The routing function is then no longer possible over this interface.

Cross-reference

For information on the new DPV1 functionality, see the section with the same name in the *CPU Data Reference Manual, CPU 31xC and CPU 31x*.

PtP interface

Availability: CPU types with the identifier "PtP".

You can use the PtP (Point to Point) interface on your CPU to connect external devices such as a barcode reader, printer, etc. to a serial port. Baud rates of up to 19.2 Kbps for full duplex (RS 422) and up to 38.4 Kbps for half duplex (RS 485) are possible.

The following PtP communication drivers are installed in the CPUs:

- ASCII driver
- 3964(R) Protocol
- RK 512 (only CPU 314C-2 PtP)

Which devices can I connect to which interface?

Table 3-8 The following devices may be connected

MPI	PROFIBUS-DP	PtP
• PG/PC • OP/TP • S7-300/400 with MPI interface • S7-200 (19.2 Kbps only)	• PG/PC • OP/TP • DP slaves • DP master • Actuators/Sensors • S7-300/400 with PROFIBUS-DP interface	• Devices equipped with a serial port, e.g. barcode readers, printers, etc.

Further information

Further information on specific connections can be found in the *Communication with SIMATIC* manual.

Details on PtP communication is found in the *Technological Functions* Manual.

3.4 DPV1 functions

What do we mean by DPV1?

New automation and process engineering tasks require the range of functions performed by the existing DP protocol to be extended. In addition to cyclical communication functions, acyclical access to non-S7 field devices is another important requirement of our customers, and was implemented in the standard EN 50170. In the past, acyclical access was only possible with S7 slaves.

Definition DPV1

The term DPV1 is defined as a functional extension of the acyclical services (to include new interrupts, for example) provided by the DP protocol.

The distributed I/O standard EN 50170 has been further developed. All the changes concerning new DPV1 functions are included in IEC 61158/ EN 50170, volume 2, PROFIBUS.

DPV1 offers the following enhanced functions:

- Use of any DP1 slaves from external vendors (in addition to the existing DPV0 and S7 slaves, of course).
- Selective handling of DPV1-specific interrupt events by new interrupt blocks.
- Reading/writing SFBs that conform to standards to the record (although this can only be used for centralized modules).
- User-friendly SFB for reading diagnostics.

The following CPUs serving as DP masters support DPV1 functionality

All CPUs with DP interface(s) and serving as DP masters feature the enhanced DPV1 functionality.

Note

If you want to use the CPU as an intelligent slave, remember that it does not have DPV1 functionality.

Requirement for using the DPV1 functionality with DP slaves

For DPV1 slaves from other vendors, you will need a GSD file conforming to EN 50170, revision 3 or later.

Interrupt blocks that support the DPV1 functionality.

Table 3-9 Interrupt blocks with DPV1 functionality

OB	Functionality
OB 82	Diagnostic interrupt
OB 40	Process interrupt
OB 55	Status interrupt
OB 56	Update interrupt
OB 57	Vendor-specific interrupt

Note

You can now also use organizational blocks OB82 and OB40 for DPV1 interrupts.

System function blocks that support the DPV1 functionality.

Table 3-10 System function blocks with DPV1 functionality

SFB	Functionality
SFB 52	Read record from DP slave or centralized module
SFB 53	Write record to DP slave or centralized module
SFB 54	Read additional alarm information from a DP slave or a centralized module in the relevant OB.
SFB 75	Set any interrupts for intelligent slaves

Note

You can also use SFB 52 to SFB 54 for centralized I/O modules.

Cross-reference

In this context, you should also note the *Information on upgrading to a CPU 31xC, 312, 314, 315-2 DP.* Read the chapter of the same title in the *CPU Data Reference Manual, 31xC and 31x*.

You will find further information on the blocks mentioned above in the *System Software for S7-300/400* Reference Manual*: System and Standard Software,* or directly in the *STEP7 Online Help*.

3.5 Real-time clock

Properties and Functions

The table below shows the properties and functions of the real-time clock.

Table 3-11 Properties and functions of the real-time clock

Characteristics	CPU 312C, CPU 312	All other CPUs
Type	Software clock	Hardware clock
Manufacturer setting	DT#1994-01-01-00:00:00	DT#1994-01-01-00:00:00
Buffering	No	with integrated capacitor
Backup period	–	Typically 6 weeks (at an ambient temperature of 40 °C)
Behavior of the real-time clock after POWER ON	The clock keeps running, continuing with the time it had when the power was switched off.	The clock continues running after the POWER OFF.
Behavior of the clock on expiration of the backup period	–	The clock keeps running, continuing at the time-of-day it had when power was switched off.

Information on ...

- Synchronization and correction factor:

  When you configure your CPU in *STEP 7*, you can customize functions such as synchronization via MPI interface and the correction factor. Refer to the *STEP 7 Online Help*.

- Setting, reading and programming the real-time clock:

  You can read and set the real-time clock with your PG (refer to the Manual *Programming with STEP 7*). or you program the respective SFCs in your application program (refer to the *System and Standard functions*) Reference Manual.

3.6 S7 Connections

Introduction

An S7 connection is established when S7 modules communicate with one another. This connection represents the communication path.

Note

Global data communications and PtP communications do not require an S7 connection.

Every communication link requires S7 connection resources on the CPU for the entire duration of each link.

Thus, every S7 CPU provides a specific number of S7 connection resources. These are used by various communication services (PG/OP communication, S7 communication or S7 basic communication).

What are S7 connection points?

An S7 connection between modules with communication capability is established between connection points. The S7 connection always has two connection points: the active and the passive connection point:

- The active connection point is assigned to the module that establishes the S7 connection.
- The passive connection point is assigned to the module that accepts the S7 connection.

Any module that is capable of communication can thus act as an S7 connection point. At the connection point, the established communication link always uses **one** S7 connection of the module concerned.

Transition point of an S7 connection

If you use the routing functionality, the S7 connection between two modules capable of communication is established across a number of subnets. These subnets are interconnected via a gateway. The module that implements this gateway is known as a router. The router is thus the point through which an S7 connection passes.

Any CPU with a DP interface can be the router for an S7 connection. They can establish up to four routed connections (or up to 8 with CPU 317-2 DP) without restricting the equipment required for the S7 connections.

Allocating S7 connections

There are several ways to allocate S7 connections on a communication-capable module:

Reservation when programming

- *STEP 7* automatically reserves one S7 connection per PG communication, respectively OP communication in a CPU inserted during hardware configuration.
- In *STEP 7* you can reserve S7 connections for PG / OP / S7-based communication.

Allocating connections via programming

S7-based communication is established by the user program. The CPU's operating system initiates the connection and allocates the respective S7 connection.

Assigning connections during commissioning, testing and diagnostics

The online function of the engineering station (PG/PC with *STEP 7*) is used to assign S7 connections for PG communication:

- An S7 connection resource for PG communication which was reserved in your CPU hardware configuration is assigned to the engineering station, that is, it only needs to be allocated.
- If all reserved S7 connection resources for PG communication are occupied, the operating system assigns a free S7 connection resource which has not yet been reserved. If no more connection resources are available, the engineering station cannot go online to the CPU.

Allocating connection resources to O&M services

An Online function of the B&B station (OP/TP/... with *ProTool*) uses S7 connections for OP communication:

- An S7 connection resource for OP communication you have reserved in your CPU hardware configuration is therefore assigned to the O&M station engineering station, that is, it only needs to be allocated.
- If all reserved S7 connection resources for OP communication have been allocated, the operating system assigns a free S7 connection resource. If no more connection resources are available, the O&M station cannot go online to the CPU.

Time sequence for the allocation of S7 connection resources

Parameter assignment blocks are generated during configuration in *STEP 7*. They are called up on startup of the module. Here the module's operating system reserves or assigns the respective S7 connections. This implies, for example, that an operator station cannot access a reserved S7 connection for PG communication.

The module's S7 connection resources which were not reserved (CPU) can be used freely. These S7 connection resources are allocated in the order they are requested.

Example:

If there is only one free S7 connection left on the CPU, you can still connect a PG to the bus. The PG can then communicate with the CPU. The S7 connection is only used, however, when the PG is communicating with the CPU.

If you attach an OP to the bus while the PG is not communicating, the OP can establish a connection to the CPU. Since an OP maintains its communication link at all times, in contrast to the PG, you cannot then establish another connection via the PG.

Distribution of S7 connection resources

The following table illustrates how the S7 connection resources of CPUs are distributed:

Table 3-12 Distribution of S7 connection resources

Communication Service	Distribution
PG communication OP communication S7-based communication	In order to make the allocation of connection resources dependent not only on the chronological sequence in which various communication services are registered, S7 connection resources can be reserved for the following services. For PD and OP communication respectively, at least one S7 connection resource is reserved by default. In the table below, and in the specifications of the CPUs, you can find the configurable S7 connection resources and the default configuration for each CPU. You can "redistribute" the S7 connection resources in *STEP 7*, when you configure the CPU parameters.
S7 communication Other communication resources (e.g. via CP 343-1, with a data length of > 240 bytes)	Here you can assign free S7 connection resources which have not been reserved for a specific service (PG/OP communication, S7 Basic communication.
Routing PG functions (only for CPUs with DP interface)	The CPUs can establish up to four connections for routing (or up to 8 with CPU 317-2 DP). These connection resources are available in addition to S7 connection resources.
Global data communication PtP communication	These communication services do **not** use S7 connection resources.

Availability of S7 connection resources

The table below shows S7 connection resources available on specific CPUs.

Table 3-13 Availability of S7 connection resources

Parameters	Total number of S7 connection	Reserved for PG communication	Reserved for OP communication	Reserved for S7-based communication	Free S7 connections
312C	6	1 to 5, default 1	1 to 5, default 1	0 to 2, default 2	Displays S7 connection resources which are not reserved as free connection resources.
313C/ 313C-2 PtP 313C-2 DP	8	1 to 7, default 1	1 to 7, default 1	0 to 4, default 4	
314C-2 PtP 314C-2 DP	12	1 to 11, default 1	1 to 11, default 1	0 to 8, default 8	
312	6	1 to 5, default 1	1 to 5, default 1	0 to 2, default 2	
314	12	1 to 11, default 1	1 to 11, default 1	0 to 8, default 8	
315-2 DP	16	1 to 15, default 1	1 to 15, default 1	0 to 12, default 12	
317-2 DP	32	1 to 31, default 1	1 to 31, default 1	0 to 30, default 0	

Example of a CPU 314C-2 DP

The CPU 314C-2 DP provides 12 S7 connections:

- You reserve two S7 connections for PG communication.
- Reserve three S7 connection resources for OP communication.
- Reserve one S7 connection resource for S7-based communication.

This leaves six S7 connection resources available for any communication service, e.g. S7 communication, OP communication etc.

Details ...

- on SFCs are found in the *Instruction list*, for details refer to the *Online Help for STEP 7* or to the *System and Standard Functions* Reference Manual.
- on communication are found in the Manual *Communication with SIMATIC*.
- on routing can be found in the Routing chapter and in the *STEP 7 Online Help*.

3.7 Communications

Communication Services of the CPUs

You need to decide on a communication service depending on the desired functionality. Your choice of communication service will have no effect on:

- the functionality to be provided,
- whether an S7 connection is required, or
- when the connection is established.

User interface characteristics can be quite different (SFC, SFB, ...), depending on the hardware used (SIMATIC CPU, PC, ...).

The following table summarizes the communication services provided by the CPUs.

Table 3-14 Communication services provided by CPUs

Communication service	**Functionality**	**Time at which the S7 connection is established ...**	**via MPI**	**via DP**	**via PtP**
PG communication	Start-up, test, diagnostics	via PG when the service is being used	X	X	–
OP communication	Operator control and monitoring	via OP at POWER ON	X	X	–
S7-based communication	Data exchange	is programmed via blocks (SFC parameters)	X	–	–
S7 communication	Data exchange	Only as a server; the connection is established by the communication partner	X	X	–
Global data communication	cyclic data exchange (e.g. memory bits)	does not require an S7 connection	X	–	–
Routing PG functions (only for CPUs with DP interface)	e.g. testing, diagnostics extending over network limits	via PG when the service is being used	X	X	–
PtP communication (only for CPUs with PtP interface	Data exchange via serial interface	does not require an S7 connection	–	–	X

PG communication

PG communication is used to exchange data between engineering stations (e.g. PG, PC) and SIMATIC modules that are capable of communication. This service is possible via MPI / PROFIBUS / industrial Ethernet subnets. Transition between subnets is also supported.

PG communication provides functions required for loading programs and configuration data, as well as for testing and evaluating diagnostic information. These functions are integrated in the operating system of SIMATIC S7 modules.

A CPU can maintain several simultaneous online connections to one or multiple PGs.

OP communication

OP communication is used to exchange data between operator stations (e.g. OP, TP) and communication-capable SIMATIC modules. This service is possible via MPI / PROFIBUS / industrial Ethernet subnets.

OP communication provides functions required for operating and monitoring. These functions are integrated in the operating system of SIMATIC S7 modules.

A CPU can maintain several simultaneous connections to one or several OPs.

S7-based communication

S7-based communication is used to exchange data between S7 CPUs and the communication-capable SIMATIC modules within an S7 station (acknowledged data exchange). Data exchange takes place via non-configured S7 connections. The service can be used on an MPI subnet or for internal communication between the station and function modules (FM).

S7 basic communication provides functions required for data exchange. These functions are integrated into the CPU operating system.

The user can utilize this service via "System function" (SFC) user interface.

S7 Communication

The CPUs as the server in S7 communication. The connection is always established by the communication partner. This service is possible via MPI / PROFIBUS / industrial Ethernet subnets.

The operating system processes these services without explicit user interface.

Note

S7 communication as a client can be implemented using CPs and loadable FBs.

Global data communication

Global data communication is used for cyclic exchange of global data (e.g. I, Q, M) between SIMATIC S7 CPUs (data exchange with no acknowledgement). One CPU broadcasts the data to all other CPUs on the MPI subnet. This function is integrated in the CPU operating system.

Conditions for sending and receiving

For GD circuit communication, the following conditions should always be fulfilled:

- For the station sending a GD packet:
  $\text{Scan rate}_{\text{Sending station}} \times \text{Cycle time}_{\text{Sending station}} \geq 60\text{ ms}$
- For the station receiving a GD packet:
  $\text{Scan rate}_{\text{Receiving station}} \times \text{Cycle time}_{\text{Receiving station}}$
  $< \text{Scan rate}_{\text{Sending station}} \times \text{Cycle time}_{\text{Sending station}}$

A GD packet may be lost if you do not maintain these conditions. The reasons for this are:

- the performance of the "smallest" CPU in the GD circuit
- the sending/receiving stations exchange global data asynchronously

if you specify in *STEP 7* : "Send data after every CPU cycle" - with a short CPU cycle time (< 60 ms) - the operating system might overwrite the CPU's GD package before it is transmitted. Loss of global data is indicated in the status field of the GD circuit, provided you have configured this feature in *STEP 7.*

Scan rate

The scan rate specifies the cycle intervals for GD communication. You can customize this scan rate when you configure global data communication in *STEP 7* . For example, if you select a scan rate of 7, global data is transferred only after every 7th cycle. This reduces CPU load.

GD resources

The table below shows the GD resources of CPUs.

Table 3-15 GD resources of CPUs

Parameters	CPU 31xC, 312, 314	CPU 315-2 DP, 317-2 DP
Number of GD circuits per CPU	max. 4	max. 8
Number of send GD packets per GD circuit	max. 1	max. 1
Number of send GD packets of all GD circuits	max. 4	max. 8
Number of receive GD packets per GD circuit	max. 1	max. 1
Number of receive GD packets of all GD circuits	max. 4	max. 8
Data length per GD packet	max. 22 bytes	max. 22 bytes
Consistency	max. 22 bytes	max. 22 bytes
Min. scan rate (default)	1 (8)	1 (8)

Routing

With the CPU configured as the DP master and *STEP 7* V 5.1 + Service Pack 4 or later, you can use a PG/PC to access S7 stations via various subnets (MPI interface / PROFIBUS DP interface).

You can download user programs or a hardware configuration, or run testing and commissioning functions, for example.

Note

If you use your CPU as an intelligent slave, the routing function can only be used with an actively-configured DP interface.

In the properties of the DP interface in STEP 7, tick the Commissioning / Test mode check box.

You will find further information in the *Programming with STEP 7manual* or in the STEP 7 Online Help.

Point-to-Point Communication

PtP communication enables data exchange via serial interface. PtP communication can be used to interconnect automation devices, computers or other communication-capable non-Siemens systems. Adaptation to the communication partner's protocol is also possible.

Cross-reference

- on SFCs are found in the *Instruction list*, for details refer to the *Online Help for STEP 7* or to the *System and Standard Functions* Reference Manual.
- on communication are found in the Manual *Communication with SIMATIC*.

3.8 Routing

PG/PC access to stations on another subnet

Beginning with *STEP 7* V5.1 + SP 4, the PG/PC can connect to S7 stations beyond subnet boundaries, for example, to:

- Load user programs
- Load hardware configurations
- Perform tests and diagnostic functions

The routing function allows you to connect a PG at any point on the network, and to establish a connection to all stations that can be accessed via gateways.

The CPUs with DP interface provide four connection resources for routing PG functions. These connection resources are available in addition to S7 connection resources.

Note

If you use your CPU as an intelligent slave, the routing function can only be used with an actively-configured DP interface.

In the properties of the DP interface in STEP 7, tick the Commissioning / Test mode check box.

You will find further information in the *Programming with STEP 7manual* or in the STEP 7 Online Help.

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gateway

Gateways between subnets are routed in a SIMATIC station that is equipped with interfaces to the respective subnets. In the illustration below, the CPU serving as the DP master acts as the router between subnet 1 and subnet 2.

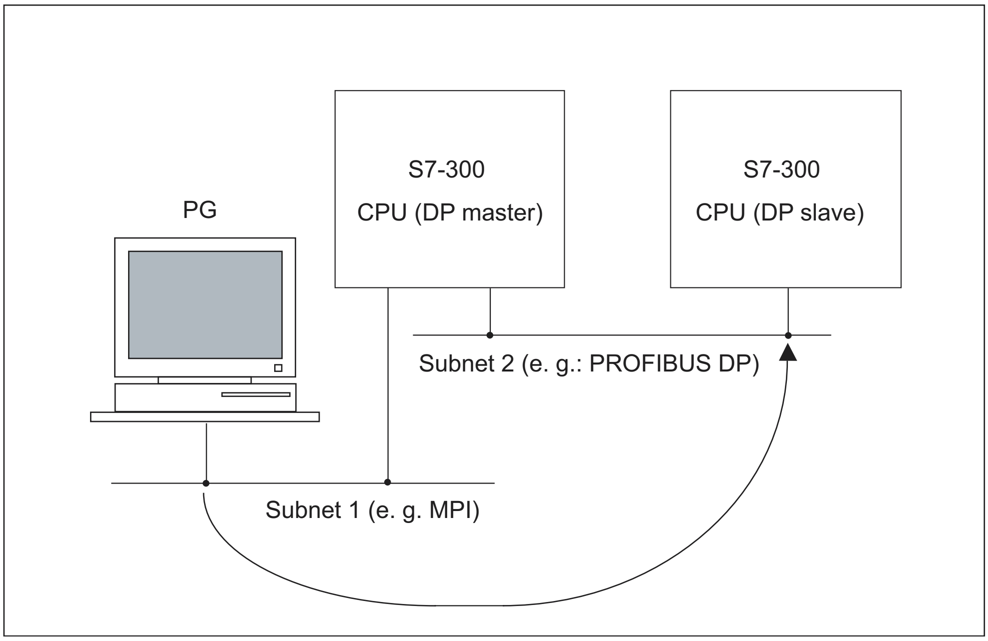


Figure 3-5 Routing - Network node

Requirements

- The station modules must be "routing-compatible" (CPUs or CPs).
- The network configuration does not exceed project limits.
- The modules must have downloaded the configuration data containing the latest "knowledge" of the entire project network configuration.

  Reason: All modules accessing the network node must receive information on available subnets and network paths (= routing information).
- In your network configuration, the PG/PC you want to use to establish a connection via network node must be assigned to the network it is physically connected to.
- The CPUs must either be configured as the master or
- If the CPU is configured as the slave, then the Commissioning / Test mode functionality must be activated under the properties of the DP interface for DP slaves in STEP 7.

Sample application: TeleService

The picture below contains a sample application: remote maintenance of an S7 station by a PG. The connection is established across subnet boundaries and requires a modem.

The lower part of the figure shows you how easy it is to configure this feature in *STEP 7*.

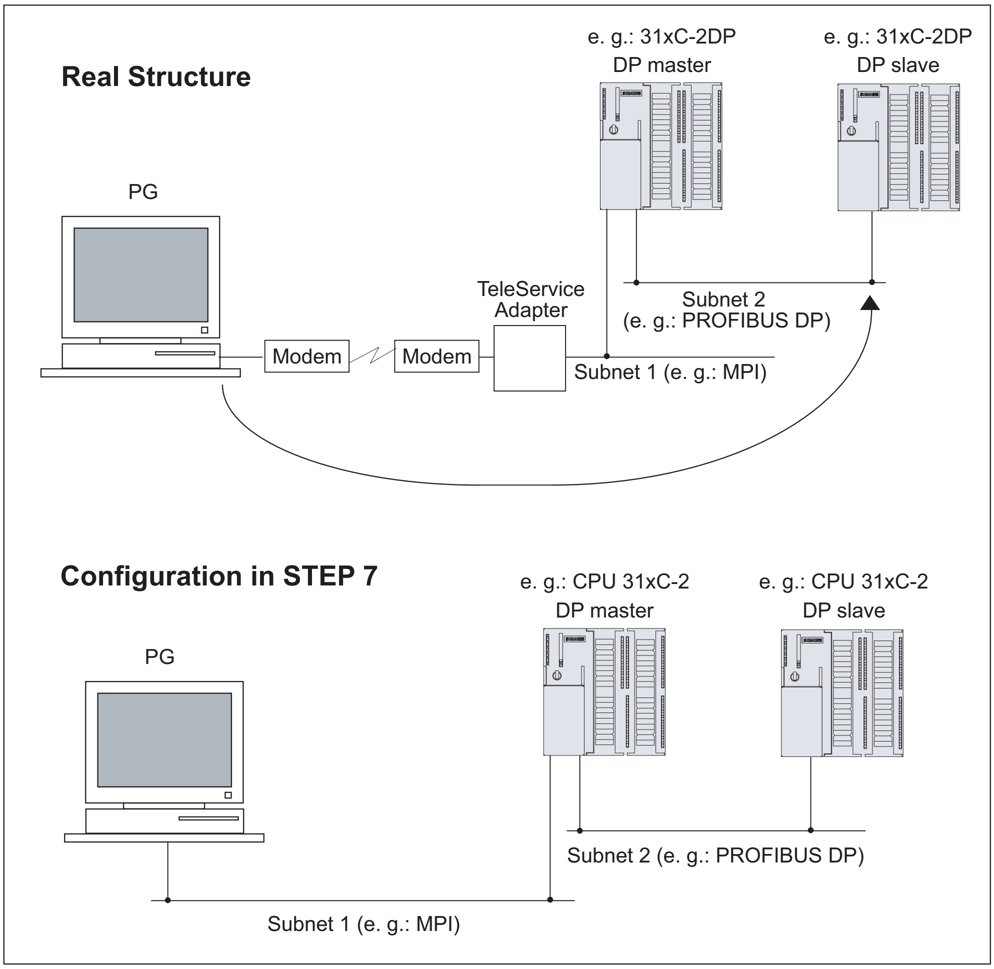


Figure 3-6 Routing - Sample application TeleService

Further information ...

- on configuration with *STEP 7* is found in the *Configuring Hardware and Connections with STEP 7* manual.
- of a basic nature is contained in the *Communication with SIMATIC* manual.
- on the TeleService adapter can be found on the Internet at http://www.ad.siemens.de/support. In the Manual Search section you can enter the search term A5E00078070 to download the documentation.

3.9 Data consistency

A data area is considered consistent, if the operating system can read/write access the data area in a continuous block. Data exchanged collectively between the stations should belong together and originate from a single processing cycle, that is, be consistent.

If there is a programmed communication function such as X-SEND/ X-RCV which accesses shared data, then access to that data area can be coordinated by means of the parameter "BUSY“ itself.

With PUT/GET functions

With S7 communication functions, such as PUT/GET or write / read via OP communication that do not require a block in the user program on the CPU (acting as the server), then the extent of the data consistency must have been considered at the programming stage.

The PUT/GET functions for S7 communication or for reading/writing variables via OP communication are executed at the CPU's scan cycle checkpoint.

To ensure a defined process interrupt response time, communication variables are copied consistently to/from user memory, in blocks with a maximum size of 64 bytes (CPU 317-2 DP: 160 bytes), during the scan cycle checkpoint of the operating system. Data consistency is not guaranteed for data areas that are any larger.

Note

If a defined level of data consistency is required, the length of communication variables in the user program must therefore not exceed 64 bytes (CPU 317-2 DP: 160 bytes).

Memory concept

4

4.1 Memory areas

4.1.1 Distribution of the memory

Introduction

The CPU memory can be divided into three areas:

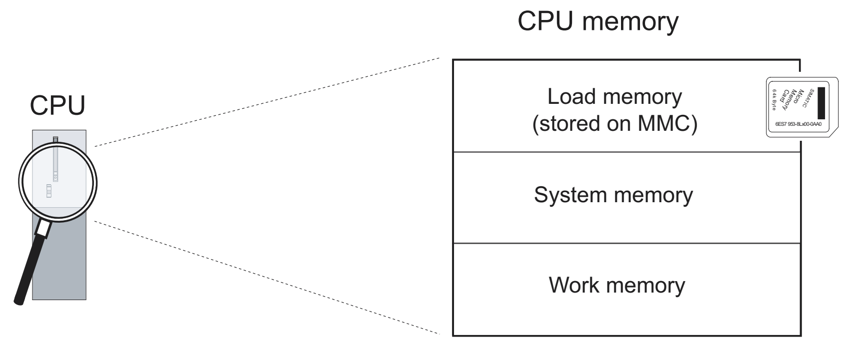


Figure 4-1 CPU memory areas

Load memory

The load memory is located on a Micro Memory Card (MMC). The amount of load memory corresponds exactly to the MMC. It serves to store code and data blocks as well as system data (configuration, connection, module parameters, etc.).

Blocks that are identified as non runtime-related are stored exclusively in load memory.

You can also store all the configuration data for your project on the MMC.

Note

The user program can only be downloaded and thus the CPU can only be used if the MMC is inserted.

RAM (work memory)

The RAM is integrated in the CPU and cannot be extended. Its only purpose is processing of code and user program data. Programs only run in RAM and system memory.

The RAM of **CPU 31xC, 312, 314** and **315-2 DP** is always retentive.

For **CPU 317-2 DP**,256 Kbytes of RAM can be used for retentive data blocks. The remainder of the RAM can only be used for code blocks and non-retentive data blocks.

System memory

The RAM system memory is integrated in the CPU and cannot be expanded.

It contains

- the address areas for memory bits, timers and counters
- the process image of the I/Os
- local data

4.1.2 Retentive memory

Introduction

Your CPU is equipped with retentive memory . Retentive memory is provided by the MMC and CPU. Data is kept in retentive memory across POWER OFF and restart (warm start).

Load memory

Your program in the load memory is always retentive; It is saved upon loading on the MMC to protect against network failure and resets.

System memory

In your configuration (CPU properties, Retentive memory tab), specify which part of flag bits, timers and counters should be kept retentive and which of them are to be initialized with "0" on restart (warm restart).

Generally, the diagnostic buffer, MPI address (and transmission rate) and operating hour counter are written to retentive CPU memory. Retentivity of the MPI address and transmission rate ensures that your CPU is still capable of communication even after power loss, memory reset or loss of communication parameters (e.g. removal of the MMC or deletion of communication parameters).

Work memory

On POWER OFF the retentive data is saved to the MMC. Therefore, the content of retentive data blocks is always retentive.

Non-retentive DBs are also supported for CPU 317-2 DP (the non-retentive DBs are initialized with their start values from the load memory even for restarts (warm starts) and POWER ON).

Cross-reference

see Retentive response of the DBs for CPU 317-2 DP

Retentive behavior of memory objects

The table below shows the retentive behavior of memory objects during specific operating state transitions.

Table 4-1 Retentive behavior of memory objects

Memory Object	**Operating state transition**		
	POWER ON / POWER OFF	**RUN → STOP**	**Memory reset**
User program/data (Load memory)	X	X	X
• Retentive response of the DBs for CPU 31xC, 312, 314, 315-2 DP	X	X	–
• Retentive response of the DBs for CPU 317-2 DP	Can be set in the properties of the DBs in STEP, V5.2 + SP1.		–
flag bits, timers and counters configured as retentive data	X	X	–
diagnostics buffer, operating hour counter	X	X	X
MPI address, transmission rate (or DP address, baud rate of the CPU 317-2 DP MPI/DP interface if this configured as a DP station).	X	X	X

x = retentive; - = not retentive

Retentive response of a DBs for CPU 31xC, 312, 314 and 315-2 DP

A data block (DB) is always saved to the MMC at POWER OFF. At POWER ON, the most recent actual values of the DB are copied from the MMC back into the CPU RAM.

The contents of the DBs are always retentive at POWER ON or STOP-RUN for CPU 31xC, 312, 314 and 315-2 DP .

Retentive response of a DB for CPU 317-2 DP

For CPU 317-2 DP you can specify in STEP 7 (beginning with version 5.1 + SP 1) or using SFC 82 “CREA_DBL“ (parameter ATTRIB -> Bit NON_RETAIN) if a DB at POWER ON/OFF or RUN-STOP

- keeps the actual values (retentive DB) or
- takes the start values from the load memory (non-retentive DB)

Table 4-2 Retentive response of the DBs for CPU 317-2 DP

At POWER ON/OFF or a restart (warm start) of the CPU, the DB should	
Get the start values (non-retentive DB)	**Keep the actual values (retentive DB)**
Background: At POWER ON/OFF and restart (STOP-RUN) of the CPU, the actual values of the DB are non-retentive. The DB gets the start values from the load memory.	Background: At POWER OFF/ON and restart (STOP-RUN) of the CPU, the actual values of the DB are maintained.
Requirement in STEP 7: • The "Non-retain“ check box must be activated in the block properties of the DB or • a non-retentive DB has been generated with SFC 82 “CREA_DBL“ and the corresponding block attribute (ATTRIB -> Bit NON_RETAIN).	Requirement in STEP 7: • The "Non-retain“ check box must be deactivated in the block properties of the DB or • a retentive DB has been generated with SFC 82.

Note

Not that for CPU 317-2 DP, only 256 Kbytes of RAM are for retentive data blocks. The remainder of the RAM is used by code blocks and non-retentive data blocks.

4.2 Memory functions

Introduction

Memory functions are used to generate, modify or delete entire user programs or specific blocks. You can also ensure that your data is retained by archiving your own project data.

General: Basics of downloading a user program via PG/ PC

All user program data is downloaded from your PG/PC to the CPU via MMC.

Blocks use the load memory area as specified under "Load memory requirements" in "General block properties".

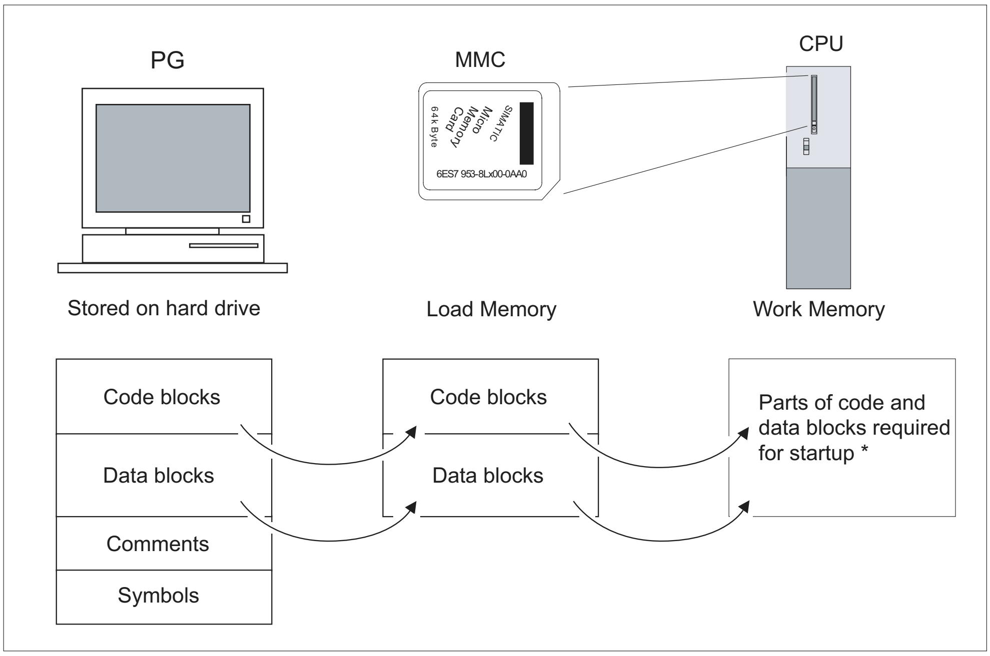


Figure 4-2 Load memory and RAM

* If the RAM is not completely retentive, the retentive portion of the RAM is displayed as retentive memory in the STEP 7 module status (as with CPU 317-2 DP).

You cannot run the program until all the blocks have downloaded.

Note

This function is only permitted when the CPU is in STOP mode.
Load memory is empty if this load operation could not be interrupted due to power loss or illegal block data.

Downloading a user program from the PG/ PC to the MMC

Case A: Download of a new user program

You have created a new user program. Download the complete program from your PG/PC to the MMC.

Case B: Download of additional blocks

You have already created a user program and downloaded it to the MMC (Case A). You then want to add function blocks to the program. In this case, you do not need to reload the entire user program to the MMC. Rather, you can download only the new blocks to the MMC (this procedure reduces the time required to download highly complex programs).

Case C: Overwriting with downloaded data

In this case, you modify blocks in your user program. In the next step, you download and overwrite the user program or only the modified blocks to the MMC, using the PG/PC.

Warning

When you download and overwrite blocks/a user program, all data stored under the same name on the MMC are lost.

After a block is loaded, data of runtime relevant blocks is transferred to memory and activated.

Deleting blocks

When you delete a block, it is deleted from load memory. In *STEP 7* you can also delete a block via the user program (DBs also with SFC 23 "DEL_DB").

RAM used by this block is released.

Upload

Contrary to download operations, upload is referred to as the upload of specific blocks or of a complete user program **from the CPU to the PG/PC**. The blocks have the content last loaded in the MMC. Runtime data blocks represent an exception to this; the actual values are sent to them.

In *STEP 7*, an upload of blocks or of the user program from the CPU does not influence the CPU's memory allocation.

Compression

When data are compressed, gaps which have developed between memory objects in load memory/work memory as a result of load/delete operations will be eliminated. thus reorganizing free memory area in a continuous block.

Data can be compressed while the CPU is in STOP or RUN mode.

Copying RAM to ROM

When copying the RAM content to ROM, the actual values of the DBs are transferred from RAM to load memory to form the start values for the DBs.

Note

This function is only permitted when the CPU is in STOP mode.

There will subsequently be no data in load memory if this operation is interrupted by power failure.

Memory reset

After the insertion/removal of a Micro Memory Card, a CPU memory reset establishes defined conditions for CPU restart (warm start).

Memory reset rebuilds the CPU's memory management. Blocks in load memory are retentive. All runtime-related blocks are transferred again from load memory to RAM. The effect of this operation, in particular, is to initialize the data blocks in RAM (i.e. resets them to their initial values).

Memory reset and the corresponding peculiarities are described in the S7-300 Installation Manual, Chapter *CPU Memory Reset*.

Restart (warm start)

- All retentive DBs maintain their actual values (non-retentive DBs are also supported with CPU 317-2 DP). Non-retentive DBs get back their start values).
- The values of all retentive M, C, T are maintained.
- All non-retentive user data is initialized:
  - M, C, T, I, O with "0"
- All tasks are initialized.
- The process images are deleted.

4.3 Address areas

Overview

S7 CPU system memory is split into address areas (refer to the table below). Using corresponding operations, address data in the user program directly in the respective address area.

Table 4-3 Address areas of system memory

Address areas	Description
Process image of the inputs	At the start of every OB 1 cycle, the CPU reads the values at the input of the input modules and saves them the process image of the inputs.
Output Process Image	During its cycle, the program calculates the values for the outputs and writes them to the process image of the outputs. At the end of the OB1 cycle, the CPU writes the calculated output values to the output modules.
flag bits	This area provides memory for saving the intermediate results of a program calculation.
Timers	Timers are available in this area.
Counters	Counters are available in this area.
Local data	Temporary data of a code block (OB, FB, FC) are saved to this memory area for the time the respective block is being edited.
Data blocks	Refer to Chapter *Handling of DB data*

Cross-reference

The address areas that are available on your CPU are listed in the *Instruction list for CPUs 31xCand 31x*.

I/O process image

When the user program addresses the Input (I) and Output (O) address areas, it not query the signal states of digital signal modules. Instead, it rather accesses a memory area in CPU system memory. This memory area is referred to as process image.

The process image is split into two sections: Process image of the inputs and the process image of the outputs.

Advantages of the process image

Process image access, compared to direct I/O access, offers the advantage that a consistent image of process signals is made available to the CPU during cyclic program execution. When the signal status at an input module changes during program execution, the signal status in the process image is maintained until the image is updated in the next cycle. Moreover, since the process image is stored in CPU system memory, access is significantly faster than direct access to the signal modules.

Process image update

The operating system updates the process image periodically. The figure below shows the sequence of this operation within a cycle.

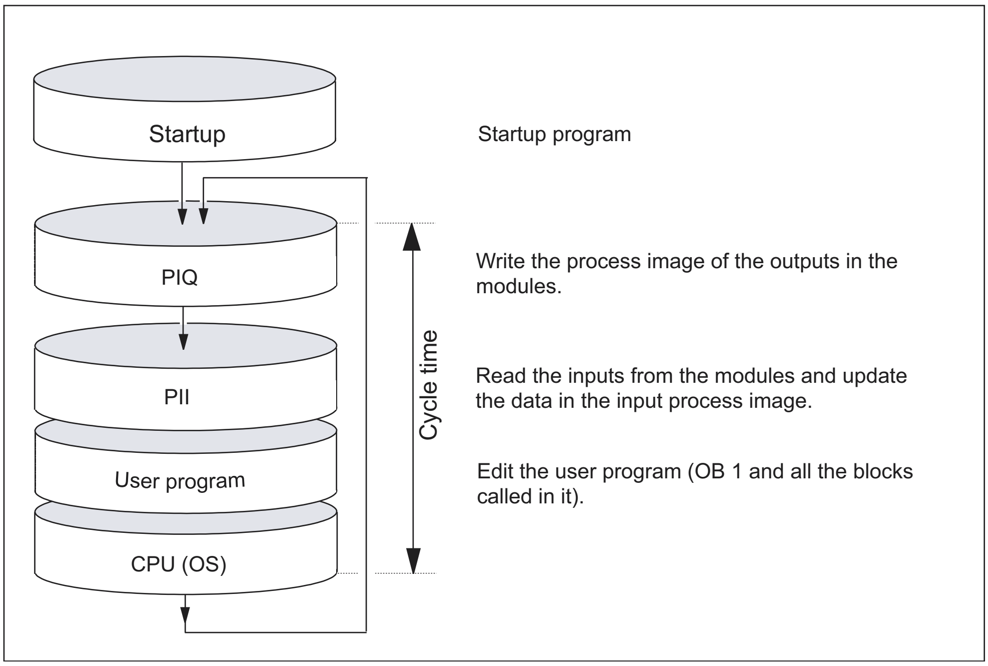


Figure 4-3 Sequence of operation within a cycle

Local data

Local data contains:

- the temporary variables of code blocks
- the start information of the OBs
- transfer parameters
- intermediate results

Temporary Variables

When you create blocks, you can declare temporary variables (TEMP) which are only available during block execution and then overwritten again. These local data have a fixed length per OB. Local data must be initialized prior to the first read access. Each OB also requires 20 bytes of local data for its start information. Local data access is faster than access to the data in DBs.

The CPU is equipped with memory for storing temporary variables (local data) of currently executed blocks. The size of this memory area depends on the CPU. It is distributed in partitions of equal size to the priority classes. Every priority class has its own local data area.

Caution

All temporary variables (TEMP) of an OB and its subordinate blocks are stored in local data. If you use multiple nesting levels for block processing, you may cause an overflow in the local data area.
The CPUs will change to STOP mode if you exceed the permitted length of local data for a priority class.
Take local data volume required for synchronous error OBs into account; this is assigned to the respective priority class.

4.4 Handling of DB data

4.4.1 Recipes

Introduction

A recipe represents a collection of user data.

You can implement a simple recipe concept using DBs which are not linked to runtime. In this case, the recipes should have the same structure (length). One DB should exist per recipe.

Processing sequence

Recipes should be stored in load memory:

- in *STEP 7*, the specific records of recipes are generated as non-runtime DBs, and are then downloaded to the CPU. Therefore, recipes utilize load memory, rather than RAM.

Working with recipe data:

- SFC 83 "READ_DBL" is called from the user program to copy the record for the current recipe from the DB in load memory to a runtime-related DB in RAM. This has the effect that work memory only needs to receive the data volume of one data record.

  The user program can now access data of the current recipe.

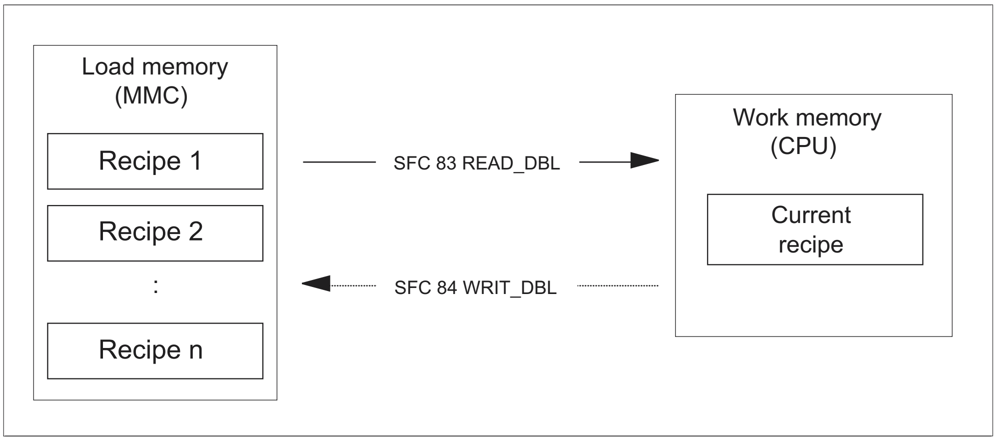


Figure 4-4 Handling of recipe data

Saving a changed recipe:

- New or changed recipe records generated during program processing can be transferred to load memory. To do this, call SFC 84 "WRIT_DBL" in the user program.

  These data which were written to load memory are portable, and are also retentive on memory reset.

  If you want to backup modified records (recipes) on a PG/PC, you can upload and save them in a single block.

Note

The active system functions SFC82 to 84 (current accesses to the MMC) have a distinct influence on PG functions (e.g. block status, variable status, load block, upload, open).

They typically reduce performance (compared to inactive system functions) by the factor 10.

Note

As a precaution against data loss, always make sure that the maximum number of delete/write operations is not exceeded. Also refer to the SIMATIC Micro Memory Card (MMC) section in the "Structure and Communication Connections of a CPU" chapter.

Caution

Data on a SIMATIC Micro Memory Card can be corrupted if you remove the card during write access. In this case you might have to insert the MMC memory in your PG to delete it, or you format the card in the CPU.

Never remove an MMC in RUN mode. Always remove when power is off or when the CPU is in STOP state and when no PG performs a write access the card. Disconnect the communication lines if you cannot safely exclude active write access functions from the PG (e.g. load/delete function block).

4.4.2 Measurement value archives

Introduction

Measurement values are generated when the CPU executes the user program. These values are to be evaluated and archived.

Processing sequence

Acquisition of measurement values:

- The CPU writes measured values to a DB (for alternating backup mode in several DBs) which is located in RAM.

Archiving measurement values:

- You can call SFC 84 "WRIT_DBL" in the user program to swap measured values stored in the DB to load memory, before the data volume can exceed main memory capacity.

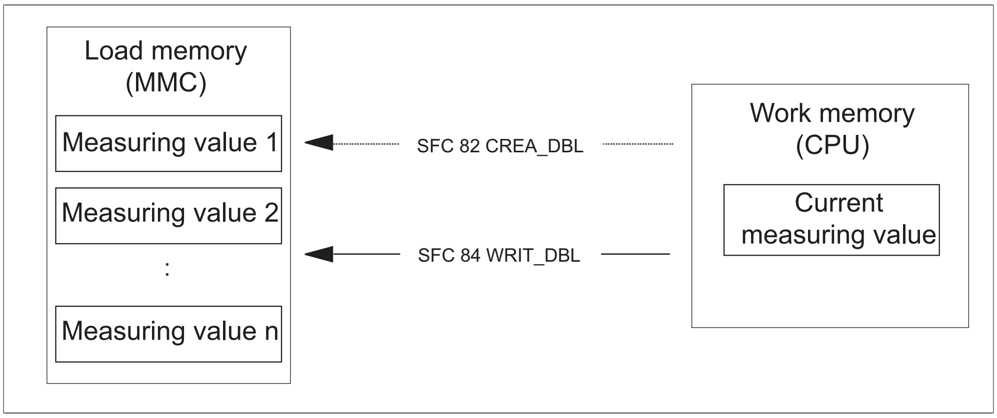


Figure 4-5 Handling of measurement value archives

- You can call SFC 82 "CREA_DBL" in the user program to generate new (additional) DBs in load memory which are not linked to runtime and do not require RAM space.

Cross-reference

The *System Software for S7-300/400* Reference Manual*, System and Standard Functions* or the STEP 7 Online Help all contain further information about the SFC 82 block.

Note

SFC 82 is terminated and an error message is generated if a DB already exists under the same number in load memory and/or work memory.

These data which were written to load memory are portable, and are also retentive on memory reset.

Evaluation of measurement values:

- Measurement value DBs saved to load memory can be uploaded and evaluated by other communication partners (e.g. PG, PC, ...).

Note

The active system functions SFC82 to 84 (current accesses to the MMC) have a distinct influence on PG functions (e.g. block status, variable status, load block, upload, open).

They typically reduce performance (compared to inactive system functions) by the factor 10.

Note

For CPU 317-2 DP, non-retentive DBs can also be generated using SFC 82 (parameter ATTRIB -> Bit NON_RETAIN).

To prevent loss of data, always make sure that you do not exceed the maximum number of delete/write cycles. See also the SIMATIC Micro Memory Card (MMC) section in the "Structure and Communication Functions of a CPUs 31xC" chapter.

Caution

Data on a SIMATIC Micro Memory Card can be corrupted if you remove the card during write access. In this case you might have to insert the MMC memory in your PG to delete it, or you format the card in the CPU.

Never remove an MMC in RUN mode. Always remove when power is off or when the CPU is in STOP state and when no PG performs a write access the card. Disconnect the communication lines if you cannot safely exclude active write access functions from the PG (e.g. load/delete function block).

4.5 Saving/retrieving complete projects to/from Micro Memory Card

Function mode of operation

Using the **Save project to Memory Card** and **Fetch project from Memory Card** functions, you can save all project data to a SIMATIC Micro Memory Card for future retrieval. For this operation, the SIMATIC Micro Memory Card can be located in a CPU or in the MMC programming device of a PG or PC.

Project data is compressed before they are saved to a SIMATIC Micro Memory Card, and uncompressed on retrieval.

Note

You may also have to store your user data on the micro memory card, in addition to just the project data. You should therefore check in advance whether your chosen MMC has sufficient memory.

A message will indicate if your MMC is running out of memory.

The volume of project data to be saved corresponds with the size of the project's archive file.

Note

For technical reasons, you can only transfer the entire contents (user program and project data) using the **Save project to memory card** action.

Handling the Functions

How you use the **Save project to memory card** / **Retrieve project from memory card** functions depends on the location of the SIMATIC micro memory card:

- If the micro memory card is inserted in the MMC slot, select a project level that is uniquely assigned to the CPU from the SIMATIC Manager project window (e.g. CPU, program, source or blocks). Select the **Target system > Save project to memory card** or **Target system > Retrieve project from memory card** menu command. All project data is written to the MMC, or retrieved from the card.
- If project data is not available on the currently used programming device (PG/PC), you can select the source CPU via "Available nodes" window. Select menu command **PLC > Show available nodes** to open the "Available nodes" window. Select the connection/CPU that contains your project data on Micro Memory Card. Now select the menu item **Retrieve project from Memory Card**.
- If the Micro Memory Card is in the MMC programming slot of a PG or PC, you can open the "S7-Memory Card window" via the menu command **File > S7-Memory Card > Open**. Select the **Target system > Save project to memory card** or **Target system > Retrieve project from memory card** menu command. to open a dialog in which you can select the source or target project.

Note

Project data may generate a high volume of data. Especially in RUN mode and during read/write access to the CPU, this can lead to waiting periods of several minutes.

Sample application

Once you have more than one member of service and maintenance staff occupied with a maintenance or service task on a SIMATIC PLC, it may be difficult to make current project data quickly available to each staff member.

However, if these staff members have access to project data that is available locally on a serviced CPU, they can make their changes and quickly release the updated version to other staff members.

Cycle and response times

5

5.1 Overview

Overview

This chapter contains detailed information about the following topics:

- Cycle time
- Response rime
- Interrupt response time
- Sample calculations

Reference: Cycle Time

You can read the cycle time of your user program with you programming device. You will find more information in the *STEP 7Online Help or* in the manual *Configuring Hardware and Communication Connections - STEP 7*

Reference: Processing time

More information can be found in the *S7-300 Instruction List for CPUs 31xC* and 31x, which is a spreadsheet containing the run times for all

- *STEP 7* instructions the respective CPU can process,
- SFCs/SFBs integrated in the CPUs,
- IEC functions which can be called in *STEP 7*.

5.2 Cycle Time

5.2.1 Overview

Introduction

This section explains what we mean by the term "cycle time", what this consists of and how you can calculate it.

What do we mean by "cycle time"?

The cycle time represents the time the operating system requires for processing one program cycle, that is, one OB 1 cycle, including all program sections and system activities that interrupt this cycle.

This time is monitored.

Time sharing model

Cyclic program processing, and therefore user program execution, is carried out in time shares. To clarify these processes, let us assume that every time share has a length of precisely 1 ms.

Process image

During cyclic program processing, the CPU requires a consistent image of the process signals. This is ensured by reading/writing the process signals prior to program processing. Subsequently, during program execution and when addressing input (I) and output (Q) address areas, the CPU does not directly access the signal modules, but rather accesses the system memory area which contains the I/O process image.

Sequence of cyclic program processing

The table and figure below show the phases of cyclic program processing.

Table 5-1 Cyclical program processing

Step	Sequence
1	The operating system initiates cycle time monitoring.
2	The CPU writes the values of the output process image to the output modules.
3	The CPU reads the status at the inputs of the input modules and then updates the process image of the inputs.
4	The CPU processes the user program in time shares and executes program instructions.
5	At the end of a cycle the operating system executes queued tasks, e.g. it loads and deletes blocks.
6	The CPU then returns to the start of the cycle and restarts cycle time monitoring.

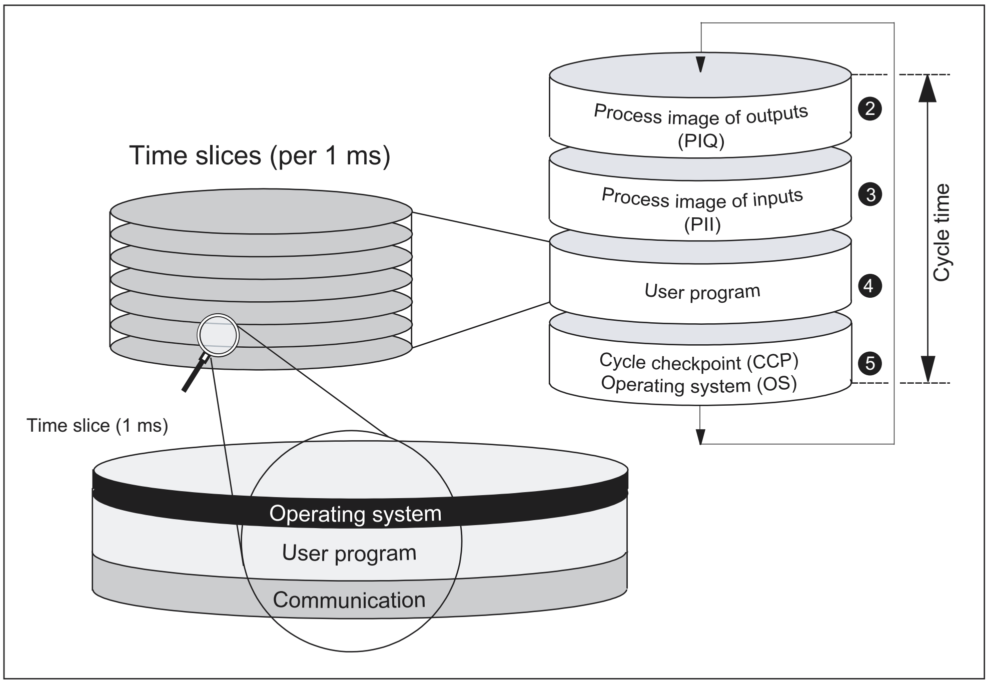


Figure 5-1 Time-sharing model

In contrast to the S7-400 CPUs (and the CPU 318-2 DP), with the S7-300 CPUs the data is accessed with an OP/TP (control and monitoring functions) only at the scan cycle checkpoint (see the specifications chapter for data consistency). Processing of the user program is not interrupted by the control and monitoring functions.

Extension of the Cycle Time

Always take into consideration that the cycle time of a user program is extended by:

- Time-controlled interrupt handling
- Process interrupt handling (also refer to Chapter *Interrupt response time*)
- Diagnostics and Error Handling
- Communication with programming devices (PGs), operator panels (OPs) and via connected CPs (e.g. Ethernet, PROFIBUS-DP)
- Testing and commissioning routines, e.g. status/controlling of variables or block status functions.
- Transfer and deletion of blocks, compressing user program memory
- Writing/reading the MMC, using SFC 82 to 84 in the user program

5.2.2 Calculating the cycle time

Introduction

The cycle time is made up of following influencing factors.

Process image update

The table below shows the time a CPU requires to update the process image (process image transfer time). The times specified might be prolonged by interrupts or by communication of the CPU.

The process image transfer time is calculated as follows:

Table 5-2 Formula for calculating the process image (PI) transfer time

The transfer time of the process image is calculated as follows:	
Base load K	+ Number of bytes in the PI in rack 0 x (A)
	+ Number of bytes in the PI in rack 1 to 3 x (B)
	+ Number of bytes in the PI via DP x (D)
	= Transfer time for the process image

Table 5-3 CPU 31xC: Data for calculating the process image transfer time

Const.	Components	CPU 312C	CPU 313C	CPU 313C-2 DP	CPU 313C-2 PtP	CPU 314C-2 DP	CPU 314C-2 PtP
K	Base load	150 µs	100 µs	100 µs		100 µs	
A	per byte in module rack 0	37 µs	35 µs	37 µs		37 µs	
B	per byte in racks 1 to 3 *	-	43 µs	47 µs		47 µs	
D (DP only)	per WORD in the DP area for the integrated DP interface	-	-	1 µs	-	1 µs	-

- + 60 µs per rack

Table 5-4 CPU 31x: Data for calculating the process image transfer time

Const.	Components	CPU 312	CPU 314	CPU 315-2 DP	CPU 317-2 DP
K	Base load	150 µs	100 µs	100 µs	50 µs
A	per byte in module rack 0	37 µs	35 µs	37 µs	15 µs
B	per byte in racks 1 to 3 *	-	43 µs	47 µs	25 µs
D (DP only)	per WORD in the DP area for the integrated DP interface	-	-	1 µs	1 µs

* + 60 µs per rack

Extending the user program processing time

In addition to actually working through the user program, your CPU's operating system also runs a number of processes in parallel, such as timer management for the core operating system. These processes extend the processing time of the user program.

The table below lists the multiplication factors required to calculate your user program processing time.

Table 5-5 Extending the user program processing time

CPU	Factor
312C	1.06
313C	1.10
313C-2DP	1.10
313C-PtP	1.06
314C-2DP	1.10
314C-2PtP	1.09
312	1.06
314	1.10
315-2 DP	1.10
317-2 DP	1.07

Operating system processing time at the scan cycle checkpoint

The table below shows the operating system processing time at the scan cycle checkpoint of the CPUs. These times are calculated without taking into consideration times for:

- Testing and commissioning routines, e.g. status/controlling of variables or block status functions
- Transfer and deletion of blocks, compressing user program memory
- Communications
- Read/write access to the MMC, using SFC82 to 84

Table 5-6 Operating system processing time at the scan cycle checkpoint

CPU	Cycle control at the cycle control point (CCP)
312C	500 µs
313C	500 µs
313C-2	500 µs
314C-2	500 µs
312	500 µs
314	500 µs
315-2	500 µs
317-2 DP	150 µs

Extended cycle times as a result of errors and nested interrupts

Enabled interrupts also extend cycle time. Details are found in the table below.

Table 5-7 Extended cycle time due to nested interrupts

Interrupt type	Process interrupt	Diagnostic interrupt	Time of day interrupt	Delay interrupt	Watchdog Interrupt
312C	700 µs	700 µs	600 µs	400 µs	250 µs
313C	500 µs	600 µs	400 µs	300 µs	150 µs
313C-2	500 µs	600 µs	400 µs	300 µs	150 µs
314C-2	500 µs	600 µs	400 µs	300 µs	150 µs
312	700 µs	700 µs	600 µs	400 µs	250 µs
314	500 µs	600 µs	400 µs	300 µs	150 µs
315-2	500 µs	600 µs	400 µs	300 µs	150 µs
317-2 DP	190 µs	240 µs	200 µs	150 µs	90 µs

The program runtime at interrupt level must be added to this time extension.

Table 5-8 Cycle time extension as a result of errors

Type of error	Programming errors	I/O access error
312C	600 µs	600 µs
313C	400 µs	400 µs
313C2	400 µs	400 µs
314C-2	400 µs	400 µs
312	600 µs	600 µs
314	400 µs	400 µs
315-2 DP	400 µs	400 µs
317-2 DP	100 µs	100 µs

The interrupt OB processing time must be added to this extended time.

The times required for multiple nested interrupt/error OBs are added accordingly.

see also

Calculating method for calculating the cycle/response time.

Different cycle times.

Overview

The cycle time (T_{cyc}) length is not the same in every cycle. The following illustration show different cycle times, T_{cyc1} and T_{cyc2}. T_{cyc2} is greater than T_{cyc1} because the cyclically process OB 1 is interrupted by a time of day interrupt OB (OB 10 in this case).

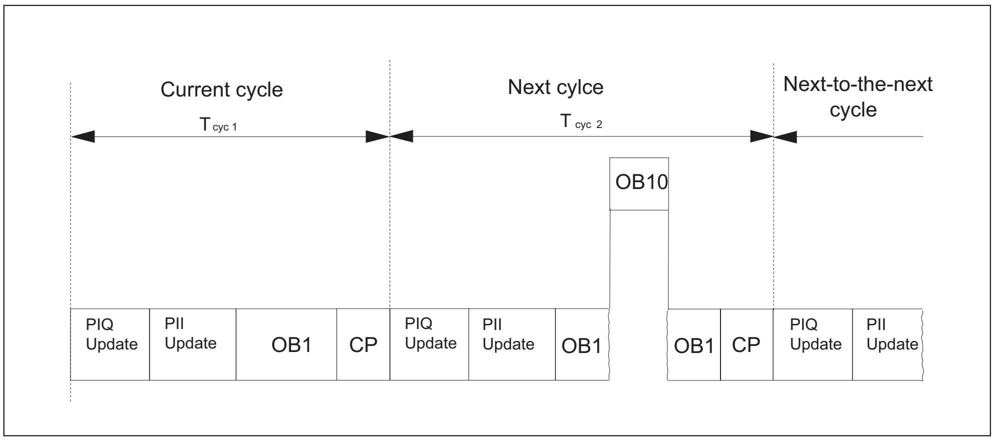


Figure 5-2 Different cycle times

Block processing times may fluctuate

Fluctuation of the block processing time (e.g. OB 1) may also be a factor causing cycle time fluctuation, due to:

- conditional instructions,
- conditional block calls,
- different program paths,
- loops etc.

Maximum cycle time

In *STEP 7* you can modify the default maximum cycle time. OB80 is called on when this time expires. In this block you can specify the CPU's response to this timeout error.

The CPU switches to STOP mode if OB80 does not exist in its memory.

5.2.3 Communication load

Configured communication load (PG/OP communication)

The CPU operating system continuously provides a specified percentage of total CPU processing performance (Time-sharing technology) for communication tasks. Processing performance not required for communication is made available to other processes.

In HW Config, you can specify a communication load value between 5% and 50%. Default value is 20%.

You can use the following formula for calculating the cycle time extension factor:

100 / (100 – configured communication load in %)

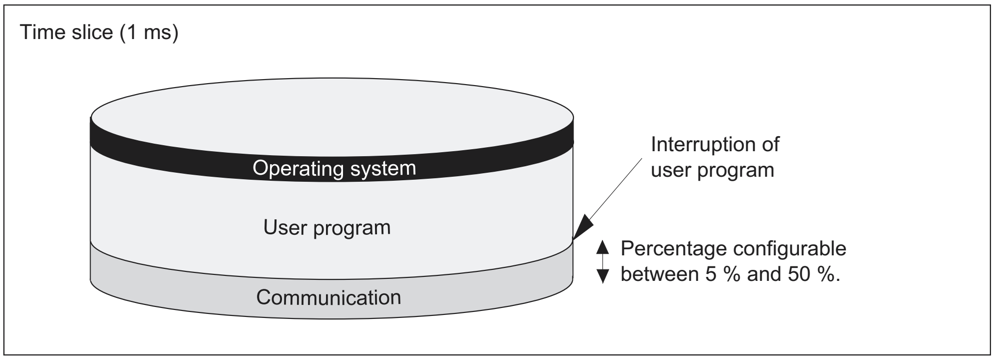


Figure 5-3 Splitting a time share

Example: 20% communication load

In your hardware configuration, you have specified a communication load of 20%.

The calculated cycle time is 10 ms.

Using the above formula, the cycle time is extended by the factor 1.25.

Example: 50% communication load

In your hardware configuration, you have specified a communication load of 50%.

The calculated cycle time is 10 ms.

Using the above formula, the cycle time is extended by the factor 2.

Physical cycle time depending on communication load

The figure below describes the non-linear dependency of the physical cycle time on communication load. In our sample we have chosen a cycle time of 10 ms.

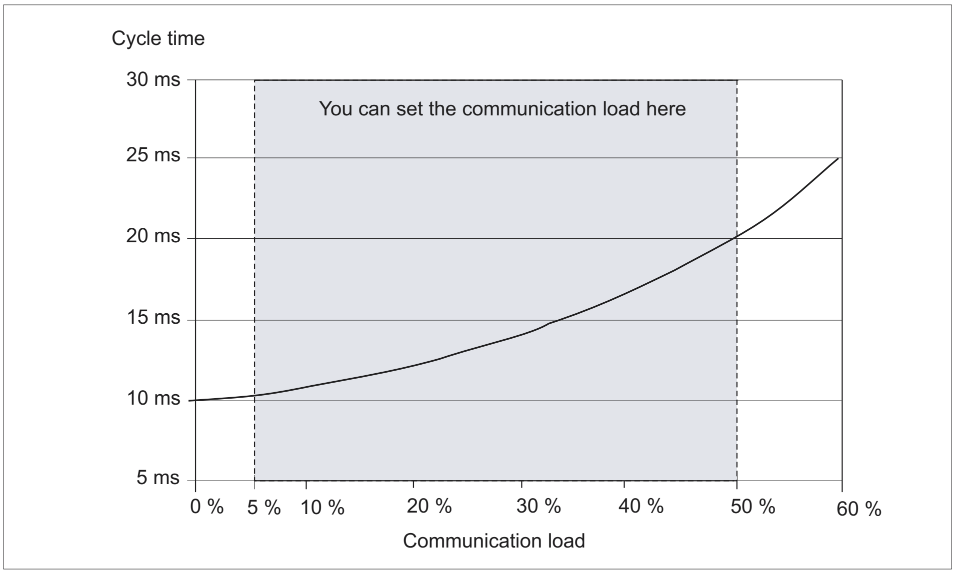


Figure 5-4 Cycle time depending on communication load

Influence on the physical cycle time

From the statistical viewpoint, asynchronous events - such as interrupts - occur more frequently within the OB1 cycle when the cycle time is extended as a result of communication load. This further extends the OB1 cycle. This extension depends on the number of events that occur per OB1 cycle and the time required to process these events.

Note

Change the value of the "communication load" parameter to check the effects on the cycle time at system runtime. You must consider the communication load when you set the maximum cycle time, otherwise timing errors can occur.

Tips

- Use the default setting wherever possible.
- Increase this value only if the CPU is used primarily for communications and if the user program is not time critical.
- In all other situations you should only reduce this value.

5.2.4 Cycle time extension as a result of testing and commissioning functions

Runtimes

The runtimes of the testing and commissioning functions are operating system runtimes, so they are the same for every CPU. Initially, there is no difference between process mode and testing mode.

How the cycle time is extended as a result of active testing and commissioning functions is shown in the table below.

Table 5-9 Cycle time extension as a result of testing and commissioning functions

Function	CPU 31xC/ CPU 31x
Status variable	50 µs for each variable
Control variable	50 µs for each variable
Status block	200 µs for each monitored line

Configuration during parameter assignment

In **process mode**, the maximum permitted communication load by is not only set in "Communication load". It is also determined by "Process mode: maximum permitted cycle time extension due to testing functions". Thus, the configured time is monitored absolutely in process mode and data acquisition is stopped if a timeout occurs. This is how *STEP 7* stops data requests in loops before a loop ends, for example.

When running in **Testing mode**, the complete loop is executed in every cycle. This can significantly increase cycle time.

5.3 Response Time

5.3.1 Overview

Definition of response time

The response time is the time between the detection of an input signal and the change of a linked output signal.

Fluctuation width

The actual response time lies between a shortest and a longest response time. You must always reckon with the longest response time when configuring your system.

The shortest and longest response times are shown below, to give you an idea of the fluctuation width of the response time.

Factors

The response time depends on the cycle time and following factors:

- Delay of the inputs and outputs of signal modules or integrated I/O.
- Additional DP cycle times in a PROFIBUS-DP network (only with CPUs 31xC-2 DP)
- Execution in the user program

You can find the delay times ...

- in the specifications of the signal modules (Reference Manual *Module data*)
- for integrated I/Os in *Specifications of integrated I/O*

DP cycle times in a PROFIBUS-DP network

if you have configured your PROFIBUS-DP network in *STEP 7* , *STEP 7* calculates the typical DP cycle time to be expected. You can then view the DP cycle time of your configuration on the PG.

The figure below gives you an overview of the DP cycle time. In this example, let us assume that the data of each DP slave has an average length of 4 bytes.

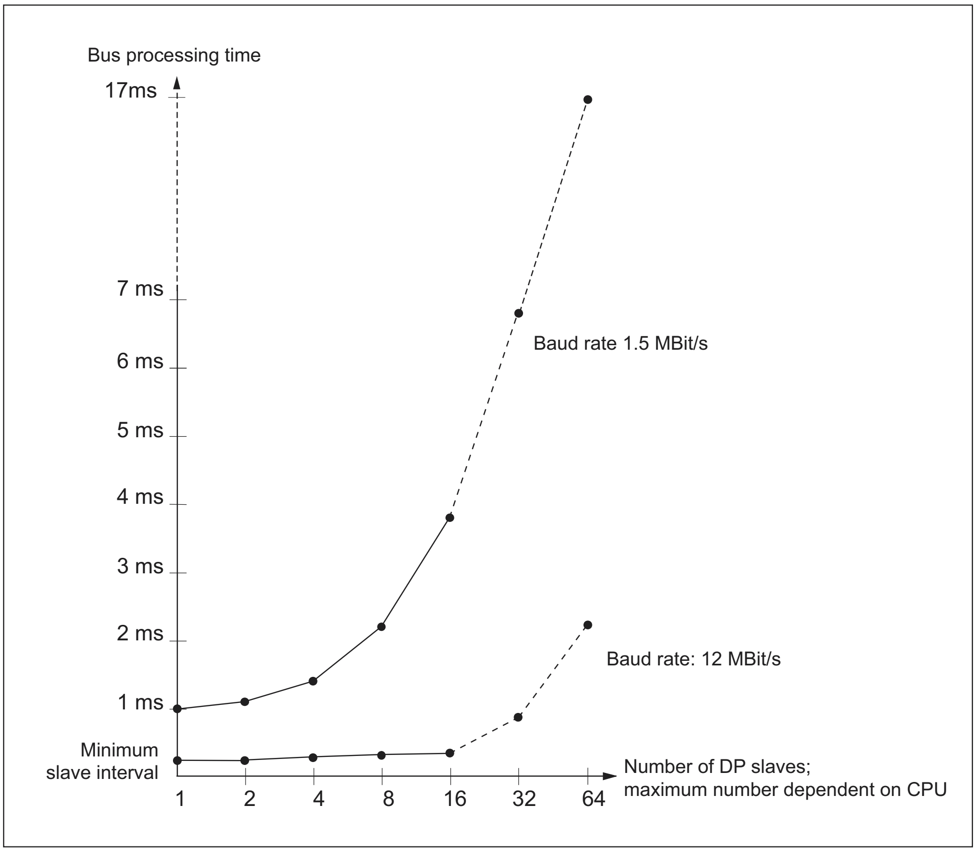


Figure 5-5 DP cycle times in a PROFIBUS-DP network

With multi-master operation on a PROFIBUS-DP network, you must consider the DP cycle time for each individual master. That is, you will have to calculate the times for each master separately and then add up the results.

see also

Longest response time

Shortest response time

5.3.2 Shortest response time

Conditions for shortest response time

The figure below shows you the conditions under which the shortest response time is reached.

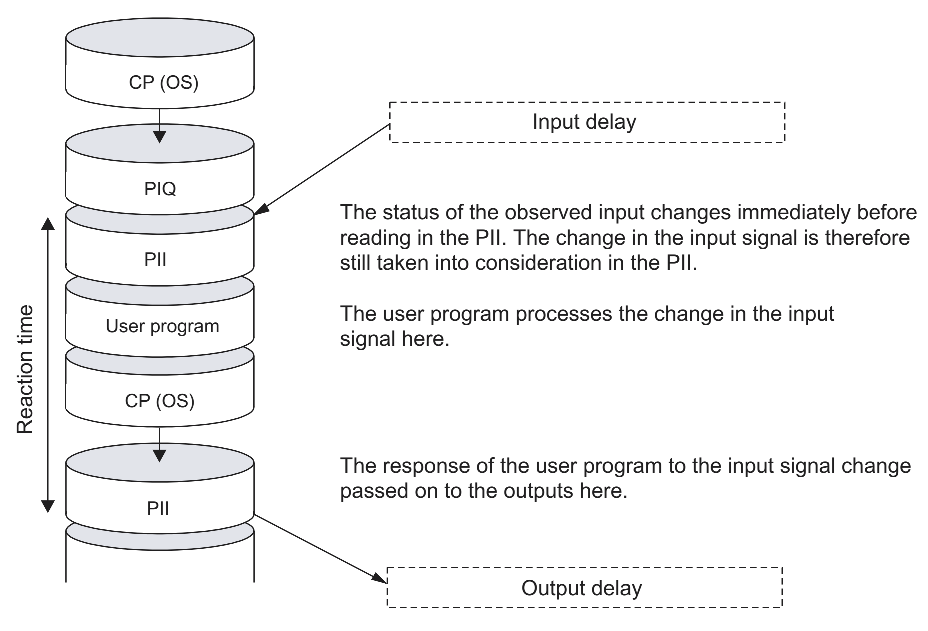


Figure 5-6 Shortest response time

Calculation

The (shortest) response time is the sum of:

- 1 x process image transfer time for the inputs +
- 1 x process image transfer time for the outputs +
- 1 x program processing time +
- 1 × operating system processing time at the SCC +
- I/O delay

The result is equivalent to the sum of the cycle time plus the I/O delay times.

see also

Calculating method for calculating the cycle/response time.

Reducing the response time with direct I/O access.

The times required for multiple nested interrupt/error OBs are added accordingly.

5.3.3 Longest response time

Conditions for the longest response time

The figure below shows the conditions under which the longest response time is reached.

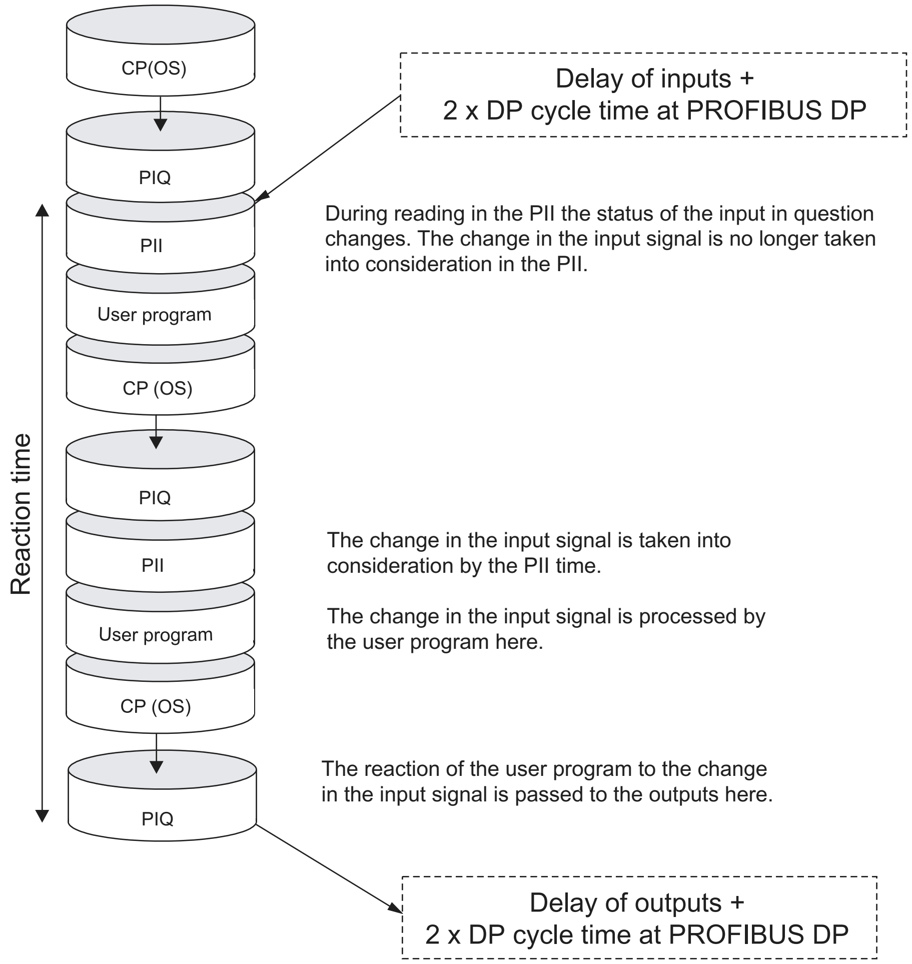


Figure 5-7 Longest response time

Calculation

The (longest) response time is the sum of:

- 2 x process image transfer time for the inputs +
- 2 x process image transfer time for the outputs +
- 2 x operating system processing time +
- 2 x program processing time +
- 4 x the runtime of DP Slave message frames (includes processing in the DP Master) +
- I/O delay

The result is equivalent to twice the cycle time + input and output delay + twice the bus runtime.

see also

Calculating method for calculating the cycle/response time.

Reducing the response time with direct I/O access

5.3.4 Reducing the response time with direct I/O access

Reducing the response time

You can reach faster response times with direct access to the I/O in your user program, for example with

- L PIB or
- T PQW

you can partially avoid the response times described above.

Note

You can also achieve fast response times by using process interrupts. Refer to the following chapters.

5.4 Calculating method for calculating the cycle/response time

Introduction

This chapter gives you an overview of how to calculate the cycle/response time.

All tables are found in Chapter *Calculating the cycle time*.

Cycle Time

1. Determine the user program runtime with the help of the *Instruction list*.
2. Multiply the calculated value by the CPU-specific factor from the table *Extension of user program processing time*.
3. Calculate and add the process image transfer time. Corresponding guide values are found in table *Data for calculating process image transfer time*.
4. Add the processing time at the scan cycle checkpoint. Corresponding guide values are found in the table *Operating system processing time at the scan cycle checkpoint*.
5. Include the extensions as a result of testing and commissioning functions in your calculation. These values can be found in the *Cycle time extension as a result of testing and commissioning functions* table*. The result is the*
6. **Cycle time**.

Extension of the cycle time as a result of interrupts and communication load

100 / (100 – configured communication load in %)

1. Multiply the cycle time by the factor as in the formula above.
2. Calculate the runtime of interrupt-processing program sections with the help of the instruction list. Add the corresponding value from Chapter *Calculating the Cycle Time*, Table *Extended cycle time as a result of nested interrupts.*
3. Multiply both values by the CPU-specific extension factor of the user program processing time (see Table 5-3).
4. Add the value of the interrupt-processing program sequences to the theoretical cycle time, multiplied by the number of triggering (or expected) interrupt events within the cycle time.

   The result is an approximation of the **physical cycle time**. Note down the result.

Response Time

Table 5-10 Calculating the response time

Shortest response time	Longest response time
-	Multiply the physical cycle time by factor 2.
Now add I/O delay.	Now add the I/O delay and the DP cycle times of the PROFIBUS-DP network.
The result is the shortest response time.	The result is the longest response time.

5.5 Interrupt response time

5.5.1 Overview

Definition of the interrupt response time

The interrupt response time is the time that expires between the first occurrence of an interrupt signal and the call of the first interrupt OB instruction. The following rule generally applies: Higher-priority interrupts are executed first. This means that the interrupt response time is increased by the program processing time of the higher-priority interrupt OBs and the interrupt OBs of equal priority which have not yet been executed (queued).

Calculation

The formula below show how you can calculate the minimum and maximum interrupt response times.

Table 5-11 Process and diagnostic interrupt response times

Calculation of the minimum and maximum interrupt reaction time	
Minimum interrupt reaction time of the CPU + Minimum interrupt reaction time of the signal modules + DP cycle time on the PROFIBUS DP = Quickest interrupt reaction time	Maximum interrupt reaction time of the CPU + Maximum interrupt reaction time of the signal modules + 2 x DP cycle time on the PROFIBUS DP The maximum interrupt reaction time is longer when the communication functions are active. The extra time is calculated with the following formula: **tv: 200 µs + 1000 µs x n%** Substantial longer time is possible when n = longer cycle due communication

Process/diagnostic interrupt response times of the CPUs

Table 5-12 Process and diagnostic interrupt response times

	Process interrupt response times			**Diagnostic interrupt response times**	
CPU	**external min.**	**external max.**	**Integrated I/O max.**	**Min.**	**Max.**
CPU 312	0.5 ms	0.8 ms	-	0.5 ms	1.0 ms
CPU 312C	0.5 ms	0.8 ms	0.6 ms	0.5 ms	1.0 ms
CPU 313C	0.4 ms	0.6 ms	0.5 ms	0.4 ms	1.0 ms
CPU 313C-2	0.4 ms	0.7 ms	0.5 ms	0.4 ms	1.0 ms
CPU 314	0.4 ms	0.7 ms	-	0.4 ms	1.0 ms
CPU 314C-2	0.4 ms	0.7 ms	0.5 ms	0.4 ms	1.0 ms
CPU 315-2 DP	0.4 ms	0.7 ms	-	0.4 ms	1.0 ms
CPU 317-2 DP	0.2 ms	0.3 ms	-	0.2 ms	0.3 ms

Signal modules

The process interrupt response time of signal modules is determined by following factors:

- Digital input modules

  Process interrupt response time = internal interrupt preparation time + input delay

  You will find these times in the data sheet for the respective digital input module.

- Analog input modules

  Process interrupt response time = internal interrupt preparation time + input delay

  The internal interrupt preparation time for analog input modules can be neglected. The conversion times can be found in the data sheet for the individual analog input modules.

The **Diagnostic interrupt response time** of signal modules is equivalent to the period that expires between the time a signal module detects a diagnostic event and the time this signal module triggers the diagnostic interrupt. This short time can be neglected.

Process interrupt processing

Process interrupt processing begins after process interrupt OB40 is called. Higher-priority interrupts stop process interrupt processing. Direct I/O access is executed during runtime of the instruction. After process interrupt processing has terminated, cyclic program execution continues or further interrupt OBs of equal or lower priority are called and processed.

5.5.2 Reproducibility of delay interrupts and watchdog interrupts

Definition of reproducibility

Delay interrupt:

The period that expires between the call of the first instruction in the interrupt OB and the programmed time of interrupt.

Watchdog interrupt:

The fluctuation width of the interval between two successive calls, measured between the respective initial instructions of the interrupt OBs.

Reproducibility

The following times apply for the CPUs described in this manual:

- Delay interrupt: +/- 200 µs
- Watchdog interrupt: +/- 200 µs

These times only apply if the interrupt can actually be executed at this time and if not interrupted, for example, by higher-priority interrupts or queued interrupts of equal priority.

5.6 Sample calculations

5.6.1 Example of cycle time calculation

Assembly

You have configured an S7shy300 and equipped it with following modules in rack "0":

- a CPU 314C-2
- 2 digital input modules SM 321; DI 32 x 24 VDC (4 bytes each in the PI)
- 2 digital output modules SM 322; DO 32 x 24 VDC/0.5 A (4 bytes each in the PI)

User program

According to the operations list your user program has a runtime of 5 ms. No communication is being performed.

Calculation of the cycle time

In this example, the cycle time is equivalent to the sum of following times:

- User program processing time:

  approx. 5 ms x CPU-specific factor 1.10 = approx. 5.5 ms
- Process image transfer time

  Process image of inputs: 100 µs + 8 bytes x 37 µs = approx. 0.4 ms

  Process image of outputs: 100 µs + 8 bytes x 37 µs = approx. 0.4 ms
- Operating system runtime at the scan cycle checkpoint:

  approx. 0.5 ms

Cycle time = 5.5 ms + 0.4 ms + 0.4 ms + 0.5 ms = 6.8 ms.

Calculating the physical cycle time

- There is no active communication.
- Interrupts are not processed.

Hence, **the physical cycle time** is 6 ms.

Calculating the longest response time

Longest response time

6.8 ms x 2 = 13.6 ms.

- I/O delay can be neglected.
- DP cycle times must not be taken into account, as all modules are inserted in rack 0.
- Interrupts are not processed.

5.6.2 Sample of response time calculation

Assembly

You have configured an S7shy300 and equipped it with following modules in two racks:

- a CPU 314C-2

  Configuring the cycle load as a result of communication: 40 %
- 4 digital input modules SM 321; DI 32 x 24 VDC (4 bytes each in the PI)
- 3 digital output modules SM 322; DO 16 x 24 VDC/0.5 A (2 bytes each in the PI)
- 2 analog input modules SM 331; AI 8 x 12-bit (not in the PI)
- 2 analog output modules SM 332; AO 4 x 12-bit (not in the PI)

User program

According to the instruction list, the user program runtime is 10.0 ms.

Calculating the cycle time

In this example, the cycle time is equivalent to the sum of following times:

- User program processing time:

  approx. 10 ms x CPU-specific factor 1.10 = approx. 11 ms
- Process image transfer time

  Process image of inputs: 100 µs + 16 bytes x 37 µs = approx. 0.7 ms

  Process image of outputs: 100 µs + 6 bytes x 37 µs = approx. 0.3 ms
- Operating system runtime at the scan cycle checkpoint:

  approx. 0.5 ms

The sum of the listed times is equivalent to the cycle time:

Cycle time = 11.0 ms + 0.7 ms + 0.3 ms + 0.5 ms = 12.5 ms.

Calculating the physical cycle time

Under consideration of communication load:

12.5 ms * 100 / (100-40) = 20.8 ms.

Thus, under consideration of time-sharing factors, the **actual cycle time** is **21 ms**.

Calculation of the longest response time

- Longest response time = 21 ms * 2 = 42 ms.
- I/O delay
  - The maximum delay of the input digital module SM 321; DI 32 x 24 VDC is **4.8 ms** per channel.
  - The output delay of the digital output module SM 322; DO 16 x 24 VDC/0.5 A **can be neglected**.
  - The analog input module SM 331; AI 8 x 12 bit was configured for an interference suppression at 50 Hz. The result is a conversion time of 22 ms per channel. Since 8 channels are active, the result is a cycle time of **176 ms** for the analog input module.
  - The analog output module SM 332; AO 4 x 12 bit was configured for a measurement range of 0 ... 10 V. The result is a conversion time of 0.8 ms per channel. Since 4 channels are active, this results in a cycle time of 3.2 ms. The settling time of 0.1 ms for a resistive load must be added to this. The result is an analog output response time of **3.3 ms**.
- DP cycle times can be neglected, as all modules are inserted in the CPU rack.
- Response times plus I/O delay:
  - **Case 1:** An output channel of the digital output module is set when a signal is received at the digital input. The result is a response time of:

    Response time = 42 ms + 4.8 ms = 46.8 ms.
  - **Case 2:** An analog value is fetched, and an analog value is output. The result is a response time of:

    Longest response time = 42 ms + 176 ms + 3.3 ms = 221.3 ms.

5.6.3 Example of interrupt response time calculation

Assembly

You have assembled an S7-300, consisting of one CPU 314C-2 and four digital modules in the CPU rack. One of the digital input modules is an SM 321; DI 16 x 24 VDC; with process/diagnostic interrupt function.

You have enabled only the process interrupt in your CPU and SM parameter configuration. You decided not to use time-controlled processing, diagnostics or error handling. You have configured a 20% communication load on the cycle.

You have configured a delay of 0.5 ms for the inputs of the DI module.

No activities are required at the scan cycle checkpoint.

Calculation

In this example, the process interrupt response time is based on following time factors:

- Process interrupt response time of CPU 314C-2: approx. 0.7 ms
- Extension by communication load according to the formula:

  200 µs + 1000 µs x 20 % = 400 µs = 0.4 ms
- Process interrupt response time of SM 321; DI 16 x 24 VDC:
  - Internal interrupt preparation time: 0.25 ms
  - Input delay: 0.5 ms
- Since the signal modules are inserted in the CPU rack, DP cycle times on the PROFIBUS-DP are irrelevant.

The process interrupt response time is equivalent to the sum of the listed time factors:

Process interrupt response time = 0.7 ms + 0.4 ms + 0.25 ms + 0.5 ms = **1.85** ms.

This calculated process interrupt response time expires between the time a signal is received at the digital input and the call of the first instruction in OB40.

Specifications

6

6.1 Height and depth of all CPUs

Every CPU has the same height and depth:

- Height: 125 mm
- Depth: 115 mm, or 180 mm with opened front cover.

The dimensions only differ in their width.

Width of CPU 31x

The following illustration shows the dimensions of CPU 312, 314 and 315-2 DP.

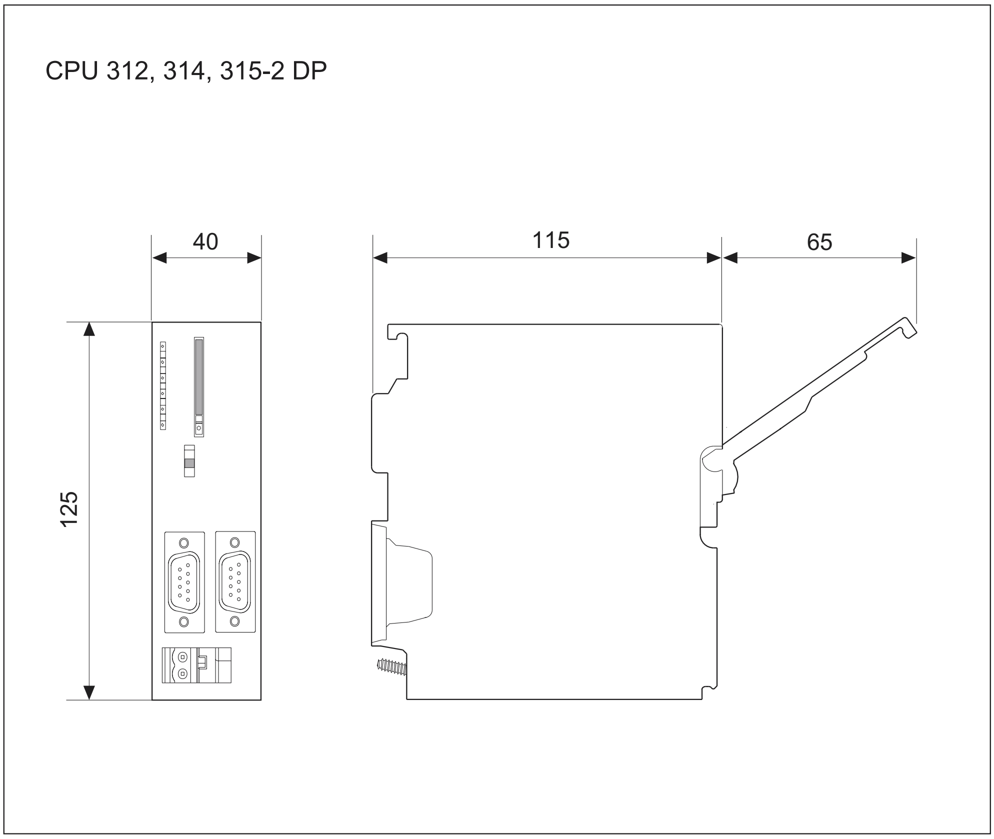


Figure 6-1 Dimensions of the CPUs

You can obtain the width of CPU 31xC or CPU 317-2 DP from the table below.

Width CPU 31xC and CPU 317-2 DP

CPU	Width
CPU 312C	80 mm
CPU 313C	120 mm
CPU 313C-2 PtP	120 mm
CPU 313C-2 DP	120 mm
CPU 314C-2 PtP	120 mm
CPU 314C-2 DP	120 mm
CPU 317-2 DP	80 mm

6.2 CPU 312

Specifications

Table 6-1 Specifications for the CPU 312

Specifications	
CPU and version	
Item number	6ES7312-1AD10-0AB0
• Hardware version	01
• Firmware version	V2.0.0
• Corresponding programming package	STEP 7, V 5.1 + SP 4 or later
Memory	
Work memory	
• Integrated	16 KB
• Expandable	No
Load memory	Plugged in with MMC (max. 4 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	ensured with MMC (maintenance-free)
Processing times	
Processing times for	
• Bit operation	Min. 0.2 µs
• Word instructions	Min. 0.4 µs
• Fixed-point arithmetic	Min. 5 µs
• Floating-point maths	Min. 6 µs
Timers/counters and their retentivity	
S7 counters	128
• Retentive memory	Configurable
• Default	from C0 to C7
• Counting range	0 to 999

Specifications	
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
S7 timers	128
• Retentive memory	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
Data areas and their retentivity	
flag bits	128 bytes
• Retentive memory	Yes
• Retentivity is default setting	MB0 to MB15
Clock memory bits	8 (1 byte per memory bit)
Data blocks	511 (DB 1 to DB 511)
• Size	16 KB
Local data per priority class	max. 256 bytes
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	max. 16 KB
Nesting depth	
• per priority class	8
• additional within an error OB	4
FBs	max. 512 (FB 0 to FB 511)
• Size	max. 16 KB
FCs	max. 512 (FC 0 to FC 511
• Size	max. 16 KB
Address areas (I/Os)	
Total I/O address area	1024 bytes /1024 bytes (can be freely addressed)
I/O process image	128 bytes/128 bytes
Digital channels	max. 256
of those local	max. 256
Analog channels	max. 64
of those local	max. 64

Specifications	
Assembly	
Module racks	max. 1
Modules per module rack	max. 8
Number of DP masters	
• Integrated	None
• via CP	1
Number of function modules and communication processors you can operate	
• FM	max. 8
• CP (PtP)	max. 8
• CP (LAN)	max. 4
Time-of-day	
Real-time clock	yes (SW clock)
• Buffered	No
• Accuracy	Deviation per day < 15 s
Operating hours counter	1
• Number	0
• Range of values	2^{31} (if SFC 101 is used)
• Granularity	1 hour
• Retentive	yes; must be manually restarted after every restart
Clock synchronization	Yes
• in the PLC	Master
• on MPI	Master/slave
S7 signaling functions	
Number of stations that can be logged on for signaling functions	6 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostic messages	Yes
• simultaneously enabled interrupt S blocks	max. 20
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number of variables	30
Of those as status variable	30
of those as control variable	14
Force	Yes
• Variable	Inputs, outputs
• Number of variables	max. 10
Status block	Yes
Single sequence	Yes

Specifications	
Breakpoint	2
Diagnostic buffer	Yes
- Number of entries (not configurable)	max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
- Number of GD circuits	4
- Number of GD packets	max. 4
Sending stations	max. 4
Receiving stations	max. 4
- Size of GD packets	max. 22 bytes
Consistent data	22 bytes
S7-based communication	Yes
- User data per job	max. 76 bytes
Consistent data	76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	
- as server	Yes
- User data per job	max. 180 bytes (with PUT/GET)
Consistent data	64 bytes
S5-compatible communication	Yes (via CP and loadable FCs)
Number of connections	max. 6
usable for	
- PG communication	max. 5
Reserved (Default)	1
Configurable	from 1 to 5
- OP communication	max. 5
Reserved (Default)	1
Configurable	from 1 to 5
- S7-based communication	
Reserved (Default)	2
Configurable	0 to 2
Routing	No
Interfaces	
1st interface	
Type of interface	integrated RS485 interface
Physics	RS485
electrically isolated	No
Interface current supply (15 to 30 V DC)	max. 200 mA

Specifications	
Functionality	
• MPI	Yes
• PROFIBUS-DP	No
• PtP communication	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	No
• Global data communication	Yes
• S7-based communication	Yes
• S7 communication	
as server	Yes
as Client	No
• Transmission rates	187.5 Kbps
Programming	
Programming language	LAD/FBD/STL
Available instructions	See the Instruction List
Nesting levels	8
System functions (SFCs)	See the Instruction List
System function blocks (SFBs)	See the Instruction List
User program security	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	40 x 125 x 130
Weight	270 g
Voltages, currents	
Power supply (nominal value)	24 VDC
• Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	normally 60 mA
Inrush current	normally 2.5 A
Power consumption (nominal value)	0.6A
I^2t	0.5 A^2s
External fusing of power supply lines (recommended)	min. 2 A
Power loss	normally 2.5 W

6.3 CPU 312C

Specifications

Table 6-2 Specifications for the CPU 312C

Specifications	
CPU and version	
Item number	6ES7 312-5BD01-0AB0
• Hardware version	01
• Firmware version	V2.0
• Corresponding programming package	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)
Memory	
Work memory	
• Integrated	16 KB
• Expandable	No
Load memory	Plugged in with MMC (max. 4 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	ensured with MMC (maintenance-free)
Processing times	
Processing times for	
• Bit operation	Min. 0.2 µs
• Word instructions	Min. 0.4 µs
• Fixed-point arithmetic	Min. 5 µs
• Floating-point maths	Min. 6 µs
Timers/counters and their retentivity	
S7 counters	128
• Retentive memory	Configurable
• Default	from C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by work memory size)
S7 timers	128
• Retentive memory	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB
• Number	unlimited (limited only by work memory size)

Specifications	
Data areas and their retentivity	
flag bits	128 bytes
• Retentive memory	Configurable
• Retentivity is default setting	MB0 to MB15
Clock memory bits	8 (1 byte per memory bit)
Data blocks	max. 511 (DB 1 to DB 511)
• Size	max. 16 KB
Local data per priority class	max. 256 bytes
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	max. 16 KB
Nesting depth	
• per priority class	8
• additional within an error OB	4
FBs	max. 512 (FB 0 to FB 511)
• Size	max. 16 KB
FCs	max. 512 (FC 0 to FC 511)
• Size	max. 16 KB
Address areas (I/Os)	
Total I/O address area	max. 1024 bytes/1024 bytes (can be freely addressed)
I/O process image	128 bytes/128 bytes
Digital channels	max. 256
• of those local	max. 256
• integrated channels	10 DI / 6 DO
Analog channels	max. 64
• of those local	max. 64
• integrated channels	None

Specifications	
Assembly	
Module racks	max. 1
Modules per module rack	max. 8
Number of DP masters	
• Integrated	None
• via CP	max. 1
Number of function modules and communication processors you can operate	
• FM	max. 8
• CP (PtP)	max. 8
• CP (LAN)	max. 4
Time-of-day	
Real-time clock	yes (SW clock)
• Buffered	No
• Accuracy	Deviation per day < 10 s
Operating hours counter	1
• Number	0
• Range of values	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	yes; must be manually restarted after every restart
Clock synchronization	Yes
• in the PLC	Master
• on MPI	Master/slave
S7 signaling functions	
Number of stations that can be logged on for signaling functions	max. 6 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostic messages	Yes
• simultaneously enabled interrupt S blocks	max. 20
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number of variables	max. 30
Of those as status variable	max. 30
of those as control variable	max. 14

Specifications	
Force	Yes
- Variable	Inputs, outputs
- Number of variables	max. 10
Status block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
- Number of entries (not configurable)	max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
- Number of GD circuits	4
- Number of GD packets	max. 4
Sending stations	max. 4
Receiving stations	max. 4
- Size of GD packets	max. 22 bytes
Consistent data	22 bytes
S7-based communication	Yes
- User data per job	max. 76 bytes
Consistent data	76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	
- as server	Yes
- User data per job	max. 180 bytes (with PUT/GET)
Consistent data	64 bytes
S5-compatible communication	Yes (via CP and loadable FCs)
Number of connections	max. 6
usable for	
- PG communication	max. 5
Reserved (Default)	1
Configurable	from 1 to 5
- OP communication	max. 5
Reserved (Default)	1
Configurable	from 1 to 5
- S7-based communication	max. 2
Reserved (Default)	2
Configurable	from 0 to 2
Routing	No

Specifications	
Interfaces	
1st interface	
Type of interface	integrated RS485 interface
Physics	RS485
electrically isolated	No
Interface current supply (15 to 30 V DC)	max. 200 mA
Functionality	
• MPI	Yes
• PROFIBUS-DP	No
• PtP communication	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	No
• Global data communication	Yes
• S7-based communication	Yes
• S7 communication	
as server	Yes
as Client	No
• Transmission rates	max. 187.5 Kbps
Programming	
Programming language	LAD/FBD/STL
Available instructions	See the Instruction List
Nesting levels	8
System functions (SFCs)	See the Instruction List
System function blocks (SFBs)	See the Instruction List
User program security	Yes
Integrated I/O	
• Default addresses of the integrated	
Digital inputs	124.0 to 125.1
Digital outputs	DO124.0 to DO124.5

Specifications	
Integrated functions	
Counters	2 Channels (see the Manual *Technological Functions*)
Frequency counters	2 channels, up to max. 10 kHz (see the Manual *Technological Functions*)
Pulse outputs	2 channels for pulse width modulation, up to max. 2.5 kHz (see the Manual *Technological Functions*)
Positioning control	No
Integrated "Controlling" SFB	No
Dimensions	
Mounting dimensions W x H x D (mm)	80 x 125 x 130
Weight	409 g
Voltages, currents	
Power supply (nominal value)	24V DC
• Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	typically 60 mA
Inrush current	typically 11 A
Power consumption (nominal value)	500 mA
I^2t	0.7 A^2s
External fusing of power supply lines (recommended)	LS switch Type C min. 2 A, LS switch Type B min. 4 A
Power loss	typically 6 W

Cross-reference

In Chapter *Specifications of the integrated I/O* you can find

- the specifications of integrated I/Os under *Digital inputs of CPUs 31xC* and *Digital outputs of CPUs 31xC*.
- the block diagrams of the integrated I/Os, under *Arrangement and usage of the integrated I/Os*.

6.4 CPU 313C

Specifications

Table 6-3 Specifications for the CPU 313C

Specifications	
CPU and version	
Item number	6ES7 313-5BE01-0AB0
• Hardware version	01
• Firmware version	V2.0.0
• Associated programming package	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)
Memory	
Work memory	
• Integrated	32 KB
• Expandable	No
Load memory	Plugged in with MMC (max. 8 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	ensured with MMC (maintenance-free)
Processing times	
Processing times for	
• Bit operation	min. 0.1 µs
• Word instructions	min. 0. µs
• Fixed-point arithmetic	Min. 2 µs
• Floating-point maths	Min. 6 µs
Timers/counters and their retentivity	
S7 counters	256
• Retentive memory	Configurable
• Default	from C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
S7 timers	256
• Retentive memory	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s

Specifications	
IEC Timers	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
Data areas and their retentivity	
flag bits	256 bytes
• Retentive memory	Configurable
• Retentivity is default setting	MB0 to MB15
Clock memory bits	8 (1 byte per memory bit)
Data blocks	max. 511 (DB 1 to DB 511)
• Size	max. 16 KB
Local data per priority class	max. 510 bytes
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	max. 16 KB
Nesting depth	
• per priority class	8
• additional within an error OB	4
FBs	max. 512 (FB 0 to FB 511)
• Size	max. 16 KB
FCs	max. 512 (FC 0 to FC 511)
• Size	max. 16 KB
Address areas (I/Os)	
Total I/O address area	max. 1024 bytes/1024 bytes (can be freely addressed)
I/O process image	128 bytes/128 bytes
Digital channels	max. 1016
• of those local	max. 992
• integrated channels	24 DI / 16 DO
Analog channels	max. 253
• of those local	max. 248
• integrated channels	4 + 1 AI / 2 AO

Specifications	
Assembly	
Module racks	max. 4
Modules per module rack	max. 8; max. 7 in rack 3
Number of DP masters	
• Integrated	None
• via CP	max. 2
Number of function modules and communication processors you can operate	
• FM	max. 8
• CP (PtP)	max. 8
• CP (LAN)	max. 6
Time-of-day	
Real-time clock	yes (HW clock)
• Buffered	Yes
• Backup period	Typically 6 weeks (at an ambient temperature of 40 °C)
• Accuracy	Deviation per day < 10 s
Operating hours counter	1
• Number	0
• Range of values	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	yes; must be manually restarted after every restart
Clock synchronization	Yes
• in the PLC	Master
• on MPI	Master/slave
S7 signaling functions	
Number of stations that can be logged on for signaling functions	max. 8 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostic messages	Yes
• simultaneously enabled interrupt S blocks	max. 20
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number of variables	max. 30
Of those as status variable	max. 30
Of those as control variable	max. 14

Specifications	
Force	Yes
• Variable	Inputs, outputs
• Number of variables	max. 10
Status block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (not configurable)	max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	4
• Number of GD packets	max. 4
Sending stations	max. 4
Receiving stations	max. 4
• Size of GD packets	max. 22 bytes
Of those are consistent	22 bytes
S7-based communication	Yes
• User data per job	max. 76 bytes
Of those are consistent	76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	
• as server	Yes
• as Client	Yes (via CP and loadable FBs)
• User data per job	max. 180 bytes (with PUT/GET)
Of those are consistent	64 bytes
S5-compatible communication	Yes (via CP and loadable FCs)
Number of connections	max. 8
usable for	
• PG communication	max. 7
Reserved (Default)	1
configurable	from 1 to 7
• OP communication	max. 7
Reserved (Default)	1
configurable	from 1 to 7
• S7-based communication	max. 4
Reserved (Default)	4
configurable	from 0 to 4
Routing	No

Specifications	
Interfaces	
1st interface	
Type of interface	integrated RS485 interface
Physics	RS485
electrically isolated	No
Interface current supply (15 to 30 V DC)	max. 200 mA
Functionality	
• MPI	Yes
• PROFIBUS-DP	No
• PtP communication	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	No
• Global data communication	Yes
• S7-based communication	Yes
• S7 communication	
as server	Yes
as Client	Yes (via CP and loadable FBs)
• Transmission rates	max. 187.5 Kbps
Programming	
Programming language	LAD/FBD/STL
Available instructions	See the Instruction List
Nesting levels	8
System functions (SFCs)	See the Instruction List
System function blocks (SFBs)	See the Instruction List
User program security	Yes
Integrated I/O	
• Default addresses of the integrated	
Digital inputs	124.0 to 126.7
Digital outputs	124.0 to 125.7
Analog inputs	752 to 761
Analog outputs	752 to 755
Integrated functions	
Counters	3 channels (see the Manual *Technological Functions*)
Frequency counters	3 channels, max. 30 kHz (see the Manual *Technological Functions*)
Pulse outputs	3 channels for pulse width modulation, up to max. 2.5 kHz (see the Manual *Technological Functions*)

Specifications	
Positioning control	No
Integrated "Controlling" SFB	PID controller (see the Manual *Technological Functions*)
Dimensions	
Mounting dimensions W x H x D (mm)	120 x 125 x 130
Weight	660 g
Voltages, currents	
Power supply (nominal value)	24V DC
• Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	typically 150 mA
Inrush current	typically 11 A
Power consumption (nominal value)	700 mA
I^2t	0.7 A^2s
External fusing of power supply lines (recommended)	LS switch Type C min. 2 A, LS switch Type B min. 4 A
Power loss	typically 14 W

Cross-reference

In Chapter *Specifications of the integrated I/O* you can find

- the specifications of integrated I/O under *Digital inputs of CPUs 31xC*, *Digital outputs of CPUs 31xC, Analog inputs of CPUs 31xC* and *Analog outputs of CPUs 31xC*.
- the block diagrams of the integrated I/Os, under *Arrangement and usage of the integrated I/Os*.

6.5 CPU 313C-2 PtP and CPU 313C-2 DP

Specifications

Table 6-4 Specifications for CPU 313C-2 PtP/ CPU 313C-2 DP

Specifications		
CPU and version	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Item number	6ES7 313-6BE01-0AB0	6ES7 313-6CE01-0AB0
• Hardware version	01	01
• Firmware version	V2.0.0	V2.0.0
Associated programming package	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)
Memory	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Work memory		
• Integrated	32 KB	
• Expandable	No	
Load memory	Plugged in with MMC (max. 8 MB)	
Data storage life on the MMC (following final programming)	At least 10 years	
Buffering	ensured with MMC (maintenance-free)	
Processing times	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Processing times for		
• Bit operation	min. 0.1 µs	
• Word instructions	min. 0. µs	
• Fixed-point arithmetic	Min. 2 µs	
• Floating-point maths	Min. 6 µs	
Timers/counters and their retentivity	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
S7 counters	256	
• Retentive memory	Configurable	
• Default	from C0 to C7	
• Counting range	0 to 999	
IEC Counters	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	
S7 timers	256	
• Retentive memory	Configurable	
• Default	Not retentive	
• Timer range	10 ms to 9990 s	

Specifications		
IEC Timers	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	
Data areas and their retentivity	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
flag bits	256 bytes	
• Retentive memory	Configurable	
• Retentivity is default setting	MB0 to MB15	
Clock memory bits	8 (1 byte per memory bit)	
Data blocks	max. 511 (DB 1 to DB 511)	
• Size	max. 16 KB	
Local data per priority class	max. 510 bytes	
Blocks	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.	
OBs	See the Instruction List	
• Size	max. 16 KB	
Nesting depth		
• per priority class	8	
• additional within an error OB	4	
FBs	max. 512 (FB 0 to FB 511)	
• Size	max. 16 KB	
FCs	max. 512 (FC 0 to FC 511)	
• Size	max. 16 KB	
Address areas (I/Os)	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Total I/O address area	max. 1024 bytes/1024 bytes (can be freely addressed)	max. 1024 bytes/1024 bytes (can be freely addressed)
• Distributed	None	max. 1008 bytes
I/O process image	128 bytes/128 bytes	128 bytes/128 bytes
Digital channels	max. 1008	max. 8192
• of those local	max. 992	max. 992
• integrated channels	16 DI / 16 DO	16 DI / 16 DO
Analog channels	max. 248	max. 512
• of those local	max. 248	max. 248
• integrated channels	None	None

Specifications		
Assembly	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Module racks	max. 4	
Modules per module rack	max. 8; max. 7 in rack 3	
Number of DP masters		
• Integrated	No	1
• via CP	max. 1	max. 1
Number of function modules and communication processors you can operate		
• FM	max. 8	
• CP (PtP)	max. 8	
• CP (LAN)	max. 6	
Time-of-day	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Real-time clock	yes (HW clock)	
• Buffered	Yes	
• Backup period	Typically 6 weeks (at an ambient temperature of 40 °C)	
• Accuracy	Deviation per day < 10 s	
Operating hours counter	1	
• Number	0	
• Range of values	2^{31} hours (if SFC 101 is used)	
• Granularity	1 hour	
• Retentive	yes; must be manually restarted after every restart	
Clock synchronization	Yes	
• in the PLC	Master	
• on MPI	Master/slave	
S7 signaling functions	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Number of stations that can log in for signaling functions (e.g. OS)	max. 8 (depends on the number of connections configured for PG / OP and S7 basic communication)	
Process diagnostic messages	Yes	
• simultaneously enabled interrupt S blocks	max. 20	
Testing and commissioning functions	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Status/Modify Variables	Yes	
• Variable	Inputs, outputs, flags, DBs, timers, counters	
• Number of variables	max. 30	
Of those as status variable	max. 30	
Of those as control variable	max. 14	

Specifications		
Force	Yes	
• Variable	Inputs, outputs	
• Number of variables	max. 10	
Status block	Yes	
Single sequence	Yes	
Breakpoint	2	
Diagnostic buffer	Yes	
• Number of entries (not configurable)	max. 100	
Communication functions	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
PG/OP communication	Yes	
Global data communication	Yes	
• Number of GD circuits	4	
• Number of GD packets	max. 4	
Sending stations	max. 4	
Receiving stations	max. 4	
• Size of GD packets	max. 22 bytes	
Of those are consistent	22 bytes	
S7-based communication	Yes (server)	
• User data per job	max. 76 bytes	
Of those are consistent	76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)	
S7 communication		
• as server	Yes	
• as Client	Yes (via CP and loadable FBs)	
• User data per job	max. 180 bytes (with PUT/GET)	
Of those are consistent	64 bytes	
S5-compatible communication	Yes (via CP and loadable FCs)	
Number of connections	max. 8	
usable for		
• PG communication	max. 7	
Reserved (Default)	1	
configurable	from 1 to 7	
• OP communication	max. 7	
Reserved (Default)	1	
configurable	from 1 to 7	
• S7-based communication	max. 4	
Reserved (Default)	4	
configurable	from 0 to 4	
Routing	No	max. 4

Specifications		
Interfaces	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
1st interface		
Type of interface	integrated RS485 interface	
Physics	RS485	
electrically isolated	No	
Interface current supply (15 to 30 V DC)	max. 200 mA	
Functionality		
• MPI	Yes	
• PROFIBUS-DP	No	
• PtP communication	No	
MPI		
Services		
• PG/OP communication	Yes	
• Routing	No	Yes
• Global data communication	Yes	
• S7-based communication	Yes	
• S7 communication		
as server	Yes	
as Client	Yes (via CP and loadable FBs)	
• Transmission rates	max. 187.5 Kbps	
2nd interface	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Type of interface	integrated RS422/RS485 interface	integrated RS485 interface
Physics	RS 422/485	RS485
electrically isolated	Yes	Yes
Interface current supply (15 to 30 V DC)	No	max. 200 mA
Number of connections	None	8
Functionality		
• MPI	No	No
• PROFIBUS-DP	No	Yes
• PtP communication	Yes	No
DP master		
Number of connections	–	8
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes
• Global data communication	–	No
• S7-based communication	–	No

Specifications		
• S7 communication	–	No
• Constant Bus Cycle Time	–	Yes
• SYNC/FREEZE	–	Yes
• Activation/deactivation of DP slaves	–	Yes
• DPV1	–	Yes
• Transmission rates	–	Up to 12 Mbps
• Number of DP slaves per station	–	max. 32;
• Address area	–	max. 1 KB I / 1 KB O
• User data per DP slave	–	max. 244 bytes I / 244 bytes O
DP Slave		
Number of connections	–	8
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes (only if interface is active)
• Global data communication	–	No
• S7-based communication	–	No
• S7 communication	–	No
• Direct Data Exchange	–	Yes
• Transmission rates	–	Up to 12 Mbps
• Automatic baud rate search	–	Yes (only if interface is passive)
• Transfer memory	–	244 bytes I / 244 bytes O
• Address Areas	–	max. 32 with max. 32 bytes each
• DPV1	–	No
GSD file	–	The latest GSD file is available at: http://www.ad.siemens.de/support in the Product Support area
Point-to-Point communication		
• Transmission rates	38.4 Kbps half duplex 19.2 Kbps full duplex	–
• Cable length	max. 1200 m	–
• The user program can control the interface	Yes	–
• The interface can trigger a break or an interrupt in the user program	Yes (message with break ID)	–
• Protocol driver	3964(R); ASCII	–

Specifications		
Programming	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Programming language	LAD/FBD/STL	
Available instructions	See the Instruction List	
Nesting levels	8	
System functions (SFCs)	See the Instruction List	
System function blocks (SFBs)	See the Instruction List	
User program security	Yes	
Integrated I/O	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
• Default addresses of the integrated		
Digital inputs	124.0 to 125.7	
Digital outputs	124.0 to 125.7	
Integrated functions		
Counters	3 channels (see the Manual *Technological Functions*)	
Frequency counters	3 channels, max. 30 kHz (see the Manual *Technological Functions*)	
Pulse outputs	3 channels for pulse width modulation, up to max. 2.5 kHz (see the Manual *Technological Functions*)	
Positioning control	No	
Integrated "Controlling" SFB	PID controller (see the Manual *Technological Functions*)	
Dimensions	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Mounting dimensions W x H x D (mm)	120 x 125 x 130	
Weight	approx. 566 g	
Voltages, currents	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Power supply (nominal value)	24V DC	
• Permitted range	20.4 V to 28.8 V	
Current consumption (no-load operation)	typically 100 mA	
Inrush current	typically 11 A	
Power consumption (nominal value)	700 mA	900 mA
I^2t	0.7 A^2s	
External fusing of power supply lines (recommended)	LS switch Type C min. 2 A, type B min. 4 A	
Power loss	typically 10 W	
Standards and Approvals	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
PNO Certificate		
• DP master	–	
• DP Slave	–	

Cross-reference

In Chapter *Specifications of the integrated I/O* you can find

- the specifications of integrated I/Os under *Digital inputs of CPUs 31xC* and *Digital outputs of CPUs 31xC*.
- the block diagrams of the integrated I/Os, under *Arrangement and usage of the integrated I/Os*.

6.6 CPU 314

Specifications for the CPU 314

Table 6-5 Specifications for the CPU 314

Specifications	
CPU and version	
Item number	6ES7314-1AF10-0AB0
• Hardware version	01
• Firmware version	V 2.0.0
• Corresponding programming package	STEP 7 as of V 5.1 + SP 4
Memory	
Work memory	
• Integrated	48 KB
• Expandable	No
Load memory	Plugged in with MMC (max. 8 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	ensured with MMC (maintenance-free)
Processing times	
Processing times for	
• Bit operation	min. 0.1 µs
• Word instructions	Min. 0.2 µs
• Fixed-point arithmetic	Min. 2.0 µs
• Floating-point maths	Min. 6 µs
Timers/counters and their retentivity	
S7 counters	256
• Retentive memory	Configurable
• Default	from C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)

Specifications	
S7 timers	256
• Retentive memory	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
Data areas and their retentivity	
flag bits	256 bytes
• Retentive memory	Yes
• Retentivity is default setting	MB0 to MB15
Clock memory bits	8 (1 byte per memory bit)
Data blocks	
• Number	511 (DB 1 to DB 511)
• Size	16 KB
Local data per priority class	max. 510
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	16 KB
Nesting depth	
• per priority class	8
• additional within an error OB	4
FBs	See the Instruction List
• Number	512 (FB 0 to FB 511)
• Size	16 KB
FCs	See the Instruction List
• Number	512 (FC 0 to FC 511)
• Size	16 KB
Address areas (I/Os)	
Total I/O address area	max. 1024 bytes/1024 bytes (can be freely addressed)
I/O process image	128 bytes/128 bytes
Digital channels	max. 1024
of those local	max. 1024

Specifications	
Analog channels	max. 256
of those local	max. 256
Assembly	
Module racks	max. 4
Modules per module rack	8
Number of DP masters	
• Integrated	None
• via CP	max. 1
Number of function modules and communication processors you can operate	
• FM	max. 8
• CP (PtP)	max. 8
• CP (LAN)	max. 10
Time-of-day	
Real-time clock	yes (HW clock)
• Buffered	Yes
• Backup period	normally 6 weeks (at an ambient temperature of 40 °C)
• Accuracy	Deviation per day: < 10 s
Operating hours counter	1
• Number	0
• Range of values	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	yes; must be manually restarted after every restart
Clock synchronization	Yes
• in the PLC	Master
• on MPI	Master/slave
S7 signaling functions	
Number of stations that can log in for signaling functions (e.g. OS)	12 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostic messages	Yes
• simultaneously enabled interrupt S blocks	max. 40
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number of variables	30
Of those as status variable	30
of those as control variable	14

Specifications	
Force	Yes
• Variable	Inputs / Outputs
• Number of variables	max. 10
Status block	Yes
Single sequence	Yes
Breakpoint	
Diagnostic buffer	Yes
• Number of entries (not configurable)	max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	4
• Number of GD packets	max. 4
Sending stations	max. 4
Receiving stations	max. 4
• Size of GD packets	max. 22 bytes
Consistent data	22 bytes
S7-based communication	Yes
• User data per job	max. 76 bytes
Consistent data	76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	Yes
• as server	Yes
• as Client	Yes (via CP and loadable FBs)
• User data per job	max. 180 (for PUT/GET)
Consistent data	64 bytes
S5-compatible communication	Yes (via CP and loadable FCs)
Number of connections	12
usable for	
• PG communication	
Reserved (Default)	1
Configurable	1 to 11
• OP communication	
Reserved (Default)	1
Configurable	1 to 11
• S7-based communication	
Reserved (Default)	8
Configurable	0 to 8
Routing	No

Specifications	
Interfaces	
1st interface	
Type of interface	integrated RS485 interface
Physics	RS485
electrically isolated	No
Interface current supply (15 to 30 V DC)	max. 200 mA
Functionality	
• MPI	Yes
• PROFIBUS-DP	No
• PtP communication	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	No
• Global data communication	Yes
• S7-based communication	Yes
• S7 communication	Yes
as server	Yes
as Client	Yes (via CP and loadable FBs)
• Transmission rates	187.5 Kbps
Programming	
Programming language	LAD/FBD/STL
Available instructions	See the Instruction List
Nesting levels	8
System functions (SFCs)	See the Instruction List
System function blocks (SFBs)	See the Instruction List
User program security	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	40 x 125 x 130
Weight	280 g
Voltages, currents	
Power supply (nominal value)	24 VDC
• Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	normally 60 mA
Inrush current	normally 2.5 A
Power consumption (nominal value)	0.6A
I^2t	0.5 A^2s
External fusing of power supply lines (recommended)	min. 2 A
Power loss	typically 2.5 W

6.7 CPU 314C-2 PtP and CPU 314C-2 DP

Specifications

Table 6-6 Specifications for the CPU 314C-2 PtP and CPU 314C-2 DP

Specifications		
CPU and version	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Item number	6ES7 314-6BF01-0AB0	6ES7 314-6CF01-0AB0
• Hardware version	01	01
• Firmware version	V2.0.0	V2.0.0
Associated programming package	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)
Memory	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Work memory		
• Integrated	48 KB	
• Expandable	No	
Load memory	Plugged in with MMC (max. 8 MB)	
Data storage life on the MMC (following final programming)	At least 10 years	
Buffering	ensured with MMC (maintenance-free)	
Processing times	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Processing times for		
• Bit operation	min. 0.1 µs	
• Word instructions	Min. 0.2 µs	
• Fixed-point arithmetic	Min. 2 µs	
• Floating-point maths	Min. 6 µs	
Timers/counters and their retentivity	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
S7 counters	256	
• Retentive memory	Configurable	
• Default	from C0 to C7	
• Counting range	0 to 999	
IEC Counters	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	
S7 timers	256	
• Retentive memory	Configurable	
• Default	Not retentive	
• Timer range	10 ms to 9990 s	

Specifications		
IEC Timers	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	
Data areas and their retentivity	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
flag bits	256 bytes	
• Retentive memory	Configurable	
• Retentivity is default setting	MB0 to MB15	
Clock memory bits	8 (1 byte per memory bit)	
Data blocks	max. 511 (DB 1 to DB 511)	
• Size	max. 16 KB	
Local data per priority class	max. 510 bytes	
Blocks	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.	
OBs	See the Instruction List	
• Size	max. 16 KB	
Nesting depth		
• per priority class	8	
• additional within an error OB	4	
FBs	max. 512 (FB 0 to FB 511)	
• Size	max. 16 KB	
FCs	max. 512 (FC 0 to FC 511)	
• Size	max. 16 KB	
Address areas (I/Os)	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Total I/O address area	max. 1024 bytes/1024 bytes (can be freely addressed)	max. 1024 bytes/1024 bytes (can be freely addressed)
• Distributed	None	max. 1,000 bytes
I/O process image	128 bytes/128 bytes	128 bytes/128 bytes
Digital channels	max. 1016	max. 8192
• of those local	max. 992	max. 992
• integrated channels	24 DI / 16 DO	24 DI / 16 DO
Analog channels	max. 253	max. 512
• of those local	max. 248	max. 248
• integrated channels	4 + 1 AI / 2 AO	4 + 1 AI / 2 AO

Specifications		
Assembly	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Module racks	max. 4	
Modules per module rack	max. 8; max. 7 in rack 3	
Number of DP masters		
• Integrated	No	1
• via CP	max. 1	max. 1
Number of function modules and communication processors you can operate		
• FM	max. 8	
• CP (PtP)	max. 8	
• CP (LAN)	max. 10	
Time-of-day	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Real-time clock	yes (HW clock)	
• Buffered	Yes	
• Backup period	Typically 6 weeks (at an ambient temperature of 40 °C)	
• Accuracy	Deviation per day < 10 s	
Operating hours counter	1	
• Number	0	
• Range of values	2^{31} hours (if SFC 101 is used)	
• Granularity	1 hour	
• Retentive	yes; must be manually restarted after every restart	
Clock synchronization	Yes	
• in the PLC	Master	
• on MPI	Master/slave	
S7 signaling functions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Number of stations that can log in for signaling functions (e.g. OS)	max. 12 (depends on the number of connections configured for PG / OP and S7 basic communication)	
Process diagnostic messages	Yes	
• simultaneously enabled interrupt S blocks	max. 40	
Testing and commissioning functions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Status/Modify Variables	Yes	
• Variable	Inputs, outputs, flags, DBs, timers, counters	
• Number of variables	max. 30	
Of those as status variable	max. 30	
Of those as control variable	max. 14	

Specifications		
Force	Yes	
• Variable	Inputs, outputs	
• Number of variables	max. 10	
Status block	Yes	
Single sequence	Yes	
Breakpoint	2	
Diagnostic buffer	Yes	
• Number of entries (not configurable)	max. 100	
Communication functions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
PG/OP communication	Yes	
Global data communication	Yes	
• Number of GD circuits	4	
• Number of GD packets	max. 4	
Sending stations	max. 4	
Receiving stations	max. 4	
• Size of GD packets	max. 22 bytes	
Of those are consistent	22 bytes	
S7-based communication	Yes	
• User data per job	max. 76 bytes	
Of those are consistent	76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)	
S7 communication		
• as server	Yes	
• as Client	Yes (via CP and loadable FBs)	
• User data per job	max. 180 bytes (with PUT/GET)	
Of those are consistent	64 bytes	
S5-compatible communication	Yes (via CP and loadable FCs)	
Number of connections	max. 12	
usable for		
• PG communication	max. 11	
Reserved (Default)	1	
configurable	from 1 to 11	
• OP communication	max. 11	
Reserved (Default)	1	
configurable	from 1 to 11	
• S7-based communication	max. 8	
Reserved (Default)	8	
configurable	from 0 to 8	
Routing	No	max. 4

Specifications		
Interfaces	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
1st interface		
Type of interface	integrated RS485 interface	
Physics	RS485	
electrically isolated	No	
Interface current supply (15 to 30 V DC)	max. 200 mA	
Functionality		
• MPI	Yes	
• PROFIBUS-DP	No	
• PtP communication	No	
MPI		
Number of connections	12	
Services		
• PG/OP communication	Yes	
• Routing	No	Yes
• Global data communication	Yes	
• S7-based communication	Yes	
• S7 communication		
as server	Yes	
as Client	Yes (via CP and loadable FBs)	
• Transmission rates	max. 187.5 Kbps	
2nd interface	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Type of interface	integrated RS422/RS485 interface	integrated RS485 interface
Physics	RS 422/485	RS485
electrically isolated	Yes	Yes
Interface current supply (15 to 30 V DC)	No	max. 200 mA
Number of connections	None	12
Functionality		
• MPI	No	No
• PROFIBUS-DP	No	Yes
• PtP communication	Yes	No
DP master		
Number of connections	–	12
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes
• Global data communication	–	No

Specifications		
• S7-based communication	–	No
• S7 communication	–	No
• Constant Bus Cycle Time	–	Yes
• SYNC/FREEZE	–	Yes
• Activation/deactivation of DP slaves	–	Yes
• DPV1	–	Yes
• Transmission rates	–	Up to 12 Mbps
• Number of DP slaves per station	–	max. 32;
• Address area	–	max. 1 Kbyte I / 1 Kbyte O
• User data per DP slave	–	max. 244 bytes I / 244 bytes O
DP Slave		
Number of connections	–	12
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes (only if interface is active)
• Global data communication	–	No
• S7-based communication	–	No
• S7 communication	–	No
• Direct Data Exchange	–	Yes
• Transmission rates	–	Up to 12 Mbps
• Transfer memory	–	244 bytes I / 244 bytes O
• Automatic baud rate search	–	Yes (only if interface is passive)
• Address Areas		max. 32 with max. 32 bytes each
• DPV1	–	No
GSD file	–	The latest GSD file is available at: http://www.ad.siemens.de/support in the Product Support area
Point-to-Point communication		
• Transmission rates	38.4 Kbps half duplex 19.2 Kbps full duplex	–
• Cable length	max. 1200 m	–
• The user program can control the interface	Yes	–
• The interface can trigger a break or an interrupt in the user program	Yes (message with break ID)	–
• Protocol driver	3964 (R); ASCII and RK512	–

Specifications		
Programming	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Programming language	LAD/FBD/STL	
Available instructions	See the Instruction List	
Nesting levels	8	
System functions (SFCs)	See the Instruction List	
System function blocks (SFBs)	See the Instruction List	
User program security	Yes	
Integrated I/O	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
• Default addresses of the integrated		
Digital inputs	124.0 to 126.7	
Digital outputs	124.0 to 125.7	
Analog inputs	752 to 761	
Analog outputs	752 to 755	
Integrated functions		
Counters	4 channels (see the Manual *Technological Functions*)	
Frequency counters	4 channels, up to max. 60 kHz (see the Manual *Technological Functions*)	
Pulse outputs	4 channels for pulse width modulation, up to max. 2.5 kHz (see the Manual *Technological Functions*)	
Positioning control	1 channel (see the Manual *Technological Functions*)	
Integrated "Controlling" SFB	PID controller (see the Manual *Technological Functions*)	
Dimensions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Mounting dimensions W x H x D (mm)	120 x 125 x 130	
Weight	approx. 676 g	
Voltages, currents	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Power supply (nominal value)	24V DC	
• Permitted range	20.4 V to 28.8 V	
Current consumption (no-load operation)	typically 150 mA	
Inrush current	normally 11A	
Power consumption (nominal value)	800 mA	1000 mA
I^2t	0.7 A^2s	
External fusing of power supply lines (recommended)	LS switch Type C min. 2 A, LS switch Type B min. 4 A	
Power loss	normally 14 W	
Standards and Approvals	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
PNO Certificate		
• DP master	–	
• DP Slave	–	

Cross-reference

In Chapter *Specifications of the integrated I/O* you can find

- the specifications of integrated I/O under *Digital inputs of CPUs 31xC*, *Digital outputs of CPUs 31xC, Analog inputs of CPUs 31xC* and *Analog outputs of CPUs 31xC*.
- the block diagrams of the integrated I/Os, under *Arrangement and usage of the integrated I/Os*.

6.8 CPU 315-2 DP

Specifications

Table 6-7 Specifications for the CPU 315-2 DP

Specifications	
CPU and version	
Item number	6ES7315-2AG10-0AB0
• Hardware version	01
• Firmware version	V 2.0.0
• Corresponding programming package	STEP 7 as of V 5.1 + SP 4
Memory	
Work memory	
• Integrated	128 KB
• Expandable	No
Load memory	Plugged in with MMC (max. 8 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	ensured with MMC (maintenance-free)
Processing times	
Processing times for	
• Bit operation	min. 0.1 µs
• Word instructions	Min. 0.2 µs
• Fixed-point arithmetic	Min. 2.0 µs
• Floating-point maths	Min. 6 µs
Timers/counters and their retentivity	
S7 counters	256
• Retentive memory	Configurable
• Default	from C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)

Specifications	
S7 timers	256
• Retentive memory	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
Data areas and their retentivity	
flag bits	2048 bytes
• Retentive memory	Yes
• Retentivity is default setting	MB0 to MB15
Clock memory bits	8 (1 byte per memory bit)
Data blocks	
• Number	1023 (DB 1 to DB 1023)
• Size	16 KB
Local data capacity	Max. 1024 bytes per task
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	16 KB
Nesting depth	
• per priority class	8
• additional within an error OB	4
FBs	See the Instruction List
• Number	2048 (FB 0 to FB 2047)
• Size	16 KB
FCs	See the Instruction List
• Number	2048 (FC 0 to FC 2047)
• Size	16 KB
Address areas (I/Os)	
Total I/O address area	max. 2048 bytes/2048 bytes (can be freely addressed)
Distributed	max. 2000

Specifications	
I/O process image	128/128
Digital channels	max. 16384
of those local	max. 1024
Analog channels	max. 1024
of those local	max. 256
Assembly	
Module racks	max. 4
Modules per module rack	8
Number of DP masters	
• Integrated	1
• via CP	1
Number of function modules and communication processors you can operate	
• FM	max. 8
• CP (PtP)	max. 8
• CP (LAN)	max. 10
Time-of-day	
Real-time clock	yes (HW clock)
• Buffered	Yes
• Backup period	normally 6 weeks (at an ambient temperature of 40 °C)
• Accuracy	Deviation per day: < 10 s
Operating hours counter	1
• Number	0
• Range of values	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	yes; must be manually restarted after every restart
Clock synchronization	Yes
• in the PLC	Master
• on MPI	Master/slave
S7 signaling functions	
Number of stations that can log in for signaling functions (e.g. OS)	16 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostic messages	Yes
• simultaneously enabled interrupt S blocks	40

Specifications	
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number of variables	30
Of those as status variable	30
of those as control variable	14
Force	
• Variable	Inputs / Outputs
• Number of variables	max. 10
Status block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (not configurable)	max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	8
• Number of GD packets	max. 8
Sending stations	max. 8
Receiving stations	max. 8
• Size of GD packets	max. 22 bytes
Consistent data	22 bytes
S7-based communication	Yes
• User data per job	max. 76 bytes
Consistent data	76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	Yes
• as server	Yes
• as Client	Yes (via CP and loadable FBs)
• User data per job	max. 180 bytes (with PUT/GET)
Consistent data	64 byte (as the server)
S5-compatible communication	Yes (via CP and loadable FCs)
Number of connections	16
usable for	
• PG communication	
Reserved (Default)	1
Configurable	1 to 15

Specifications	
• OP communication	
Reserved (Default)	1
Configurable	1 to 15
• S7-based communication	Yes
Reserved (Default)	12
Configurable	0 to 12
Routing	Yes
Interfaces	
1st interface	
Type of interface	integrated RS485 interface
Physics	RS485
electrically isolated	No
Interface current supply (15 to 30 V DC)	max. 200 mA
Functionality	
• MPI	Yes
• PROFIBUS-DP	No
• PtP communication	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	Yes
• S7-based communication	Yes
• S7 communication	Yes
as server	Yes
as Client	Yes (via CP and loadable FBs)
• Transmission rates	187.5 Kbps
2nd interface	
Type of interface	integrated RS485 interface
Physics	RS485
electrically isolated	Yes
Type of interface	integrated RS485 interface
Interface current supply (15 to 30 V DC)	max. 200 mA
Functionality	
MPI	No
PROFIBUS-DP	Yes
PtP communication	No

Specifications	
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7-based communication	No
• S7 communication	No
• Constant Bus Cycle Time	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission speed	Up to 12 Mbps
Number of DP slaves per station	124
Address area	max. 244 bytes
DP Slave	
Services	
• PG/OP communication	Yes
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7-based communication	No
• S7 communication	No
• Direct Data Exchange	Yes
• Transmission rates	Up to 12 Mbps
• Automatic baud rate search	Yes (only if interface is passive)
• Transfer memory	244 bytes I / 244 bytes O
• Address Areas	max. 32 with max. 32 bytes each
• DPV1	No
GSD file	The latest GSD file is available at: http://www.ad.siemens.de/support in the Product Support area
Programming	
Programming language	LAD/FBD/STL
Available instructions	See the Instruction List
Nesting levels	8
System functions (SFCs)	See the Instruction List
System function blocks (SFBs)	See the Instruction List
User program security	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	40 x 125 x 130
Weight	290 g

Specifications	
Voltages, currents	
Power supply (nominal value)	24 VDC
- Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	normally 60 mA
Inrush current	normally 2.5 A
Power consumption (nominal value)	0.8A
I^2t	0.5 A^2s
External fusing of power supply lines (recommended)	min. 2 A
Power loss	normally 2.5 W

6.9 CPU 317-2 DP

Specifications

Table 6-8 Specifications for the CPU 317-2 DP

Specifications	
CPU and version	
Item number	6ES7317-2AJ10-0AB0
- Hardware version	01
- Firmware version	V 2.1.0
- Corresponding programming package	STEP 7 as of V 5.2 + SP 1
Memory	
Work memory	
- Integrated	512 KB
- Expandable	No
Capacity of the retentive memory for retentive data blocks	max. 256 KB
Load memory	Plugged in with MMC (max. 8 MB)
Buffering	ensured with MMC (maintenance-free)
Data storage life on the MMC (following final programming)	At least 10 years
Processing times	
Processing times for	
- Bit operation	min. 0.1 µs
- Word instructions	min. 0.1 µs
- Fixed-point arithmetic	Min. 0.4 µs
- Floating-point maths	min. 1.5 µs

Specifications	
Timers/counters and their retentivity	
S7 counters	512
• Retentive memory	Configurable
• Default	from C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	Unlimited (limited only by RAM size)
S7 timers	512
• Retentive memory	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB
• Number	Unlimited (limited only by RAM size)
Data areas and their retentivity	
flag bits	4096 bytes
• Retentive memory	Configurable
• Retentivity is default setting	From MB0 to MB15
Clock memory bits	8 (1 byte per memory bit)
Data blocks	
• Number	2047 (DB 1 to DB 2047)
• Size	64 KB
• Non-Retain support (configured retention)	Yes
Local data per priority class	Max. 1024 bytes per priority class/ max. 510 bytes per block
Blocks	
Total	2048 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	64 KB
Nesting depth	
• per priority class	16
• additional within an error OB	4

Specifications	
FBs	See the Instruction List
- Number	2048 (FB 0 to FB 2047)
- Size	64 KB
FCs	See the Instruction List
- Number	2048 (FC 0 to FC 2047)
- Size	64 KB
Address areas (I/Os)	
Total I/O address area	max. 8192 bytes/8192 bytes (can be freely addressed)
Distributed	max. 8192 bytes
I/O process image	256/256
Digital channels	65636/65536
of those local	max. 1024
Analog channels	4096/4096
of those local	256/256
Assembly	
Module racks	max. 4
Modules per module rack	8
Number of DP masters	
- Integrated	2
- via CP	2
Number of function modules and communication processors you can operate	
- FM	max. 8
- CP (PtP)	max. 8
- CP (LAN)	max. 10
Time-of-day	
Real-time clock	yes (HW clock)
- Buffered	Yes
- Backup period	normally 6 weeks (at an ambient temperature of 40 °C)
- Accuracy	Deviation per day: < 10 s
Operating hours counter	4
- Number	0 to 3
- Range of values	2^{31} hours (if SFC 101 is used)
- Granularity	1 hour
- Retentive	yes; must be manually restarted after every restart

Specifications	
Clock synchronization	Yes
• in the PLC	Master/slave
• on MPI	Master/slave
S7 signaling functions	
Number of stations that can be logged on for signaling functions	32 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostic messages	Yes
• simultaneously enabled interrupt S blocks	60
Testing and commissioning functions	
Status/Modify Variables	Yes
• Variable	Inputs, outputs, flags, DBs, timers, counters
• Number of variables	30
Of those as status variable	max. 30
of those as control variable	max. 14
Force	
• Variable	Inputs / Outputs
• Number of variables	max. 10
Status block	Yes
Single sequence	Yes
Breakpoint	2
Diagnostic buffer	Yes
• Number of entries (not configurable)	max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	8
• Number of GD packets	max. 8
Sending stations	max. 8
Receiving stations	max. 8
• Size of GD packets	max. 22 bytes
Consistent data	22 bytes
S7-based communication	Yes
• User data per job	max. 76 bytes
Consistent data	76 bytes (for X_SEND or X_RCV) 76 bytes (for X_PUT or X_GET as the server)

Specifications	
S7 communication	Yes
- as server	Yes
- as Client	Yes (via CP and loadable FBs)
- User data per job	max. 180 bytes (with PUT/GET)
Consistent data	160 byte (as the server)
S5-compatible communication	Yes (via CP and loadable FCs)
Number of connections	32
usable for	
- PG communication	
Reserved (Default)	1
Configurable	1 to 31
- OP communication	
Reserved (Default)	1
Configurable	1 to 31
- S7-based communication	Yes
Reserved (Default)	0
Configurable	0 to 30
Routing	Yes
Interfaces	
1st interface	
Type of interface	integrated RS485 interface
Physics	RS485
electrically isolated	Yes
Interface current supply (15 to 30 V DC)	max. 200 mA
Functionality	
- MPI	Yes
- PROFIBUS-DP	Yes
- PtP communication	No
MPI	
Services	
- PG/OP communication	Yes
- Routing	Yes
- Global data communication	Yes
- S7-based communication	Yes
- S7 communication	Yes
as server	Yes
as Client	Yes (via CP and loadable FBs)
- Transmission rates	Max. 12 Mbaud

Specifications	
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7-based communication	No
• S7 communication	No
• Constant Bus Cycle Time	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission speed	Up to 12 Mbps
Number of DP slaves	124
Address range per DP slave	max. 244 bytes
DP Slave (except for DP slave at both interfaces)	
Services	
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7-based communication	No
• S7 communication	No
• Direct Data Exchange	Yes
• Transmission rates	Up to 12 Mbps
• Automatic baud rate search	Yes (only if interface is passive)
• Transfer memory	244 bytes I / 244 bytes O
• Address Areas	max. 32 with max. 32 bytes each
• DPV1	No
2nd interface	
Type of interface	integrated RS485 interface
Physics	RS485
electrically isolated	Yes
Type of interface	integrated RS485 interface
Interface current supply (15 to 30 V DC)	max. 200 mA
Functionality	
MPI	No
PROFIBUS-DP	Yes
PtP communication	No

Specifications	
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7-based communication	No
• S7 communication	No
• Constant Bus Cycle Time	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission speed	Up to 12 Mbps
Number of DP slaves per station	124
Address area	max. 244 bytes
DP Slave **(except for DP slave at both interfaces)**	
Services	
• PG/OP communication	Yes
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7-based communication	No
• S7 communication	No
• Direct Data Exchange	Yes
• Transmission rates	Up to 12 Mbps
• Automatic baud rate search	Yes (only if interface is passive)
• Transfer memory	244 bytes I / 244 bytes O
• Address Areas	max. 32 with max. 32 bytes each
• DPV1	No
GSD file	The latest GSD file is available at: http://www.ad.siemens.de/support in the Product Support area
Programming	
Programming language	LAD/FBD/STL
Available instructions	See the Instruction List
Nesting levels	8
System functions (SFCs)	See the Instruction List
System function blocks (SFBs)	See the Instruction List
User program security	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	80 x 125 x 130
Weight	460 g

Specifications	
Voltages, currents	
Power supply (nominal value)	24 VDC
• Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	normally 100 mA
Inrush current	normally 2.5 A
I^2t	1 A^2s
Power consumption (nominal value)	0,85 A
External fusing of power supply lines (recommended)	min. 2 A
Power loss	normally 4 W

Specifications for integrated I/Os (CPU 31xC only)

7

7.1 Arrangement and Usage of Integrated I/Os

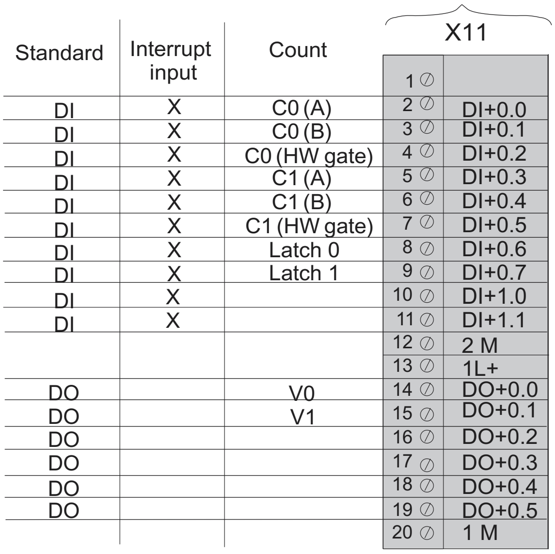
Introduction

The integrated I/O of 31xC CPUs can be used for technological functions or as standard I/O.

The figures below illustrate possible usage of I/Os integrated in the CPUs.

Further information on integrated I/O is found in the Manual "Technical Functions"

CPU 312C



Standard	Interrupt input	Count		X11
			1	
DI	X	C0 (A)	2	DI+0.0
DI	X	C0 (B)	3	DI+0.1
DI	X	C0 (HW gate)	4	DI+0.2
DI	X	C1 (A)	5	DI+0.3
DI	X	C1 (B)	6	DI+0.4
DI	X	C1 (HW gate)	7	DI+0.5
DI	X	Latch 0	8	DI+0.6
DI	X	Latch 1	9	DI+0.7
DI	X		10	DI+1.0
DI	X		11	DI+1.1
			12	2 M
			13	1L+
DO		V0	14	DO+0.0
DO		V1	15	DO+0.1
DO			16	DO+0.2
DO			17	DO+0.3
DO			18	DO+0.4
DO			19	DO+0.5
			20	1 M

Cn	Counter n
A, B	Sensor signals
Vn	Comparator n
X	Pin usable if not occupied by technological functions
HW gate	Gate control
Latch	Counting status

Figure 7-1 CPU 312C: Pin-out of the integrated DI/DO (Connector X11)

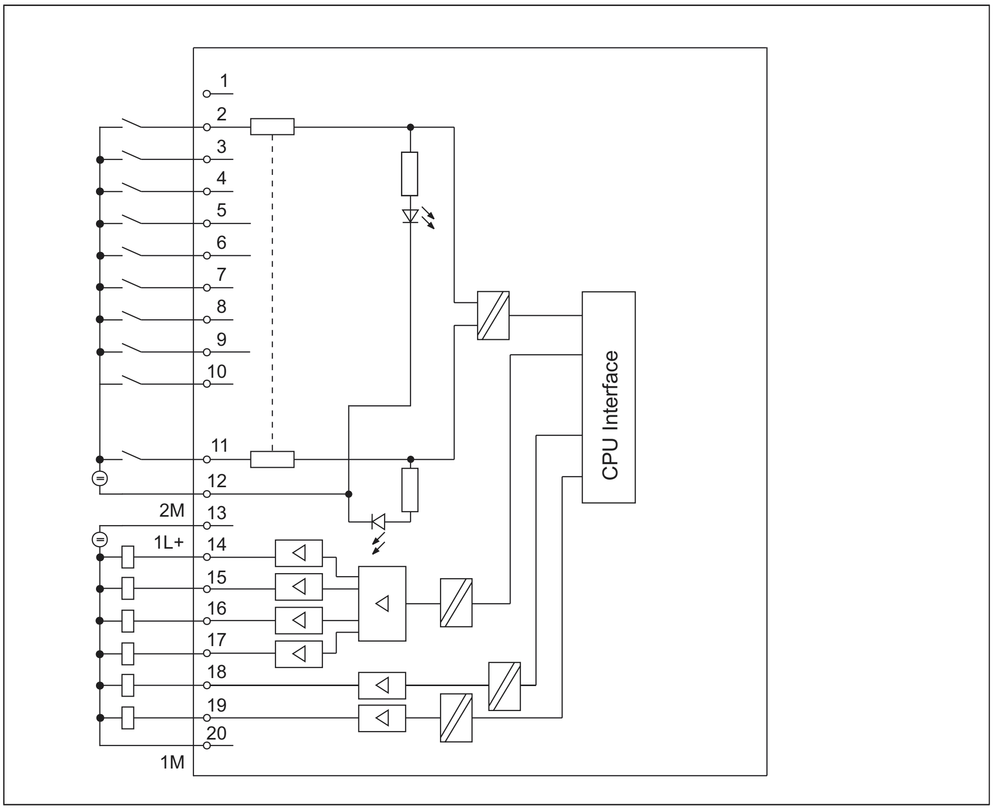
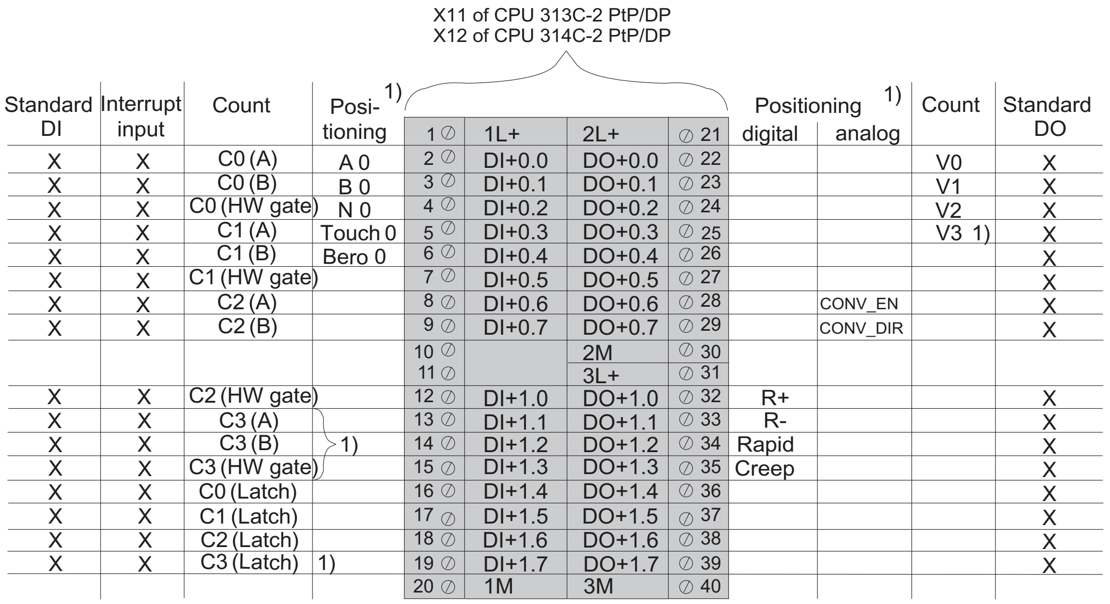


Figure 7-2 Block diagram of the integrated digital I/Os of the CPU 312C

CPU 313C, CPU 313C-2 DP/PtP, CPU 314C-2 DP/PtP



X11 of CPU 313C-2 PtP/DP
X12 of CPU 314C-2 PtP/DP

Standard DI	Interrupt input	Count	Posi-tioning 1)					Positioning 1) digital	Positioning 1) analog	Count	Standard DO
				1 ⌀	1L+	2L+	⌀ 21				
X	X	C0 (A)	A 0	2 ⌀	DI+0.0	DO+0.0	⌀ 22			V0	X
X	X	C0 (B)	B 0	3 ⌀	DI+0.1	DO+0.1	⌀ 23			V1	X
X	X	C0 (HW gate)	N 0	4 ⌀	DI+0.2	DO+0.2	⌀ 24			V2	X
X	X	C1 (A)	Touch 0	5 ⌀	DI+0.3	DO+0.3	⌀ 25			V3 1)	X
X	X	C1 (B)	Bero 0	6 ⌀	DI+0.4	DO+0.4	⌀ 26				X
X	X	C1 (HW gate)		7 ⌀	DI+0.5	DO+0.5	⌀ 27				X
X	X	C2 (A)		8 ⌀	DI+0.6	DO+0.6	⌀ 28		CONV_EN		X
X	X	C2 (B)		9 ⌀	DI+0.7	DO+0.7	⌀ 29		CONV_DIR		X
				10 ⌀		2M	⌀ 30				
				11 ⌀		3L+	⌀ 31				
X	X	C2 (HW gate)		12 ⌀	DI+1.0	DO+1.0	⌀ 32	R+			X
X	X	C3 (A)		13 ⌀	DI+1.1	DO+1.1	⌀ 33	R-			X
X	X	C3 (B)	1)	14 ⌀	DI+1.2	DO+1.2	⌀ 34	Rapid			X
X	X	C3 (HW gate)		15 ⌀	DI+1.3	DO+1.3	⌀ 35	Creep			X
X	X	C0 (Latch)		16 ⌀	DI+1.4	DO+1.4	⌀ 36				X
X	X	C1 (Latch)		17 ⌀	DI+1.5	DO+1.5	⌀ 37				X
X	X	C2 (Latch)		18 ⌀	DI+1.6	DO+1.6	⌀ 38				X
X	X	C3 (Latch)	1)	19 ⌀	DI+1.7	DO+1.7	⌀ 39				X
				20 ⌀	1M	3M	⌀ 40				

Cn	Counter n
A, B	Sensor signals
HW gate	Gate control
Latch	Save counter status
Vn	Comparator n
Touch 0	Touch probe 0
Bero 0	Reference-point switch 0
R+, R-	Directional signal
Rapid	Rapid traverse
Creep	Creep speed
CONV_EN	Enable power section
CONV_DIR	Directional signal (only for control mode "Voltage 0 up to 10 V or current from 0 to 20 mA and direction signal")
X	Pin usable if not occupied by technological functions

1) only CPU 314C-2

Figure 7-3 CPUs 313C/313C-2/314C-2: Pin-out of the integrated DI/DO (Connector X11 and X12)

Details are found in the *Manual "Technical Functions, in Chapters "Counting", "Frequency Measurement" and "Pulse Width Modulation"*

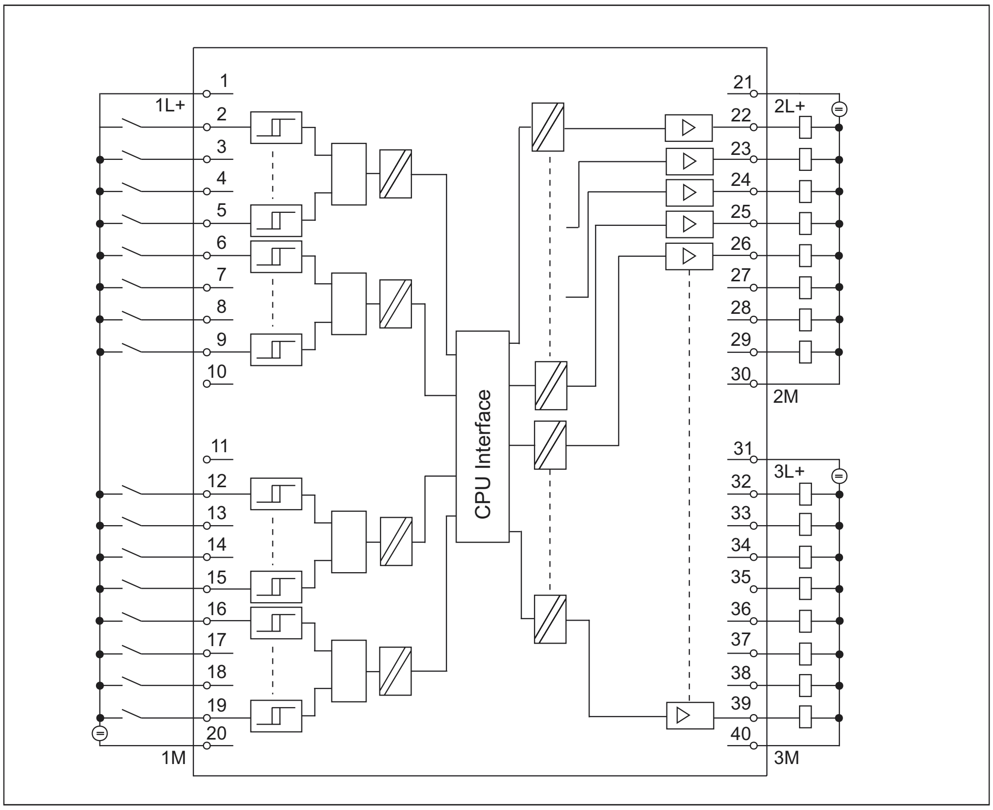
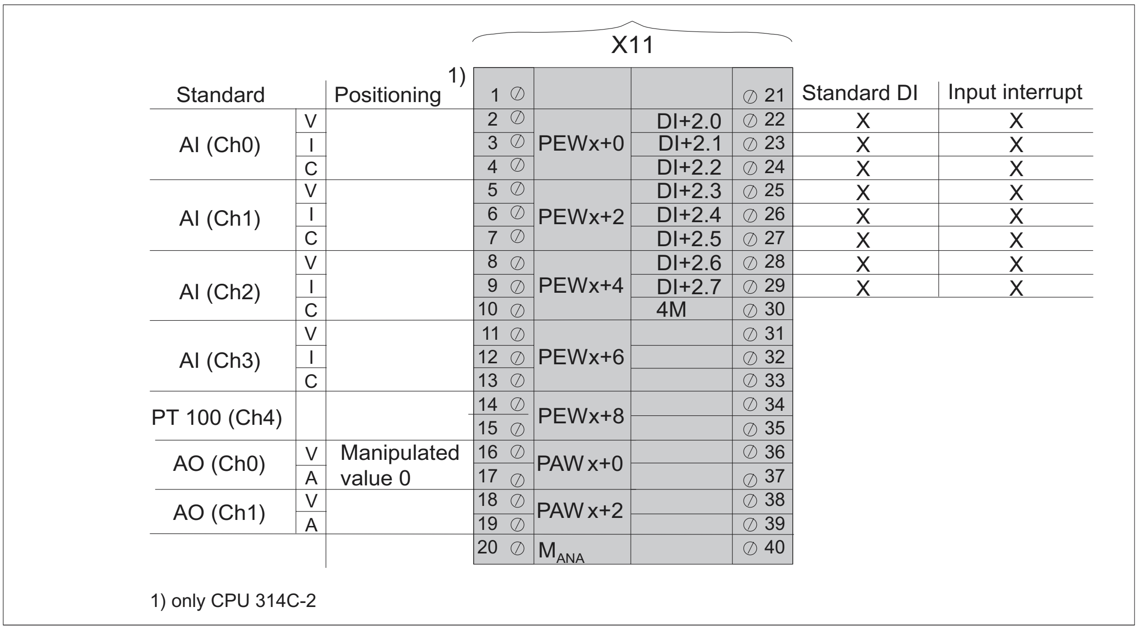


Figure 7-4 Block diagram of integrated digital I/O of CPUs 313C/313C-2/314C-2



X11

Standard		Positioning 1)					Standard DI	Input interrupt
			1 ∅			∅ 21		
AI (Ch0)	V		2 ∅	PEWx+0	DI+2.0	∅ 22	X	X
	I		3 ∅		DI+2.1	∅ 23	X	X
	C		4 ∅		DI+2.2	∅ 24	X	X
AI (Ch1)	V		5 ∅	PEWx+2	DI+2.3	∅ 25	X	X
	I		6 ∅		DI+2.4	∅ 26	X	X
	C		7 ∅		DI+2.5	∅ 27	X	X
AI (Ch2)	V		8 ∅	PEWx+4	DI+2.6	∅ 28	X	X
	I		9 ∅		DI+2.7	∅ 29	X	X
	C		10 ∅		4M	∅ 30		
AI (Ch3)	V		11 ∅	PEWx+6		∅ 31		
	I		12 ∅			∅ 32		
	C		13 ∅			∅ 33		
PT 100 (Ch4)			14 ∅	PEWx+8		∅ 34		
			15 ∅			∅ 35		
AO (Ch0)	V	Manipulated value 0	16 ∅	PAW x+0		∅ 36		
	A		17 ∅			∅ 37		
AO (Ch1)	V		18 ∅	PAW x+2		∅ 38		
	A		19 ∅			∅ 39		
			20 ∅	M_{ANA}		∅ 40		

1) only CPU 314C-2

Figure 7-5 CPUs 313C/314C-2: Pin-out of the integrated AI/AO and DI (Connector X11)

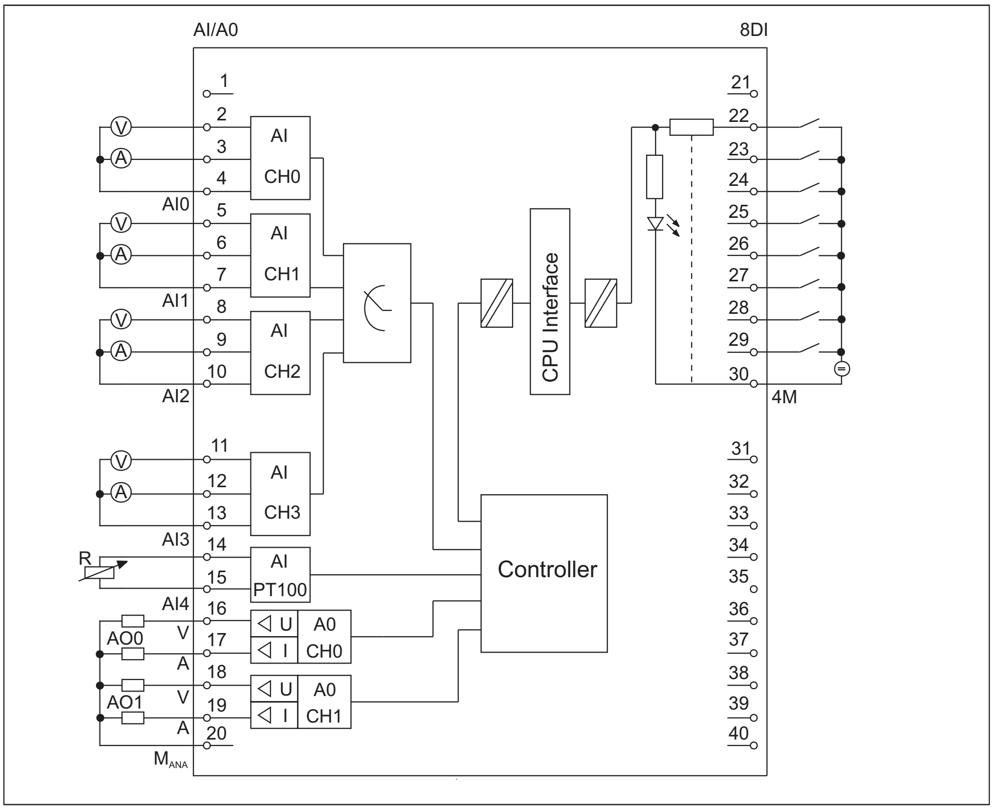


Figure 7-6 Block diagram of integrated digital/analog I/O of CPUs 313C/314C-2

Simultaneous use of technological functions and standard I/O

Technological functions and standard I/O can be used simultaneously with appropriate hardware. For example, you cannot use digital inputs as standard DI, if they are in use by counting functions.

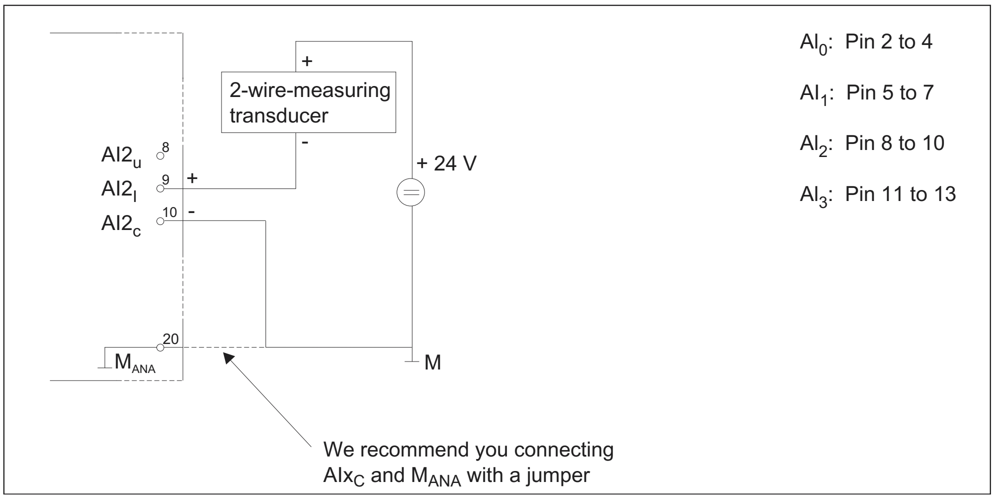
Read access to inputs used by technological functions is possible. Write access to outputs used by technological functions is not possible.

Possible effects on CPU performance are described in Chapter *Cycle/Response Times*.

7.2 Analog I/O

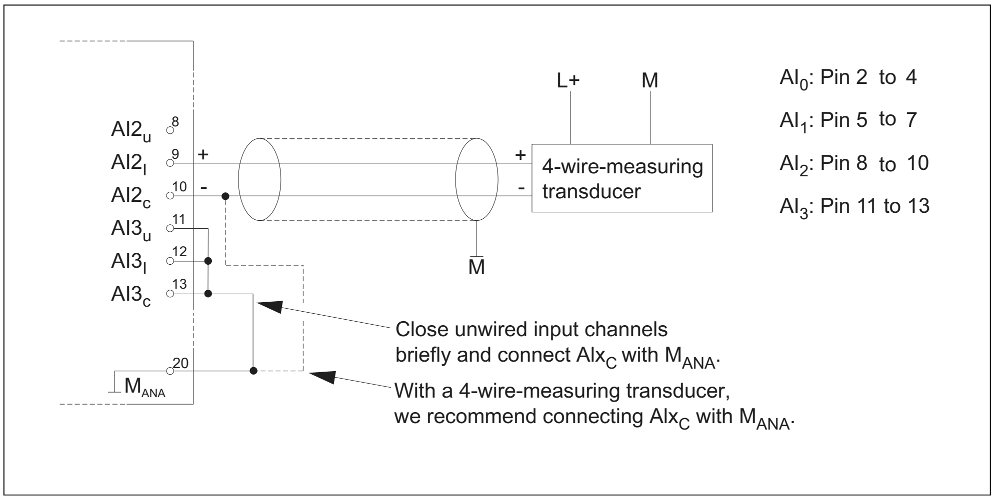
Wiring of the Current/Voltage Inputs

The figure below shows the wiring diagram of the current/voltage inputs operated with 2-/4-wire measuring transducers.



We recommend you connecting AIx_C and M_{ANA} with a jumper

Figure 7-7 Connection of a 2-wire measuring transducer to an analog current/voltage input of CPU 313C/314C-2



Close unwired input channels briefly and connect AIx_C with M_{ANA}.

With a 4-wire-measuring transducer, we recommend connecting AIx_C with M_{ANA}.

Figure 7-8 Wiring of an analog current/voltage input of CPU 313C/314C-2 with 4-wire measuring transducer

Measurement principle

CPUs 31xC use the measurement principle of actual value encoding. Here they operate with a sampling rate of 1 kHz, that is, a new value is available at the input word register once every millisecond. This value can then be read via user program (e.g. L PEW). The "old" value is read again if the access times are lower than 1 ms.

Integrated hardware low-pass filter

An integrated low-pass filter attenuates the analog input signals at channel 0 to 3. They are attenuated according to the trend in the figure below.

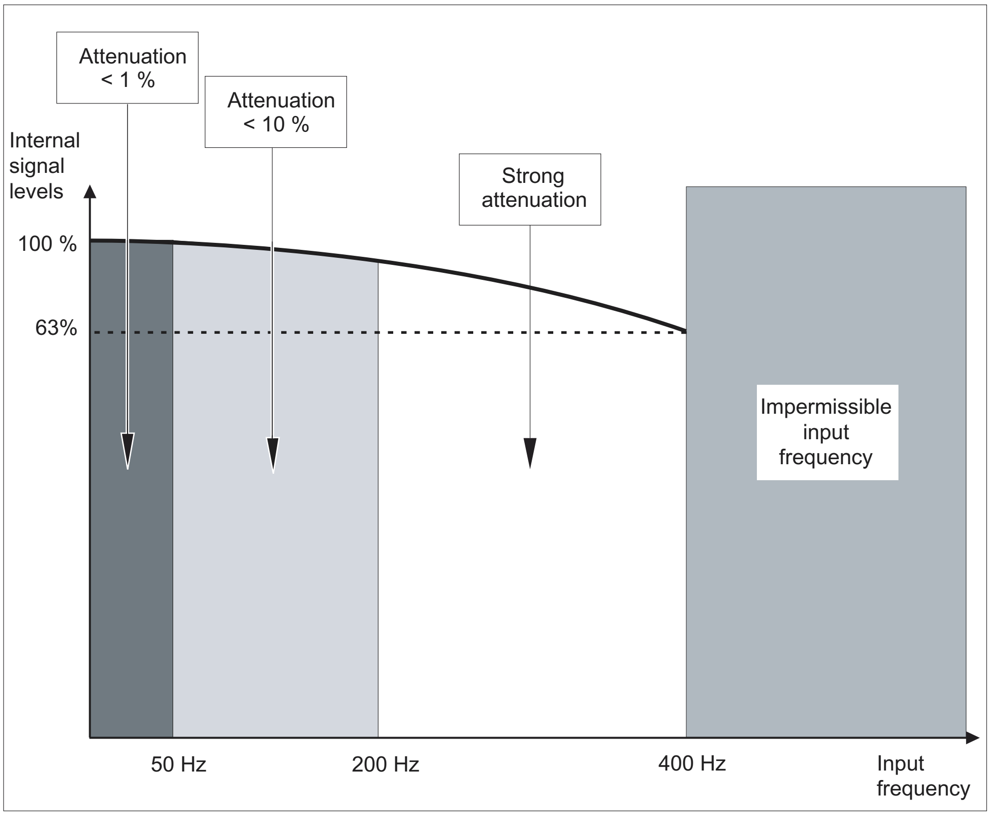


Figure 7-9 Low-pass characteristics of the integrated filter

Note

The frequency of the input signal must not exceed 400 Hz.

Input filters (Software filter)

The current / voltage inputs have a software filter for the input signals that can be programmed with STEP 7. This software filter attenuates the configured interference frequencies (50/60 Hz) and multiples thereof.

The selected interference suppression also determines the integration time.
At an interference suppression of 50 Hz the software filter forms the average based on the last 20 measurements and saves the result as measurement value.

You can suppress interference frequencies (50 Hz or 60 Hz) according to the parameters set in STEP 7. A setting of 400 Hz will not suppress interference.

An integrated low-pass filter attenuates analog input signals of channel 0 to 3.

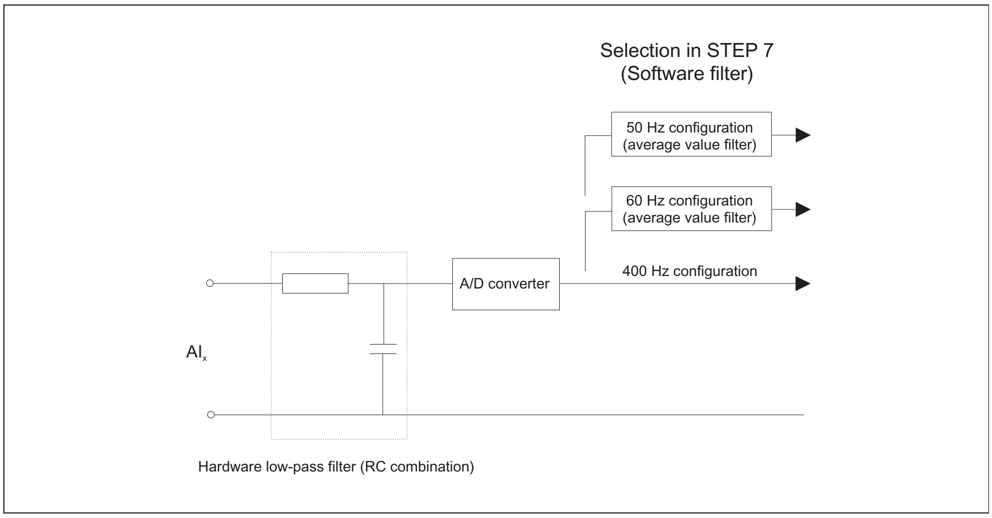


Figure 7-10 Principle of interference suppression with STEP 7

In the two graphics below we illustrate how the 50 Hz and 60 Hz interference suppression work

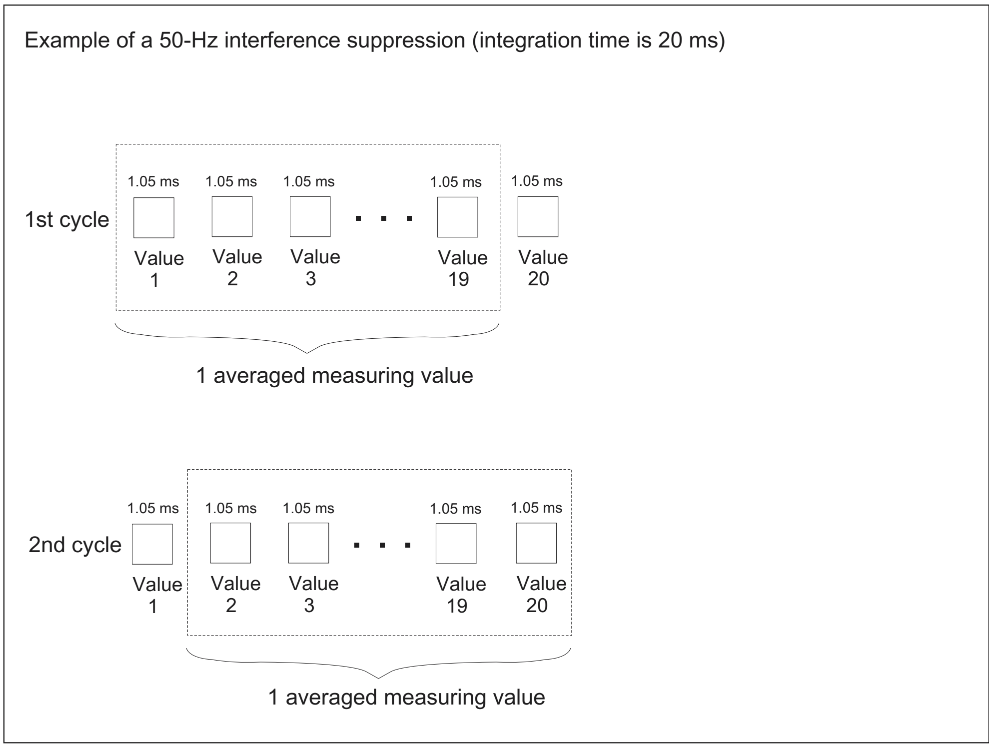


Figure 7-11 50 Hz interference suppression

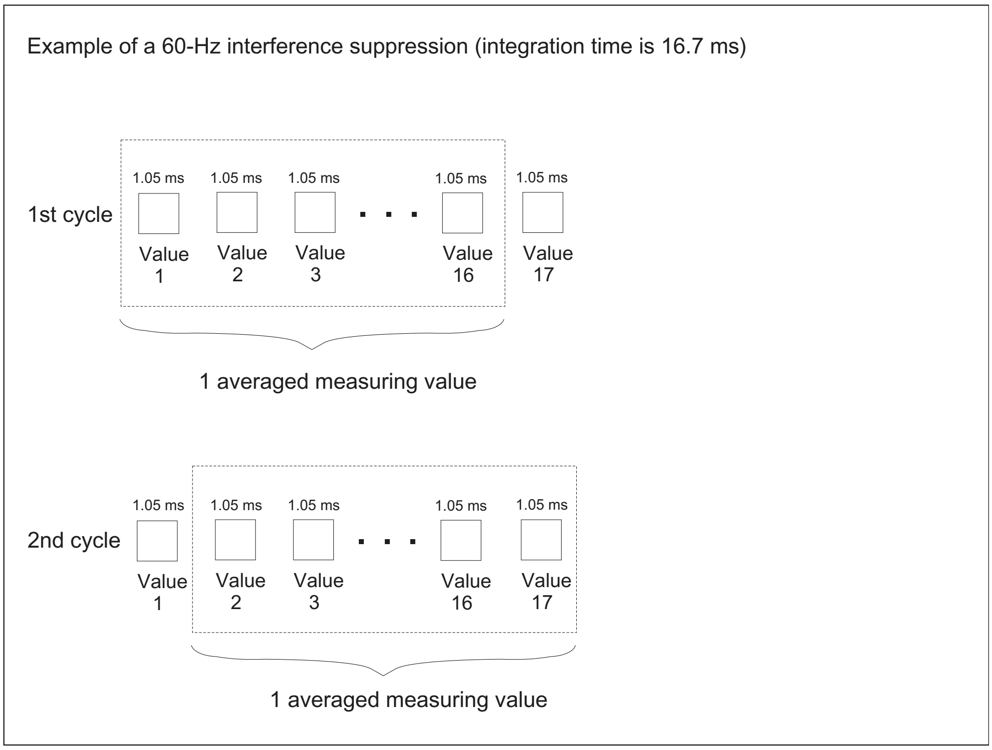


Figure 7-12 60 Hz interference suppression

Note

If the interference frequency is not 50/60 Hz or a multiple thereof, the input signal must be filtered externally,
in which case, 400 Hz must be set as the interference suppression for the affected input. This is equivalent to "disabling" the software filter.

Inputs not connected

The three inputs of a current/voltage analog output channel which are not connected should be shorted and connected to M_{ANA} (Pin 20 of the front connector). This ensures maximum interference resistance for these analog inputs.

Outputs not connected

In order to take unused analog outputs off power, you must disable and leave them open when you assign parameters in *STEP 7*.

Cross-reference

Details (e.g. display and processing of analog values) are found in Chapter 4 of the Reference Manual *Module Data*.

7.3 Configuration

Introduction

Configure the integrated I/O of CPUs 31xC in *STEP 7*. You must always configured them when the CPU is in STOP mode. The generated parameters are downloaded from the PG to the S7-300 and written to CPU memory .

You could also change the parameters with SFC55 in you user program (see the Reference Manual *System and Standard Functions*). Here, refer to the structure of data record 1 for the respective parameters.

Parameters of Standard DI

The table below gives you an overview of the parameters for standard digital inputs.

Table 7-1 Parameters for the standard DI

Parameters	Range of values	Default	Range of efficiency
Input delay (ms)	0.1/0.5/3/15	3	Channel Group

The table below gives you an overview of parameters for operating digital inputs as interrupt inputs .

Table 7-2 Parameters for the interrupt inputs

Parameters	Range of values	Default	Range of efficiency
Interrupt input	Disabled / positive edge	disabled	digital input
Interrupt input	Disabled / negative edge	disabled	digital input

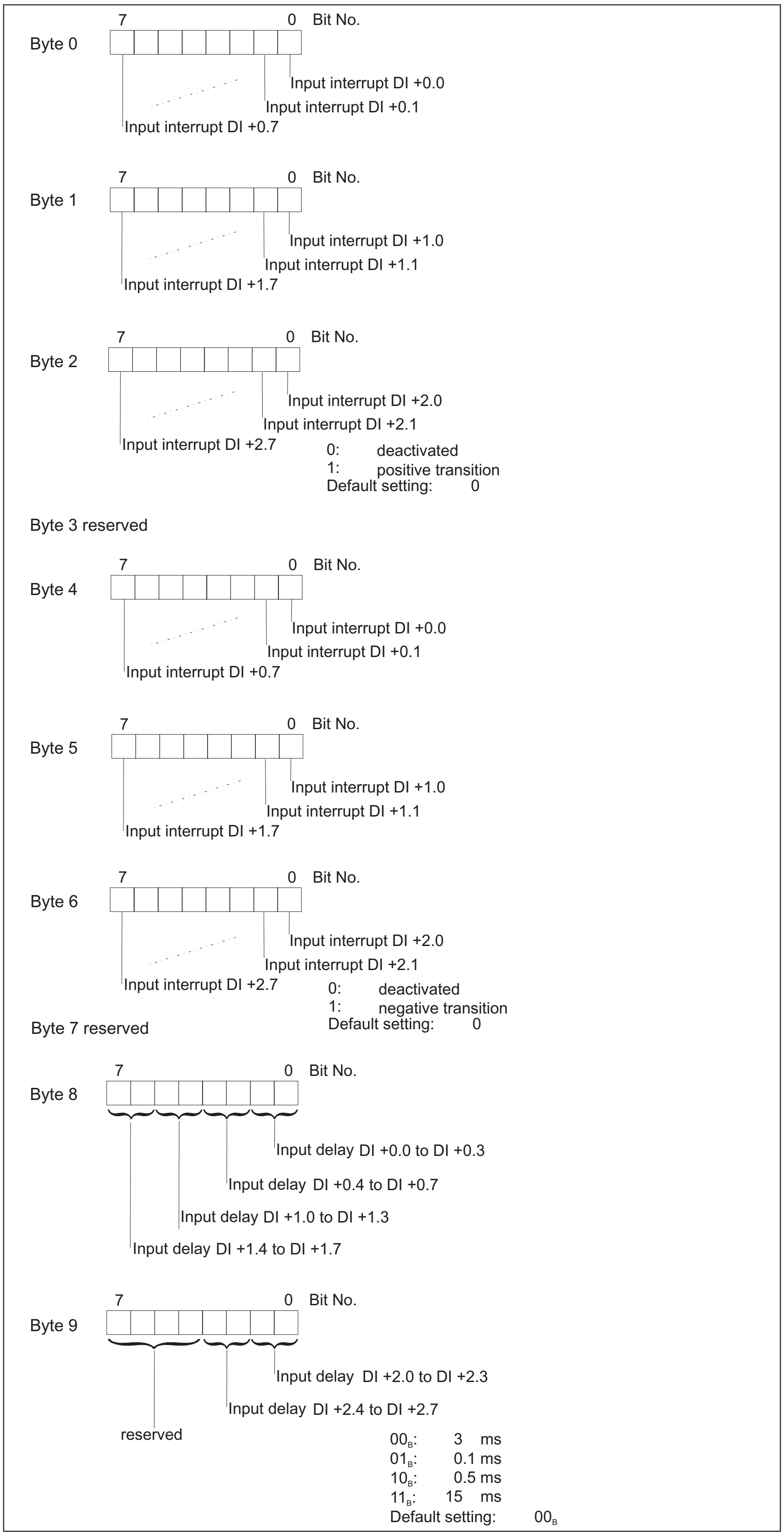


Figure 7-13 Structure of Data Record 1 for Standard DI and Interrupt Inputs (length is 10 bytes)

Parameters of standard DO

There are no parameters for standard digital outputs.

Parameters of standard AI

The following table gives you an overview of the parameters for standard analog inputs (see also Chapter 4.3 in the Reference Manual *Module Data*).

Table 7-3 Parameters for the standard AI

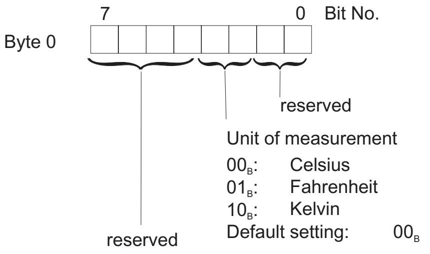
Parameters	Range of values	Default	Range of efficiency
Integration time (ms) Interference suppression (Hz) (channel 0 to 3)	2.5/16.6/20 400/60/50	20 50	Channel Channel
Measurement range (channel 0 to 3)	disabled / +/- 20 mA/ 0 ... 20 mA/ 4 ... 20 mA/ +/- 10 V/ 0 ... 10 V	+/- 10 V	Channel
Type of measurement (channel 0 to 3)	Disabled/ U voltage/ I current	U voltage	Channel
Unit of measurement (channel 4)	Celsius/Fahrenheit / Kelvin	Celsius	Channel
measurement range (Pt 100 input; channel 4)	Disabled/ Pt 100/600 Ω	600 Ω	Channel
Type of measurement (Pt 100 input; channel 4)	disabled / resistance/ thermal resistance	Resistance	Channel

Parameters of standard AO

The table below gives you an overview of standard analog output parameters (see also Chapter 4.3 in the Reference Manual *Module Data*).

Table 7-4 Parameters for the standard AO

Parameters	Range of values	Default	Range of efficiency
Output range (channel 0 to 1)	disabled / +/- 20 mA/ 0 ... 20 mA/ 4 ... 20 mA/ +/- 10 V/ 0 ... 10 V	+/- 10 V	Channel
Type of output (channel 0 to 1)	Disabled/ U voltage/ I current	U voltage	Channel

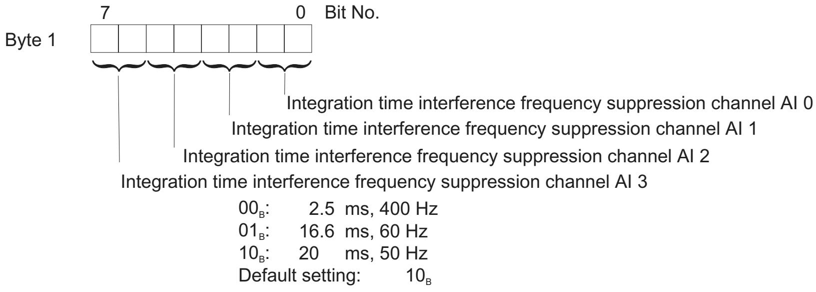


Bits 7 to 4: reserved

Bits 3 to 2: Unit of measurement

00_B: Celsius
01_B: Fahrenheit
10_B: Kelvin
Default setting: 00_B

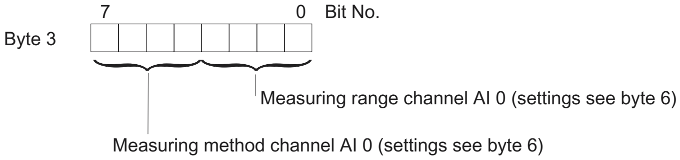
Bits 1 to 0: reserved



Integration time interference frequency suppression channel AI 0
Integration time interference frequency suppression channel AI 1
Integration time interference frequency suppression channel AI 2
Integration time interference frequency suppression channel AI 3

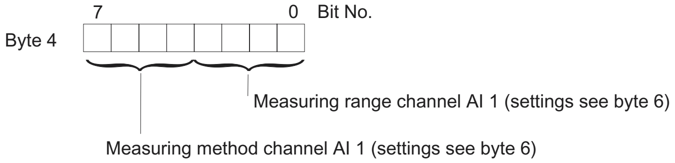
00_B: 2.5 ms, 400 Hz
01_B: 16.6 ms, 60 Hz
10_B: 20 ms, 50 Hz
Default setting: 10_B

Byte 2 reserved



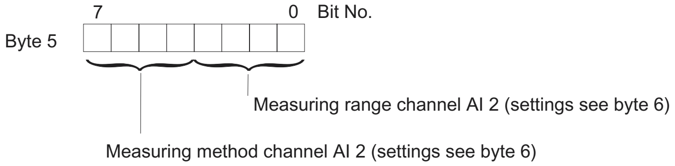
Measuring range channel AI 0 (settings see byte 6)

Measuring method channel AI 0 (settings see byte 6)



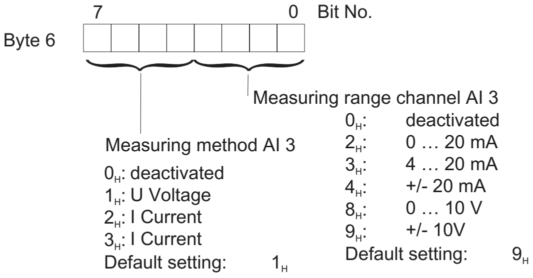
Measuring range channel AI 1 (settings see byte 6)

Measuring method channel AI 1 (settings see byte 6)



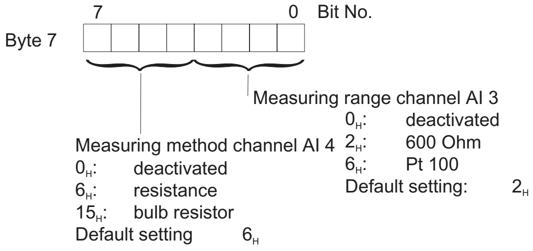
Measuring range channel AI 2 (settings see byte 6)

Measuring method channel AI 2 (settings see byte 6)



Measuring range channel AI 3
0_H: deactivated
2_H: 0 … 20 mA
3_H: 4 … 20 mA
4_H: +/- 20 mA
8_H: 0 … 10 V
9_H: +/- 10V
Default setting: 9_H

Measuring method AI 3
0_H: deactivated
1_H: U Voltage
2_H: I Current
3_H: I Current
Default setting: 1_H



Measuring range channel AI 3
0_H: deactivated
2_H: 600 Ohm
6_H: Pt 100
Default setting: 2_H

Measuring method channel AI 4
0_H: deactivated
6_H: resistance
15_H: bulb resistor
Default setting 6_H

Byte 8 to 10 reserved

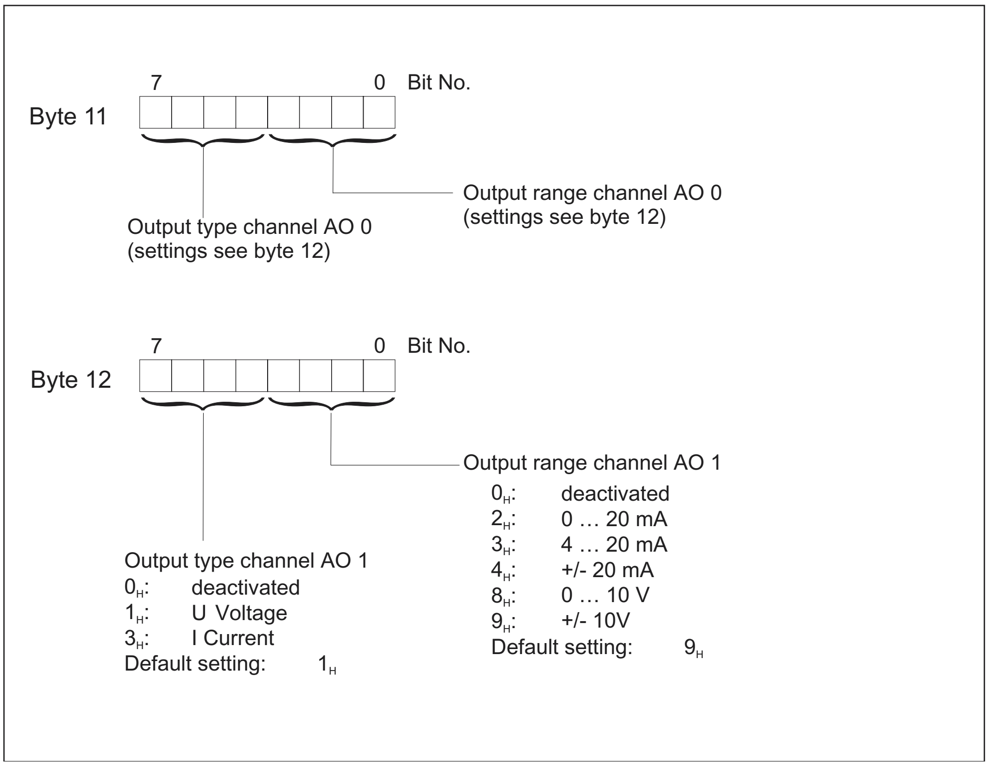


Figure 7-14 Structure of record 1 for standard AI/AO (length of 13 bytes)

Parameters for Technological Functions

The parameters for the respective function are found in the Manual *Technological Functions*.

7.4 Interrupts

Interrupt inputs

All digital inputs of the on-board I/O of CPUs 31xC can be used as interrupt inputs.

You can specify interrupt behavior for each individual input in your parameter declaration. Options are:

- no interrupt
- interrupt at the positive edge
- interrupt at the negative edge
- interrupt triggered at the positive and negative edge

Note

If the rate of incoming interrupts exceeds the handling capacity of OB40, every channel maintains one event. Further events (interrupts) will be lost, without diagnostics or explicit message.

Start information for OB40

The table below shows the relevant temporary variables (TEMP) of OB40 for the interrupt inputs of 31xC CPUs. A description of process interrupt OB40 is found in the Reference Manual *System and Standard Functions*.

Table 7-5 Starting information for OB40 relating to the interrupt inputs of the integrated I/Os

Byte	Variable	Data type		Description
6/7	OB40_MDL_ADDR	WORD	B#16#7C	Address of the interrupt-triggering module (Here: Default addresses of the digital inputs)
8 on	OB40_POINT_ADDR	DWORD	see the figure below	Displaying the interrupt triggering integrated inputs

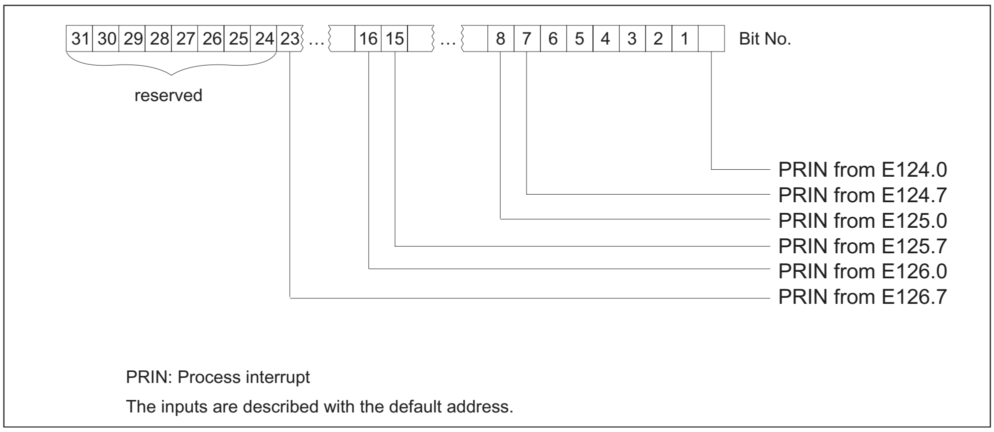


Figure 7-15 Displaying the statuses of CPU 31xC interrupt inputs

7.5 Diagnostics

Standard I/O

Diagnostic data is not available for integrated I/O which is operated as standard I/O (see also the Reference Manual *Module Data*).

Technological functions

Diagnostics options for the respective technological function are found in the Manual *Technological Functions*.

7.6 Digital inputs

Introduction

This chapter contains the specifications for the digital inputs of 31xC CPUs.

The table includes the following CPUs:

- under CPU 313C-2, the CPU 313C-2 DP and CPU 313C-2 PtP
- under CPU 314C-2, the CPU 314C-2 DP and CPU 314C-2 PtP

Specifications

Specifications				
Module-specific data	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Number of inputs	10	24	16	24
• number of these inputs which can be used for technological functions	8	12	12	16
Cable length				
• Unshielded	For standard DIs: max. 600 m For technological functions: no			
• Shielded	For standard DIs: max. 1000 m			
	For technological function at max. counting frequency			
	M 100	M 100	M 100	50 m
Voltage, currents, potentials	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Rated load voltage L+	24V DC			
• Polarity reversal protection	Yes			

Number of inputs which can be controlled simultaneously				
• horizontal assembly				
up to 40 °C	10	24	16	24
up to 60 °C	5	12	8	12
• vertical assembly				
up to 40 °C	5	12	8	12
electrical isolation				
• between the channels and the backplane bus	Yes			
• between the channels	No			
permitted potential difference				
• between different circuits	75 VDC / 60 VAC			
Insulation test voltage	500 VDC			
Current consumption				
• on load voltage L+ (no-load)	–	max. 70 mA	max. 70 mA	max. 70 mA
Status, interrupts, diagnostics	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Status display	one green LED per channel			
Interrupts	• yes, if the corresponding channel is configured as interrupt input • when using technological functions, please refer to the *Technological Functions* Manual.			
Diagnostic functions	• no diagnostics when operated as standard I/O • when using technological functions, please refer to the *Technological Functions* Manual.			
Data for the selection of an encoder for standard DI	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Input voltage				
• Rated value	24V DC			
• For signal "1"	15 V to 30 V			
• For signal "0"	-3 V to 5 V			
Input current				
• For signal "1"	typically 9 mA			

Delay of standard inputs				
• Configurable	yes (0.1 / 0.5 / 3 / 15 ms) You can reconfigure the input delay of the standard inputs during program runtime. Please not that newly set the filter time may only take effect after the previously set filter time has run out.			
• Rated value	3 ms			
For using technological functions: "Minimum pulse width/ minimum pause between pulses at maximum counting frequency"	48 µs	16 µs	16 µs	8 µs
Input characteristic	to IEC 1131, Type 1			
Connection of 2shywire BEROs	Possible			
• permitted quiescent current	max. 1.5 mA			

7.7 Digital outputs

Introduction

This chapter contains the specifications for the digital outputs of 31xC CPUs.

The table includes the following CPUs:

- under CPU 313C-2, the CPU 313C-2 DP and CPU 313C-2 PtP
- under CPU 314C-2, the CPU 314C-2 DP and CPU 314C-2 PtP

Fast Digital Outputs

Technological functions use fast digital outputs.

Specifications

Specifications				
Module-specific data	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Number of outputs	6	16	16	16
• of those are fast outputs	2	4	4	4
	Attention: You cannot connect the fast outputs of your CPU in parallel.			
Cable length				
• Unshielded	max. 600 m			
• Shielded	max. 1000 m			
Voltage, currents, potentials	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Rated load voltage L+	24V DC			
• Polarity reversal protection	Yes			
Total current of outputs (per group)				
• horizontal assembly				
up to 40 °C	max. 2.0 A	max. 3.0 A	max. 3.0 A	max. 3.0 A
up to 60 °C	max. 1.5 A	max. 2.0 A	max. 2.0 A	max. 2.0 A
• vertical assembly				
up to 40 °C	max. 1.5 A	max. 2.0 A	max. 2.0 A	max. 2.0 A
electrical isolation				
• between the channels and the backplane bus	Yes			
• between the channels	No	Yes	Yes	Yes
in groups of	–	8	8	8

Specifications				
permitted potential difference				
• between different circuits	75 VDC / 60 VAC			
Insulation test voltage	500 VDC			
Current consumption				
• with load voltage L+	max. 50 mA	max. 100 mA	max. 100 mA	max. 100 mA
Status, interrupts, diagnostics	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Status display	one green LED per channel			
Interrupts	• no interrupts when operated as standard I/O • when using technological functions, please refer to the *Technological Functions* Manual.			
Diagnostic functions	• no diagnostics when operated as standard I/O • when using technological functions, please refer to the *Technological Functions* Manual.			
Data for the selection of an actuator for standard DI	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Output voltage				
• For signal "1"	min. L+ (-0.8 V)			
Output current				
• For signal "1"				
Rated value	0.5 A			
Permitted range	5 mA to 600 mA			
• For signal "0" (residual current)	max. 0.5 mA			
Load impedance range	48 Ω to 4 kΩ			
Lamp load	max. 5 W			
Parallel connection of 2 outputs				
• for redundant load control	Possible			
• for performance increase	Not possible			
Controlling of digital inputs	Possible			
Switching frequency				
• under resistive load	max. 100 Hz			
• For inductive load to IEC 947-5, DC13	max. 0.5 Hz			
• under lamp load	max. 100 Hz			
• fast outputs under resistive load	max. 2.5 kHz			
Inductive breaking voltage limited internally to	typically (L+) - 48 V			
Short-circuit protection of the output	yes, electronic			
• Response threshold	typically 1 A			

7.8 Analog inputs

Introduction

This chapter contains the specifications for analog outputs of CPUs 31xC.

The table includes the following CPUs:

- under CPU 314C-2, the CPU 314C-2 DP and CPU 314C-2 PtP

Specifications

Specifications		
Module-specific data	**CPU 313C**	**CPU 314C-2**
Number of inputs	4 channels with current/voltage input 1 channel with resistance input	
Cable length		
• Shielded	max. 100 m	
Voltage, currents, potentials	**CPU 313C**	**CPU 314C-2**
Resistance input		
• No load voltage	typically 2.5 V	
• Measurement current	typically 1.8 mA to 3.3 mA	
electrical isolation		
• between the channels and the backplane bus	Yes	
• between the channels	No	
permitted potential difference		
• between the inputs (AI_C) and M_{ANA} (U_{CM})	8.0 VDC	
• between M_{ANA} and $M_{internal}$ (U_{ISO})	75 VDC / 60 VAC	
Insulation test voltage	600 VDC	
Analog value generation	**CPU 313C**	**CPU 314C-2**
Measurement principle	Actual value encoding (successive approximation)	
Integration time/conversion time/resolution (per channel)		
• Configurable	Yes	
• Integration time in ms	2.5 / 16.6 / 20	
• permitted input frequency	max. 400 Hz	
• Resolution (including overdrive)	11 bits + signed bit	
• Suppression of interference frequency f1	400 / 60 / 50 Hz	
Time constant of the input filter	0.38 ms	
Basic processing time	1 ms	

Specifications		
Interference suppression, error limits	**CPU 313C**	**CPU 314C-2**
Interference voltage suppression for f = nx (f1 ± 1 %), (f1 = interference frequency), n = 1, 2		
• Common-mode interference ($_{UCM}$< 1.0 V)	> 40 dB	
• Feedback interference (peak value of the interference < rated value of the input range)	> 30 dB	
Crosstalk between the inputs ($_{UCM}$ = 0 V)	> 50 dB	
Operational error limits (across the temperature range, in relation to input range)		
• Voltage/current	< 1 %	
• Resistance	< 5%	
Basic error limit (operational limit at 25 °C, in relation to input range)		
• Voltage/current	< 0.7 %	
• Resistance	< 3%	
Temperature error (in relation to input range)	± 0.006%/K	
Linearity error (referred to input range)	± 0.06%	
Repeat accuracy (in transient state at 25 °C, in relation to input range)	± 0.06%	
Status, interrupts, diagnostics	**CPU 313C**	**CPU 314C-2**
Interrupts	• no interrupts when operated as standard I/O	
Diagnostic functions	• no diagnostics when operated as standard I/O • when using technological functions, please refer to the *Technological Functions* Manual.	
Encoder selection data	**CPU 313C**	**CPU 314C-2**
Input ranges (rated value)/input resistance		
• Voltage	± 10 V/100 kΩ 0 V to 10 V/100 kΩ	
• Current	± 20 mA/50 Ω 0 mA to 20 mA/50 Ω 4 mA to 20 mA/50 Ω	
• Resistance	0 Ω to 600 Ω/10 MΩ	
• Resistance thermometer	Pt 100/10 MΩ	
permitted continuous input voltage (destruction limit)		
• for voltage inputs	max. 30 V;	
• for current inputs	max. " 2.5 V;	
permitted continuous input current (destruction limit)		
• for voltage inputs	max. " 0.5 mA;	
• for current inputs	max. 50 mA;	

Specifications	
Connection of signal generators	
• for voltage measurement	Possible
• for current measurement	
as 2-wire measuring transducer	possible, with external power supply
as 4-wire measuring transducer	Possible
• for measuring resistance	
with 2-wire connection	possible, without cable resistance compensation
with 3-wire connection	Not possible
with 4-wire connection	Not possible
Linearization of the characteristics trend	by software
• for resistance thermometers	Pt 100
Temperature compensation	No
Technical unit for temperature measurement	Degrees Celsius/Fahrenheit/Kelvin

7.9 Analog outputs

Introduction

This chapter contains the specifications for digital outputs of CPUs 31xC.

The table includes the following CPUs:

- under CPU 314C-2, the CPU 314C-2 DP and CPU 314C-2 PtP

Specifications

Specifications		
Module-specific data	**CPU 313C**	**CPU 314C-2**
Number of outputs	2	
Cable length		
• Shielded	max. 200 m	
Voltage, currents, potentials	**CPU 313C**	**CPU 314C-2**
Rated load voltage L+	24V DC	
• Polarity reversal protection	Yes	
electrical isolation		
• between the channels and the backplane bus	Yes	
• between the channels	No	
permitted potential difference		
• between M_{ANA} and $M_{internal}$ (U_{ISO})	75 VDC / 60 VAC	
Insulation test voltage	600 VDC	
Analog value generation	**CPU 313C**	**CPU 314C-2**
Resolution (including overdrive)	11 bits + signed bit	

Specifications		
Conversion time (per channel)	1 ms	
Settling time		
• with resistive load	0.6 ms	
• With capacitive load	1.0 ms	
• With inductive load	0.5 ms	
Interference suppression, error limits	**CPU 313C**	**CPU 314C-2**
Crosstalk between the outputs	> 60 dB	
Operational error limits (across the temperature range, in relation to output range)		
• Voltage/current	± 1 %	
Basic error limit (operational limit at 25C, in relation to output range)		
• Voltage/current	± 0.7%	
Temperature error (in relation to output range)	± 0.01%/K	
Linearity error (in relation to output range)	± 0.15%	
Repeat accuracy (in transient state at 25 °C, in relation to output range)	± 0.06%	
Output ripple; bandwidth 0 to 50 kHz (in relation to output range)	± 0.1%	
Status, interrupts, diagnostics	**CPU 313C**	**CPU 314C-2**
Interrupts	• no interrupts when operated as standard I/O • when using technological functions, please refer to the *Technological Functions* Manual.	
Diagnostic functions	• no diagnostics when operated as standard I/O • when using technological functions, please refer to the *Technological Functions* Manual.	
Actuator selection data	**CPU 313C**	**CPU 314C-2**
Output range (rated values)		
• Voltage	± 10 V 0 V to 10 V	
• Current	± 20 mA/ 0 mA to 20 mA 4 mA to 20 mA	
Load resistance (within output rating)		
• For voltage outputs	min. 1 kΩ	
Capacitive load	max. 0.1 µF	
• For current outputs	max. 300 Ω	
Inductive load	0.1 mH	
Voltage output		
• Short-circuit protection	Yes	
• Short-circuit current	typically 55 mA	

Specifications	
Current output	
• No load voltage	typically 17 V
Destruction limit for externally applied voltages/currents	
• Output voltage to M_{ANA}	max. 16 V, continuous;
• Current	max. 50 mA;
Connection of actuators	
• for voltage output	
-wire connection	possible, without cable resistance compensation
-wire connection (measuring line)	Not possible
• for current output	
-wire connection	Possible

Information about upgrading to a CPU 31xC or CPU 31x

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Who should read this chapter?

You are already using a CPU from the SIEMENS S7-300 series and now want to upgrade to a new device.

Please note that problems may occur while download your user program to the "new" CPU.

If you have used one of the following CPUs in the past ...

CPU	Order No.	As of version	
		Firmware	**Hardware**
CPU 312 IFM	6ES7 312-5AC02-0AB0 6ES7 312-5AC82-0AB0	1.0.0	01
CPU 313	6ES7 313-1AD03-0AB0	1.0.0	01
CPU 314	6ES7 314-1AE04-0AB0 6ES7 314-1AE84-0AB0	1.0.0	01
CPU 314 IFM	6ES7 314-5AE03-0AB0	1.0.0	01
CPU 314 IFM	6ES7 314-5AE83-0AB0	1.0.0	01
CPU 315	6ES7 315-1AF03-0AB0	1.0.0	01
CPU 315-2 DP	6ES7 315-2AF03-0AB0 6ES7 315-2AF83-0AB0	1.0.0	01
CPU 316-2 DP	6ES7 316-2AG00-0AB0	1.0.0	01
CPU 318-2DP	6ES7 318-2AJ00-0AB0	V3.0.0	03

... then please note if you upgrade to one of the

CPU	Order No.	As of version		Hereafter called
		Firmware	**Hardware**	
CPU 312	6ES7312-1AD10-0AB0	V2.0.0	01	CPU 31xC/31x
CPU 312C	6ES7312-5BD01-0AB0	V2.0.0	01	
CPU 313C	6ES7313-5BE01-0AB0	V2.0.0	01	
CPU 313C-2 PtP	6ES7313-6BE01-0AB0	V2.0.0	01	
CPU 313C-2 DP	6ES7313-6CE01-0AB0	V2.0.0	01	
CPU 314	6ES7314-1AF10-0AB0	V2.0.0	01	
CPU 314C-2 PtP	6ES7314-6BF01-0AB0	V2.0.0	01	
CPU 314C-2 DP	6ES7314-6CF01-0AB0	V2.0.0	01	
CPU 315-2 DP	6ES7315-2AG10-0AB0	V2.0.0	01	
CPU 317-2 DP	6ES7317-2AJ10-0AB0	V2.1.0	01	

SFC 56, SFC 57 and SFC 13 which work asynchronously

Some of the SFCs that work asynchronously, when used on CPUs 312IFM - 318-2 DP, were always, or under certain conditions, processed after the first call ("quasi-synchronous").

On the 31xC/31x CPUs these SFCs actually run asynchronously. Asynchronous processing may cover multiple OB1 cycles. As a result, a wait loop may turn into an endless loop within an OB.

The following SFCs are affected:

- SFC 56 "WR_DPARM"; SFC 57 "PARM_MOD"

  On CPUs 312 IFM to 318-2 DP, these SFCs always work "quasi-synchronously" during communication with centralized I/O modules and always work synchronously during communication with decentralized I/O modules.

Note

If you are using SFC 56 "WR_DPARM" or SFC 57 "PARM_MOD", you should always evaluate the SFC's BUSY bit.

- SFC 13 "DPNRM_DG"

  On CPUs 312 IFM to 318-2 DP, this SFC always works "quasi synchronously" when it is called in OB82. On CPUs 31xC/31x it generally works asynchronously.

Note

In the user program, the job should merely be started in OB 82. The data should be evaluated in the cyclical program, taking account of the BUSY bits and the value returned in RET_VAL.

Tip:

If you are using a CPU 31xC/31x, we recommend that you use SFB 54, rather than SFC 13 "DPNRM_DG".

SFC 20 "BLKMOV"

In the past, this SFC could be used with CPUs 312 IFM to 318-2 DP to copy data from a non runtime-related DB.

SFC 20 no longer has this functionality with CPUs 31xC/31x. SFC83 "READ_DBL" is now used instead.

SFC 54 "RD_DPARM"

This SFC is no longer available on CPUs 31xC/31x. Instead you should use SFC 102 "RD_DPARA", which works asynchronously.

SFCs that may return other results

You can ignore the following points if you only use logical addressing in your user program.

If you use address conversion in your user program (SFC 5 "GADR_LGC", SFC 49 "LGC_GADR"), you must check the assignment of the slot and logical start address for your DP slaves.

- In the past, the diagnostic address of a DP slave was assigned to the slave's virtual slot 2. Since DPV1 was standardized, this diagnostic address has been assigned to virtual slot 0 (station proxy) for CPUs 31xC/31x.
- If the slave has modeled a separate slot for the interface module (e.g. CPU31x-2 DP as an intelligent slave or IM 153), then its address is assigned to slot 2.

Activating / deactivating DP slaves via SFC 12

With CPUs 31xC/31x, slaves that were deactivated via SFC 12 are no longer automatically activated at the RUN to STOP transition. Now they are not activated until they are restarted (STOP to RUN transition).

Interrupt events from decentralized I/Os while the CPU status is STOP

With the new DPV1 functionality (IEC 61158/ EN 50170, volume 2, PROFIBUS), the handling of incoming interrupt events from the distributed I/Os while the CPU status is STOP has also changed.

Previous response by the CPU with STOP status:

With CPUs 312IFM – 318-2 DP, initially an interrupt event was noticed while the CPU was in STOP mode. When the CPU status subsequently returned to RUN, the interrupt was then fetched by an appropriate OB (e.g. OB 82).

New response by the CPU:

With CPUs 31xC/31x, an interrupt event (process or diagnostic interrupt, new DPV1 interrupts) is acknowledged by the decentralized I/O while the CPU is still in STOP status, and is entered in the diagnostic buffer if necessary (diagnostic interrupts only). When the CPU status subsequently returns to RUN, the interrupt is no longer fetched by the OB. Possible slave faults can be read using suitable SLL queries (e.g. read SLL 0x692 via SFC51).

Runtimes that change while the program is running

If you have created a user program that has been fine-tuned in relation to certain processing times, please note the following points if you are using a CPU 31xC/31x:

- the program will run much faster on the CPU 31xC/31x.
- Functions that require MMC access (e.g. system start-up time, program download in RUN, return of DP station, etc.), may sometimes run slower on the CPU 31xC/31x.

Converting the diagnostic addresses of DP slaves

If you are using a CPU 31xC/31x with DP interface as the master, please note that you may have to reassign the diagnostic addresses for the slaves since the changes to the DPV1 standard sometimes require two diagnostic addresses per slave.

- The virtual slot 0 has its own address (diagnostic address of the station proxy). The module status data for this slot (read SLL 0xD91 with SFC 51 "RDSYSST") contains IDs that relate to the entire slave/station, e.g. the station error ID. Failure and restoration of the station are also signaled in OB86 on the master via the diagnostic address of the virtual slot 0.
- With some slaves, the interface module is also modeled as a separate virtual slot (e.g. CPU as an intelligent slave or IM153), and a suitable separate address is assigned to virtual slot 2.
  The change of operating status is signaled in the master's diagnostic interrupt OB 82 via this address for CPU 31xC-2DP acting as an intelligent slave.

Note

Reading diagnostics with SFC 13 "DPNRM_DG":
The originally assigned diagnostic address still works. Internally, *STEP 7* assigns this address to slot 0.

When using SFC51 "RDSYSST", for example, to read module status information or module rack/station status information, you must also consider the change in slot significance as well as the additional slot 0.

Reusing existing hardware configurations

If you reuse the configuration of a CPU 312 IFM to 318-2 DP for a CPU 31xC/31x, the CPU 31xC/31x may not run correctly.

If this is the case, you will have to replace the CPU in the STEP 7 hardware configuration editor. When you replace the CPU, STEP7 will automatically accept all the settings (if appropriate and possible).

Replacing a CPU 31xC/31x

When supplied, the CPU 31xC/31x adds a connecting plug to the power supply connector.

If you replace the CPU 31xC/31x, you no longer have to detach the cables on the CPU: Simply insert a screwdriver with a 3.5 mm blade to the right of the connecting plug. Use this to release the latch and then pull the connecting plug away from the CPU. Once you have replaced the CPU, simply plug the connecting plug back into the power supply connector.

Using consistent data areas in the process image for DP slaves

See also the Consistent data section of the Addressing chapter in the Installation Manual.

Load memory concept for the CPU 31xC/31x

On CPUs 312 IFM to 318-2 DP, the load memory is integrated into the CPU and may be extended with a memory card,

The load memory of the CPU 31xC/31x is located on the micro memory card (MMC), and is retentive. When blocks are downloaded to the CPU, they are stored on the MMC and cannot be lost even in the event of a power failure or memory reset.

Cross-reference

See also the *Memory concept* chapter in the *CPU Data 31xC and 31x manual.*

Note

The user program can only be downloaded and thus the CPU can only be used if the MMC is inserted.

PG/OP functions

With CPUs 315-2 DP (6ES7315-2AFx3-0AB0), 316-2DP and 318-2 DP, PG/OP functions at the DP interface were only possible if the interface was set to active. With CPUs 31xC/31x, these functions are possible at both active and passive interfaces. The performance of the passive interface is considerably lower, however.

Routing for the CPU 31xC/31x as an intelligent slave

If you use the CPU 31xC/31x as an intelligent slave, the routing function can only be used with an actively-configured DP interface.

In the properties of the DP interface in STEP 7, tick the Commissioning / Test mode check box.

Changed retentive response for CPU 317-2 DP

For data blocks for CPU 317-2 DP

- you can set the retentive response in the block properties of the DB (as of STEP 7, V5.2 + SP 1).
- using SFC 82 “CREA_DBL“ -> Parameter ATTRIB, Bit NON_RETAIN, you can specify if the actual values of an OB should be maintained at POWER OFF/ON or STOP-RUN (retentive DB) or if the start values should be read from the load memory (non-retentive DB):

FMs/CPs with their own MPI address in the central rack of a CPU 317-2 DP

All CPUs except for CPU 317-2 DP and CPU 318-2 DP	CPU 317-2 DP and CPU 318-2 DP
If there are FM/CPs with their own MPI address in the central rack of an S7-300, then they are in the exact same CPU subnet as the CPU MPI station.	If there are FM/CPs with their own MPI address in the central rack of an S7-300, then the CPU forms its own communication bus via the backplane bus with these FM/CPs, which are separated from the other subnets. The MPI address of such an FM/CP is no longer relevant for the stations on other subnets. The communication to the FM/CP is made via the MPI address of the CPU.

When exchanging your existing CPU with a CPU 317-2 DP you therefore need to:

- Replace your existing CPU with the CPU 317-2 DP in your STEP7 project.
- Reconfigure the OPs. The control must be assigned again and the destination address must be reassigned (i.e., the MPI address of the CPU 317-2 DP and the slot of the FM in question)
- Reconfigure the project data for FM/CP to be loaded to the CPU.

This is required for the FM/CP in this rack to remain "available" to the OP/PG.

Glossary

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Accumulator

The → CPU uses the accumulator registers as intermediate memory for load, transfer, comparison, calculation and conversion operations.

Address

An address represents the ID for a specific address or address range. Examples: input I12.1; flag word MW25; data block DB3.

Analog Module

Analog modules convert process values (e.g. temperature) into digital values, so that they can be processed by the central processing unit, or convert digital values into analog manipulated variables.

Backplane Bus

The backplane bus is a serial data bus. It supplies power to the modules and is also used by the modules to communicate with each other. Bus connectors interconnect the modules.

Backup Memory

The back-up memory provides a back-up of memory areas for the → CPU without a back-up battery. It backs up a configurable number of timers, counters, memory bits, data bytes and retentive timers, counters, memory bits and data bytes).

Bus

A bus is a communication medium connecting several nodes. Data can be transferred via serial or parallel circuits, that is, via electrical conductors or fiber optic.

Bus segment

A bus segment is a self-contained section of a serial bus system. Bus segments are interconnected using repeaters.

Chassis ground

Chassis ground is the totality of all the interconnected passive parts of a piece of equipment on which dangerous fault-voltage cannot occur.

Clock memory bits

Memory bit which can be used to generate clock pulses in the user program
(1 byte per memory bit).

Note

Note in the case of S7shy300 CPUs that the clock memory byte is not overwritten in the user program.

Code Block

A SIMATIC S7 code block contains part of the **STEP 7** user program. (In contrast: a → Data Block (DB) only contains data.

Communication processor

Communication processors are modules for point-to-point and bus communication.

Compress

The programming device online function “Compress” is used to align all valid blocks contiguously in the RAM of the CPU at the start of the user memory. This eliminates all gaps which arose when blocks were deleted or modified.

Configuration

Assignment of modules to racks/slots and (e.g. for signal modules) addresses.

Consistent data

Data whose contents are related and which should not be separated are known as consistent data.

For example, the values of analog modules must always be handled consistently, that is the value of an analog module must not be corrupted by reading it out at two different times.

Counters

Counters are part of CPU → system memory. The content of "Counter cells" can be modified by **STEP 7** instructions (e.g. up/down count).

CP

→ Communication processor

CPU

Central processing unit of the S7 programmable controller with open and closed-loop control systems, memory, operating system and interface for programming device.

CPU operating system

The CPU OS organizes all functions and processes of the CPU which are not associated to a specific control task.

Cycle time

The cycle time represents the time a → CPU requires to run through the → user program once.

Data block

Data blocks (DB) are data areas in the user program which contain user data. Global data blocks can be accessed by all code blocks while instance data blocks are assigned to a specific FB call.

Data, static

Static data is data which can only be used within a function block. The data is saved in an instance data block belonging to the function block. The data stored in the instance data block is retained until the next function block call.

Data, temporary

Temporary data is local data of a block that is stored in the L stack during block execution and no longer available after execution.

Delay interrupt

→ Interrupt, Delay

Diagnostics buffer

The diagnostic buffer is a buffered memory area in the CPU in which diagnostic events are stored in the order of their occurrence.

Diagnostics

→ System Diagnostics

Diagnostic Interrupt

Modules capable of diagnostics operations report detected system errors to the

→ CPU via diagnostic interrupts.

DP Master

A → master which behaves in accordance with EN 50170, Part 3 is known as a DP master.

DP slave

A → slave operated on PROFIBUS with PROFIBUS-DP protocol and in accordance with EN 50170, Part 3 is referred to as DP slave.

DPV1

The designation DPV1 means extension of the functionality of the acyclical services (to include new interrupts, for example) provided by the DP protocol. The DPV1 functionality has been incorporated into IEC 61158/EN 50170, volume 2, PROFIBUS.

Electrically isolated

The reference potential of the control and on-load power circuits for isolated I/Os is galvanically separated; e.g. by optocouplers, relay contact or transformer. Input/output circuits can be connected to a common potential.

Equipotential bonding

Electrical connection (equipotential bonding conductor) which gives the bodies of electrical equipment and external conducting bodies the same or approximately the same potential, in order to prevent disturbing or dangerous voltages from being generated between these bodies.

Error display

One of the possible responses of the operating system to a → runtime error is to display the error. The other possible responses are: → error response in the user program, CPU STOP.

Error handling via OB

When the operating system detects a specific error (e.g. access error with **STEP 7**), it calls a dedicated organization block (Error OB) that determines subsequent CPU response.

Error response

Response to a → runtime error. The operating system can respond in the following ways: transition of the PLC to STOP mode, call of an organization block in which the user can program an error response or display.

External power supply

Power supply for the signal and function modules and the I/O connected to them.

FB

→ Function block

FC

→ Function

Flash EPROM

FEPROMs are the same as electrically erasable EEPROMS in that they can retain data in the event of a power failure, but they can be erased much more quickly (FEPROM = Flash Erasable Programmable Read Only Memory). They are used on → Memory Cards.

Floating potential

No galvanic connection to ground.

FORCE

The Force function is used to assign fixed values to certain variables from a user program or CPU (including I/Os).

In this context, please note the limitations listed in the *Overview of the test functions* section in the chapter entitled *Test functions, diagnostics and troubleshooting* in the *S7-300 Installation* manual

Function

According to IEC 1131-3 a function is a → code block that contains no → statical data. A function allows parameters to be passed in the user program. Functions are therefore suitable for programming frequently occurring complex functions, e.g. calculations.

Function block

According to IEC 1131-3, a function block is a → code block that contains → static data. An FB allows the user program to pass parameters. Function blocks are therefore suitable for programming complex functions, e.g. closed-loop controls, mode selections, which are repeated frequently.

Functional grounding

Grounding which has the sole purpose of safeguarding the intended function of electrical equipment. With functional grounding you short-circuit interference voltage which would otherwise have an unacceptable impact on equipment.

GD circuit

A GD circle encompasses a number of CPUs which exchange data by means of global data communication and which are used as follows:

- One CPU broadcasts a GD packet to the other CPUs.
- One CPU sends and receives a GD packet from another CPU.

A GD circuit is identified by a GD circuit number.

GD Element

A GD element is generated by assigning shared → global data. It is identified by a unique global data ID in the global data table.

GD packet

A GD packet can consist of one or more GD objects which are transmitted together in a frame.

Global data

Global data can be addressed by any → code block (FC, FB, OB). Specifically, the bit memory M, inputs I, outputs A, timers, counters, and data blocks DB. Global data can be accessed absolutely or symbolically.

Global data communication

Global data communication is a procedure used to transfer → global data between CPUs (without CFBs).

Ground

The conductive earth whose electrical potential can be set equal to zero at any point.

Ground potential can be different to zero in the area of grounding electrodes. The term “reference ground” is frequently used to describe this situation.

Grounding

To ground means to connect an electrically conducting component to the grounding electrode (one or more conducting components which have a very good contact with the earth) across a grounding system.

GSD file (device master file)

The device master file (GSD file) stores all slave specific properties. The GSD file format is specified in EN 50170,Volume 2, PROFIBUS.

Instance data block

A DB is automatically generated and assigned to every function block in the **STEP 7** user program. The values of the input, output and in/out parameters are stored in the instance data block, together with local block data.

Interface, multipoint

→ MPI

Interrupt

The CPU's → operating system knows 10 different priority classes for controlling user program execution. These priority classes include interrupts, such as process interrupts. When an interrupt is triggered, the operating system automatically calls an assigned OB. In this OB the user can program the desired response (for example in an FB).

Interrupt, Delay

The delay interrupt belongs to one of the priority classes when processing programs in SIMATIC S7. It is started on expiration of a time generated in the user program. A corresponding organization block is then executed.

Interrupt, diagnostic

→ Diagnostic interrupt

Interrupt, Process

→ Process interrupt

Interrupt, status

A status interrupt can be generated by a DPV1 slave and causes OB55 to be called on the DPV1 master. For detailed information on OB55, see the *Reference Manual "System software for S7-300/400: System and Standard Functions*"

Interrupt, time-of-day

The time-of-day interrupt belongs to one of the priority classes in SIMATIC S7 program processing. It is generated depending on a specific date (or daily) and time-of-day (e.g. 9:50 or hourly, or every minute). A corresponding organization block is then executed.

Interrupt, update

An update interrupt can be generated by a DPV1 slave and causes OB 56 to be called on the DPV1 master. For detailed information on OB 56, see the *Reference Manual "System software for S7-300/400: System and Standard Functions*

Interrupt, vendor-specific

A vendor-specific interrupt can be generated by a DPV1 slave. It causes OB57 to be called on the DPV1 master.

Detailed information on OB 57 can be found in the *Reference Manual "System Software for S7-300/400: System and Standard Functions*"

Interrupt, watchdog

A watchdog interrupt is generated periodically by the CPU in a configurable time pattern. A corresponding → organization block is then executed.

Load memory

Load memory is part of the CPU. It contains objects generated by the programming device. It is implemented either as a plug-in Memory Card or permanently integrated memory.

Local data

→ Data, temporary

Main memory

Work memory is a RAM memory in the → CPU accessed by the processor during user program execution.

Master

Masters in possession of the → Token can send/request data to/from other nodes (= active node).

Memory bits

Memory bits are part of the CPU's → system memory. They store intermediate results of calculations. They can be accessed in bit, byte, word or doubleword units.

Memory Card (MC)

Memory Cards are memory media for CPUs and CPs. They are implemented in the form of → RAM or → FEPROM. An MC differs from an → Micro Memory Card only in its dimensions (MC is approximately the size of a credit card).

Micro Memory Card (MMC)

Micro Memory Cards are memory media for CPUs and CPs. Its smaller dimensions form the only difference compared to the → Memory Card.

Module Parameters

Module parameters are values which can be used to control the response of the module. A distinction is made between static and dynamic module parameters.

MPI

This interface is capable of multipoint communication (MPI). It forms part of the SIMATIC S7 PG interface. It enables multiple-node operation (PGs, text-based displays, OPs) on one or several PLCs. Each node is identified by a unique address (MPI address).

MPI address

→ MPI

Nesting depth

A block can be called from another by means of a block call. Nesting depth is defined as the number of simultaneously called → code blocks.

Non-isolated

The reference potential of the control and on-load power circuits for non-isolated I/Os is electrically interconnected.

OB

→ Organization Blocks

OB priority

The CPU → operating system distinguishes between different priority classes, e.g. cyclic program execution, program execution controlled by process interrupt. Each priority class is assigned → organization blocks (OB) in which the S7 user can program a response. The OBs have different standard priorities which determine the order in which they are executed or interrupted in the event that they are activated simultaneously.

Operating mode

SIMATIC S7 PLC operating modes are: STOP, → STARTUP, RUN.

Organization Blocks

Organization blocks (OBs) form the interface between CPU operating system and the user program. OBs determine the sequence for user program execution.

Parameters

1. Variable of a **STEP 7** code block
2. Variable for declaring module response (one or several per module). All modules have a suitable basic factory setting which can be customized in **STEP 7**.
There are → static parameters and → dynamic parameters

Parameters, dynamic

Unlike static parameters, dynamic parameters of modules can be changed during operation by calling an SFC in the user program, for example limit values of an analog signal input module.

Parameters, static

Unlike dynamic parameters, static parameters of modules cannot be changed by the user program. You can only modify these parameters by editing your configuration in **STEP 7**, e.g. modification of input delay parameters of a digital signal input module.

PG

→ Programming device

PLC

Programmable controllers (PLCs) are electronic controllers whose function is saved as a program in the control unit. The configuration and wiring of the unit are therefore independent of the function of the control system. The PLC has a computer structure; it consists of the → CPU (Central Processing Unit) with memories, I/O modules and internal bus system. The I/Os and the programming language are oriented to control engineering needs.

PLC

→ Programmable controller

PLC

An automation system in the context of SIMATIC S7 → is a programmable logic controller.

Priority class

The S7 CPU operating system provides up to 26 priority classes (or "Program execution levels"). Specific OBs are assigned to these classes. The priority classes determine which OBs interrupt other OBs. Multiple OBs of the same priority class do not interrupt each other. In this case, they are executed sequentially.

Process Image

The process image is part of CPU → system memory. At the start of cyclic program execution, the signal states at the input modules are written to the process image of the inputs. At the end of cyclic program execution, the signal status of the process image of the outputs is transferred to the output modules.

Process interrupt

A process interrupt is triggered by interrupt-triggering modules as a result of a specific event in the process. The process interrupt is reported to the CPU. The assigned → organization block is then processed, according to interrupt priority.

Product version

The product version identifies differences between products which have the same order number. The product version is incremented when forward-compatible functions are enhanced, after production-related modifications (use of new parts/components) and for bug fixes.

PROFIBUS DP

The PLC distributes controls for digital, analog and intelligent modules as well as a wide range of field devices to EN 50170, part 3, for example, drives or valve blocks, to processes at external locations - even across distances exceeding 23 km.

The modules and field devices are connected to the programmable controller via the PROFIBUS-DP fieldbus and addressed in the same way as centralized I/Os.

Programming device

Basically speaking, PGs are compact and portable PCs which are suitable for industrial applications. They are equipped with special hardware and software for SIMATIC PLCs.

RAM

RAM (Random Access Memory) is a semiconductor read/write memory.

Reference ground

→ Ground

Reference potential

Potential with reference to which the voltages of participating circuits are observed and/or measured.

Restart

On CPU startup (e.g. after is switched from STOP to RUN mode via selector switch or with POWER ON), OB100 (restart) is initially executed, prior to cyclic program execution (OB1). On restart, the input process image is read in and the **STEP 7** user program is executed, starting at the first instruction in OB 1.

Retentive memory

A memory area is considered retentive if its contents are retained even after a power loss and transitions from STOP to RUN. The non-retentive area of memory markers, timers and counters is reset following a power failure and a transition from the STOP mode to the RUN mode.

The following can be made retentive:

- flag bits
- S7 timers
- S7 counters
- Data areas

Runtime error

Errors occurred in the PLC (that is, not in the process itself) during user program execution.

Scan rate

The reduction rate determines the send/receive frequency for → GD packets on the basis of the CPU cycle.

Segment

→ Bus segment

SFB

→ System function block

SFC

→ System function

Signal module

Signal modules (SM) form the interface between the process and the PLC. Input and output modules can be digital (input/output module, digital) or analog I/O modules (input/output module, analog)

Slave

A slave may only exchange data with the → Master on request.

START-UP

A STARTUP routine is executed at the transition from STOP to RUN mode. Can be triggered by the → mode selector switch or after power on, or by an operator action on the programming device. An S7–300 performs → a restart.

STEP 7

Programming language for developing user programs for SIMATIC S7 PLCs.

Substitute value

Substitute values are configurable values which output modules transfer to the process when the CPU switches to STOP mode.

In the event of an input access error, a substitute value can be written to the accumulator instead of the input value which could not be read (SFC 44).

System Diagnostics

System diagnostics refers to the detection, evaluation and signaling of errors which occur within the PLC, for example, program errors or module errors. System errors can be displayed with LED indicators or in **STEP 7**.

System function

A system function (SFC) is a → function integrated in the operating system of the CPU that can be called, as required, in the STEP 7 user program.

System Functions Block

A System Function Block (SFB) is a → function block integrated in the CPU operating system. If required, it can be called in the STEP 7 user program.

System memory

The system memory (RAM) is integrated on the central processing unit. System memory contains the address areas (e.g. timers, counters, memory bits) and the data areas required internally by the → operating system (e.g. buffers for communication).

System state list

The system status list contains data describing the current status of an S7shy300. You can always use this list to obtain an overview of:

- The S7shy300 configuration
- the current CPU configuration and configurable signal modules
- Current status and processes in the CPU and configurable signal modules.

Terminating resistor

A terminating resistor is used to terminate data links in order to prevent reflections.

Timer

→Timer

Timers

Timers are part of CPU → system memory. The content of “timer cells” is automatically updated by the operating system, asynchronously to the user program. **STEP 7** instructions are used to define the exact function of the timer cells (for example on-delay) and initiate their execution (e.g. start).

Time-of-day interrupt

→ Interrupt, Time-of-day

Token

Bus access rights

Transmission rate

Data transfer rate (in bps)

User memory

User memory contains → code and → data blocks of the user program. The user memory can be integrated in the CPU or can be provided on plug-in memory cards or memory modules. However, user programs are always executed from → CPU main memory.

User Program

The SIMATIC system distinguishes between the → CPU operating system and user programs. The latter are created with → **STEP 7** programming software, using optional programming languages (LAD and STL). User programs are stored in code blocks. data is stored in data blocks.

Varistor

voltage-dependent resistor

Watchdog Interrupt

→ Interrupt, Watchdog

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