Level 3 Service Manual

Draft 1.1

MOTOROLA™

DIGITAL WIRELESS TELEPHONE

Model A920/A925

UMTS 2100MHz/ PCS 1900MHz/ DCS 1800MHz/ GSM 800MHz

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3G Flash Procedures

Introduction

This document is intended to describe the flashing (software updates) and procedures for 3G terminals. The 3G terminal described in this document will be limited to the A920/A925.

Software updates need to be handled in a controlled manner. Carrier software approvals need to be considered before initializing a flashing procedure. Consult a Motorola representative to ensure that the correct software is programmed.

Software updates allows the service organization to resolve field software issues that customers may be experiencing. Some issues may pertain to specific conditions, therefore, not all units will contain identical software versions.

Hardware Requirements

The following hardware will be required to properly flash the phone.

Power Solution

1. Fully Charged battery (SNN5638A)

2. Full-rate Charger (PSM5049A)

Interface Solution

1. USB PST Tool Kit (S8951)
   USB Cable (SKN6311A)
   Security Key
   Adapter kit
   Power supply (SPN4059A)

PST Software

The Product Support Tool (PST) is used to allow functions such as flashing, flexing, memory transfers, and datalogging. Please contact your local Motorola service representative to obtain user documentation for the PST.

Insure that the Motorola service representative also provides installation documentation, security key requirements, and other related information.

Flash Software Access

Flash software can be accessed by Motorola personnel only. Contact your local Motorola service representative to obtain updated software releases.

In some cases the software may be distributed in ZIP format. The user will need to extract the original (.SHX) file from the ZIP file before is can be used with the PST. WINZIP is the application that can be used to extract the original flash file. For more information on WINZIP, visit,

http://www.winzip.com

Phone Flashing

Before beginning any flashing procedure, always insure that all hardware connections are secured. Refer to figure 1 for flash connection guides. Any intermittent hardware connections may cause the procedure to fail and result in a nonfunctional (Bricked) 3G terminal.

The A920/A925 contains a set of Flash EPROMs for the Adjunct Processor and a separate set of Flash EPROMs for the Baseband Processor. Due to this design, the A920/A925 will require separate Flash files for each processor if a "Combo" file is not provided.

A "Combo" file contains the following files,

Adjunct Processor Flash
Baseband Processor Flash
Customer image flex

Power Solutions

There are two types of power solutions to perform a flashing procedure.

1. Fully Charged Battery Solution
2. Full-Rate Charger Solution (recommended)

If the user decides on using the battery solution, he/she must verify that the battery is fully charged. Failing to verify the capacity of the battery may result in battery depletion prior to completing the flash process. This action may cause unrecoverable failures to the 3G terminal.

Hardware Connection Solution

A920 flash procedures require a USB hardware configuration. Refer to Figure 1 for details.

Figure 1. PST Hardware Configuration

PST Flash Procedure

Use the listed procedure to complete the flash procedure for a 3G terminal. The baseband processor needs to be flashed first. Once the baseband processor flash is successful, follow up with flashing the adjunct processor.

1. Download the desired flash software into the computer.

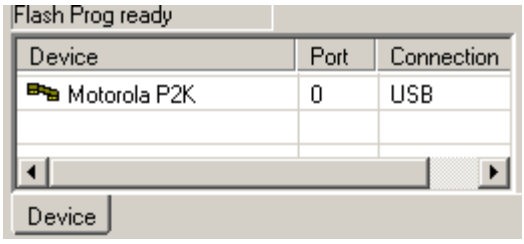
2. Launch the PST application by choosing Start/ Programs/Motorola PST/Flash & Test Commands.

3. Attach battery and connect hardware as illustrated in figure 1.

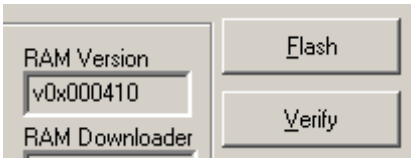
4. Press the Power key and insure that the phone is completely powered on.

5. In the PST application, click on the Browse button and select the desired flash software

6. Select the device that will be flashed.



7. The 3G terminal will be placed in Adjunct flash mode, select the device again to enable the Flash button.



8. Click on the Flash button to begin flashing. DO NOT interrupt any hardware connections during the flash process. Connection interruptions may cause the flashing process to fail and render the 3G terminal non-operational.

9. When flashing is complete, a message will pop up stating," Flash another phone?". Select "No" and waiting for 30 seconds before continuing.

10. Power up the 3G terminal to insure that the flash procedure was successful.

11. On the first power up, the user will be prompted to select a language and calibrate the touch screen.

A920/A925 Special Procedures

There are some variables that need to be considered when updating software for a A920/A925. Improper update procedures may cause the 3G terminal to fail. Always read the release notes for software releases prior to updating the software on a A920/A925.

The user needs to insure that the adjunct and baseband flash files are part of the same build. Also, the user needs to be aware of any step-up procedures. This may require the user to flash an updated bootloader. Step-up procedures can be found in the software release notes.

In order to successfully flash a A920, the following sequence is recommended.

1. Backup user data
2. Flash/upgrade the software
3. Perform a "Master Clear"
4. Restore user data

Flash Procedure Summary

The following is a summary of the procedures for flashing a A920.

1. Launch PST.
2. Connect USB hardware. Insure 3G terminal remains off.
3. Power up 3G terminal.
4. Use the Browse button to open the "Combo" flash file.
5. Select the device for flashing.
6. Select the device again to enable Flash.
7. Click Flash.
8. Click Yes to all the prompts if the user is certain that software being flashed is correct.
9. When flashing is completed, click "No" when prompted, "Flash another phone?."
10. Power cycle phone. Verify functionality.

Handset Test Commands

Introduction

The Handset Test Command mode of the phone is provided primarily for service personnel without access to equipment capable of exercising Test Commands over a computer connection. This mode collects input from the user and packages it in the format required by the Test Command component within the phone.

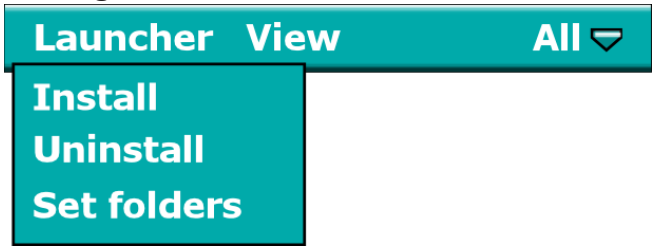
Application Installation*

The user needs to install the Handset Test Command application before it can be accessed. Obtain the file, "testcmdui.sis", file from your local Motorola service representative. Use the following procedure to properly install the handset test command application.

1. Copy the testcmdui file into a memory card (SD or MMC) and insure that the card is inserted in the phone.

2. From the App Launcher screen, select *Install* from the Launcher drop down list

Figure 1. Launcher Menu

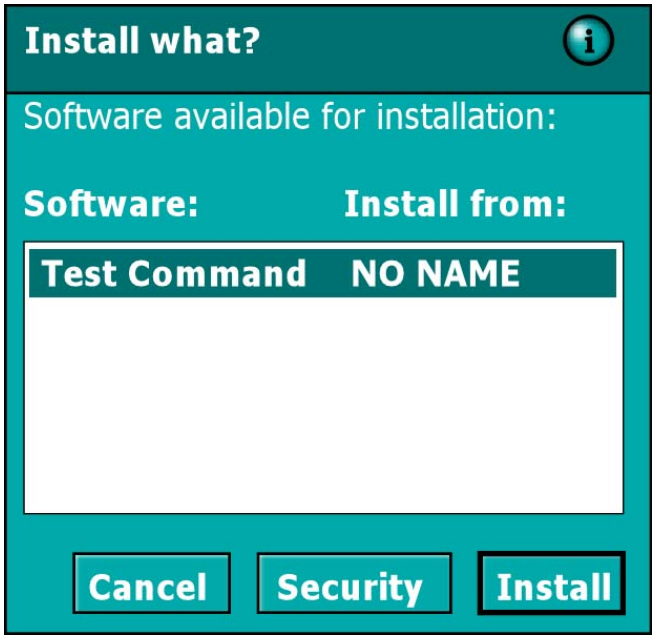


*Test application can only be loaded if application loading is not secured.

3. The user will be prompt with a list of software installation files.

4. Highlight *Test Command* and select *Install*

Figure 2. Install Window



5. When installation is complete, the Test Command icon will be displayed in the App Launcher screen.

Figure 3. Test Command Icon

Handset Test Command Mode Entry

Follow these procedures to launch the handset test command aplication.

1. Under the App Launcher screeen select the Handset test command icon.

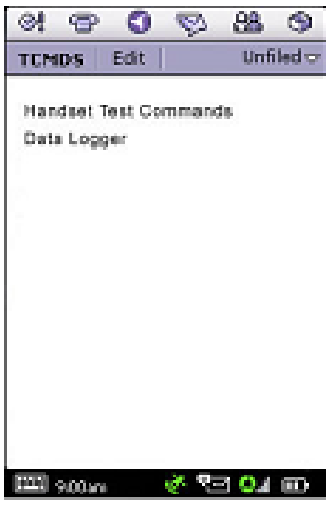
2. The user will then be prompt to input a password

Figure 4. Password Prompt

3. The password is 0HTCMD#
Note: Password is case sensitive

4. Once the application is launched, the user is presented with a list of sub applications

Figure 5. Sub Applications

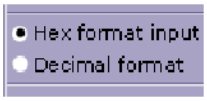


5. Choose Handset Test Commands to enter the Test command Opcode screen

Figure 6. Main Entry Screen

6. Before entering any commands, the user will should select the data input format under the *Edit* menu

Figure 6. Input Format



7. The user can select Hexidecimal or decimal.

8. Under the Edit menu, the user can also clear a field or all fields

9. The *Back* key will return the user to the App Launcher screen

Entry Method

Once the test command mode is entered, two prompts are used to collect command request information from the user. The opcode entry prompt (Figure 5) allows the entry of either an entire command as described in this section, or entry of a partial command. If a partial command is entered, the user will be prompted to enter the remaining required information via an appropriate number of field entry prompts (Figure 7). Selecting Test with no data entered in the opcode or field entry screen will cause a parse error (unless the field is optional).

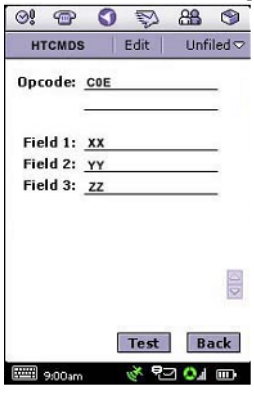
The comma is used to delimit fields on the opcode entry prompt and is not allowed on the field entry prompt. On the opcode entry prompt, it is not legal to have a comma immediately follow another comma.

Opcode entry

The opcode entry prompt allows the user to enter the opcode for the test command, or the opcode plus additional parameters delimited by the "," character.

The user may select *Test* after entering the opcode. If the opcode requires further parameters, the list of Fields shall be shown starting with 1. After all the fields are entered the user shall select *Test*. The results are then shown on the screen.

Figure 7. Fields entered Separately



The *Back* selection will clear the command contents and return the user to the opcode prompt.

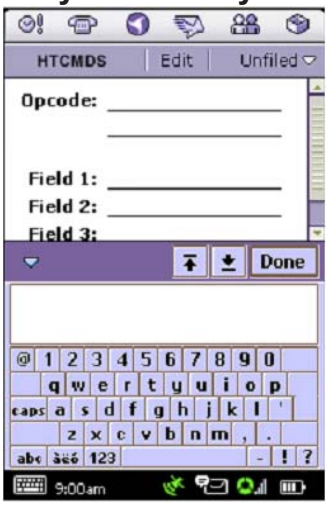
If the user chooses to enter the entire command with the necessary parameters in the Opcode prompt, "," delimiters will be used.

Figure 8. Fields Entered with Delimiter

Entering Data

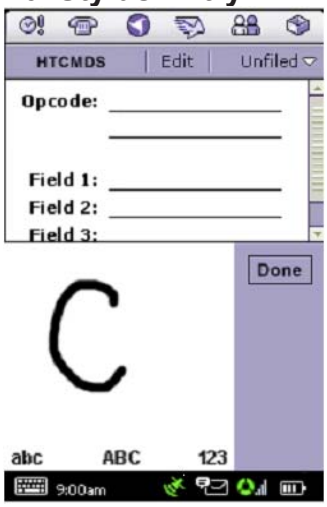
When the User wants to enter the Fields, they shall click the Keyboard Icon at the bottom of the screen to input the values.

Figure 9. Keyboard Entry



They can also use the Stylus, depending on the settings selected by the user in the control panel.

Figure 10. Stylus Entry

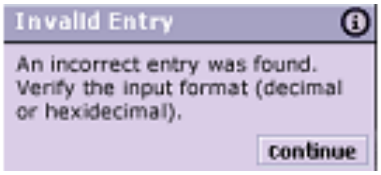


The user shall enter values in Hex or Decimal. The following values shall be allowed for each entry method:

- Hex: A to F and 0 to 9. (not case sensitive)
- Decimal: 0 to 9

When the user presses, "Test", the values shall be checked whether they match the values that are allowed. If not, they shall get an Error Message as follows:

Figure 11. Invalid Entry



After the user presses, "Continue", they shall be taken back to the field where the incorrect entry method was found.

If command processing takes more than 2 seconds a message will display, “Running Test...”

Result Screen

The display of the output shall always be in Hexadecimal Format.

Figure 12. Results Screen

Pressing the "Back" Key shall always take the user back to the Main Entry Screen as shown in Figure 6

Table 1. Handset Test Command Summary

Opcode Hexadecimal	Opcode Decimal	Opcode Mnemonic	Key Entry Format	Op Code Description
0	0	AUD_TN_LST	0 *<Action> * <Tone Identifier>OK	Generate/disable predefined tone
3	3	AUD_CTRL	3 *<Device/Process> * <Action>OK	Control various audio functions; enable/disable vibrator
4	4	AUD_LPB	4 *<Loopback Type> * <Action>OK	Enable audio loopback
5	5	AUD_LVL	5 *<Get/Set>*<Volume>OK	Set audio level
6	6	AUD_PATH	6 *<Input Path>*<Output Path>*<RX Mute>*<TX Mute>OK	Change audio path
7	7	CARRIER	7 * <Option> * <Action> OK	Enable GSM TX carrier
0A	10	CP_MODE	10 * <Set/Get> * <Sub-mode> OK	Set Call Processing Mode
12	18	INVM	18 * <level> OK	Master clear or reset
14	20	LOAD_SYN	20 * <Channel> * 0 OK	Set GSM channel
22	34	RESTART	34 * OK	Generate a software restart
2D	45	SET_RF_PWR	45 * <Power level> OK	Set GSM Power level
36	54	SUSPEND	54 OK	Terminate normal mode and enter test mode
37	55	TST_DISP	55 * <Parameter> * <Parameter Data> OK	Display predefined patterns
39	57	VERSION	57 *<version Type>OK	Retrieve SW version information
3E	62	LEDS	62 * <LED> * <Action> * <Data> OK	Control status LEDs
C0B	3083	WLOAD_SYN	3083 * <RX_FREQ_ID> * <TX_FREQ_ID> OK	Set WCDMA channels
C0E	3086	W_CARRIER	3086 * <Channel ID> * <Action> * <Tx Pwr> * <Max Pwr> * <Min Pwr> * <Data Pattern> * <Channelization> * <Scrambling> * <DPCCH Spread Factor> * <DPDCH Spread Factor> * <Channelization Code> * <Scrambling Code> OK	Enable WCDMA TX carrier

Table 2. Standard Response Codes

Opcode (Hexadecimal)	Opcode (Decimal)	Response Field Definition
0000b (0x00)	0	parse error (no data follows): invalid data length for command
0001b (0x01)	1	parse error (no data follows): inadequate security level for command/parameter
0010b (0x02)	2	parser error (no data follows): command/parameter not supported for current protocol (CDMA, GSM, TDMA)
0011b (0x03)	3	parse error (no data follows): command/parameter not supported for current mode (normal, test mode, handset test mode)
0100b (0x04)	4	parse error (no data follows): unsupported/invalid opcode
0101b (0x05)	5	parse error (no data follows): unsupported/invalid parameter for opcode
0110b (0x06)	6	command response: generic success (no data follows)
0111b (0x07)	7	command response: generic failure (no data follows)
1000b (0x08)	8	command response: data follows
1001b (0x09)	9	unsolicited/multiple response: data follows (sequence tag is 0)
1010b (0x0A)	10	error: couldn't allocate memory
1011b (0x0B)	11	error: internal task error
1100b (0x0C)	12	error: Test Command task timed out waiting for response from another SW component
1101b (0x0D)	13	CDMA: parse error (no data follows): command/parameter not supported for current sub-mode TDMA: command not supported in current Call Stack Test Mode
1110b (0x0E)	14	error: length specified in command header greater than length received by transport layer
1111b (0x0F)	15	error: irrecoverable error; phone state has been lost. Phone is being powered down

Table 3. Field and Parameter descriptions

Opcode (Decimal)	Opcode Mnemonic	Field	Description
0	AUD_TN_LST	Field 1	0 = stop a tone 1 = start a tone
		Field 2	55 through 64 = DTMF tones, refer to table xx for more tones
3	AUD_CTRL	Field 1	0 = Vibrator 2 = Echo canceling 3 = Noise suppressor
		Field 2	0 = Disable 1 = Enable
4	AUD_LPB	Field 1	0 = PCAP loopback 6 = CODEC loopback 7 = VOCODER (speech) loopback
		Field 2	0 = Disable Audio loopback 1 = Enable Audio loopback
		Field 3	This field is valid only for VOCODER loopback 0 = AMR 4.75 1 = AMR 5.15 2 = AMR 5.90 3 = AMR 6.70 4 = AMR 7.40 5 = AMR 7.95 6 = AMR 10.20 7 = AMR 12.20 8 = Full Rate 16 = Enhanced Full Rate 32 = Half Rate
5	AUD_LVL	Field 1	0 = Set the volume specified
		Field 2	0 = lowest, 7 = loudest

Table 3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
6	AUD_PATH	Field 1	0 = As is. 1 = Mute input path 2 = Internal (handset) mic 3 = Ext audio input (CE Bus) 4 = Boom (headset) mic 5 = Ext digital audio (USB) 7 = Bluetooth time slot 1 audio input 8 = Bluetooth time slot 2 audio input 9 = Bluetooth time slot 3 audio input
		Field 2	0 = As is 1 = Mute output path 2 = Internal (handset) Speaker 3 = Alert 4 = Ext audio output (CE Bus) 5 = Speakerphone 6 = Boom (headset) speaker
7	CARRIER	Field 1	0 = All zeroes 1 = All ones 2 = pseudo random sequence w/midamble 0 3 = pseudo random sequence w/midamble 1 4 = pseudo random sequence w/midamble 2 5 = pseudo random sequence w/midamble 3 6 = pseudo random sequence w/midamble 4 7 = pseudo random sequence w/midamble 5 8 = pseudo random sequence w/midamble 6 9 = pseudo random sequence w/midamble 7 10 = RACH BURST 12 = pseudo random sequence w/midamble 0 two time slot 13 = pseudo random sequence w/midamble 0 three time slot
		Field 2	0 = disable 1 = enable

Table 3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
10	CP_MODE	Field 1	0=set submode 1=get submode
		Field 2	5 = GSM 1900 6 = GSM dual band GSM900/GSM1800 8 = WCDMA Region 1 10 = Automatic - Dual mode: WCDMA region 1 and GSM dual band GSM900/GSM1800.a
18	INVM	Field 1	0 = Master Reset 1 = Master Clear
20	LOAD_SYN	Field 1	Channel number in decimal. Valid channel numbers are: • 1-124 (PGSM 900 MHz) • 0, 975-1023 (EGSM 900 MHz) • 512-885 (DCS 1800 MHz) • 512-810 (PCS 1900 MHz)
		Field 2	Reserved for future use and TDMA; set to 0.
34	RESTART	Field 1	As is
45	SET_RF_PWR	Field 1	PA power level (0-19)
54	SUSPEND	Field 1	As is
55	TST_DISP	Field 1	2 = Display Predefined Pattern 9 = Turn On/Off the Front Light
		Field 2 (Data)	Data for 2, 000 = All pixels off (all black) 001 = All pixels on (all white) 005 = Grey scale block: 16 level, Black to white 006 = Horizontal Zebra Line 014 = Eight Color Box Pattern Data for 9, 000 = Front Light Off 001 = Front Light On, Full Intensity

Table 3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
57	VERSION	Field 1	016000 = DSP Version
			017000 = User (login) pf process that created this file
			017001 = Build time (universal) in ISO-8601 format
			017002 = Clearcase view tag name
			017003 = Product base label from Clearcase config spec
			017004 = Product ID
			017005 = Version Number
			017006 = Build commentary
			018000 = Flash Booter version number (P2K Booter Only)
62	LEDS	Field 1	0 = Keypad Backlight LED 3 = Red LED 4 = Green LED
		Field 2	3 = Set duty cycle (Red/Green LEDS Only)
		Field 3	Duty Cycle setup, 000 = Off 012 = ON
3083	WLOAD_SYN	Field 1	UARFCN for Receive Frequency ID. Valid values are between 0 and 16383. If TX_FREQ_ID is set to 0xFFFF, then RX_FREQ_ID must take values between 190*5 and 16383. **Note:** If a valid TX_FREQ_ID will be entered, RX_FREQ_ID must be set to FFFF.
		Field 2	UARFCN for Transmit Frequency ID. Valid values are between 0 and 16383. If it is set to 0xFFFF the TEST_TASK will derive the TX_FREQ_ID from the RX_FREQ_ID. **Note:** If a valid RX_FREQ_ID is entered, TX_FREQ_ID must be set to FFFF.

Table 3. Field and Parameter descriptions - continued

Opcode (Decimal)	Opcode Mnemonic	Field	Description
3086	W_CARRIER	Field 1	Channel identifier (0-16383).
		Field 2	0 = Enable carrier. 1 = Disable carrier.
		Field 3	Initial transmit power (dBm). -128 dBm to 127 dBm
		Field 4	Maximum transmit power (dBm). -128 dBm to 127 dBm
		Field 5	Minimum transmit power (dBm). -128 dBm to 127 dBm
		Field 6	0 = All 0s. 1 = All 1s. 2 = PN9. 3 = PN15.
		Field 7	0 = Disable spreading. 1 = Enable spreading.
		Field 8	0 = Disable scrambling. 1 = Enable long scrambling. 2 = Enable short scrambling.
		Field 9	0 = SF256, slot format 0. 1 = SF256, slot format 1. ... 5 = SF256, slot format 5.
		Field 10	0 = SF256, slot format 0. 1 = SF128, slot format 1. ... 6 = SF4, slot format 6.
		Field 11	Channelization Code Number.
		Field 12	Scrambling Code Number.

Manual Test Procedures

Introduction

The phone allows keypad and computer controlled testing of various digital test parameters.

This chapter includes the keypad/computer functions and recommended equipment setup to use when testing a phone manually.

Call-Processing Tests

Most communications analyzers can simulate a cell site in order to perform automatic call-processing tests. Automatic call processing tests can be performed while the phone is in standby mode.

Refer to the communications analyzer's manual for details about performing call-processing tests. The following call-processing test sequence is recommended:

1. GSM Mobile Originated Call
2. WCDMA Mobile Originated Call
3. GSM handover
4. DCS handover
5. PCS handover

Non-Signalling Test Measurements

In an event that the phone exhibits RF failures that prevent call processing, the service technician may need to perform some non-signalling tests. These tests will provide information regarding which stage of the phone is failing prior to opening the phone for troubleshooting. The following tests will be described in this chapter.

- GSM/DCS/PCS TX Power Output
- GSM RSSI
- WCDMA TX Power Output

The digital phasing parameters are stored in a EPROM on the Transceiver Board. Each transceiver is shipped from the factory with these parameters already calibrated. However, if a board is repaired, these parameters should be measured and, if necessary, adjusted with the GP-Gate System. Checking and adjusting calibration parameters is also useful as a troubleshooting/diagnostic tool to isolate defective assemblies.

GSM/DCS/PCS Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians to perform simulations without accessing the customer's cellular account.

Hardware Requirements

There are various hardware configurations to perform manual call processing procedures. Below, is a list of the various options. All options require the battery to be attached. A GP-gate system can also be used for manual testing. Refer to the GP-gate user's manual for details.

Power Options

- Fully Charged Battery (SNN5639B[1] or equivalent)
- Full-Rate Power Supply (PSM5049A[1])
- Battery Eliminator (5-00-3F-10000[2]) with 2-Wire Adapter (2-00-68-10000[2])
  Note: Requires a single output power supply

Control Interface Options (PCS Only)

- USB Cable (SKN6311A[1])
- Serial Cable (SKN6315A[1]) with CE converter (SYN0279B[1])

Note: If handset test commands are being used, a control interface is not needed.

RF Interface (Everything listed is required)

- SMA/N-type Adapter (0-00-00-40042[2])
- SMA Cable 0.5m (0-00-00-40047[2])
- Repair Fixture (5-00-4T-10000[2])
- USIM (0-00-00-40810[2])

Software Requirements (PCS only)

If PCS call processing procedures are necessary, the user will need to send a test command to the phone prior to beginning the test. The command can be initiated through handset test commands or computer test commands. Software requirements for each method is listed below.

Handset Test Command

- No software needed

Computer Test Command

- Radio Comm (latest release)

[1]Contact your local Motorola dealer for ordering
[2]Contact AMS Software and Elektronik GmbH for ordering

Call Origination (GSM and DCS only)

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200. The procedures can be adopted to any other test box that will be used to perform call processing.

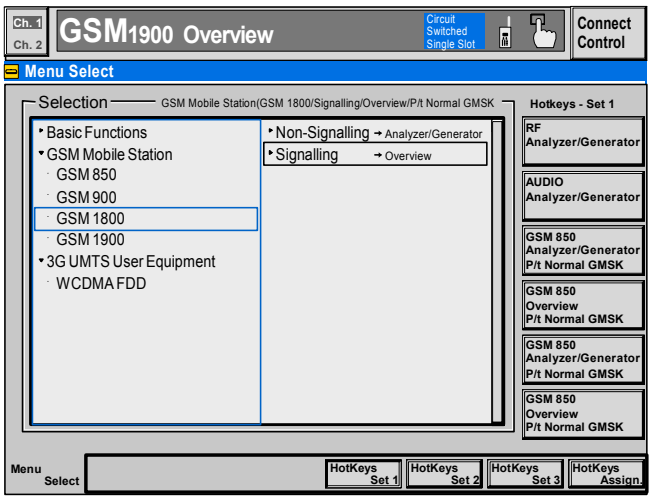
1. Install the test USIM in phone.

2. Connect hardware as illustrated in figure 13.

   Note: Control interface doesn't need to be connected at this time.

3. Setup up the test box for GSM or DCS Signalling

Figure 10. GSM Signalling Setup



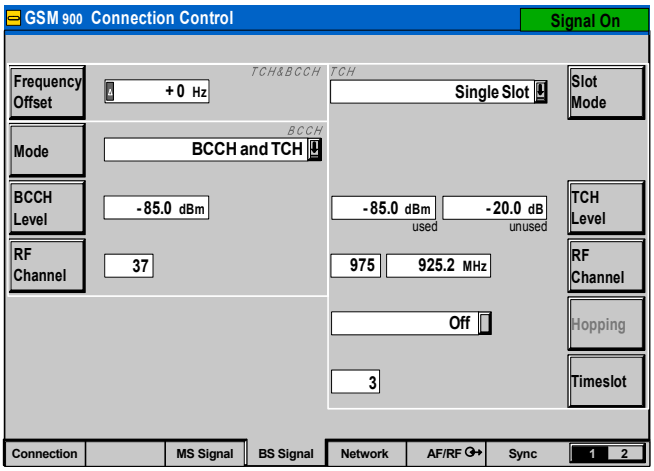
4. Set Broadcast Channel (BCH) to 120 (GSM) or 700 (DCS)

5. Set Broadcast channel level to -85dBm

6. Set Traffic Channel (TCH) to 38 (GSM) or 512 (DCS)

7. Set Traffic channel level to -85dBm

Figure 11. GSM Connection Control



8. Wait until the phone indicates a receive signal

9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 12. GSM Call Connected

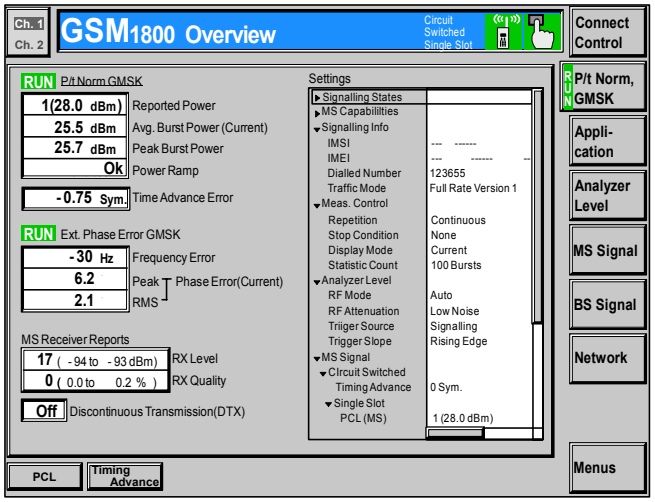
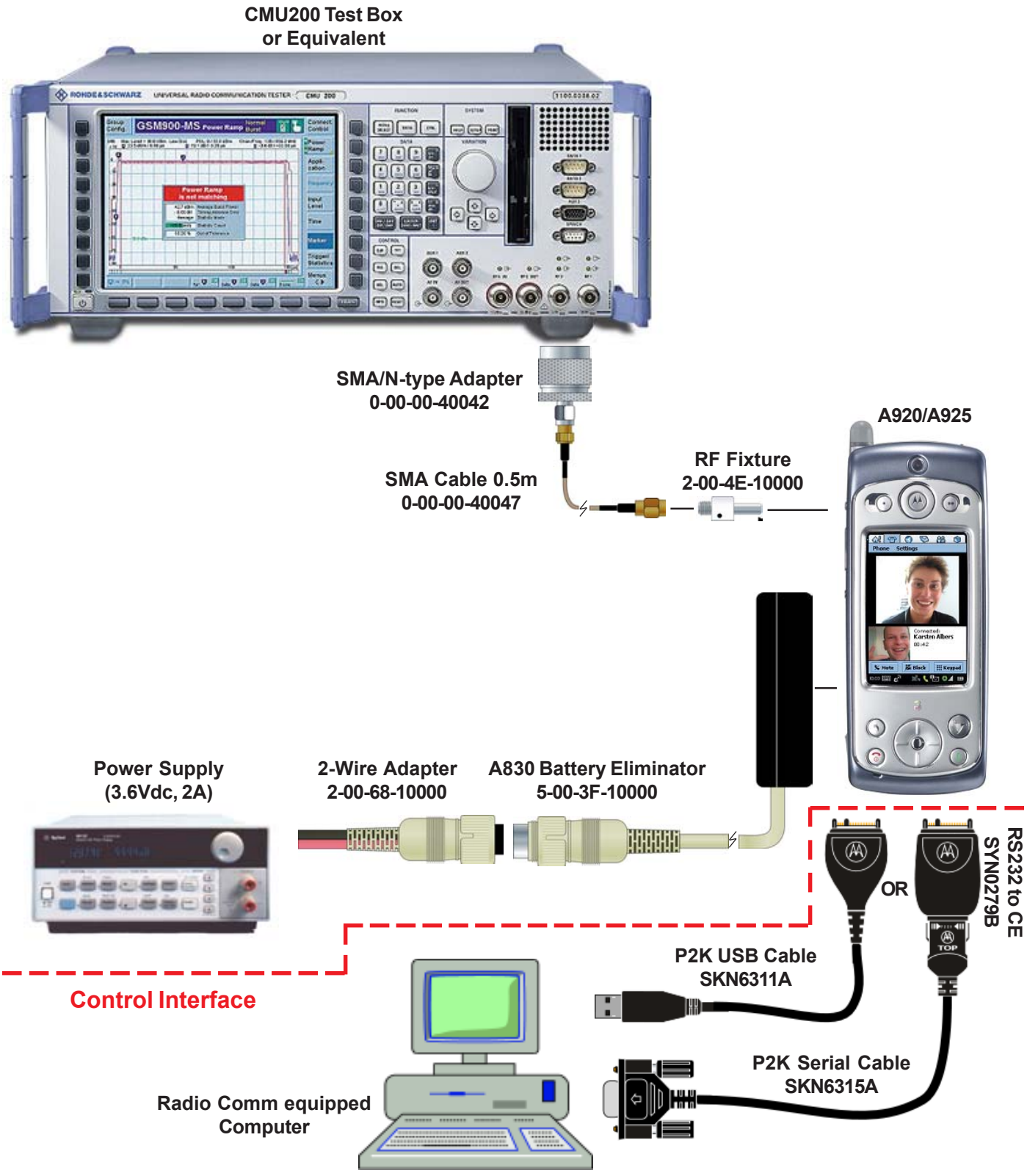


Figure 13. A920 Manual Test Hardware Configuration



Call Origination (PCS Only)

Before beginning, one of the following test command procedures needs to be completed.

Handset Test Command

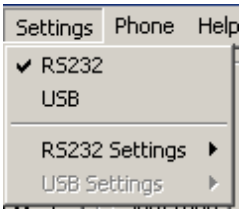
- Power up phone
- Enter the following key sequence
- Menu 0 H T C M D *

- Enter the following test commands in the Opcode screen
- 54 ok SUSPEND
- 10*0*5 CPLOAD, GSM 1900
- Power cycle phone

RadioComm Test Command

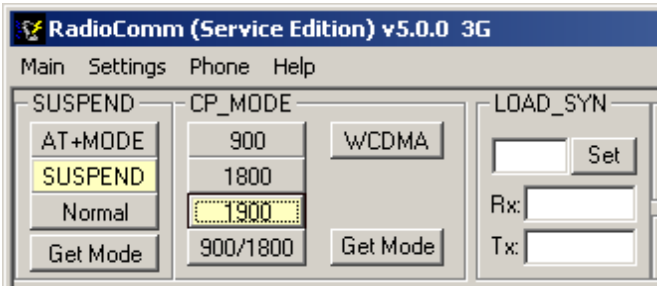
- Connect as illustrated in figure 13
- Power up phone
- Start RadioComm application
- Correctly select Settings option for USB or serial

Figure 14. RadioComm COM Port



- Click on AT+/mode, suspend, CP_Mode 1900, respectfully

Figure 15. Radio Comm Screen



- Power cycle phone

Repeat steps 1 through 10 in the ,“Call Origination (GSM and DCS only),” section with the following modifications,

- Set PCS Signalling
- BCH = 661
- TCH = 512

Once PCS call processing is complete, return the phone to its original state by performing the following procedure,

Handset Test Command

- 54 ok SUSPEND
- 10*0*10 CPLOAD, Dual mode
- Power cycle phone

Computer Test Command (Radio Comm)

- Click on AT+/mode, Suspend, CP_Mode 900/1800, respectfully
- Power cycle phone

Call Test Parameters (GSM/DCS/PCS)

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 4. GSM Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	31	33	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-90	90	Hz
RX Level Error@-105 dBm[2]	1	9	
RX Quality @-105 dBm[2]	0	4	
BER @-105, 10k bits[3]	0	2	%

[1]Power Level = 5
[2]Set BS TCH level to -105 dBm
[3]Set BER TCH level to -105 dBm with 10k bits or 128 Frames

Table 5. DCS Call Parameters

Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	28	32	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-180	180	Hz
RX Level Error@-103 dBm[2]	3	11	
RX Quality @-103 dBm[2]	0	4	
BER @-103, 10k bits[3]	0	2	%

[1]Power Level = 0
[2]Set BS TCH level to -103 dBm
[3]Set BER TCH level to -103 dBm with 10k bits or 128 Frames

Table 6. PCS Call Parameters

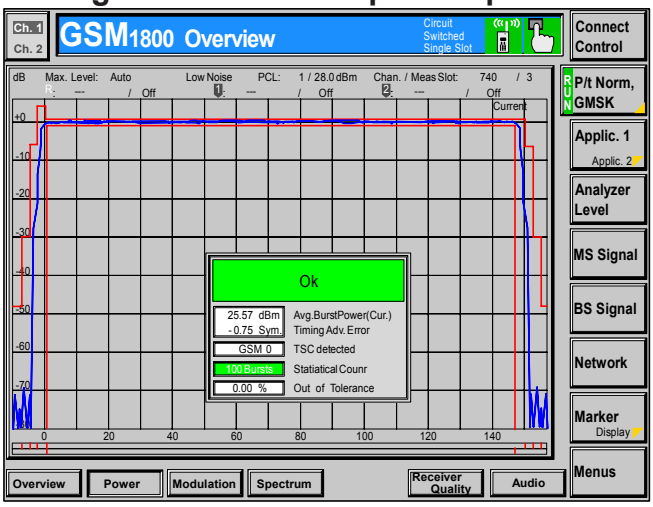
Parameter	Low Limit	High Limit	Unit
Burst Avg Power Out[1]	28	32	dBm
Burst Output Shape	1	1	P/F
Time Advance Error	-1	1	bit/sym
RMS Phase Error	0	5	deg
Peak Phase Error	-20	20	deg
Frequency Error	-190	190	Hz
RX Level Error@-104 dBm[2]	2	10	
RX Quality @-104 dBm[2]	0	4	
BER @-104, 10k bits[3]	0	2	%

[1]Power Level = 0
[2]Set BS TCH level to -104 dBm
[3]Set BER TCH level to -104 dBm with 10k bits or 128 Frames

Burst Output Shape should fall within the standard limits of the Power Ramp.

BER measurements is only required if RX Quality reads a value of 4 or greater.

Figure 16. Burst Output Shape



It is recommended that handover procedures be performed as shown in the following table.

Table 7. GSM/DCS/PCS Handover

Band	From		To	
	Traffic Channel	Power Control	Traffic Channel	Power Control
GSM	975	5	124	19
DCS	512	0	885	15
PCS	512	0	810	15

WCDMA Call Processing

In order to successfully complete a GSM call processing procedure, a test USIM card needs to be available. Test USIM cards have default call parameters that allow users to perform call processing tests through GSM base station simulators. This allows service technicians perform simulations without accessing the customer's cellular account.

Hardware Requirements

Refer to , "Hardware requirements," under, "GSM/DCS/PCS Call Processing." Also Refer to Figure 13.

Software Requirements

None.

Call Origination (WCDMA)

Use the following procedures for call processing. The screen shots are from a Rohde and Schwarz CMU 200 with WCDMA signalling options installed. The procedures can be adopted to any other test box that will be used to perform call processing.

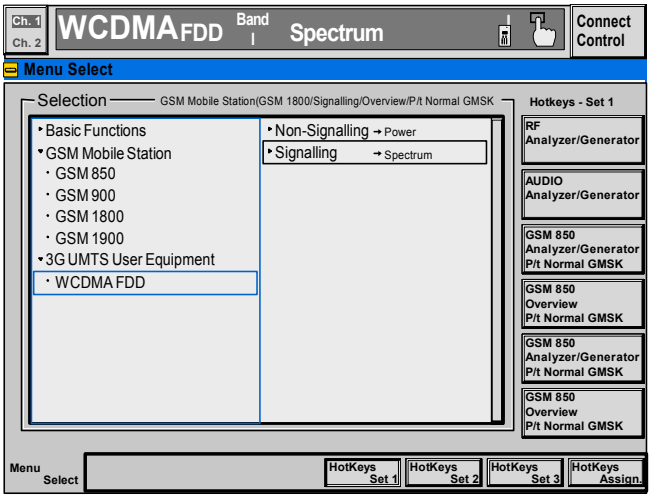
1. Install the test USIM in phone.

2. Connect hardware as illustrated in figure 4.

   Note: Control interface doesn't need to be connected at this time.

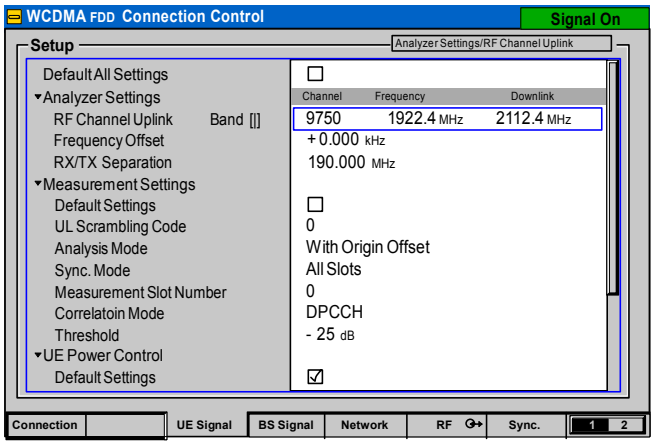
3. Setup up the test box for WCDMA FDD Signalling

Figure 17. WCDMA Signalling Setup



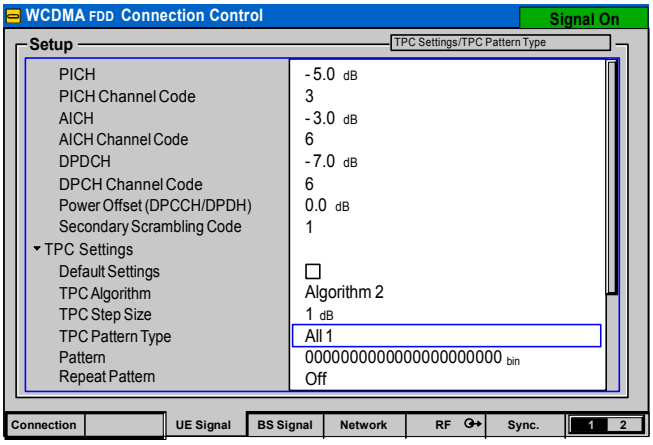
4. Set UE Signal, RF Channel Uplink to 9750

Figure 18. Channel Uplink(UE Signal)



5. Set TPC Pattern Type to All 1

Figure 19. TPC Pattern Type(UE Signal)

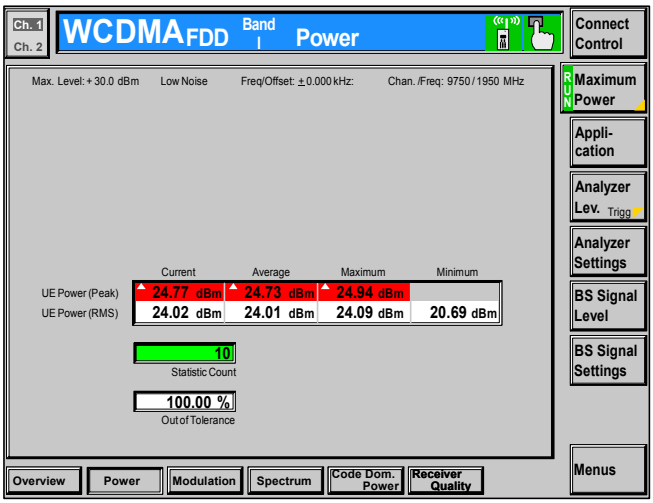


6. Wait until the phone indicates a signal

9. Dial a number from the phone and press the send button.

10. The phone is now connected.

Figure 20. WCDMA Call Connected



WCDMA Call Test Parameters

While the phone under test is in an active call, the parameters for each band should be verified as described.

Table 5. WCDMA Call Parameters

Parameter	Low Limit	High Limit	Unit
Avg. RMS Power Out[1]	20.5	21.5	dBm
Avg. Frequency Error[2]	-195	195	Hz
Avg. RMS EVM[2]	0	13.5	%
Avg. RMS ACLR - 2[3]	-100	-43	dB
Avg. RMS ACLR - 1[3]	-100	-33	dB
Avg. RMS ACLR + 1[3]	-100	-33	dB
Avg. RMS ACLR + 2[3]	-100	-43	dB

[1]Refer to Figure 10
[2]Refer to Figure 11
[3]Refer to Figure 12

Figure 21. WCDMA Modulation

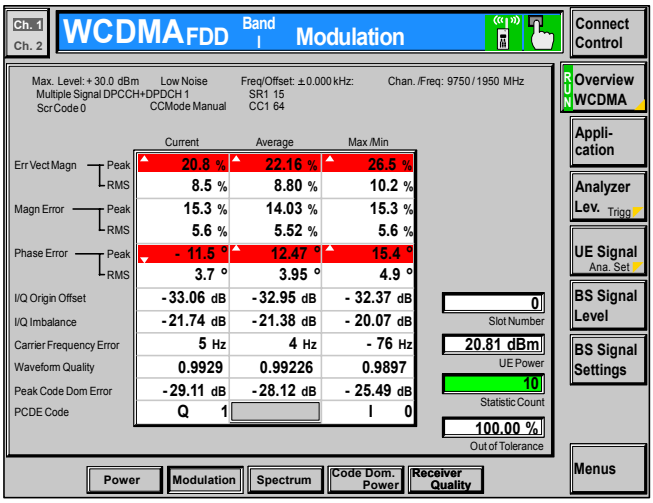
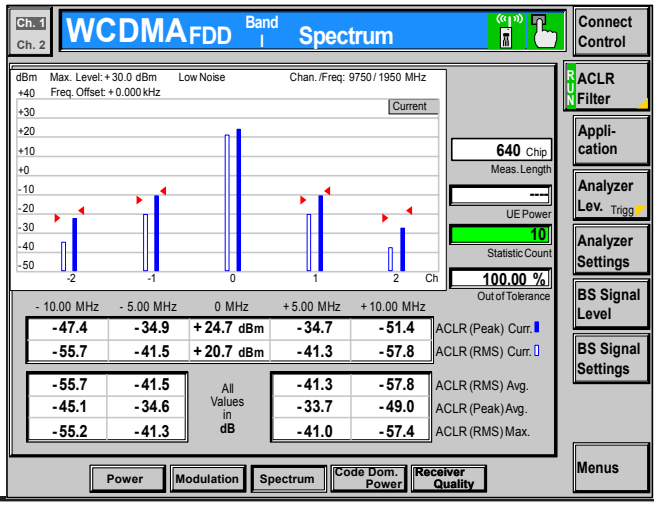


Figure 22. ACLR Screen



Non-Signalling Test Procedures (GSM/DCS/PCS)

To perform non-signalling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands can be sent using the Handset test command interface or through a computer. Please refer to section, "Handset Test commands," for details on how to send test commands through phone keypad entry.

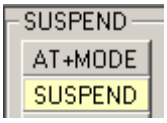
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Hardware Requirements

Refer to page 3-2 for a list of Hardware. Refer to Figure 13 for a configuration illustration.

Software Requirements

Handset Test Command

- No software needed

Computer Test Command

- Radio Comm (latest release)

Verify TX Power Output (GSM/DCS/PCS)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 8. TX Power Limits

Parameter	Low Limit	High Limit	Unit
GSM TX Power Out	31	33	dBm
DCS TX Power Out	28	29.5	dBm
PCS TX Power Out	28	29.5	dBm

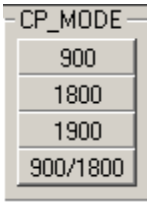
Handset Test Commands

54	Suspend
10*0*10[1]	WCDMA/GSM/DCS mode
20*38*0[2]	Set Channel 38
45*5[3]	Set GSM Power Level 5
7*6*1	Enable Carrier

[1]10*0*5 for PCS mode
[2]20*700*0 for DCS Channel 700; 20*661*0 for PCS Channel 661
[3]45*0 for DCS/PCS Power level 0

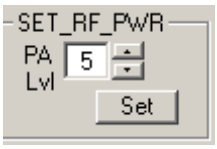
Radio Comm Test Commands

Click on 900/1800 (GSM/DCS) or 1900 (PCS)

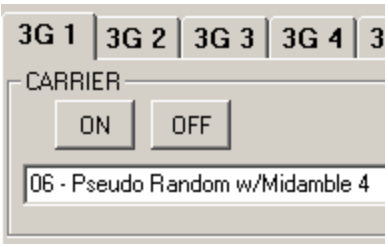


Enter 38 (GSM), 700 (DCS), or 661 (PCS) and then click Set

Enter 5 (GSM) or 0 (DCS/PCS) and then click Set



Select 06 and then click ON



GSM RSSI

Verify GSM RSSI by initiating the commands in this section. Verify that the RSSI results are equal to the Broadcast Channel (BCH) level. The user will need to set the RF generator with the following parameters.

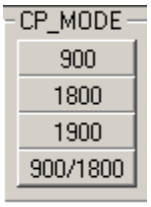
Broadcast Channel (BCH): 20
Broadcast Channel (BCH) Level: -105 dBm

Handset Test Commands

No supported test commands

Radio Comm Test Commands

Click on 900/1800 (GSM/DCS) or 1900 (PCS)



Enter Channel 20
Click INIT

Click Execute
Verify return data is approximately -105 dBm

Non-signalling Test Procedures (WCDMA)

To perform non-signalling test procedures, the user is required to be familiarized with sending test commands to the phone under test. The test commands can be sent using the Handset test command interface or through a computer. Please refer to section,"Handset Test commands," for details on how to send test commands through phone keypad entry. Also, refer to, "Computer Test Commands," for details on how to send test commands through the computer.

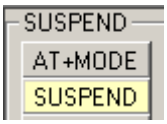
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Hardware Requirements

Refer to page 2 for a list of Hardware. Refer to Figure 4 for a configuration illustration.

Software Requirements

Handset Test Command

- No software needed

Computer Test Command

- Radio Comm (latest release)

Verify TX Power Output (WCDMA)

Verify the TX Power output by initiating the commands in this section. Verify that the results fall within the following limits.

Table 9. WCDMA TX Power Output

Parameter	Low Limit	High Limit	Unit
WCDMA Power Out	20.5	21.5	dBm

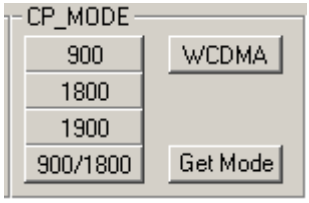
Handset Test Commands

54		Suspend
3086		W_CARRIER
Field 1	9750	Set Channel
Field 2	0	Enable Carrier
Field 3	023	Max Power Out
Field 4	027	Max TX Power
Field 5	206	Min TX power
Field 6	002	PN9 Data pattern
Field 7	1	Enable spreading
Field 8	01	Long scrambling
Field 9	000	SF256, Slot format 0
Field 10	000	SF256, Slot format 0
Field 11	000	Channelization Code
Field 12	000000000	Scrambling Code

Note: Enter 1 in field 2 to disable carrier

Radio Comm Test Commands

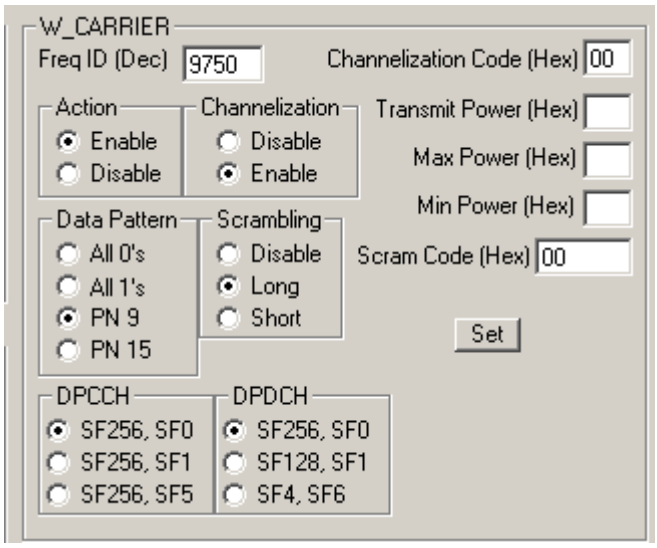
Click on WCDMA



For W_CARRIER assign these actions to each field

Freq ID (Dec)	9750
Action	Enable
Channelization	Enable
Data Pattern	PN 9
Scrambling	Long
DPCCH	SF256, SF0
DPDCH	SF256, SF0
Channelization Code	00
Transmit Power	15[1]
Max Power	15[1]
Min Power	80[2]
Scram Code	00

[1]0x0015 -> 21 dec -> +21dBm
[2]0x0080 -> 128 dec -> (128-256 = -128 dBm)



Audio/Vibrator Test Procedures

This section describes how to use test commands to verify audio and vibrate functions.

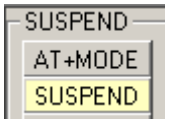
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



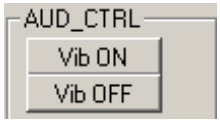
Vibrator Test

Handset Test Commands

3*0*1 Enable Vibrator
3*0*0 Disable Vibrator

Radio Comm Test Commands

Enable or Disable Vibrator



Verification

Verfiy vibration function when enabled.

Handset Mic/Speaker test

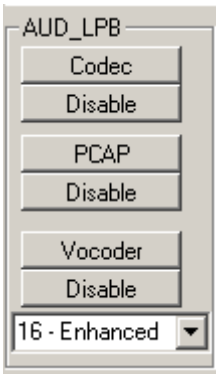
Handset Test Commands

6*2*2	Enable internal mic and handset speaker
4*7*1*16	Enable VOCODER loopback at Enhanced Full Rate

Radio Comm Test Commands

Enable internal mic and headset speaker

Enable Vocoder loopback at Enhanced Full Rate



Verification

Speak into the handset mic and listen for undistorted speech in the handset speaker.

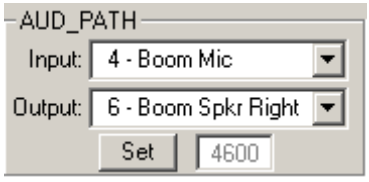
Mono Headset Mic/Speaker test

Handset Test Commands

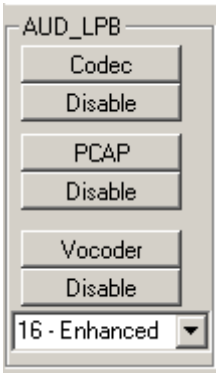
6*4*6	Enable headset mic and headset speaker
4*7*1*16	Enable VOCODER loopback at Enhanced Full Rate

RadioComm Test Commands

Enable headset mic and headset speaker



Enable Vocoder loopback at Enhanced Full Rate



Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

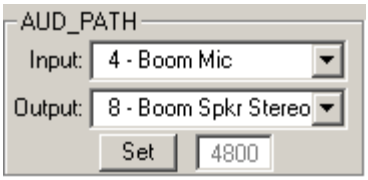
Stereo Headset Mic/Speaker test

Handset Test Commands

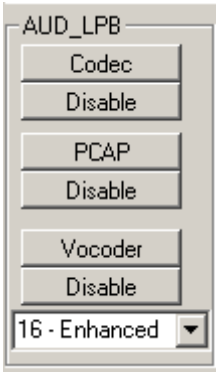
6*4*8	Enable headset mic and headset speaker
4*7*1*16	Enable VOCODER loopback at Enhanced Full Rate

RadioComm Test Commands

Enable headset mic and headset speaker



Enable Vocoder loopback at Enhanced Full Rate



Verification

Speak into the headset mic and listen for undistorted speech in the headset speaker.

Melody Speaker test

Handset Test Commands

0*1*245	Play BACH_INVENTION_1
0*0*245	Stop BACH_INVENTION_1

NOTE: DO NOT issue a Suspend command (54 ok) for this test.

RadioComm Test Commands

Currently not supported

Verification

Listen for undistorted audio.

Software Version Check

Use the following procedures to retrieve software information. Software information can also be retrieved from the phone's customer User Interface. Refer to the phone's user manual for details.

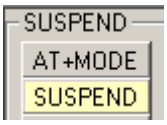
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands

Handset Test Commands

None

Radio Comm Test Commands

Click AT+MODE (Serial Only)
Click PST Initialize (USB Only)



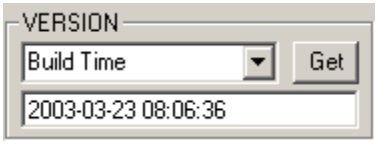
Test Commands

57*017003 Read Software Version
57*017001 Read Build Date

RadioComm Test Commands

Select Product Base Label and click "Get" to retrieve software version

Select Build Time and click "Get" to retrieve Build Date



Display Test Procedures

This section will describe the proper test procedures to determine the functionality of the color display. Any tests that involve displaying a predefined pattern can be returned to the Opcode screen by pressing the right softkey of the phone.

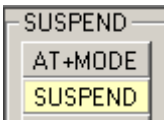
In order to successfully send test commands to the phone under test, the phone needs to be in suspend mode. Follow the listed procedure to place the phone in suspend mode.

Handset Test Commands

54 ok Suspend

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



Display Backlight Test

Handset Test Commands

55*9*000 Backlight Off
55*9*001 Backlight On, full intensity

RadioComm Test Commands

Click "FL Off" to disable backlight
Click "FL On-Full" to enable backlight

Verification

Verify that the backlights respond for each issued command.

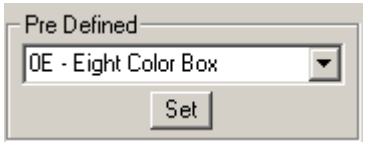
Display Color Test

Handset Test Commands

55*2*014 Eight Color Box Pattern

RadioComm Test Commands

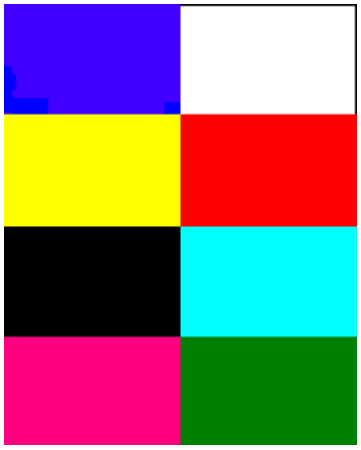
Select Eight Color Box and click "Set"



Verification

Verify that the color pattern on the phone's display matches the color box in figure 23. Also verify edges (uniform/smooth).

Figure 23. Eight Color Box Pattern



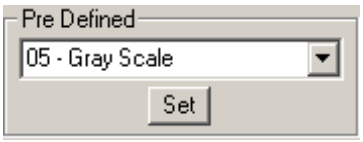
Display Linearity Test

Handset Test Commands

55*2*005 Grey Scale Block

RadioComm Test Commands

Select Grey Scale and click "Set"



Verification

Verify that the Grey scale block on the phone's display matches the Grey scale block in figure 14. This test can also be used to confirm that the color intensity is linear.

Figure 24. Grey Scale Block

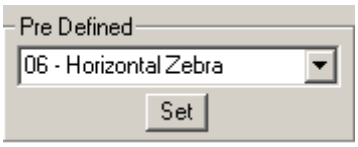
Display Flicker Test

Handset Test Command

55*2*006 Horizontal Zebra Line

RadioComm Test Commands

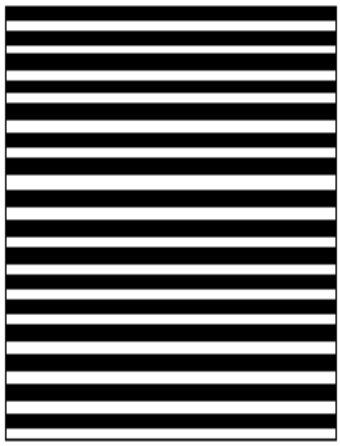
Select Horizontal Zebra and click "Set"



Verification

Verify that no noticable flicker exists.

Figure 25. Zebra Pattern



Display Pixel Defect (Bright)

Handset Test Commands

55*2*001 All pixels on (all white)

RadioComm Test Commands

Select All Pixels Off and click "Set"

Verification

Verify that no greater than two pixels are off.

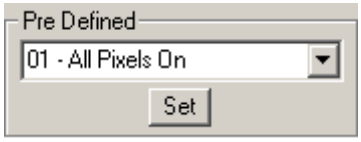
Display Pixel Defect (Dark)

Handset Test Commands

55*2*000 All pixels off (all black)

RadioComm Test Commands

Select All Pixels On and click "Set"



Verification

Verify that no greater than two pixels are on.

LEDS and Keypad Backlight

Use the following procedures to verify status LED and keypad backlight.

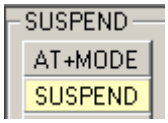
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Handset Test Commands

None

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



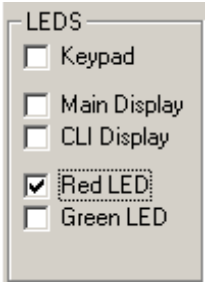
Status LEDS

Handset Test Commands

62*3*3*012[1] Enable Red LED
62*4*3*012[1] Enable Green LED
[1]000 to disable

RadioComm Test Commands

Select Red LED or Green LED to enable. Deselect Red LED or Green LED to disable.



Verification

Verify that the Red and Green status LEDS activate.

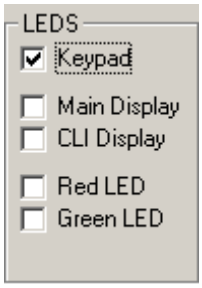
Keypad Backlight

Handset Test Commands

62*0*1[1] Enable Keypad Backlight
62*0*0[1] Disable Keypad Backlight
[1]Leave field 3 blank and press OK

RadioComm Test Commands

Select Keypad to enable. Deselect Keypad to disable.



Verification

Verify that all keypad backlight LEDs activate.

Bluetooth Tests (V500/V600 only)

Use the following procedures to verify functionality of the Bluetooth device integrated in the phone.

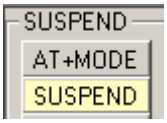
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Handset Test Commands

None

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click PST Initialize and click SUSPEND when initialization is complete (USB Only)



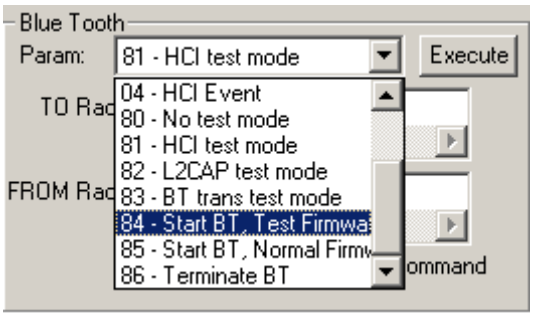
Unmodulated CW TX test

Handset Test Commands

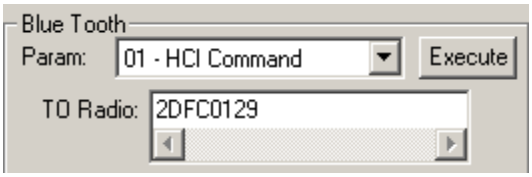
Not Supported

RadioComm Test Commands

Under Bluetooth, select parameter 84 and click execute, then select 81 and click execute.



Under Bluetooth, select parameter 01 and enter 2DFC0129 in the "TO Radio" field. Click Execute.



NOTE: The Bluetooth TX signal will activate momentarily once the HCI command is issued. You must have the RF probe positioned for measurement once you click execute.

Verification

Verify that a 2441MHz signal is present. If the phone is closed, use a RF probe to sniff the strongest signal around the "7" key of the keypad. If the phone is open (shields off), verify that -2dBm to +4dBm is read from R320. An high impedance RF probe is required to read this range. Use of lower quality RF probes will result in signal level differences.

Camera Testing

This document is intended to describe the procedures that will determine whether the camera function of a Motorola terminal is under normal operating conditions.

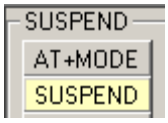
In order to successfully send test commands to the phone under test, the phone doesn't need to be in suspend mode. Follow the listed procedure to configure the phone to accept test commands.

Handset Test Commands

Not supported

Radio Comm Test Commands

Click AT+MODE then SUSPEND (Serial Only)
Click USB Initialize and click SUSPEND when initialization is complete (USB Only)



Hardware Requirements

The following hardware will be required to properly test the camera function of the phone.

1. Desktop Charger (SPN5032A or equivalent)
2. USB or RS232 control interface (refer to figure 4)
3. Fast Rate Charger (SPN5078A or equivalent)
4. Hardcopy of Macbeth Color Chart
5. Hardcopy of Focus Chart
6. Hardcopy of Grey Chart

Camera Test Configuration

Use any color printer to print a hardcopy of the Macbeth color chart. The Focus chart and Grey chart can be printed using any B/W printer.

For best results follow this recommended setup,

1. Attach chart to a flat vertical surface (wall)
2. Attach the phone to the desktop charger
3. Attach the control interface to desktop charger
4. If necessary, attach power supply to control interface.
5. Turn on phone.
6. Select Camera option in phone
7. Position Desktop charger so that the camera test chart completely fills the viewfinder.

Assign a permanent space in the test lab for these test procedures. Always use the same lighting conditions. Also, it's recommended that a "golden picture" is saved and used for comparison.

There is a variety of ways the camera test charts can be attached to a vertical flat surface. They can be taped, tacked, attached to flip charts, etc. Use your best judgement.

The desktop charger is being used as a fixture to position the phone for test, therefore, it's recommended that the desktop charger is attached to a countertop to prevent any movement.

Figure 9. Camera Test Configuration

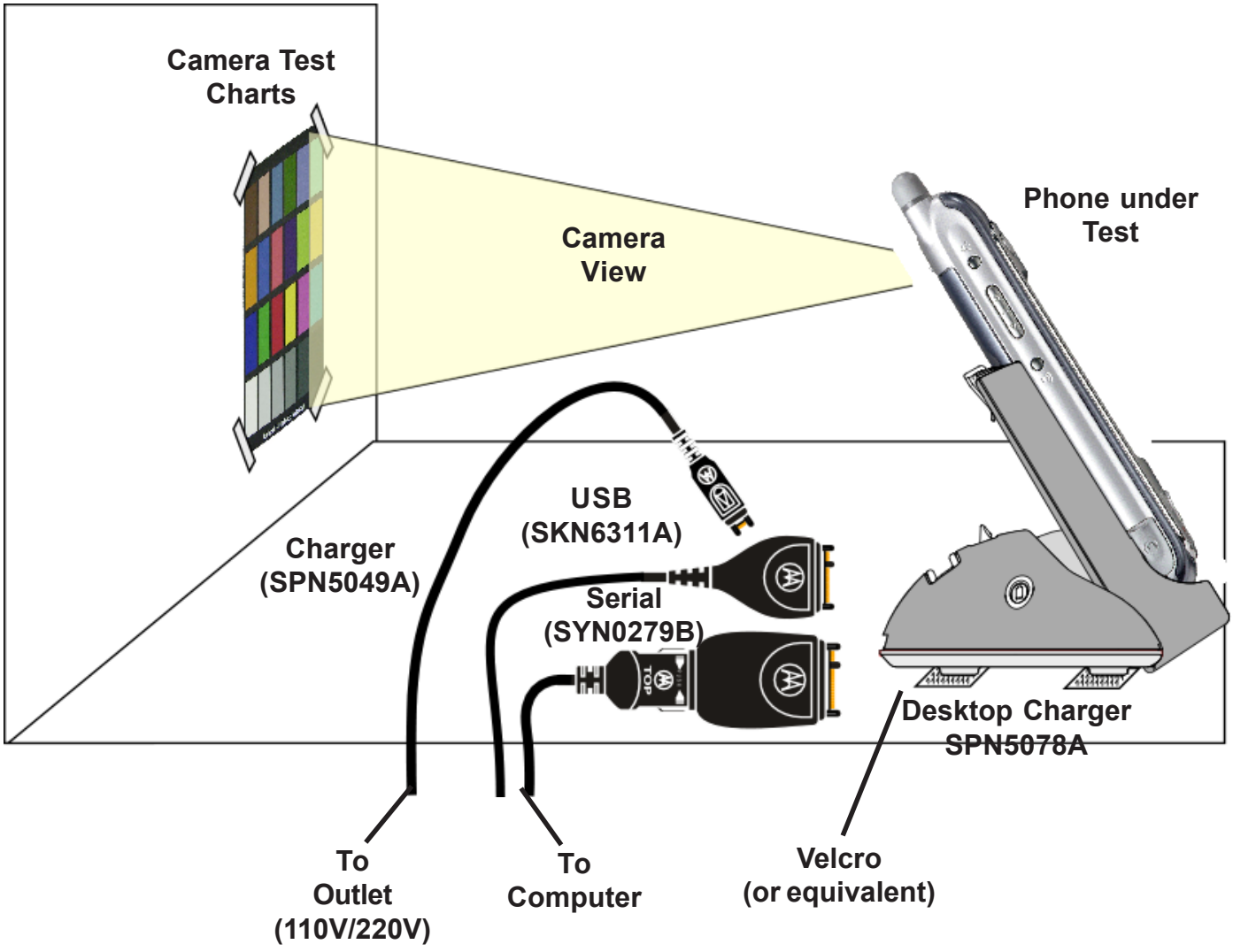


Image Capture

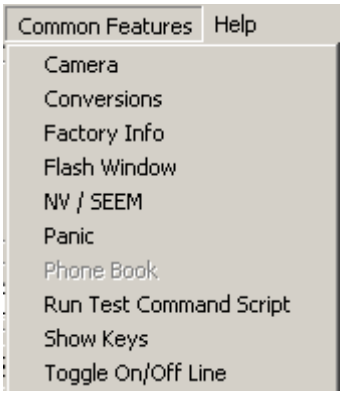
The listed steps should be followed to capture three images (1) the Macbeth color chart, (2) the focus chart, and (3) the grey scale chart. The user will be required to print all images found in Appendix A.

Handset Test Commands

Not supported

Radio Comm Test Commands

Under "Common Features" select Camera



Click "Take Picture"

Once the picture is captured, it'll be displayed on the screen. Click "Save To File"

Macbeth Color Chart

1. From the computer, open the captured color chart image.

2. Compare, the color blocks of the printed Macbeth color chart to the captured image.

Follow the listed verifications to determine the quality of the image.

1. Minimal noise level for Blue, Green and Red on blocks 19 through 24.

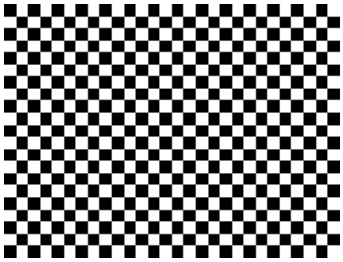
2. Uniformity for grey scale blocks 19 through 24.

3. Good white balance on blocks 19 through 24.

4. Good color reproduction on blocks 13 through 18.

Focus Chart

1. From the computer, open the captured focus chart image.



Verify the focus quality at the center, top-left corner, bottom-left corner, top-right corner, and bottom-right corner.

Grey Scale Chart (Shading Test)

1. From the computer, open the captured grey scale chart image.

Verify that there is minimal shading deviations on all four corners when compared to the center of the image.

Service Diagrams

Introduction

The service diagrams were carefully prepared to allow a Motorola certified technician to easily troubleshoot cellular phone failures. Our professional staff provided directional labels, color coded traces, measurement values and other guidelines to help a technician troubleshoot a cellular phone with speed and accuracy.

We worked hard in trying to provide the best service diagrams, therefore, to avoid cluttered diagrams, we may exclude some components from the service diagrams. Our professional staff carefully selected to excluded components that are unlikely to fail.

Test Point Measurements

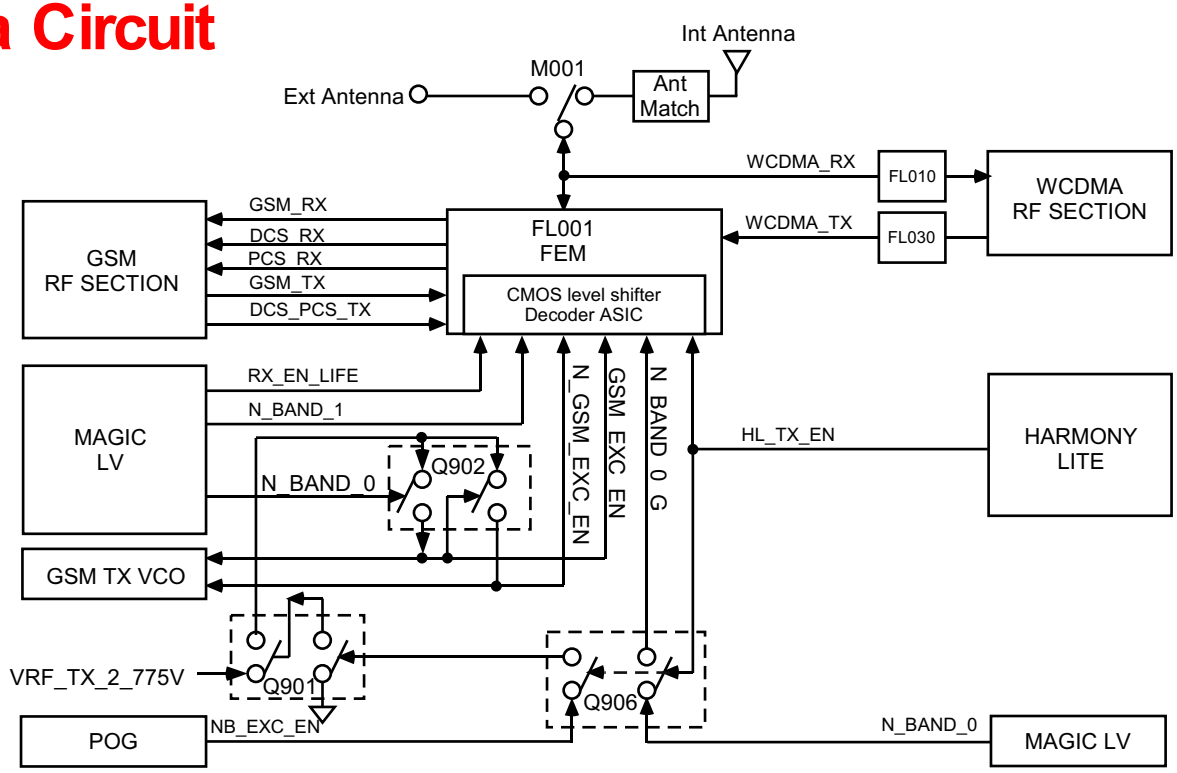
The measurements labeled on the service diagrams are approximate values and may vary slightly. These measurements are dependent on the accuracy of the test equipment.

It is strongly recommended that the test equipment calibration schedule be followed as stated by the manufacturer. RF probes should be calibrated for each frequency in which tests are going to be performed.

The types of probes used will also affect measurement values. Test probes and cables should be tested for RF losses and loose connections.

Because of the sensitivity of RF, measured readings will be greatly affected if they're taken in certain locations. To get the most accurate readings, take measurements nearest to the labeled measurement on the service diagram.

A920: Antenna Circuit



Description

All cellular receive bands are fed into either the internal antenna or external antenna. M001 is a mechanical switch which has the internal antenna path connected when a no insertion condition exists. The RF path will switch to external antenna upon insertion of a male SMA connector to M001. The internal antenna path is fed to the FEM(Front End Module) through antenna matching components. The FEM provides band selection and filtering between the EGSM, DCS, PCS and WCDMA receive and transmit bands to a single antenna port. GSM band selection is done by control lines N_BAND_1 and N_BAND_0_G. Mode selection is done by control lines HL_TX_EN, RX_EN_LIFE, N_GSM_EXC_EN, and GSM_EXC_EN. The diplexing arrangement permits reception of WCDMA signals in any FEM switch position. This allows the phone, while in a GSM call in any band, to detect signals from a WCDMA base station. The decision may then be made to hand over to the WCDMA system. Similarly, EGSM base station signals can be detected while the phone is in a WCDMA call to permit a handover decision from WCDMA to EGSM (This is not possible for base station signals in the DCS and PCS bands.).

Signals received at the antenna between 2110 - 2170MHz will see the RF switch as an open circuit at any position. Consequently WCDMA Rx signals will go through FL2 to the WCDMA receiver. FL2 should have a maximum insertion loss of ~0.5dB. Outside of the WCDMA Rx band, FL2 behaves as an open circuit, preventing out-of-band signals from reaching the WCDMA receiver.

GSM, DCS, and PCS receive signals from the antenna port through the FEM should have a maximum insertion loss of -4.4dB. The FEM EGSM transmit path should have a maximum insertion loss of -2.5dB. The FEM DCS transmit path should have a maximum insertion loss of -3.1dB. The FEM PCS transmit path should have a maximum insertion loss of -3.7dB.

Q902 is a dual FET package that's being used to multiplex function of the N_BAND_0 control signal coming from the Magic LV. With the use of Q902, N_GSM_EXC_EN will follow N_BAND_0. GSM_EXC_EN will be the inverted level of N_BAND_0. Q906 is another dual FET package that's used to prevent simultaneous GSM and WCDMA transmission conditions. During WCDMA transmission conditions, HL_TX_EN will be in a high state. This will open both FETs in Q906, thus, disabling any signal functions from control lines NB_EXC_EN and N_BAND_0. Q901 is used to invert the control signal coming from Q906.

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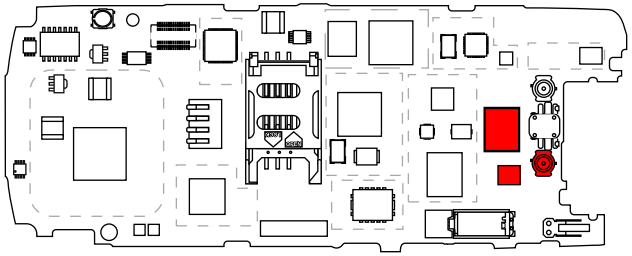
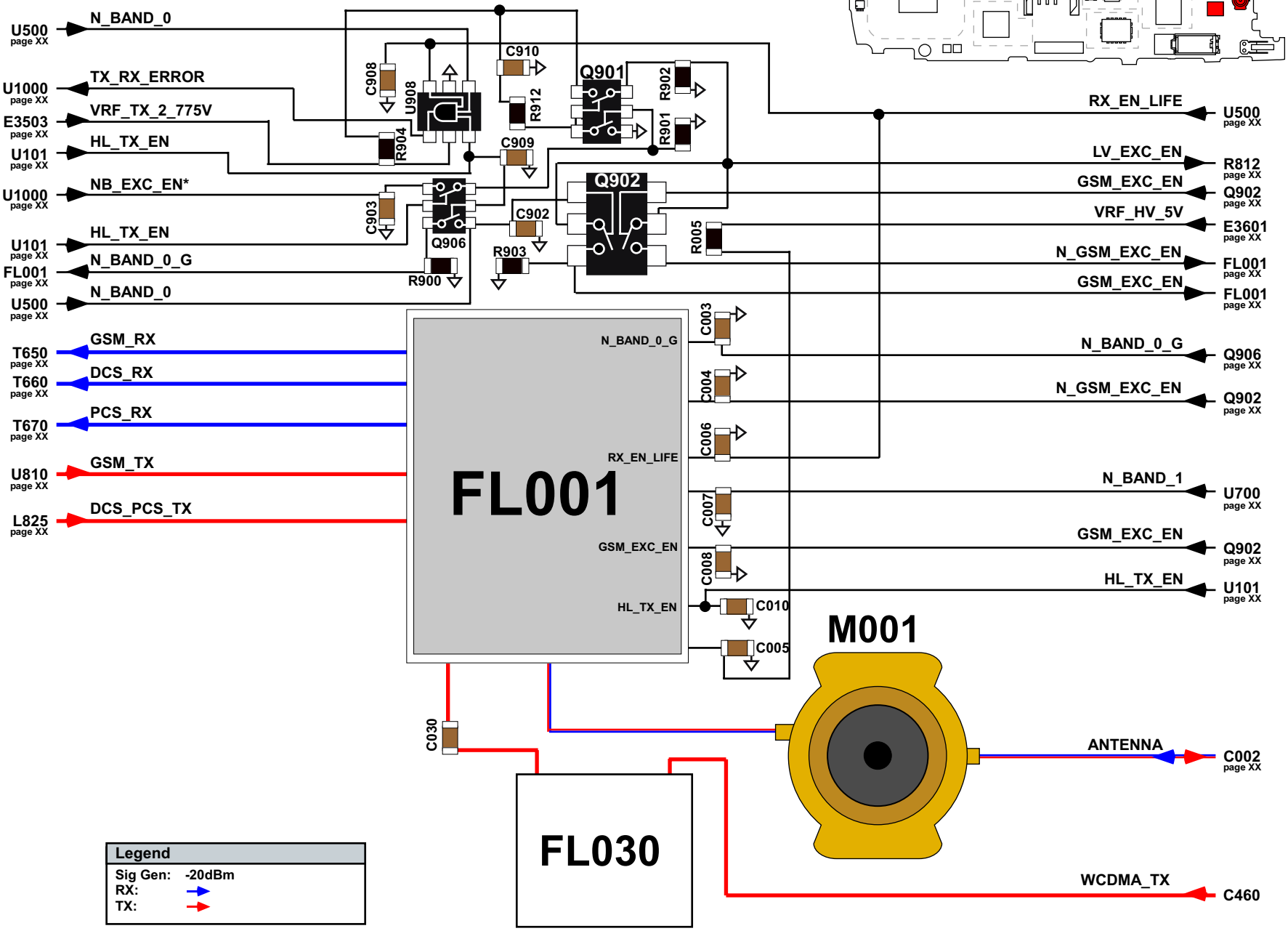
A920: Antenna Circuit





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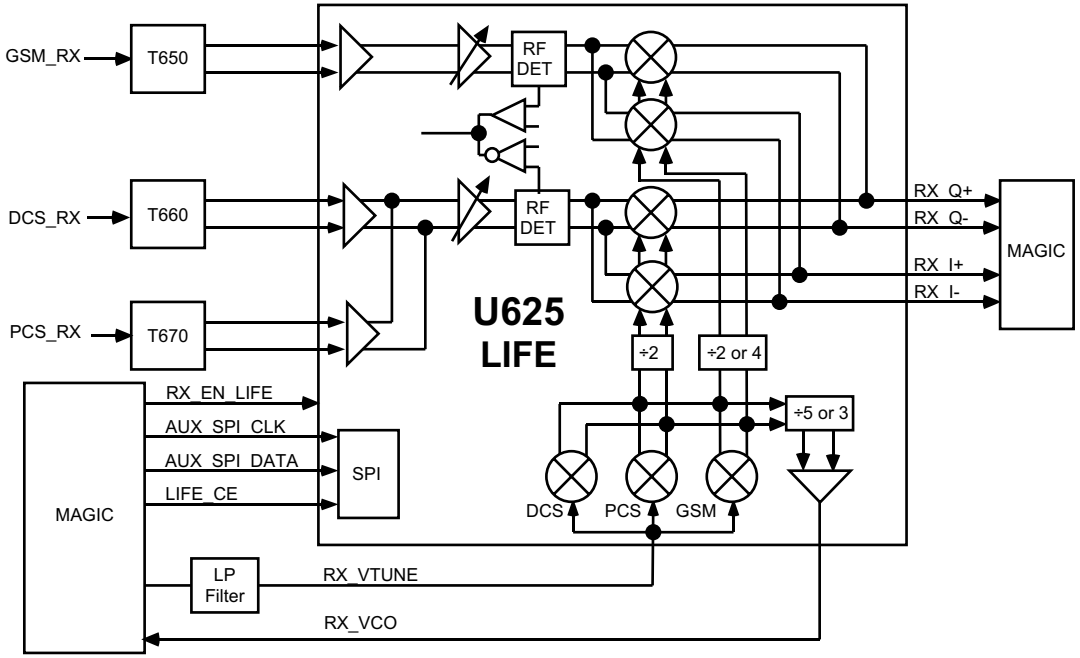
A920: GSM RX Front End



Description

The EGSM, PCS and DCS signals must first pass through baluns before reaching the LIFE IC. Since the LIFE expects differential inputs, the baluns will provide this. Baluns provide the change from an unbalanced to a balanced line condition. By directly connecting to lines together, a possibility might arise where one line might ground a signal and impair the operation of a circuit. This situation is solved through the use of an un-balanced to balanced transformer, a balun. Expected nominal losses is ~.5 - 1.0dBm.

The first IC in the EGSM, DCS, and PCS RX line up is U625 (LIFE), which is an LNA, VCO, and down converter mixer. The RX frequency is mixed down to a Very Low Intermediate Frequency (VLIF) of ~ 100KHz. This design is utilized to improve LO leakage causing RF self-mixing, DC offsets, and noise performance. The LIFE IC operates from the MAGIC_LV (tracking regulator), MAGIC_RF_V2_475. and MAGIC_SF (isolated supply for the VCO).
LIFE is comprised of four low noise amplifiers (three of which are used) with two quadrature mixer paths for use in receive GSM 900 (925- 960MHz), DCS (1805-1880MHz), and PCS (1930-1990MHz) frequency bands, all SPI programmable. The RX_VCO signal is fed back to the MAGIC_LV prescaler input. Although the frequency will be dependent of the channel selected, the amplitude signal is ~30dBm.

LIFE contains three fully contained VCOs which operate at ~4GHz. These VCOs are internally divided to provide precise quadrature down conversion for the three frequency bands. The input signal RX_VTUNE from the RX backend processor (MAGIC_LV) selects the VCO frequency to operate at. The tune range is .5 - 4.5V. The VCO frequencies for the three technologies are: DCS 3610 - 35759MHz, EGSM 3700 - 3838MHz, and PCS 3859 - 3980MHz.

The AGC is provided by a common amplifier section, which is shared by all four LNAs. The AGC amplifier gain control is controlled by the voltage on the AGC pin, utilizing the internal 6-bit D/A to set the AGC via the SPI lines (SPIDATA, SPI_CLK, and SPI_CE). LIFE has an internal RF detector at the input of the AGC amplifier. The detected DC output level will be compared against a reference, which corresponds to the maximum safe input level to the mixer. This reference is SPI selectable so that the threshold can be set to 0dB, 3dB, 6dB, or 9dB below the level, which results in the mixer malfunction. If the detected level is above the reference then AGC_FLAG will go high. The MAGIC_LV will receive this signal as an interrupt and will reprogram the AGC until the level drops below the safe mixer input level as signified by AGC_FLAG returning low.

The output signals I / IX and Q / QX are @ ~100KHz IF value for the Very Low IF. The input pin, RX_EN_LIFE controls the on / off state of the receiver and the PLL circuits. For input amplitude at the antenna of -50 to -40dBm the expected nominal output should be an AC rms peak-to-peak voltage of ~4.5 - 14mV.

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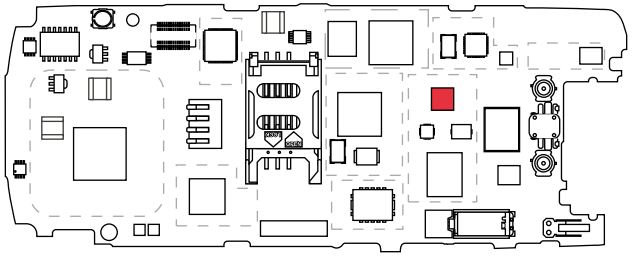
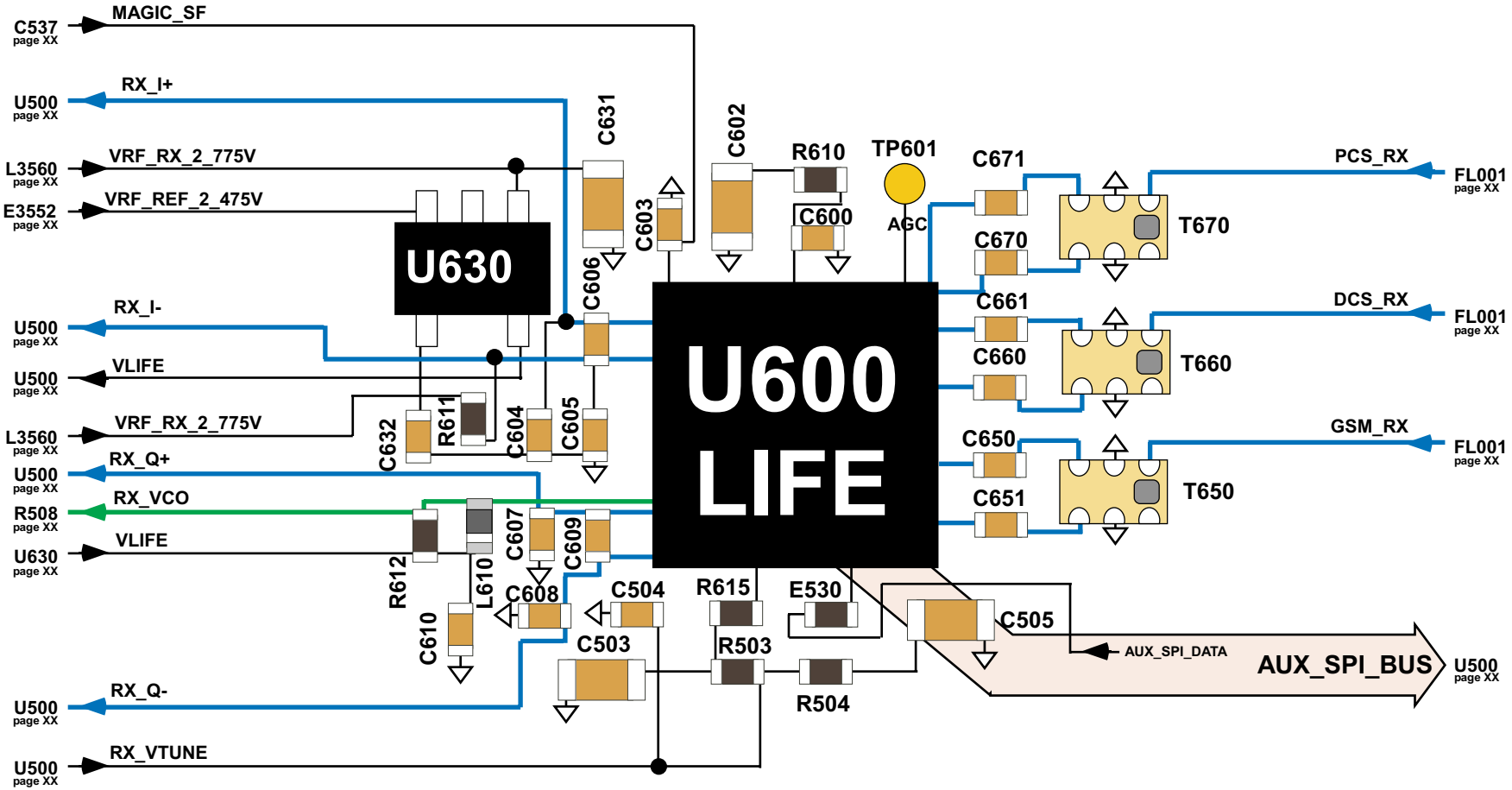
A920: GSM Receiver Front End





Legend	
Sig Gen:	-20dBm
RX:	→
VCO:	→

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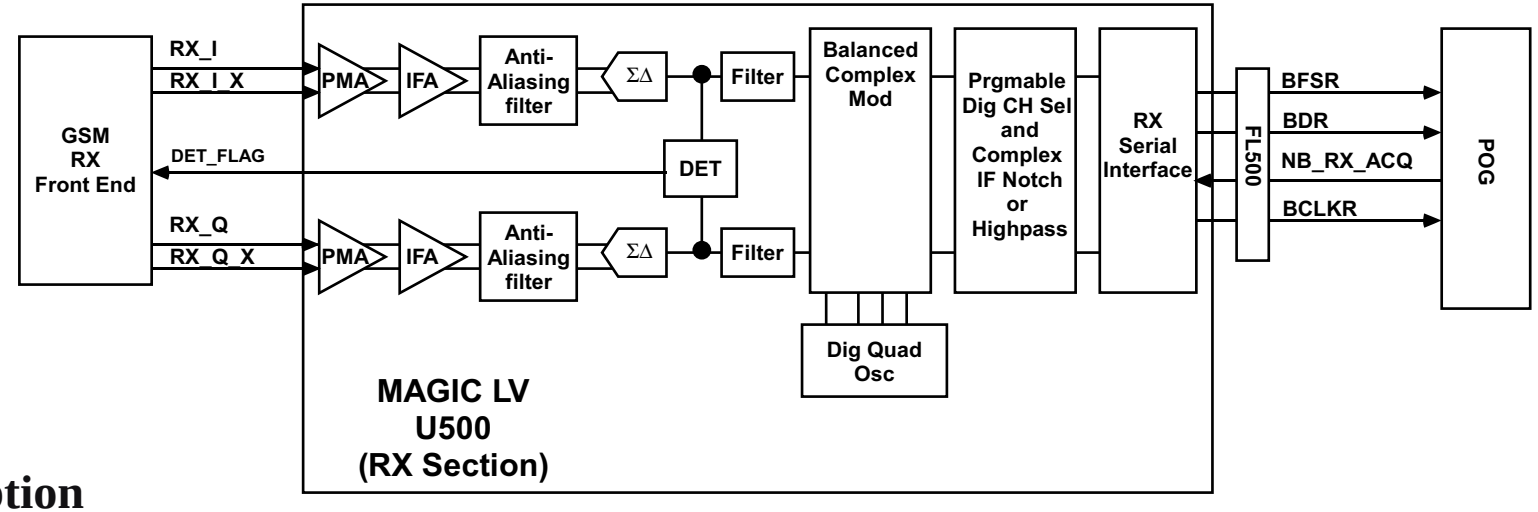
A920: GSM RX Back End (Magic LV)



Description

The MAGIC_LV (U500) handles the backend processing for the EGSM, DCS and PCS (VLIF: RX_I, RX_I_X, RX_Q, and RX_Q_X) signal lines from LIFE. Simply, the MAGIC_LV performs an analog to digital conversion of I /Q and sends it to the data to the board processor (POG) via the SSI (serial synchronous interface). The MAGIC_LV also has a programmable and phase-able digital IF to improve image rejection.

In MAGICLV, each channel is comprised of a Post Mixer Amplifier (PMA), an integrated passive two pole filter, a gain stage (AMP1) followed by an active programmable 2 pole anti-aliasing filter (mainly required to meet the blocking specs). This is followed by a lowpass sigma-delta ADC with a programmable oversampling clock OVSCLK (derived from the reference oscillator) equal to 13MHz for 200kHz channel spacing (13bits).

Digital detector circuits are placed on each channel at the output of the sigma delta converters. The outputs of these detectors are compared against a level defined by DET_LVL. If either of the detected levels exceeds the programmed threshold then the pin DET_FLAG is set high. This indicates that the signal level is excessively high for the sigma delta modulator. DET_FLAG is read by the processor, which will respond by re-programming one of the AGC settings to a lower gain until DET_FLAG returns low.
The outputs of the sigma-delta modulators are digitally processed through a noise cancellation circuit, comb and decimation filters. A second programmable digital LO based on a look up ROM generates digital quadrature oscillators with programmable gain/phase correction (called balanced complex multiplier) to digitally downconvert the I/Q signals to baseband (digital zero IF) through four quadrature mixers that provide image rejection of adjacent/alternate channels. Gain/ Phase correction at a single baseband frequency is performed on the Digital Quadrature Oscillator to compensate the analog gain/phase mismatch of the quadrature I and Q paths. After baseband downconversion and image reduction, the quadrature I and Q signals are further processed by digital filters that perform channel selectivity and out of band noise rejection.

A serial bus consisting of SDFS and SDRX will transmit the RXI and RXQ data in 2‘s complement format. BDR and BFSR are outputs from MAGIC LV. BFSR is a framing signal which marks the beginning of an I,Q transfer. BDR is the serial data. The clock used for the serial transfer is BCLKR. When NB_RX_ACQ goes high MAGIC LV will activate the SSI interface in the digital receiver section. The data transmission over the serial bus will begin at the next normal occurrence of valid I and Q data, as defined internally to the digital receiver.

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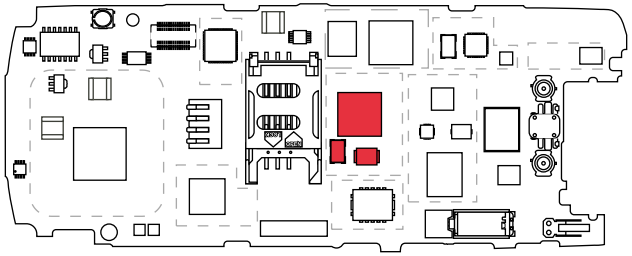
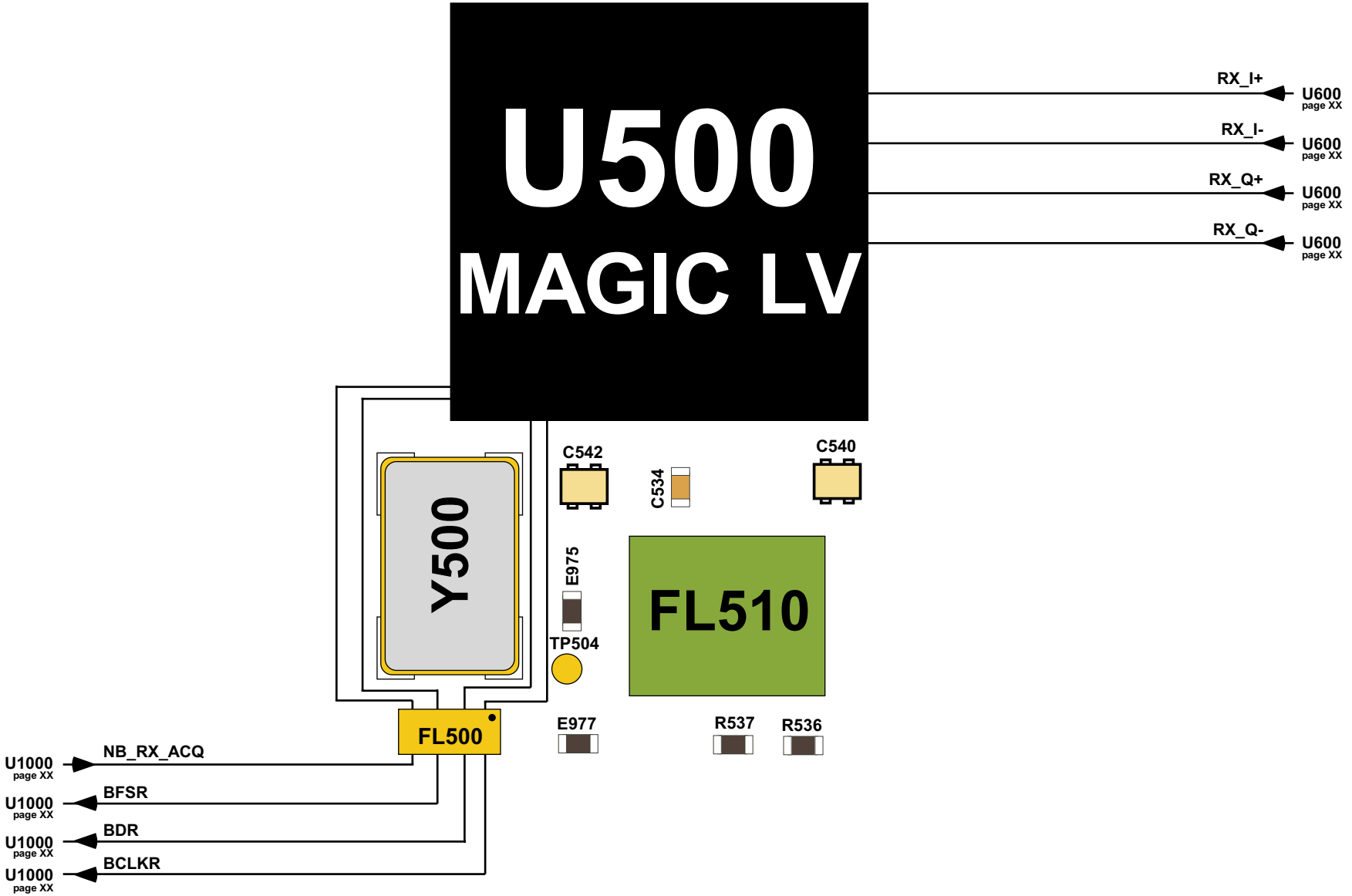
A920: Magic LV (Receiver Back End)





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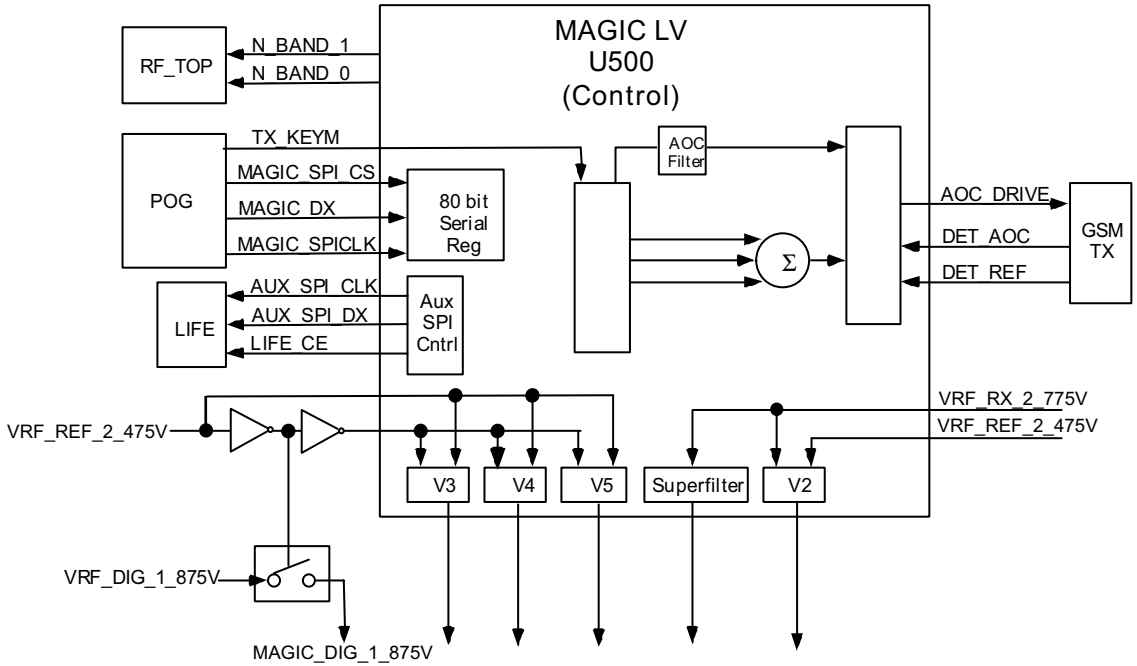
A920: MAGIC LV Control Functions



Description

The MAGIC LV contains 4 tracking regulators and one superfilter, which will generate the supplies for most of the IC as well as the front end and the main VCO. The tracking regulators derive their internal power from the REG_REF pins. The reference voltages are filtered and buffered for use on the IC. The buffered voltages should track the references within +/-1.5%. A raw supply voltage is provided to the tracking regulators which is higher than REG_REF as specified below for each regulator. A superfilter is needed for the external VCO power supply. This superfilter, cascaded with an external regulator and any filtering in front of the IC, will need to provide 80dB of rejection to a 0.1V step occurring at a 217Hz rate with a risetime of 20us on the raw supply (battery) and a duty cycle of 0.125. The superfilter will use an internal pass transistor that is capable of driving a 30 mA load with a voltage drop of less than 0.4V relative to SF_SPLY from the SF_OUT pin. An external 1uf cap is required on SF_OUT. As the superfilter will track SF_SPLY it will need to sense the power on reset and turn off even though its supply may remain active. All supplies within the IC must be within 5% of their final values after 5msec from the start of POR_LB. The power on reset circuit contained within the crystal reference oscillator is used to aid this functionality.

The MAGIC_LV has two sets of SPI interfaces; one set is for handling the control interface for the LIFE IC (AUXSPI lines) and ones for interfacing with POG (SPI lines). AUX_SPI_DX is the serial data input line. AUX_SPI_CLK is the clock input line, where data shifting occurs at the rising edge of this signal. LIFE_CE is the clock enable line, active high, for the LIFE IC.

MAGIC_LV will integrate a system of D/As and control logic to generate the power amplifier control ramps. In addition, MAGIC_LV will integrate the op-amps and comparators which receive the detected output of the power amplifier and create the necessary control voltage to drive the power amplifier control port based on the control ramps. When TX_KEYM goes high, the ramp controller receives an positive input. This will cause the AOC_DRIVE pin to linearly rise which in turn will cause the PA output power to rise. The rising PA output power will cause DET_AOC to begin to rise until the DC level on DET_AOC exceeds the DC level on DET_REF by the intentional offset of the RF detector versus it‘s reference. At this point the “Active Detect” comparator will go low and break the input voltage to the integrator with the ramp controller. This will cause the PA power to stop rising and hold the present power level as determined by the 8 bit offset value fed to the ramp controller. The PA control loop is now at a minimal power needed to keep the control system in a closed loop for a controlled ramp up of the power.

The MAGIC uses two SPI driven GPO lines which are used to control the operating bands of the GSM RF circuits. They are N_BAND_0 and N_BAND_1.

When the MAGIC LV is set to battery save mode it will shutdown the receiver analog sectioins (via RX_EN_LIFE), the AOC, the main synthesizer and the superfilter.

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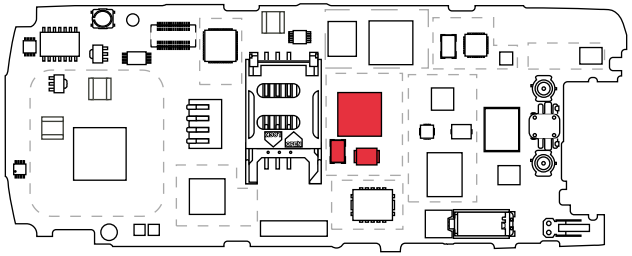
A920: Magic LV (Control)



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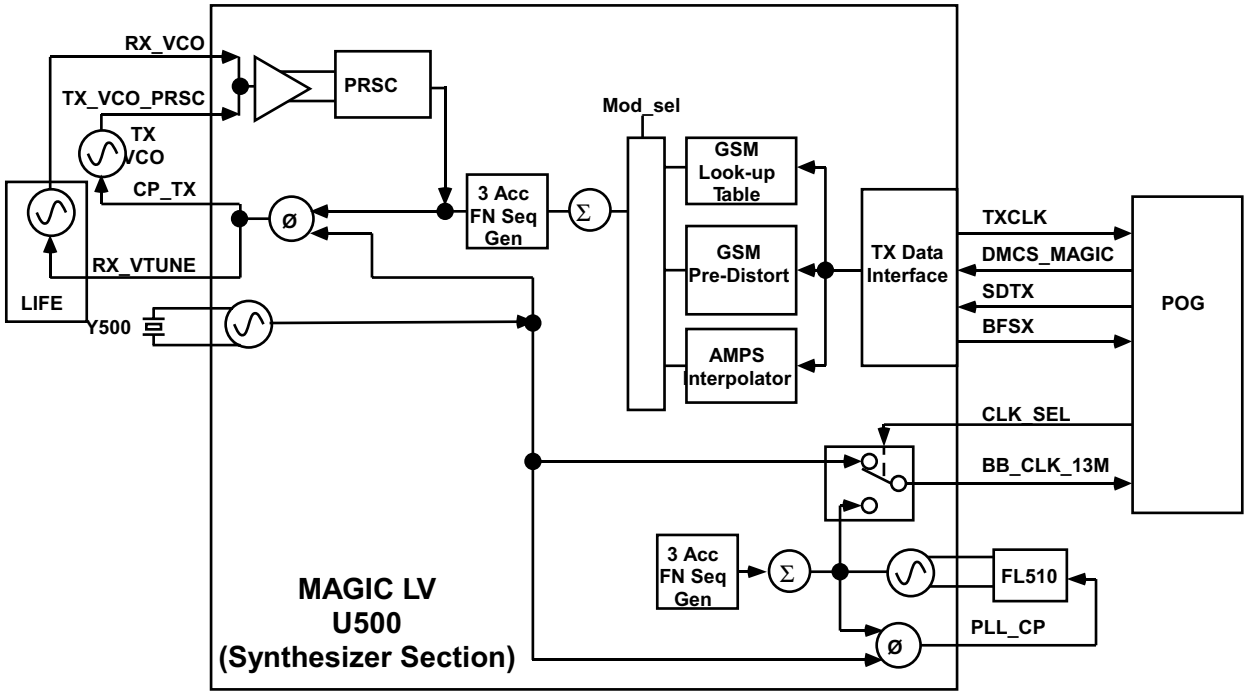
A920: MAGIC LV (Synthesizers/Transmitter)



Description

The MAGIC_LV receives SSI Tx data at DMCS (digital input to start Tx modulation), TXCLK (clock for serial transfer) and SDTX (serial Tx data) from POG. The present serial data bit and the three previous data bits are used to set up one of 16 possible waveforms based on the sum of Gaussian pulses stored in a look up ROM. The resulting signal will then be clocked out at a 16x over-sampling rate. This data pattern input to three-accumumalator fractional N synthesizer with a 24-bit resolution. The VCO control lines must have compliance over an output voltage range of 0.3VDC to Vcc-0.3V. The charge pumps will have their own supply pin. The voltage on this pin is expected to be 2.775V typically to obtain sufficient compliance. This will drive external loop filters, which will in turn drive external VCOs. A dual port modulation mode is obtained with a 9 bit D/A which follows the modulation look up table output waveform is output on the GPO3 pin.This signal is then coupled into the loop filter to add in the higher frequency components of the modulation which may have been attenuated in the main PLL path. This will allow the use of a lower bandwidth main PLL to improve the spectral purity of the transmit signal.For EGSM the synthesizer output is 880 - 915MHz, DCS is 1710 - 1785MHz with GMSK modulation and is directly amplified to the transmitter output.

The prescaler for the main LO is able to accept input frequencies as high as 2.0GHz. The level of this signal shall be between -20dbm and -10dbm. There are two prescaler inputs to this point each has a 100W resistor in series between the pin and the actual prescaler input.

The reference oscillator is a free running 26MHz crystal. AFC is provided through the SPI bus as a programming offset to the fractional N division system. Since the 26MHz crystal is not locked to the AFC, a second fractional divider system is necessary to derive an accurate 200KHz system reference. This reference is then multiplied in a PLL to 13MHz for use as an accurate clock to the logic sections of the transceiver.

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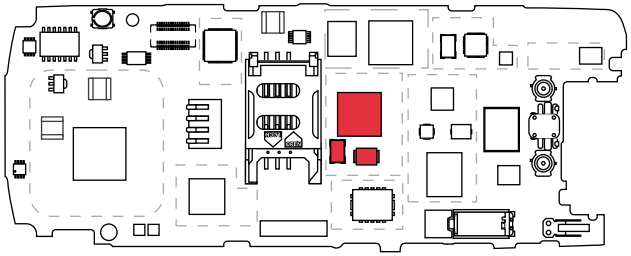
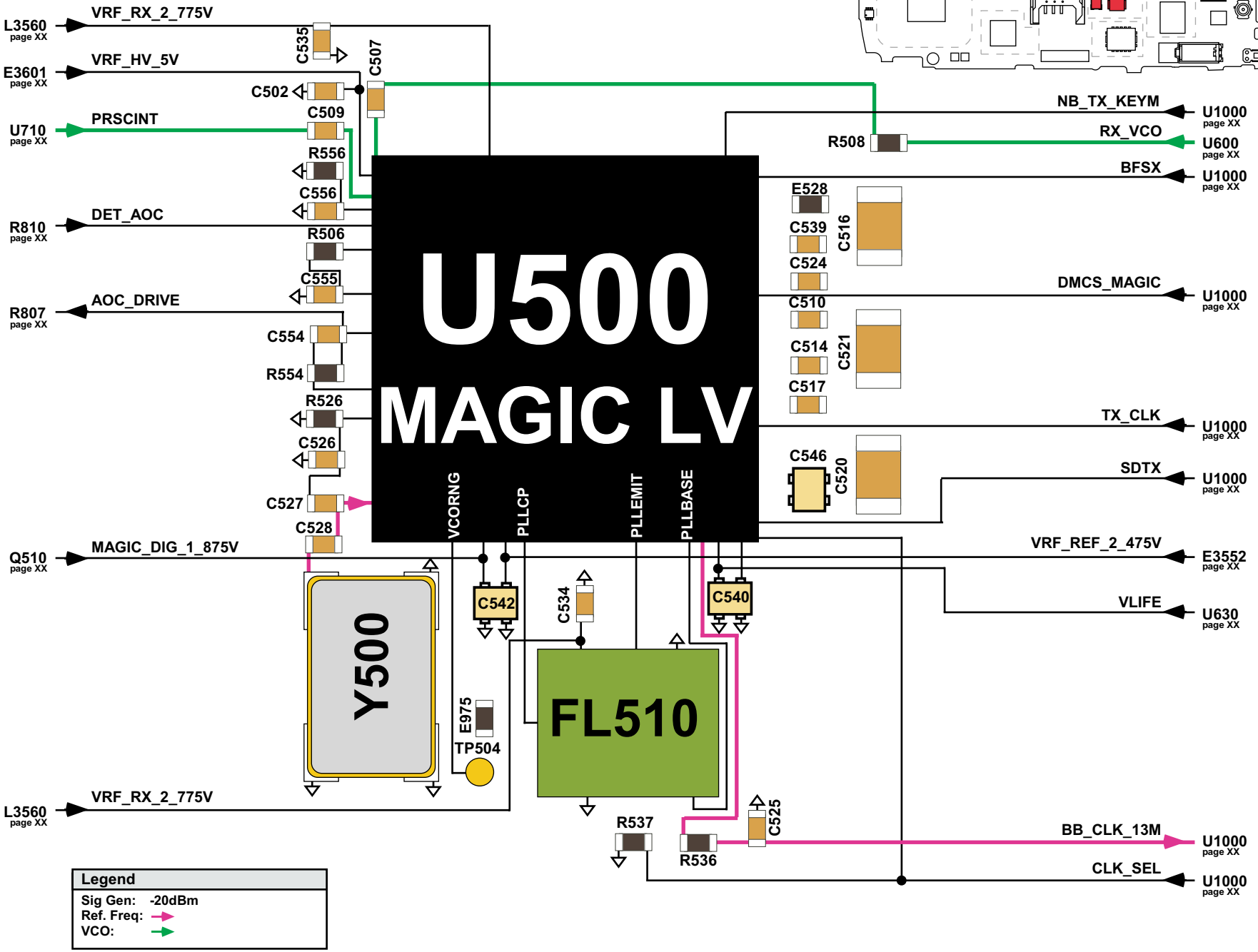
A920: Magic LV (Synthesizer/Transmitter)





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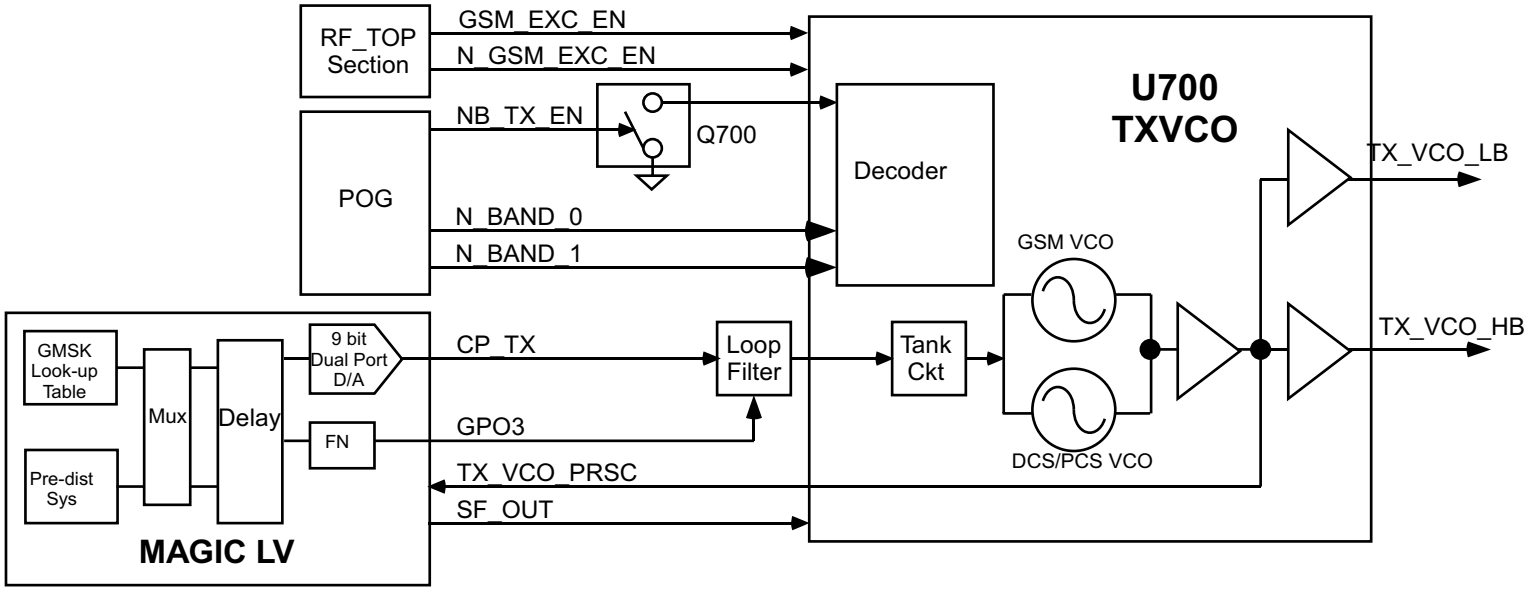
A920: GSM TX VCO



Description

The VCO frequencies are 897 - 1880MHz, handling the three technology bands. The technology bands are controlled by MAGIC_LV via the data lines: N_BAND_0 and N_BAND_1. CP_TX and GPO3 provides a dual port modulation mode for the TXVCO. N_BAND_0 and N_BAND_1 will select which VCO band will be activated. GSM_EXC_EN and N_GSM_EXC_EN will enable the buffer stage of U570. TX_EN is activated prior to enabling the buffer and PA. TX_VCO_PRSC is fed back to the MAGICLV for proper PLL operation. The output frequency for GSM is TX_VCO_LB and PCS / DCS is TX_VCO_HB. The charge pump output (CPTX) from MAGIC_LV is the input (VT) for the VCO.

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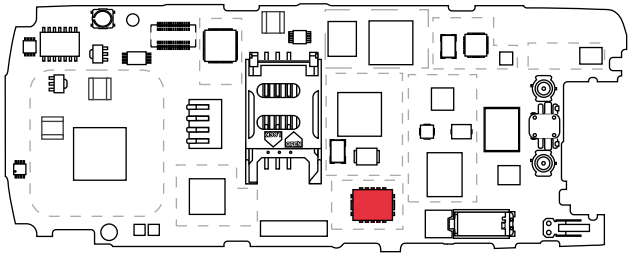
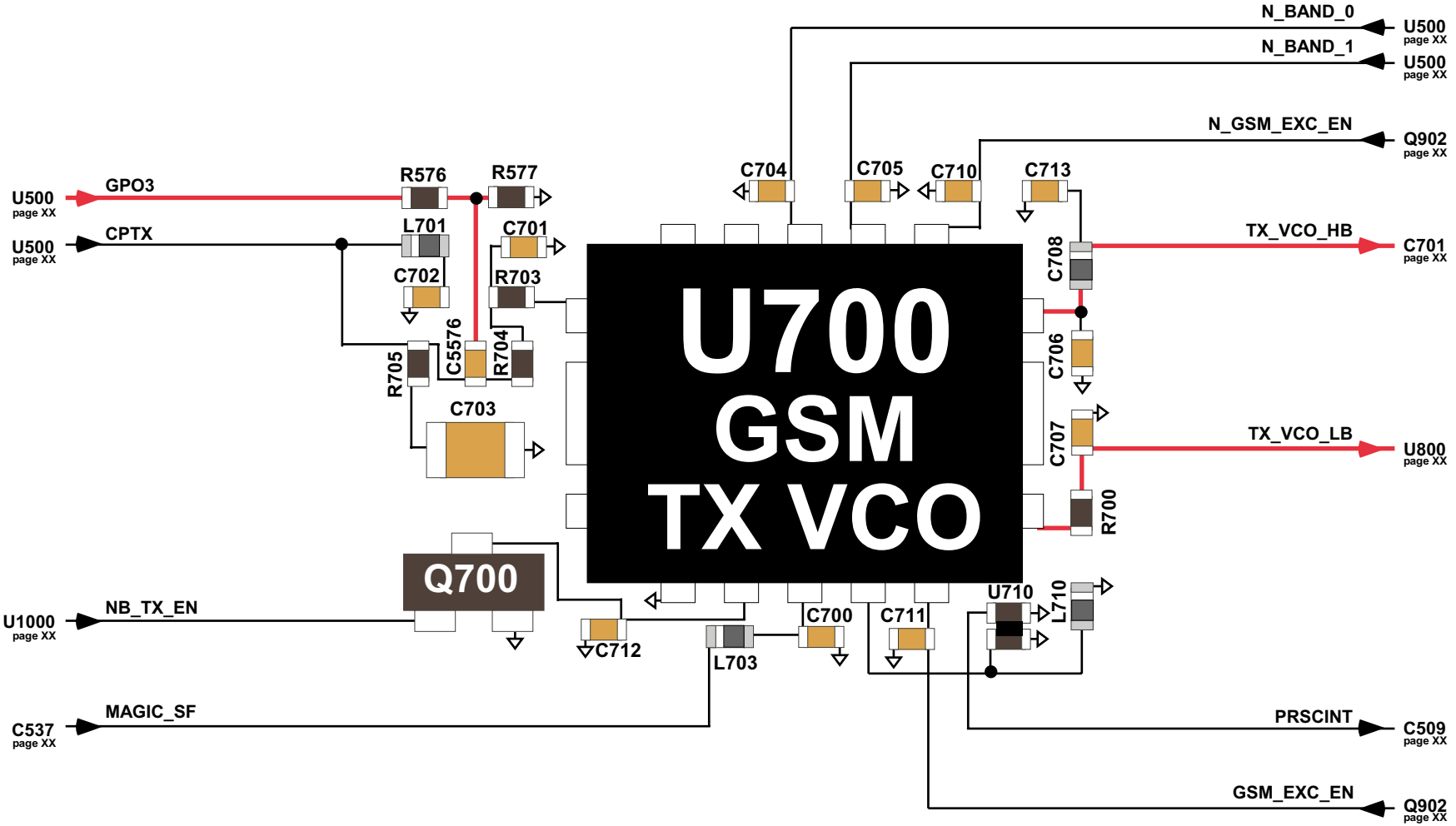
A920: GSM TX VCO





Legend	
Sig Gen:	-20dBm
TX:	→

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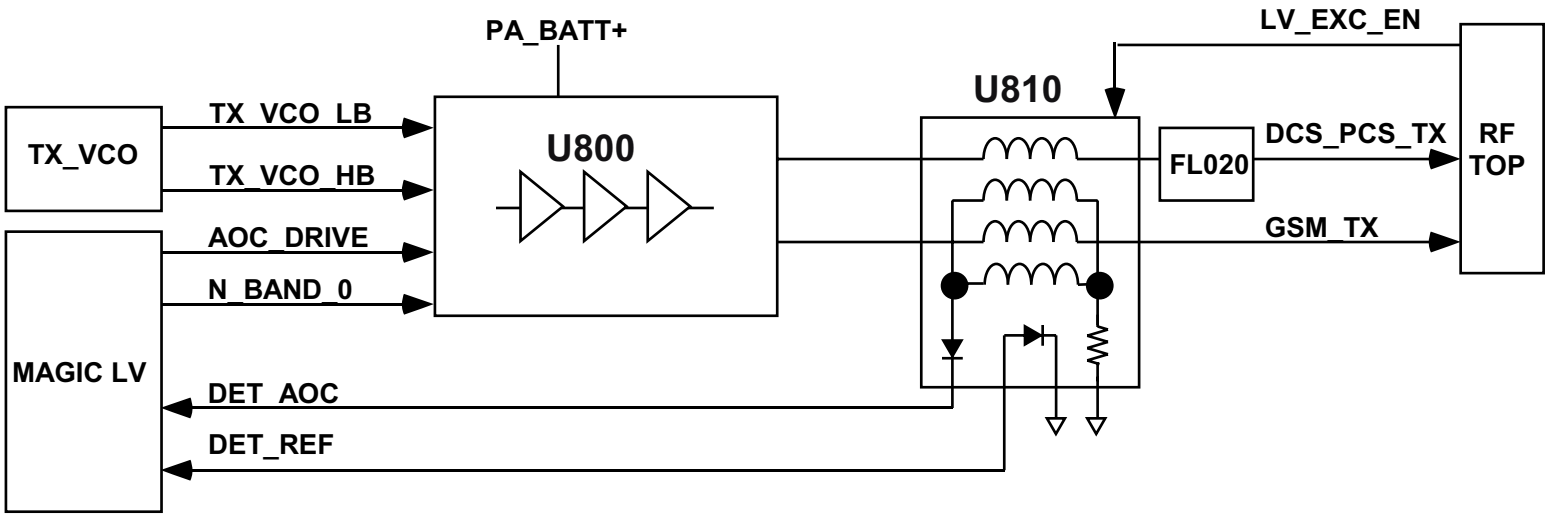
A920: GSM PA



Description

U800 is a tri-band PA module that operates in EGSM, DCS and PCS bands. The nominal expected maximum gain is ~30dB. .
The AOC_DRIVE input from MAGIC_LV controls the PA output. The voltage applied at the pin is proportionally related to the output power of the PA, as the voltage increases the gain or power level increases. N_BAND_0 is used to select the operating band. LV_EXC_EN will enable PA operation.

The power detector receives the amplified GSM signal at #1 (EGSM_IN), PCS and DCS at pin #12 (DCS_PCS_IN) from the U800. U810 is a dual combination directional coupler and temperature compensated power detector output. The power detector couples the Tx power input and feedbacks an output DET_AOC to MAGIC_LV. A comparator within the MAGIC LV will sample DET_AOC and based on the power amplifier ramps will provide any necessary control voltage adjustments to AOC_DRIVE The DET_REF is a reference voltage to MAGIC_LV. Expected nominal loss is <. 3dB.

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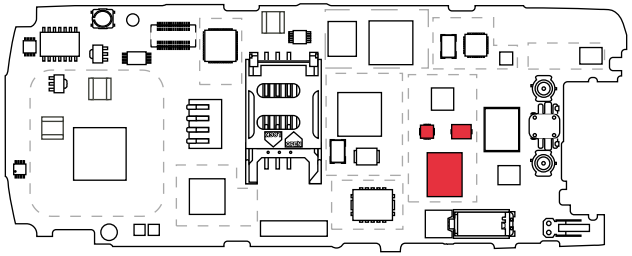
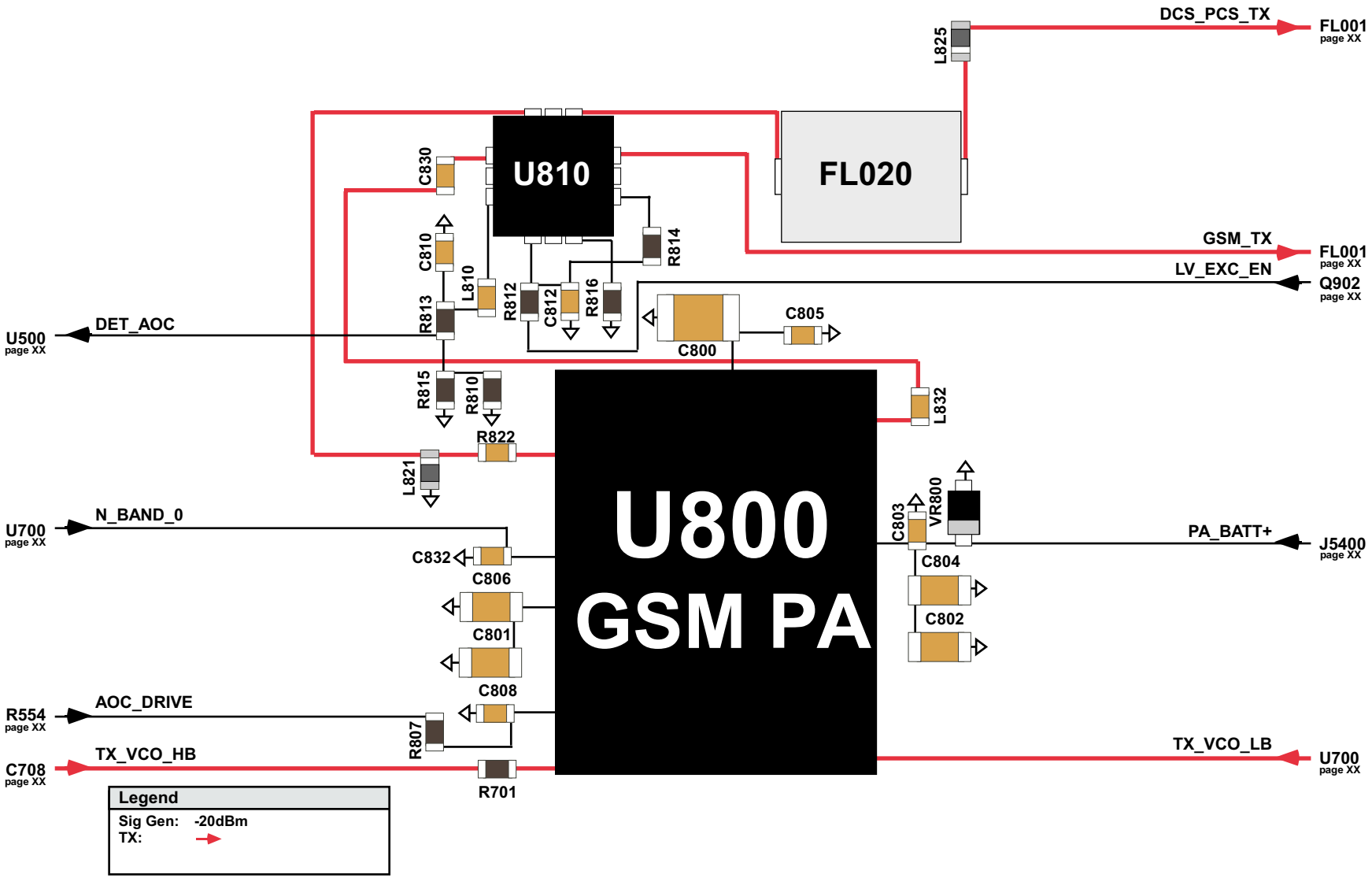
A920: GSM TX





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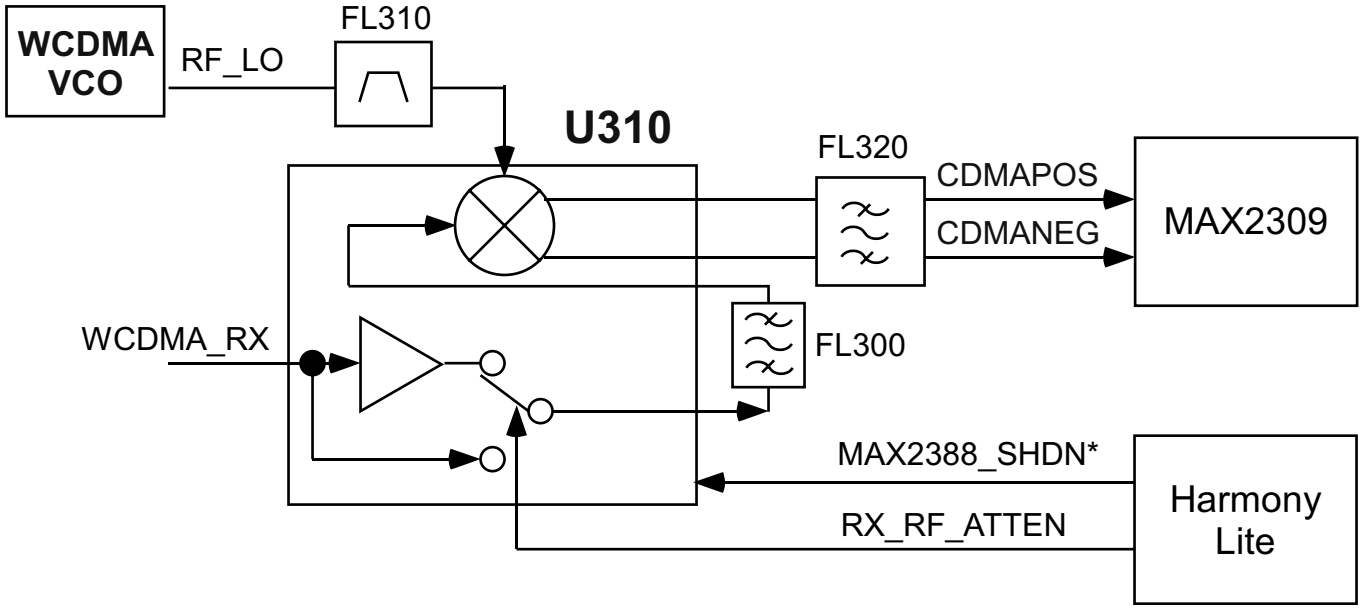
A920: WCDMA RX Downconverter (MAX2388)



Description

The first IC in the WCDMA Rx line up is U310 (MAX2388), which is an LNA and down converter mixer combination. The RX frequency will be mixed down to an IF frequency of 190MHz. The MAX2388 also has a shutdown mode to power down the IC, via MAX2388_SHDN*, during the front-end receiver's idling period to conserve battery life. U310 operates from the PCAP supply voltage RC_VCCA (derived from VRF_RX_2_775V). The nominal gain expect is ~15dB.

U310 operates in high gain mode selectable from RX_RF_ATTEN by the HARMONY_LITE . The nominal gain expected while in this mode is 15dB. During high input signal levels the LNA will be off.

The receive mixer is a wideband, single-balanced design. The input RF_LO (pin #5) receives the VCO frequency (2330 - 2360MHz) through FL310 from U140 (VCO). The RF input (LNA_IN, pin #10) receives the RX frequency (2110 - 2170MHz) from FL002.

The MIX_IN (pin #3) input is connected to LNAOUT (pin #1) through FL300. The function of FL300 is to provide image rejection and out-of-band interferers filtering. The frequency conversion process performed by the mixer / oscillator combination sometimes will allow a frequency other than desired frequency to be fed into the IF and subsequently amplified.

The IF mixer output (190MHz) appears on the differential IFPOS (pin #8) and IFNEG (pin #7). These open-collector outputs require an external inductor (L320 & L321) to VCC for DC biasing.

The 190MHz IF frequency passes through FL320. The IF SAW filter has a nominal center frequency of 190MHz and a bandwidth of 3.84MHz. Between the input match (C323, C324 & L322), output match (L327, L328, C328, C329, & C325) and the filter (FL320)- the expected nominal losses is ~10dB.

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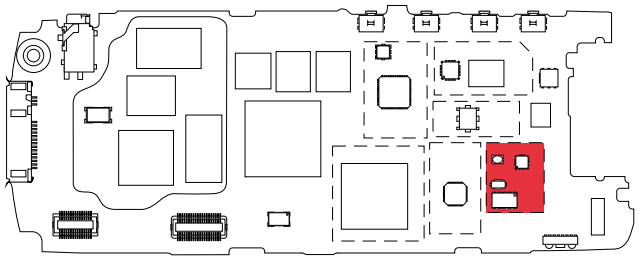
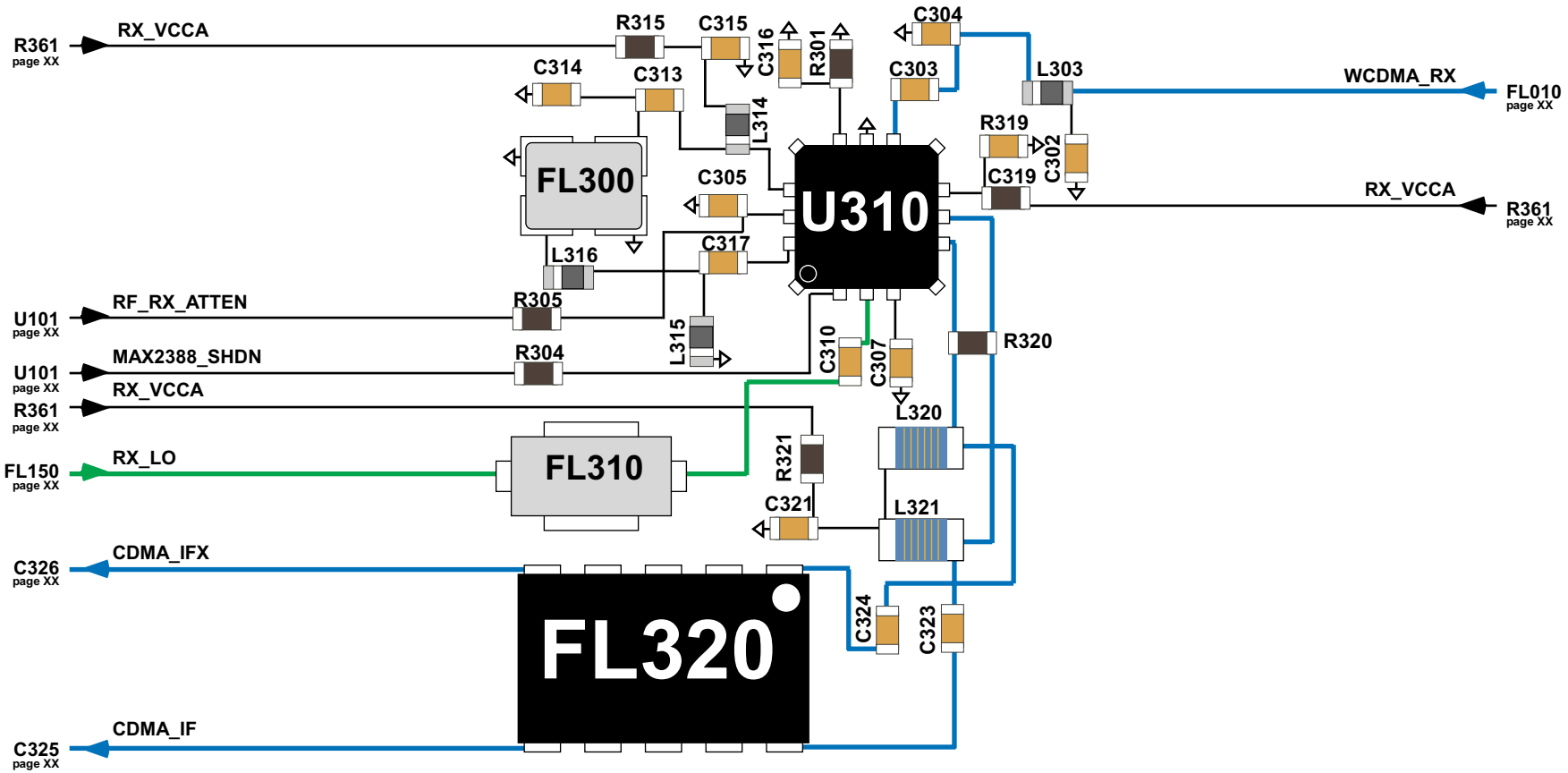
A920: WCDMA RX Front End





Legend	
Sig Gen:	-20dBm
RX:	→
VCO:	→

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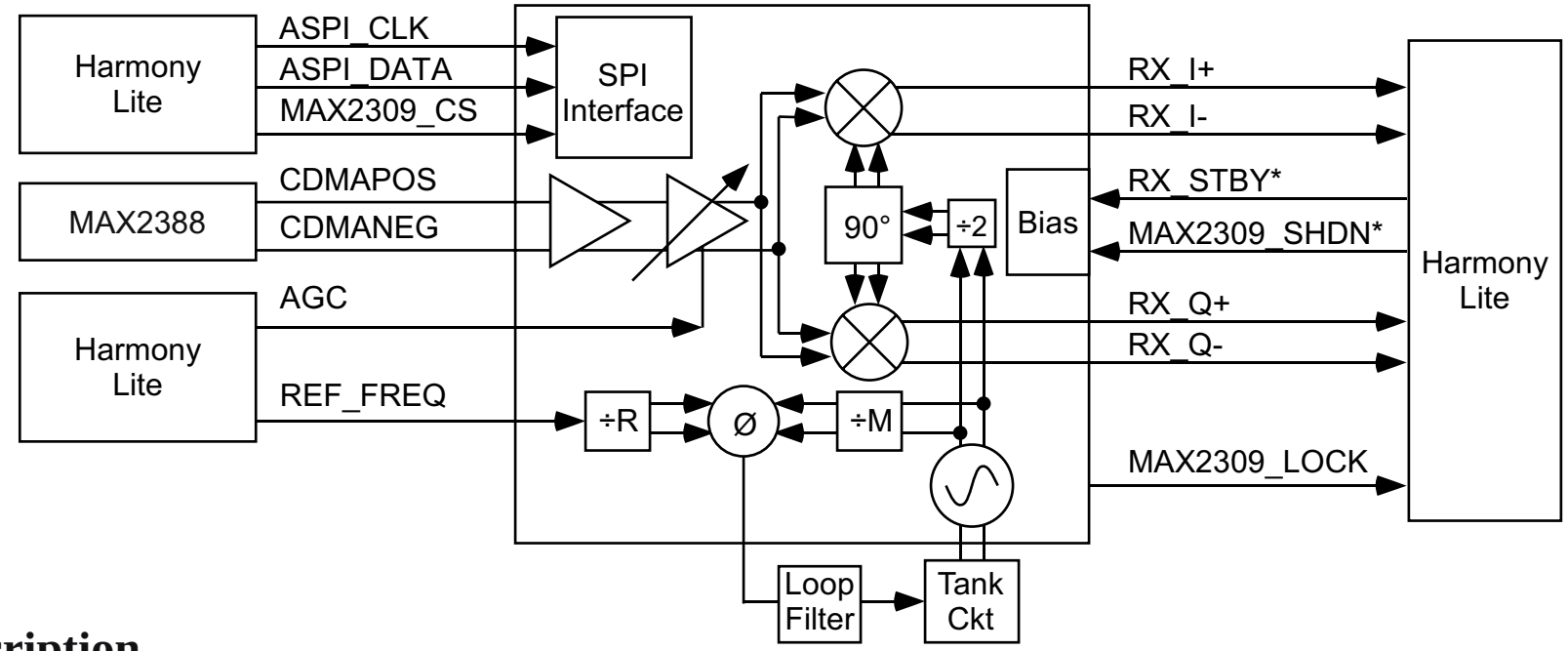
A920: WCDMA RX Demodulator (MAX2309)



Description

The MAX2309 is an IF quadrature demodulator with the signal paths consisting of a variable-gain amplifier (VGA) and an I/Q demodulator. The IF LO synthesizer's reference and RF dividers are fully programmable through the 3-wire serial bus (ASPI_CLK, aSPI_DATA, MAX2309_CS). The 190MHz IF is demodulated to BaseBand differential in phase (I+ / I-) and quadrature (Q+ / Q-) signals to be passed through to the receiver's backend IC, HARMONY LITE. The IC operates from a pair of supply voltages RX_VCCD & RX_VCCA derived from VRF_RX_2_775V.

The MAX2309 VCO output frequency is controlled by an internal phase lock loop (PLL) synthesizer. The external loop filter consists of the components connected to pins #1 and #2 (& pin #26). The VCO output frequency (Tank+ / Tank-) at pins #1and pin #2 are divided down internally, to a desired comparison frequency. The reference signal at pin #7 (REF_15.36MHz) is also divided down to the same comparison frequency. The two divided signals are compared with a three state digital phase detector. The internal phase detector drives the charge pump as well as the lock-detect logic. The charge pump output at pin #26(CP_OUT) is processed by the external loop filter and drives the tunable resonant network, altering the VCO frequency (380MHz) and closing the loop.

The AGC ensures that the I/Q inputs to HARMONY LITE are at constant signal level. The IF_AGC line is controlled by HARMONY_LITE with a DC control range of 1.2V to 2.1V.

The MAX2309 has a shutdown mode to power down the IC, via MAX2309_SHDN*, during the front-end receiver's idling period to conserve battery life. RX_STBY* is used to shut down VGA and demodulator while maintaining the VCO, PLL, and serial interface active.

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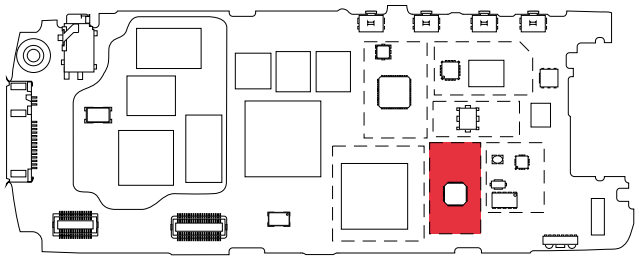
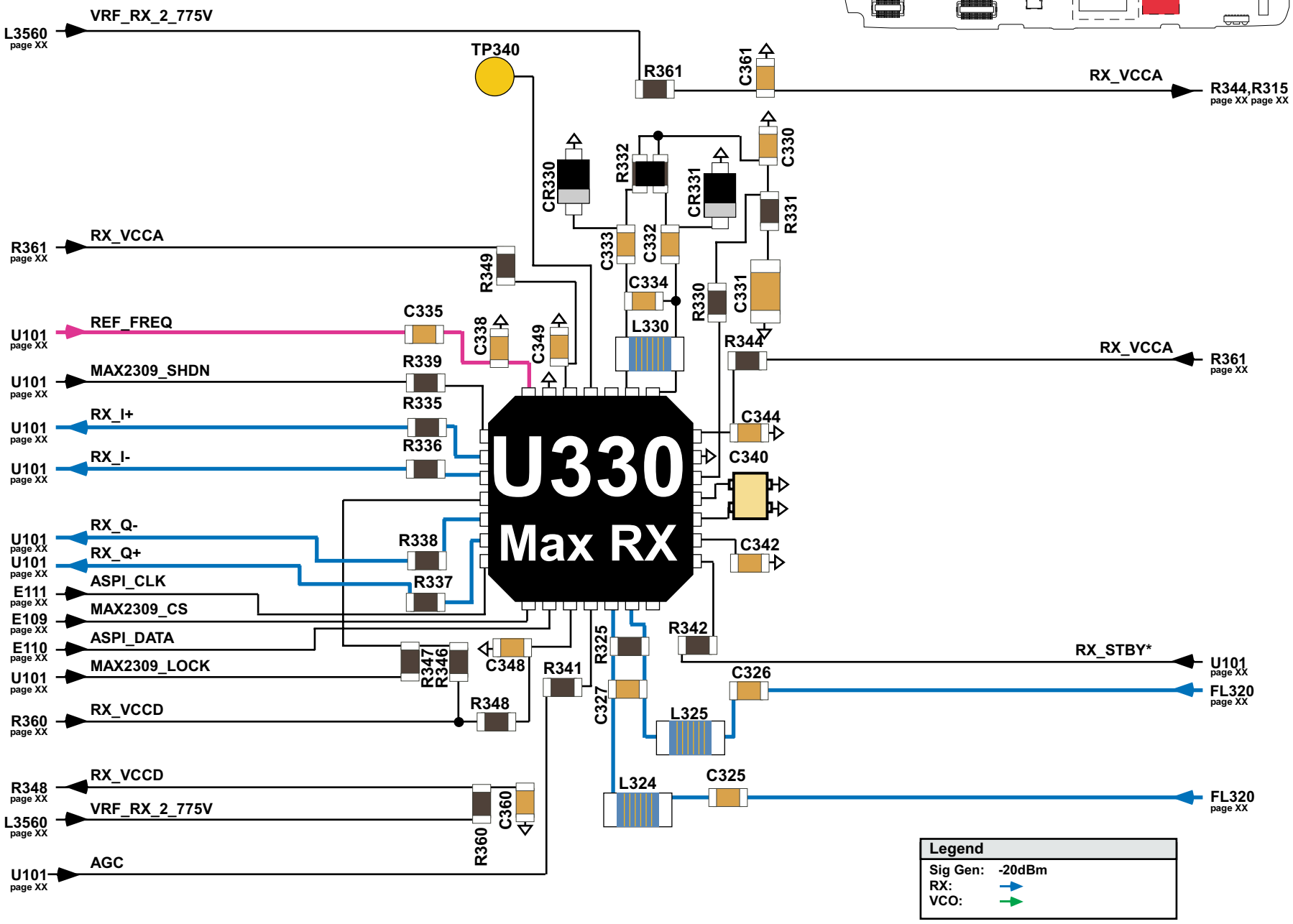
A920: WCDMA RX MAX2309





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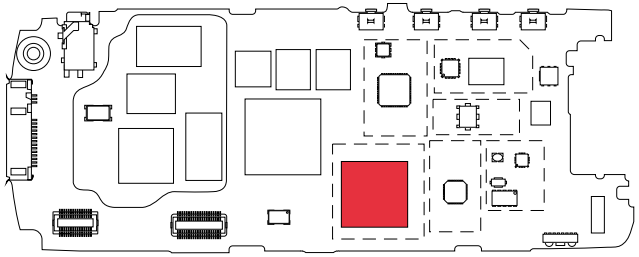
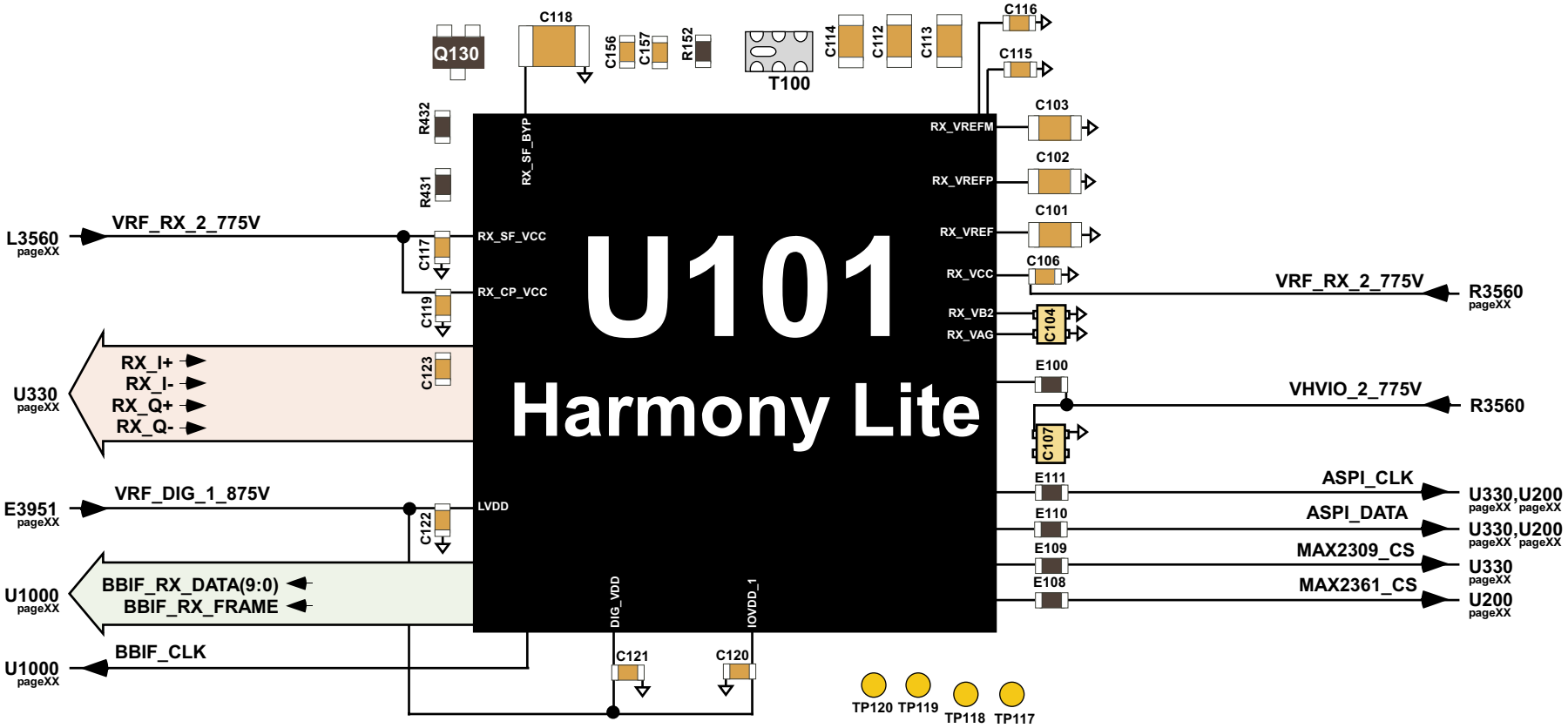
A920: Harmony Lite (RX Section)





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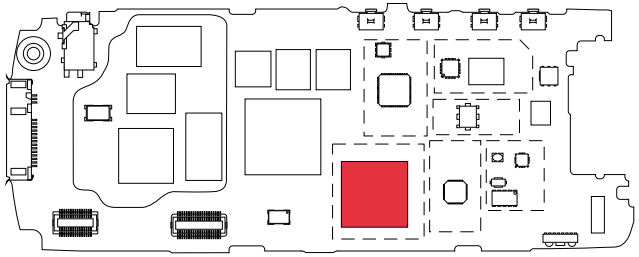
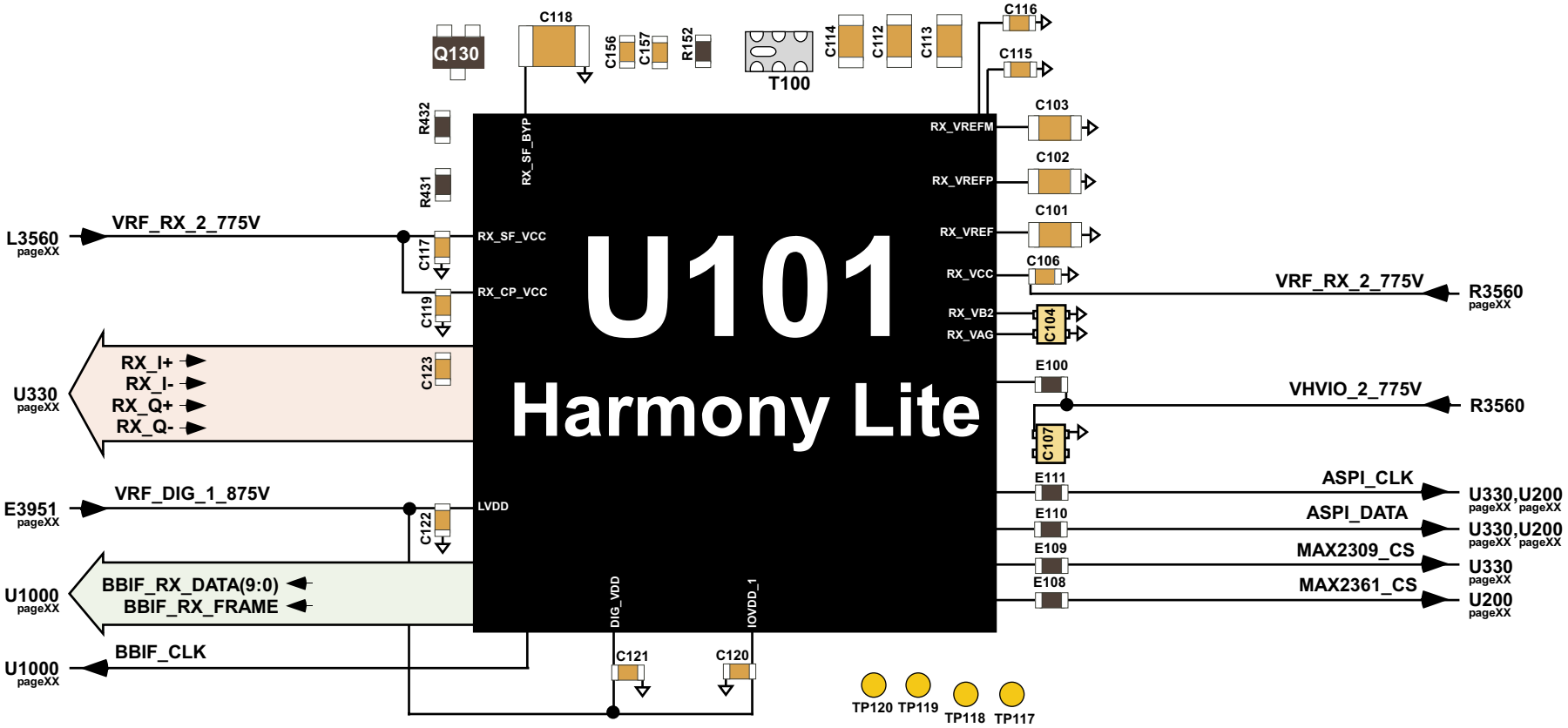
A920: Harmony Lite (RX Section)





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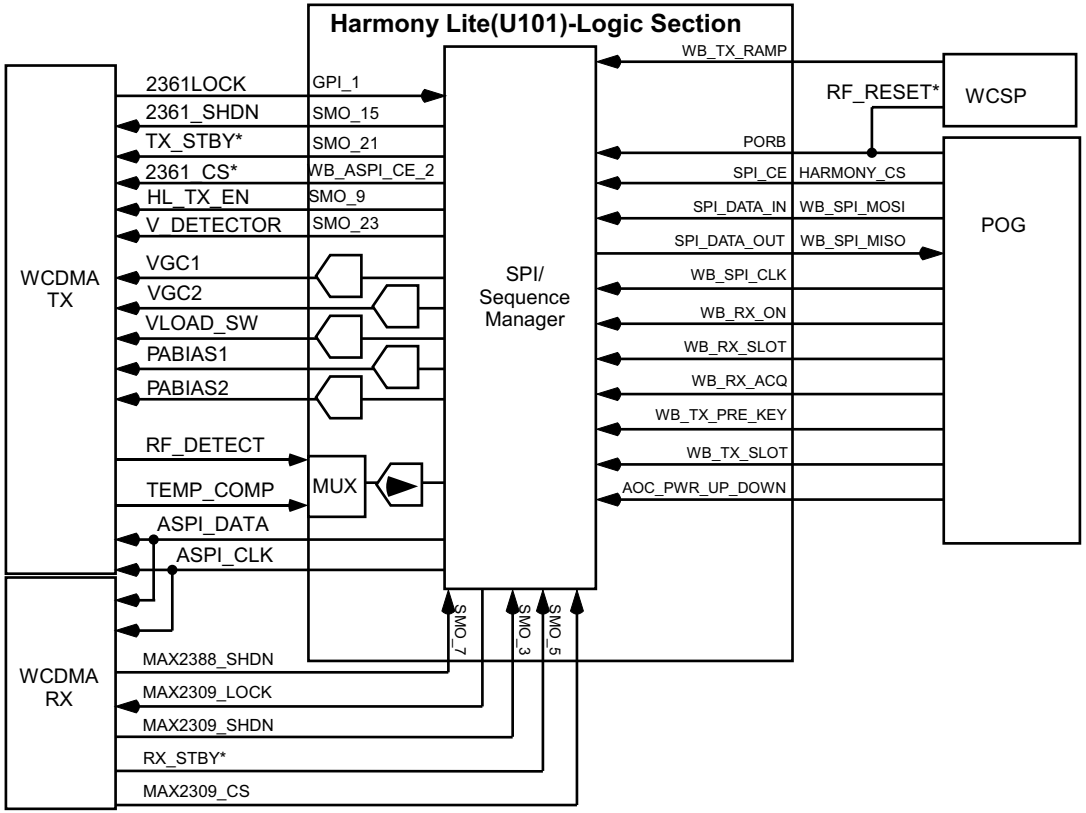
A920: Harmony Lite (Control Section)



Description

There are several functions that the sequence manager is controlling.

1. Sequence manager outputs to external devices
2. On/Off control of clocks, battery save signals etc…
3. Clock frequency selection for correction paths
4. DCOC register selection coarse, medium and fine modes

The HARMONY LITE has two sets of SPI interfaces; one set is for handling the control interface for the transceiver (AUXSPI lines) and ones for interfacing with POG (SPI lines). Further, all SPI interface is generated from POG and written to HARMONY_LITE or parsed through to the MAXIM (U200 & U310) parts.

Layer one timing signals control the functionality of the RF section of the transceiver relative to the air interface. There are three signals defined on each transmit and receive section of the transceiver. TX_PRE_KEY and RX_ON are asserted before the need to receive or transmit in order to launch the necessary sequence of events to warm up the required functional blocks. TX_RAMP and RX_AQUIRE are asserted when actual transmission and reception are to begin. RX_SLOT and TX_SLOT are used during continuous transmission and reception to trigger events that must be aligned with slot boundaries. It‘s important to reiterate, the TX_RAMP directly corresponds to the PA turning on and RX_AQUIRE corresponds to data being sent to the WCSP.

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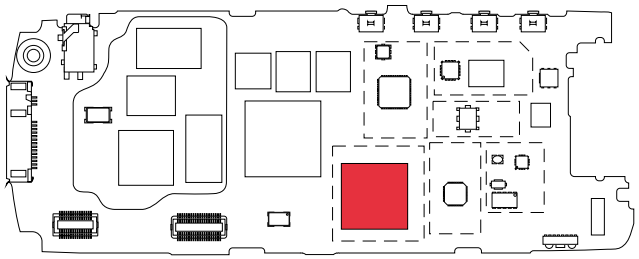
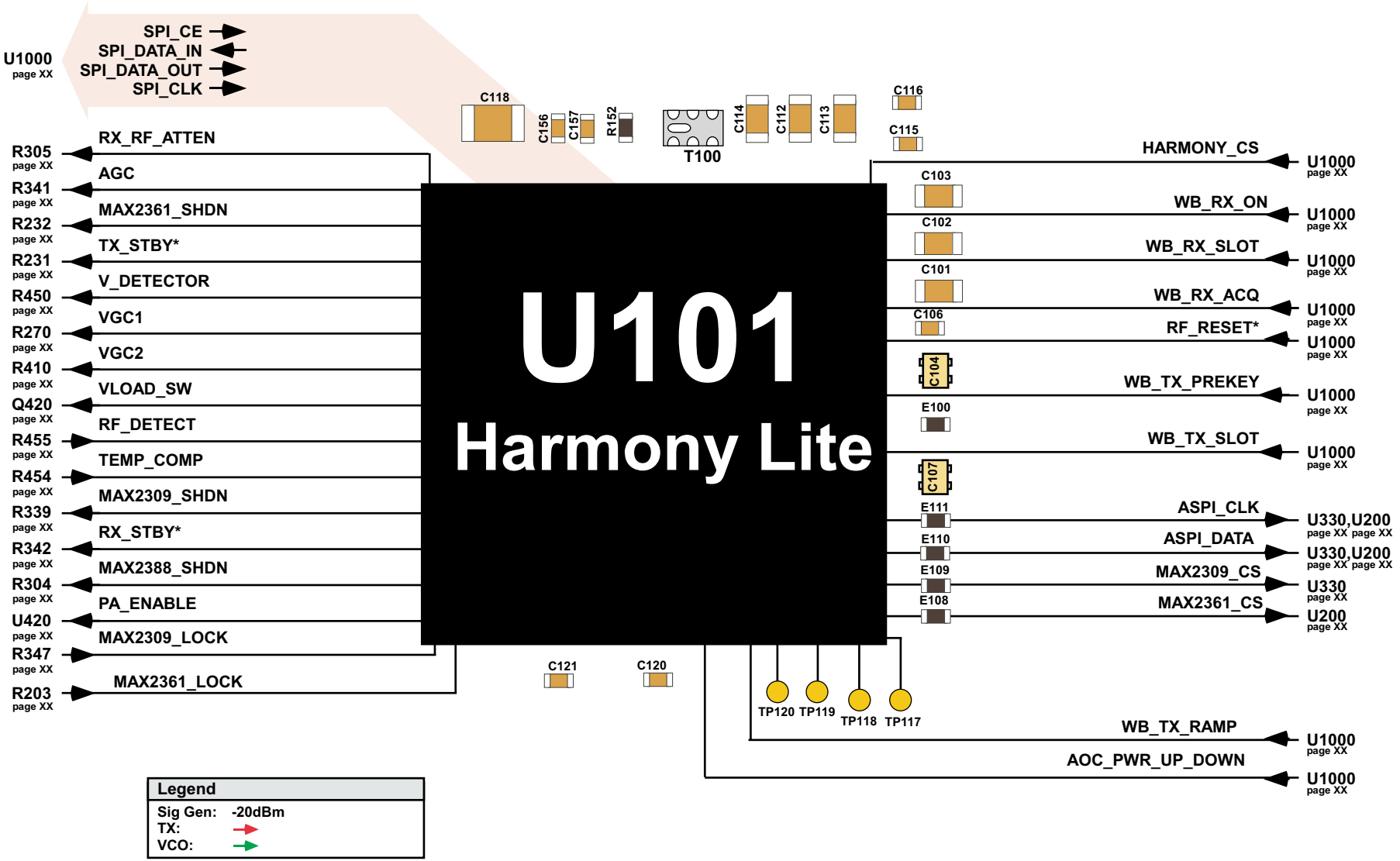
A920: Harmony Lite (Control Section)





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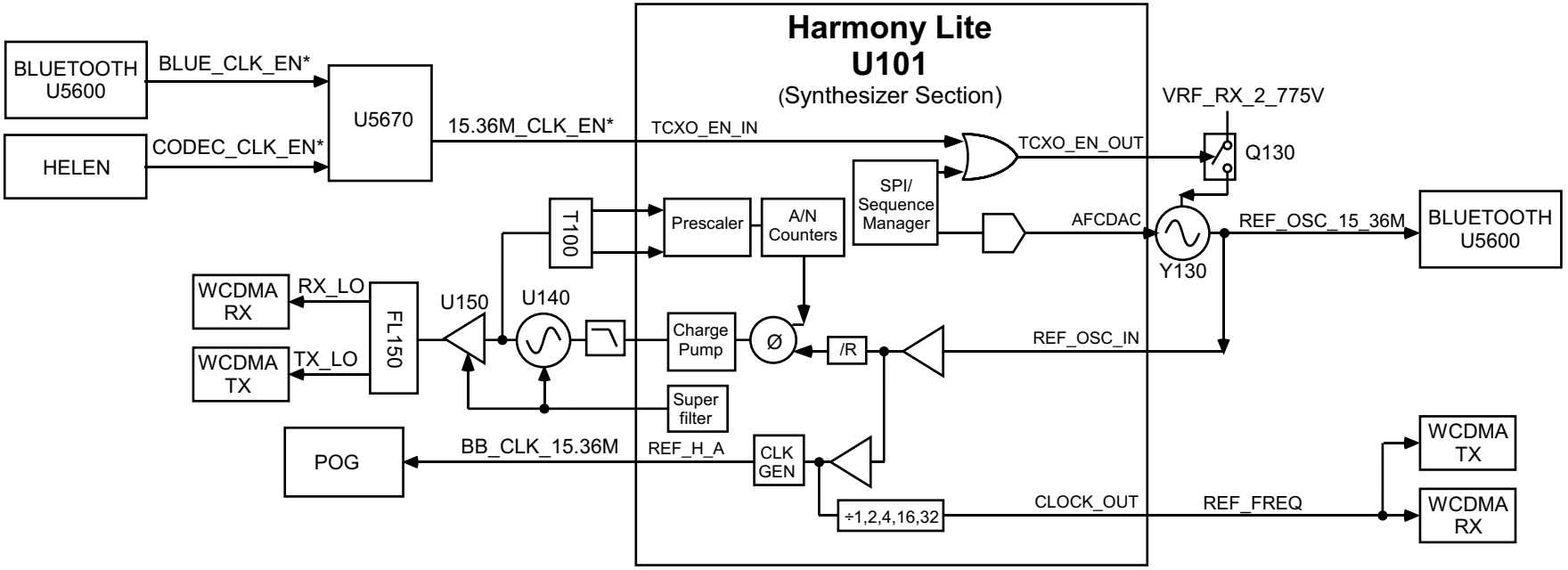
A920: Harmony Lite (Synthesizer Section)



Description

The clock source for the Harmony Lite (HLite) is a 15.36Mhz oscillator (TCXO). Y130 is used to generated the 15.36MHz clock source. AFC for Y130 is controlled by the Harmony Lite sequence manager via the AFCDAC line. The 15.36MHz clock source is enabled by an internal SPI bit and external control signal coming from 15.36M_CLK_EN*). The 15.36MHz clock source provides clocks to all A/Ds, DACs, external references and internal digital circuits of the Harmony Lite. In addition, clock references are generated for the POG, RX and TX RF circuits.

The WCDMA VCO(U140) has a frequency range of 2.3G thru 2.36GHz, supplying both the receiver and transmitter with an LO. The control range is controlled by HARMONY_LITE with a control range between 0.5 - 2.5V, with an output power @ ~-3 - 3dBm. The WCDMA VCO output frequency is controlled by an internal phase lock loop (PLL) synthesizer. The phase locked loops use a fractional loop divider to permit fast lock times and low phase noise on their output signals. The VCO output frequency is fed into a prescalar and devided down into a desired comparison frequency. The 15.36MHz reference frequency is also divided down into a comparison frequency. The two divided frequencies are then compared with a phase detector. The phase detector will then drive the charge pump. The charge pump output is processed by the external loop filter and drives the tunable resonant network, altering the VCO frequency and closing the loop.

The superfilter block is used to provide a filtered supply voltage to the WCDMA VCO.

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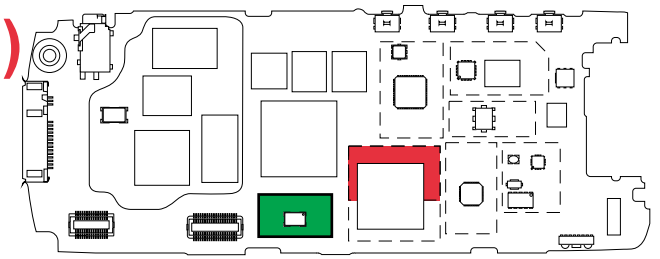
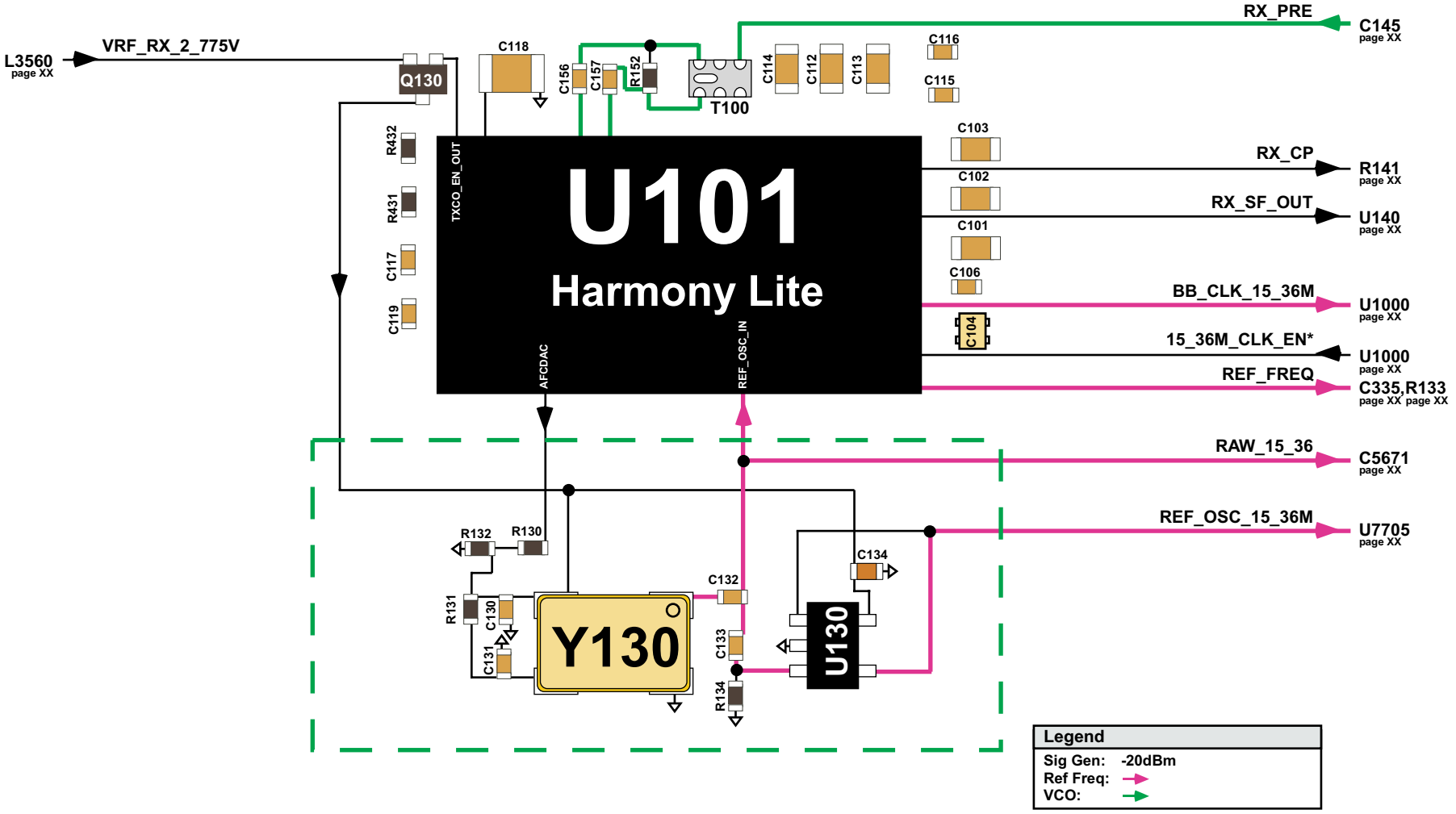
A920: Harmony Lite (Synthesizer Section)





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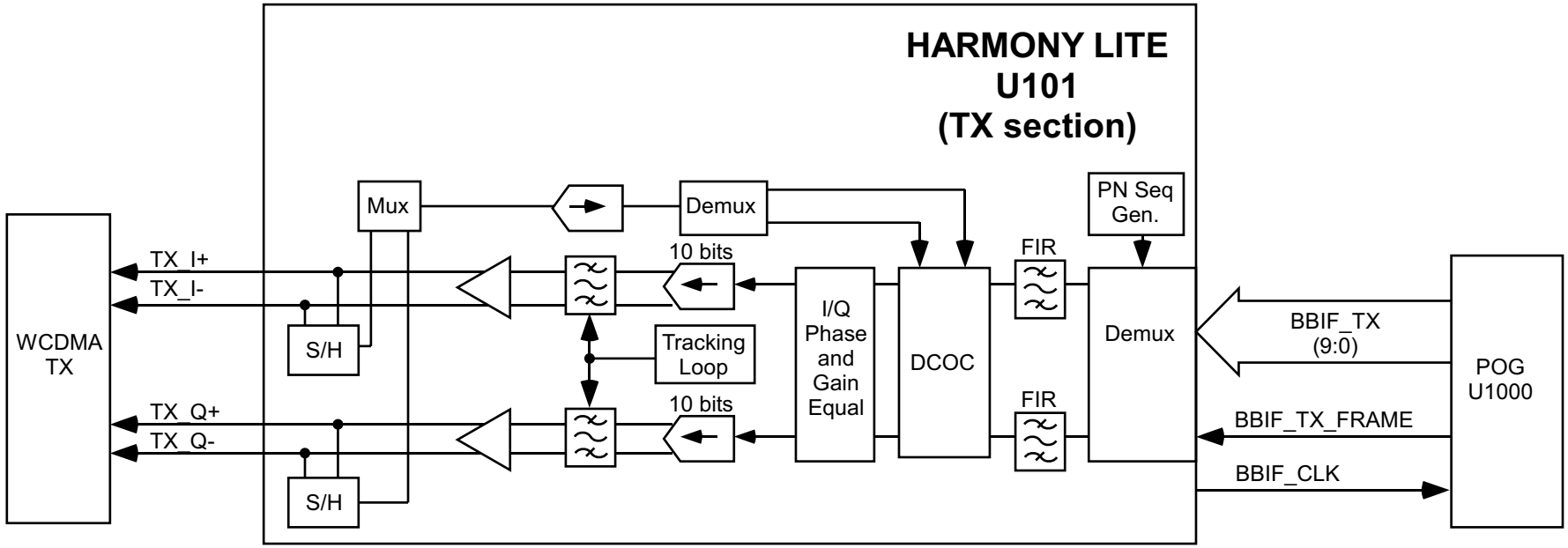
A920: Harmony Lite (TX Section)



Description

The BBIF(BBIF_TX) is the transmit data path for transferring digitally sampled I / Q data from the POG. The demultiplexing unit performs the I/Q deinterleaving function to supply separate I and Q channel data into the transmit FIR filters. The FIR filter design is used to meet 3GPP spec requirements of simultaneous transmission of a pilot channel and of multiple data channels each requiring a different spreading code and each requiring separate power control. The PN sequence generator provides I/Q interleaved 8-bit PN data into the demultiplexing section. The DC correction(DCOC) block is able to correct for DC offsets due to the D/A‘s, anti-aliasing filters, and transmit FIR filters in a feedback control loop. A mixed mode control loop located at the output of the transmit FIR filter is employed to correct DC offsets and I/Q gain imbalances, i.e. DCOC and I/Q Phase and Gain equalizer. The outputs of the I/Q gain equalization unit is fed into 10-bit I and Q DAC‘s. The programmable gain anti-aliasing filters, or TX smoothing filters, accepts differential I/Q signals of DC to 1.92MHz frequency components from the D/A Converters to attenuate the unwanted clock signals of 15.36MHz and to smooth the signals for the TX modulator(MAX2363). The output of the TX smoothing filters are then fed into a multiplexed 6-bit A/D with sample/hold scheme. This gives the information of the amplitude and the DC common mode voltage from the I / Q Tx filter outputs by a single Analog-to-Digital Converter (ADC) as the part of digital correction loop.

The differential TX I and TX Q signal are finally fed into the TX modulator(MAX2363).

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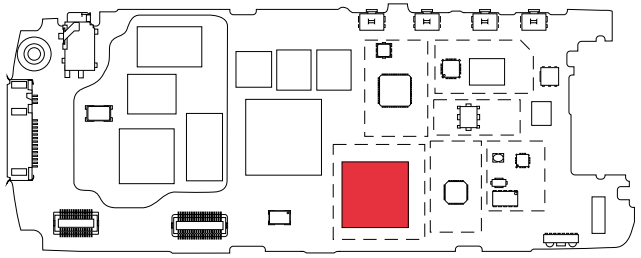
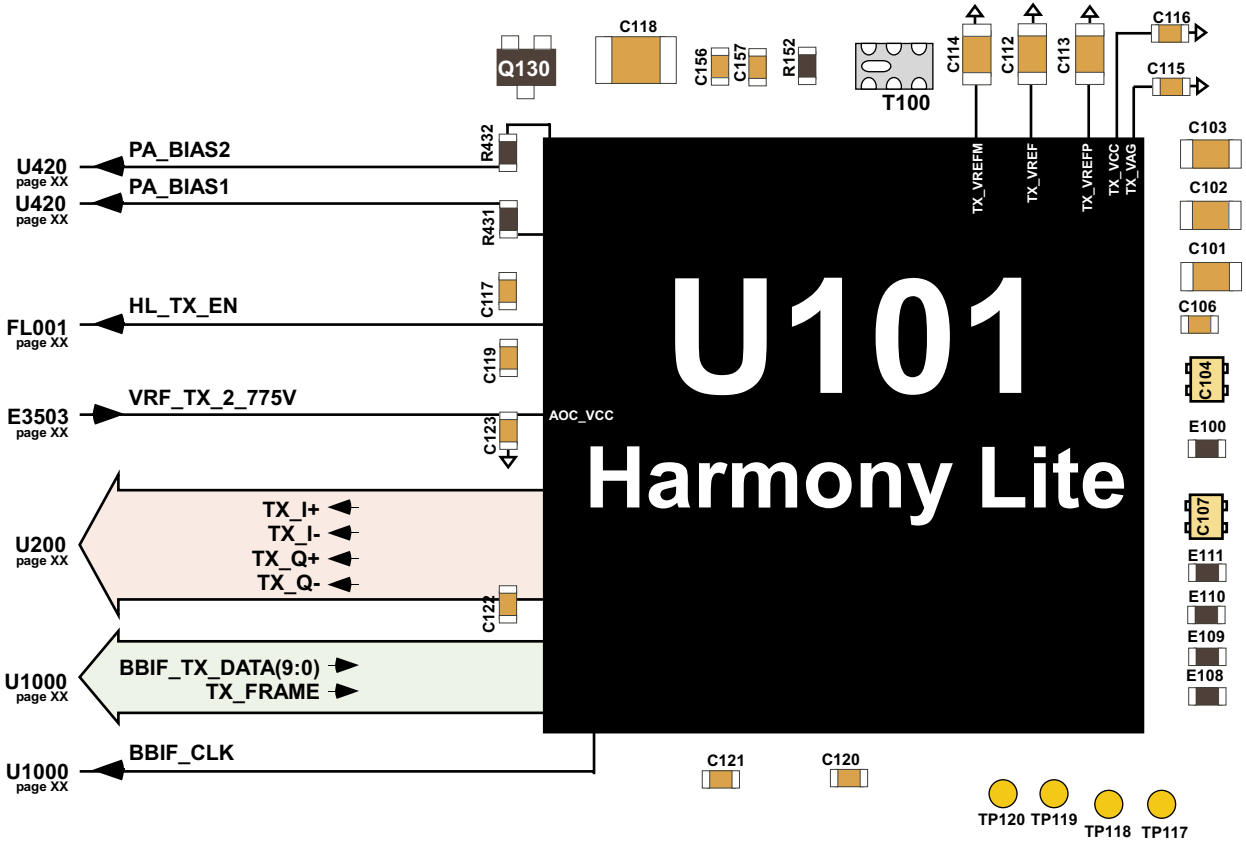
A920: Harmony Lite (Transmitter Section)





Legend	
Sig Gen:	-20dBm
TX:	→
VCO:	→

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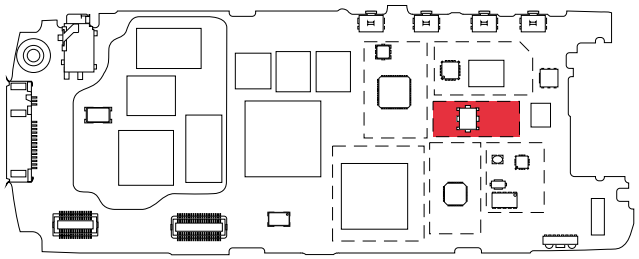
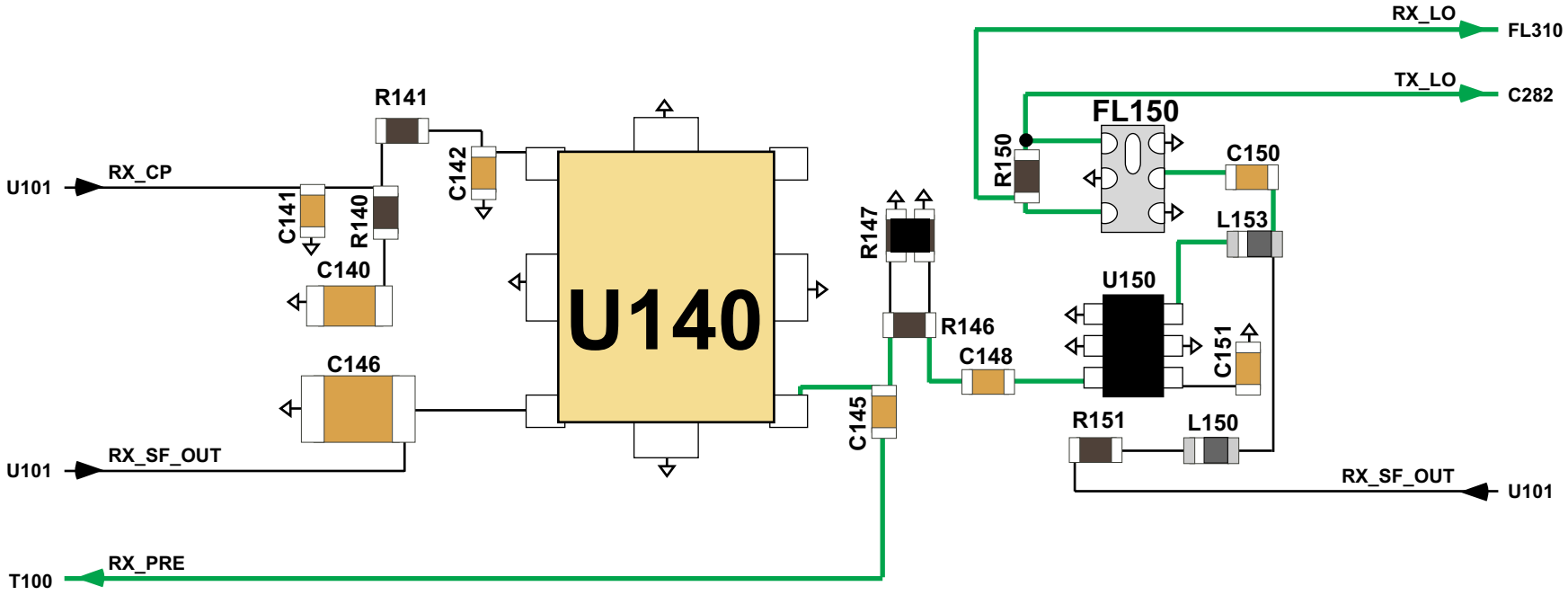
A920: WCDMA VCO





Legend	
Sig Gen:	-20dBm
VCO:	→

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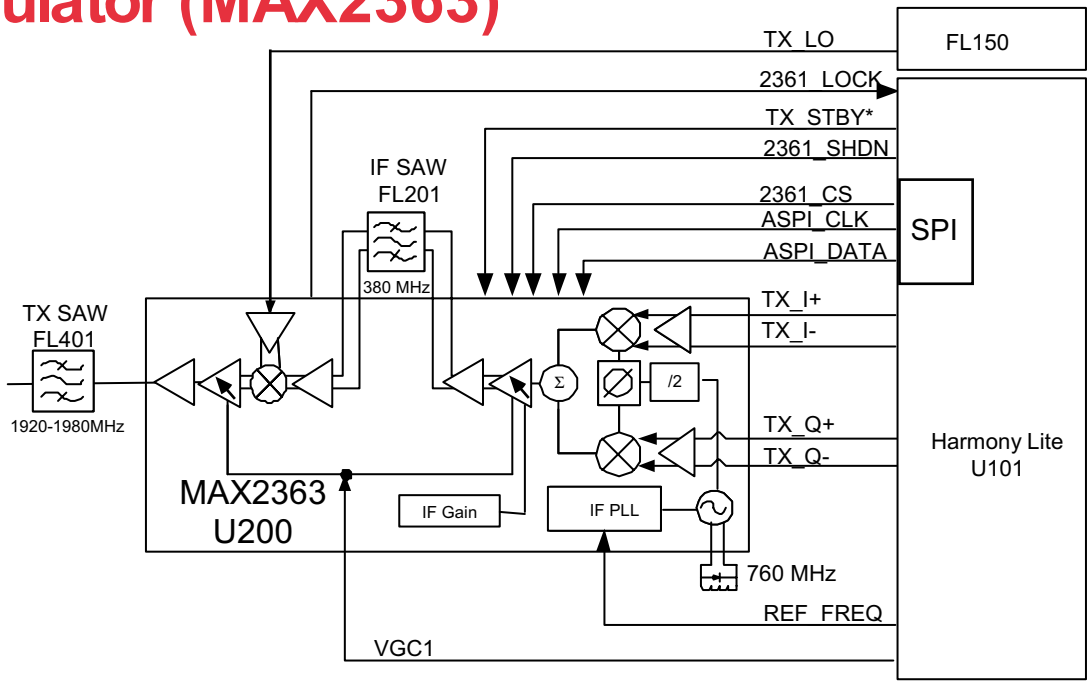
A920: TX Modulator (MAX2363)



Description

The in phase (I) and quadrature phase (Q) inputs are received at pins #23 (Q+), #24(Q-), #25(I+), & #26(I-) of U200. The expected DC bias levels are 1.30V - 1.40V with a minimum 300mVpp signal upon the DC level.

The MAX2363 receives the differential I/Q BaseBand input and converts it up to the IF frequency of 380MHz through a quadrature modulator and IF variable gain amplifier (VGA). The IFINH+ (pin #10) and IFINH- (pin #11) input are connected through off-chip FL201 from IFOUT+ (pin #17) and IFOUT- (pin #16), respectively. The function of FL201 is to provide image rejection and out-of-band interferers filtering. The frequency conversion process performed by the mixer / oscillator combination sometimes will allow a frequency other than desired frequency to be fed into the IF and subsequently amplified. The SAW filter (FL201) has a nominal center frequency of 380MHz and an insertion loss of ~ 3.5dB with a total bandwidth of 5MHz.

The IF and RF VGA (VGC1) are common and allow for varying the IF / RF output level . HARMONY_LITE controls the VGC signal with a range of ~1.3 - 2.6V and provides gain a control range of ~75dB.

The MAX2363 VCO output frequency is controlled by an internal phase lock loop (PLL) synthesizer. The external loop filter consists of the components connected to pins #33 and #32 (& pin #38). The VCO output frequency (TankH+ / TankH-) at pin #33and pin #32 are divided down internally, to a desired comparison frequency. The reference signal at pin #36 (REF_FREQ) is also divided down to the same comparison frequency. The two divided signals are then compared with a three state digital phase detector. The internal phase detector drives the charge pump as well as the lock-detect logic(2361_LOCK). The charge pump output (IFCP, pin # 38) is processed by the external loop filter and drives the tunable resonant network, altering the VCO frequency (760MHz) and closing the loop.

The differential IF output at pins #17 & #16 (IFOUTH+ / IFOUTH-) support high IF operation of frequency of 380MHz. The signal is routed to an off-chip IF SAW filter (FL201) and up-mixed to RF through an image reject mixer and RF VGA. The signal is further amplified with an on-chip PA driver. The RF signal is then routed to an interstage RF SAW filter (FL401).

The IF synthesizer (760 MHz VCO) and local oscillator (RF_LO) buffer are both programmable through the 3-wire bus. The sequence manager from HARMONY_LITE programs standby mode(TX_STBY*) and shutdown mode(2361_SHDN). This IC operates from a pair of supply voltages VCC_DIG (isolated supply for IF_CP and 760 VCO) & VCC_ANA derived from VRF_TX_2_775V.

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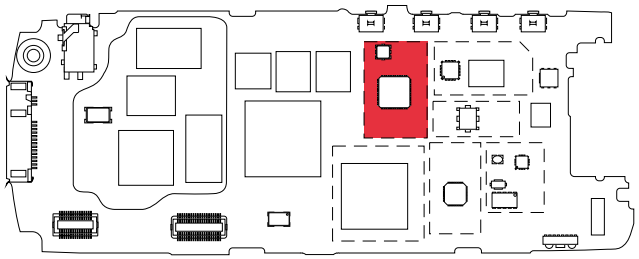
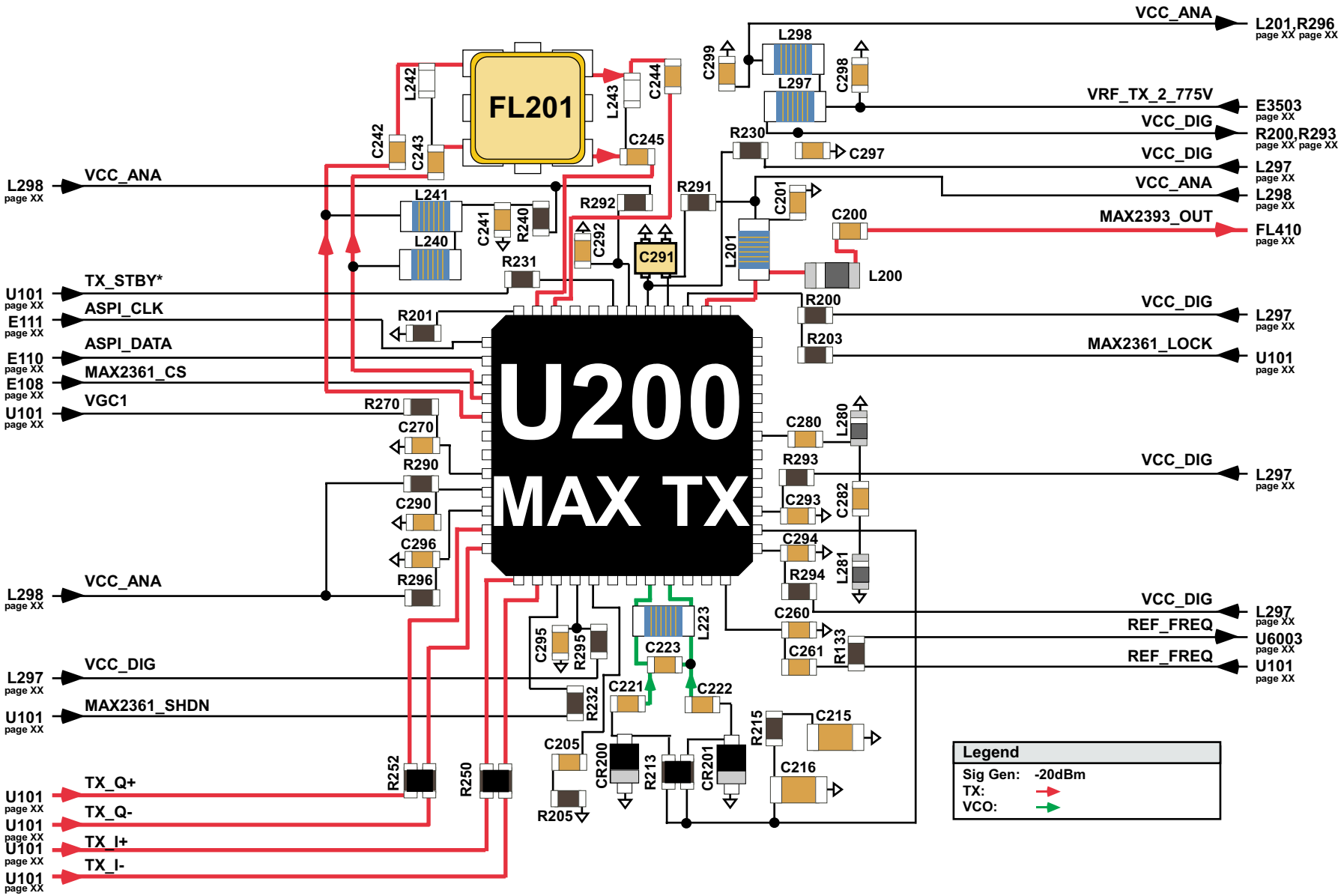
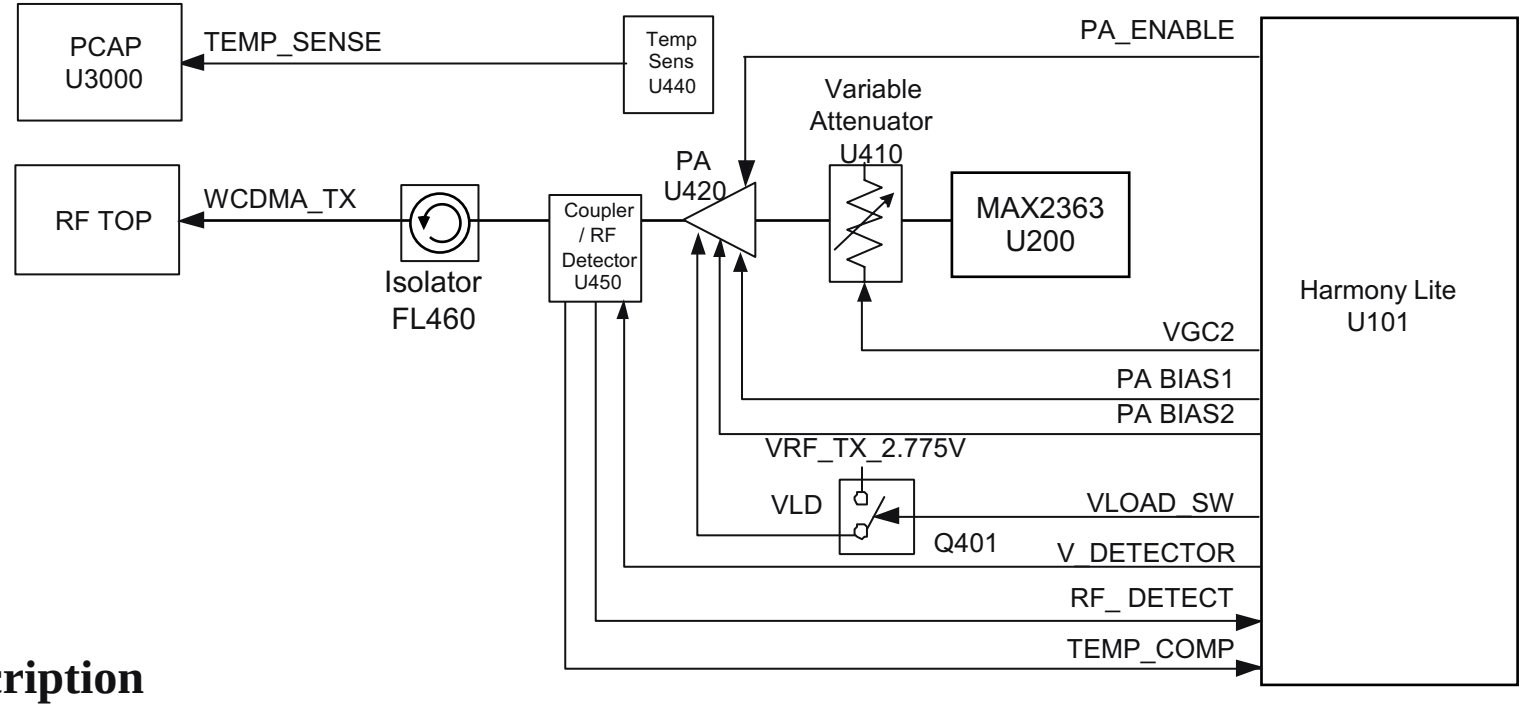
A920: WCDMA TX Modulator





A920: WCDMA PA



Description

The U410 provides necessary attenuation of the TX carrier before reaching the PA so that it doesn‘t exceed the maximum allowable input of 1dBm of the PA and to control the overall power output of the transceiver. U410 has a 16-18 dB of attenuation depending on the control voltage VGC2 applied at HYBOUT1 and HYBOUT2, which is controlled by Harmony Lite.

U420 is a three-stage power amplifier handling the band of WCDMA Tx frequencies between 1920 - 1980MHz. The nominal expected maximum gain is ~30dB. HARMONY_LITE controls the RF biasing of the amplifier at pins #4 (PA_BIAS1) and #5 (PA_BIAS2) with a control range of 0 - 2.5v. HARMONY_LITE also controls pin #12 (VLD) for PA load switching. Although not implemented, the theory of PA load switching in WCDMA is vitally important to conserve battery life and to avoid unnecessary radio interference with base stations. When VLD is at a low state (0v), the transmitter is in high power mode, consuming higher current but with overall better PA performance. When VLD is at a high state, the transmitter is in low power mode, consuming less current with overall poor PA performance. In theory, as the Tx power level increases or decreases beyond a certain power threshold, VLD is enabled or disabled. As Tx power decreases (as requested from a base station) down to ~14.5dBm, VLD will switch high. If Tx power is requested to increase beyond ~19dBm, VLD is switched low.

The power detector receives the amplified WCDMA RF signal at RF_IN (pin #6) from the PA. U450 is a combination directional coupler and temperature compensated power detector with a differential output. The power detector couples the TX power input and feedbacks an output RF_DETECT to HARMONY LITE. The TEMP_COMP also obtains the coupled power but removes the RF signal content, leaving a DC level. The DC level is feedback to HARMONY LITE. Expected nominal loss is <. 3dB.

The isolator (FL460) provides isolation between Front-End Module (FEM) and transmitter path. Nominal insertion loss is ~ 0. 55dB.

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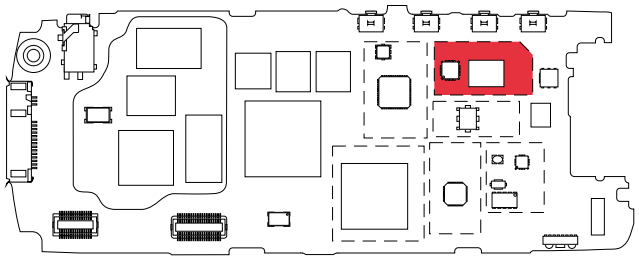
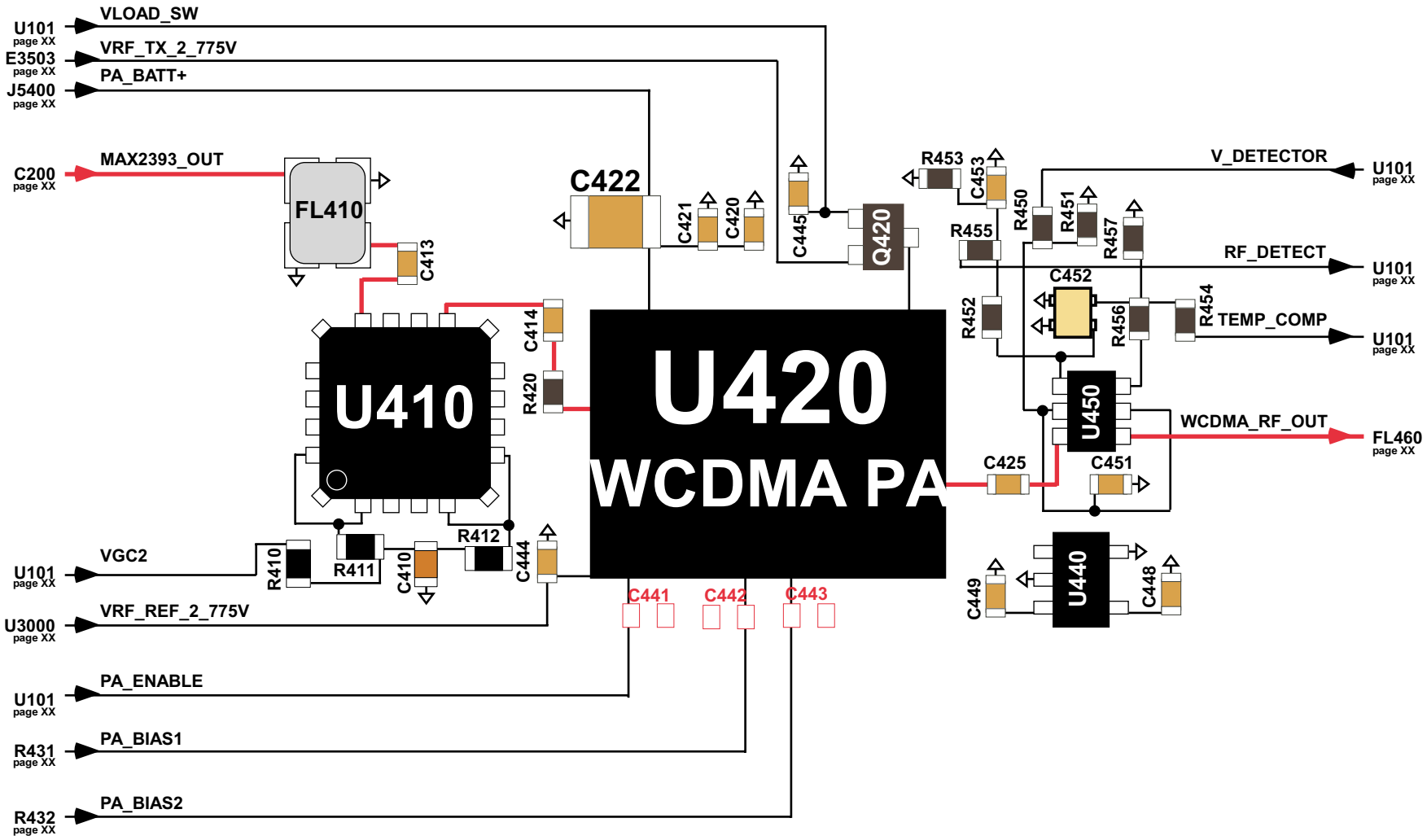
A920: WCDMA Transmitter





Legend	
Sig Gen:	-20dBm
TX:	→

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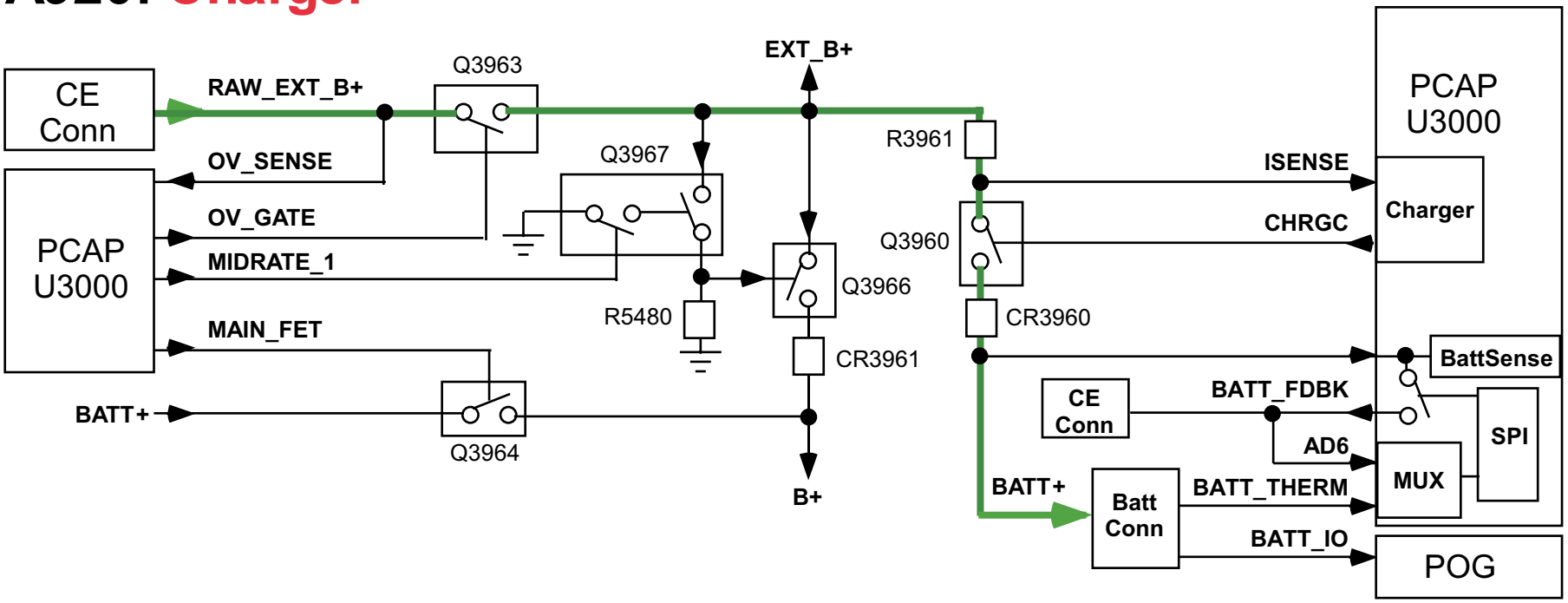
A920: Charger



Description

The majority of the charging circuit is integrated in PCAP. This includes a digital to analog converter, analog to digital converter, battery feedback switch, thermistor switch/pullup, and current control sense. External FETs (Q3966 and Q3954) are provided to enable/disable EXT_B+ and BATTERY supply paths to radio circuitry (B+). An external sense resistor (R3961) and a charging FET (Q3960) are provided to control charging current between EXT_B+ and BATTERY.

Due to pin count constraints on the CE bus, the Charger Identification input signal and Battery Feedback output signal share the same accessory connector pin. Software will first detect the Charger ID Voltage (AD6) before enabling the Battery Feedback Voltage via the Battery Feedback Switch in PCAP. The Battery Feedback switch must not be enabled at any time for an accessory that is not a valid Fast Charger.

Battery Feedback Voltage provides a reference voltage to the external power supply during charging. The battery feedback switch is needed to remove the battery feedback voltage from the feedback loop of the AC/DC Adapter or VPA when charging is complete or after a fault has occurred. This switch will be enabled before the charger DAC is programmed when charging is to begin. Battery feedback will turn on before the charger is enabled. The charger will be turned off before battery feedback is disabled.

A thermistor in the battery package is used to determine cell temperature of the battery pack before charging begins. The battery EPROM (BATT_IO) will contain limit parameters that determine the minimum and maximum temperatures at which charging can occur.

PCAP has an integrated over-voltage detection circuit that provides protection against damage caused by external charger voltages exceeding 7.0Vdc. If an over-voltage condition occurs, the EXT_B+ FET (Q3963) will be disabled. This will prevent high voltage (>7Vdc) from being applied to radio circuitry (B+).

Mid-rate charging is supported if a valid mid-rate charger and valid battery are detected. A mid-rate charger will source up to 400mA of current to the radio circuitry and charging circuitry during idle mode. The mid-rate charger will supply 5.9Vdc (up to 400mA) to the phone, regardless of the BATT_FDBK voltage. If the phone is in transmit mode, mid-rate current will be supplied to the battery and radio circuitry via the charging path only (EXT_B+ FET (Q3966) will be disabled via the MIDRATE_1 line). Dead battery TX operation or ‘No Battery’ operation is not supported with a mid-rate charger.

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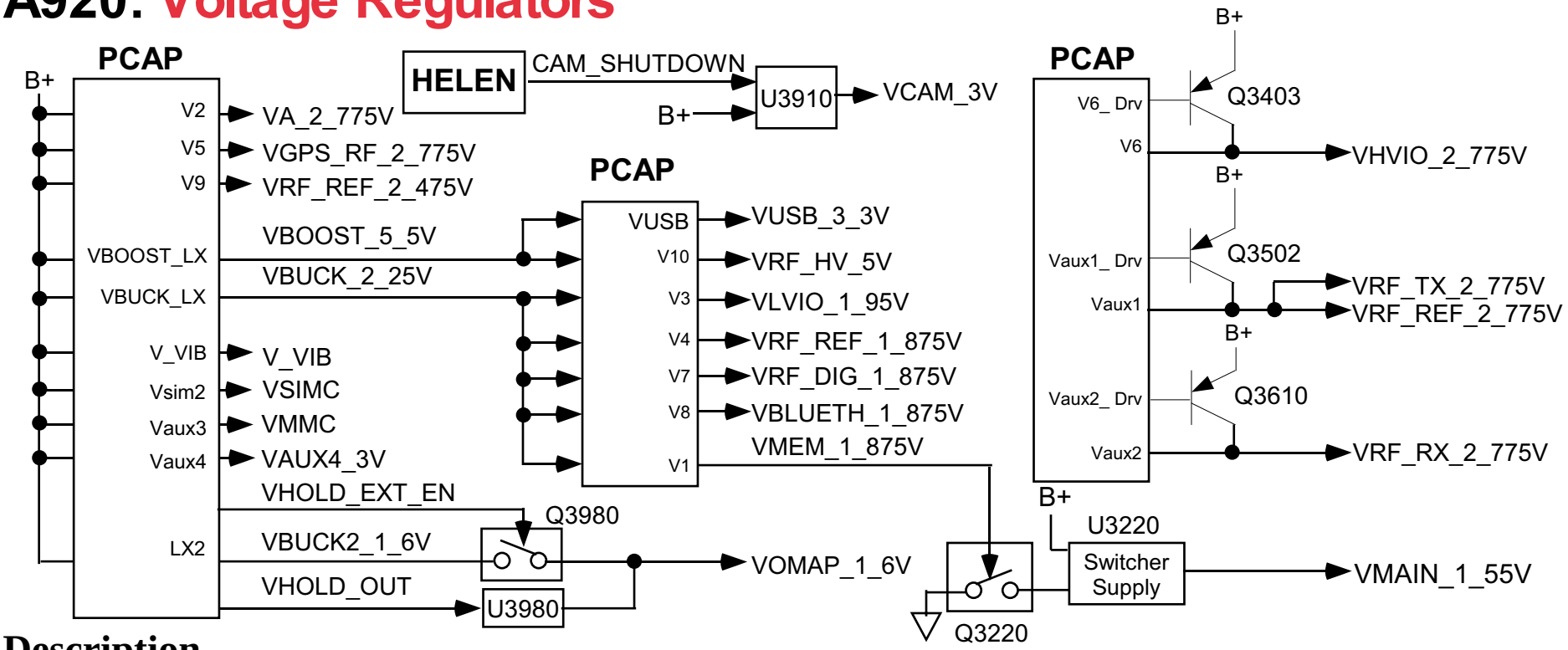
A920: Voltage Regulators



Description

Voltage regulation is provided by the PCAP IC (U3000). Multiple regulators are used to provide better isolation between sensitive load circuitry and noisy circuitry. The regulators and their load circuitry are described below:

· VBOOST_LX(VBOOST_5_5V) - VUSB abd V10 input voltage regulator
· VBUCK_LX(VBUCK_2_25V) - V1, V3, V4, V7, and V8 input voltage regulator
· LX2(VBUCK2_1_6V) - Helen core
· V_VIB - Vibrator
· Vsim2(VSIMC) - SIM card interface
· Vaux1(VRF_TX_2_775V) - RF TX circuits
· Vaux2(VRF_RX_2_775V) - RF RX circuits
· Vaux3(VMMC_2_8V) - SD/MMC interface
· Vaux4(VAUX4_3V) - Image processor, USB xcvrs (Application processor and Bluetooth USB)
· VUSB - PCAP USB xcvr
· V1(VMEM_1_875V) - Application Processor Flash I/O, Application Procesor DRAM I/O, Baseband Processor Flash Core
· V2(VA_2_775V) - Audio
· V3(VLVIO_1_95V) - Magic LV I/O, WCSP
· V4(VRF_REF_1_875V) - RF reference
· V5(VGPS_RF_2_775V) - GPS RF
· V6(VHVIO_2_775V) - HV I/O, Display(20), Imager(12), GPS Baseband(8), GPS Flash, Application Processor SDRAM core(200)
· V7(VRF_DIG_1_875V) - RF digital
· V8(VBLUETH_1_875V) - Bluetooth
· V9(VRF_REF_2_475V) - RF Reference
· V10(VRF_HV_5V) - RF HV

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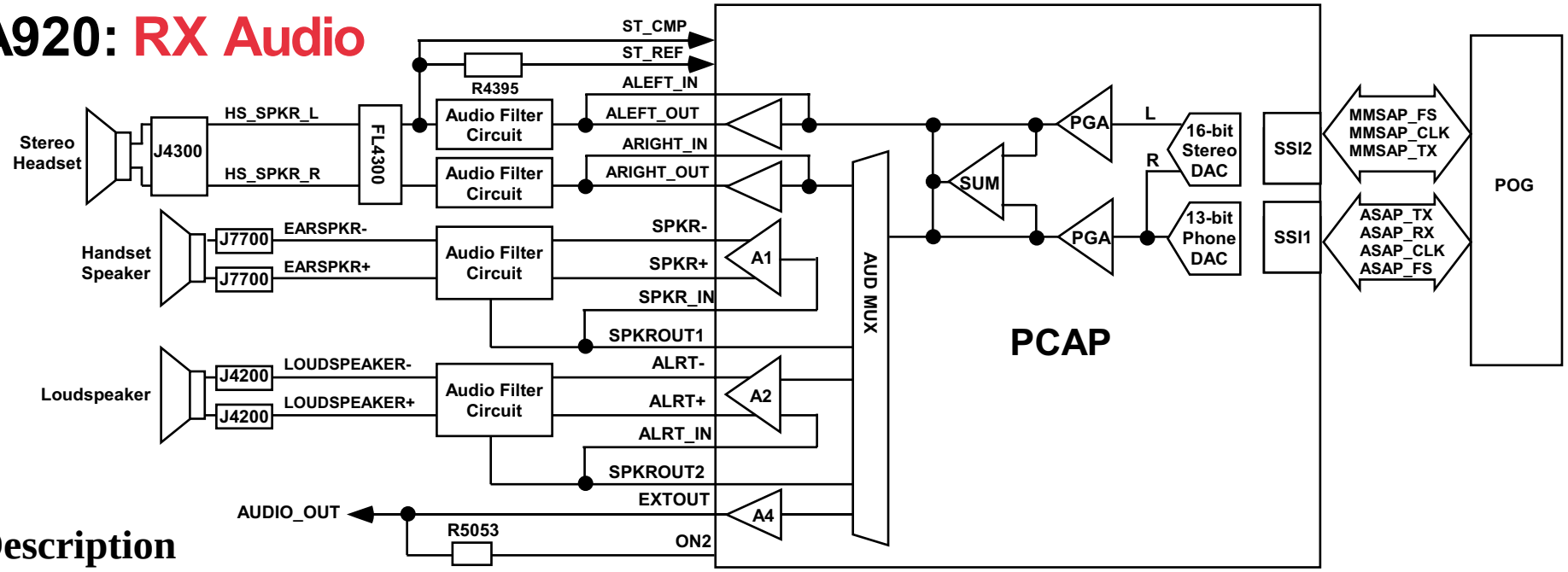
A920: RX Audio



Description

Receive audio data is transferred from the POG to the PCAP through the ASAP interface for mono audio and the VSAP interface for stereo audio data. The data is then converted into an analog form through a 16-bit Stereo DAC or 13-bit phone DAC. The output of PCAP's internal DAC drives the internal PGA. The output of the PGA can be routed to one of the four supported outputs via the internal multiplexer. All outputs use the same D/A converter so only one output can be active at one time. The user can adjust the gain of the audio outputs with the volume control buttons.

The Handset Speaker is driven by PCAP's internal SPKR differential amplifier. Following the speaker path from the PCAP pins SPKR- and SPKR+, they are routed through R4004 and R4005 respectively, and then connected to the transducer. Off the SPKR- path, SPKR_IN is routed through C4002 for the inverting input of the speaker amp A1. SPKR_OUT1 from PCAP is routed through C4000 and C4002 to SPKR- which is the DAC output of the CODEC. SPKR_IN and SPKR_OUT1 will output their respective bias voltages on these pins during standby times. This is to maintain the voltage across an external coupling capacitor to avoid audio "pops" when the amplifier is enabled.

The headset uses a standard 2.5mm stereo phone jack. The phone will detect the presence of a stereo headset using HS_SPKR_L of the headset jack, which is pulled high by R4395 and connected to the ST_COMP of PCAP (this is an interrupt of PCAP which gets sent to MCU over the SPI bus). This pin will be pulled to a logic low whenever the stereo headset plug is inserted into the jack. The headset may contain a momentary switch, which is normally closed and is in series with the microphone cartridge. When the momentary switch is pressed, the bias current being supplied to the microphone will be interrupted. The phone will detect this action and make an appropriate response to this action, which could be to answer a call, end a call, or dial the last number from scratchpad.

The Headset Speaker is driven by PCAP's internal Left and Right amplifier. Following the speaker path from the PCAP pins ARight_Out and ALeft_Out, they are routed through C4356, R4352 and C4306, R4302 respectively, and then connected to the headset jack. Off the ARight _Out path, AR_IN is tapped off through C4354 for the inverting input of the audio amp ARIGHT. Off the ALeft_Out path, AL_IN is tapped off through C4304 for the inverting input of the audio amp ALEFT.

The External Speaker is connected to pin 15 of J5000 (AUDIO_OUT), the accessory connector for the mobile phone. The audio path is routed through R4400 and C4400 and connected to EXTOUT of PCAP. The DC level of this Audio_Out signal is also used to externally command the phone to toggle it's ON/OFF state. The Audio_Out signal connects to PCAP's ON2 pin via R5053 to provide this capability. When a DC level of <0.4V is applied by an accessory for a minimum of 700 milliseconds on the Audio_Out line, the phone will toggle it's ON/ OFF state.

The Loadspeaker is driven by PCAP's ALRT amplifier (A2). The alert path from the PCAP pins ALRT- and ALRT+ are routed directly to the alert transducer. Off the ALRT- path, ALRT_IN is routed through R4201 for the inverting input of the alert amp A2. SPKROUT2 from PCAP is routed through C4200 and R4200 to ALRT- which is the DAC output of the CODEC.

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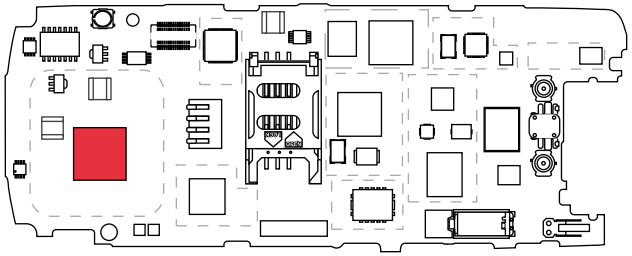
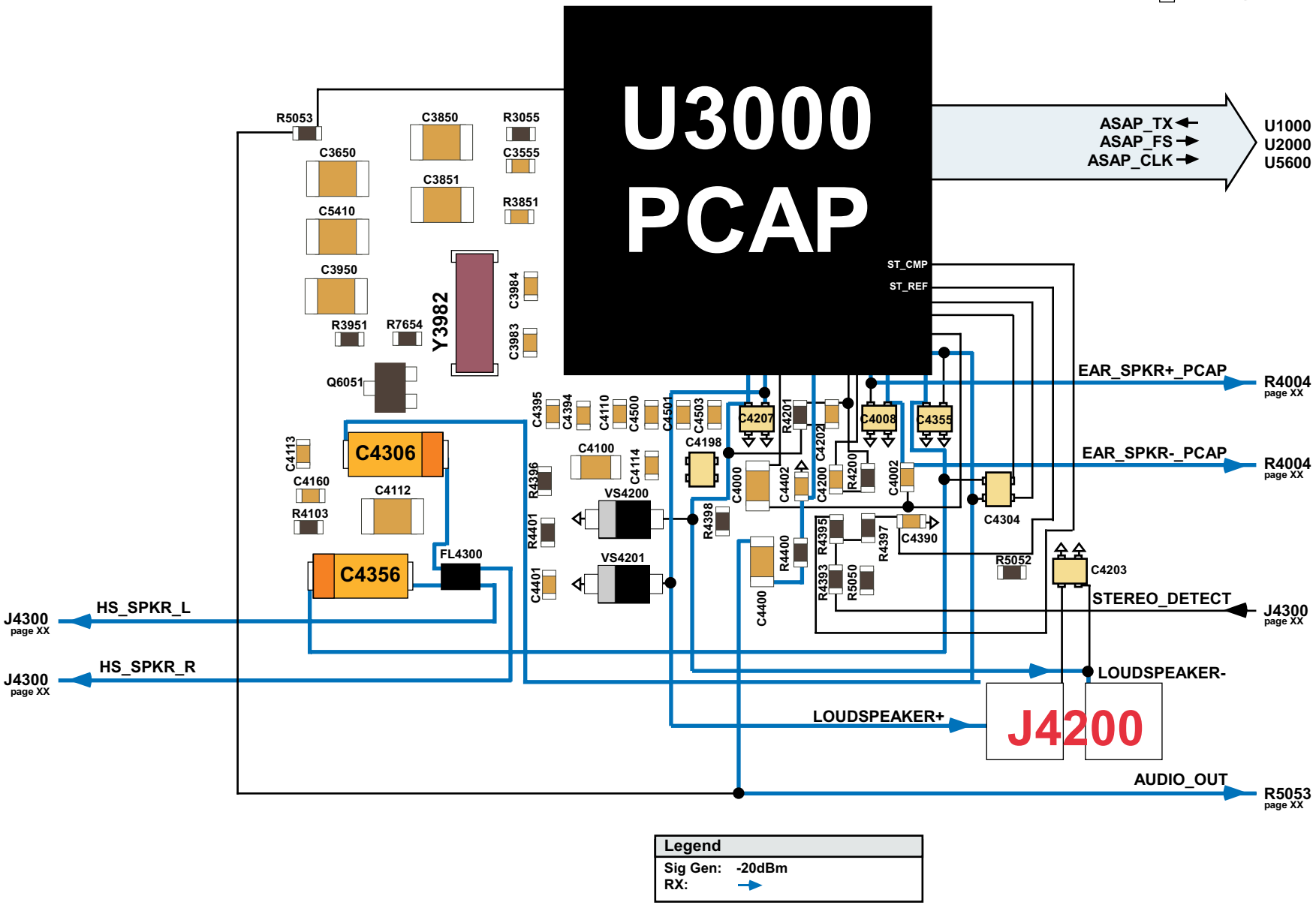
A920: RX Audio





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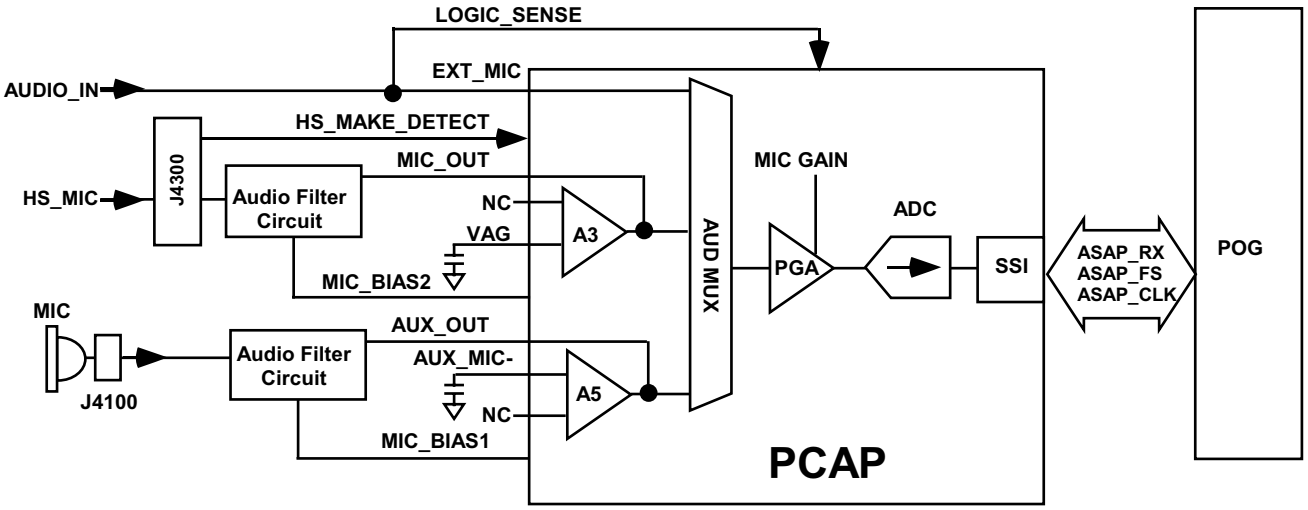
A830: TX Audio



Description

The Internal Microphone is a single ended part. Following the Internal microphone path, the microphone is biased by R4103 to provide a MIC_BIAS of 2.0V from pin MIC_BIAS1 of PCAP. C4198 is connected to MIC_BIAS1 and MB_CAP1 pin on PCAP to bypass the gain from the VAG to MIC_BIAS1 which keeps the noise balanced. From there, the signal is routed through C4100 to AUX_OUT pin on PCAP, bypassing the input to the A5 amplifier.

The headset microphone path (HS_MIC) is biased through R4396 and R4392, which is connected to pin MIC_BIAS2 on PCAP and bypassed with C4199 connected to pin MB_CAP2. From here the signal is routed through C4395 and R4388 to MIC_IN- pin on PCAP, which is the input to the A3 Amplifier. The Microphone path is tapped off after R4388 before the MIC_IN- input to R4389 connected to the MIC_OUT pin on PCAP, which is the output of the A3 Amplifier. The HS_MAKE_DET line monitors the presence of a headset by detecting the voltage at A1_INT of PCAP, which passes through R4398. A switching mechanism integrated in the headset jack will open or close the HS_MAKE_DET path to ground, depending on whether the headset is attached or not.

The External Microphone input (AUDIO_IN) is connected to the accessory connector for the mobile phone. The path is routed through L4400, C4401 and R4401 to the EXT_MIC pin on PCAP. This signal feeds directly to the input multiplexer without an intervening gain stage. In addition to audio signals, AUDIO_IN supports detection of accessory devices. The accessory attached to the CE bus shall have an output impedance that will load LOGIC_SENSE to a predetermined level. The POG will read the input level of LOGIC_SENSE and configure the audio accordingly.

The proper Microphone path is selected by the AUD MUX controller and path gain is programmable at the PGA. The A/D converter willl convert incoming analog signals into 13-bit, 2's compliment, linear PCM words. The digital audio signals are then transferred to the POG DSP through a four wire serial interface (ASAP).

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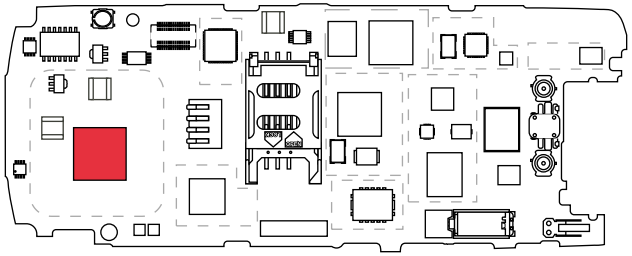
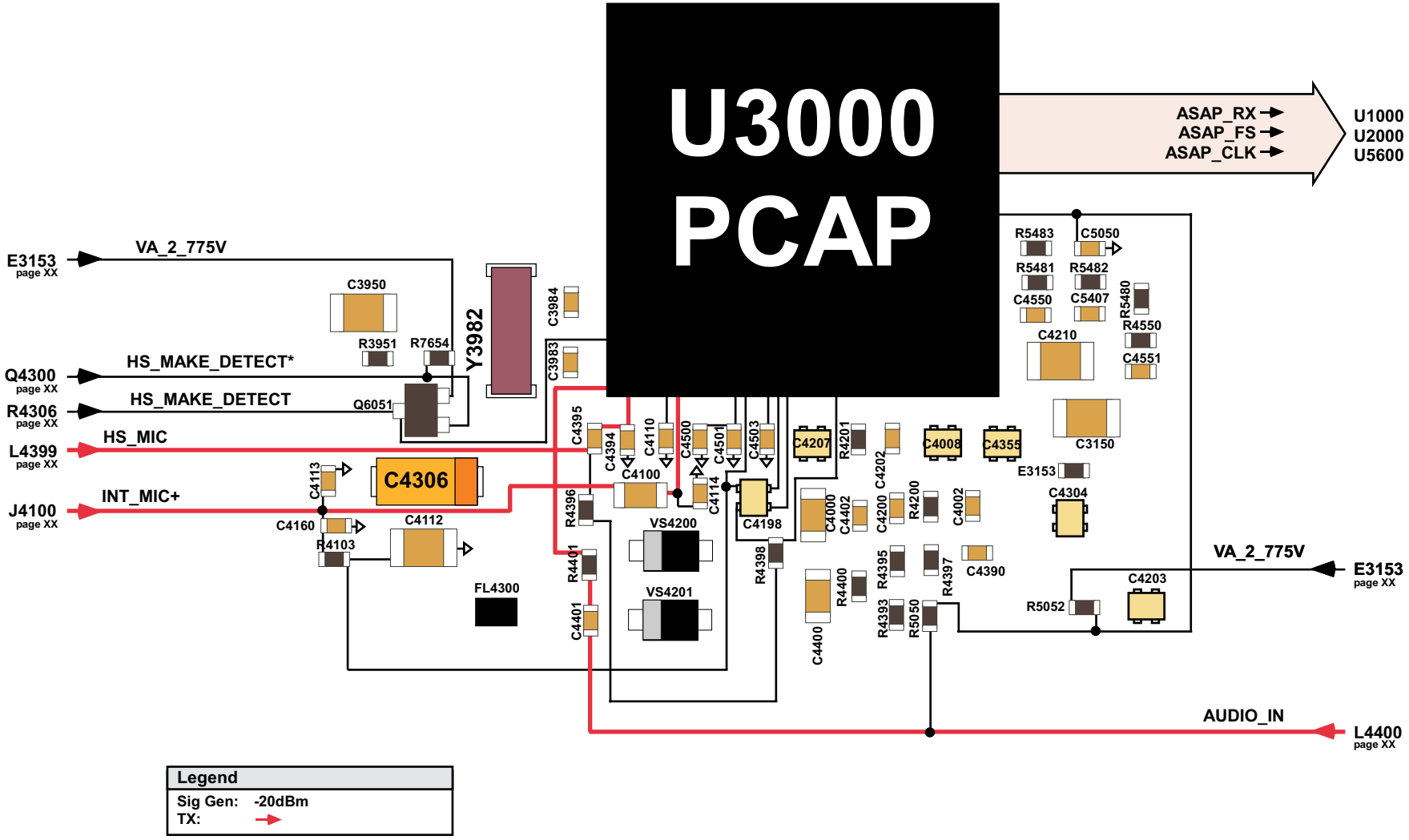
A920: Transmit Audio





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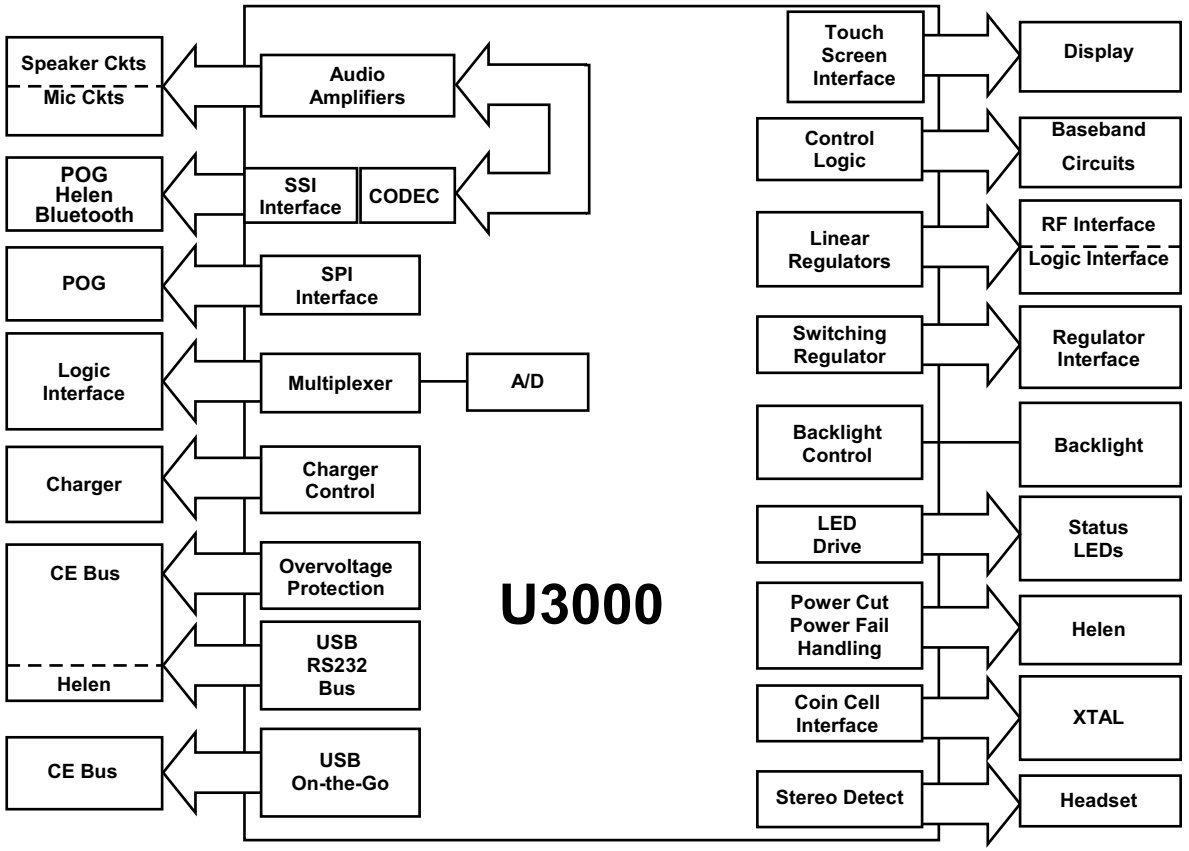
A920: PCAP



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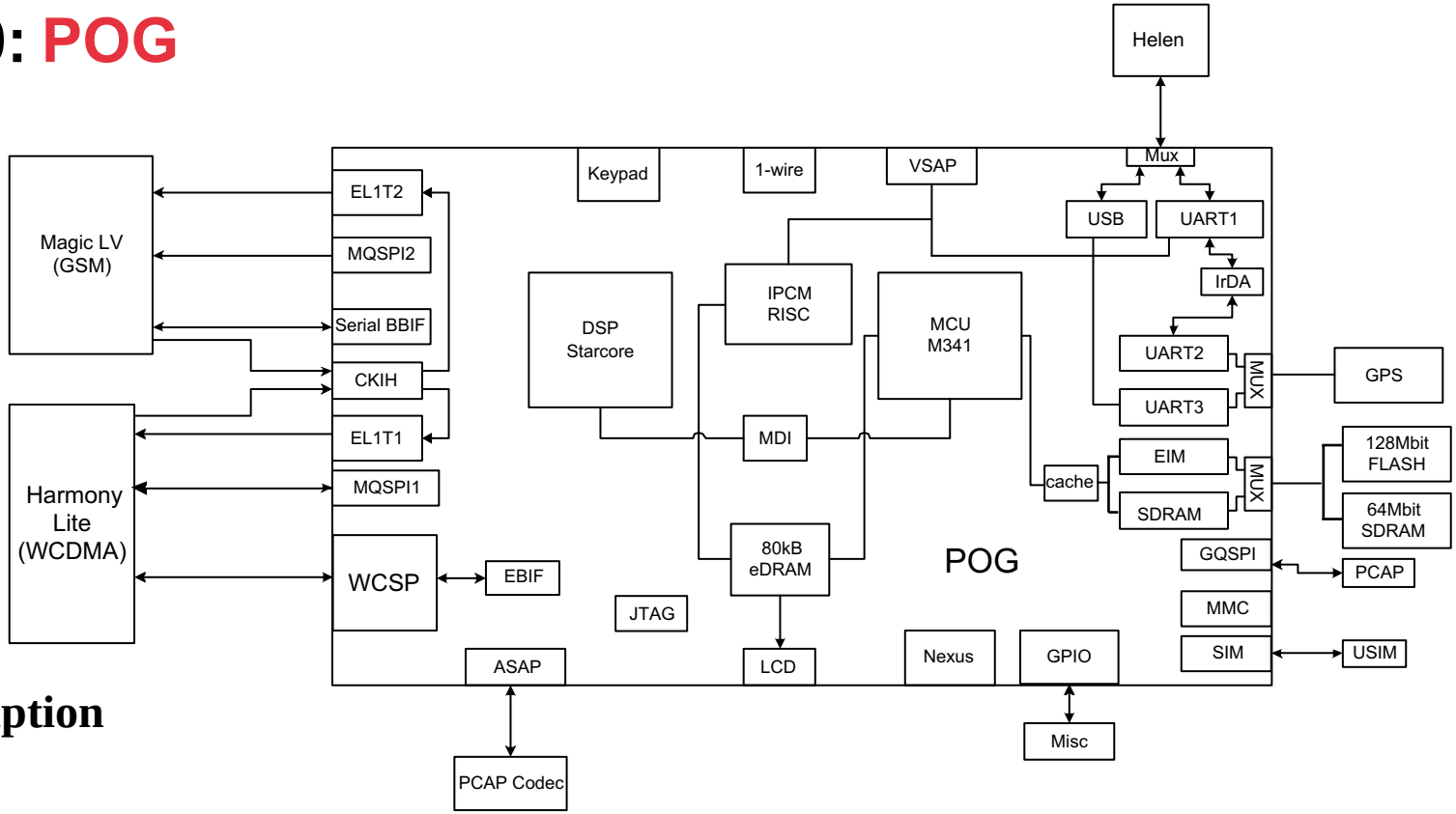
Description

The Platform Control Audio Power IC (PCAP), U3000, is a mixed signal IC that contains the following features:

- Audio input/output amplification and filtering
- Audio path selection
- Voltage regulation
- Battery charging control
- Real time clock
- Ringer/vibrator control
- RS-232/USB drivers
- Back-light control
- Status LED control
- Multiplexed DAC inputs for temperature and voltage monitoring
- Dual SPI control interface to allow access from two independent baseband processors
- Stereo DAC
- Overvoltage protection
- Touch Screen

The PCAP IC is controlled and configured by the Baseband Processor IC through a four-wire SPI interface. The Baseband Processor has read/write access to the PCAP IC. Audio data is transmitted/received via the Baseband Processor through a four-wire SSI interface.

A920: POG



Description

The POG(baseband processor) integrates a 32-bit RISC Communications Engine (MCU), a 32-bit DSP Core and an Interprocessor Communications Module (IPCM) along with associated peripherals and co-processors. The following provides a brief description of the cores and associated peripherals being used in this design.

·MCU – Micro Controller
·DSP for GSM Signal processing
·EIM(external interface module) interfaces to FLASH and DRAM
·USB/Serial Communications
·GPIO - For A/Ds
·IPCM which provides a multichannel DMA between the Mcore, DSP and peripherals.
·WCSP Interface
·GQSPI - PCAP Interface
·EBIF(External Bus Interface) DMA – WCDMA Data Transportation
·MQSPI1(Qued Serial Peripheral Interface) – WCDMA Control Signals
·EL1T1(Enhance Layer Timer) – WCDMA Event timer
·CKIH - WCDMA 15.36MHz clock
·GPS Interface
·USIM interface
·ASAP interface for PCAP and Bluetooth audio interface
·Serial BBIF(Baseband Interface) – GSM Data Transportation
·MQSPI2(Qued Serial Peripheral Interface) – GSM Control Signals
·EL1T2(Enhance Layer Timer) – GSM Event timer
·CKIH - GSM 13MHz clock

In addition to POG's internal memory system, the architecture provides 128Mbits (16M byte) of external flash memory via two Intel Danali 64M bit parts. The memory bus is 23 address bits and 32 data bits. The flash memory runs at 42-45MHz.

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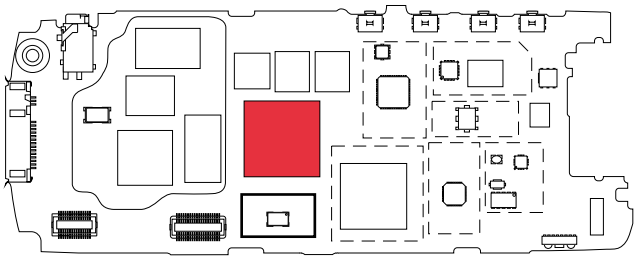
A920: POG



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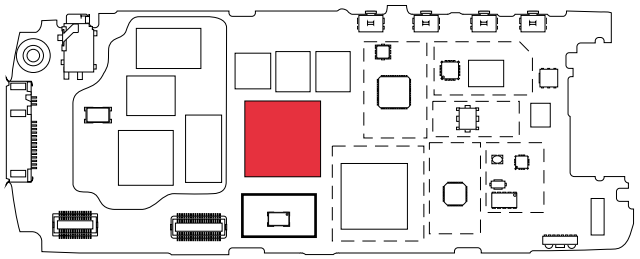
A920: POG



U1000
(POG)

U6000 page XX
- GSP_WAKEUP*
- GPS_ON_B
- GPS_BOOT_SEL
- GPS_TX
- GPS_RX
- GPS_RESET

U2071 page XX — STANDBY
FL500 page XX — NB_RX_ACQ
FL500 page XX — BFSR
FL500 page XX — BDR
FL500 page XX — BCLKR
FL500 page XX — DET_FLAG
U500 page XX — SYS_BB_CLK
U3000 page XX — BB_CLK_15_36M
U101 page XX — BATT_DETB
U3000 page XX — MIDRATE_1
Q3967 page XX — CLK_32_768K
U3000 page XX — PCAP_RESET*
U3000 page XX — MUX_CTL
U3000 page XX — PCAP_INT
U3000 page XX — POWER_FAIL
U3000 page XX

U101 page XX
- HARMONY_CS
- WB_SPI_MOSI
- WB_SPI_MISO
- WB_SPI_CLK

U3000 page XX
- BB_SPI_CLK
- BB_SPI_MISO
- BB_SPI_MOSI
- PCAP_CS

U1300,U1310 page XX page XX
- FLASH_CS*
- FLASH_OE*
- FLASH_CLK
- FLASH_URW_DQM0
- FLASH_ECB*
- FLASH_LBA*
- POR_RESET*

U2000 page XX
- USB_VMOUT
- USB_VPIN
- USB_TXEN*
- RTS_XRXD
- RXD_VMIN
- TXD_VPOUT

SWB+_EN — U5000 page XX
NB_EXC_EN* — Q906 page 4-3
BATT_IO — R5485 page XX
TX_RX_ERROR — U908 page 4-3
NB_TX_KEYM — U500 page XX
CLK_SEL — U500 page XX
NB_TX_EN — Q700 page XX
HL_TX_EN — U101 page XX
ADDR(24:0) — U1300,U1310 page XX page XX
DATA(31:0) — U1300,U1310 page XX page XX
USIM_EN — U3000 page XX

J5500 page XX
- USIM_CLK
- USIM_RST
- USIM_IO

U500 page XX
- NB_SPI_CLK
- MAGIC_CS
- NB_SPI_MOSI

U500 page XX
- SDTX
- DMCS_MAGIC
- TX_CLK
- BFSX

U3000 U2000 U5600
- ASAP_TX
- ASAP_RX
- ASAP_CLK
- ASAP_FS

U101 page XX
- BBIF_RX_FRAME
- BBIF_TX_FRAME
- BBIF_CLK
- BBIF_RX(5:0)
- BBIF_TX(7:0)

U101 page XX
- WB_RX_ON
- WB_RX_SLOT
- WB_RX_ACQ
- RF_RESET*
- WB_TX_PREKEY
- WB_TX_SLOT
- WB_TX_RAMP
- AOC_PWR_UP_DOWN

Legend

Sig Gen:	-20dBm
Ref Freq:	→
VCO:	→

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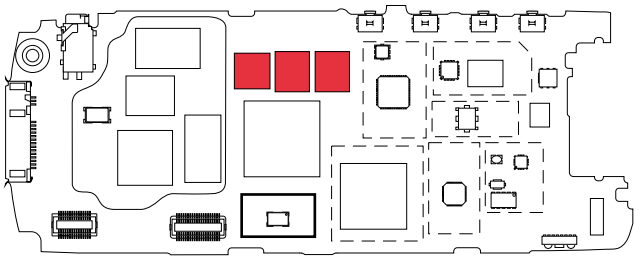
A920: POG Memory



U1300,U1310 page XX page XX
V_FLASH
U3000 page XX
VMEM_1_875V
R1304 page XX
V_FLASH_IO
U3000 page XX
VMEM_1_875V
U1400 page XX
V_SDRAM
R1402 page XX
V_SDRAM_IO
C1400
R1400
C1402
C1403
C1307
R1303
C1302
C1303
C1300
C1306
R1300
CR1300
C1305
C1301
C1308
V_FLASH_IO
R1304 page XX
V_FLASH
R1303 page XX
FLASH_12V
TP1300 page XX
V_FLASH_IO
R1304 page XX

U1400 SDRAM

U1300 Flash

U1310 Flash

U1400 page XX
V_SDRAM_IO
C1401
R1402
R1400 page XX
V_SDRAM
E3352 page XX
VLVIO_1_95V
C1309
V_FLASH_IO
R1304 page XX
R1304
VLVIO_1_95V
E3352 page XX
V_FLASH_IO
U1310,U1300 page XX page XX

U1000 page XX
DATA(31:0)
U1000 page XX
ADDR(24:0)
U1000 page XX
FLASH_ECB*
U1000 page XX
FLASH_CLK
U1000 page XX
FLASH_CS*
U1000 page XX
FLASH_OE*
U1000 page XX
FLASH_URW*_DQM0
U1000 page XX
FLASH_LBA
U1000 page XX
POG_RESET*

Legend	
Sig Gen:	-20dBm
Ref Freq:	→
VCO:	→

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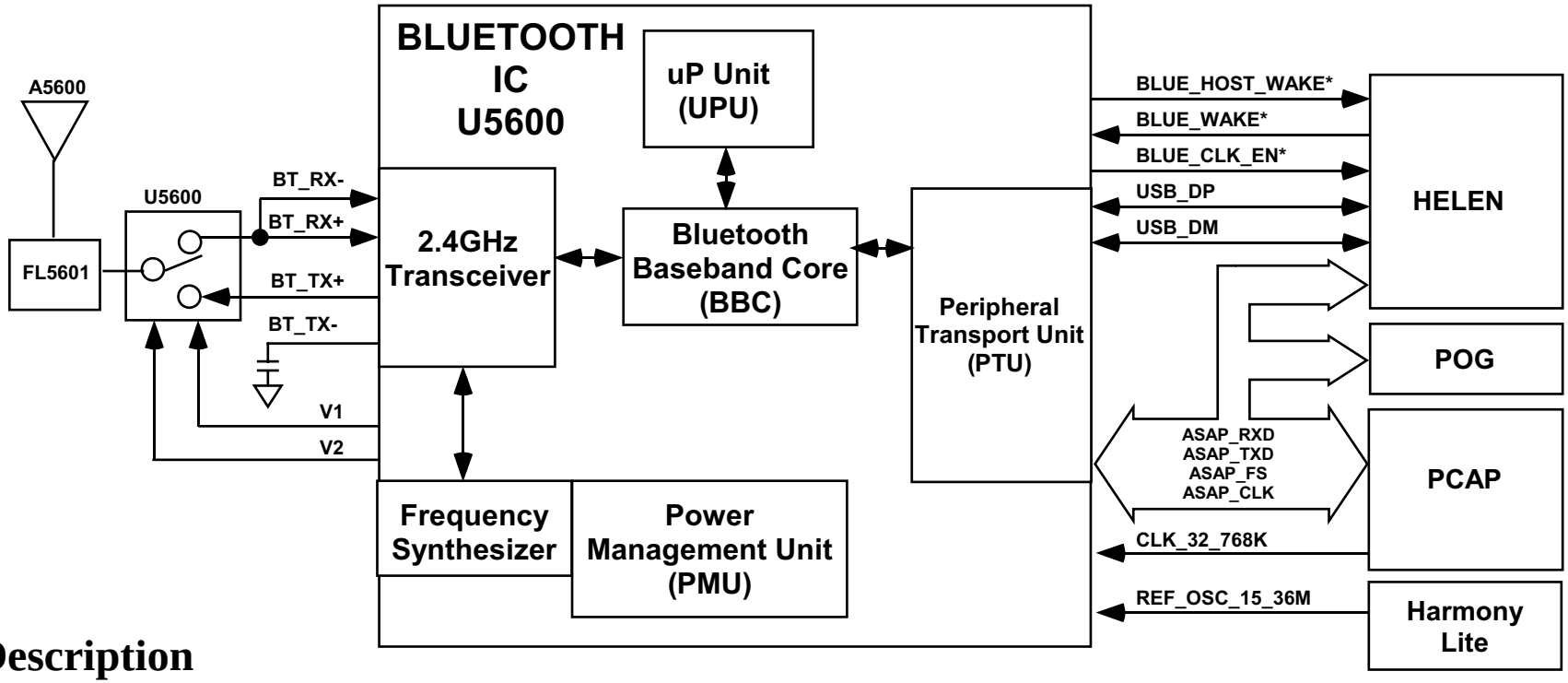
A920: Bluetooth IC



Description

The BCM2033 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth RF Specification v1.1 and meets or exceeds the requirements to provide the highest communication link quality of service.

The receiver has a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The BCM2033 also features a fully integrated transmitter. Baseband data is GFSK modulated and upconverted to the 2.4 GHz ISM band via an internal mixer. The output Power Amplifier (PA) provides a nominal power output of 0 dBm and has a power control to provide 24 dB of gain control in 8 dB step sizes. Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels.

The uPU runs software from the Link Control (LC) layer, up to the Host Controller Interface (HCI). The microprocessor is an enhanced performance 8051 microcontroller.

The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets.

The Peripheral Transport Unit (PTU) handles the Device Interface. The PTU supports three types of devices: USB, UART, and PCM.

The PMU provides power management features that can be invoked by either software through power management registers, or “packet handling” in the baseband core.

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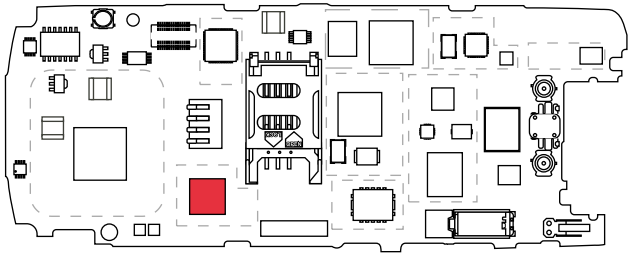
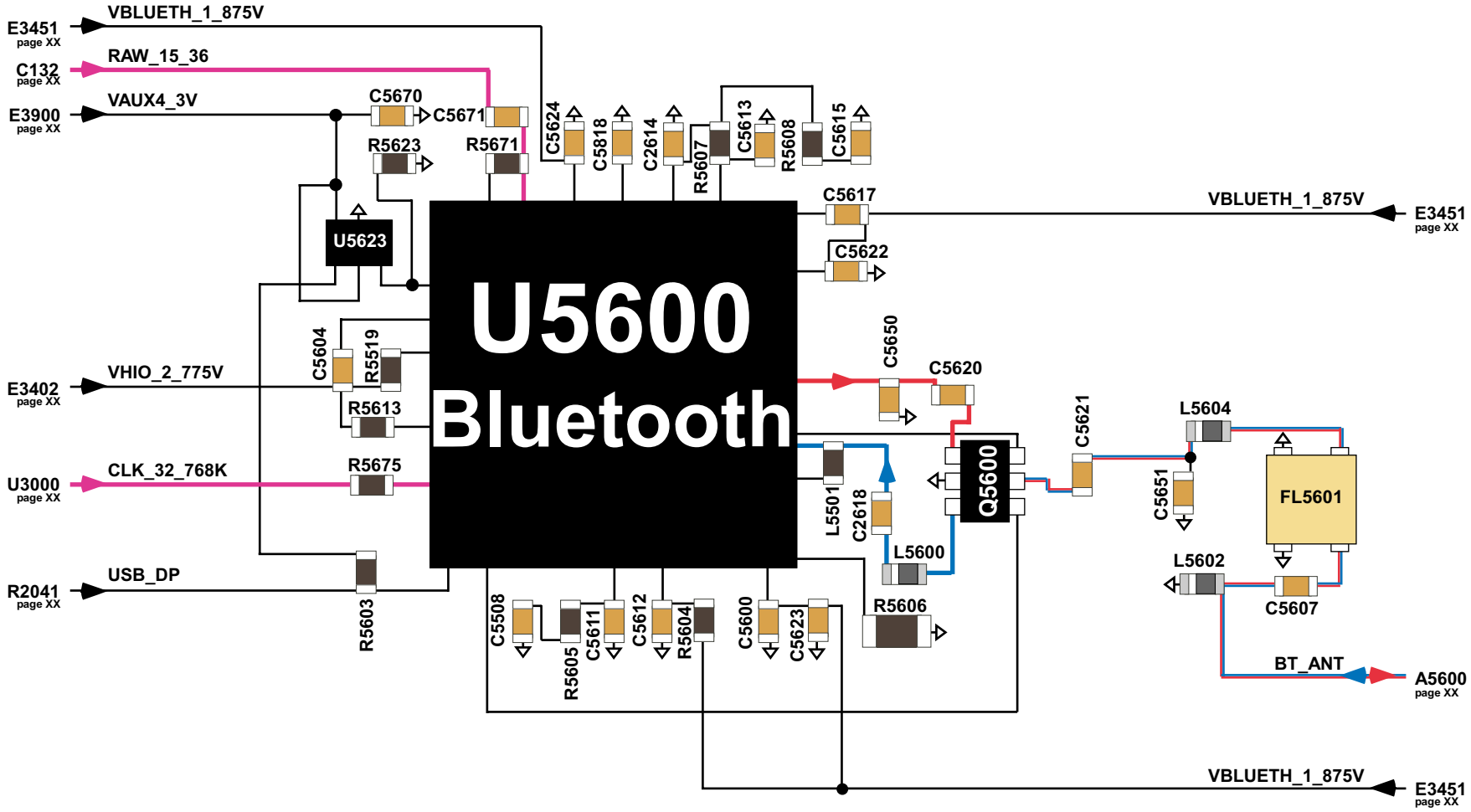
A920: Bluetooth





Legend	
Sig Gen:	-20dBm
TX:	
RX:	
Ref Freq:	

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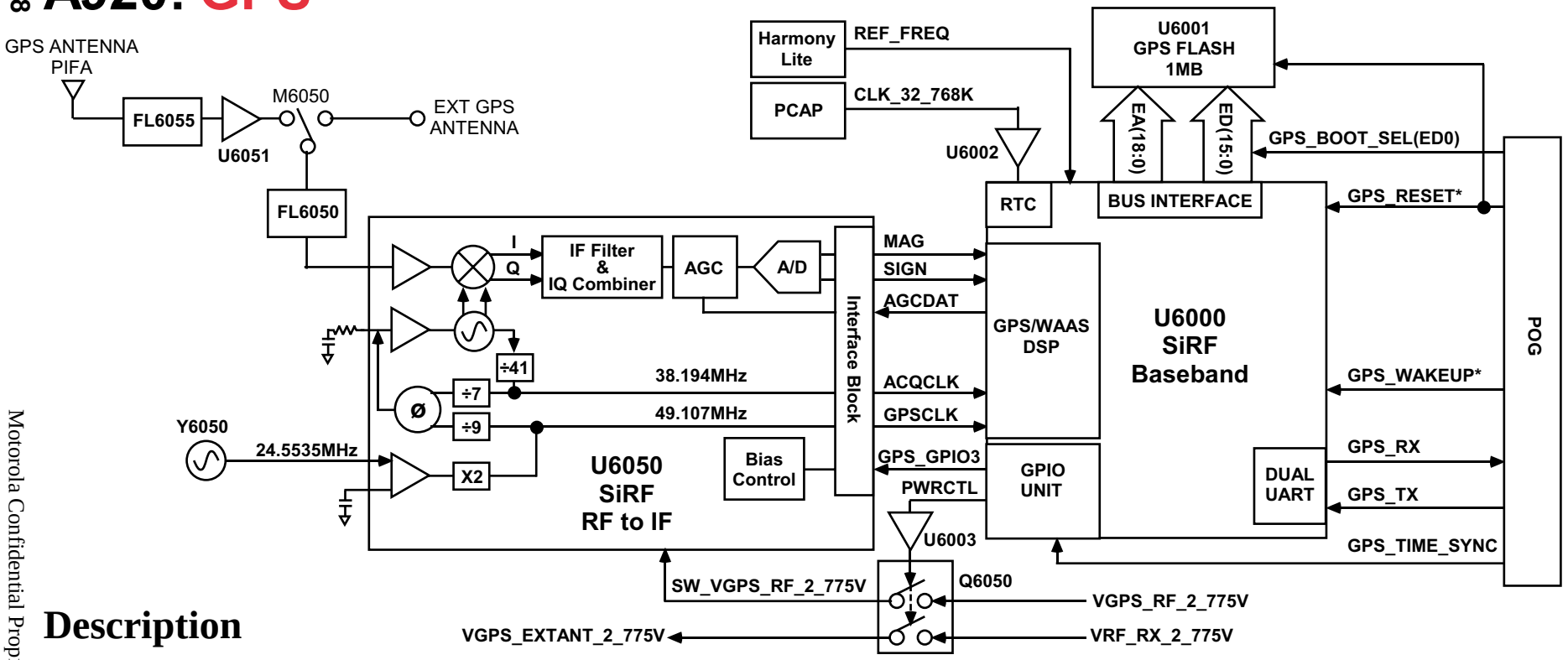
A920: GPS



Description

The 1575.42 MHz satellite signal can be received through the GPS antenna PIFA_Planar Inverted F Antenna) or exernal GPS antenna. GPS signal received through the PIFA will pass through FL6055 and LNA U6051. The signal is then passed to the LNA input of U6050 through FL6050.

The input signal at the LNA of U6050 is a Direct Sequence Spread Spectrum (DSSS) signal at 1575.42MHz with a 1.023 Mbps Bi-Phase Shift Keying (BPSK) modulated spreading code. The DSSS signal is then injected into an image reject mixer. The Mixer and on-chip 1565.97 MHz VCO will produce an IF center frequency of 9.45MHz. An IF filter is required between the Mixer and AGC Amplifier to provide an anti-aliasing function before A/D conversion. The IF filter block also contains an I-Q phase shift combiner. This circuit properly phase shifts and sums the I and Q outputs from the image reject mixer to a single channel. The AGC amplifier provides the additional gain needed to optimally load the signal range of the 2-bit A/D Converter. The 2-bit A/D onverter will then provide signal and magnitude output bits to the Interface Block. The outputs of the Interface Block provide clocks and the 2-bit sample data to the CGSP2e/LP(U6000). These signals use single-ended PECL(Positive Emitter-Coupled Logic) signaling to simplify the complexity of this interface. The interface block inputs are the single-wire AGC interface, (AGCDAT) and the Power Control pin (PWRCTL).

The GPS DSP within U6000 correlates the incoming MAG and SIGN data. Wide parallel search architecture enables simultaneous search of 1,920 time/frequency bins which enables a powerful combination of very fast reacquisition along with the capability to find and track very weak signals. The UART residing in U6000 is used to interface data information between the GSP2e/LP(U6000) and POG. An integrated GPIO unit provides support for a variety of peripherals.

RTC is an ultra-low power implementation of a high precision 32-kHz driven clock derived from the PCAP. It is separately powered by the VDDRTC to allow maximum battery life by maintaining time for the next power on. REF_FREQ is used as an external clock source for U6000.

GPS_WAKEUP* is an active low signal from POG to wake up SiRFLoc client from the deep sleep mode. GPS_RESET* is an active low hard reset signal for the SiRF BB IC and Flash. GPS_BOOT_SEL is used by POG to set boot configuration upon reset. GPS_TIME_SYNC is an active high signal to provide time stamping of the precise time aiding that is sent over from POG over the UART.

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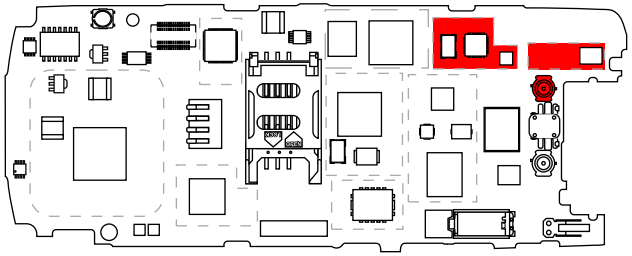
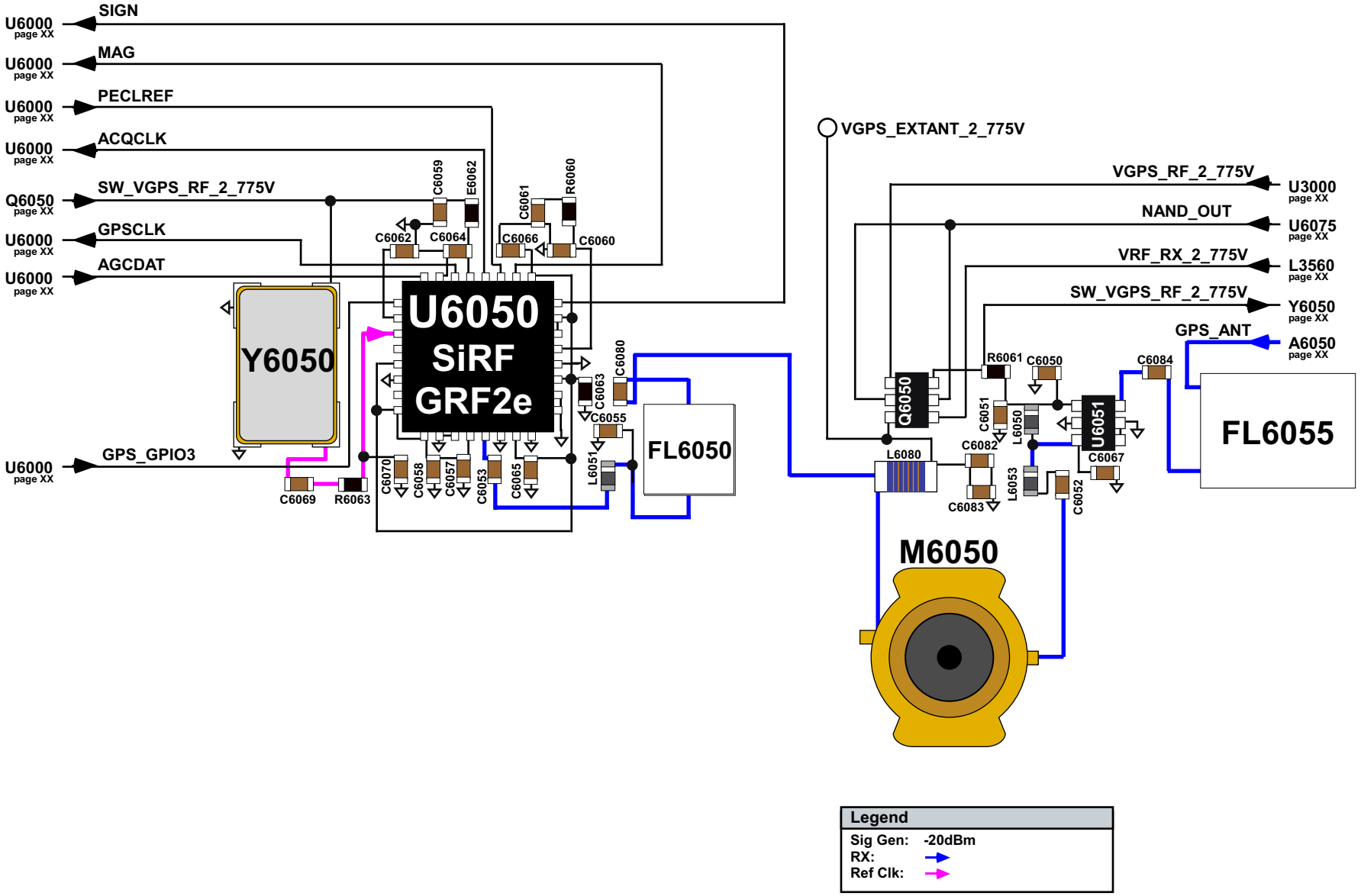
A920: GPS RF Circuit





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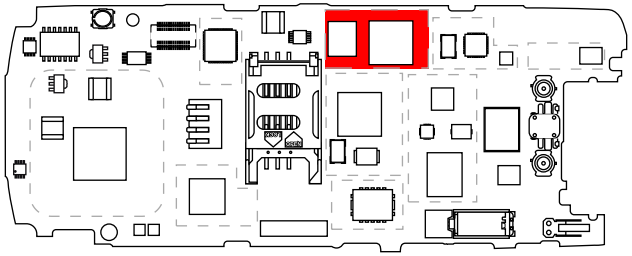
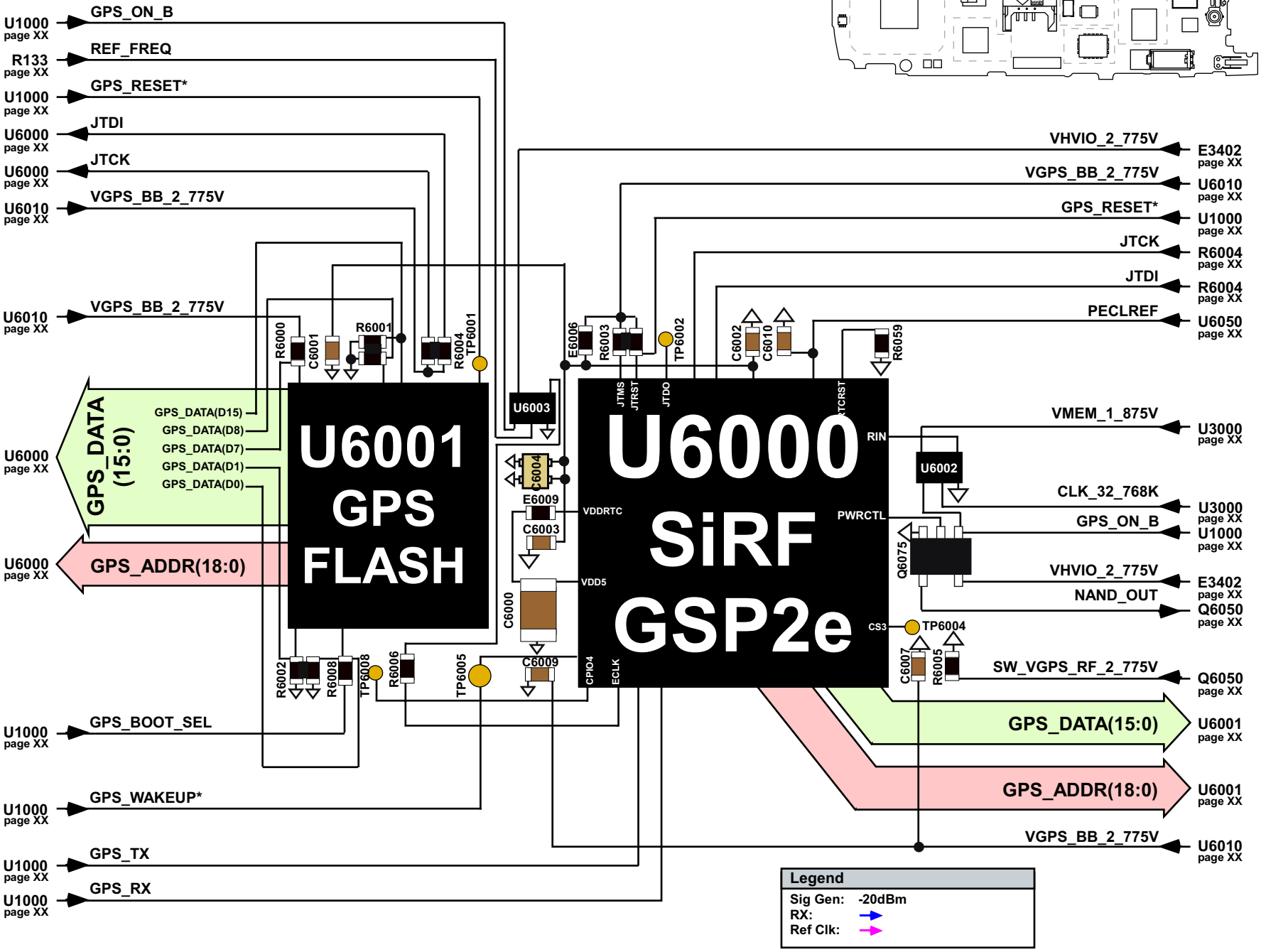
A920: GPS Baseband Circuit





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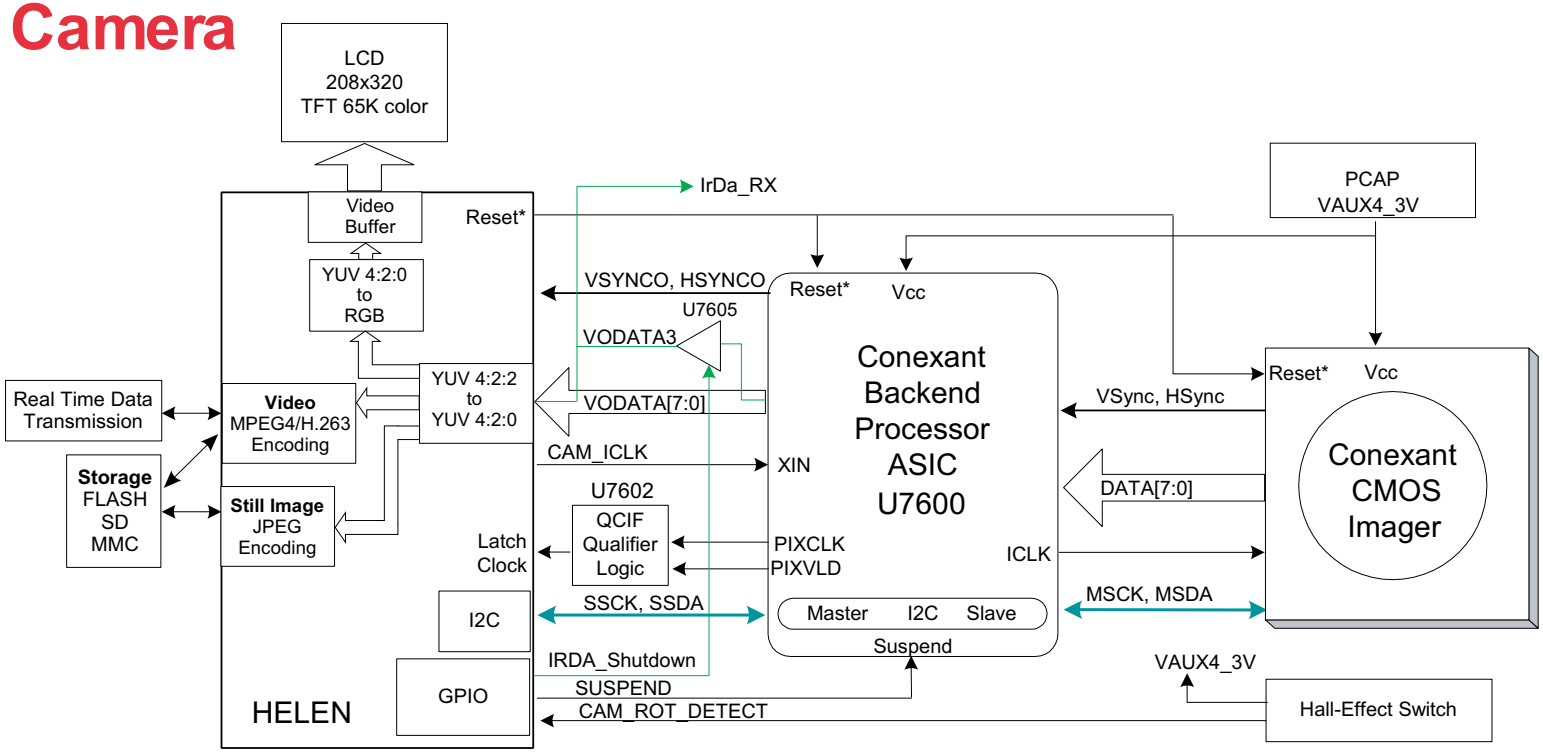
A920: Camera



Description

The Conexant imager allows15 fps(frames per second) image readouts at VGA resolution. The Conexant imager will output raw Bayer RGB 8-bit/pixel data to the Conexant backend processor (U7600).

The Conexant backend processor will receive the Bayer RGB data from the imager and process the image data into 8-bit YUV uncompressed or compressed data that is send through the VODATA bus to the Helen application processor. U7600 can process the YUV data in VGA(640x480), QVGA(320x240), CIF(352x288), and QCIF(176x144) output resolutions. Control functions for U7600 are done through a 2-wire serial interface(SSCLK and SSDA).

The QCIF qualifier logic devices(U7602 and U7603) are used for viewfinder and video capture functions. VSYNC and HSYNC signals provide vertical and horizontal synchronization of the image signals. VSYNC indicates a start and end of a valid video frame while HSYNC indicated the start and end of a valid video line.

VODATA sends 8-bit processed image data in YUV 4:2:2 format to the Helen processor. VODATA3 is shared by the camera and IrDA devices. Due to the hardware restrictions, Camera and IrDA wouldn‘t work simultaneously. For this reason, IRDA_SHUTDOWN is used to enable VODATA3 during camera operation.

CAM_ROT_DETECT is used to indicate the rotated position of the imager. A magnet integrated in the Conexant imager will activate the Hall effect switch and cause a state change for CAM_ROT_DETECT. The Helen will respond with a horizontal inversion of the image.

The image that Helen receives goes through a DSP pre-processing stage where the YUV 4:2:2 is converted to YUV 4:2:0. To display the image on the unit’s display, the YUV 4:2:0 signal passes through a DSP post-processing stage and converts it to RGB. The RGB signal is then passed through a video buffer and to the display. For still image storage cases, the YUV 4:2:0 image passes through JPEG encoding and then transferred to a user selectable storage device(Flash, SD, MMC). For video cases, the YUV 4:2:0 image is passed through MPEG4 or H.263 encoding. The video is then transferred to a user selectable storage device or sent as real time data transmission.

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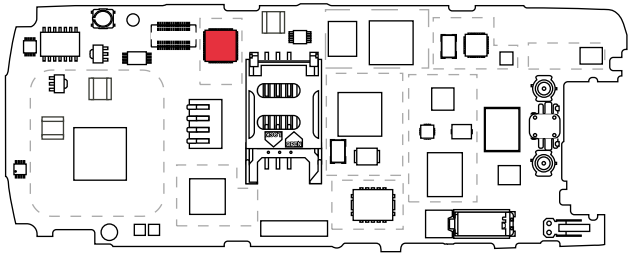
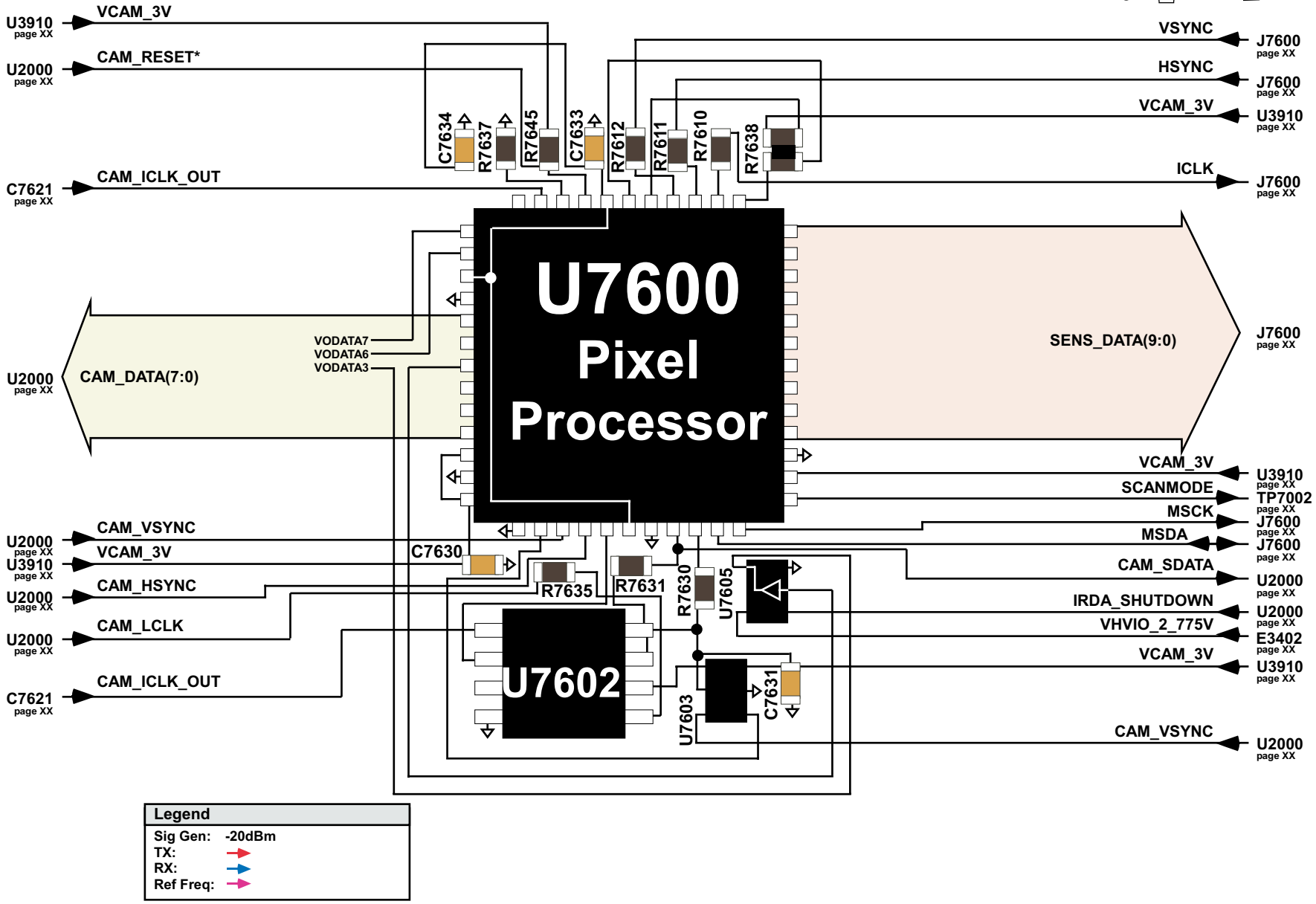
A920: Video Circuit





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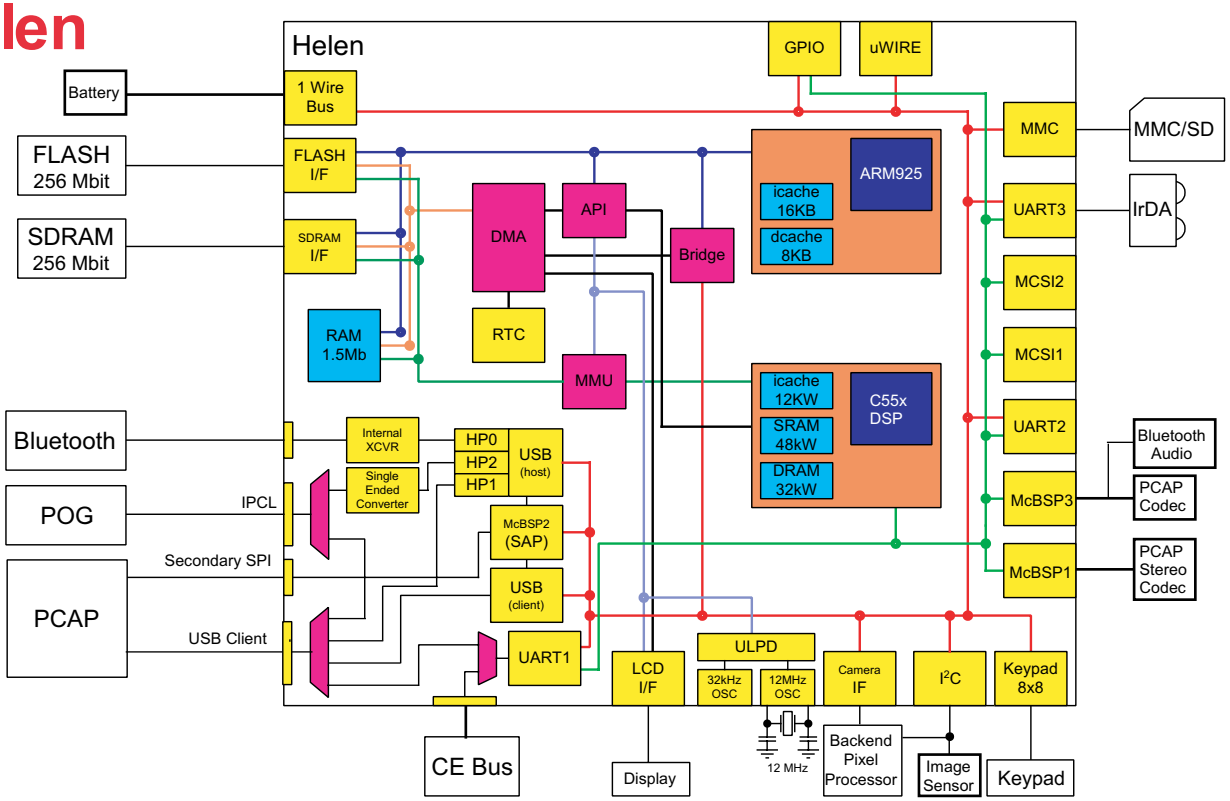
A920: Helen



Description

The Helen(adjunct processor) is a dual core processor architecture which incorporates a high-performane TI925T MPU core and a TI TMS320C55x DSP core. The following provides a brief description of the cores and associated peripherals being used in this design.

·Flash I/F, SDRAM I/F - Interfaces to FLASH and SDRAM
·Keypad Interface
·LCD I/F - Display Interface
·UART3 - IrDA interface
·MMC interface
·GPIO - For A/Ds
·Secondary SPI - PCAP interface
·Bluetooth Interface
·Camera IF - Backend Pixel Processor interface
·I2C - Inter-Integrated Circuit Master and Slave interface
·IPCL - Inter-Processor Communications Link for Helen to POG interface
·ULPD - Ultralow-Power Device
·1 wire Communication for Battery EPROM
·USB(client) - Helen USB is used as a client, signals are routed through PCAP's USB transceiver
·UART1 - RS232 interface to CE bus
·McBSP1 - Multichannel Buffered Serial Port (VSAP) for the PCAP stereo audio interface
·McBSP2 - Multichannel Buffered Serial Port (ASAP) for the PCAP and Bluetooth audio interface

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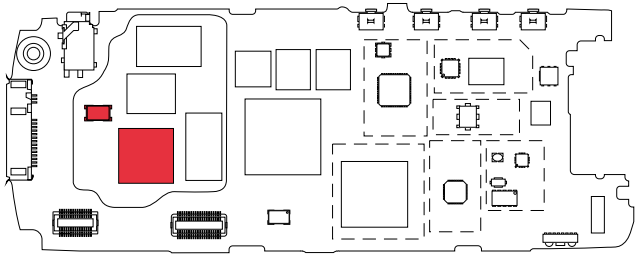
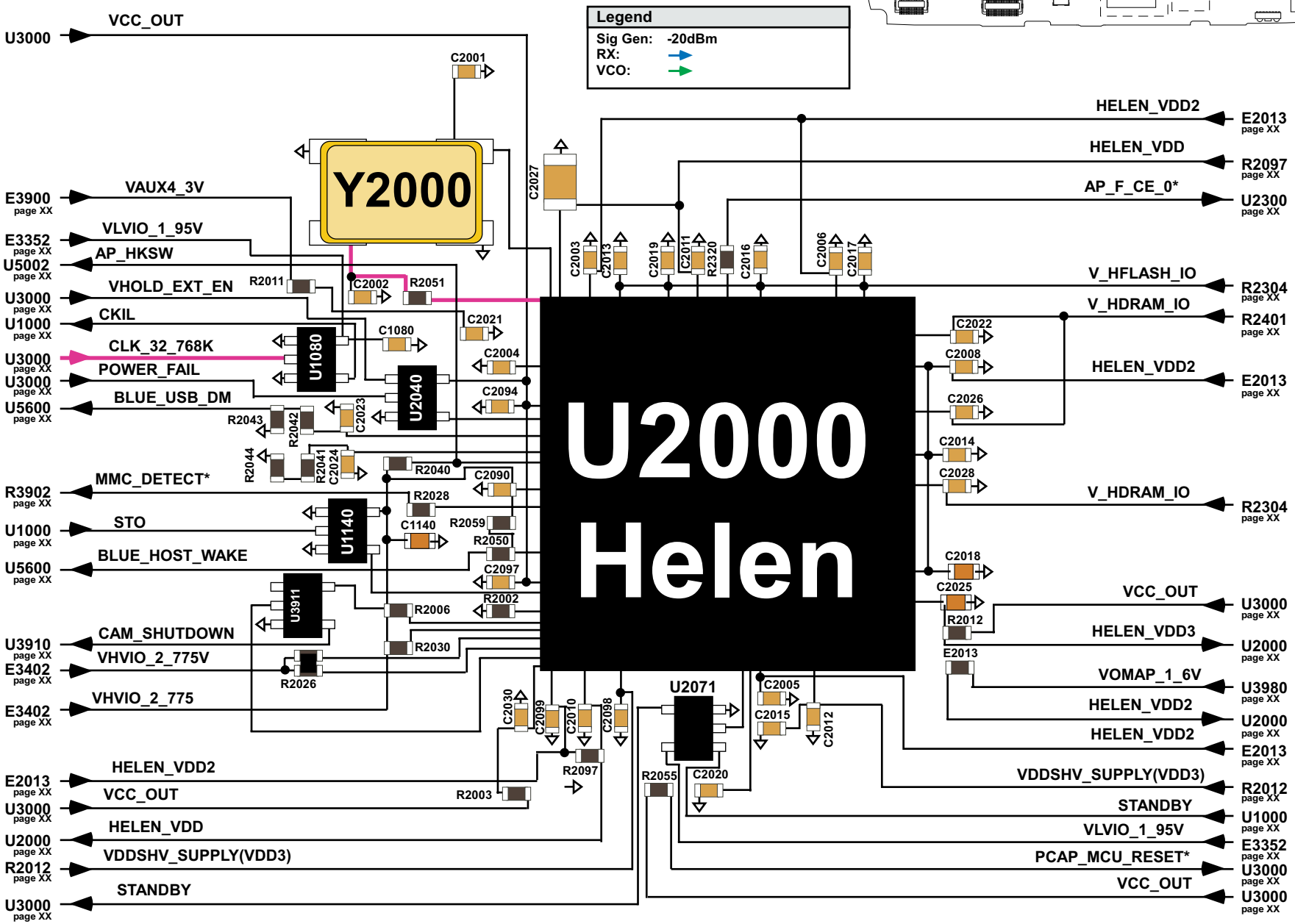
A920: Helen





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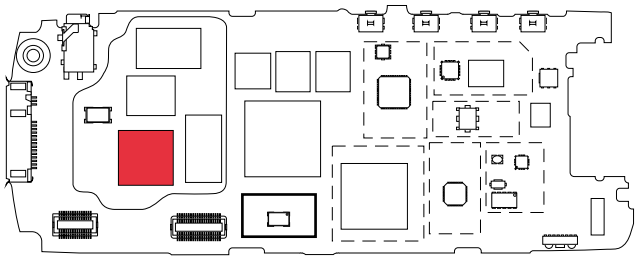
A920: Helen



U2000
(Helen)

U3000 page XX: RXD_VMIN, TXD_VPOUT, RTS_XRXD, USB_TXEN*, SE0_IN, USB_VPIN

U3000 page XX: AP_SD_CKE_HL
U3000 page XX: RESET_OUT*
R3997 page XX: WDI
U5003 page XX: OPT2
U5003 page XX: OPT1
U5003 page XX: DSEL0
U5004 page XX: DSEL1
U5003 page XX: DSEL2
U5005 page XX: HELEN_DCD
U5001 page XX: BLUE_USB_DP
U5600 page XX: AP_RTS
CR5005 page XX: AP_CTS
U5002 page XX: AP_TX
U5005 page XX: AP_RX
U5004 page XX: BP_READY
U1000 page XX: AP_DEEP_SLEEP
U1000 page XX

U3000 page XX: MMSAP_FS, MMSAP_CLK, MMSAP_TX

J5200 page XX: LCD_PIXEL(15:0), LCD_PCLK, LCD_HSYNC, LCD_VSYNC, LCD_OE, LCD_FRONTLIGHT, LCD_SHUTDOWN*

U1000 page XX: USB_VMOUT, USB_VPIN, USB_TXEN*, RTS_XRXD, RXD_VMIN, TXD_VPOUT

DITHER_CLK → U7640 page XX
CAM_ROT_DETECT → R7615 page XX
CAM_ICLK → R7620 page XX
CAM_LCLK → R7635 page XX

AP_SDADD(12:0) → U2400 page XX
AP_SD_DATA(15:0) → U2400 page XX
AP_F_ADD(23:0) → U2300,U2380 page XX page XX
AP_FDATA(15:0) → U2300,U2380 page XX page XX

CODEC_CLK_EN* → U5670 page XX

IRDA_TX, IRDA_RX, IRDA_SHUTDOWN → U6500 page XX

KBC(6), KBR(4:0), KBC(5:0) → Keyboard page XX

MMC_CMD, MMC_CLK, MMC_DAT, MMC_WP → J3900 page XX

ASAP_TX, ASAP_RX, ASAP_CLK, ASAP_FS → U3000 page XX, U1000 page XX, U5600 page XX

AP_SPI_MOSI, AP_SPI_MISO, AP_SPI_CLK, AP_SPI_CS, AP_PCAP_INT → U3000 page XX

CAM_DATA(7:0), CAM_VSYNC, CAM_HSYNC, CAM_RESET*, CAM_SCLK, CAM_SDATA → U7600 page XX

Legend	
Sig Gen:	-20dBm
Ref Freq:	→
VCO:	→

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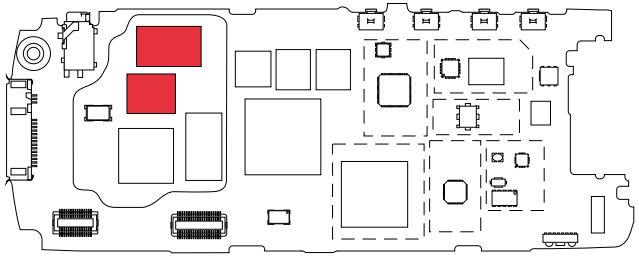
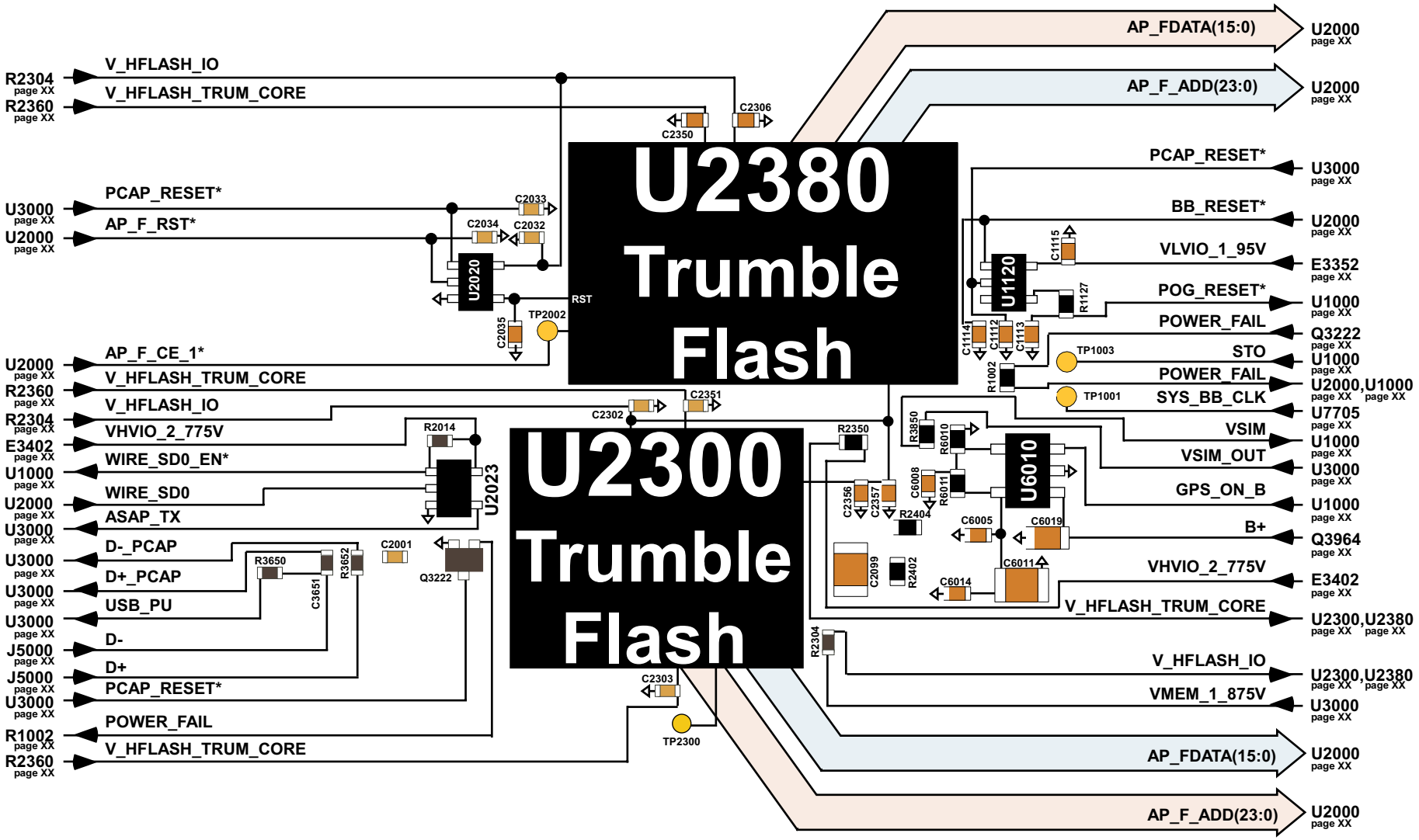
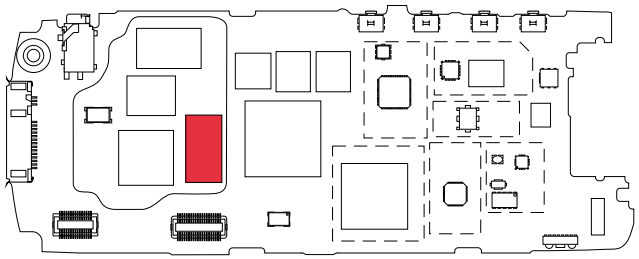
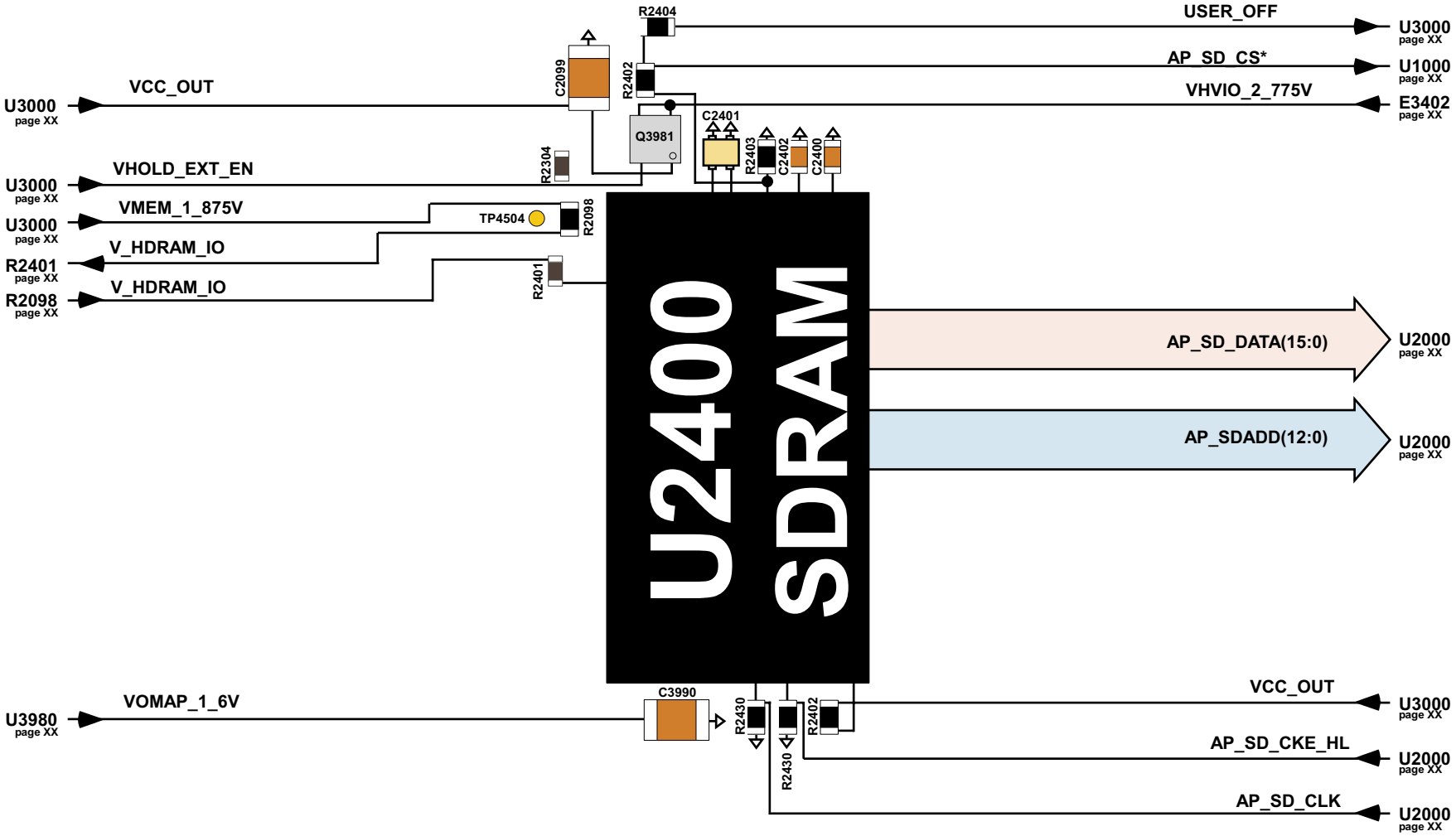
A920: Helen Flash Memory





A920: Helen SDRAM





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Parts List

Introduction

Motorola maintains a parts office staffed to process parts orders, identify part numbers, and otherwise assist in the maintenance and repair of Motorola Cellular products.
Orders for all parts listed in this document should be directed to the following Motorola International Logistics Department:

To order parts please use the following link:

https://wissc.motorola.com/wissc_root/main/BrowserOK.html
(Password is Required)

For information on ordering parts please contact EMEA at +49 461 803 1638.

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis.

If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

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Electrical Parts List

The following table lists the electrical parts list for the A920/A925 UMTS/GSM handset.

Table 10. Electrical Parts List

Reference Number	Part Number	Description
A1	3987724N02	CONTACT
A6050DNP	3988220M01	CONTACT
C001	2113743N03	CAP, 1pF
C002	0662057C01	RES, 0
C003	2113743N36	CAP, 27pF
C004	2113743N36	CAP, 27pF
C005	2113743N42	CAP, 47pF
C006	2113743N50	CAP, 100pF
C007	2113743N50	CAP, 100pF
C008	2113743N50	CAP, 100pF
C010	2113743N36	CAP, 27pF
C011	2113743N03	CAP, 1pF
C030	2113743N16	CAP, 3.9pF
C101	2113928P04	CAP, 1.0uF
C102	2113928P04	CAP, 1.0uF
C103	2113928P04	CAP, 1.0uF
C104	2113947C01	CAP, 1000pF
C106	2113928N01	CAP, 0.1uF
C107	2113947H01	CAP, 0.1uF
C112	2113928P04	CAP, 1.0uF
C113	2113928P04	CAP, 1.0uF
C114	2113928P04	CAP, 1.0uF
C115	2113743L17	CAP, 1000pF
C116	2113928N01	CAP, 0.1uF
C117	2113743M24	CAP, 0.1uF
C118	2113928C04	CAP, 4.7uF
C119	2113743M24	CAP, 0.1uF
C120	2113928N01	CAP, 0.1uF
C121	2113928N01	CAP, 0.1uF
C122	2113743M24	CAP, 0.1uF
C123	2113743M24	CAP, 0.1uF
C130	2113928N01	CAP, 0.1uF
C131	2113743L41	CAP, .01uF
C132	2113743L41	CAP, .01uF
C133	2113743L41	CAP, .01uF
C134	2113743L41	CAP, .01uF
C140	2113743E07	CAP, .022uF
C141	2113743L25	CAP, 2200pF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C142	2113743N46	CAP, 68pF
C145	2113743N01	CAP, 0.5pF
C146	2113928C04	CAP, 4.7uF
C148	2113743N22	CAP, 6.8pF
C150	2113743N28	CAP, 12pF
C151	2113743N28	CAP, 12pF
C156	2113743N16	CAP, 3.9pF
C157	2113743N16	CAP, 3.9pF
C200	2113743N38	CAP, 33pF
C201	2113743N50	CAP, 100pF
C205	2113743L17	CAP, 1000pF
C202DNP	2113743N03	CAP, 1pF
C203DNP	2113743N50	CAP, 100pF
C215	2113743E07	CAP, .022uF
C216	2113741F37	CAP, 3300pF
C221	2113743N30	CAP, 15pF
C222	2113743N30	CAP, 15pF
C223	2104801Z08	CAP, 1.2pF
C241	2113743L17	CAP, 1000pF
C242	2113743L17	CAP, 1000pF
C243	2113743L17	CAP, 1000pF
C244	2113743L05	CAP, 330pF
C245	2113743L05	CAP, 330pF
C250DNP	2113947B01	CAP, 10pF
C252DNP	2113947B01	CAP, 10pF
C260	2113743N28	CAP, 12pF
C261	2113743N16	CAP, 3.9pF
C270	2113743N50	CAP, 100pF
C280	2113743N50	CAP, 100pF
C282	2113743N09	CAP, 2pF
C290	2113743L17	CAP, 1000pF
C291	2113947C01	CAP, 1000pF
C292	2113743L17	CAP, 1000pF
C293	2113743L17	CAP, 1000pF
C294	2113743L17	CAP, 1000pF
C295	2113743L17	CAP, 1000pF
C296	2113743L17	CAP, 1000pF
C297	2113743L41	CAP, .01uF
C298	2113743N50	CAP, 100pF
C299	2113743L41	CAP, .01uF
C302	2113743N02	CAP, 0.75pF
C303	2113743N26	CAP, 10pF
C304	2113743N01	CAP, 0.5pF
C305	2113743N50	CAP, 100pF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C307	2113743N50	CAP, 100pF
C310	2113743N26	CAP, 10pF
C313	2409154M60	IDCTR, 5.6nH
C314	2113743Q07	CAP, 1.5pF
C315	2113743L41	CAP, .01uF
C316	2113743N26	CAP, 10pF
C317	2113743L41	CAP, .01uF
C319	2113743L41	CAP, .01uF
C321	2113743L41	CAP, .01uF
C323	2113743N34	CAP, 22pF
C324	2113743N34	CAP, 22pF
C325	2113743L17	CAP, 1000pF
C326	2113743L17	CAP, 1000pF
C327	2113743N23	CAP, 7.5pF
C330	2113743L29	CAP, 3300pF
C331	2113743E07	CAP, .022uF
C332	2113743N28	CAP, 12pF
C333	2113743N28	CAP, 12pF
C334	2113743N18	CAP, 4.7pF
C335	2113743N16	CAP, 3.9pF
C338	2113743N28	CAP, 12pF
C340	2113947C01	CAP, 1000pF
C342	2113743N50	CAP, 100pF
C344	2113743L05	CAP, 330pF
C348	2113743L41	CAP, .01uF
C349	2113743L41	CAP, .01uF
C360	2113743L41	CAP, .01uF
C361	2113743L41	CAP, .01uF
C410	2113743L01	CAP, 220pF
C413	2113743N38	CAP, 33pF
C414	2113743N38	CAP, 33pF
C420	2113743N30	CAP, 15pF
C421	2113743L41	CAP, .01uF
C422	2113928C04	CAP, 4.7uF
C425	2113743N28	CAP, 12pF
C444	2113743L41	CAP, .01uF
C445	2113743N50	CAP, 100pF
C448	2113743N26	CAP, 10pF
C449	2113743L41	CAP, .01uF
C451	2113743N28	CAP, 12pF
C452	2113947B05	CAP, 33pF
C453	2113743L17	CAP, 1000pF
C460	2113743N26	CAP, 10pF
C502	2113743L37	CAP, 6800pF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C503	2113740F59	CAP, 220pF
C504	2113743L13	CAP, 680pF
C505	2113741F45	CAP, 6800pF
C506	2113743L41	CAP, .01uF
C507	2113743N50	CAP, 100pF
C509	2113743N50	CAP, 100pF
C510	2113743M24	CAP, 0.1uF
C511	2113928C03	CAP, 1.0uF
C514	2113743L41	CAP, .01uF
C516	2113928C03	CAP, 1.0uF
C517	2113743L17	CAP, 1000pF
C520	2113928C04	CAP, 4.7uF
C521	2113928C04	CAP, 4.7uF
C522	2113928C04	CAP, 4.7uF
C523	2113928C04	CAP, 4.7uF
C524	2113743N34	CAP, 22pF
C525	2113743N28	CAP, 12pF
C526	2113743N32	CAP, 18pF
C527	2113743N32	CAP, 18pF
C528	2113743N38	CAP, 33pF
C535	2113928N01	CAP, 0.1uF
C536	2113743L41	CAP, .01uF
C537	2113928C04	CAP, 4.7uF
C538	2113928A01	CAP, 1.0uF
C539	2113743L41	CAP, .01uF
C540	2113947E01	CAP, .01uF
C542	2113947E01	CAP, .01uF
C543	2113928P04	CAP, 1.0uF
C544	2113928P04	CAP, 1.0uF
C545	2113928P04	CAP, 1.0uF
C546	2113947E01	CAP, .01uF
C554	2113743L01	CAP, 220pF
C555	2113743L01	CAP, 220pF
C556	2113743L05	CAP, 330pF
C560	2113743M24	CAP, 0.1uF
C576	2113743L05	CAP, 330pF
C600	2113743N34	CAP, 22pF
C602	2113928A01	CAP, 1.0uF
C603	2113743N12	CAP, 2.7pF
C604	2113743L05	CAP, 330pF
C605	2113743L05	CAP, 330pF
C606	2113743N54	CAP, 150pF
C607	2113743L05	CAP, 330pF
C608	2113743L05	CAP, 330pF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C609	2113743N54	CAP, 150pF
C610	2113743N36	CAP, 27pF
C631	2113928A01	CAP, 1.0uF
C632	2113743L41	CAP, .01uF
C650	2113743N38	CAP, 33pF
C651	2113743N38	CAP, 33pF
C660	2113743N28	CAP, 12pF
C661	2113743N28	CAP, 12pF
C670	2113743N28	CAP, 12pF
C671	2113743N28	CAP, 12pF
C700	2113928N01	CAP, 0.1uF
C701	2113743L03	CAP, 270pF
C702	2113743L17	CAP, 1000pF
C703	0888600M19	CAP, 3300pF
C704	2113743N12	CAP, 2.7pF
C705	2113743N28	CAP, 12pF
C708	2113743N20	CAP, 5.6pF
C710	2113743N28	CAP, 12pF
C711	2113743N50	CAP, 100pF
C712	2113743N28	CAP, 12pF
C800	2113928C04	CAP, 4.7uF
C801	2113743E20	CAP, 0.1uF
C802	2113743E20	CAP, 0.1uF
C803	2113743N26	CAP, 10pF
C804	2113743E20	CAP, 0.1uF
C805	2113928N01	CAP, 0.1uF
C806	2113743E20	CAP, 0.1uF
C808	2113743L01	CAP, 220pF
C810	2113743N38	CAP, 33pF
C812	2113743P01	CAP, 180pF
C830	0662057M01	RES, 0
C832	2113743N28	CAP, 12pF
C902	2113743N36	CAP, 27pF
C903	2113743N28	CAP, 12pF
C908	2113743N38	CAP, 33pF
C909	2113743N38	CAP, 33pF
C910	2113743L41	CAP, .01uF
C1000	2113743M24	CAP, 0.1uF
C1001	2113743M24	CAP, 0.1uF
C1002	2113743M24	CAP, 0.1uF
C1003	2113743M24	CAP, 0.1uF
C1004	2113743M24	CAP, 0.1uF
C1005	2113743M24	CAP, 0.1uF
C1006	2113743M24	CAP, 0.1uF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C1007	2113743M24	CAP, 0.1uF
C1008	2113743M24	CAP, 0.1uF
C1009	2113743M24	CAP, 0.1uF
C1010	2113743M24	CAP, 0.1uF
C1011	2113743M24	CAP, 0.1uF
C1012	2113743M24	CAP, 0.1uF
C1013	2113743M24	CAP, 0.1uF
C1014	2113743M24	CAP, 0.1uF
C1015	2113743M24	CAP, 0.1uF
C1016	2113743M24	CAP, 0.1uF
C1017	2113743M24	CAP, 0.1uF
C1018	2113743M24	CAP, 0.1uF
C1019	2113743M24	CAP, 0.1uF
C1020	2113743M24	CAP, 0.1uF
C1021	2113743M24	CAP, 0.1uF
C1022	2113743M24	CAP, 0.1uF
C1026	2113743M24	CAP, 0.1uF
C1027	2113743M24	CAP, 0.1uF
C1028	2113743M24	CAP, 0.1uF
C1029	2113743M24	CAP, 0.1uF
C1030	2113743M24	CAP, 0.1uF
C1031	2113743M24	CAP, 0.1uF
C1032	2113743M24	CAP, 0.1uF
C1033	2113743M24	CAP, 0.1uF
C1034	2113743M24	CAP, 0.1uF
C1110	2113743M24	CAP, 0.1uF
C1112	2113743M24	CAP, 0.1uF
C1113	2113743L41	CAP, .01uF
C1114	2113743M24	CAP, 0.1uF
C1115	2113743M24	CAP, 0.1uF
C1140	2113743M24	CAP, 0.1uF
C1150	2113743M24	CAP, 0.1uF
C1300	2113743M24	CAP, 0.1uF
C1301	2113743M24	CAP, 0.1uF
C1302	2113743M24	CAP, 0.1uF
C1303	2113743M24	CAP, 0.1uF
C1304	2113743M24	CAP, 0.1uF
C1305	2113743M24	CAP, 0.1uF
C1306	2113743M24	CAP, 0.1uF
C1307	2113743M24	CAP, 0.1uF
C1308	2113743M24	CAP, 0.1uF
C1309	2113743M24	CAP, 0.1uF
C1400	2113743M24	CAP, 0.1uF
C1401	2113743M24	CAP, 0.1uF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C1402	2113743M24	CAP, 0.1uF
C1403	2113743M24	CAP, 0.1uF
C2001	2113743N30	CAP, 15pF
C2002	2113743N30	CAP, 15pF
C2003	2113928N01	CAP, 0.1uF
C2004	2113928N01	CAP, 0.1uF
C2005	2113928N01	CAP, 0.1uF
C2006	2113928N01	CAP, 0.1uF
C2008	2113928N01	CAP, 0.1uF
C2009	2113928N01	CAP, 0.1uF
C2010	2113928N01	CAP, 0.1uF
C2011	2113928N01	CAP, 0.1uF
C2012	2113928N01	CAP, 0.1uF
C2013	2113928N01	CAP, 0.1uF
C2014	2113928N01	CAP, 0.1uF
C2015	2113928N01	CAP, 0.1uF
C2016	2113928N01	CAP, 0.1uF
C2017	2113928N01	CAP, 0.1uF
C2018	2113928N01	CAP, 0.1uF
C2019	2113928N01	CAP, 0.1uF
C2020	2113743M24	CAP, 0.1uF
C2021	2113928N01	CAP, 0.1uF
C2022	2113928N01	CAP, 0.1uF
C2023	2113743N34	CAP, 22pF
C2024	2113743N34	CAP, 22pF
C2025	2113928N01	CAP, 0.1uF
C2026	2113743M24	CAP, 0.1uF
C2027	2113928C12	CAP, 10uF
C2028	2113928N01	CAP, 0.1uF
C2030	2113928N01	CAP, 0.1uF
C2032	2113928N01	CAP, 0.1uF
C2033	2113928N01	CAP, 0.1uF
C2034	2113928N01	CAP, 0.1uF
C2035	2113928N01	CAP, 0.1uF
C2070	2113743N38	CAP, 33pF
C2090	2113928N01	CAP, 0.1uF
C2094	2113928N01	CAP, 0.1uF
C2097	2113928N01	CAP, 0.1uF
C2098	2113928N01	CAP, 0.1uF
C2099	2113928C12	CAP, 10uF
C2302	2113928N01	CAP, 0.1uF
C2303	2113928N01	CAP, 0.1uF
C2306	2113928N01	CAP, 0.1uF
C2350	2113928N01	CAP, 0.1uF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C2351	2113928N01	CAP, 0.1uF
C2356	2113928N01	CAP, 0.1uF
C2357	2113928N01	CAP, 0.1uF
C2400	2113928N01	CAP, 0.1uF
C2401	2113947H01	CAP, 0.1uF
C2402	2113928N01	CAP, 0.1uF
C3000	2113928C12	CAP, 10uF
C3001	2113928C12	CAP, 10uF
C3002	2113928N01	CAP, 0.1uF
C301DNP	2113743N02	CAP, 0.75pF
C3050	2113928C12	CAP, 10uF
C3051	2113928C12	CAP, 10uF
C3052	2113928N01	CAP, 0.1uF
C3053	2113928N01	CAP, 0.1uF
C3100	2113928C12	CAP, 10uF
C3101	2113928C12	CAP, 10uF
C3150	2113928C04	CAP, 4.7uF
C3151DNP	2113743N38	CAP, 33pF
C3200	2113928C12	CAP, 10uF
C3201	2113928C12	CAP, 10uF
C3220	2113928C12	CAP, 10uF
C3221	2113743L17	CAP, 1000pF
C3222	2113743N35	CAP, 24pF
C3224	2113928C12	CAP, 10uF
C3225	2113928C12	CAP, 10uF
C3226	2113928C12	CAP, 10uF
C3228	2113743N38	CAP, 33pF
C3229	2113743N38	CAP, 33pF
C3227DNP	2113743N38	CAP, 33pF
C3250	2113928C04	CAP, 4.7uF
C3300	2113928C04	CAP, 4.7uF
C3350	2113928C12	CAP, 10uF
C339DNP	2113743N50	CAP, 100pF
C3400	2113928C12	CAP, 10uF
C3401	2113928C12	CAP, 10uF
C3402	2113743M24	CAP, 0.1uF
C3450	2113928C04	CAP, 4.7uF
C345DNP	2113743L17	CAP, 1000pF
C3500	2113928C12	CAP, 10uF
C3501	2113928C12	CAP, 10uF
C3502	2113743M24	CAP, 0.1uF
C3550	2113928C04	CAP, 4.7uF
C3555	2113743N35	CAP, 24pF
C3560	2113928C12	CAP, 10uF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C3561	2113928C12	CAP, 10uF
C3562	2113743M24	CAP, 0.1uF
C3600	2113928C12	CAP, 10uF
C3602	2113743N40	CAP, 39pF
C3601DNP	2113743N40	CAP, 39pF
C3650	2113928C04	CAP, 4.7uF
C3651DNP	2113947B05	CAP, 33pF
C3801	2113928C04	CAP, 4.7uF
C3850	2113928C04	CAP, 4.7uF
C3851	2113928C04	CAP, 4.7uF
C3852	2113928N01	CAP, 0.1uF
C3900	2113928C04	CAP, 4.7uF
C3903	2113743N38	CAP, 33pF
C3904	2113743N38	CAP, 33pF
C3906	2113743N50	CAP, 100pF
C3901DNP	2113947B05	CAP, 33pF
C3902DNP	2113743N38	CAP, 33pF
C3910	2113928C12	CAP, 10uF
C3911	2113928C12	CAP, 10uF
C3912	2113928N01	CAP, 0.1uF
C3914DNP	2113743N26	CAP, 10pF
C3950	2113928C04	CAP, 4.7uF
C3951	2113743M24	CAP, 0.1uF
C3961	2113928C12	CAP, 10uF
C3962	2113743M24	CAP, 0.1uF
C3963	2113928N01	CAP, 0.1uF
C3964	2113928N01	CAP, 0.1uF
C3965	2113928N01	CAP, 0.1uF
C3966	2113743N38	CAP, 33pF
C3967	2113743N38	CAP, 33pF
C3960DNP	2113743L35	CAP, 5600pF
C3980	2113928C03	CAP, 1.0uF
C3981	2113743N38	CAP, 33pF
C3983	2113743N37	CAP, 30pF
C3984	2113743N34	CAP, 22pF
C3985	2113928C12	CAP, 10uF
C3987	2113928C12	CAP, 10uF
C3989	2113928P04	CAP, 1.0uF
C3990	2113928C12	CAP, 10uF
C3991	2113928C12	CAP, 10uF
C3993	2113743L41	CAP, .01uF
C3992DNP	2113743L41	CAP, .01uF
C3998DNP	2113743L35	CAP, 5600pF
C4000	2113928P04	CAP, 1.0uF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C4002	2113743L13	CAP, 680pF
C4003	2113947B05	CAP, 33pF
C4008	2113947B05	CAP, 33pF
C4100	2113928P04	CAP, 1.0uF
C4110	2113743N38	CAP, 33pF
C4112	2113928C04	CAP, 4.7uF
C4113	2113743N26	CAP, 10pF
C4114	2113743N38	CAP, 33pF
C4160	2113743N38	CAP, 33pF
C4198	2113947H01	CAP, 0.1uF
C4200	2113743M24	CAP, 0.1uF
C4202	2113743L13	CAP, 680pF
C4203	2113947B05	CAP, 33pF
C4207	2113947B05	CAP, 33pF
C4210	2113928C04	CAP, 4.7uF
C4213	2113743M24	CAP, 0.1uF
C4301	2113743N38	CAP, 33pF
C4302	2113743N38	CAP, 33pF
C4303	2113743N38	CAP, 33pF
C4304	2113947E01	CAP, .01uF
C4306	2311049A89	CAPP, 22uF
C4355	2113947B05	CAP, 33pF
C4356	2311049A89	CAPP, 22uF
C4380DNP	2113928C04	CAP, 4.7uF
C4390	2113743M24	CAP, 0.1uF
C4392	2113743N38	CAP, 33pF
C4393	2113743N38	CAP, 33pF
C4394	2113743N38	CAP, 33pF
C4395	2113743M24	CAP, 0.1uF
C4400	2113928A01	CAP, 1.0uF
C4401	2113743M24	CAP, 0.1uF
C4402	2113743N26	CAP, 10pF
C441DNP	2113743L41	CAP, .01uF
C442DNP	2113743N50	CAP, 100pF
C443DNP	2113743N50	CAP, 100pF
C4500	2113743M24	CAP, 0.1uF
C4501	2113743N38	CAP, 33pF
C4502	2113928C04	CAP, 4.7uF
C4503	2113743M24	CAP, 0.1uF
C4504	2113928C04	CAP, 4.7uF
C4550	2113743L25	CAP, 2200pF
C4551	2113743L41	CAP, .01uF
C5000	2113743M24	CAP, 0.1uF
C5002	2113743N38	CAP, 33pF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C5003	2113743N38	CAP, 33pF
C5010	2113743L41	CAP, .01uF
C5050	2113743M24	CAP, 0.1uF
C5053	2113928A01	CAP, 1.0uF
C508DNP	2113743N28	CAP, 12pF
C5100	2113743L41	CAP, .01uF
C5101	2113743L41	CAP, .01uF
C5102	2113743L41	CAP, .01uF
C5103	2113743L41	CAP, .01uF
C5104	2113743L41	CAP, .01uF
C5105	2113743L41	CAP, .01uF
C5106	2113743L41	CAP, .01uF
C5107	2113743L41	CAP, .01uF
C5200	2113947B05	CAP, 33pF
C5202	2113947B05	CAP, 33pF
C5204	2113947B05	CAP, 33pF
C5206	2113947B05	CAP, 33pF
C5208	2113947B05	CAP, 33pF
C5210	2113947B05	CAP, 33pF
C5212	2113743N38	CAP, 33pF
C5213	2113743N38	CAP, 33pF
C5214	2113947B05	CAP, 33pF
C5218	2113947B05	CAP, 33pF
C5220	2113947B05	CAP, 33pF
C5222	2113947B05	CAP, 33pF
C5224	2113947B05	CAP, 33pF
C5226	2113743N38	CAP, 33pF
C5227	2113743N38	CAP, 33pF
C5228	2113947B05	CAP, 33pF
C5229	2113743L25	CAP, 2200pF
C5230	2113743L25	CAP, 2200pF
C534DNP	2113743N34	CAP, 22pF
C5400	2113928C12	CAP, 10uF
C5401	2113743N22	CAP, 6.8pF
C5402	2113743M24	CAP, 0.1uF
C5403	2113743N38	CAP, 33pF
C5404	2113743N38	CAP, 33pF
C5405	2113743N38	CAP, 33pF
C5407	2113743L41	CAP, .01uF
C5410	2113928C12	CAP, 10uF
C5411	2113928N01	CAP, 0.1uF
C5412	2113928N01	CAP, 0.1uF
C5413	2113928P04	CAP, 1.0uF
C5501	2113743N38	CAP, 33pF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C5503	2113743N38	CAP, 33pF
C5504	2113743N38	CAP, 33pF
C5505	2113743N38	CAP, 33pF
C5506	2113928N01	CAP, 0.1uF
C5507	2113743N38	CAP, 33pF
C5508	2113928N01	CAP, 0.1uF
C5509DNP	2113928N01	CAP, 0.1uF
C5600	2113743M24	CAP, 0.1uF
C5604	2113743M24	CAP, 0.1uF
C5607	2113743N09	CAP, 2pF
C5608	2113743L23	CAP, 1800pF
C5605DNP	2113743N03	CAP, 1pF
C5611	2113743N52	CAP, 120pF
C5612	2113743L41	CAP, .01uF
C5613	2113743L01	CAP, 220pF
C5614	2113743L07	CAP, 390pF
C5615	2113743L37	CAP, 6800pF
C5616	2113743M24	CAP, 0.1uF
C5617	2113743L41	CAP, .01uF
C5618	2113743N26	CAP, 10pF
C5620	2113743N26	CAP, 10pF
C5621	2113743N26	CAP, 10pF
C5622	2113928N01	CAP, 0.1uF
C5623	2113928N01	CAP, 0.1uF
C5624	2113928N01	CAP, 0.1uF
C5649DNP	2113743N26	CAP, 10pF
C5650	2113743N03	CAP, 1pF
C5651	2113743N01	CAP, 0.5pF
C5670	2113928N01	CAP, 0.1uF
C5671	2113743L17	CAP, 1000pF
C5700	2113743N38	CAP, 33pF
C6000	2113743F18	CAP, 2.2uF
C6001	2113743M24	CAP, 0.1uF
C6002	2113743M24	CAP, 0.1uF
C6003	2113743M24	CAP, 0.1uF
C6004	2113947H01	CAP, 0.1uF
C6005	2113743N38	CAP, 33pF
C6007	2113743M24	CAP, 0.1uF
C6008	2113743N38	CAP, 33pF
C6009	2113743M24	CAP, 0.1uF
C6010	2113743L41	CAP, .01uF
C6011	2113928C12	CAP, 10uF
C6012	2113743L01	CAP, 220pF
C6014	2113928N01	CAP, 0.1uF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C6019	2113928P04	CAP, 1.0uF
C6050	2113743N32	CAP, 18pF
C6051	2113743L09	CAP, 470pF
C6052	2113743N52	CAP, 120pF
C6053	2113743N09	CAP, 2pF
C6055	2113743N12	CAP, 2.7pF
C6057	2113743L09	CAP, 470pF
C6058	2113743M24	CAP, 0.1uF
C6059	2113743M24	CAP, 0.1uF
C6056DNP	2113743N03	CAP, 1pF
C6060	2113743N42	CAP, 47pF
C6061	2113743L13	CAP, 680pF
C6062	2113743L41	CAP, .01uF
C6063	2113743M24	CAP, 0.1uF
C6064	2113743M24	CAP, 0.1uF
C6065	2113743M24	CAP, 0.1uF
C6066	2113743M24	CAP, 0.1uF
C6067	2113743N05	CAP, 1.2pF
C6069	2113743L17	CAP, 1000pF
C6070	2113743N26	CAP, 10pF
C6080	2113743N32	CAP, 18pF
C6082	2187893N01	CAP, 1.0uF
C6083	2187893N01	CAP, 1.0uF
C6084	2113743N52	CAP, 120pF
C6090DNP	2113743N09	CAP, 2pF
C6091DNP	2113743N03	CAP, 1pF
C6500	2113928P04	CAP, 1.0uF
C6501	2113928C12	CAP, 10uF
C6502	2113743N38	CAP, 33pF
C6503	2113743N38	CAP, 33pF
C6504	2113743N38	CAP, 33pF
C6510DNP	2113743N38	CAP, 33pF
C6511DNP	2113743N38	CAP, 33pF
C706DNP	2113743N03	CAP, 1pF
C7610	2113743N38	CAP, 33pF
C7611	2113743N38	CAP, 33pF
C7612	2113947B05	CAP, 33pF
C7613	2113743N38	CAP, 33pF
C7615	2113946D02	CAP, 1.0uF
C7616	2113946D02	CAP, 1.0uF
C7617	2113946D02	CAP, 1.0uF
C7618	2113928N01	CAP, 0.1uF
C7620	2113743N30	CAP, 15pF
C7621	2113743L09	CAP, 470pF

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
C7630	2113928N01	CAP, 0.1uF
C7631	2113928N01	CAP, 0.1uF
C7632	2113928N01	CAP, 0.1uF
C7633	2113928N01	CAP, 0.1uF
C7634	2113928N01	CAP, 0.1uF
C7640	2113743L17	CAP, 1000pF
C7641	2113743L41	CAP, .01uF
C7642	2113743L17	CAP, 1000pF
C7643	2113743M24	CAP, 0.1uF
C7644	2113743M24	CAP, 0.1uF
C7726	2113743N38	CAP, 33pF
C7729	2113743N38	CAP, 33pF
C7721DNP	2113743N38	CAP, 33pF
C7730	2113743N38	CAP, 33pF
C7731	2113743M24	CAP, 0.1uF
C813DNP	2113743N38	CAP, 33pF
C901DNP	2113743M24	CAP, 0.1uF
CR200	4809877C32	SMV1763
CR201	4809877C32	SMV1763
CR330	4809877C32	SMV1763
CR331	4809877C32	SMV1763
CR1300	4809924D18	RB520S-30
CR3000	4809924D18	RB520S-30
CR3050	4809653F02	MBRM120T3
CR3100	4809924D18	RB520S-30
CR3960	4809653F02	MBRM120T3
CR3961	4809653F02	MBRM120T3
CR5005	4809948D42	RB751V40
D5101	4809788E17	EDZ68B
D5110	4809788E17	EDZ68B
D5300	4809118D02	LNJ115W8P0MT
E100	SHORT_RES0402	SHORT
E108	SHORT_RES0402	SHORT
E109	SHORT_RES0402	SHORT
E110	SHORT_RES0402	SHORT
E111	SHORT_RES0402	SHORT
E528	SHORT_RES0402	SHORT
E529	SHORT_RES0402	SHORT
E530	SHORT_RES0402	SHORT
E975	SHORT_RES0402	SHORT
E976	SHORT_RES0402	SHORT
E977	SHORT_RES0402	SHORT
E2013	SHORT_RES0402	SHORT
E2320	SHORT_RES0402	SHORT

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
E3003	SHORT_RES0402	SHORT
E3050	SHORT_RES0402	SHORT
E3103	SHORT_RES0402	SHORT
E3153	SHORT_RES0402	SHORT
E3203	SHORT_RES0402	SHORT
E3251	SHORT_RES0402	SHORT
E3352	SHORT_RES0402	SHORT
E3402	SHORT_RES0402	SHORT
E3403	SHORT_RES0402	SHORT
E3451	SHORT_RES0402	SHORT
E3503	SHORT_RES0402	SHORT
E3552	SHORT_RES0402	SHORT
E3601	SHORT_RES0402	SHORT
E3900	SHORT_RES0402	SHORT
E3916	SHORT_RES0402	SHORT
E3951	SHORT_RES0402	SHORT
E3965	SHORT_RES0402	SHORT
E6001	SHORT_BAR0_61	SHORTING_BAR
E6002	SHORT_BAR0_61	SHORTING_BAR
E6003	SHORT_BAR0_61	SHORTING_BAR
E6006	SHORT_RES0402	SHORT
E6009	SHORT_RES0402	SHORT
E6062	SHORT_RES0402	SHORT
FL001	4889695L12	ASM3201B
FL010	9109674L20	S0351
FL020	9109674L22	74L22
FL030	9109674L18	S0350
FL150	5885949K03	LDD15A
FL201	9109405J17	SAFCD380
FL300	9109239M28 fl	SAF2G14KB0
FL310	9109674L14	LFSG20N25
FL320	9109405J16	FLTR
FL410	9109239M16 fl	SAF1G95KB0
FL460	5888234M01	34M01
FL500	9188695K04 bg	95K04
FL510	4887925N01	FLTR
FL4300	4889526L04 bg	FLTR
FL5601	9109239M23	LE65A
FL6050	9109239M26	855969
FL6055	9185223E01	DFM2R1575
J001	0788468M03	CONTACT
J3900	0988365M02 c	CONN_J
J4100DNP	5085600J01	SPKR
J4200DNP	2888328M01	CONN_P

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number		Description
J4300	0904136G01		CONN_J
J5000	0987636K05	c	CONN_J
J5200	0987817K05	c	CONN_J
J5400	3987522K03		CONTACT
J5500	3909426M05		BM050406
J7600	0987817K04	c	CONN_J
J7700	0987817K04	c	CONN_J
L003	2462587P55		IDCTR, 82nH
L005	2409154M14		IDCTR, 12.0nH
L010	2409154M59		IDCTR, 4.7nH
L150	2409154M79		IDCTR, 1.8nH
L152	2409154M81		IDCTR, 2.7nH
L153	SHORT_RES0402		SHORT
L200	0660076S01		RES, 0
L201	2485793G04		IDCTR, 10nH
L223	2485793G04		IDCTR, 10nH
L240	2409377M16		IDCTR, 82nH
L241	2409377M16		IDCTR, 82nH
L242	2488289M24		IDCTR, 82nH
L243	2488289M25		IDCTR, 100nH
L280	2409154M09		IDCTR, 4.7nH
L281	2409154M09		IDCTR, 4.7nH
L297	2409377M16		IDCTR, 82nH
L298	2409377M16		IDCTR, 82nH
L302DNP	2409154M07		IDCTR, 3.3nH
L313	2409154M56		IDCTR, 2.7nH
L314	2409154M73		IDCTR, 68.0nH
L315	2113743N02		CAP, 0.75pF
L316	2113743N26		CAP, 10pF
L320	2409646M86		IDCTR, 27nH
L321	2409646M86		IDCTR, 27nH
L324	2485793G15		IDCTR, 82nH
L325	2485793G15		IDCTR, 82nH
L330	2409377M08		IDCTR, 22nH
L610	2409154M11		IDCTR, 6.8nH
L701	2409154M70		IDCTR, 39.0nH
L703	2409154M47		IDCTR, 82.0nH
L710	2113743N12		CAP, 2.7pF
L713	2409154M65		IDCTR, 15.0nH
L810	2409154M09		IDCTR, 4.7nH
L821	2409154M61		IDCTR, 6.8nH
L825	2409154M52		IDCTR, 1.2nH
L832	2409154M09		IDCTR, 4.7nH
L3000	2588866L14		IDCTR, 47uH

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number		Description
L3050	2588866L14		IDCTR, 47uH
L3100	2487659M11		IDCTR, 47uH
L3220	2588866L05		IDCTR, 2.2uH
L3560	2487996L04		EXCML16
L4399	2409646M13		IDCTR, 39nH
L4400	2409154M71		IDCTR, 47.0nH
L4401	2409154M71		IDCTR, 47.0nH
L5600	2409154M08		IDCTR, 3.9nH
L5601	2409154M08		IDCTR, 3.9nH
L5602	2409154M08		IDCTR, 3.9nH
L5604	2409154M03		IDCTR, 1.5nH
L6000	0662057M01		RES, 0
L6050	2409154M11		IDCTR, 6.8nH
L6051	2409154M11		IDCTR, 6.8nH
L6053	2409154M12		IDCTR, 8.2nH
L6080	2409704K43		IDCTR, 33nH
L7600	2462587Q46		IDCTR, 820nH
L7640	2462587Q59		IDCTR, 10uH
L831DNP	2409154M65		IDCTR, 15.0nH
M001	0987378K01		SWITCH
M5700	5909382K09		MOTOR
M6050	0987378K01		SWITCH
Q130	4809579E24		2SJ347
Q420	4809608E03		DTA114YE
Q510	4862830F01	bga	SI8401DB
Q700	4809579E16		TN0200T
Q901	4809579E58		FDG6332C
Q902	4809579E48		FDC6306P
Q906	4809939C34		EMB10
Q3220	4809579E43		FDG6303N
Q3222	4809579E02		2SK1830
Q3403	4809607E04		2SB1132
Q3502	4809607E04		2SB1132
Q3610	4809607E04		2SB1132
Q3960	4862830F01	bga	SI8401DB
Q3963	4862830F01	bga	SI8401DB
Q3964	4862830F01	bga	SI8401DB
Q3966	4862830F01	bga	SI8401DB
Q3967	4809939C39		EMD9
Q3980	4809579E49		SI6467DQ
Q3981	4862830F01	bga	SI8401DB
Q4300	4809940E03		DTC114TE
Q5000	4809579E58		FDG6332C
Q5600	5109572E39		AS179_92

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
Q6050	4809579E50	SI1905
Q6051	4809579E24	2SJ347
R009	0662057M01	RES, 0
R1003DNP	0662057M01	RES, 0
R1004DNP	0662057M01	RES, 0
R1006DNP	0662057N15	RES, 47K
R1060DNP	0662057M01	RES, 0
R1100DNP	0662057M98	RES, 10K
R1102DNP	0662057N23	RES, 100K
R1104DNP	0662057M01	RES, 0
R1122DNP	0662057M98	RES, 10K
R1150DNP	0662057M98	RES, 10K
R1200DNP	0662057M01	RES, 0
R130	0662057M74	RES, 1K
R131	0662057N09	RES, 27K
R132	0662057N09	RES, 27K
R133	0662057M01	RES, 0
R134	0662057N39	RES, 470K
R1000	0662057M01	RES, 0
R1001	0662057M01	RES, 0
R1002	0662057M01	RES, 0
R1061	0662057M01	RES, 0
R1101	0662057N23	RES, 100K
R1103	0662057N23	RES, 100K
R1105	0662057M01	RES, 0
R1127	0662057M74	RES, 1K
R1300	0662057M98	RES, 10K
R1303	0662057M01	RES, 0
R1304	0662057M01	RES, 0
R1301DNP	0662057M98	RES, 10K
R135DNP	0662057M01	RES, 0
R140	0662057M70	RES, 680
R141	0662057M94	RES, 6.8K
R146	0662057M36	RES, 27
R147	0609591M17	RESNET, 220
R1401DNP	0662057M01	RES, 0
R150	0662057M50	RES, 100
R151	SHORT_RES0402	SHORT
R200	0662057N15	RES, 47K
R201	0662057M98	RES, 10K
R203	SHORT_RES0402	SHORT
R205	0662057M43	RES, 51
R2009DNP	0662057B27	RES, 1.6MEG
R213	0609591M37	RESNET, 10K

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R215	0662057V02	RES, 10K
R230	0662057N15	RES, 47K
R231	SHORT_RES0402	SHORT
R232	SHORT_RES0402	SHORT
R240	0662057M26	RES, 10
R250	0609591M01	RESNET, 10
R252	0609591M01	RESNET, 10
R270	0662057M50	RES, 100
R290	SHORT_RES0402	SHORT
R291	SHORT_RES0402	SHORT
R292	SHORT_RES0402	SHORT
R293	0662057M01	RES, 0
R294	0662057M01	RES, 0
R295	0662057M01	RES, 0
R296	SHORT_RES0402	SHORT
R301	0662057M85	RES, 3K
R304	0662057M50	RES, 100
R305	0662057M26	RES, 10
R315	0662057M26	RES, 10
R319	0662057M26	RES, 10
R320	2113743N22	CAP, 6.8pF
R321	0662057M26	RES, 10
R325	0662057M70	RES, 680
R330	0662057M01	RES, 0
R331	0662057M98	RES, 10K
R332	0609591M37	RESNET, 10K
R335	0662057M01	RES, 0
R336	0662057M01	RES, 0
R337	0662057M01	RES, 0
R338	0662057M01	RES, 0
R339	0662057M01	RES, 0
R341	0662057M01	RES, 0
R342	0662057M01	RES, 0
R344	0662057M74	RES, 1K
R346	0662057N15	RES, 47K
R347	SHORT_RES0402	SHORT
R348	0662057M26	RES, 10
R349	0662057M26	RES, 10
R360	SHORT_RES0402	SHORT
R361	SHORT_RES0402	SHORT
R410	0662057M90	RES, 4.7K
R411	0662057M70	RES, 680
R412	0662057M70	RES, 680
R420	0662057M01	RES, 0

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R431	SHORT_RES0402	SHORT
R432	SHORT_RES0402	SHORT
R450	0662057M95	RES, 7.5K
R451	0662057M90	RES, 4.7K
R452	0662057M98	RES, 10K
R453	0662057N20	RES, 75K
R454	SHORT_RES0402	SHORT
R455	SHORT_RES0402	SHORT
R456	0662057M90	RES, 4.7K
R457	0662057N11	RES, 33K
R503	0662057M83	RES, 2.4K
R504	0662057M74	RES, 1K
R506	0662057N19	RES, 68K
R508	0662057M01	RES, 0
R511	0662057N21	RES, 82K
R536	SHORT_RES0402	SHORT
R537	0662057M98	RES, 10K
R554	0662057N19	RES, 68K
R556	0662057N30	RES, 200K
R576	0662057N15	RES, 47K
R577	0662057M96	RES, 8.2K
R610	SHORT_RES0402	SHORT
R611	0662057N30	RES, 200K
R612	0662057M58	RES, 220
R615	0662057M01	RES, 0
R700	0662057M28	RES, 12
R701	0662057M38	RES, 33
R704	0662057M64	RES, 390
R705	0662057M76	RES, 1.2K
R707	0662057M56	RES, 180
R807	0662057M39	RES, 36
R810	0662057U95	RES, 5.6K
R812	0662057V02	RES, 10K
R813	0662057V02	RES, 10K
R814	0662057M43	RES, 51
R815	0662057U98	RES, 7.5K
R816	0662057U60	RES, 220
R822	0662057M01	RES, 0
R900	0662057M98	RES, 10K
R901	0662057M98	RES, 10K
R902	0662057M98	RES, 10K
R903	0662057N15	RES, 47K
R904	0662057M01	RES, 0
R912	0662057N15	RES, 47K

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R1400	0662057M01	RES, 0
R1402	0662057M01	RES, 0
R2002	0662057M98	RES, 10K
R2003	0662057M98	RES, 10K
R2006	0662057M98	RES, 10K
R2011	0662057M01	RES, 0
R2012	0662057M01	RES, 0
R2014	0662057N11	RES, 33K
R2026	0609591M37	RESNET, 10K
R2027	0662057N23	RES, 100K
R2028	0662057M50	RES, 100
R2029	0662057M50	RES, 100
R2030	0662057M98	RES, 10K
R2040	0662057N23	RES, 100K
R2041	0662057M35	RES, 24
R2042	0662057M35	RES, 24
R2043	0662057N03	RES, 15K
R2044	0662057N03	RES, 15K
R2045	0662057N23	RES, 100K
R2050	0662057M82	RES, 2.2K
R2051	0662057M01	RES, 0
R2055	0662057M98	RES, 10K
R2059	0662057M98	RES, 10K
R2056DNP	0662057M98	RES, 10K
R2070	0662057M50	RES, 100
R2097	0662057M26	RES, 10
R2098	0662057M01	RES, 0
R2304	0662057M01	RES, 0
R2350	0662057M01	RES, 0
R2400	0662057M01	RES, 0
R2401	0662057M01	RES, 0
R2402	0662057N23	RES, 100K
R2403	0662057V35	RES, 200K
R2404	0662057M01	RES, 0
R2430	0662057V35	RES, 200K
R2431	0662057V35	RES, 200K
R3004	0687874L02	RES, 0.1
R3051	0687874L02	RES, 0.1
R3055	0662057U85	RES, 2.2K
R3056	0662057V13	RES, 27K
R3057	0662057M01	RES, 0
R3104	0687874L02	RES, 0.1
R3205DNP	0662057M01	RES, 0
R3221	0662057N23	RES, 100K

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R3222	0662057N01	RES, 12K
R3223	0662057N35	RES, 330K
R3224	0662057V32	RES, 150K
R3225	0662057V32	RES, 150K
R3228	0662057N47	RES, 1MEG
R3400	0687874L02	RES, 0.1
R3504	0687874L02	RES, 0.1
R350DNP	0662057M01	RES, 0
R3553	0662057M50	RES, 100
R3561	0687874L02	RES, 0.1
R3650	0662057M78	RES, 1.5K
R3651	0662057M37	RES, 30
R3652	0662057M37	RES, 30
R3850	SHORT_RES0402	SHORT
R3902	0662057M50	RES, 100
R3904	0662057M50	RES, 100
R3910	0662057U98	RES, 7.5K
R3911	0662057V02	RES, 10K
R3912	0662057N23	RES, 100K
R3961	0687874L01	RES, 0.24
R3963	0662057V35	RES, 200K
R3990	0662057V35	RES, 200K
R3995	0662057N23	RES, 100K
R3997	0662057N23	RES, 100K
R3998	0662057V35	RES, 200K
R3999	0662057M01	RES, 0
R3994DNP	0662057M01	RES, 0
R4004	0609591M05	RESNET, 22
R4103	0662057M90	RES, 4.7K
R4200	0662057N03	RES, 15K
R4201	0662057N06	RES, 20K
R421DNP	0662057M98	RES, 10K
R4305	0662057N47	RES, 1MEG
R4306	0662057N39	RES, 470K
R4393	0662057M98	RES, 10K
R4395	0662057M98	RES, 10K
R4396	0662057M90	RES, 4.7K
R4397	0662057N39	RES, 470K
R4398	0662057M68	RES, 560
R4400	0662057M50	RES, 100
R4401	0662057M74	RES, 1K
R4550	0662057N06	RES, 20K
R5000	0662057N23	RES, 100K
R5001	0662057N15	RES, 47K

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R5002	0662057M98	RES, 10K
R5003	0662057N13	RES, 39K
R5004	0662057N23	RES, 100K
R5005	0662057N15	RES, 47K
R5006	0609591M49	RESNET, 100K
R5009	0662057N39	RES, 470K
R5007DNP	0662057N23	RES, 100K
R5008DNP	0662057M01	RES, 0
R5050	0662057N15	RES, 47K
R5052	0662057N33	RES, 270K
R5053	0662057M86	RES, 3.3K
R5100	0662057M98	RES, 10K
R5101	0609591M37	RESNET, 10K
R5102	0609591M37	RESNET, 10K
R5113	0662057M26	RES, 10
R5114	0662057M50	RES, 100
R5115	0662057M50	RES, 100
R5116	0662057M50	RES, 100
R5117	0662057M50	RES, 100
R5118	0662057M50	RES, 100
R5119	0662057M50	RES, 100
R5120	0662057M50	RES, 100
R5121	0662057M50	RES, 100
R5200	0662057M98	RES, 10K
R526DNP	0662057M98	RES, 10K
R5300	0662057M34	RES, 22
R5301	0662057M34	RES, 22
R5401	0662057M90	RES, 4.7K
R5480	0662057M80	RES, 1.8K
R5481	0662057V11	RES, 22K
R5482	0662057V43	RES, 330K
R5483	0662057V02	RES, 10K
R5485	0662057M50	RES, 100
R5500	0662057M01	RES, 0
R5501	0662057M92	RES, 5.6K
R5502	0662057M01	RES, 0
R5503	0662057M01	RES, 0
R5603	0662057M78	RES, 1.5K
R5604	0662057N08	RES, 24K
R5605	0662057M96	RES, 8.2K
R5606	0655086C39	RES, 2870
R5607	0662057M80	RES, 1.8K
R5608	0662057M80	RES, 1.8K
R5613	0662057M96	RES, 8.2K

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
R5619	0662057M98	RES, 10K
R5610DNP	0662057M98	RES, 10K
R5623	0662057M98	RES, 10K
R5624	0662057M98	RES, 10K
R5675	0662057N39	RES, 470K
R5683	0662057N47	RES, 1MEG
R6000	0662057V19	RES, 47K
R6001	0609591M45	RESNET, 47K
R6002	0609591M45	RESNET, 47K
R6003	0609591M45	RESNET, 47K
R6004	0609591M45	RESNET, 47K
R6005	0662057N23	RES, 100K
R6006	0662057M01	RES, 0
R6008	0662057M82	RES, 2.2K
R6007DNP	0662057M01	RES, 0
R6010	0662057V32	RES, 150K
R6011	0662057V35	RES, 200K
R6059	0662057M01	RES, 0
R6060	0662057M94	RES, 6.8K
R6061	0662057M01	RES, 0
R6063	0662057M46	RES, 68
R7610	0662057M50	RES, 100
R7611	0662057M50	RES, 100
R7612	0662057M50	RES, 100
R7613	0662057N23	RES, 100K
R7615	0662057M01	RES, 0
R7614DNP	0662057M01	RES, 0
R7616DNP	0662057M01	RES, 0
R7620	0662057M50	RES, 100
R7630	0662057M82	RES, 2.2K
R7631	0662057M82	RES, 2.2K
R7632	0609591M29	RESNET, 2.2K
R7635	0662057M46	RES, 68
R7637	0662057M98	RES, 10K
R7638	0609591M37	RESNET, 10K
R7641	0662057M78	RES, 1.5K
R7642	0662057M92	RES, 5.6K
R7643	0662057M98	RES, 10K
R7644	0662057N23	RES, 100K
R7645	0662057N23	RES, 100K
R7646	0662057N23	RES, 100K
R7654	0662057N39	RES, 470K
R7650DNP	0662057M01	RES, 0
S2070	4085805H02	SWITCH

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number		Description
S5100	4087635K01		SWITCH
S5101	4087635K01		SWITCH
S5102	4087635K01		SWITCH
S5103	4087635K01		SWITCH
SH130	2688976N01		SHIELD
SH140	2687472N03		SHIELD
SH150	2687476N03		SHIELD
SH200	2687475N03		SHIELD
SH310	2687473N03		SHIELD
SH330	2687474N03		SHIELD
SH400	2687471N03		SHIELD
SH500	2688037M01		SHIELD
SH700	2688036M01		SHIELD
SH800	2688035M03		SHIELD
SH1000	2688975N01		SHIELD
SH2000	2688974N02		SHIELD
SH3000	2688727M02		SHIELD
SH5600	2688038M01		SHIELD
SH6000	2688033M01		SHIELD
SH6100	2688031M01		SHIELD
SH6200	2688034M01		SHIELD
SH7600	2688089M02		SHIELD
T100	5887510M01	x	HHM1520
T650	5885949K08	x	HHM1409
T660	5885949K09	x	HHM1410
T670	5885949K05	x	HHM1525
U101	5188450M07	bg	50M07
U130	5187634N01		KM4110
U140	4809283D73		MQL304
U150	5109940K32		UPC8151TB
U200	5109817F71	q	MAX2363
U310	5109944C53	q	MC13770
U330	5109817F69	q	MAX2309
U410	5187970L05	m	AV122
U420	5109908K55		PA2001_5W
U440	5109768D08		LM20
U450	5187970L13		DD02-92
U500	5188450M05		50M05
U510	5109522E63		NC7WZ04
U600	5109940K41	bg	LIFE_30PIN
U6004DNP	5182159Y04		MAX6381
U630	5109512F47		LP3985
U700	4809283D97		83D97
U710	5887694L17		EXB24ATE

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
U800	5109908K74	08K74
U810	5885811G11 q	DD05-EN722
U908	5109522E83	NC7SZ11
U1000	5199134J02 bga1	8 DSPIO
U1110	5109522E53 s	NC7SZ125
U1120	5109522E60	TC7SZ08FU
U1140	5109522E53 s	NC7SZ125
U1150	5162852A59	MAX4599EXT
U1300	5199144J01 b	44J01
U1310	5199144J01 b	44J01
U1400	5109509A55 bg	K4M64163
U2000	5189251L05 bg	OMAP1510
U2020	5109522E60	TC7SZ08FU
U2023	5109522E53 s	NC7SZ125
U2040	5109522E25	TC7SH02FU
U2070	5109522E16	TC7W74FU
U2071	5109522E60	TC7SZ08FU
U2300	5199121J01 bga	5 28F128K18
U2380	5199139J01 bga	5 GE28F256K18
U2400	5109509A45 bga	K4S56163LC
U3000	5188450M06 b	50M06
U3220	5187324N01	LTC3411
U3910	5109512F46	ILC7081
U3911	5164751E01	MC74VHC1GT50
U3980	5187344N01 bga	LP3983
U5000	5109817F58	17F58
U5001	4889526L02 bga	0 CSPEMI-307
U5002	5109522E82 mi	NC7SB3157
U5003	4889526L01 bga	0 CSPEMI-306
U5004	5109522E82 mi	NC7SB3157
U5005	5109522E82 mi	NC7SB3157
U5600	5189316L01	BCM2033A
U5623	5109522E82 mi	NC7SB3157
U5670	5109522E60	TC7SZ08FU
U6000	5109841C70 bga1	30 GSP2E
U6001	5199342A01 bga	GT28F800B
U6002	5186311J23 mi	NC7SZ126
U6003	5186311J23 mi	NC7SZ126
U6010	5109512F46	ILC7081
U6050	5187970L16	GRF2I_LP
U6051	5105739X12	BGA428
U6075	5109522E17	TC7S00FU
U6500	5162852A33 l	HSDL3202
U7600	5189251L01	CX1164621

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Table 10. Electrical Parts List - cont'd

Reference Number	Part Number	Description
U7601	5109817F66	TLE4913
U7602	5109522E16	TC7W74FU
U7603	5109522E82 mi	NC7SB3157
U7605	5186311J23 mi	NC7SZ126
U7640	5109522E16	TC7W74FU
U7701	4889526L01 bga	0 CSPEMI-306
U7702	4889526L01 bga	0 CSPEMI-306
U7703	0662057M50	RES, 100
U7704	2409154M66	IDCTR, 18.0nH
U7705	5109522E82 mi	NC7SB3157
VR800	4809788E17	EDZ68B
VR3912	4809788E17	EDZ68B
VR3914	4809788E17	EDZ68B
VR5500	4809948D44 bg	CSPESD304
VS1001	4809948D44 bg	CSPESD304
VS1002	4809948D44 bg	CSPESD304
VS4200	4809788E06	UDZTE-176.8B
VS4201	4809788E06	UDZTE-176.8B
VS4392	4809788E17	EDZ68B
VS5000	4809788E08	UDZS8_2B
VS5001	4813830C29	MMSZ5246B
VS5002	4809788E06	UDZTE-176.8B
VS5003	4809788E06	UDZTE-176.8B
VS5004	4813830C29	MMSZ5246B
VS5200	4809948D44 bg	CSPESD304
VS5400	4809788E06	UDZTE-176.8B
VS5401	4809788E06	UDZTE-176.8B
VS5402	4809788E06	UDZTE-176.8B
VS7600	4809948D44 bg	CSPESD304
VS7602	4809948D44 bg	CSPESD304
VS7603	4809948D44 bg	CSPESD304
VS7604	4809948D44 bg	CSPESD304
VS7605	4809788E17	EDZ68B
VS7601DNP	4809948D44 bg	CSPESD304
VS7730	4809788E17	EDZ68B
VS7731	4809788E17	EDZ68B
Y130	4809718L14	NT5032SA
Y500	4809612J43	XTAL
Y2000	4809612J45	CX-91F
Y3982	4809995L13	CC5V
Y6050	4885169E03	TX2949

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