AK8999A/AW/AD

Pressure Sensor Control IC

1. Genaral Description

The AK8999A is a piezoresistive semiconductor pressure sensor control IC that compensates temperature drifts and sensor variations. Variations in the sensor can be corrected with compensation values stored in an integrated non-volatile memory (EEPROM).
The primary characteristics and its associated temperature drifts of pressure sensors are corrected with the 1st order coefficient for temperature compensation or the quasi 2nd order coefficient for temperature compensation by piecewise linear approximation (1st order independent coefficients can be set for high and low temperature side on the basis of 25°C) by integrated temperature compensation circuits for offset voltage and span voltage.
The AK8999A integrates two pressure threshold detectors. When a pressure exceeds the detection threshold stored in the EEPROM is applied, the DET1 and the DET2/PTH pins output "H" or "L" (the output polarity is selectable). This output can be used as a control signal of pressure switch applications.
Accessing to the AK8999A is made via the 2-wire serial interface on CSCLK pin and VOUT pin (set as digital I/O mode) for setting functions and storing compensation values.
The AK8999A is available in a 16-pin UQFN package, in wafer form or in a die on a tray.

2. Feartures

- **Pressure sensor compensation and excitation IC (Analog output)**
- **Supply voltage current : 8.5mA max @ 8.33kHz sampling**
- **Supply voltage : 3.0V ± 10%, 3.3V ± 10%, 5.0V ± 10%**
- **Operating temperature range : -40 to 105 °C**
- **Integrated sensor output compensation (AK8999A Input conversion)**
  - **Offset voltage adjustment**
    - **Adjustment range : Coarse ±13 to ±373mV, Fine ±1 to ±34mV @VDD:5.0V**
    - **Adjustment step : Coarse 2 to 53mV /step, Fine 0.01 to 0.27mV /step @ VDD:5.0V**
  - **Offset voltage temperature drift adjustment (1st order or Quasi 2nd order correction by piecewise linear approximation)**
    - **Adjustment range : ±0.04 to ±1.23mV/°C @ VDD:5.0V**
    - **Adjustment step : 0.2 to 4.8µV/°C @ VDD:5.0V**
  - **Output span voltage adjustment (G1, G2, G3)**
    - **Total adjustment range : 3.4 to 261.6mV @ VDD:5.0V**
    - **G1 adjustment step : 0.57 to 74.7mV /step @ VDD:5.0V**
    - **G2 adjustment step : 3.43 to 130.8mV /step @ VDD:5.0V**
    - **G3 adjustment step : 0.01 to 0.40mV /step @ VDD:5.0V**
  - **Sensitivity temperature drift adjustment (1st order or Quasi 2nd order correction by piecewise linear approximation)**
    - **Adjustment range : -4000ppm/ °C to 2500ppm/ °C**
    - **Adjustment step : 18ppm/ °C /step**
- **Integrated output reference voltage adjustment function**
  - **Adjustment range : 0.02*VDD to 0.98*VDD**
  - **Adjustment step : 0.002*VDD /step**
- **Integrated sampling frequency switching function : 0.83kHz, 8.33kHz**
- **Integrated analog circuit reference voltage stabilizer**
- **SCF and SMF included for band limitation : fc = 1.0kHz, 500Hz, 250 Hz**
- **2-wire serial interface (CSCLK, VOUT pin)**
- **Ratiometric voltage output**

- **Integrated constant voltage source for pressure sensor**
  : 2.2V @ VDD:3.0, 3.3V ± 10%, 4.0V or 2.2V @ VDD:5.0V ± 10%
- **Integrated pressure threshold detectors (x2)**
  - **Detection threshold adjustment control**
    - **Adjustment range : 0.125*VDD to 0.9*VDD**
    - **Adjustment step : 0.025*VDD /step**
  - **Detection threshold external setting function (DET2/PTH pin use)**
  - **Hysteresis voltage adjustment control**
    - **Adjustment range : 0.03*VDD to 0.06*VDD**
    - **Adjustment step : 0.01*VDD /step**
- **Integrated reference voltage & reference current generator**
  - **VREF voltage adjustment control**
    - **Resolution : 3bits**
    - **Adjustment step : 1% /step**
  - **VREF current adjustment control**
    - **Resolution : 4bits**
    - **Adjustment step : 2.8% /step typ.**
- **Temperature sensor (internal or external)**
  - **Temperature range : -40 to 105 °C**
  - **Internal temperature sensor output voltage adjustment control**
    - **Resolution : 6 bits**
    - **Adjustment step : 0.2% /step**
  - **External temperature sensor output voltage adjustment control**
    - **Resolution : 9 bits (Coarse=3bits, Fine=6bits)**
    - **Adjustment step : Coarse 10% /step, Fine 0.2% /step**
  - **Integrated external temperature sensor constant current circuit:±50μA typ.**
- **Integrated oscillator for intermittent operation (1000kHz typ.)**
  - **Oscillating frequency adjustment control**
    - **Resolution : 4 bits**
    - **Adjustment step : 5% /step typ.**
- **Integrated EEPROM for compensation values and control data storage**
  - **Size : 135 bits**
  - **Endurance : 1,000 times or more**
  - **Retention time : 10 years or more @Ta: 105°C**
- **Supply Type : Die (Tray), Wafer, PKG (UQFN16)**

Product name	Supply Type	Description
AK8999A	PKG (UQFN16)	
AK8999AW	Wafer	
AK8999AD	Die (Tray)	

3. Table of Contents

4. Adjustment Characteristics

1) Sensor Characteristics

Adjustable characteristics of pressure sensors are shown below.

■VDD: 5V ± 10%, Sensor drive voltage: 4V, Temperature range: -40 to 105°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Description
Sensor resistance	Sres	1.00	4.00	6.50	kΩ	
Voltage input span range	Sspnin1	12.00	44.00	76.00	mV	Sensor1
	Sspnin2	17.00	70.00	125.00	mV	Sensor2
Offset voltage adjustment range	Soff1	-15.00	0.00	15.00	mV	Sensor1
	Soff2	-35.00	0.00	35.00	mV	Sensor2
Sensitivity temp. drift coefficient	Sst1	-4000		2500	ppm/°C	Sensor1
	Sst2	-4000		2500	ppm/°C	Sensor2
Offset temp. drift coefficient	Sot1	-0.040	0.00	0.040	mV/°C	Sensor1
	Sot2	-0.080	0.00	0.080	mV/°C	Sensor2

Note) To combine characteristics of Sensor 1/2 is not allowed. For example, when the characteristic of span voltage is used as Sensor 1, the characteristic of offset voltage can choose only Sensor 1.

■VDD: 3V ± 10%, 3.3V ± 10%, 5V ± 10%, Sensor drive voltage: 2.2V, Temperature range: -40 to 105°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Description
Sensor resistance	Sres	0.82	4.00	6.50	kΩ	
Voltage input span range	Sspnin1	6.60	24.20	41.80	mV	Sensor1
	Sspnin2	9.00	40.00	70.00	mV	Sensor2
Offset voltage adjustment range	Soff1	-8.25	0.00	8.25	mV	Sensor1
	Soff2	-19.25	0.00	19.25	mV	Sensor2
Sensitivity temp. drift coefficient	Sst1	-4000		2500	ppm/°C	Sensor1
	Sst2	-4000		2500	ppm/°C	Sensor2
Offset temp. drift coefficient	Sot1	-0.022	0.00	0.022	mV/°C	Sensor1
	Sot2	-0.044	0.00	0.044	mV/°C	Sensor2

Note) To combine characteristics of Sensor 1/2 is not allowed. For example, when the characteristic of span voltage is used as Sensor 1, the characteristic of offset voltage can choose only Sensor 1.

2) Adjustment Accuracy
Adjustment accuracy targets are shown below.

2.1) The case of 1st order adjustment

Parameter	Symbol	Min.	Typ. Note4)	Max. Note5)	Units	Description
Offset adjustment accuracy	Cof		0.083		%FS	
Offset temp. drift adjustment accuracy	Coft		0.120		%FS	
Output span adjustment accuracy	Csn		0.146		%FS	
Sensitivity temp. adjustment accuracy	Csnt		0.114		%FS	
Sensitivity supply voltage and temp. variation step	Cstv		0.057		%FS	
Sample and hold circuit output error	Cshe		0.0		%FS	
Offset adjustment accuracy Note1)	Cofall		0.146	1.0	%FS	
Span adjustment accuracy Note2)	Csnall		0.194	1.0	%FS	
Offset adjustment accuracy Note3)	Call		0.194	1.0	%FS	

Note1) Cofall = (Cof^2+Coft^2)^(1/2)
Note2) Csnall = (Csn^2+Csnt^2+Cstv^2+Cshe^2)^(1/2)
Note3) Call = max(Cofall,Csnall)
Note4) Temp. = 25ºC, VDD = 5V, G1 = 10x, G2 = 1.5x, G3 = 1.8x, Offset temp. drift 1st order coefficient = Min. or Max., Sensitivity temp. drift 1st order coefficient = Min., VOUT output band-limited effective (≤ 500Hz@Fs = 8.33kHz, ≤ 50Hz@Fs = 0.83kHz)
Note5) Temp. = -40 to 105ºC, VDD = 5V ± 10%, 3.3V ± 10%, 3.0V ± 10%, G1/G2/G3 = Min. to Max., Each temp. coefficient = Min. to Max., VOUT output band-limited effective (≤ 500Hz@Fs = 8.33kHz, ≤ 50Hz@Fs = 0.83kHz)

2.2) The case of quasi 2nd order adjustment by piecewise linear approximation

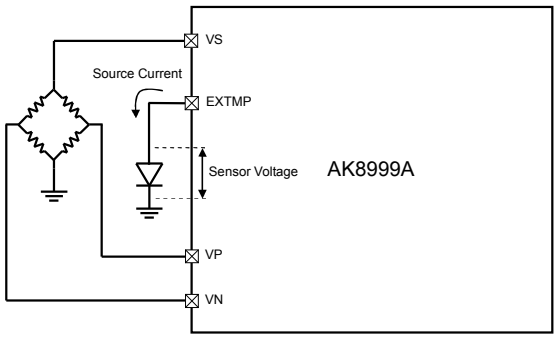
Parameter	Symbol	Min.	Typ. Note9)	Max. Note10)	Units	Description
Offset adjustment accuracy	Cof		0.083		%FS	
Offset temp. drift adjustment accuracy	Coft		0.120		%FS	
Offset temp. drift adjustment switching accuracy using the piecewise linear approximation method	Coftc		0.0		%FS	
Output span adjustment accuracy	Csn		0.146		%FS	
Sensitivity temp. adjustment accuracy	Csnt		0.114		%FS	
Sensitivity temp. adjustment switching accuracy using the piecewise linear approximation method	Csntc		0.0		%FS	
Sensitivity supply voltage and temp. variation step	Cstv		0.057		%FS	
Sample and hold circuit output error	Cshe		0.0		%FS	
Offset adjustment accuracy Note6)	Cofall		0.146	1.0	%FS	
Span adjustment accuracy Note7)	Csnall		0.194	1.0	%FS	
Offset adjustment accuracy Note8)	Call		0.194	1.0	%FS	

Note6) Cofall = (Cof^2+Coft^2)^(1/2)
Note7) Csnall = (Csn^2+Csnt^2+Cstv^2+Cshe^2)^(1/2)
Note8) Call = max(Cofall,Csnall)
Note9) Temp. = 25ºC, VDD = 5V, G1 = 10x, G2 = 1.5x, G3 = 1.8x, Offset temp. drift 1st order coefficient = Min. or Max., Sensitivity temp. drift 1st order coefficient = Min., VOUT output band-limited effective (≤ 500Hz@Fs = 8.33kHz, ≤50Hz@Fs=0.83kHz)
Note10) Temp. = -40 to 105ºC, VDD = 5V ± 10%, 3.3V ± 10%, 3.0V ± 10%, G1/G2/G3 = Min. to Max., Each temp. coefficient = Min. to Max., VOUT output band-limited effective (≤ 500Hz@Fs = 8.33kHz, ≤ 50Hz@Fs = 0.83kHz)
* The adjustment accuracy is based on our definition. Please be careful the accuracy of product depends on the sensor characteristics and adjustment method.

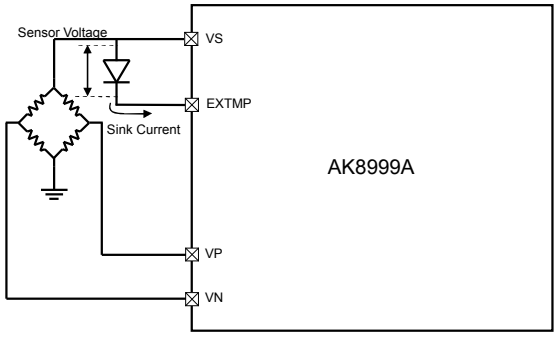
3) External Temperature Sensor Characteristics
The characteristics of an external temperature sensor are shown below.

Parameter	Symbol	Min.	Typ.	Max.	Units	Description
Sensor drive current (sink)	Tsdi		-50		µA	
Sensor drive current (source)	Tsdo		+50		µA	
Sensor temp. variation	Tss	-2.4	-2.2	-2.0	mV/°C	50µA current drive
Sensor voltage @25°C	Tsv25	550	600	650	mV	50µA current drive

4) Connection of Pressure Sensor and External Temperature Sensor
The recommended connection examples of a pressure sensor and an external temperature sensor (Source or Sink current drive) are shown below.

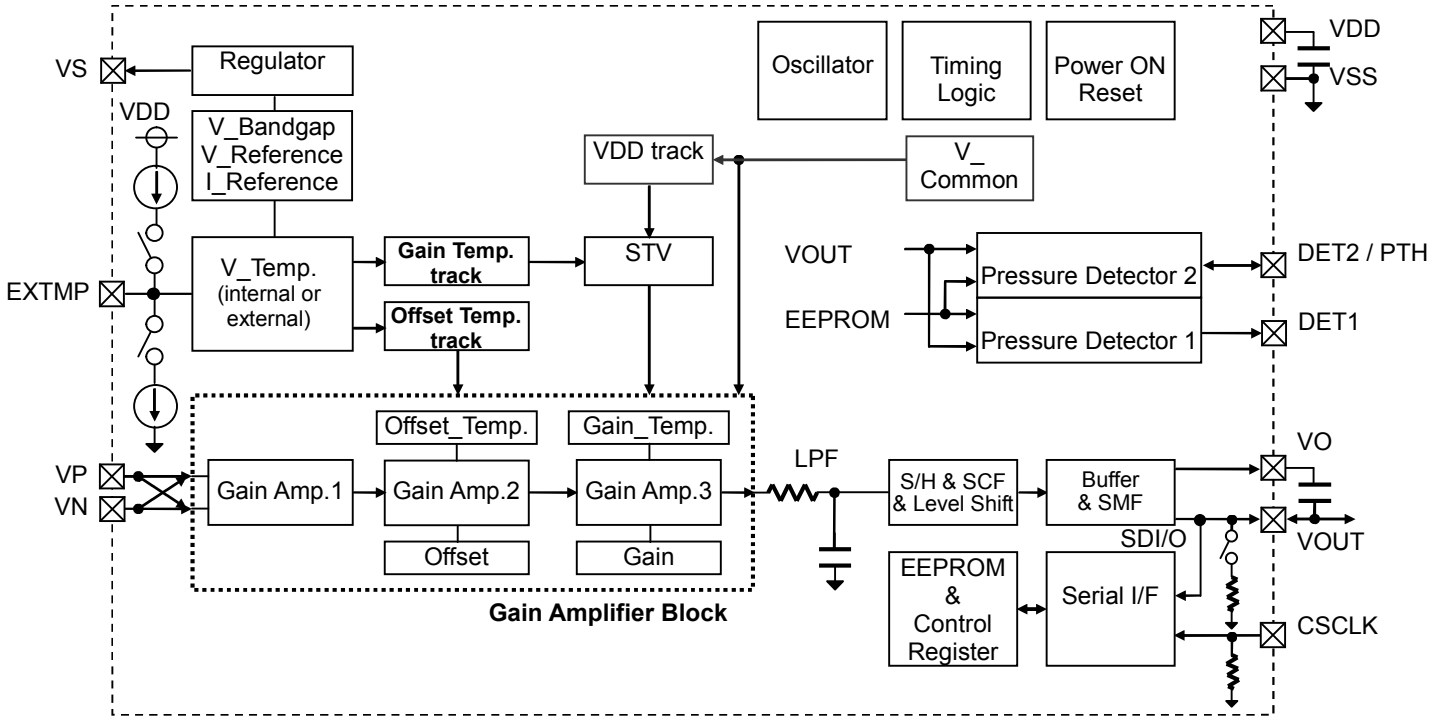


Sensor drive source current



Sensor drive sink current

5. Block Diagram and Functions



Gain Amplifier Block, LPF, S/H&SCF& Level shifter, Buffer & SMF

The set of these blocks amplifies, compensates and outputs the pressure sensor signal.

The circuits from Gain Amplifier to S/H amplify, compensate, sample and hold the pressure sensor output by time sharing. The output stage, with an internal resistor of 146kΩ, band-limited with an external capacitor on VO pin, can provide a low impedance output via buffer. By enabling SCF and SMF, band limit can be done, eliminating the need for the external capacitors. The output reference voltage can be set with an integrated level shifter. Percentage indications define a 4800mVdc output as 100%, which is 60times magnified level of 80mVdc differential input.

Block	Functions		
Gain Amp. 1/2/3 Gain (G1/2/3)	Gain Amp.1 is a low-noise high-gain amplifier at the front. The differential signal is amplified by a factor of 10x typ. (5x to 70x). Gain Amp.2 converts the G1 differential output to single-ended with reference to 0.5*VDD and amplifies by a factor of 1.5x typ. (or 3.0x). Gain Amp.3 amplifies by a factor of 1.8x typ. (or 3.0x). Span voltage is adjusted with G1/2/3 Gain (G1/2: coarse adjustment, G3: fine adjustment).		
Offset_Temp. Offset Offset Temp. track (G2)	The pressure sensor offset voltage and offset temperature drift are compensated by using the preloaded compensation data in the EEPROM. The following value is converted into the input value at @5.0V.		
	Offset adj.	Adj. range	Coarse: ±13 to ±373mV Fine: ±1 to ±34mV
		Adj. step	Coarse: 2 to 53mV /step Fine: 0.01 to 0.27mV /step
	Offset temp. drift. adj.	Adj. range	±0.04 to ±1.23mV/ ºC
		Adj. step	0.2 to 4.8µV/ºC step

Block	Functions
STV VDD track Gain_Temp. (STV)	Supply voltage and sensitivity temperature variation compensation circuit. The pressure sensor sensitivity temperature drift and the supply voltage variation are compensated by using the magnitude of supply voltage variation and the preloaded compensation data in the EEPROM. Sensitivity temp. drift. adj. Adj. range -4000ppm/ ºC to +2500ppm/ ºC Adj. step 18ppm/ ºC step
LPF	Anti-aliasing filter to eliminate the aliasing noise generated in the next sample and hold circuit (S/H). The cutoff frequency is fc=60kHz.
S/H & Level Shift & SCF	S/H doubles the LPF output and samples and holds it. The output reference voltage can be changed. Output reference voltage adj. Adj. range 0.02*VDD to 0.98*VD Adj. step 0.002*VDD /step SCF is a low-pass filter without using the external capacitors. The cutoff frequency (fc: 1kHz /500Hz /250Hz) of the filter can be set by EEPROM.
Buffer & SMF	Buffer to provide 1.111x output and produce a band limited output with low impedance. 146kΩ internal resistance and an external capacitor (C) make the LPF characteristics. Change the external capacitance value according to the desired signal band for detection using the following equation: fc=1/(2*π* 146kΩ*C) (Hz) SMF is a low-pass filter (fc=10kHz) for eliminating the clock noise generated by the previous SCF. SMF is switched on or off in combination with the previous stage SCF using the EEPROM data.
Timing Logic	Generates timing sync signals for internal operation and sampling frequencies for sensor output signals. Sampling frequency (fs): 0.83kHz or 8.33kHz
Regulator	Constant voltage generator to drive the sensor. The drive voltage can be selected from the EEPROM depending on the supply voltage being used. Drive voltage: 2.2V@VDD:3, 3.3V ± 10%, 4.0/2.2V@VDD:5V ± 10%
Pressure Threshold Detector1/2	Two sets of pressure threshold detectors. The pressure threshold detection range can be individually selected depending on the EEPROM data. • Pressure above a certain value is detected • Pressure below a certain value is detected The DET1 and DET2/PTH pins go high when the detected pressure exceeds the threshold (the polarity change by EEPROM is possible). The detection threshold can be set by the input of DET2/PTH pin (in this case, Pressure Threshold Detector 2 cannot use) or using the EEPROM data. The hysteresis voltage can be adjusted at 2 bits, and it varies ratiometrically with respect to the supply voltage as well as the detection threshold. Note) The exact pressure determination cannot be achieved until the VOUT pin output is stabilized after power-up.

Reference Section & Others

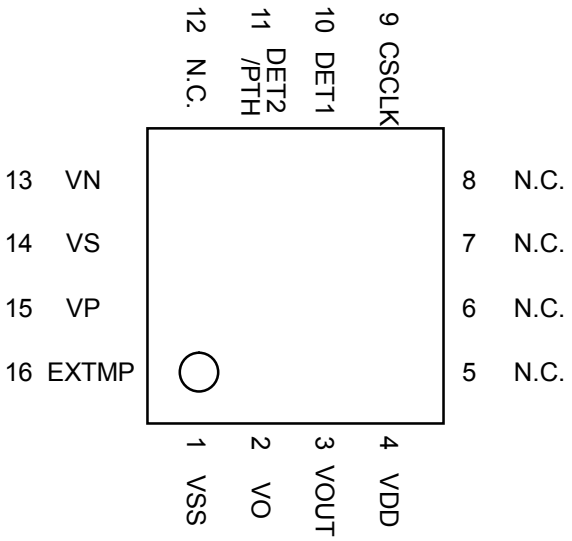
Block	Functions
V_Bandgap (VBG) V_Reference (VREF) I_Reference (IREF)	Generates the reference voltage or bias current required for each circuit. The VREF voltage is adjusted to 1.0V. VREF voltage adj. Resolution 3bits Adj. step 1% / step IREF current is adjusted to 1.0V, in state of connecting 1MΩ external resistor to VOUT pin. IREF current adj. Resolution 4bits Adj. step 2.8% / step
Oscillator (OSC)	Oscillator to generate timing sync signals for internal operation and sampling frequencies. Oscillation frequency is adjusted as the counter result reaches the expected value, the internal counter counts for the period of CSCLK is high (2msec typ.). For the detail, refer to the Functional Descriptions **1) Adjustment Procedure Description (Example)**. OSC adj. Resolution 4bits Adj. step 5% / step
V_temp. (VTMP)	Temperature sensor converting the ambient temperature to voltage. Adjust the temperature sensor output voltage so that it is equal to VREF voltage at 25ºC.And it is also possible to select the external temperature sensor by EEPROM in the case where a pressure sensor and the AK8999A are separated physically. When the external temperature sensor is chosen, it is driven by 50uA constant current which is sunk or sourced from the EXTMP pin. VTMP voltage adj.(internal) Resolution 6bits Adj. step 0.2% / step VTMP voltage adj.(external) Resolution 9bits (Coarse /Fine=3/6bits) Adj. step Coarse 10% /step / Fine 0.2% /step
V_Common (VCOM)	Generates analog circuit reference voltage 0.5*VDD. The internal power-up circuit causes it to start up within the settling time for stable analog operation.
Power ON Reset(POR)	Power Up circuit is for stable analog operation upon power-up. In order to make the power-on reset effective, be sure to power up the supply voltage from below 0.1*VDD.
Serial I/F	Serial interface for accessing EEPROM and control register (volatile memory). It accesses using the CSCLK pin and the VOUT pin.
EEPROM & Control Register	EEPROM and control register (volatile memory). Used to store compensation values and measurement modes and to set up the measurement modes for adjustment.

6. Pin Configurations

1) Wafer Configuration

For the detail, please contact your local sales office or authorized distributor.

2) Package Outline (UQFN16)



7. Pin conditions

PAD	Name	I/O	C load max.	R load min.	Type	Description
1	VSS				GND	
2	VO	I			Analog	Resistive load connection prohibited ESCF[1:0]: Open when 1,2,3h
3	VOUT	O	50pF	9.5kΩ	Analog	Resistance load is connectable with VDD or VSS
		I/O	100pF		CMOS	Pull-down resistor (100kΩ) included when SDI/O mode
		O	300pF	1MΩ typ.	Analog	Adjustment mode
4	VDD				Power	
5-8	N.C.					Do not connect
9	CSCLK	I			CMOS	Pull-down resistor (100kΩ) included
10	DET1	O			CMOS	
11	DET2 /PTH	O			CMOS	
		I			Analog	EPTH1[0] = 1h
12	N.C.					Do not connect
13	VN	I			Analog	
14	VS	O	30pF	1kΩ	Analog	EVD[1:0] = 3h Pull-down resistor (200kΩ) included
		O	30pF	0.82kΩ	Analog	EVD[1:0] = 0, 1, 2h Pull-down resistor (200kΩ) included
15	VP	I			Analog	
16	EXTMP	I	400pF		Analog	Do not connect when not in use

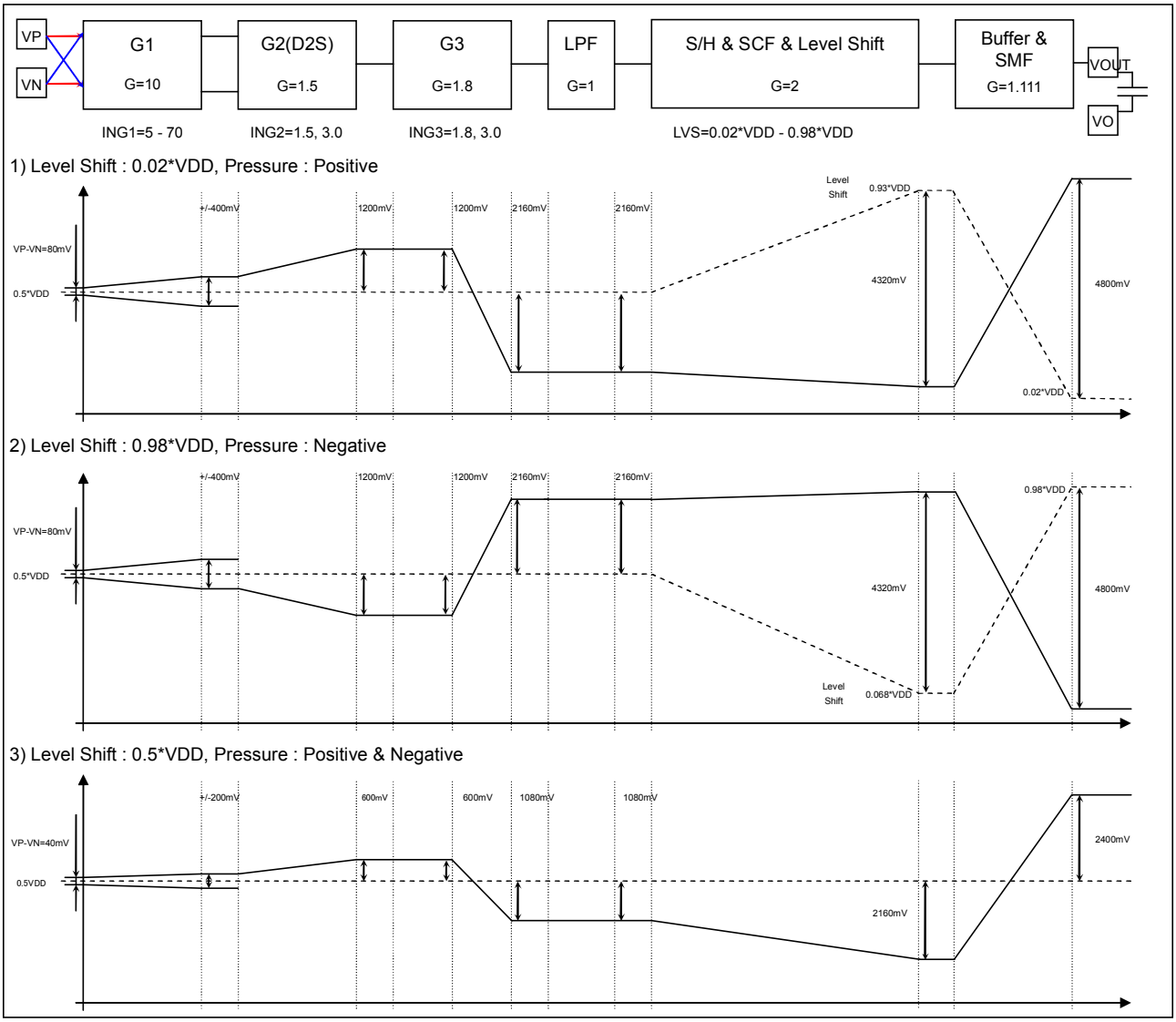
8. Pin Assignments and Functions

PAD	Name	Functions	Pin conditions Start up Note1)	Pin conditions EINV1,2[0] : "0h" / "1h"	Pin conditions EINE1,2[0] : "1h"
1	VSS	Negative voltage supply pin	-	-	-
2	VO	Capacitance connection pin for sensor signal band-limiting	VSS/ VDD/ 0.5*VDD	Normal operation	Normal operation
3	VOUT	Sensor signal / Data I/O / Calibration interface pin	VSS/ VDD/ 0.5*VDD	Normal operation	Normal operation
4	VDD	Positive supply voltage pin	-	-	-
5-8	N.C.		-	-	-
9	CSCLK	Chip select / Serial clock pin	-	-	-
10	DET1	Output pin for pressure threshold detection 1	VSS/VDD	VDD/VSS	VSS
11	DET2 /PTH	Output pin for pressure threshold detection 2 / Pressure threshold detector 1 threshold external input			
12	N.C.		-	-	-
13	VN	Sensor differential signal input pin (-)	-	-	-
14	VS	Constant voltage supply pin for sensor drive	VSS	Normal operation	Normal operation
15	VP	Sensor differential signal input pin (+)	-	-	-
16	EXTMP	External temperature sensor voltage input pin	Hi-z	-	-

Note1) VOUT and VO pin: In the case of EVOUT[1:0] = 0h, 1h, 2h
DET1 and DET2/PTH pin: In the case of EINV1/2[0] = 0h, 1h

9. Level Diagram

VDD: 5V



10. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Description
Supply voltage	VDD	-0.3	6.5	V	
Input voltage	VDIN	VSS - 0.3	VDD + 0.3	V	
Input current	IIN	-10	10	mA	
Output current	IOUT	-10	10	mA	
Storage temp.	TST	-55	125	°C	EEPROM retention characteristics ≤105°C

Note) Operation at or beyond these limits may result in permanent damage to the device.

11. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Description
Operating temp.	Ta	-40		105	°C	
Supply voltage	VDD1	2.7	3.0	3.3	V	EVD[1:0] = 0h
	VDD2	2.97	3.3	3.63	V	EVD[1:0] = 1h
	VDD3	4.5	5.0	5.5	V	EVD[1:0] = 2h, 3h

12. Electrical Characteristics

1) Supply Voltage Current (Refer to Functional Descriptions)

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Description
Supply voltage current 1	IDD1		6900	8500	μA	VDD = 5V ± 10%, VS = 4V, Fs = 8.33kHz, Note1)
Supply voltage current 2	IDD2		4900	6200	μA	VDD = 3V ± 10%, VS = 2.2V, Fs = 8.33kHz, Note1)
Supply voltage current 3	IDD3		1700	2400	μA	VDD = 5V ± 10%, VS = 4V, Fs = 0.83kHz, Note1)
Supply voltage current 4	IDD4		1300	2000	μA	VDD = 3V ± 10%, VS = 2.2V, Fs = 0.83kHz, Note1)
Supply voltage current 5 (SCF & SMF circuit)	IDD5		100	150	μA	VDD = 5V ± 10%, ESCF[1:0] = 1h
Supply voltage current 6 (Pressure threshold detector 1/2)	IDD6		150	250	μA	VDD = 5V ± 10%
Supply voltage current 7 (External temperature sensor drive circuit)	IDD7		150	250	μA	VDD = 5V ± 10%

Note) At the time of measurement, the VS pin connects 1kΩ load, the VOUT pin is connects no load, and the VP and VN pins supply 0.5*VS. VREF volgtage, VTMP voltage, IREF current and OSC frequency are complete with adjustment.

Note1) SCF&SMFcircuit: Off, External temperature sensor drive circuit: Off

2) EEPROM Characteristics

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units
EEPROM write temp.	Eta	-40		85	°C
EEPROM endurance	Etime	1000			Times
EEPROM data retention time(@105 ºC)	Ehold	10			Years

3) Digital DC Characteristics

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise noted

Parameter	Symbol	Pin	Conditions	Min.	Typ.	Max.	Units
High level input voltage	VIH	Note1)		0.7*VDD	-	-	V
Low level input voltage	VIL	Note1)		-	-	0.3*VDD	V
High level input current	IIH	Note1)		+10	-	+200	µA
Low level input current 1	IIL1	Note2)		-10	-	+10	µA
Low level input current 2	IIL2	Note3)		-50	-	+50	µA
High level output voltage	VOH	Note4)	IOH = -200µA	0.9*VDD	-	-	V
Low level output voltage	VOL	Note4)	IOL = +200µA	-	-	0.1*VDD	V

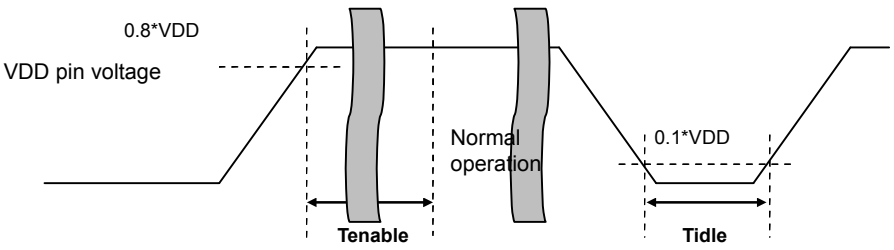
Note1) CSCLK (integrated 100kΩ pull-down resistor),
VOUT (integrated 100kΩ pull-down resistor when SDI/O mode)
Note2) CSCLK (integrated 100kΩ pull-down resistor)
Note3) VOUT (integrated 100kΩ pull-down resistor when SDI/O mode)
Note4) VOUT (when SDI/O mode), DET1, DET2/PTH

4) Power On/Off time and Analog circuit settling time for stable operation

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Description
Power On/Off time	Tidle	1			msec	VDD pin voltage <0.1*VDD
Settling time for stable analog operation	Tenable			700	µsec	Power On time (0.1*VDD to 0.8*VDD) 2msec >

Note) Design reference value; no production test performed.



5) Digital AC Characteristics

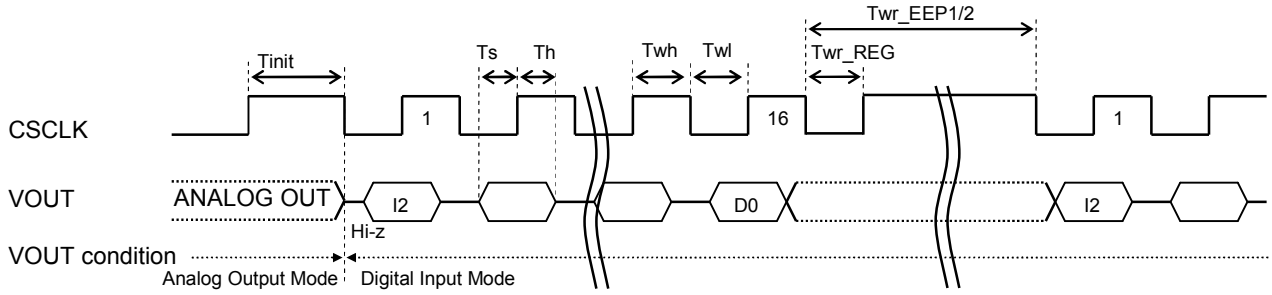
VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units
Write time (EEPROM address write)	Twr_EEP1	5		100	msec
Write time (EEPROM batch write)	Twr_EEP2	10		100	msec
Write time (Register)	Twr_REG	10			µsec
Digital Mode Transition time	Tinit	1.0			msec
Analog Mode Transition time	Tdigout	0.5			msec
Data setup time	Ts	100			msec
Data hold time	Th	100			msec
CSCLK high time	Twh	0.5		100	µsec
CSCLK low time	Twl	0.5		100	µsec
CSCLK→DO delay time Note1)	Td			200	nsec
CSCLK rising time Note 2)	Tr			10	nsec
CSCLK falling time Note 2)	Tf			10	nsec

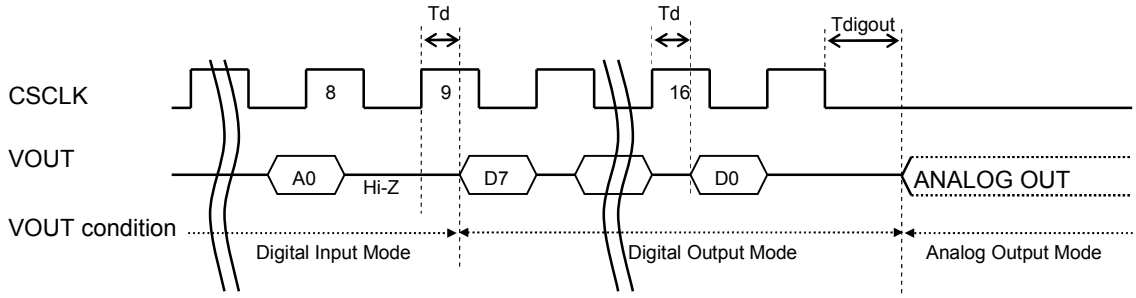
Note1) SDO load capacitance = 100pF

Note2) Design reference value; no production test performed.

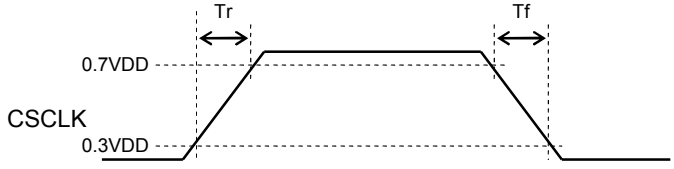
[Serial I/F timing (Write)]



[Serial I/F timing (Read)]



[CSCLK Raising/Falling timing]

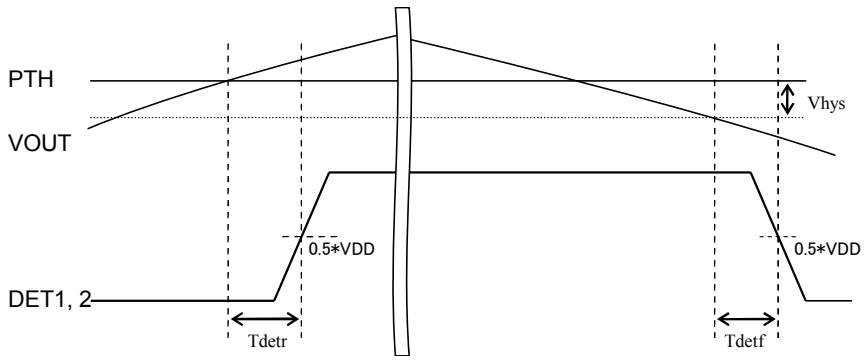


6) Pressure Threshold Detector 1 & 2

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Pressure detection threshold External input range	Vdete	EINE1[0] = 0h EINE2[0] = 1h EPTH1[0] = 1h	0.1*VDD		0.9*VDD	V	
Pressure detection threshold Internal set value	Vdet	EPT1, 2[4:0] = 00h	0.500 *VDD -0.05	0.500 *VDD	0.500 *VDD +0.05	V	
Pressure detection threshold Internal set value Adjust. width	Vdet+	Max EPT1, 2[4:0] = 10h		0.900 *VDD		V	
	Vdet-	Min EPT1, 2[4:0] = 0Fh		0.125 *VDD		V	
Adjust. step	Vdstp			0.025 *VDD		V	
Hysteresis voltage Adjust. width	Vhys5+	Max VDD = 5V ± 10% EHYS1, 2[1:0] = 1h	0.060 *VDD -0.055	0.060 *VDD	0.060 *VDD +0.055	V	
	Vhys5-	Min VDD = 5V ± 10% EHYS1, 2[1:0] = 2h	0.030 *VDD -0.03	0.030 *VDD	0.030 *VDD +0.03	V	
	Vhys3+	Max VDD = 3, 3.3V ± 10% EHYS1, 2[1:0] = 1h	0.060 *VDD -0.035	0.060 *VDD	0.060 *VDD +0.035	V	
	Vhys3-	Min VDD = 3, 3.3V ± 10% EHYS1, 2[1:0] = 2h	0.030 *VDD -0.02	0.030 *VDD	0.030 *VDD +0.02	V	
Adjust. step	Vhysst			0.010 *VDD		V	
Pressure detection time	Tdetr	ESCF[1:0] = 0h			180	µsec	Note1)
Pressure non-detection time	Tdetf	ESCF[1:0] = 0h			180	µsec	Note1)

Note1) Design reference value; no production test performed.



7) Analog Characteristics

7.1) Reference Section

7.1.1) Reference Section Characteristics

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
VREF voltage	Vr0	AM[3:0] = 1h VOUT out	0.97	1.0	1.04	V	@25 ºC Unadjusted
VREF adj. width	Vr+	Max EVR[2:0] = 3h		+30		mV	With respect to Vr0
	Vr-	Min EVR[2:0] = 4h		-40		mV	With respect to Vr0
VREF adj. step	Vrstp			10		mV	
VS voltage	VS4	After VREF adj. Load resistance 1kΩ VS pin out	3.88	4.00	4.12	V	
	VS2	After VREF adj. Load resistance 0.82kΩ VS pin out	2.134	2.20	2.266	V	
IREF current	Ir0	AM[3:0] = 2h VOUT out	0.8	1.00	1.2	µA	@25 ºC Unadjusted
IREF adj. width	Ir+	Max EIR[3:0] = 7h		0.24		µA	With respect to Ir0
	Ir-	Min EIR[3:0] = 8h		-0.17		µA	With respect to Ir0
IREF adj. step	Irstp			0.028		µA	
OSC freq.	Fr0	AM[3:0] = 3h VOUT out	0.750	1.000	1.250	MHz	@25 ºC Unadjusted
OSC adj. width	Fr+	Max EFR[3:0] = 7h		384		kHz	With respect to Fr0
	Fr-	Min EFR[3:0] = Bh		-251		kHz	With respect to Fr0
OSC adj. step	Frstp			50		kHz	
VTMP voltage	Vt0	ETMP[1:0] = 2h AM[3:0] = 4h VOUT output	0.936	1.0	1.062	V	@25 ºC Unadjusted
	Vt0-	ETMP[1:0] = 0h AM[3:0] = 4h VOUT output	0.900	1.0	1.100		@25 ºC Unadjusted
	Vt0+	ETMP[1:0] = 1h AM[3:0] = 4h VOUT output	0.930	1.03	1.130		@25 ºC Unadjusted
VTMP adj. width (Coarse)	Vtr+	Max ETMP[1:0] = 0, 1h ETM[8:6] = 6h		+200		mV	With respect to Vt0
	Vtr-	Min ETMP[1:0] = 0, 1h ETM[8:6] = 2h		-200		mV	With respect to Vt0
Coarse adj. step	Vtrstp	ETMP[1:0] = 0, 1h		100		mV	
VTMP adj. width (fine)	Vtf+	Max ETM[5:0] = 20h		+64		mV	With respect to Vt0
	Vtf-	Min ETM[5:0] = 1Fh		-62		mV	With respect to Vt0
Fine adj. step	Vtfstp			2.0		mV	
VTMP temp variation	Vt	ETMP[1:0] = 2h		4.6		mV/°C	Note1)

Note1) Design reference value; no production test performed.

7.1.2) Reference Section (packaged version only) Characteristics

VDD = 5V ± 10%, Ta = -40 to 105ºC, unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
VREF voltage	Vr0P		0.99	1.0	1.01	V	@25 ºC After adj.
VS voltage	VS4P	Load resistance 1kΩ	3.88	4.00	4.12	V	@25 ºC After adj.
	VS2P	Load resistance 0.82kΩ	2.134	2.20	2.266	V	@25 ºC After adj.
IREF current	Ir0P		0.9	1.0	1.1	µA	@25 ºC After adj.
OSC freq.	Fr0P		0.9	1.0	1.1	MHz	@25 ºC After adj.
VTMP voltage	Vt0P	ETMP[1:0]=2h	0.994	1.0	1.006	V	@25 ºC After adj.

Note) AK8999A is shipped with adjustment at VDD=5V&VS=4V (EVD[1:0]=3h) and internal temperature sensor use (ETMP[1:0]=2h). If VDD=5V&VS=2.2V (EVD[1:0]=1h), VDD=3.3V&VS=2.2V(EVD[1:0]=2h), VDD=3V&VS=2.2V(EVD[1:0]=3h) and external temperature sensor use (ETMP[1:0]=0, 1h) are the actual operating condition, readjustment is required

7.2) Gain Amplifier etc.

Unless otherwise specified, the following requirements apply.

- Reference Section is complete with adjustment.
- For supply voltage of 5V (3V), sensor drive voltage of 4V (2.2V), total gain of 60x (the level diagram includes G1 gain of 10x, G2 gain of 1.5x and G3 gain of 1.8x) and Level shift 0.02*VDD, the output voltage 4800mV (2400mV) is set as 100% based on a differential input of 80mV (40mV).

7.2.1) Overall Characteristics

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Std. gain	Gtyp	VP/VN→VOUT		60		times	
Input common voltage	Vicom		0.45VS	0.5*VS	0.55VS	V	
Output common voltage	Vcom0	VP/VN→VOUT VP = VN = 0.5*VS		0.5*VDD		V	
Max. output range	Vmax+	VP/VN→VOUT VP-VN = VSS or VDD	0.98 *VDD			V	
	Vmax-				0.02 *VDD	V	

7.2.2) Noise Characteristics

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

Parameter	Symbol	Conditions	Min.	Typ. note1)	Max. note2)	Units	Description
Noise	Nout1	VP/VN→VOUT External feedback capacitance 2.2nF ESCR[0]=1h		230	530	µVrms	@1Hz - 100kHz
	Nout2	VP/VN→VOUT ESCF[1:0]=1h ESCR[0]=1h		250	550	µVrms	@1Hz - 100kHz

note1) VDD = 5V, Temp. = 25°C, Total gain: 60x (G1 gain: 10x, G2 gain: 1.5x, G3 gain: 1.8x, S/H gain: 2x, Buffer gain: 1.111x), Output reference voltage = 0.02*VDD, Sampling frequency = 8.33kHz, Sensor drive voltage=4V, Internal temperature sensor use, Offset Voltage = 0mV, Offset temp. drift 1st order coefficient = 0mV/°C, Span Voltage = 80mV, Sensitivity temp. drift 1st order coefficient = 0ppm/°C. Design reference value; no production test performed.

note2) Total gain: 60x@25°C (G1 gain: 10x, G2 gain: 1.5x, G3 gain: 1.8x, S/H gain: 2x, Buffer gain: 1.111x), Output reference voltage = 0.02*VDD, Sampling frequency = 8.33kHz, Internal temperature sensor use, Sensor drive voltage=4V(VDD=5V±10%)/2.2V(VDD=3V, 3.3V±10%), Offset Voltage@25°C = ±35mV(VS = 4V)/±19.25mV(VS = 2.2V), Offset temp. drift 1st order coefficient = ±0.08mV/°C (VS = 4V)/±0.044mV/°C (VS = 2.2V), Span Voltage @25°C = 0 to 80mV(VS = 4V) / 0 to 40mV(VS = 2.2V), Sensitivity temp. drift 1st order coefficient = -4000 to +2500ppm/°C. Design reference value; no production test performed.

7.2.3) G1/2 Gain Adjustment Circuit

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Measurement in test mode							
Unadjusted G1/2 output voltage	Vg1	VP-VN = 80mV VDD = 5V ± 10%	1150	1200	1250	mV	
	Vg2	VP-VN = 40mV VDD = 3, 3.3 ± 10%	550	600	650	mV	
G1 adjustment range	G1sc+	EIG[3:0] = Ch		5		times	
	G1sc-	EIG[3:0] = 0h		70		times	
Adj. Step	G1stp			2,3,5,10		times	
G2	G2sc1+	EIG[4] = 0h		3		times	
	G2sc1-	EIG[4] = 1h		1.5		times	

7.2.4) Offset Voltage Adjustment Circuit

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Measurement in test mode							
Unadjusted output voltage	Vo01	VDD = 3, 3.3, 5V ± 10%	0.5*VDD -0.15	0.5*VDD	0.5*VDD +0.15	V	
Offset coarse adj. DAC adj. range	Ocr5+	EOCR[3] = 0h EOCR[2:0] = 7h VDD = 5V ± 10%		+11200		mV	
	Ocr5-	EOCR[3] = 1h EOCR[2:0] = 7h VDD = 5V ± 10%		-11200		mV	
	Ocr3+	EOCR[3] = 0h EOCR[2:0] = 7h VDD = 3, 3.3 ± 10%		+5600		mV	
	Ocr3-	EOCR[3] = 1h EOCR[2:0] = 7h VDD = 3, 3.3 ± 10%		-5600		mV	
Adj. step	Ocr5stp	VDD = 5V ± 10%		1600		mV	
	Ocr3stp	VDD = 3, 3.3 ± 10%		800		mV	
Offset fine adj. DAC adj. range	Ocf5+	EOCF[7] = 0h EOCF[6:0] = 3Fh VDD = 5V ± 10%		+1016		mV	
	Ocf5-	EOCF[7] = 1h EOCF[6:0] = 3Fh VDD = 5V ± 10%		-1016		mV	
	Ocf3+	EOCF[7] = 0h EOCF[6:0] = 3Fh VDD = 3, 3.3 ± 10%		+508		mV	
	Ocf3-	EOCF[7] = 1h EOCF[6:0] = 3Fh VDD = 3, 3.3 ± 10%		-508		mV	
Adj. step	Ocf5stp	VDD = 5V ± 10%		8		mV	
	Ocf3stp	VDD = 3, 3.3 ± 10%		4		mV	

Note) The case of ESCR[0] = 1h.

7.2.5) Span Voltage Adjustment Circuit

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Measurement in test mode after offset voltage adjustment							
Unadjusted Span voltage	Vs01a	VP-VN = 80mV VDD = 5V ESCR[0] = 1h	1910	2160	2410	mV	
	Vs01b	VP-VN = 80mV VDD = 5V	1590	1800	2010	mV	
	Vs02a	VP-VN = 40mV VDD = 3, 3.3V ESCR[0] = 1h	930	1080	1230	mV	
	Vs02b	VP-VN = 40mV VDD = 3, 3.3V	770	900	1030	mV	
Span adj. range	Sc1+	ESC[7:0] = 00h ESCR[0] = 1h		1.80		times	
	Sc1-	ESC[7:0] = FFh ESCR[0] = 1h		1.10		times	
	Sc2+	ESC[7:0] = 00h ESCR[0] = 0h		3.00		times	
	Sc2-	ESC[7:0] = FFh ESCR[0] = 0h		1.56		times	
Adj. Step	Sc stp1	N = 0 - +255 ESCR[0] = 1h		(275-0.2*N) /(153+0.2*N)		times	
	Sc stp2	N = 0 - +255 ESCR[0] = 0h		(275-0.2*N) /(91+0.2*N)		times	

7.2.6) Offset Temperature Drift & Sensitivity Temperature Drift Adjustment Circuit

7.2.6.1) Offset Temperature Drift Adjustment Circuit

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. Adj. range	DO5+	EOTP,N[8] = 0h EOTP,N[7:0] = FFh VDD = 5V ± 10%		+36.8		mV/°C	
	DO5-	EOTP,N[8] = 1h EOTP,N [7:0] = FFh VDD = 5V ± 10%		-36.8		mV/°C	
	DO3+	EOTP,N[8] = 0h EOTP,N[7:0] = FFh VDD = 3, 3.3 ± 10%		+18.4		mV/°C	
	DO3-	EOTP,N[8] = 1h EOTP,N[7:0] = FFh VDD = 3, 3.3 ± 10%		-18.4		mV/°C	
Adj. step	DO5 stp	VDD = 5V ± 10%		0.144		mV/°C	
	DO3 stp	VDD = 3, 3.3 ± 10%		0.072		mV/°C	

Note) Design reference value; no production test performed. The case of ESCR[0] = 1h.

7.2.6.2) Sensitivity Temperature Drift Adjustment Circuit

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. Adj. range	DS1+	ESTP/N[8] = 0h ESTP/N[7:0] = 8Bh		+2500		ppm/°C	
	DS1-	ESTP/N[8] = 1h ESTP/N[7:0] = DEh		-4000		ppm/°C	
Adj. step	DS stp			18		ppm/°C	

Note) Design reference value; no production test performed.

7.2.7) LPF, S/H & Buffer

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Measurement in test mode after offset voltage and span voltage adjustment							
LPF cufoff frequency	Fc1		40	60	80	kHz	
S/H&Buffer gain	SHG		1.935	2.222	2.523	times	
S/H&Buffer out pre-adj. error	SHerr		-65		65	mV	
BUF gain adj. width	Bufg		1.000	1.111	1.222	times	
VOUT output voltage range	Vbuf+	Load resistance 9.5kΩ (to VDD or VSS)	0.98 *VDD			V	
	Vbuf-				0.02 *VDD	V	
BUF feedback resistor value	Rbuf		102	146	190	kΩ	

7.2.8) Level shift

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Measurement in test mode after offset voltage and span voltage adjustment							
Output reference Voltage adj. width (Level shift)	Vlv+	Max ELV[8] = 1h ELV[7:0] = FFh		1.00 *VDD		V	Note1)
	Vlv-	Min ELV[8] = 0h ELV[7:0] = FFh		0.00 *VDD		V	Note1)
Adj. step	Vlstp			0.002 *VDD		V	

Note1) It is limited from 0.02*VDD to 0.98*VDD by the VOUT output range (Vbuf+, Vbuf-).

7.2.9) SCF & SMF

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

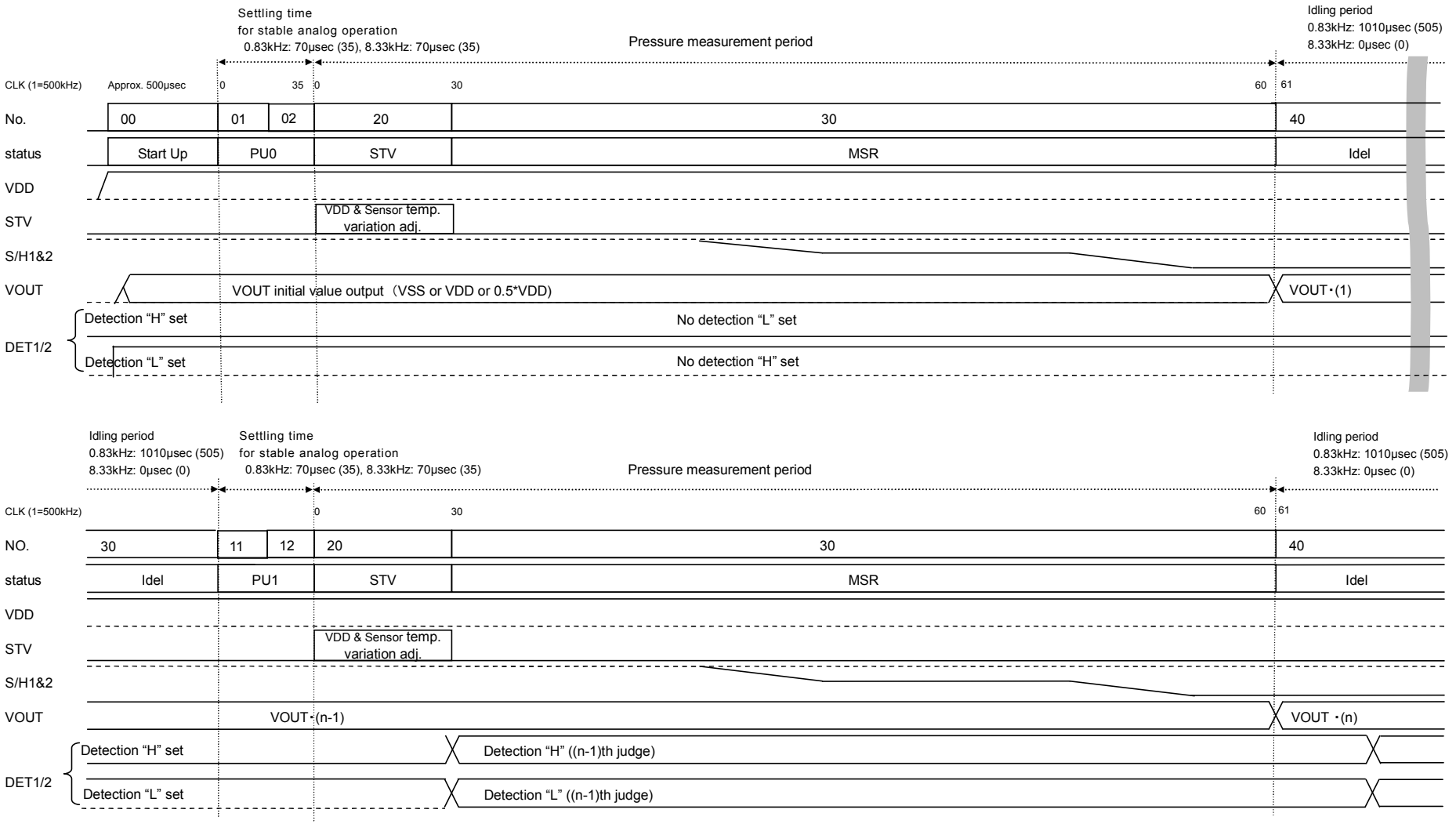
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Measurement in test mode after offset voltage and span voltage adjustment							
SCF&SMF freq. response	Fc1	ESCF[1:0] = 1h 10Hz referenced -3dB	0.8	1.0	1.2	kHz	
	Fc2	ESCF[1:0] = 2h 10Hz referenced -3dB	400	500	600	Hz	
	Fc3	ESCF[1:0] = 3h 10Hz referenced -3dB	200	250	300	Hz	
SCF&SMF gain	SCFG1	ESCF[1:0] = 1h	1.000	1.111	1.222	times	

7.2.10) External temperature sensor drive circuit

VDD = 3, 3.3, 5V ± 10%, Ta = -40 to 105ºC, register default, unless otherwise note

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Description
Temp. sensor sink current	Iconst1	After IREF adj.	45	50	55	µA	
Temp. sensor source current	Iconst2	After IREF adj. ETMP[1:0] = 1h	-55	-50	-45	µA	
Input voltage range (sink)	Extpsi4	VS = 4V	3160	3400	3610	mV	
	Extpsi2	VS = 2.2V	1350	1600	1810	mV	
Input voltage range (surce)	Extpso	ETMP[1:0] = 1h	392	600	866	mV	

13. Operation Sequence



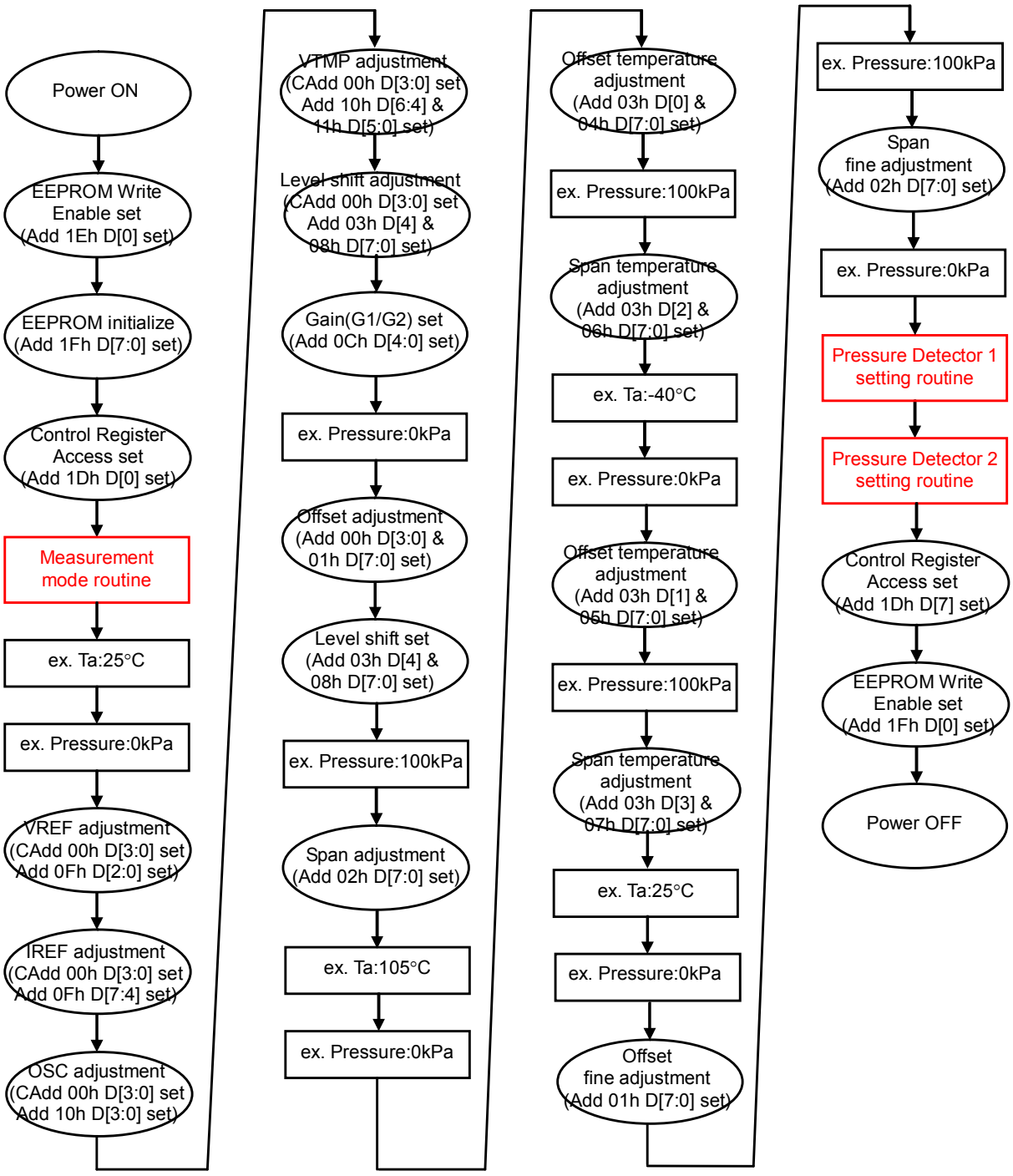
■ **Description of Operation Timing Status (pressure detection circuit effective)**

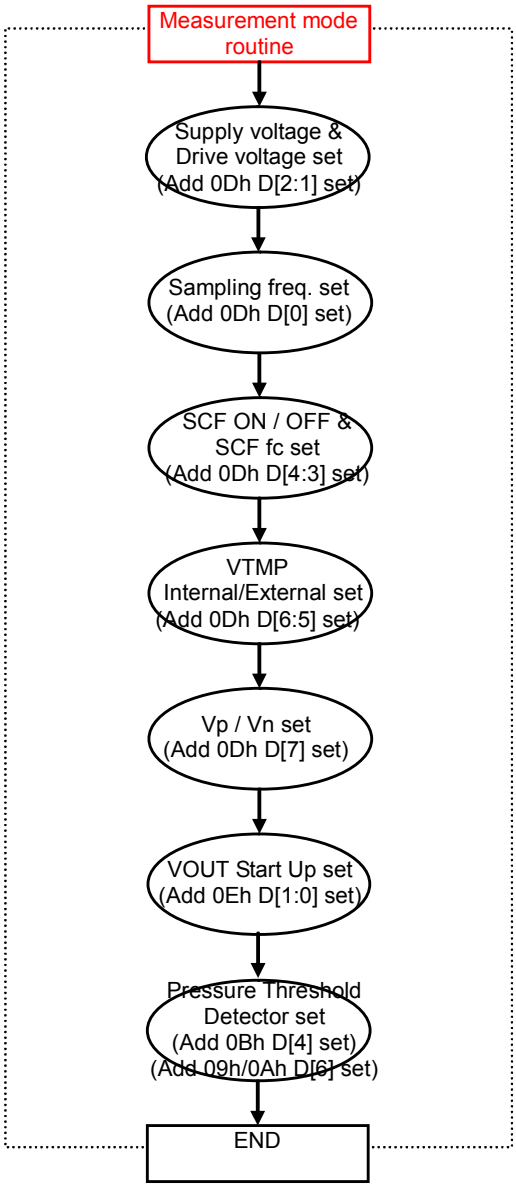
State	No.	CLK	Operations
Start Up	00		It is the time until analog circuits operate stably. Analog reference circuits as VREF, IREF, etc. start up and adjusted output reference voltage (VSS or VDD or 0.5*VDD) is output from the VOUT pin.
PU0	01	CLK = 30	Clock count start Analog circuits startup
	02	CLK = 0 or 5	Ta = 25°C detected comparator operation Note1)
STV	20	CLK = 30	STV circuits operation
MSR	30	CLK = 30	Result of pressure correction is output from VOUT pin.
Idel	40	CLK = 0 or 505	Idling With Fs = 8.33kHz, no idling and in continuous operation. Idling period Fs = 0.83kHz 505 CLK Fs = 8.33kHz 0 CLK
PU1	11	CLK = 0 or 30	Clock count start Analog circuits startup Note2)
	12	CLK = 0 or 5	Ta = 25°C detected comparator operation Note1)
:		:	:

Note1) Only operation in the quasi 2nd order correction mode by piecewise linear approximation
Note2) Only operation in the Fs = 0.83kHz mode

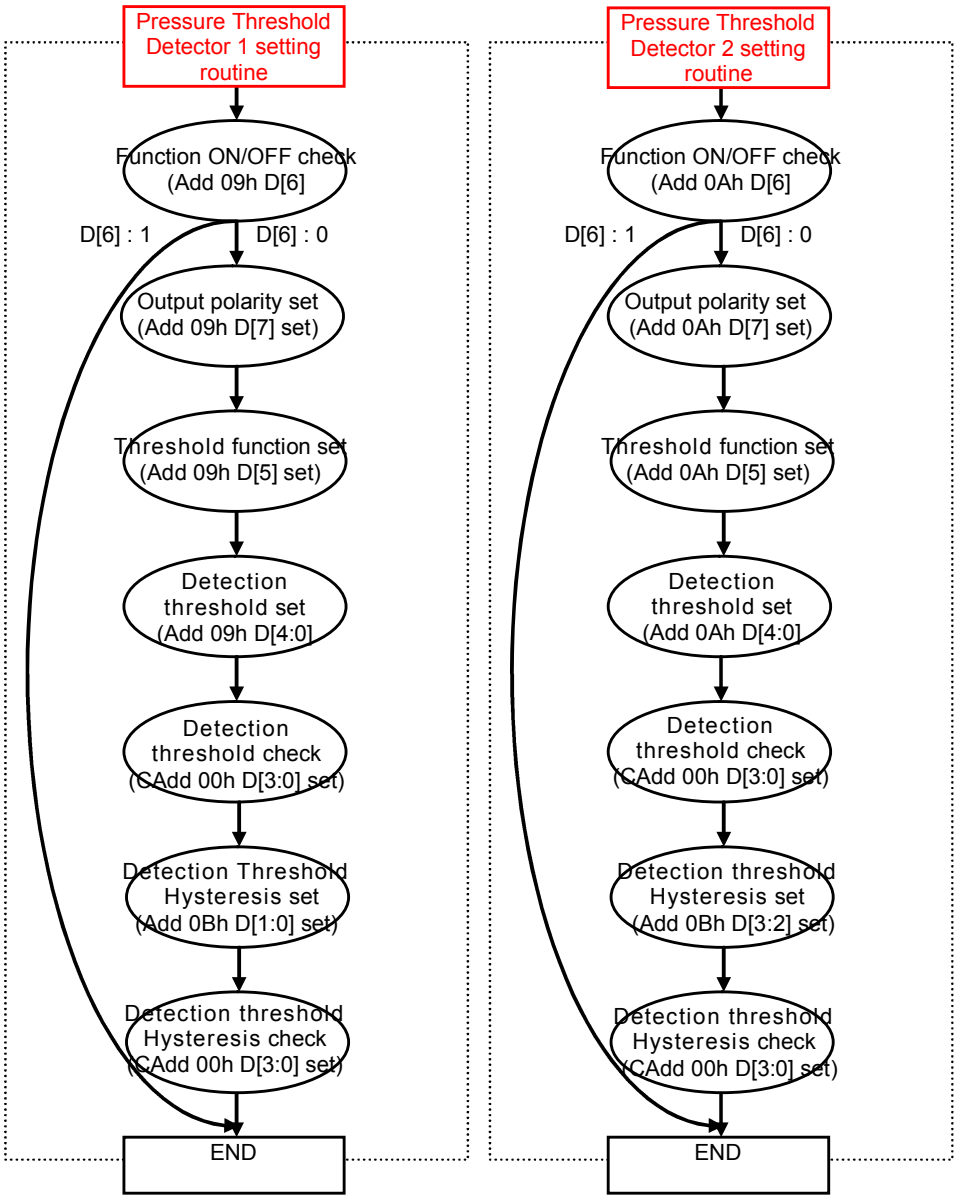
14. Adjustment Sequence

note)
EEPROM Address is indicated by “Add”, Control Register Address is indicated by “CAdd”.
Please refer the digital part flow chart for EEPROM / Control Register writing and reading.





Note)
EEPROM Address is indicated by “Add”, Control Register Address is indicated by “CAdd”.



Note)
EEPROM Address is indicated by “Add”, Control Register Address is indicated by “CAdd”.

15. Functional Descriptions

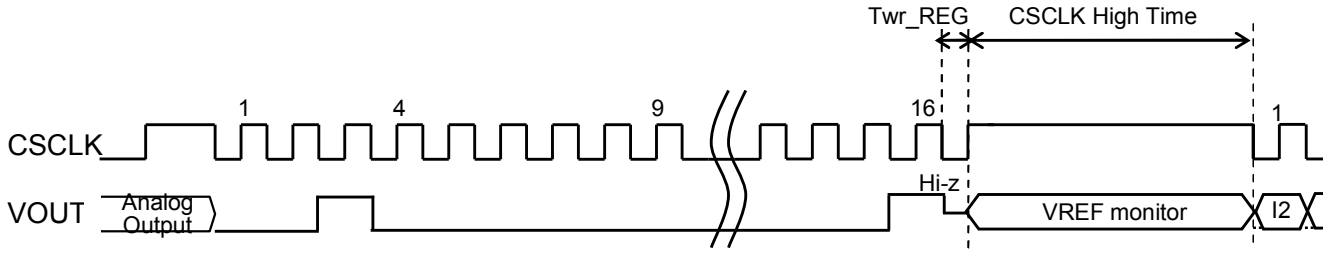
1) Adjustment Procedure Description (Example)

The adjustment procedure for the AK8999A follows (See "**Adjustment Sequence**").

Note) Keep the sequence as adjustment of VREF adjustment, IREF adjustment, OSC adjustment, and VTMP adjustment in turn. If VREF adjustment and IREF adjustment are performed after OSC adjustment, adjusted OSC frequency will shift.
The EEPROM address is referred to as "address", while the control register (volatile memory) address is referred to as "C address".

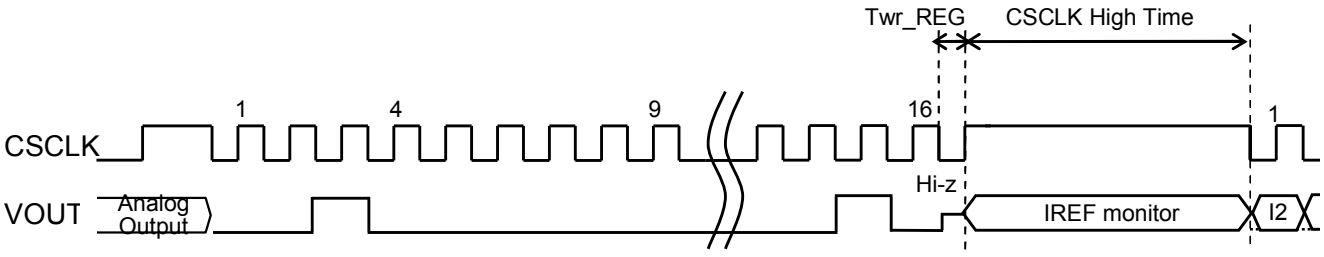
1.1) VREF Adjustment (completed when shipped in package form)

The reference voltage is adjusted to 1.0V by VREF voltage adjustment EEPROM (address: 0Fh, data: EVR[2:0]). Adjusting the VREF voltage also means adjustment of the sensor drive voltage (VS). VREF voltage is observed at VOUT pin (See "**Recommended External Circuits**") while the CSCLK pin High (CSCLK High Time) after the writing of an adjustment mode register (C address: 00h, data: AM[3:0] = 1h).



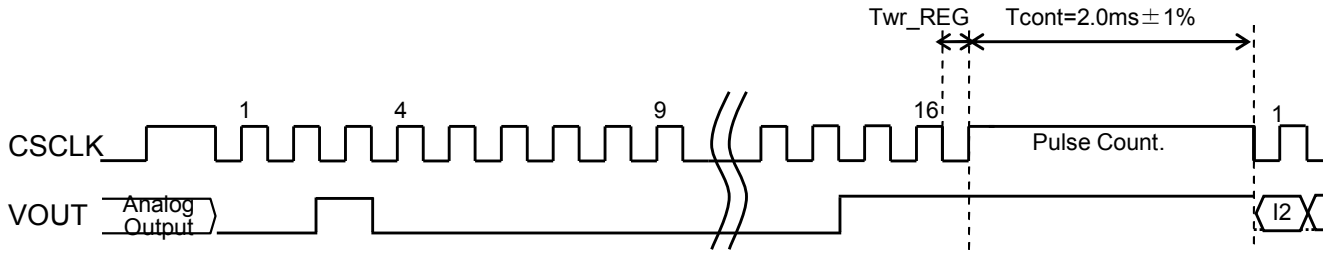
1.2) IREF Adjustment (completed when shipped in package form)

The reference current is adjusted to 1.0μA.
The external resistor (1MΩ) is connected to VOUT pin. Reference current is supplied to the external resistor, and IREF current adjustment EEPROM (address: 0Fh, data: EIR[3:0]) is adjusted so that the voltage across the both ends of the external resistor is set to 1.0V. And it can adjust more accurate by taking into consideration the input impedance (input resistance) of adjustment equipment. With 1MΩ external resistor to the VOUT pin, it is adjusted in voltage domain. The external 1MΩ should be connected only at the time of IREF adjustment. When with resistance 1MΩ is connected always in outside, please be careful of the input impedance of adjustment equipment. The input impedance of adjustment equipment should become more than 10GΩ. IREF current is observed at VOUT pin (See "**Recommended External Circuits**") while the CSCLK pin High (CSCLK High Time) after the writing of an adjustment mode register (C address: 00h, data: AM[3:0] = 2h).



1.3) OSC Adjustment (completed when shipped in package form)

The intermittent operation control clock is adjusted to 1000kHz.
Oscillation frequency can be adjusted without monitoring frequency directly.
The high level for the fixed period (2.0msec ± 1%) is inputted from the CSCLK pin after the writing of an adjustment mode register (C address: 00h, data: AM[3:0] = 3h). The internal clock pulses are counted in the integrated counter circuit, and the count value is stored in the control register (C address: 01h, data: CT[7:0]). The adjustment data (address: 10h, data: EFR[3:0]) for oscillation frequency is calculated from the stored count value. The adjustment can be done within 1000kHz ± 5% accuracy by writing the adjustment data in EEPROM. Since the error of High period turns into an adjustment error of frequency, please set period as 2.0ms ± 1%.



The explanation of oscillation frequency adjustment data (address: 10h, data: EFR[3:0]) is as follows.

The count value stored in the control register (C address: 01h, data: CT[7:0]) is read for the ratio check. A ratio will be 0% (ideal value), when the High level period of CSCLK pin is 2 msec and the frequency of the internal oscillator is 1000kHz. The ratio varies from 0% by the error of High level period and the frequency variation of the internal oscillator. And the High time which can be set up becomes a range from which a ratio will be -99% to 154%. Be aware that the error is easily affected when the ratio is small. The counter value shown as FF hex means overflow, please measure again by changing High level period.

Please set the adjustment data of oscillation frequency as the sum of the ratio of CT [7:0] data and the ratio of EFR [3:0] data is close to 0%.

Address : 01 hex D[7:0]= CT[7:0]

CT[7:0]			Count value	Ratio	Description
Dec	Hex	Bin	(time)	(%)	
0	00	00000000	0	0	Default
1	01	00000001	1	-99	
:	:	:	:	:	
98	62	01100010	98	-2	
99	63	01100011	99	-1	
100	64	01100100	100	0	Ideal value
101	65	01100101	101	1	
102	66	01100110	102	2	
:	:	:	:	:	
254	FE	11111110	254	154	
255	FF	11111111	-	-	Counter error

Address : 10 hex D[3:0] = EFR[3:0]

EFR[3:0]			Ratio	Frequency Δf	Description
Dec	Hex	Bin	(%)	(kHz)	
-5	B	1011	-34	-251	
-4	C	1100	-25	-197	
-3	D	1101	-17	-146	
-2	E	1110	-11	-99	
-1	F	1111	-5	-52	
0	0	0000	0	0	Default
1	1	0001	5	49	
2	2	0010	10	106	
3	3	0011	14	162	
4	4	0100	18	224	
5	5	0101	22	274	
6	6	0110	25	329	
7	7	0111	28	384	

Note1) Hex 8 to A are prohibited for setup.

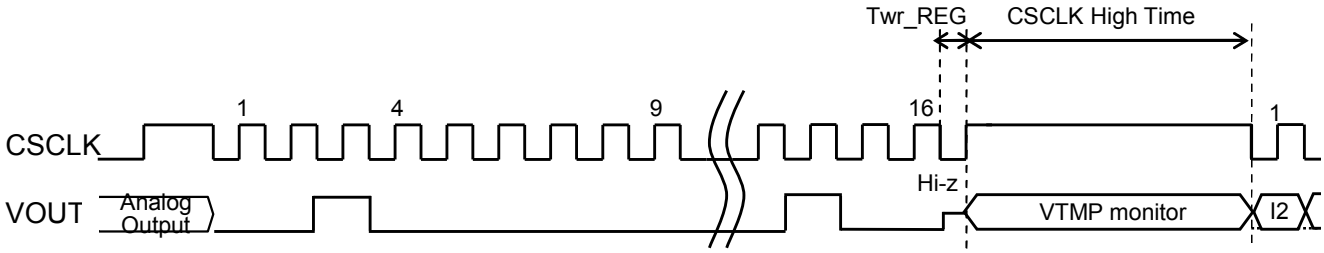
When High level period is not 2msec, the ideal value of CT [7:0] can be calculated as follows. Considering the calculated ideal value as 100%, and a ratio should be redefined. Please set the adjustment data of oscillation frequency as the sum of the ratio of CT [7:0] data and the ratio of EFR [3:0] data is close to 0%.

Count value[time] = High time[msec] / 2 * 100
ex.) In the case of 3 msec, 100time → 150time.

1.4) VTMP Adjustment (completed when shipped in package form)

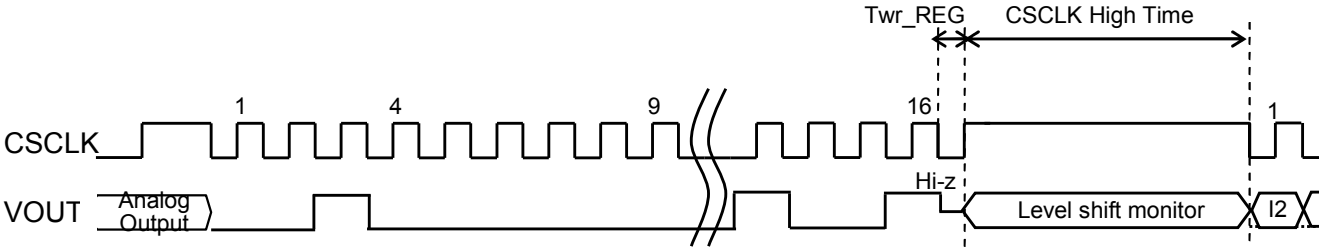
Temperature sensor output (VTMP) voltage is adjusted to match the VREF voltage.
When the external temperature sensor is used, connect the external temperature sensor to the EXTMP pin, and set up a measurement mode 1 EEPROM (address: 0Dh, data: ETMP[1:0] = 0 or 1h).
VTMP voltage is observed at VOUT pin while the CSCLK pin High (CSCLK High Time) after the writing of an adjustment mode register (C address: 00h, data: AM[3:0] = 4h).

*At the VTMP adjustment using the external temperature sensor, the External Temperature Sensor Drive circuit is normal ON in the sampling frequency 8.33kHz mode (ESF[0] = 0h).
If the actual operationg condition is the sampling frequency 0.83kHz mode (ESF[0] = 1h), AK8999A operates intermittent. The external temoperature sensor output voltage may be different from the voltage after the VTMP adjustment.



1.5) S/H Circuit Output Error Adjustment

The S/H circuit output voltage is adjusted to become 0.5*VDD at VOUT pin by using the Output reference voltage adjustment EEPROM (address: 03h, 08h, data: ELV[8], ELV[7:0]).



1.6) Input gain (G1/G2) setup

Set up G1/G2 gain so that Gain Amp.1/2 output voltages become the ranges (In the case of VDD = 5V, G1 ≤ 1600mV, G2 ≤ 1850mV). The voltage and temperature coefficient which are used for calculation is as follows.

The offset voltage and the span voltage at 25°C take the MAX values of the pressure sensor to be used. And the offset voltage temperature drift coefficient and the sensitivity temperature drift coefficient take the MIN values (minus polarity) of the pressure sensor to be used.

Voff25: Offset voltage of the pressure sensor@25°C
Vsp25: Span voltage of the pressure sensor @25°C
Ktoff: Offset voltage temperature drift coefficient of the pressure sensor (MIN value)
Ktsp: Sensitivity temperature drift coefficient of the pressure sensor (MIN value)

■ In the case of VDD = 5V and temperature = -40 to 105°C
Gain Amp.1 output
= G1*(Voff25+Vsp25+ktoff*(-40[°C]-25[°C])+Vsp25*ktsp*(-40[°C]-25[°C])) ≤ 1600mV
Gain Amp.2 output
= G1*G2*(Vsp25+Vsp25*ktsp*(-40[°C]-25[°C])) ≤ 1850mV

■ In the case of VDD = 3.3V/3.0V and temperature = -40 to 105°C
Gain Amp.1 output
= G1*(Voff25+Vsp25+ktoff*(-40[°C]-25[°C])+Vsp25*ktsp*(-40[°C]-25[°C])) ≤ 750mV/750mV
Gain Amp.2 output
= G1*G2*(Vsp25+Vsp25*ktsp*(-40[°C]-25[°C])) ≤ 990mV/850mV

1.7) Offset Voltage Adjustment

The offset voltage for the pressure sensor is adjusted including the AK8999A internal error by using the offset voltage adjustment EEPROM (address: 00h, 01h, data: EOCR[3:0], EOCF[7:0]).

■Offset Voltage Adjustment Example (@VDD:5V)
EOCR[3]: Offset voltage coarse adjustment sign bit
If unadjusted output is more than 0.5*VDD, set EOCR[3] = 1h.
If unadjusted output is less than 0.5*VDD, set EOCR[3] = 0h.
EOCR[2:0]: Offset voltage coarse adjustment: Adjust in 1600 mV steps.
EOCF[7]: Offset voltage fine adjustment sign bit
If unadjusted output is more than 0.5*VDD, set EOCF[7] = 1h.
If unadjusted output is less than 0.5*VDD, set EOCF[7] = 0h.
EOCF[6:0]: Offset voltage fine adjustment: Adjust in 8 mV steps.

When the offset voltage is +360mV (0.5*VDD reference), set EOCF[7] = 1h and EOCF[6:0] = 45dec.
360[mV]-(8[mV]*45[dec]) = 0.0[mV]

1.8) Output Reference Voltage Adjustment

Adjust the output reference voltage. The output reference voltage is adjusted by using the output reference voltage adjustment EEPROM (address: 03h, 08h, data: ELV[8], ELV[7:0]).

■Output Reference Voltage Adjustment Example (@VDD:5V)
When the output reference voltage is 100mV, set ELV[8] = 0h and ELV[7:0] = 240dec.
2500[mV]+(-0.002*240[dec])*5000[mV] = 100[mV]

1.9) Output Span Voltage Adjustment

The output span voltage for the connected pressure sensor is adjusted, including the AK8999A internal error, by using the output span voltage adjustment EEPROM. (address: 00h, 02h, data: ESCR[0], ESC[7:0])

In the case, the output span voltage cannot be adjusted to the target span voltage by the max code (ESC[7:0] = FFh), please raise 1 code at G1 gain and readjust **1.7) Offset Voltage Adjustments**.

■Output Span Voltage Adjustment Example (@VDD:5V)
When the output is 3700mV, set ESCR[0] = 1, ESC[7:0] = 153dec (target span voltage 4800mV).
(3700[mV]-100[mV])*1.8*(1-0.2*153/275)/(1+0.2*153/152.86) = 4800[mV]

1.10) Offset Temperature Drift Adjustment

The offset temperature drift for the pressure sensor is adjusted, including the AK8999A internal error, by using the offset voltage temperature drift adjustment EEPROM (address: 03h, 04h, 05h, data: EOTP/N[8], EOTP/N[7:0]).

■Offset Temperature Drift Adjustment Example (@VDD:5V)

Adjusting the low and high temperature coefficient is explained separately.
When this function is not used, set the same data as EOTP[8:0] and EOTN[8:0].

- Adjusting the high temperature coefficient

  EOTP[8]: Offset voltage adjustment sign bit

  If unadjusted output is greater than the output reference voltage at Ta = 105 ºC, set EOTP[8] = 1h.

  If unadjusted output is smaller than the output reference voltage at Ta = 105 ºC, set EOTP[8] = 0h.

  EOTP[7:0]: Offset voltage adjustment bit: Adjust in 0.144mV/ºC steps (@VDD: 5V).

  If the offset voltage is +300mV (with respect to the output reference voltage e.g.100mV) at Ta = 105°C, set EOTP[1] = 1h, EOTP[6:0] = 26dec.

  (100[mV]+300[mV])-(105[°C]-25[°C])*(0.144[mV/°C]*26[dec]) = 100.5[mV]

- Adjusting the low temperature coefficient

  EOTN[8]: Offset voltage adjustment sign bit

  If unadjusted output is greater than the output reference voltage at Ta = -40 ºC, set EOTN[8] = 0h.

  If unadjusted output is smaller than the output reference voltage at Ta = -40 ºC, set EOTN[8] = 1h.

  EOTN[7:0]: Offset voltage adjustment: Adjust in -0.144mV/ºC steps (@VDD: 5V).

  If the offset voltage is +300mV (with respect to the output reference voltage e.g.100mV) at Ta=-40°C, set EOTN[7] = 0h, EOTN[6:0] = 32dec.

  (100[mV]+300[mV])-(-40[°C]-25[°C])*(-0.144[mV/°C]*32[dec]) = 100.5[mV]

1.11) Sensitivity Temperature Drift Adjustment

The sensitivity temperature drift for the pressure sensor is adjusted, including the AK8999A internal error, by using the sensitivity temperature drift adjustment EEPROM (address: 03h, 05h, 06h, data: ESTP/N[8], ESTP/N[7:0]).

■Sensitivity Temperature Drift Adjustment Example (@VDD:5V, ESTC[0] = 1h)
Adjusting the low and high temperature coefficient is explained separately.
When this function is not used, set the same data as ESTP[8:0] and ESTN[8:0].

- Adjusting the high temperature coefficient

ESTP[8]: Sensitivity temperature drift adjustment sign bit (target span voltage 4800mV)
If unadjusted output is greater than 4800mV (with respect to the output reference voltage) at Ta = 105°C, set ESTP[8] = 0h.
If unadjusted output is smaller than 4800mV (with respect to the output reference voltage) at Ta = 105°C, set ESTP[8] = 1h.
ESTP[7:0]: Sensitivity temperature drift adjustment: Adjust in -18ppm/°C steps.

If the output voltage is +4,400mV (with respect to the output reference voltage e.g.100mV) at Ta = 105°C, set ESTP[8] = 1h, EST[7:0] = 58dec.
4400[mV]-(105[°C]-25[°C])*(-18[ppm/°C]*58[dec])*4800[mV] = 4800.9[mV]

- Adjusting the high temperature coefficient

ESTN[8]: Sensitivity temperature drift adjustment sign bit (target span voltage 4800mV)
If unadjusted output is greater than 4800mV (with respect to the output reference voltage) at Ta = -40°C, set ESTN[8] = 1h.
If unadjusted output is smaller than 4800mV (with respect to the output reference voltage) at Ta = -40°C, set ESTN[8] = 0h.
ESTN[7:0]: Sensitivity temperature drift adjustment: Adjust in 18ppm/°C steps.

If the output voltage is +4,400mV (with respect to the output reference voltage e.g.100mV) at Ta = -40°C, set ESTN[8] = 0h, ESTN[7:0] = 71dec.
4400[mV]-(-40[°C]-25[°C])*(18[ppm/°C]*71[dec])*4800[mV] = 4798.7[mV]

1.12) Offset Voltage Fine Adjustment

The offset voltage error is caused by compensating the offset voltage temperature drift. The offset voltage is adjusted using the offset voltage fine adjustment EEPROM (Address: 01h, data: EOCF[6:0]).

Note) Can not chage the polarity of EOCF[7] bit at this adjustment process, because the polarity of an offset temperature coefficient changes with chaging the polarity of EOCF[7] bit.

1.13) Output Span Voltage Fine Adjustment

The output span voltage error is caused by compensating the span voltage temperature drift. The output span voltage is adjusted using the output span voltage adjustment EEPROM (Address: 02h, data: ESC[7:0]).

2) Finding the VOUT and VO Pins External Capacitance (Cap)

This section explains how the VOUT and VO pins external capacitance is defined.
The requirements for determining the VOUT and VO pins external capacitance values are the stabilization time on power-up and noise characteristic.

2.1) VOUT Pin Output Voltage Stabilization Time

Note that depending on the VOUT and VO pins external capacitance values, the measurement values (VOUT pin voltage) may contain errors upon power-up.

"99% Settling time (③+④ in the figure)" in the table below represents the analog stabilization time ③ in the figure and the time required to settle down to 99% of the output voltage (0.1*VDD in this case) according to the pressure applied during the period (③+④ in the figure).
The period ③ in the figure is 0.512msec (typ).
Subsequently, the output voltage will settle to 99% according to the pressure during period ④ in the figure. When the VO pin capacitance is 1µF, the period ④ in the figure will settle within 672.4msec.

Settling time (period ④ in the figure) = -146[kΩ]*1[µF]*ln(1-99/100) = 672.4 [msec]

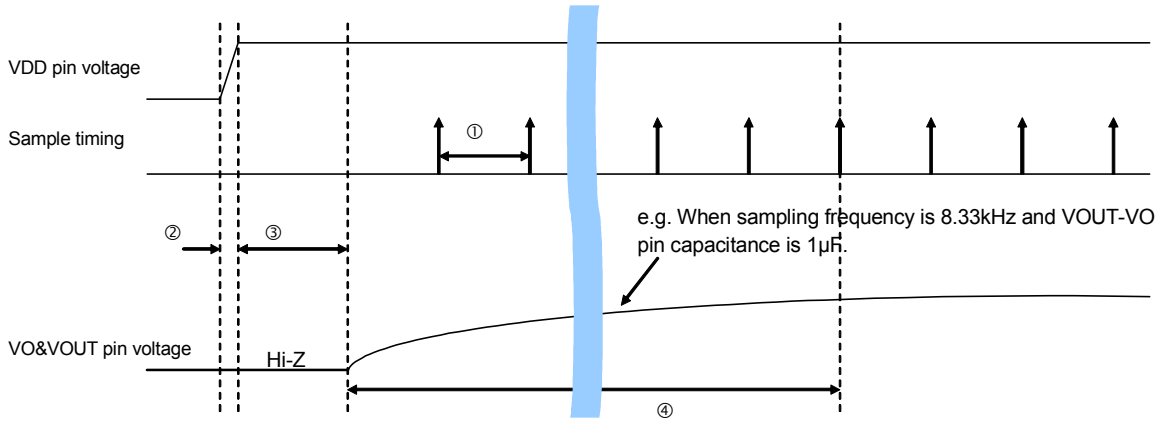
Therefore, the settling time up to 99% (period ③+④ in the figure) will be as follows:

99% settling time (period ③+④ in the figure) = 0.512[msec] +672.4[msec] = 672.912 [msec]

Referring to the previous calculation example, determine the stabilization time based on true terms of use:

Prerequisites:	VO pin external capacitance:	Cap（Cap[µF] typ., Cap*1.1[µF] worst）
	VO pin internal resistance:	Res（146[kΩ] typ., 190[kΩ] worst）
	Period ③ in the figure:	Time（0.512[msec] typ., 0.70[msec] worst）

Settling time (period ④ in the figure) = -Res*Cap*In(1-99/100)
99% settling time (period ③+④ in the figure) = Time + Settling time



① - ④ Reference designators
①: Sampling timing; this diagram represents 8.33kHz (0.12msec).
②: Power-up rise time (VDD).
③: Settling time for stable analog operation.
④: Pressure signal detection time. This time depends on the VO pin external capacitance and the internal 146kΩ resistance.

VO pin Ext. cap (nF)	Cutoff Freq.(Hz) (Typical)	Fig ③Time (msec)		99% Settling time (ms) (④)		99% Settling time (ms) (③+④)	
		Typical case	Worst case Note)	Typical case	Worst case Note)	Typical case	Worst case Note)
1000	1.090	0.512	0.700	672.4	962.5	672.9	963.2
220	4.955	0.512	0.700	147.9	211.7	148.4	212.4
22	49.55	0.512	0.700	14.79	21.17	15.30	21.87
2.2	495.5	0.512	0.700	1.479	2.117	1.991	2.817
0.22	4.96k	0.512	0.700	0.148	0.212	0.660	0.912
0.1	10.9k	0.512	0.700	0.067	0.096	0.579	0.796

Note) External capacitance ± 10% and worst case for lot variations.

2.2) Noise Reduction Effects with Band Limitation

The relationship between an external capacitance of the VO pin and noise reduction effect is shown below.

Sampling Freq.(Hz)	VO pin Ext. cap (nF)	Typical Cutoff Freq.(Hz)	Noise Reduction Effect (dB)	
			Typical case	Worst case Note)
0.83k	1000	1.090	-23.03	-22.30
	220	4.955	-16.96	-16.18
	22	49.55	-7.70	-6.98
	2.2	495.5	-1.25	-1.01
	No capacitor	-	0.00	0.00
8.33k	220	4.955	-24.41	-24.39
	22	49.55	-16.70	-16.66
	2.2	495.5	-7.67	-6.96
	0.22	4.96k	-1.25	-1.01
	No capacitor	-	0.00	0.00

Note) External capacitance ± 10% and worst case for lot variations.

As seen in Sections "2.1) VOUT pin output voltage stabilization time" and "2.2) Noise Reduction Effect with Band Limitation", the VO pin external capacitance value should be reduced to decrease the measurement time. The VO pin external capacitance value should be larger to reduce the noise.
On determining the VO pin external capacitance value, various conditions should be thoroughly reviewed according to the application requirements.

3) Pressure Threshold Detection Operation at Power-Up

Note that pressure threshold detectors operate at power up.
VOUT pin output voltage is settled down based on the time constant determined by the internal resistance 146kΩ and VO pin external capacitance Cap value (see **2) Finding the VOUT and VO Pins External Capacitance (Cap)**). Note that errors may be detected during the time in which VOUT pin output is not settled down to the voltage required according to the pressure applied.

4) Power Consumption

Current values described in **3) Supply Voltage Current in the Electrical Characteristics** are those for the average current. The maximum current is shown in the table below. Use a power supply with sufficient supply capacity by referring to this table:

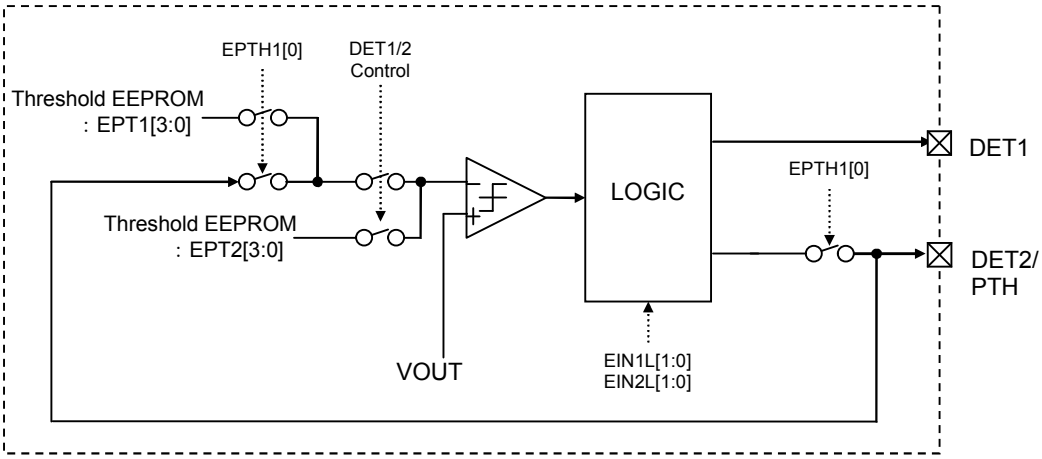
	Units	VDD:3.6V	VDD:5.5V	Description
Max. Current	mA	6.8	9.5	Reference value for design

5) Pressure Threshold Detectors 1 and 2

5.1) Pressure Threshold Detector's Detection Threshold

The internal and external detection threshold setup for the pressure threshold detectors 1 and 2 is described.

Block diagram of the pressure threshold detectors 1 and 2:



The detection threshold of the pressure threshold detector 1 can be set either through the external input (DET/PTH pin) or internal setup (EEPROM setup EPT1[4:0]). The detection threshold of the pressure threshold detector 2 can be only set the internal setup (EEPROM setup EPT2[4:0]).

5.2) Pressure Threshold Detector's hysteresis voltage

The relation between the hysteresis voltage and the detection voltage of the pressure threshold detectors 1 and 2 is described

The hysteresis voltage related with the detection threshold voltage of the pressure threshold detectors 1 and 2 is as follows by the detection threshold setup (EEPROM setup EIN1L[0], EIN2L[0]).

Detect pressure above threshold : Detection threshold – Hysteresis voltage
Detect pressure below threshold : Detection threshold + Hysteresis voltage

In addition, same as the detection threshold of the pressure threshold detectors 1 and 2, the setting range of "Detection threshold ± Hysteresis voltage" should be set between from 0.125*VDD to 0.9*VDD.

6) The Compensation of the 2nd Order Temperature Characteristics of Offset and Span Voltage

Offset temperature drift and sensitivity temperature drift characteristics of a pressure sensor can be adjusted by the 1st order compensation coefficient or the 2nd order compensation coefficient by piecewise linear approximation.

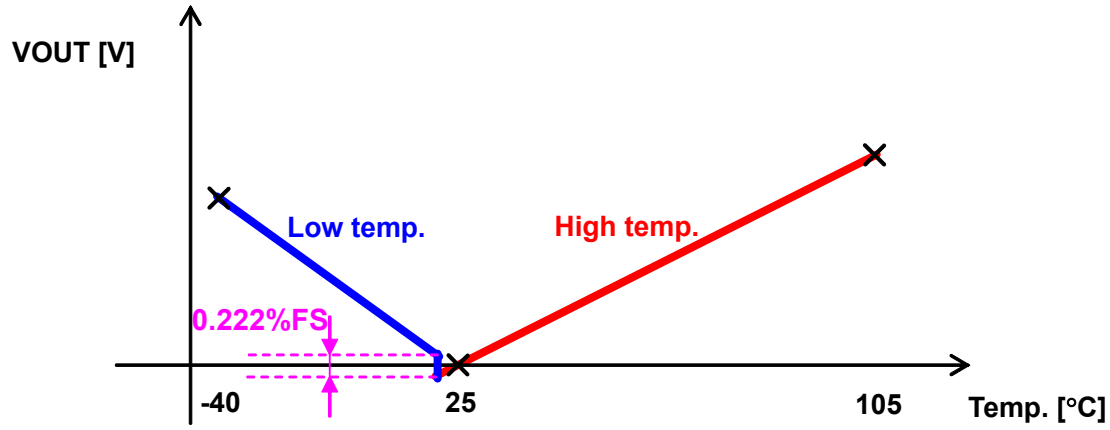
The AK8999A can compensate the 1st and 2nd order temperature characteristics of offset and span voltage temperature drift. The compensation of the quasi 2nd order temperature characteristics uses the piecewise linear approximation that has each correction coefficient for the high and low temperature side on the basis of 25°C.

When the 1st order temperature characteristics of offset and span voltage temperature drift is adjusted, the offset and span voltage temperature coefficients are calculated from the measurement results of at least two temperatures (for example, 25°C and -40°C and/or 105°C) and set the same coefficient for the high and low temperature side.

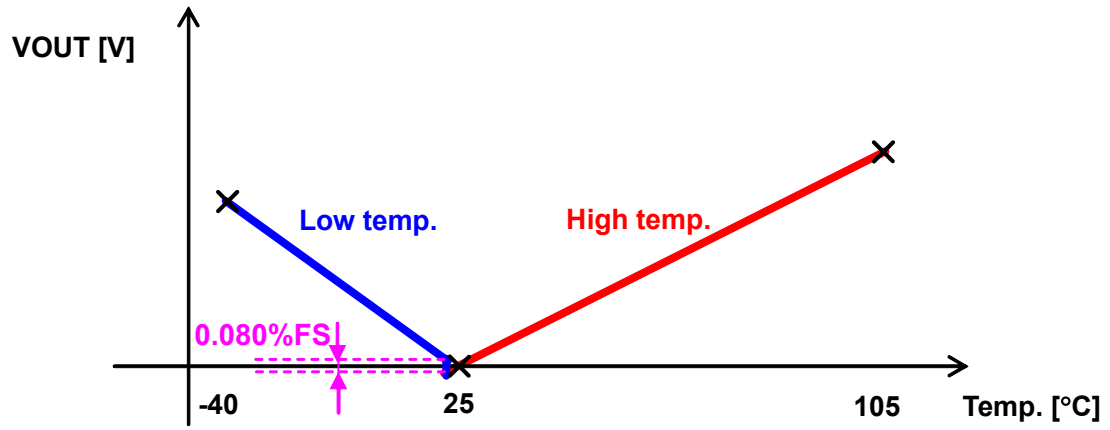
When the quasi 2nd order temperature characteristics of offset and span voltage temperature drift is adjusted, the offset and span vltage temperature coefficients are calculated from the measurement results for each the high and low temperature side (for example, 25°C and -40°C and/or 105°C) and set separately.

When the quasi 2nd order temperature characteristics is compensated by using the piecewise linear approximation, the adjustment error (Span adjustment error : 0.080%FS max., Offset adjustment error : 0.222%FS max.) can be appeared by the comparator offset etc. on the turning point near 25°C.

The compensation of offset voltage temperature characteristics @VOUT



The compensation of span voltage temperature characteristics @VOUT

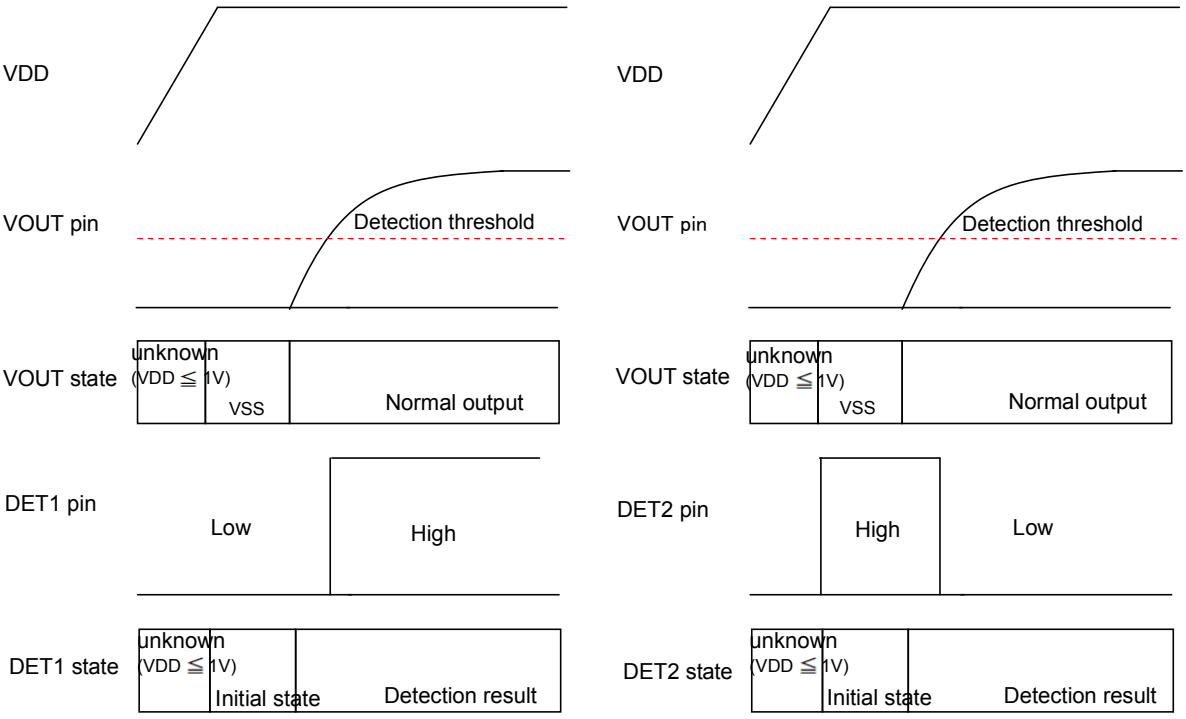


7) The Initial State Setup of VOUT pin, DET1 pin and DET2 pin at Power-Up

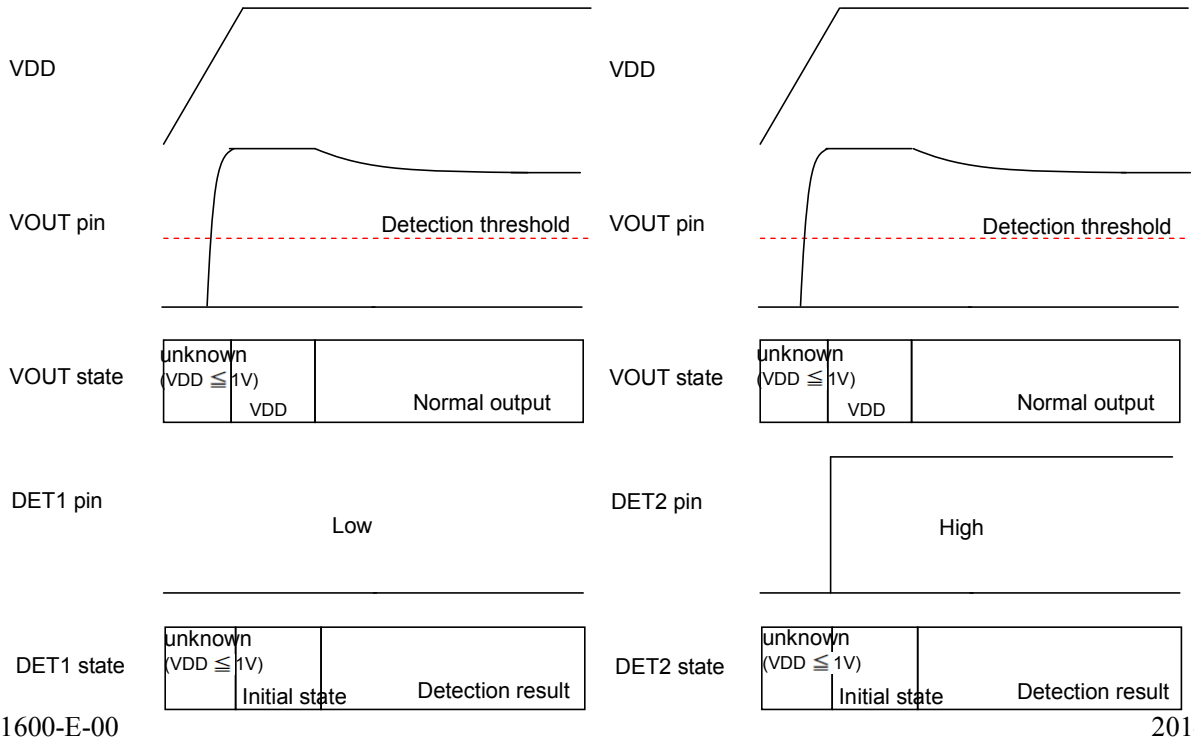
To make the Pressure Threshold Detectors generate the correct result at power up, the initial state of VOUT pin, and the output polarity and the detection direction of the Pressure Threshold Detectors must be set by EEPROM (EVOUT[1:0], EINV1[0], EIN1L[0], EINV2[0], EIN2L[0]).

The relation between the data in EEPROM and the output waveform of VOUT pin, DET1 pin and DET2 pin is explained in the following figures.

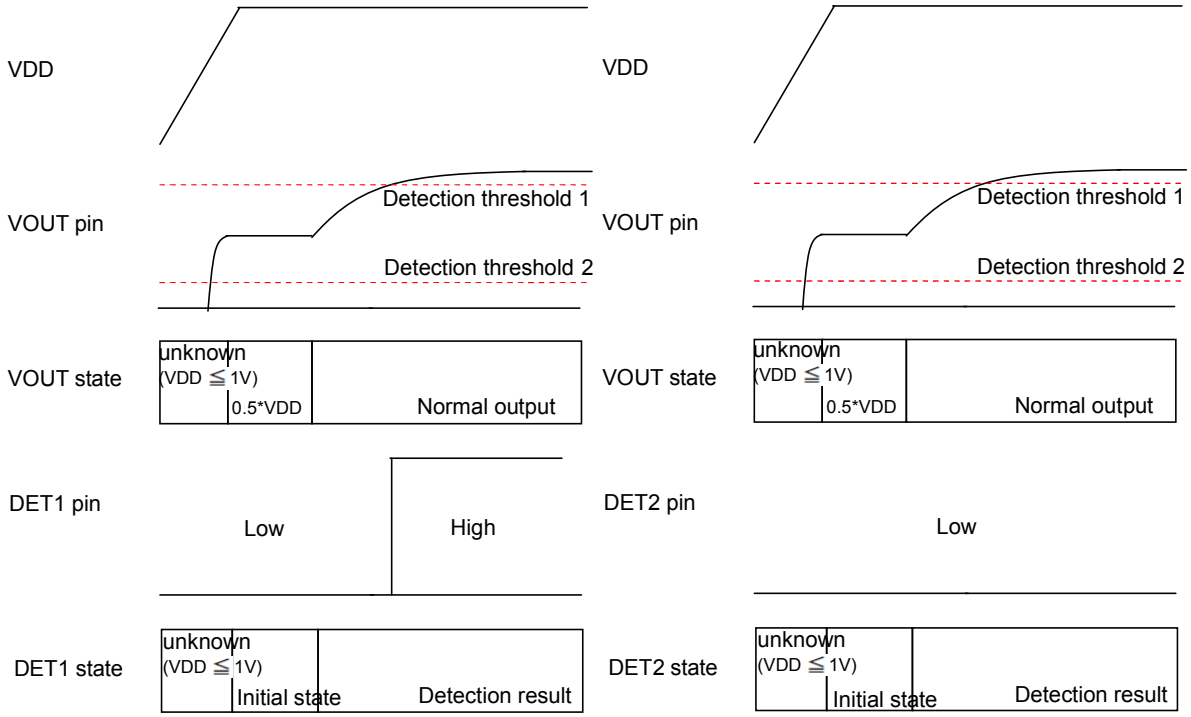
7.1) Detection Conditions: EIN1L[0]=EIN2L[0]=EINV1[0]=0h, EINV2[0]=1h, EVOUT[1:0]=0h



7.2) Detection Conditions: EIN1L[0]=EIN2L[0]=1h, EINV1[0]=0h, EINV2[0]=1h, EVOUT[1:0]=1h



7.3) Detection Conditions : EIN1L[0]=1h, EIN2L[0]=0h, EINV1[0]=EINV2[0]=0h, EVOUT[1:0]=2h



8) Note on the Use of Output Reference Voltage

When output reference voltage adjustment is used, please be aware of the following.

When ELV[8] is changed from 0h to 1h, VOUT output voltage may shift by offset of an internal circuit (around 1 code of ELV[7:0] as maximum). When adjusted using ELV[8] = 1h, please check VOUT output voltage by ELV[7:0] = 00h, and as the start point adjust to the target output reference voltage.

9) Note on the Use of Offset Voltage Fine Adjustment

When offset voltage fine adjustment is used, please be aware of the following. (It becomes the same contents as the preceding paragraph.)

When EOCF[7] is changed from 0h to 1h, VOUT output voltage may shift by offset of an internal circuit (around 1 code of EOCF[6:0] as maximum). When adjusted using EOCF[7] = 1h, please check VOUT output voltage by EOCF[6:0] = 00h, and as the start point adjust to the target offset voltage.

16. Serial Interface Description

The data of EEPROM and control register (volatile memory) in the AK8999A can be written and read through a 2-wire serial interface on CSCLK pin and VOUT pin. When CSCLK = High is maintained beyond a definite period of time (1.0msec), VOUT output will change from the Analog output to SDI/O (Serial data I/O).
And data is captured from VOUT synchronously with the rising edge of CSCLK after SDI/O shift. Input data contains three instruction bits (I2 - I0), five address bits (A4 - A0) and eight data bits (D7 - D0). Provide the data in the order of I2 → I0 → A4 → A0 → D7 → D0. And when CSCLK=Low is maintained beyond a definite period of time (0.5msec), VOUT output will return from SDI/O to the Analog output.
On the WRITE instruction, allow 5msec or more write time for EEPROM and 10μsec or more write time for the control register (see **7) Digital AC Characteristics in the Electrical Characteristics**). For the READ instruction, data is written up to 8CLK for CSCLK and the data output starting at the rising edge of 9CLK is read out.

1) Data Configuration

Configuration of data written to or read out through the serial interface is shown below. There are 16 specific bits of data in total comprised of three instruction bits, five address bits and eight data bits.

Instruction			Address					Data							
I2	I1	I0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

←**Data input direction**

2) Description of Instructions

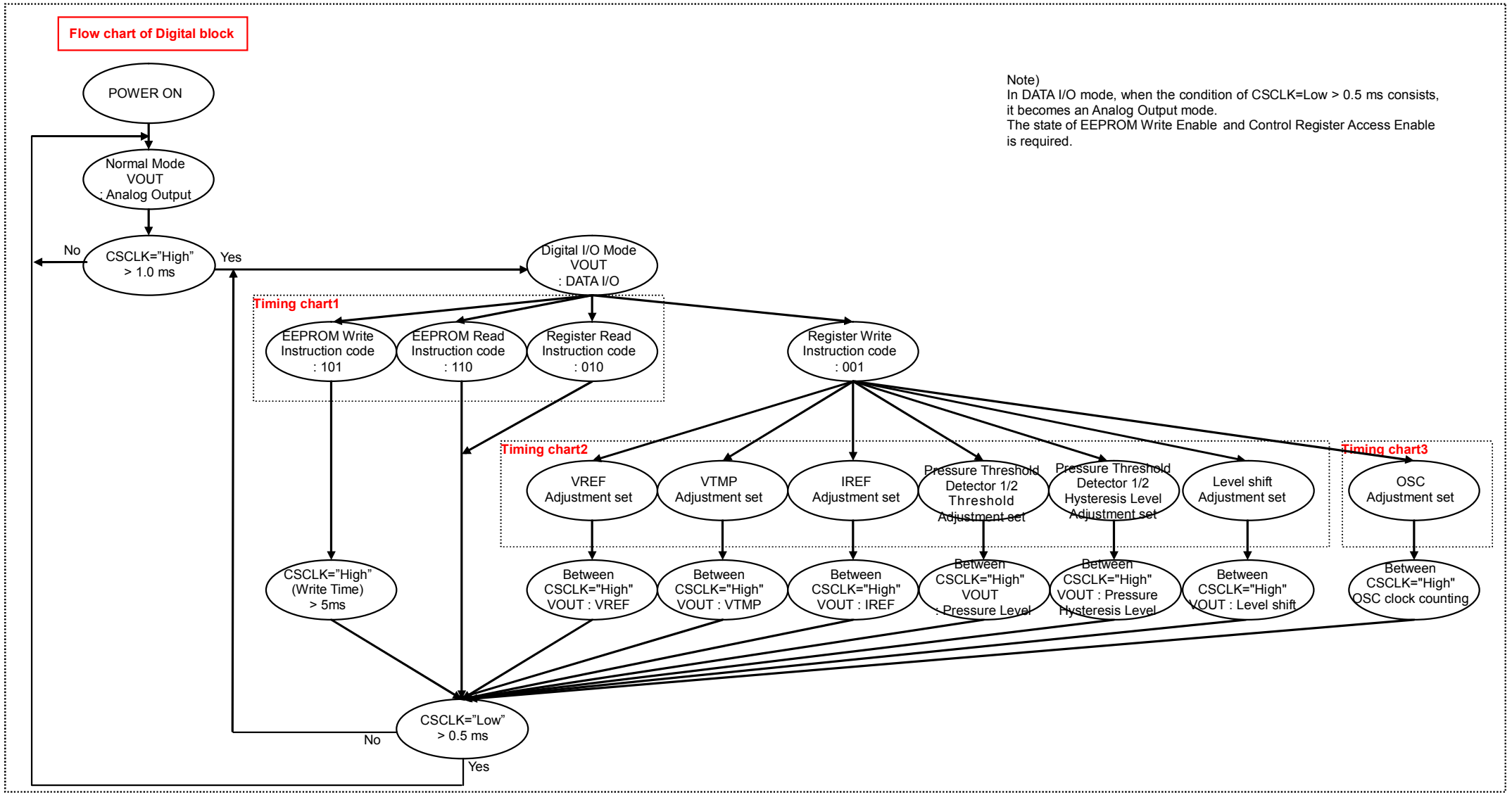
Instruction codes are summarized below.

Code Note)			Instruction	Description
I2	I1	I0		
1	1	0	EEPROM read (Read Mode)	Read out the data written in the EEPROM
1	0	1	EEPROM write (Write Mode)	Write data to the EEPROM. Write time (from 16th CSCLK rising edge to CSCLK falling edge) requires 5msec or more.
			EEPROM batch write (Write Mode)	If the 1Fh address is written, input data is written to all addresses except for 1Eh. Write time (from 16th CSCLK rising edge to CSCLK falling edge) requires 10msec or more.
0	1	0	Control reg. read (Read Mode)	Read out the data written in the control register.
0	0	1	Control reg. write (Write Mode)	Write the data to the control register. Write time (from 16th CSCLK rising edge to CSCLK falling edge) requires 10μsec or more.

Note) Instructions other than this are prohibited.

3) Flow chart of Digital block

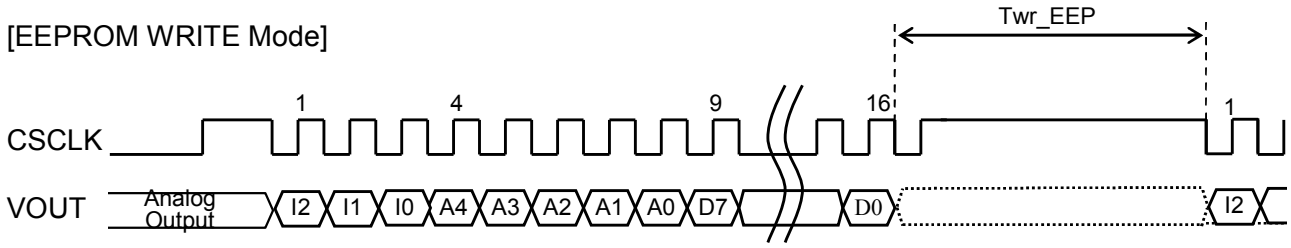
The flow chart of digital block is shown below.



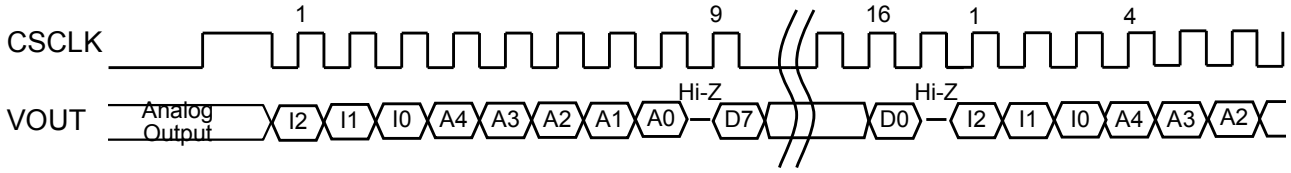
4) Serial Interface Timing Diagram

4.1) **Timing chart1**

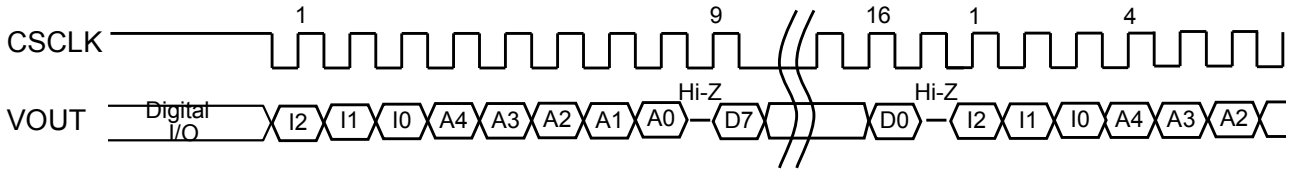
[EEPROM WRITE Mode]



[EEPROM READ Mode]

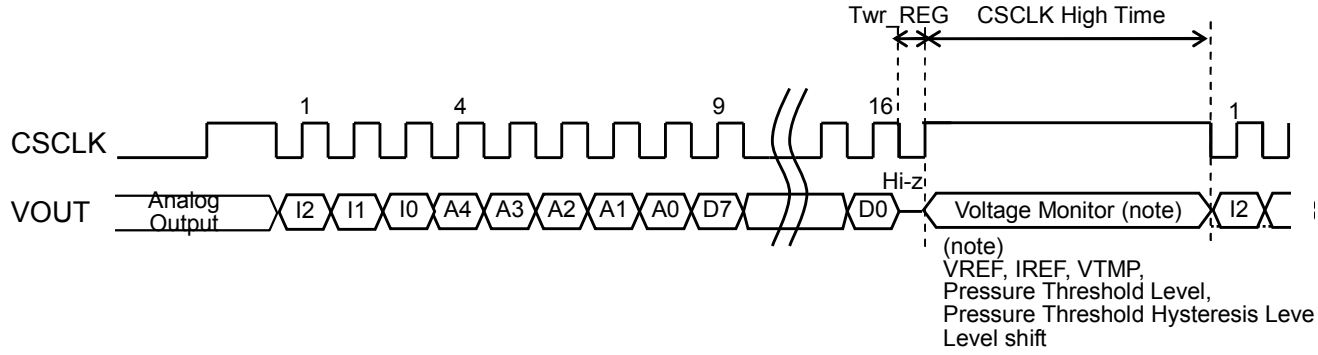


[Register READ Mode]



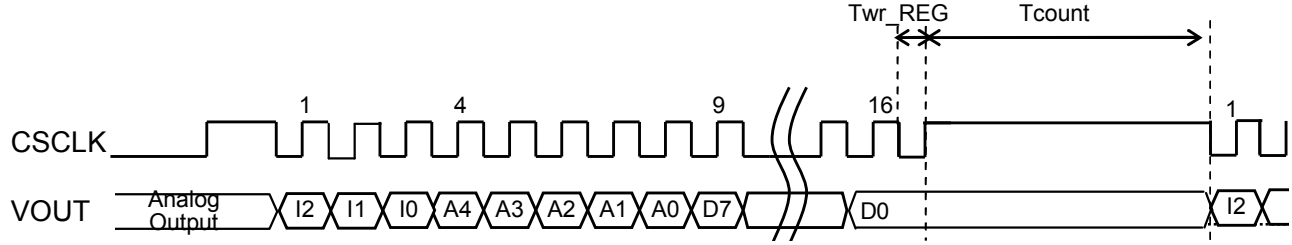
4.2) **Timing chart2**

[Register Write Mode1]
VREF, IREF, VTMP, Pressure Threshold Level, Pressure Threshold Hysteresis Level, Level shift Adjustment set



4.3) **Timing chart3**

[Register Write Mode2]
OSC Adjustment set



5) Register Map

5.1) EEPROM Map

Name	Content	Address (hex)	Data D7	D6	D5	D4	D3	D2	D1	D0
OCR SCR	Offset voltage coarse adj. Output span voltage coarse adj.	00h	ESCR[0]	dummy	dummy	dummy	EOCR[3]	EOCR[2]	EOCR[1]	EOCR[0]
			0	0	0	0	0	0	0	0
OCF	Offset voltage fine adj.	01h	EOCF[7]	EOCF[6]	EOCF[5]	EOCF[4]	EOCF[3]	EOCF[2]	ECCF[1]	EOCF[0]
			0	0	0	0	0	0	0	0
SC	Output span voltage adj.	02h	ESC[7]	ESC[6]	ESC[5]	ESC[4]	ESC[3]	ESC[2]	ESC[1]	ESC[0]
			0	0	0	0	0	0	0	0
OTS STS LVS	Offset voltage temp. drift adj. Sens. temp. drift adj. (MSB) Output ref. voltage adj. (MSB)	03h				ELV[8]	ESTN[8]	ESTP[8]	EOTN[8]	EOT[8]
						0	0	0	0	0
OTP	Offset voltage temp. drift adj. (High temp. side)	04h	EOTP[7]	EOTP[6]	EOTP[5]	EOTP[4]	EOTP[3]	EOTP[2]	EOTP[1]	EOTP[0]
			0	0	0	0	0	0	0	0
OTN	Offset voltage temp. drift adj. (Low temp. side)	05h	EOTN[7]	EOTN[6]	EOTN[5]	EOTN[4]	EOTN[3]	EOTN[2]	EOTN[1]	EOTN[0]
			0	0	0	0	0	0	0	0
STP	Sens. temp. drift adj. (High temp. side)	06h	ESTP[7]	ESTP[6]	ESTP[5]	ESTP[4]	ESTP[3]	ESTP[2]	ESTP[1]	ESTP[0]
			0	0	0	0	0	0	0	0
STN	Sens. temp. drift adj. (Low temp. side)	07h	ESTN[7]	ESTN[6]	ESTN[5]	ESTN[4]	ESTN[3]	ESTN[2]	ESTN[1]	ESTN[0]
			0	0	0	0	0	0	0	0
LV	Output ref. voltage adj.	08h	ELV[7]	ELV[6]	ELV[5]	ELV[4]	ELV[3]	ELV[2]	ELV[1]	ELV[0]
			0	0	0	0	0	0	0	0
PTH1	Pressure threshold detector 1	09h	EINV1[0]	EINE1[0]	EIN1L[0]	EPT1[4]	EPT1[3]	EPT1[2]	EPT1[1]	EPT1[0]
			0	0	0	0	0	0	0	0
PTH2	Pressure threshold detector 2	0Ah	EINV2[0]	EINE2[0]	EIN2L[0]	EPT2[4]	EPT2[3]	EPT2[2]	EPT2[1]	EPT2[0]
			0	0	0	0	0	0	0	0
HYS1 HYS2	Pressure threshold detector comparator hysteresis voltage adj.	0Bh				EPTH1[0]	EHYS2[1]	EHYS2[0]	EHYS1[1]	EHYS1[0]
						0	0	0	0	0
ING	Input gain adj.	0Ch				EIG[4]	EIG[3]	EIG[2]	EIG[1]	EIG[0]
						0	0	0	0	0
MM1	Meas. mode1	0Dh	EVPN[0]	ETMP[1]	ETMP[0]	ESCF[1]	ESCF[0]	EVD[1]	EVD[0]	ESF[0]
			0	0	0	0	0	0	0	0
MM2	Meas. mode2	0Eh							EVOUT[1]	EVOUT[0]
									0	0
VREF IREF Note1)	VREF voltage adj. IREF current adj.	0Fh	EIR[3]	EIR[2]	EIR[1]	EIR[0]		EVR[2]	EVR[1]	EVR[0]
			0	0	0	0		0	0	0
OSC VTMP Note1)	OSC frequency adj. VTMP coasce adlj.	10h		ETM[8]	ETM[7]	ETM[6]	EFR[3]	EFR[2]	EFR[1]	EFR[0]
				0	0	0	0	0	0	0
VTMP Note1)	VTMP fine adj.	11h			ETM[5]	ETM[4]	ETM[3]	ETM[2]	ETM[1]	ETM[0]
					0	0	0	0	0	0
UE	User-writable data	12h	EUE[7]	EUE[6]	EUE[5]	EUE[4]	EUE[3]	EUE[2]	EUE[1]	EUE[0]
			0	0	0	0	0	0	0	0
		13h – 1Ch								
MM3	Control register access setup	1Dh								ETST[0]
										0
EWE	EEPROM Write Enable	1Eh								EWE[0]
										0
AW	EEPROM batch write mode	1Fh	EAW[7]	EAW[6]	EAW[5]	EAW [4]	EAW[3]	EAW[2]	EAW[1]	EAW[0]

Note) Lower line of each data represents the factory settings written to EEPROM.
Access to the reserved addresses is prohibited.
Write “0” to the unused D[7:0].

Note1) For a packaged device, registers are adjusted before shipment. Therefore, defaults are not "0".

5.2) Control Register (Volatile Memory) Map

Name	Content	Address (hex)	Data D7	D6	D5	D4	D3	D2	D1	D0
CM1	Adjustment mode	00h					AM[3]	AM[2]	AM[1]	AM[0]
							0	0	0	0
CM2	OSC variable ratio Note1)	01h	CT[7]	CT[6]	CT[5]	CT[4]	CT[3]	CT[2]	CT[1]	CT[0]
			0	0	0	0	0	0	0	0
	Reserved	02h – 1Fh								

Note) Lower line of each data represents the control register data upon power-up.
Access to the reserved addresses is prohibited.
Write "0" to the unused D[7:0].
Note1) Access to this register serves as ReadOnly.

6) EEPROM and control register Description

6.1) Description of EEPROM

Offset and span adjustment should be made after measurement mode setup and adjustment of the reference generator including VREF, IREF, OSC and VTMP.

a) Offset voltage adjustment (EEPROM names: OCR, OCF)

Coarse adjustment should be performed first, followed by a fine adjustment for the offset voltage. The content of the adjustment EEPROMs are shown here.

a.1) Offset voltage coarse adjustment (OCR)

The offset voltage is adjusted coarsely.
The offset adjustment voltage varies ratiometrically with respect to the supply voltage.
The ratio in the table below is benchmarked to a VOUT output of 4800 mV (@VDD: 5V) as 100%
(Ratio = (Offset voltage @VDD: 5V)/4800[mV]*100[%]).

Address : 00 hex D[3:0] = EOCR[3:0]

EOCR [2:0] Dec	Hex	Bin	Ratio (%)	VDD:3V, 3.3V EOCR [3] = 0 (mV)	EOCR [3] = 1 (mV)	VDD:5V EOCR [3] = 0 (mV)	EOCR [3] = 1 (mV)	Description
0	0	000	0.00	0	0	0	0	Default
1	1	001	33.33	800	-800	1600	-1600	
2	2	010	66.67	1600	-1600	3200	-3200	
3	3	011	100.00	2400	-2400	4800	-4800	
4	4	100	133.33	3200	-3200	6400	-6400	
5	5	101	166.67	4000	-4000	8000	-8000	
6	6	110	200.00	4800	-4800	9600	-9600	
7	7	111	233.33	5600	-5600	11200	-11200	

a.2) Offset voltage fine adjustment (OCF)

The offset voltage is adjusted finely.
The offset adjustment voltage varies ratiometrically with respect to the supply voltage.
The ratio in the table below is benchmarked to a VOUT output of 4800mV (@VDD: 5V) as 100%
(Ratio = (Offset voltage @VDD: 5V)/4800[mV]*100[%]).

Address : 01hex D[7:0] = EOCF[7:0]

EOCF [6:0]			Ratio	VDD:3V, 3.3V		VDD:5V		Description
Dec	Hex	Bin	(%)	EOCF [7] = 0 (mV)	EOCF [7] = 1 (mV)	EOCF [7] = 0 (mV)	EOCF [7] = 1 (mV)	
0	00	0000000	0	0	0	0	0	Default
1	01	0000001	0.17	4	-4	8	-8	
:	:	:	:	:	:	:	:	
15	0F	0001111	2.50	60	-60	120	-120	
16	10	0010000	2.67	64	-64	128	-128	
:	:	:	:	:	:	:	:	
31	1F	0011111	5.17	124	-124	248	-248	
32	20	0100000	5.33	128	-128	256	-256	
:	:	:	:	:	:	:	:	
63	3F	0111111	10.50	252	-252	504	-504	
64	40	1000000	10.67	256	-256	512	-512	
:	:	:	:	:	:	:	:	
126	7E	1111110	21.00	504	-504	1008	-1008	
127	7F	1111111	21.17	508	-508	1016	-1016	

b) Output span voltage adjustment (EEPROM name: SCR, SC)

The span voltage is adjusted.
The magnification in the table below is benchmarked to a VOUT output of 4800 mV (@VDD: 5V) as 100%
(Ratio = (Output voltage @VDD: 5V)/4800[mV]*100[%]).
The output and sensitivity describes the adjustable output voltages with the assumed reference output
(2400mV@VDD: 3V, 4800mV@VDD: 5V) when ESC[7:0] = 0 dec.

b.1) Output span voltage coarse adjustment (EEPROM name: SCR)

The output span voltage is adjusted coarsely.

Address : 00 hex D[7] = ESCR[0]

D[7:0]	Symbol	Mode setup
D[7]	ESCR[0]	Output span voltage coarse adjustment
0	SCRH	3.0x (1.57x to 3.0x) (defult)
1	SCRL	1.8x (1.1x to 1.8x)

b.2) Output span voltage fine adjustment (EEPROM name: SC, ESCR[0] = 1h)

The output span voltage is adjusted finely.

Address : 02 hex D[7:0] = ESC[7:0]

ESC[7:0]			Magnification	VDD:3V, 3.3V		VDD:5V		Description
Dec	Hex	Bin	(%)	Output (mV)	Sens. (times)	Output (mV)	Sens. (times)	
0	00	00000000	100	2400	60.0	4800	60.0	Default
1	01	00000001	99.8	2395	59.9	4790	59.9	
2	02	00000010	99.6	2390	59.8	4781	59.8	
3	03	00000011	99.4	2385	59.6	4771	59.6	
4	04	00000100	99.2	2381	59.5	4761	59.5	
:	:	:	:	:	:	:	:	
123	7B	01111011	78.4	1882	47.1	3765	47.1	
124	7C	01111100	78.3	1879	47.0	3757	47.0	
125	7D	01111101	78.1	1875	46.9	3750	46.9	
126	7E	01111110	78	1872	46.8	3743	46.8	
127	7F	01111111	77.8	1868	46.7	3736	46.7	
128	80	10000000	77.7	1864	46.6	3729	46.6	Center
129	81	10000001	77.5	1861	46.5	3721	46.5	
130	82	10000010	77.4	1857	46.4	3714	46.4	
131	83	10000011	77.2	1854	46.3	3707	46.3	
132	84	10000100	77.1	1850	46.3	3700	46.3	
133	85	10000101	76.9	1846	46.2	3693	46.2	
:	:	:	:	:	:	:	:	
251	FB	11111011	61.5	1477	36.9	2954	36.9	
252	FC	11111100	61.4	1474	36.9	2948	36.9	
253	FD	11111101	61.3	1471	36.8	2943	36.8	
254	FE	11111110	61.2	1469	36.7	2937	36.7	
255	FF	11111111	61.1	1466	36.6	2932	36.6	

b.3) Output span voltage fine adjustment (EEPROM name: SC, ESCR[0]=0h)

The output span voltage is adjusted finely.

Address : 02 hex D[7:0] = ESC[7:0]

ESC[7:0]			Magnification	VDD:3V, 3.3V		VDD:5V		
Dec	Hex	Bin	(%)	Output (mV)	Sens. (times)	Output (mV)	Sens. (times)	Description
0	00	00000000	100.0	4000	100.0	8000	100.0	Default
1	01	00000001	99.7	3992	99.7	7983	99.7	
2	02	00000010	99.4	3983	99.5	7968	99.5	
3	03	00000011	99.1	3975	99.2	7952	99.2	
4	04	00000100	98.8	3968	98.8	7935	98.8	
:	:	:	:	:	:	:	:	
123	7B	01111011	71.8	3137	71.8	6275	71.8	
124	7C	01111100	71.6	3132	71.7	6262	71.7	
125	7D	01111101	71.4	3125	71.5	6250	71.5	
126	7E	01111110	71.3	3120	71.3	6238	71.3	
127	7F	01111111	71.1	3113	71.0	6227	71.0	
128	80	10000000	70.9	3107	70.8	6215	70.8	Center
129	81	10000001	70.7	3102	70.7	6202	70.7	
130	82	10000010	70.5	3095	70.5	6190	70.5	
131	83	10000011	70.4	3090	70.3	6178	70.3	
132	84	10000100	70.2	3083	70.2	6167	70.2	
133	85	10000101	70.0	3077	70.0	6155	70.0	
:	:	:	:	:	:	:	:	
251	FB	11111011	52.8	2462	52.8	4923	52.8	
252	FC	11111100	52.7	2457	52.7	4913	52.7	
253	FD	11111101	52.6	2452	52.7	4905	52.7	
254	FE	11111110	52.5	2448	52.5	4895	52.5	
255	FF	11111111	52.3	2443	52.3	4887	52.3	

c) Offset voltage temperature drift, sensitivity temperature drift and output reference voltage adjustment (EEPROM name: OTS, STS, LVS)

When the offset and sensitivity voltage temperature drift and the output reference voltage are adjusted, the adjustment polarity is set.

Address : 03 hex D[4:0] = EOTP[8], EOTN[8], ESTP[8], ESTN[8], ELV[8]

D[4:0]	Symbol	Mode setup
D[4]	ELV[8]	Output reference voltage adjustment polarity setup EEPROM
0	LVM	Subtraction on the basis of 0.5*VDD (default)
1	LVP	Addition on the basis of 0.5*VDD
D[3]	ESTN[8]	Sensitivity temp. drift adjustment polarity setup EEPROM (Low temp. side)
0	STNP	Polarity “+” (default)
1	STNM	Polarity “-“
D[2]	ESTP[8]	Sensitivity temp. drift adjustment polarity setup EEPROM (High temp. side)
0	STPP	Polarity “+” (default)
1	STPM	Polarity “-“
D[1]	EOTN[8]	Offset voltage temp. drift adjustment polarity setup EEPROM (Low temp. side)
0	OTNP	Polarity “+” (EOCF[7] = 0h) (default) Polarity “-“ (EOCF[7] = 1h)
1	OTNM	Polarity “-“ (EOCF[7] = 0h) Polarity “+” (EOCF[7] = 1h)
D[0]	EOTP[8]	Offset voltage temp. drift adjustment polarity setup EEPROM (High temp. side)
0	OTPP	Polarity “+” (EOCF[7] = 0h) (default) Polarity “-“ (EOCF[7] = 1h)
1	OTPM	Polarity “-“ (EOCF[7] = 0h) Polarity “+” (EOCF[7] = 1h)

d) Offset voltage temperature drift adjustment (EEPROM name: OTP, OTN)

The offset voltage temperature drift for the pressure sensor is adjusted, including the AK8999A internal error.
After performing the offset voltage adjustment at 25°C, use the EEPROM's offset voltage temperature characteristic coefficients for adjustment so that the absolute values of the AK8999A's coefficient are matched to those of the sensor's coefficient.

d.1) Offset voltage temperature drift adjustment (EEPROM name: OTP, OTN, EOCF[7] = 0h)

Address : 03 hex D[1:0] = EOTP/N[8], Address :04 hex, 05 hex D[7:0] = EOTP/N[7:0]

EOTP/N[7:0]			Ratio	VDD:3V, 3.3V		VDD:5V		Description
Dec	Hex	Bin	(%)	EOTP/N [8] = 0 (mV/°C)	EOTP/N [8] = 1 (mV/°C)	EOTP/N [8] = 0 (mV/°C)	EOTP/N [8] = 1 (mV/°C)	
0	00	00000000	0.00	0.000	0.000	0.000	0.000	Default
1	01	00000001	0.39	0.072	-0.072	0.144	-0.144	
2	02	00000010	0.78	0.145	-0.145	0.289	-0.289	
3	03	00000011	1.18	0.217	-0.217	0.433	-0.433	
4	04	00000100	1.57	0.289	-0.289	0.577	-0.577	
:	:	:	:	:	:	:	:	
122	7A	01111010	47.84	8.803	-8.803	17.606	-17.606	
123	7B	01111011	48.24	8.876	-8.876	17.751	-17.751	
126	7E	01111110	49.41	9.092	-9.092	18.184	-18.184	
127	7F	01111111	49.80	9.164	-9.164	18.328	-18.328	
128	80	10000000	50.20	9.236	-9.236	18.472	-18.472	
129	81	10000001	50.59	9.308	-9.308	18.616	-18.616	
130	82	10000010	50.98	9.381	-9.381	18.761	-18.761	
131	83	10000011	51.37	9.453	-9.453	18.905	-18.905	
132	84	10000100	51.76	9.525	-9.525	19.049	-19.049	
133	85	10000101	52.16	9.597	-9.597	19.194	-19.194	
:	:	:	:	:	:	:	:	
204	CC	11001100	80.00	14.72	-14.72	29.44	-29.44	
205	CD	11001101	80.39	14.79	-14.79	29.58	-29.58	
:	:	:	:	:	:	:	:	
223	DF	11011111	87.45	16.09	-16.09	32.18	-32.18	
:	:	:	:	:	:	:	:	
236	EC	11101100	92.55	17.029	-17.029	34.058	-34.058	
237	ED	11101101	92.94	17.101	-17.101	34.202	-34.202	
:	:	:	:	:	:	:	:	
255	FF	11111111	100.00	18.400	-18.400	36.800	-36.800	

d.2) Offset voltage temperature drift adjustment (EEPROM name: OTP, OTN, EOCF[7] = 1h)

Address : 03 hex D[1:0] = EOTP/N[8], 04 hex, 05 hex D[7:0] = EOTP/N[7:0]

EOTP/N[7:0]			Ratio	VDD:3V, 3.3V		VDD:5V		Description
Dec	Hex	Bin	(%)	EOTP/N [8] = 1 (mV/°C)	EOTP/N [8] = 0 (mV/°C)	EOTP/N [8] = 1 (mV/°C)	EOTP/N [8] = 0 (mV/°C)	
0	00	00000000	0.00	0.000	0.000	0.000	0.000	Default
1	01	00000001	0.39	0.072	-0.072	0.144	-0.144	
2	02	00000010	0.78	0.145	-0.145	0.289	-0.289	
3	03	00000011	1.18	0.217	-0.217	0.433	-0.433	
4	04	00000100	1.57	0.289	-0.289	0.577	-0.577	
:	:	:	:	:	:	:	:	
122	7A	01111010	47.84	8.803	-8.803	17.606	-17.606	
123	7B	01111011	48.24	8.876	-8.876	17.751	-17.751	
126	7E	01111110	49.41	9.092	-9.092	18.184	-18.184	
127	7F	01111111	49.80	9.164	-9.164	18.328	-18.328	
128	80	10000000	50.20	9.236	-9.236	18.472	-18.472	
129	81	10000001	50.59	9.308	-9.308	18.616	-18.616	
130	82	10000010	50.98	9.381	-9.381	18.761	-18.761	
131	83	10000011	51.37	9.453	-9.453	18.905	-18.905	
132	84	10000100	51.76	9.525	-9.525	19.049	-19.049	
133	85	10000101	52.16	9.597	-9.597	19.194	-19.194	
:	:	:	:	:	:	:	:	
204	CC	11001100	80.00	14.72	-14.72	29.44	-29.44	
205	CD	11001101	80.39	14.79	-14.79	29.58	-29.58	
:	:	:	:	:	:	:	:	
223	DF	11011111	87.45	16.09	-16.09	32.18	-32.18	
:	:	:	:	:	:	:	:	
236	EC	11101100	92.55	17.029	-17.029	34.058	-34.058	
237	ED	11101101	92.94	17.101	-17.101	34.202	-34.202	
:	:	:	:	:	:	:	:	
255	FF	11111111	100.00	18.400	-18.400	36.800	-36.800	

e) Sensitivity temperature drift adjustment (EEPROM name: STP, STN)

The sensitivity temperature drift for the pressure sensor is adjusted, including the AK8999A internal error. After performing the span voltage adjustment at 25ºC, use the EEPROM's sensitivity temperature drift coefficients for adjustment so that the absolute values of the AK8999A's coefficient are matched to those of the sensor's coefficient.

Address : 03 hex D[3:2] = ESTP/N[8], Address : 06 hex, 07 hex D[7:0] = ESTP/N[7:0]

ESTP/N [7:0]			Ratio	VDD:3V, 3.3V		VDD:5V		Description
Dec	Hex	Bin	(%)	ESTP/N [8] = 0 (ppm/°C)	ESTP/N [8] = 1 (ppm/°C)	ESTP/N [8] = 0 (ppm/°C)	ESTP/N [8] = 1 (ppm/°C)	
0	0	00000000	0.00	0	0	0	0	Default
1	1	00000001	0.39	18	-18	18	-18	
2	2	00000010	0.78	36	-36	36	-36	
:	:	:	:	:	:	:	:	
25	19	00011001	9.80	451	-451	451	-451	
26	1A	00011010	10.20	469	-469	469	-469	
27	1B	00011011	10.59	487	-487	487	-487	
28	1C	00011100	10.98	505	-505	505	-505	
:	:	:	:	:	:	:	:	
137	89	10001001	53.73	2471	-2471	2471	-2471	
138	8A	10001010	54.12	2489	-2489	2489	-2489	
139	8B	10001011	54.51	2507	-2507	2507	-2507	
140	8C	10001100	54.90	2525	-2525	2525	-2525	
:	:	:	:	:	:	:	:	
220	DC	11011100	86.27	3969	-3969	3969	-3969	
221	DD	11011101	86.67	3987	-3987	3987	-3987	
222	DE	11011110	87.06	4005	-4005	4005	-4005	
223	DF	11011111	87.45	4023	-4023	4023	-4023	
:	:	:	:	:	:	:	:	
254	FE	11111110	99.61	4582	-4582	4582	-4582	
255	FF	11111111	100.00	4600	-4600	4600	-4600	

f) Output reference voltage adjustment (EEPROM names: LVS, LV)

This EEPROM is used for adjusting the output reference.
The content of the adjustment EEPROMs is shown here.

Address : 03 hex D[4] = ELV[8], Address : 08 hex D[7:0] = ELV[7:0]

ELV[7:0]			VOUT pin (* VDD)		Description
Dec	Hex	Bin	ELV[8]=0	ELV[8]=1	
0	00	00000000	0.500	0.500	Default
1	01	00000001	0.498	0.502	
2	02	00000010	0.496	0.504	
3	03	00000011	0.494	0.506	
4	04	00000100	0.492	0.508	
:	:	:	:	:	
124	7C	01111100	0.252	0.748	
125	7D	01111101	0.250	0.750	
126	7E	01111110	0.248	0.752	
127	7F	01111111	0.246	0.754	
128	80	10000000	0.244	0.756	
:	:	:	:	:	
240	F0	11110000	0.020	0.980	
241	F1	11110001	0.018	0.982	
242	F2	11110010	0.016	0.984	
243	F3	11110011	0.014	0.986	
:	:	:	:	:	
250	FA	11111010	0.000	1.000	
251	FB	11111011	0.000	1.000	
252	FC	11111100	0.000	1.000	
253	FD	11111101	0.000	1.000	
254	FE	11111110	0.000	1.000	
255	FF	11111111	0.000	1.000	

g) Pressure threshold detector 1 (EEPROM name: PTH1, HYS1)

The operating mode, the detection threshold values and the hysteresis voltage of the comparator for the pressure threshold detector 1 are set up.
The detector threshold voltage and the hysteresis voltage vary ratiometrically with respect to the supply voltage.

g.1) Pressure threshold detector operating mode setup

Address : 09 hex D[7:5] = EINV1[0], EINE1[0], EIN1L[0]

D[7:5]	Symbol	Mode setup
D[7]	EINV1[0]	Pressure threshold detector output polarity setup EEPROM
0	EINV11	High output when detected (default)
1	EINV10	Low output when detected
D[6]	EINE1[0]	Pressure threshold detector enabled setup EEPROM
0	INT1E	Pressure threshold detector 1 enable (default)
1	INT1D	Pressure threshold detector 1 disable
D[5]	EIN1L[0]	Pressure threshold detector 1 detection threshold setup EEPROM
0	INT1<	Detect pressure above threshold (default)
1	INT1>	Detect pressure below threshold

Address : 0B hex D[4] = EPTH1[0]

D[4]	Symbol	Mode setup
D[4]	EPTH1[0]	Pressure threshold detector 1 detection threshold selection EEPROM
0	PTH1R	EEPROM setup (default)
1	PTH1E	DET2/PTH pin external setup

g.2) Pressure threshold detector detection threshold adjustment

Address : 09 hex D[4:0] = EPT1[4:0]

EPT1[4:0]			Detection threshold (V)		Description
Dec	Hex	Bin	Detect threshold	ex. VDD:5V	
-16	10	10000	0.900*VDD	4.500	
-15	11	10001	0.875*VDD	4.375	
-14	12	10010	0.850*VDD	4.250	
:	:	:	:	:	
-3	1D	11101	0.575*VDD	2.875	
-2	1E	11110	0.550*VDD	2.750	
-1	1F	11111	0.525*VDD	2.625	
0	00	00000	0.500*VDD	2.500	Default
1	01	00001	0.475*VDD	2.375	
2	02	00010	0.450*VDD	2.250	
:	:	:	:	:	
14	0E	01110	0.150*VDD	0.750	
15	0F	01111	0.125*VDD	0.625	

g.3) Comparator hysteresis voltage adjustment for pressure threshold detection

Address : 0B hex D[1:0] = EHYS1[1:0]

EHYS1[1:0]			Hysteresis voltage (mV)		Description
Dec	Hex	Bin	Hysteresis voltage	ex. VDD:5V	
2	2	10	0.030*VDD	150.0	
3	3	11	0.040*VDD	200.0	
0	0	00	0.050*VDD	250.0	Default
1	1	01	0.060*VDD	300.0	

h) Pressure threshold detector 2 (EEPROM name: PTH2, HYS2)

The operating mode, the detection threshold values and the hysteresis voltage of the comparator for the pressure threshold detector 2 are set up.
The detector threshold voltage and the hysteresis voltage vary ratiometrically with respect to the supply voltage.

h.1) Pressure threshold detector operating mode setup

Address : 0A hex D[7:5] = EINV2[0], EINE2[0], EIN2L[0]

D[7:5]	Symbol	Mode setup
D[7]	EINV2[0]	Pressure threshold detector output polarity setup EEPROM
0	EINV21	High output when detected (default)
1	EINV20	Low output when detected
D[6]	EINE2[0]	Pressure threshold detector enabled setup EEPROM
0	INT2E	Pressure threshold detector 2 enable (default)
1	INT2D	Pressure threshold detector 2 disable
D[5]	EIN2L[0]	Pressure threshold detector 2 detection threshold setup EEPROM
0	INT2<	Detect pressure above threshold (default)
1	INT2>	Detect pressure below threshold

h.2) Pressure threshold detector detection threshold adjustment

Address : 0A hex D[4:0] = EPT2[4:0]

EPT2[4:0]			Detection threshold (V)		Description
Dec	Hex	Bin	Detect threshold	ex. VDD:5V	
-16	10	10000	0.900*VDD	4.500	
-15	11	10001	0.875*VDD	4.375	
-14	12	10010	0.850*VDD	4.250	
:	:	:	:	:	
-3	1D	11101	0.575*VDD	2.875	
-2	1E	11110	0.550*VDD	2.750	
-1	1F	11111	0.525*VDD	2.625	
0	00	00000	0.500*VDD	2.500	Default
1	01	00001	0.475*VDD	2.375	
2	02	00010	0.450*VDD	2.250	
:	:	:	:	:	
13	0D	01101	0.175*VDD	0.875	
14	0E	01110	0.150*VDD	0.750	
15	0F	01111	0.125*VDD	0.625	

h.3) Comparator hysteresis voltage adjustment for pressure threshold detection

Address : 0B hex D[3:2] = EHYS2[1:0]

EHYS2[1:0]			Hysteresis voltage (mV)		Description
Dec	Hex	Bin	Hysteresis voltage	ex. VDD:5V	
2	2	10	0.030*VDD	150.0	
3	3	11	0.040*VDD	200.0	
0	0	00	0.050*VDD	250.0	Default
1	1	01	0.060*VDD	300.0	

i) Input gain adjustment (EEPROM name: ING)

This EEPROM is used for setting the total gain.
The input gain is adjusted according to the full-scale voltage of the pressure sensor.

Address : 0C hex D[4:0] = EIG[4:0]

EIG[3:0]			G1 Gain (times)	G1*G2 Gain (times)		Description
Dec	Hex	Bin		EIG[4]=0 G2: 3x	EIG[4]=1 G2: 1.5x	
0	0	0000	70.0	210.0	105.0	Default
1	1	0001	60.0	180.0	90.0	
2	2	0010	50.0	150.0	75.0	
3	3	0011	40.0	120.0	60.0	
4	4	0100	35.0	105.0	52.5	
5	5	0101	30.0	90.0	45.0	
6	6	0110	25.0	75.0	37.5	
7	7	0111	20.0	60.0	30.0	
8	8	1000	15.0	45.0	22.5	
9	9	1001	12.0	36.0	18.0	
10	A	1010	10.0	30.0	15.0	
11	B	1011	7.0	21.0	10.5	
12	C	1100	5.0	15.0	7.5	
13	D	1101	Setup prohibited	Setup prohibited	Setup prohibited	
14	E	1110				
15	F	1111				

j) Measurement mode setup (EEPROM name: MM1, MM2)

This EEPROM is used for setting up the measurement mode for the AK8999A.
A setup of a sampling frequency, supply voltage & sensor drive voltage, the enable / disable of Internal SCF & SMF, the internal / external of a temperature sensor, the internal switching of VP & VN, and the initial state of VOUT pin at power-up can be performed.

Address : 0D hex D[7:0] = ESCF[1:0], EVD[1:0], ESF[0] , EVPN[0], ETMP[1:0]

D[7:0]	Symbol	Mode setup
D[7]	EVPN[0]	VP & VN internal switching EEPROM
0	VPNN	VP->VP, VN->VN (default)
1	VPNR	VP->VN, VN->VP
D[6:5]	ETMP[1:0]	Temperature sensor Internal & External change EEPROM
00	TMPESi	External temperature sensor use & Drive sink current (default)
01	TMPESo	External temperature sensor use & Drive source current
10	TMPI	Internal temperature sensor use
11	Reserved	Setup prohibited
D[4:3]	ESCF[1:0]	Internal SCF & SMF setup EEPROM
00	SCDS	Internal SCF & SMF disable (default)
01	SCEN1	Internal SCF & SMF enable & Cutoff frequency 1kHz
10	SCEN2	Internal SCF & SMF enable & Cutoff frequency 500Hz
11	SCEN3	Internal SCF & SMF enable & Cutoff frequency 250Hz
D[2:1]	EVD[1:0]	Supply voltage & sensor drive voltage setup EEPROM
00	VDD302	Supply voltage at 3V & sensor drive voltage at 2.2V (default)
01	VDD332	Supply voltage at 3.3V & sensor drive voltage at 2.2V
10	VDD502	Supply voltage at 5V & sensor drive voltage at 2.2V
11	VDD504	Supply voltage at 5V & sensor drive voltage at 4V
D[0]	ESF[0]	Sampling frequency setup EEPROM
0	SF11	Sampling frequency 8.33kHz (default)
1	SF1	Sampling frequency 0.83kHz

Address : 0E hex D[1:0] = EVOUT[1:0]

D[1:0]	Symbol	Mode setup
D[1:0]	EVOUT[1:0]	Initial state of VOUT pin at power-up setup EEPROM
00	STVSS	VSS set at power-up (default)
01	STVDD	VDD set at power-up
10	ST1/2VDD	0.5*VDD set at power-up
11	Reserved	Setup prohibited

k) VREF voltage adjustment (EEPROM name: VREF)

This EEPROM is used for adjusting the AK8999A reference voltage. Perform an adjustment to attain the reference voltage of 1000mV (See "**Recommended External Circuits**").
ΔVREF3/5 in the table below indicates a value varying with the setup values of the EEPROM.
ΔVS3/5 represents the values of ΔVREF3/5 multiplied by two and four, respectively. The ratio in the table below is benchmarked to 1000mV (VREF ideal value) as 100%
(Ratio = (ΔVREF3/5) /1000[mV]*100[%]).

Address : 0F hex D[2:0] = EVR[2:0]

EVR[2:0]			Ratio	VDD:3V, 3.3V mode		VDD:5V		Description
Dec	Hex	Bin	(%)	ΔVREF3 (mV)	ΔVS3 (mV)	ΔVREF5 (mV)	ΔVS5 (mV)	
-4	4	100	-4	-40	-80	-40	-160	
-3	5	101	-3	-30	-60	-30	-120	
-2	6	110	-2	-20	-40	-20	-80	
-1	7	111	-1	-10	-20	-10	-40	
0	0	000	0	0	0	0	0	Default
1	1	001	1	+10	+20	+10	+40	
2	2	010	2	+20	+40	+20	+80	
3	3	011	3	+30	+60	+30	+120	

l) IREF current adjustment (EEPROM name: IREF)

This EEPROM is used for adjusting the AK8999A reference current. The external resistor (1MΩ) is connected to VOUT pin. The reference current is adjusted so that the voltage droped by external resistor may be set to 1.0V. (See "**Recommended External Circuits**").
IREF in the table below indicates a current value with the setup values of the EEPROM.
VIREF (=IREF*1[MΩ]) is a voltage value varying with the external resistance (1MΩ) at the time of adjustment. The ratio is benchmarked to 1.0μA (IREF ideal value) as 100%
(Ratio = (IREF-1.0 [μA])/1.0 [μA]*100[%]).

Address : 0F hex D[7:4] = EIR[3:0]

EIR[3:0]			Ratio	IREF	VIREF	Description
Dec	Hex	Bin	(%)	(μA)	(V)	
-8	8	1000	-17.0	0.830	0.830	
-7	9	1001	-15.2	0.848	0.848	
-6	A	1010	-13.4	0.866	0.866	
-5	B	1011	-11.5	0.885	0.885	
-4	C	1100	-9.5	0.905	0.905	
-3	D	1101	-7.3	0.927	0.927	
-2	E	1110	-5.0	0.950	0.950	
-1	F	1111	-2.6	0.974	0.974	
0	0	0000	0.0	1.000	1.000	Default
1	1	0001	2.8	1.028	1.028	
2	2	0010	5.7	1.057	1.057	
3	3	0011	8.8	1.088	1.088	
4	4	0100	12.2	1.122	1.122	
5	5	0101	15.9	1.159	1.159	
6	6	0110	19.8	1.198	1.198	
7	7	0111	24.1	1.241	1.241	

m) OSC frequency adjustment (EEPROM name: OSC)

This EEPROM is used for adjusting the AK8999A operation clock. Perform an adjustment to attain a frequency of 1000kHz. Reading the ratio data from the OSC variable ratio storing register (Register name: CM2), the adjustment data of the OSC frequency adjustment EERPOM is calculated.
Frequency Δf in the table below indicates a value varying with the setup values of the EEPROM. The ratio is benchmarked to 1000kHz (OSC ideal value) as 100%
(Ratio = Frequency Δf/(Frequency Δf+1000[kHz])*100[%]).

Address : 10 hex D[3:0] = EFR[3:0]

EFR[3:0]			Ratio	FrequencyΔf	Description
Dec	Hex	Bin	(%)	(kHz)	
-5	B	1011	-34	-251	
-4	C	1100	-25	-197	
-3	D	1101	-17	-146	
-2	E	1110	-11	-99	
-1	F	1111	-5	-52	
0	0	0000	0	0	Default
1	1	0001	5	49	
2	2	0010	10	106	
3	3	0011	14	162	
4	4	0100	18	224	
5	5	0101	22	274	
6	6	0110	25	329	
7	7	0111	28	384	

Note) Hex 8 to A are prohibited for setup.

n) VTMP voltage adjustment (EEPROM name: VTMP)

Compensates the offset values for the AK8999A's internal temperature sensor and external temperature sensor. Adjusts the values so that the difference between VTMP voltage and VREF voltage is close to 0 mV (If VREF is 1005mV, adjust so that VTMP is also 1005mV).
The coarse adjustment (ETM[8:6]) is invalid when the internal temperature sensor is used (ETMP[1:0] = 2h). The coarse adjustment is effective when the external temperature sensor is used (ETMP[1:0] = 0, 1h).
ΔVTMP in the table below indicates a value varying with the setup values of the EEPROM. The ratio is benchmarked to 1000mV (VREF ideal value) as 100% (Ratio = ΔVTMP/1000[mV]*100[%]).

Address : 11 hex D[5:0] = ETM[5:0]

ETM[5:0]			Ratio	ΔVTMP	Description
Dec	Hex	Bin	(%)	(mV)	
-32	20	100000	+6.4	+64	
:	:	:	:	:	
-16	30	110000	+3.2	+32	
:	:	:	:	:	
-8	38	111000	+1.6	+16	
:	:	:	:	:	
-4	3C	111100	+0.8	+8	
:	:	:	:	:	
-1	3F	111111	+0.2	+2	
0	00	000000	0.0	0	Default
1	01	000001	-0.2	-2	
:	:	:	:	:	
4	04	000100	-0.8	-8	
:	:	:	:	:	
8	08	001000	-1.6	-16	
:	:	:	:	:	
16	10	010000	-3.2	-32	
:	:	:	:	:	
31	1F	011111	-6.2	-62	

Address : 10 hex D[6:4] = ETM[8:6]

ETM[8:6]			Ratio	ΔVTMP	Description
Dec	Hex	Bin	(%)	(mV)	
4	4	100	Setup prohibited	Setup prohibited	
5	5	101	Setup prohibited	Setup prohibited	
6	6	110	+20.0	+200	
7	7	111	+10.0	+100	
0	0	000	0.0	0	Default
1	1	001	-10.0	-100	
2	2	010	-20.0	-200	
3	3	011	Setup prohibited	Setup prohibited	

o) User-writable data space (EEPROM name: UE)

Free area (EEPROM) available to the user.

Address : 12 hex D[7:0] = EUE[7:0]

Name	Content	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
UE	User-writable data	EUE7	EUE6	EUE5	EUE4	EUE3	EUE2	EUE1	EUE0
Default		0	0	0	0	0	0	0	0

p) Control register access setup (EEPROM name: MM3)

The access setup to the control register (volatile memory) is performed.
When the control register access setup is disabled (ETST[0] = 0h), the control register (C address: 0h) is fixed to the initial value, and cannot be accessed, unless control register access is validated.

Address : 1D hex D[0] = ETST[0]

D[0]	Symbol	Mode setup
D[0]	ETST[0]	Control register access setup
0	TSTDS	Control register access disable(default)
1	TSTEN	Control register access enable

q) EEPROM Write Enable setup (EEPROM name: EWE)

The EEPROM write enable setup is performed.
When the setup of EEPROM Write Enable is validated (EWE[0] = 1h), the writing to EEPROM is permitted. If it is invalid, the writing to EEPROM other then EEPROM Write Enable (address: 00 -1Dh, 1Fh) becomes impossible. And this address cannot be written by batch writing. However, EEPROM read (all the addresses) is possible even in that case.

Address : 1E hex D[0] = EWE[0]

D[0]	Symbol	Mode setup
D[0]	EWE[0]	EEPROM Write Enable setup
0	WEDS	EEPROM Write disable (default)
1	WEEN	EEPROM Write enable

r) EEPROM batch write mode (EEPROM name: AW)

Initializes the addresses 00 hex to 1D hex in the EEPROM map at once or writes identical data. This address is not available in the EEPROM.

Address : 1F hex D[7:0] = EAW[7:0]

Name	Content	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
AW	EEPROM batch write	EAW7	EAW6	EAW5	EAW4	EAW3	EAW2	EAW1	EAW0

6.2) Description of Control Register (Volatile Memory)

a) Adjustment mode (Register name: CM1)

This register is used to adjust the AK8999A reference voltage and pressure sensor's offset, span, offset temperature drift and sensitivity temperature drift including those of the AK8999A.
In addition, the value of the register returns to the initial value on the following conditions.

- At the power up
- When CSCLK = Low is maintained 0.5msec or more
- When ETST[0] is set to "L"

Address : 00 hex D[3:0] = AM[3:0]
(This is not a nonvolatile EEPROM, but a volatile register.)

D[7:0]	Symbol	Mode setup	Description
D[7:4]		Reserved	Setup prohibited
D[3:0]	AM[3:0]	IC adjustment mode	
0000			(default)
0001	AVR	VREF adjustment	The VREF voltage is output at the VOUT pin.
0010	AIR	IREF adjustment	The IREF current is output at the VOUT pin.
0011	AFR	OSC adjustment	Input the fixed period of High level (2.0msec) from the CSCLK pin. The count value in the internal counter is stored in the register.
0100	ATO	VTMP adjustment	The VTMP voltage is output at the VOUT pin. Adjust this voltage so that it matches the VREF voltage at 25°C.
0101	ADT1	judge threshold 1 adjustment	The internally set judge threshold value 1 is output at the VOUT pin.
0110	ADT2	judge threshold 2 adjustment	The internally set judge threshold value 2 is output at the VOUT pin.
0111	AHY1	hysteresis voltage 1	The hysteresis voltage of the comparator 1 is output at the VOUT pin.
1000	AHY2	hysteresis voltage 2	The hysteresis voltage of the comparator 2 is output at the VOUT pin.
1001	ALV	Output reference voltage adjustment	The output reference voltage is output at the VOUT pin.
1001-1111		Reserved	Setup prohibited

b) OSC variable ratio storing register (Register name: CM2)

This register is used for adjustment of the oscillator frequency of AK8999A. The counted value in the internal counter is stored. Since the internal counter is overflowing when a count value shows FF hex, measure again by re-defining High level period.
This register is read only. In addition, the value of the register returns to the initial value on the following conditions.

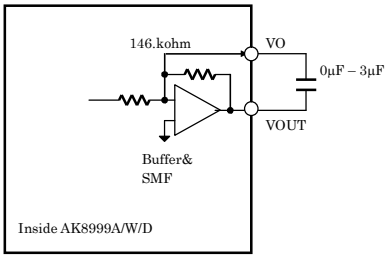
- At the power up
- When CM1 register is written
- When CSCLK = Low is maintained 0.5msec or more
- When ETST[0] is set to "L"

Address : 01 hex D[7:0] = CT[7:0]
(This is not a nonvolatile EEPROM, but a volatile register.)

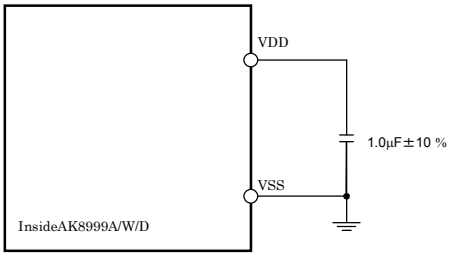
CT[7:0]			Count value	Ratio	Description
Dec	Hex	Bin	(time)	(%)	
0	00	00000000	0	0	Default
1	01	00000001	1	-99	
:	:	:	:	:	
98	62	01100010	98	-2	
99	63	01100011	99	-1	
100	64	01100100	100	0	Ideal value
101	65	01100101	101	1	
102	66	01100110	102	2	
:	:	:	:	:	
254	FE	11111110	254	154	
255	FF	11111111	-	-	Counter error

17. Recommended External Circuits

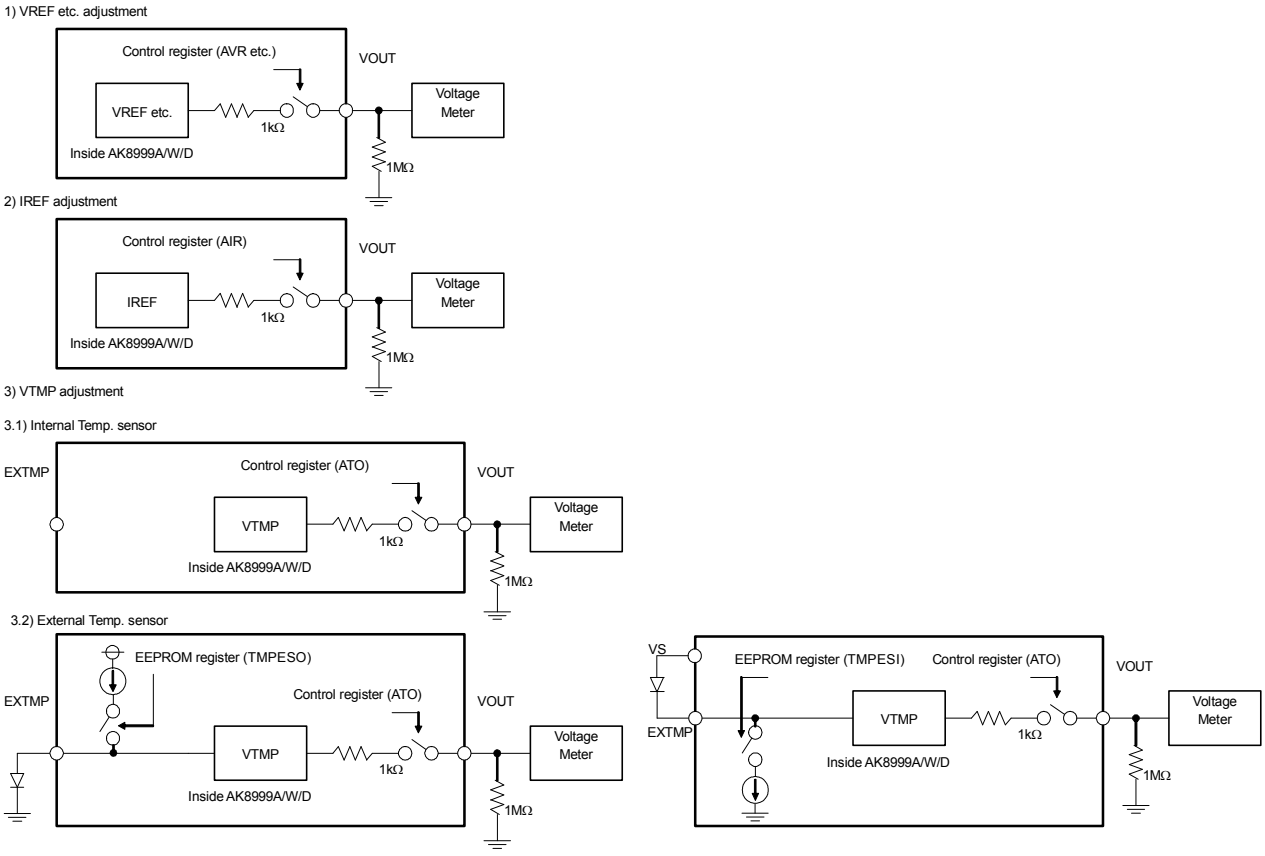
1) VO pin connection example



2) Power supply pin connection example



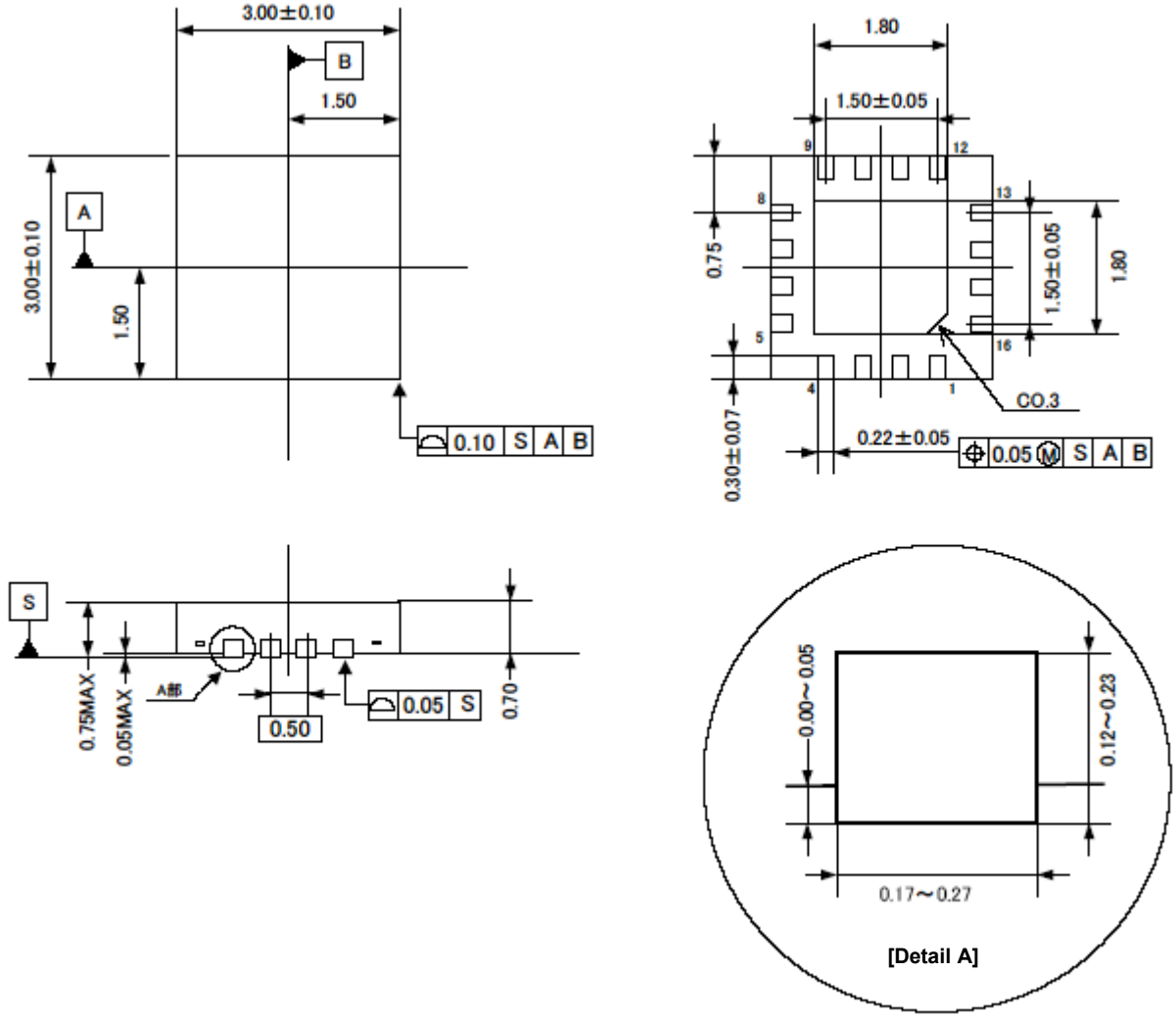
3) VOUT pin connection examples for adjustment



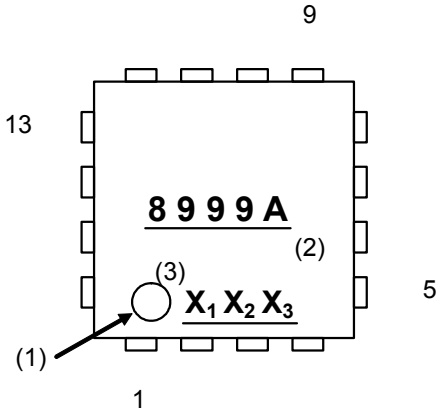
18. Package

1) Outline Dimensions

The rear-side TAB is recommended to be mounted on the substrate to ensure strength. Do not connect to the power supply, GND or any signal.



2) Marking



(1) Pin Number 1 indication mark

(2) Part Number

(3) Date Code (3 digits)

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