# LittleBoard™ 800
# Single Board Computer
# Reference Manual

**P/N 5001743A  Revision A**

## Notice Page

**NOTICE**



**DISCLAIMER**

Ampro Computers, Incorporated makes no representations or warranties with respect to the contents of this manual or of the associated Ampro products, and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose. Ampro shall under no circumstances be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damages. Ampro reserves the right to revise this publication from time to time without obligation to notify any person of such revisions. If errors are found, please contact Ampro at the address listed below on the Notice page of this document.

**TRADEMARKS**



**REVISION HISTORY**

| Revision | Reason for Change | Date |
|---|---|---|
| A, A | Initial Release | May/05 |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

Ampro Computers, Incorporated
5215 Hellyer Avenue
San Jose, CA 95138-1007
Tel. 408 360-0200
Fax 408 360-0222
www.ampro.com



## Audience Assumptions

This reference manual is for the person who designs computer related equipment, including but not limited to hardware and software design and implementation of the same. Ampro Computers, Inc. assumes you are qualified in designing and implementing your hardware designs and its related software into your prototype computer equipment.

# Contents

**List of Figures**

**List of Tables**

# Chapter 1 About This Manual

## Purpose of this Manual

This manual is for designers of systems based on the LittleBoard™ 800 single board computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

**Information provided** in this reference manual includes:

- LittleBoard 800 Specifications
- Environmental requirements
- Major integrated circuits (chips) and features implemented
- LittleBoard 800 connector/pin numbers and definition
- BIOS Setup information

**Information not provided** in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

## Reference Material

The following list of reference materials may be helpful for you to complete your design successfully. Most of this reference material is also available on the Ampro web site in the Embedded Design Resource Center. The Embedded Design Resource Center was created for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience.

**Specifications**

- EBX Spec Revision 1.1, July 1997 2003

  For the latest version of the EBX specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org

- PC/104 Spec Revision 2.5, November 2003
- PC/104-Plus Spec Revision 2, November 2003

  For latest revision of the PC/104 specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org

- PCI 2.3 Compliant Specifications

  For latest revision of the PCI specifications, contact the PCI Special Interest Group Office at:

  Web site: http://www.pcisig.com

**Chip specifications** used on the LittleBoard 800:

- Intel Corporation and the Celeron M or Pentium M processors used for the embedded CPU.

  Web site: http://www.intel.com/design/mobile/datashts/252612.htm = Pentium M

  Web site: http://www.intel.com/design/intarch/datashts/301753.htm = Celeron M

- Intel Corporation and the chips, 82855GME and 82801DBM, used for the Memory Hub/Video controller and I/O Hub respectively.

  Web site: http://www.intel.com/design/chipsets/mobile/855gme.htm = Memory Hub

  Web site: http://www.intel.com/design/mobile/datashts/252337.htm = I/O Hub

- Intel Corporation and the chips, 82551ER and 82541(GI/PI), used for the Ethernet controllers respectively.

  Web site: http://www.intel.com/design/network/datashts/82551ER_ds.htm = Ethernet

  Web site: http://www.intel.com/design/network/datashts/82541gi_ei.htm = Gigabit Ethernet

- Standard Microsystems Corp and the chip, LPC47B272, used for both Super I/O controllers.

  Web site: http://www.smsc.com/main/catalog/lpc47b27x.html

- Realtek and the chip ALC202A, used for the Audio CODEC.

  Web site: http://w3serv.realtek.com.tw/products/products1-1.aspx?lineid=5

# Related Ampro Products

The following items are directly related to successfully using the Ampro product you have just purchased or plan to purchase. Ampro highly recommends that you purchase and utilize a LittleBoard 800 QuickStart Kit or Development System.

**LittleBoard 800 Support Products**

- LittleBoard 800 QuickStart Kit (QSK)

  The QuickStart Kit includes the LittleBoard 800, RAM, an I/O interface board, a cable kit, documentation, and drivers for the unique devices used with Ampro supported operating systems.

- LittleBoard 800 Development System

  The Development System is a benchtop system, which provides a “known good” environment for your development work. The Development System provides an integrated and easy-to-use self-hosted development environment that lets you maximize the benefit of using an off-the-shelf board as the basis of your embedded system design. You can install ISA bus or PCI bus expansion boards on the Development System chassis. The Development System is arranged to make all the components of your system accessible. Refer to Ampro's web site or the LittleBoard 800 Development System Users Guide on the LittleBoard 800 Documentation and Support Software (Doc & SW) CD-ROM for more information.

- LittleBoard 800 Documentation and Support Software CD-ROM

  The LittleBoard 800 Documentation and Support Software (Doc & SW) CD-ROM is provided with the LittleBoard 800 QuickStart Kit and the LittleBoard 800 Development System. The CD-ROM includes all of the LittleBoard 800 documentation in PDF format, including this reference manual, the LittleBoard 800 QuickStart Guide, the LittleBoard 800 Development System Users Guide, software utilities, Operating System (OS) Board Support Packages (BSPs), and drivers.

**Other LittleBoard Products**

- LittleBoard™ 550 – This EBX single board computer (SBC) is a highly integrated, high performance, rugged, high quality system based on the Via Eden™ 1GHz ESP 10000, 533MHz ESP 5000, or 300MHz ESP 3000 CPUs. In addition to the standard LittleBoard features (EBX form factor, PC/104 & PC/104-Plus interfaces, +5 volt power, watchdog timer, serial console, etc.), the LittleBoard 550 supports up to four EIDE Ultra DMA 33/66/100 IDE drives including a CompactFlash™ socket, two floppy disk drives, one ECP/EPP parallel port, four RS232/422/485 serial ports, four USB V1.1 ports, two Ethernet ports, IrDA, AC'97 audio interface, and PS/2 keyboard & serial mouse. It also supports Ampro BIOS extensions for OEM boot customization, power management features, up to 1GB of SDRAM in a DIMM slot, up to 32MB UMA of AGP 4X video with built-in LVDS, CRT, and 36-bit TFT support.

- LittleBoard™ 700 – This EBX single board computer (SBC) is a highly integrated, high performance, rugged, high quality system based on Intel's 933MHz Low Voltage Pentium® III, 650MHz Low Voltage Celeron®, or 400MHz Ultra Low Voltage Celeron processors. In addition to the standard LittleBoard features (EBX form factor, PC/104 & PC/104-Plus interfaces, +5 volt power, watchdog timer, serial console, etc.), the LittleBoard 700 supports up to four EIDE Ultra DMA 33/66/100 IDE drives including a CompactFlash™ socket, two floppy disk drives, one ECP/EPP parallel port, four RS232/422/485 serial ports, four USB V1.1 ports, two Ethernet ports, IrDA, AC'97 audio interface, and PS/2 keyboard & serial mouse. It also supports Ampro BIOS extensions for OEM boot customization, power management features, up to 1GB of SDRAM in a DIMM slot, up to 32MB UMA of AGP 4X video with built-in LVDS, CRT, and 36-bit TFT support.

**Other Ampro Products**

- CoreModule™ Family – These complete embedded-PC subsystems on single PC/104 or PC/104-Plus form-factor (3.6” x 3.8” inches) modules feature 486, VIA Eden, Celeron®, and Celeron M CPUs. Each CoreModule includes a full complement of PC core logic functions, plus disk controllers, and serial and parallel ports. Most modules also include CRT and flat panel graphics controllers and an Ethernet interface. The CoreModules also come with built-in extras to meet the critical reliability requirements of embedded applications. These include onboard solid state disk compatibility, watchdog timer, smart power monitor, and other embedded-PC BIOS extentions.

- MiniModule™ Family – This extensive line of peripheral interface modules compliant with PC/104 and PC/104-Plus can be used with Ampro CoreModule and LittleBoard single-board computers to configure embedded system solutions. Ampro's highly reliable MiniModule products currently support USB 2.0, IEEE 1394 (FireWire™), Ethernet, PC Card expansion, analog/data acquisition, additional RS232/RS485 serial ports, and general-purpose I/O (GPIO).

- MightyBoard™ Family – These low-cost, high-performance single-board computers (SBC) use the Mini-ITX form factor (6.7" x 6.7") and are available with Intel® processors, including Pentium M. MightyBoard products offer the equivalent functions of a complete laptop or desktop PC system, including DDR memory, high performance graphics, USB 2.0, Gigabit Ethernet, plus standard PCI expansion capability in one card slot. Ampro includes configuration control and embedded BIOS extension such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.

- ReadyBoard™ Family – These low-cost, high-performance single-board computers (SBC) use the EPIC form factor (4.5” x 6.5”) and are available with the VIA Eden™, Intel Pentium® III, Intel Celeron®, and Pentium M and Celeron M processors. ReadyBoard products offer functions equivalent to a complete laptop or desktop PC system, plus several expansion cards. Ampro includes configuration control and embedded BIOS extension such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.

- ReadySystem™ – This complete, low cost, turn-key system gives you a choice of ReadyBoard high performance, low power, SBCs with RAM installed plus a hard disk drive (HDD) pre-loaded with a choice of operating systems powered by a 150W ATX power supply. Each ReadySystem provides standard peripherals, including video, serial, parallel, PS/2 keyboard and mouse interfaces, Ethernet and USB ports, and sound available through the front I/O panel. A CompactFlash socket is accessible through a protective cover and two optional PC/104 modules can be accessed through panel cutouts for PC/104 expansion I/O.
- ETX Family – These high-performance, compact Computer-on-Module (COM) solutions use various x86 processors from VIA Eden ESP to Pentium M CPUs in an ETX form factor to plug into your custom baseboard. Each ETX module provides standard peripherals, including dual Ultra/DMA 33/66/100 IDE, floppy drive interface, PCI bus, ISA bus, serial, parallel, PS/2 keyboard and mouse interfaces, 10/100BaseT Ethernet, USB ports, Video, and AC'97 sound. Optional –40°C to +85°C operation is available to meet your application requirements.
- EnCore™ Family - These high-performance, compact, Computer-on Module (COM) solutions use various processor technologies including Intel x86, MIPS, and PowerPC architectures to plug into your custom baseboard. Each EnCore module provides standard peripherals, including Ultra/DMA 33/66/100 IDE, floppy drive interface, PCI bus, serial, parallel, PS/2 keyboard and mouse interfaces, 10/100BaseT Ethernet, and USB ports. Some EnCore modules also provide video and AC'97 sound. Depending on the model, EnCore modules support up to 256MB or 512MB of SODIMM DRAM.

# Chapter 2 Product Overview

This introduction presents general information about the EBX Architecture and the LittleBoard 800 single board computer (SBC). After reading this chapter you should understand:

- EBX Architecture
- LittleBoard 800 architecture
- LittleBoard 800 features
- Major components
- Connectors
- Specifications

## EBX Architecture

The "Embedded Board, eXpandable" (EBX) standard is the result of a collaboration between industry leaders, Motorola and Ampro, to unify the embedded computing industry on a full featured embedded single-board computer (SBC) standard. The EBX standard principally defines physical size, mounting hole pattern, and power connector locations. It does not specify processor type or electrical characteristics. There are recommended connector placements for serial/parallel, Ethernet, graphics, and memory expansion.

Derived from the Ampro LittleBoard™ form-factor originated in 1984, EBX combines a standard footprint with open interfaces. The EBX form-factor is small enough for deeply embedded applications, yet large enough to contain the functions of a full embedded SBC (single board computer) including CPU, memory, mass storage interfaces, display controller, serial/parallel ports, today's advanced operating systems, and other system functions. This embedded SBC standard ensures that embedded system OEMs can standardize their designs and that embedded computing solutions can be designed into space constrained environments with off-the-shelf components.

The EBX standard boasts highly flexible and adaptable system expansion, allowing easy and modular addition of functions such as additional USB 2.0 ports, Firewire or wireless networking not usually contained in standard product offerings. The EBX system expansion is based on popular existing industry standards, PC/104™ and PC/104-Plus™. PC/104 places the ISA bus on compact 3.6" x 3.8" modules with self-stacking capability. PC/104-Plus adds the power of a PCI bus to PC/104 while retaining the basic form-factor. Using PC/104 expansion cards, the PCMCIA standard offers access to PC Cards from the mobile and handheld computing markets.

The EBX standard integrates all these off-the-shelf standards into a highly embeddable SBC form-factor. EBX supports the legacy of PC/104, hosting the wide variety of embedded system oriented expansion modules from hundreds of companies worldwide. PCMCIA brings the advantages of the latest portable and mobile system expansion technologies to embedded applications. See Figure 2-1.

The EBX standard also brings stability to the embedded board market and offers OEMs assurance that a wide range of products will be available from multiple sources – now and in the future. The EBX standard is open to continuing technology advancements, since it is both processor and payload independent. It creates opportunity for economies of scale in chassis, power supply, and peripheral devices.

The EBX specification is freely available to all interested. For further technical information on the EBX standard, go to the PC/104 Consortium web site at www.pc104.org.

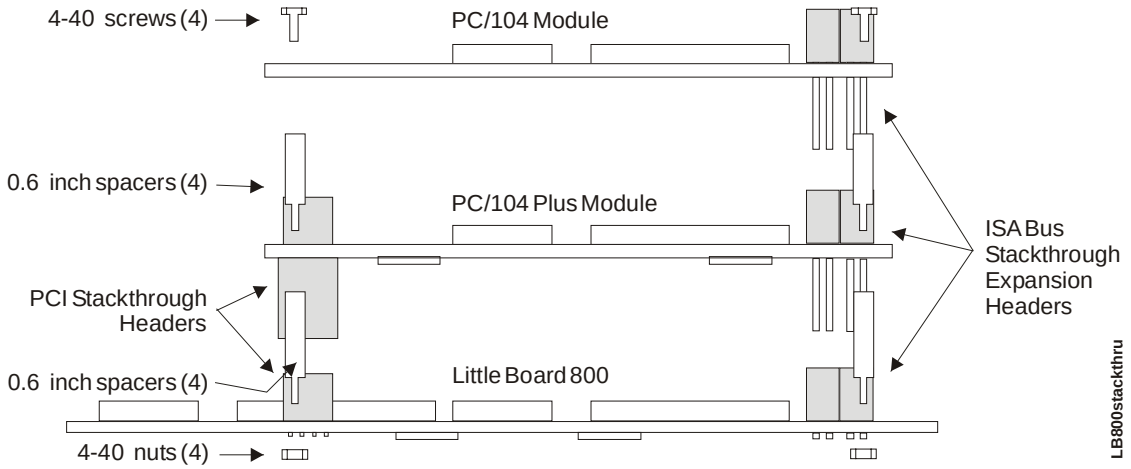



**Figure 2-1. Stacking PC/104 Modules with the LittleBoard 800**

# Product Description

The LittleBoard 800 is an exceptionally high integration, high performance, rugged, and high quality single-board system, which contains all the component subsystems of a PC motherboard plus the equivalent of up to 3 expansion boards. Based on the Intel Pentium® M and Celeron® M ultra high performance, high-integration processor, the LittleBoard 800 gives designers a complete, high performance embedded processor based on the EBX form factor and conforms to the EBX V1.1 specifications.

Each LittleBoard 800 incorporates a Intel 855GME chipset for the Graphics and Memory Hub (Northbridge) and the I/O Hub (Southbridge) controllers. This set includes the 82855GME, Graphics and Memory Controller Hub, (also GMCH), which controls the graphics and memory interface. The other chip in this set is the 82801DBM, I/O Controller Hub 4 Mobile (also ICH4-M), which controls some of the I/O functions on the board. There are two additional chips that provide the reminder of the I/O functions, specifically, the Standard Microsystems, LPC47B272, Super I/O controllers. Together the Intel and SMSC chips provides four serial ports, a EPP/ECP parallel port, four USB 2.0 ports, PS/2 keyboard and mouse interfaces, floppy and two Ultra/DMA 33/66/100 IDE controllers supporting two IDE drives each, independent 10/100BaseT and 10/100/1000BaseT Ethernet interfaces, and an audio AC'97 CODEC on the board. To provide the ISA bus on the board through the PC/104 connector, an ITE, IT8888F, PCI-to-ISA Bridge is included. The LittleBoard 800 also supports up to 1GB of DDR RAM in a single 184-pin DDR DIMM slot, and an AGP4x equivalent graphics controller, which provides CRT and LVDS flat panel video interfaces for most popular LCD panels.

The LittleBoard 800 can be expanded through the PC/104 and PC/104-Plus expansion for additional system functions, as these buses offer compact, self-stacking, modular expandability. The PC/104 and PC/104-Plus buses are the embedded system version of the signal set provided on a desktop PC's ISA and PCI buses at 8MHz and 33MHz clock speeds respectively.

Among the many embedded-PC enhancements on the LittleBoard 800 that ensure embedded system operation and application versatility are a watchdog timer, serial console support, battery-free boot, on-board high-density CompactFlash disk, and BIOS extensions for OEM boot customization.

The LittleBoard 800 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with Ampro MiniModules™ or other PC/104-compliant expansion boards, or it can be used as powerful computing engine. The LittleBoard 800 requires a single +5V power supply.

## Board Features

- CPU features
  - Intel 1.4GHz LV, Pentium® M 738, 1.0GHz ULV Celeron M 373, or 600MHz ULV Celeron M Processors
  - 2MB (Pentium) or 512KB (Celeron) L2 cache
  - 400MHz FSB
- Memory
  - Single standard 184-pin DDR DIMM slot
  - Supports non-ECC or unbuffered ECC memory
  - Supports +2.5V DDR RAM up to 1GB
  - Supports up to PC2700 DDR 333 (166MHz)
- PC/104-Plus Bus Interfaces
  - PCI Bus up to 33MHz
  - PCI 2.2 compliant signals
  - PC/104 (ISA) Bus up to 8MHz
- IDE Interfaces
  - Provides two enhanced IDE controllers (4 devices)
  - Supports dual bus master mode
  - Supports Ultra DMA 33/66/100 modes
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
  - Provides CompactFlash socket
    - Supports Type I or Type II cards
    - Supports CompactFlash Card
    - Supports secondary IDE bus with Master/Slave jumper
    - Supports bootable CompactFlash card
- Floppy Disk Interface (Separate from Parallel Port)
  - Supports one standard floppy disk drive interface and one USB floppy drive
  - Supports all standard PC/AT formats: 360KB, 1.2MB, 720KB, 1.44MB, 2.88MB
- Parallel Port (Separate from Floppy connector)
  - Provides a standard printer interface
  - Supports IEEE standard 1284 protocols of EPP and ECP outputs
  - Supports Bi-directional data lines
  - Supports 16 byte FIFO for ECP mode.
- Serial Ports
  - Four buffered serial ports with full handshaking
  - Provides 16550-equivalent controllers, each with a built-in 16-byte FIFO buffer
  - Supports full modem capability on two of the four ports

- Supports RS232, RS485, or RS422 operation on each port
- Supports programmable word length, stop bits, and parity
- Supports 16-bit programmable baud-rate generator and a interrupt generator.

- USB Ports
  - Provides two root USB hubs
  - Provides up to four USB ports
  - Supports USB boot devices
  - Supports USB v2.0 EHCI and UHCI v1.1
  - Supports over-current detection status
- Infrared Interface
  - Supports IrDA 1.1 signals through Utility 2 connector
- Keyboard/Mouse Interface
  - Provides PS/2 keyboard interface
  - Provides PS/2 mouse interface
- Audio interface
  - Provides an audio interface
  - Provides AC'97 CODEC on board
  - Supports AC'97 standard
- Ethernet Interface
  - Provides two fully independent Ethernet ports
  - Provides integrated LEDs on each port (Link/Activity and Speed)
  - Provides Intel 82551ER and 82541(GI/PI ) controller chips
  - Supports IEEE 802.3 10/100BaseT and 10/100/1000BaseT compatible physical layers
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full duplex mode
    - Half-duplex mode supports enhance proprietary collision reduction mode
- Video Interfaces (CRT/LVDS)
  - Support CRT (1600 x 1200) with up to 64MB UMA (Unified Memory Architecture)
  - AGP 4X equivalent graphics performance
  - Dual channel 9-, 12-, or 18-bit LVDS
  - LVDS outputs (1 or 2 channel, four differential signals: 3-bits + clock)
- Miscellaneous
  - Real-time clock (RTC) with replaceable battery
  - Battery-free boot (Boots even if battery is dead or missing)
  - Supports both on-board or external battery for Real Time Clock operation
  - Thermal and Voltage monitoring

- Oops! Jumper (BIOS recovery) support
- Serial Console
- Watchdog timer (WDT)
- USB Boot
- LAN Boot (PXE or DHCP) (See Appendix B)

## Block Diagram

Figure 2-2 shows the functional components of the board.

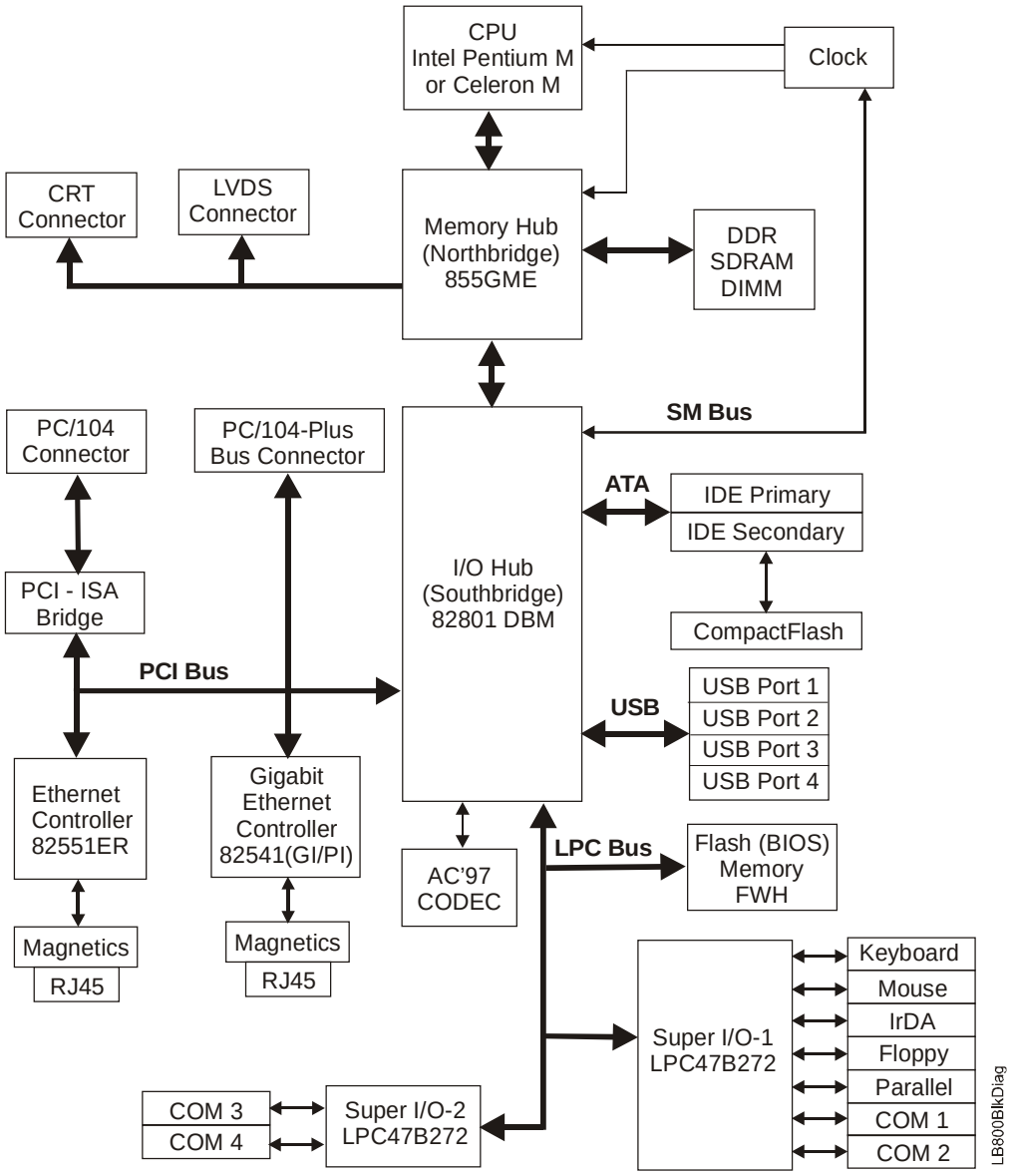



**Figure 2-2. Functional Block Diagram**

## Major Integrated Circuits (Chips)

Table 2-1 lists the major integrated circuits, including a brief description of each, on the LittleBoard 800 and Figures 2-3 and 2-4 show the locations of the major integrated circuits (chips).

**Table 2-1. Major Integrated Circuit Description and Function**

| Chip Type | Mfg. | Model | Description | Function |
|---|---|---|---|---|
| CPUs (U1) | Intel | Pentium M or Celeron M | CPUs offered at 1.4GHz (LV Pentium M), 1.0GHz (ULV Celeron M), or 600MHz (ULV Celeron M) | Embedded CPUs |
| Memory Hub (U2) | Intel | 82855GME | Memory functions plus Video | Memory and Video |
| I/O Hub (U3) | Intel | 82801DBM | Some of the I/O functions | I/O Functions |
| Super I/O 1 & 2 (U14, U16) | SMSC | LPC47B272 | The remaining I/O controller functions | I/O Functions |
| Ethernet Controllers (U9, U11) | Intel | 82551ER 82541(GI/PI) | 10/100BaseT and 10/100/1000BaseT Ethernet controllers respectively | Ethernet functions |
| ISA Bridge (U41) | ITE | IT8888F | PCI-to-ISA bridge conversion | ISA Bus |

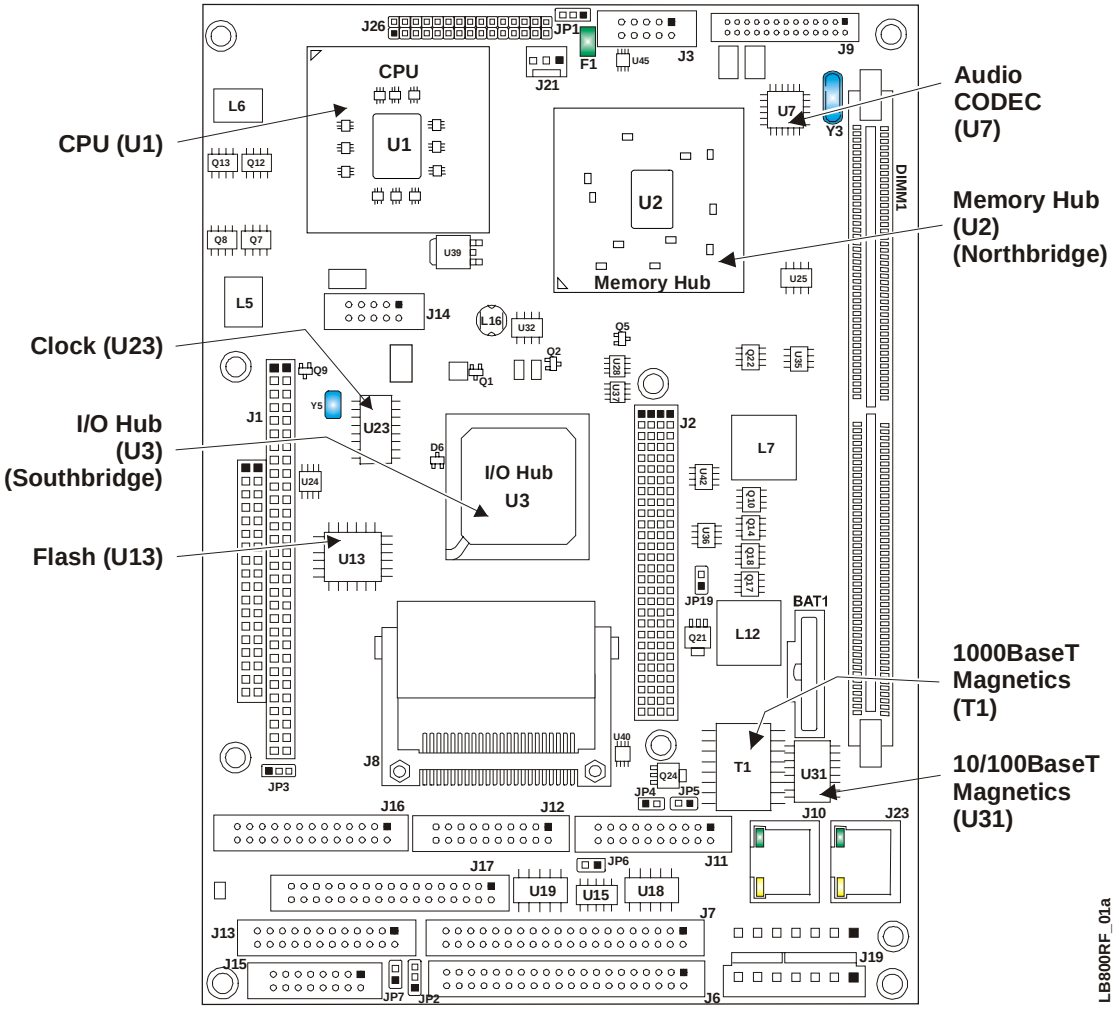



**Figure 2-3. Component Location (Top view)**

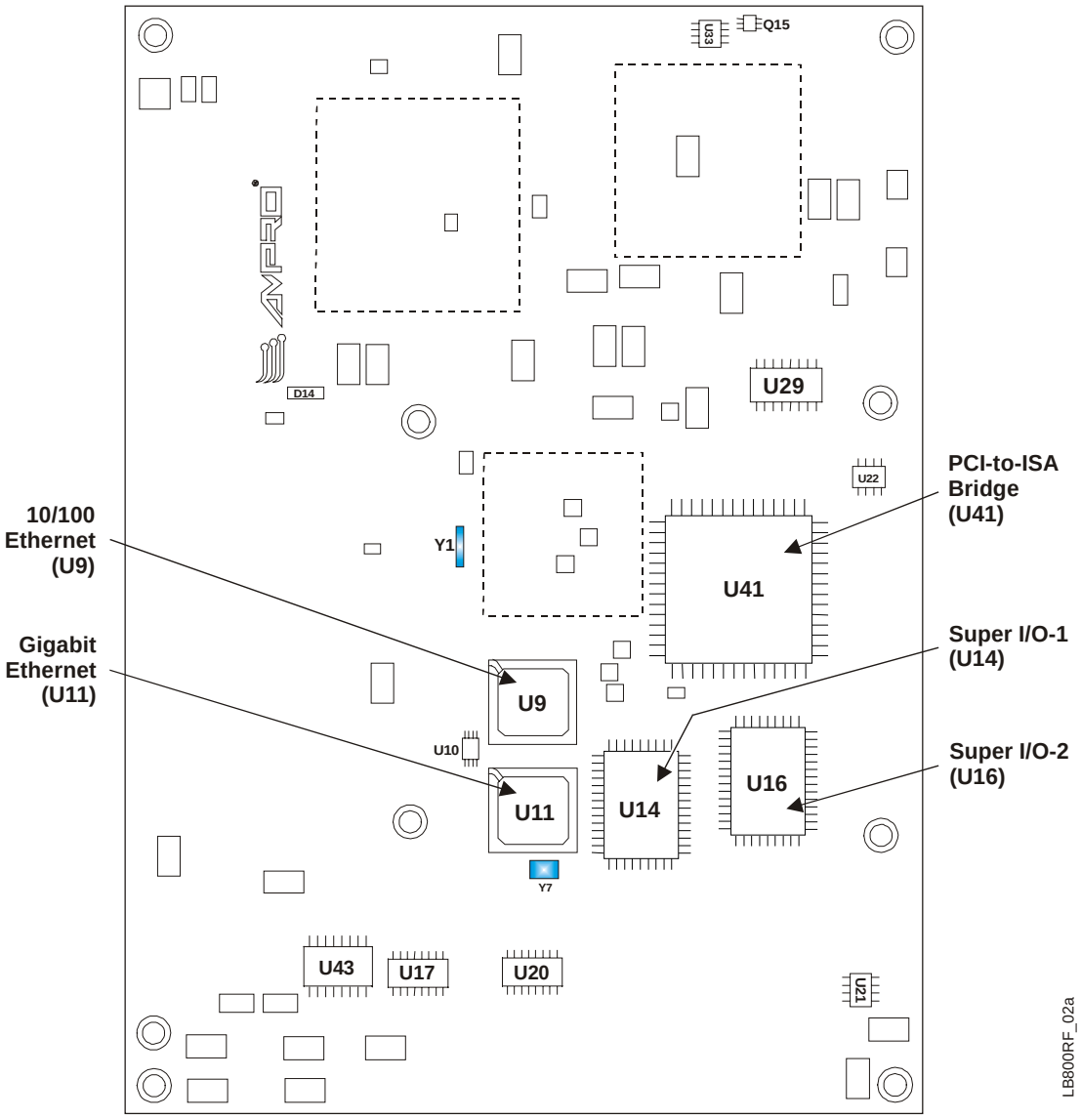



**Figure 2-4. Component Locations (Bottom view)**

## Connector Definitions

Table 2-2 describes the connectors shown in Figure 2-6. All I/O connectors use 0.100" pin (2.54mm) spacing unless otherwise indicated.

**Table 2-2. Connector Descriptions**

| Jack # | Name | Description |
|---|---|---|
| BT1 | Battery Socket | Battery socket for 3.2 volt Lithium battery |
| DIMM1 | Memory | 184-pin, 1.27mm, slot for a single DDR RAM DIMM |
| J1A,B,C,D | PC/104 bus | 104-pins for PC/104 connector |
| J2A,B,C,D | PC/104-Plus | 120-pin, 2mm, connector for PCI bus |
| J3 | Video (CRT) | 10-pin connector for output to a CRT type monitor |
| J6 | Primary IDE | 40-pin connector for the primary IDE interface |
| J7 | Secondary IDE | 40-pin connector for the secondary IDE interface |
| J8 | CompactFlash | 50-pin, 1.27mm, socket accepts Type 1 or Type II CompactFlash cards |
| J9 | Audio In/Out | 26-pin, 2mm, connector for all of the Audio signals (input/output) |
| J10 | Ethernet 2 | 8-pin RJ45 connector for 10/100/1000BaseT Ethernet port |
| J11 | Serial A | 20-pin connector for serial ports 1 and 2 (COM 1 & COM 2) |
| J12 | Serial B | 20-pin connector for serial ports 3 and 4 (COM 3 & COM 4) |
| J13 | Utility 2 | 24-pin connector for mouse, IrDA, SMBus, USB 0 & 1, power button |
| J14 | Utility 3 | 10-pin connector for USB2 and USB3 ports (bi-direction) |
| J15 | Utility 1 | 16-pin connector for keyboard, external battery, reset switch, speaker |
| J16 | Parallel | 26-pin connector for parallel port |
| J17 | Floppy | 34-pin connector for floppy disk drive interface |
| J19 | Power In | 7-pin, 0.156" (3.96mm), connector for input power |
| J21 | Optional Fan | 3-pin header provides +5V, tach, and ground to optional CPU fan |
| J23 | Ethernet 1 | 8-pin RJ45 connector for 10/100BaseT Ethernet port |
| J26 | Video (LVDS) | 30-pin, 2mm, connector for LVDS type video displays |

**NOTE** Ampro uses a connector/header identification method in Chapter 3 to avoid difficult to see visible numbering next to the connectors. For example, a 20-pin header with two rows of pins, using odd/even numbering, where pin-2 is directly across and adjacent to pin-1, is noted in this way; 20-pin, two rows, odd/even (1, 2). Alternately, a 20-pin connector using consecutive numbering, where pin-11 is directly across and adjacent to pin-1, is noted in this way; 20-pin, two rows, consecutive (1, 11). The second number in the parenthesis is always directly across from and adjacent to pin-1, with a few exceptions (DIMM1 slot, PC/104-Plus, PC/104). See Figure 2-5.

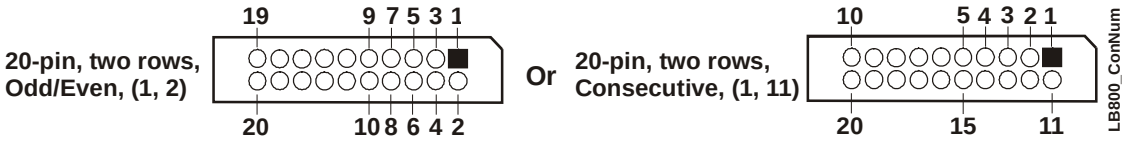



**Figure 2-5. Connector Pin-Out Identification**

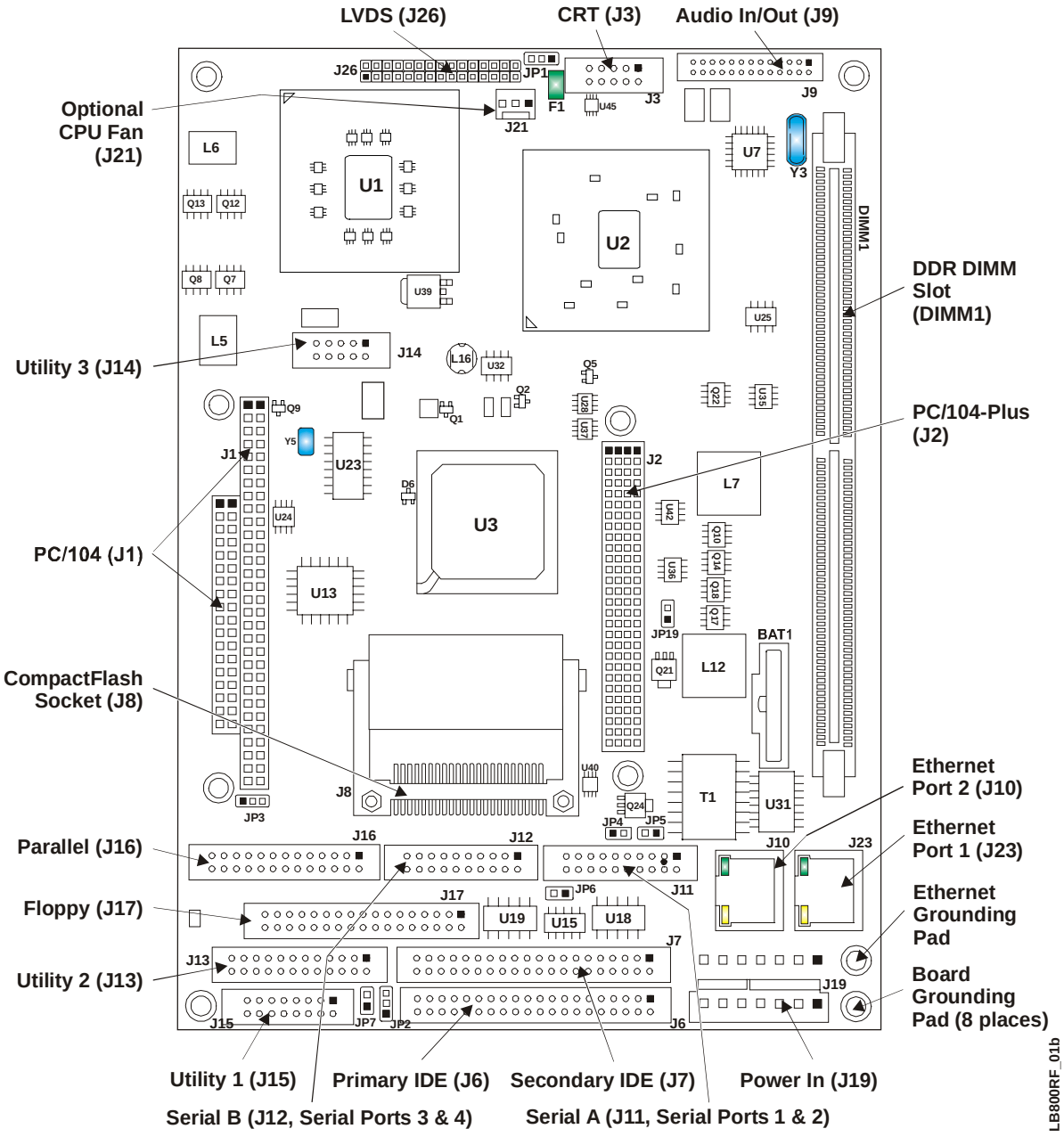



**Figure 2-6. Connector Locations (Top view)**

| | |
|---|---|
| **CAUTION** | The two Ethernet ports share a common ground (transformer center tap), that is floating until you determine how the common ground is connected. The grounding holes (8) of the LittleBoard 800 are connected to ground potential (return) of the DC power supply connected to the board through J19. |

| | |
|---|---|
| **NOTE** | Pin-1 is shown as a black pin (square or round) in all connectors and jumpers in all illustrations. |

## LED Definitions

Tables 2-3 and 2-4 provide the LED colors and definitions for the Ethernet ports, Port 1 (J23) and Port 2 (J10) located on the LittleBoard 800. Refer to Figure 2-6.

**Table 2-3. Ethernet Port 1 (J23) LED Indicators**

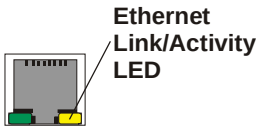
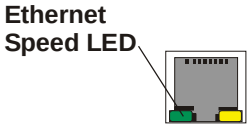
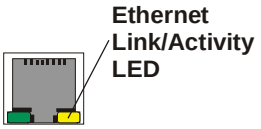
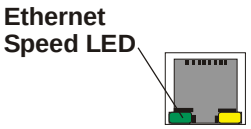
| Indicator | Definition |
|---|---|
|  | Link/Activity LED – This yellow LED is the activity/link indicator and provides the status of Ethernet port 1 (J23).<br>• A **steady On** LED indicates a link is established<br>• A **flashing** LED indicates active data transfers |
|  | Speed LED – This green LED is the Speed indictor and indicates transmit or receive speed of Ethernet port 1 (J23).<br>• A **steady Off** LED shows the port at 10BaseT speed<br>• A **steady On** LED shows the port at 100BaseT speed |

**Table 2-4. Ethernet Port 2 (J10) LED Indicators**

| Indicator | Definition |
|---|---|
|  | Link/Activity LED – This yellow LED is the activity/link indicator and provides the status of Ethernet port 2 (J10).<br>• A **steady On** LED indicates a link is established<br>• A **flashing** LED indicates active data transfers |
|  | Speed LED – This green LED is the Speed indictor and indicates transmit or receive speed of Ethernet port 2 (J10).<br>• A **steady On** LED indicates the port is at 10/100BaseT speed<br>• A **steady Off** LED indicates the port is at 1000BaseT speed |

## Jumper Definitions

Table 2-5 describes the jumpers shown in Figure 2-7.

**Table 2-5. Jumper Settings**

| Jumper # | Installed | Removed/Installed |
|---|---|---|
| JP1 – LVDS Voltage Select | Enable +3.3V (pins 1-2) | Enable +5V (pins 2-3) |
| JP2 – CompactFlash Master/Slave | Enable Master (pins 1-2) | Enable Slave (pins 2-3) **Default** |
| JP3 – CompactFlash Voltage Selection | Enable +5V (pins 1-2) | Enable +3.3V (pins 2-3) |
| JP4 – Serial Port 1 RS485 Termination | Enable Termination (pins 1-2) | Disable Termination (Removed) **Default** |
| JP5 – Serial Port 2 RS485 Termination | Enable Termination (pins 1-2) | Disable Termination (Removed) **Default** |
| JP6 – Serial Port 3 RS485 Termination | Enable Termination (pins 1-2) | Disable Termination (Removed) **Default** |
| JP7 – Serial Port 4 RS485 Termination | Enable Termination (pins 1-2) | Disable Termination (Removed) **Default** |
| JP19 – CMOS Normal/Clear | Clear CMOS (pins 1-2) | Normal (Removed) **Default** |

**Note:** Only the jumpers listed above are populated on the board. Jumpers or shunts use 2mm spacing.

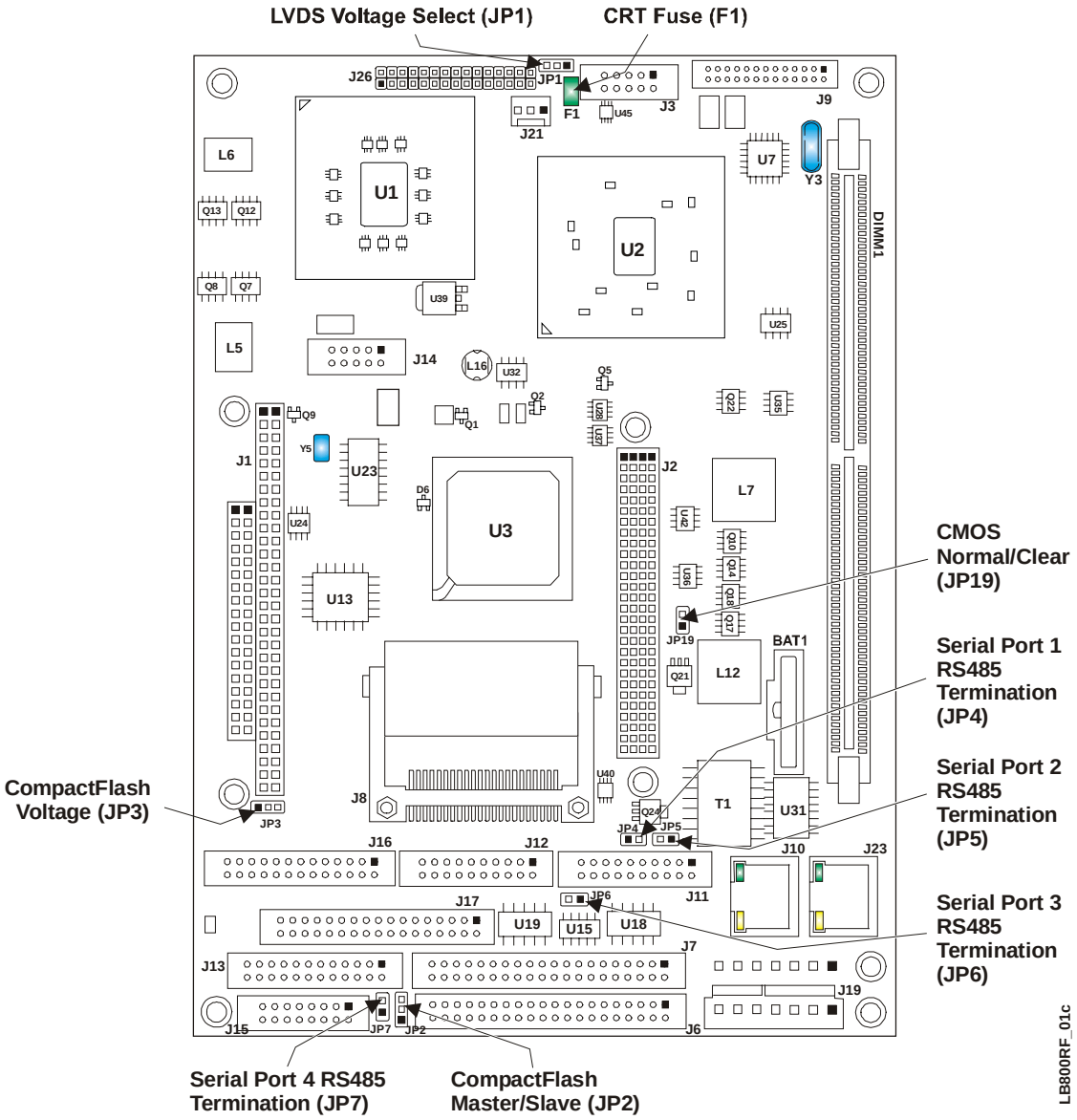



**Figure 2-7. Jumpers and Fuse Locations (Top view)**

## Additional Components

The fuse in Table 2-6 is shown in Figure 2-7.

**Table 2-6. Additional Component Descriptions**

| Component | Description |
|---|---|
| F1 (1.5A) Auto Reset | Overcurrent Fuse for the CRT on connector J3 |

# Specifications

## Physical Specifications

Table 2-7 gives the physical dimensions of the board and Figures 2-8 and 2-9 give the mounting dimensions and pin-1 connector locations.

**Table 2-7. Weight and Footprint Dimensions**

| Item | Dimension |
|---|---|
| Weight | 0.351kg. (0.775lbs.) |
| Height (overall) | 24.94mm (0.982”) |
| Width | 146mm (5.75”) |
| Length | 203mm (8.0”) |
| Thickness | 2.36mm (0.093”) |

**NOTE** Overall height is measured from the upper board surface to the highest permanent component (battery in socket) on the upper board surface. This measurement does not include the various heatsinks or various size DIMMs inserted into the socket. The DIMMs or heatsinks could increase this dimension.

## Environmental Specifications

Table 2-8 provides the most efficient operating and storage condition ranges required for this board.

**Table 2-8. Environmental Requirements**

| | Parameter | 600MHz Celeron M Conditions | 1.0GHz Celeron M Conditions | 1.4GHz Pentium M Conditions |
|---|---|---|---|---|
| Temperature | Operating | +0°to+70°C (32°to +158°F) | +0°to+70°C (32°to +158°F) | +0°to+70°C (32°to +158°F) |
| | Extended (Optional) | –40°to+85°C (–40°to+185°F) | –40°to+85°C (–40°to+185°F) | –40°to+85°C* (–40°to+185°F) |
| | Storage | –55°to+85°C (–67°to+185°F) | –55°to+85°C (–67°to+185°F) | –55°to+85°C (–67°to+185°F) |
| Humidity | Operating | 5% to 95% relative humidity, non-condensing | 5% to 95% relative humidity, non-condensing | 5% to 95% relative humidity, non-condensing |
| | Non-operating | 5% to 95% relative humidity, non-condensing | 5% to 95% relative humidity, non-condensing | 5% to 95% relative humidity, non-condensing |

**Note:** *The 1.4GHz Pentium M requires a fan above 70°C.

## Power Specifications

Table 2-9 shows the power requirements from the baseboard and the board power output.

**Table 2-9. Power Supply Requirements**

| Parameter | 600MHz Celeron M Characteristics | 1.0GHz Celeron M Characteristics | 1.4GHz Pentium M Characteristics |
|---|---|---|---|
| Input Type | Regulated DC voltages | Regulated DC voltages | Regulated DC voltages |
| In-rush Current* (Typical) | 11Amps | 15Amps | 10.2Amps |
| BIT** Current (Typical) | 2.7A (13.5W) | 2.8A (14W) | 3.4A (17W) |

**Notes:** *In-rush measured with video, 128MB DDR PC2700 RAM memory, and power connected.

**The BIT (burn in test) current was measured using with 128MB DDR PC2700 RAM, video, Ampro I/O Interface board, floppy (1), IDE HDD (1), PS/2 keyboard & mouse, 4 Serial loopbacks, externally powered USB CD-ROM (1), externally powered USB HDD (1), USB Jump-Drive (1), USB CompactFlash reader with 64MB CompactFlash card (1), onboard 64MB CompactFlash card, and two operating Ethernet channels. LittleBoard 800 used Windows 2000 as OS.

## Thermal/Cooling Requirements

The CPU, Memory Hub, I/O Hub, and voltage regulators are the sources of heat on the board. The LittleBoard 800 is designed to operate at the maximum speed of the respective CPUs, 600MHz, 1.0GHz, or 1.4GHz. The Celeron M CPUs require a heatsink but no fan for –40°to+85°C operation. The Pentium M CPU requires a heatsink but no fan for +0°to+70°C operation, but does require a fan above +70°C (+70°C to+85°C operation).

## Mechanical Specifications

Figures 2-8 and 2-9 show top views of the LittleBoard 800 with the mechanical mounting dimensions.

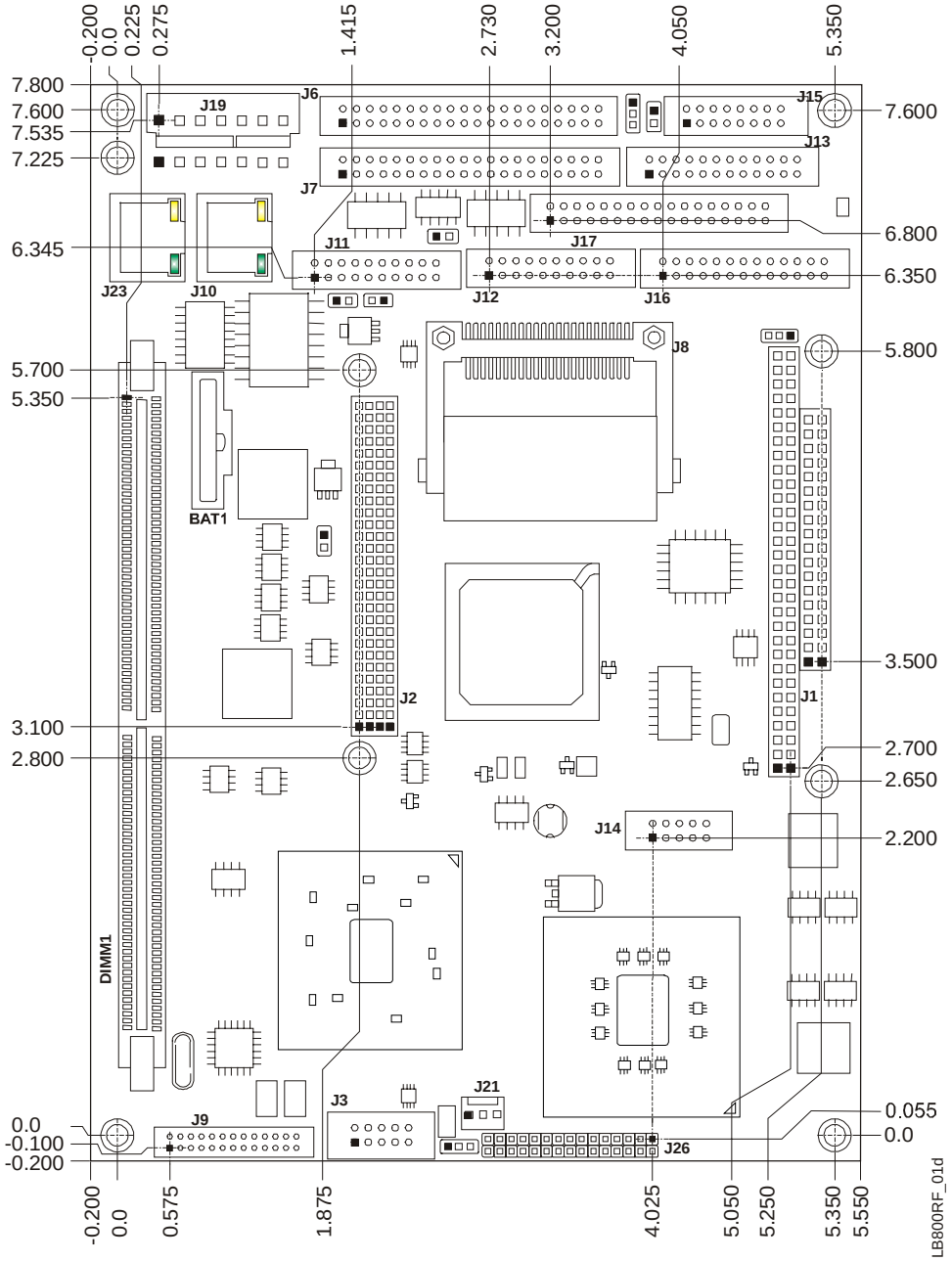



**Figure 2-8. LittleBoard 800 Dimensions (Top view, #1)**

| **NOTE** | All dimensions are given in inches. |
|---|---|

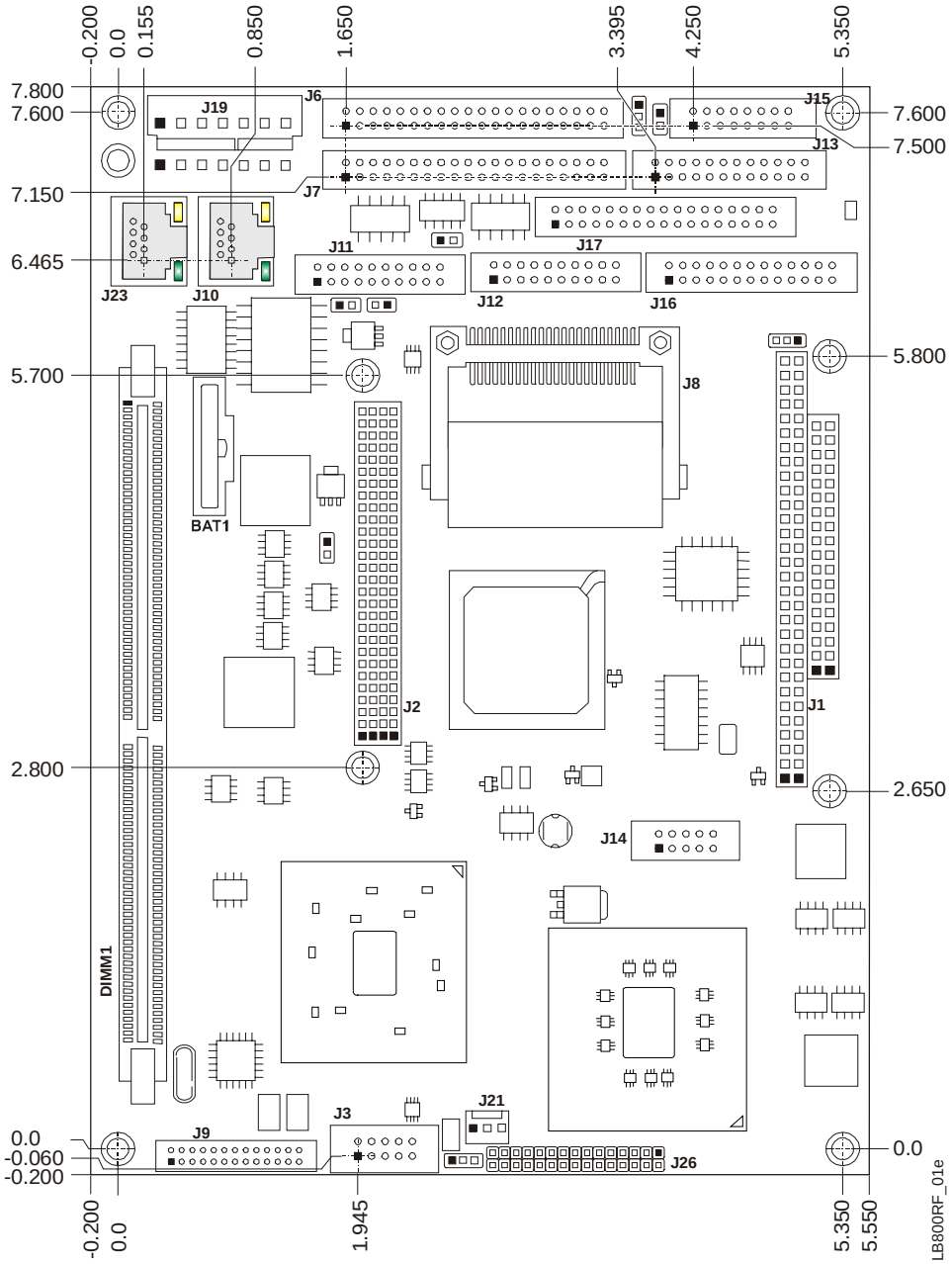



**Figure 2-9. LittleBoard 800 Dimensions (Top view, #2)**

| **NOTE** | All dimensions are given in inches. |
|---|---|

# Chapter 3 Hardware

## Overview

This chapter discusses the chips and features of the connectors in the following order:

- CPU (U1)
- Memory (DIMM1)
- PC/104-Plus (J2A, B, C, D)
- PC/104 (J1A, B, C, D)
- IDE Interfaces (J6, J7)
- CompactFlash Socket (J8)
- Floppy Interface (J17)
- Serial Interfaces (J11, J12)
- Parallel Interface (J16)
- Utility Interfaces (J13, J14, J15)
  - Keyboard
  - Mouse
  - Battery
  - Reset Switch
  - Speaker
  - USB
  - SMBus
  - Infrared (IrDA)
- Ethernet Interfaces (J10, J23)
- Audio Interface (J5)
- CRT/LVDS Video Interfaces (J3, J4)
- Miscellaneous
  - Time of Day/RTC
  - Temperature Monitoring
  - Oops! Jumper (BIOS recovery)
  - Serial Console
  - Watchdog timer
- Power Interface (J19)

| **NOTE** | Ampro Computers, Inc. only supports the features/options tested and listed in this manual. The main integrated circuits (chips) used in the LittleBoard 800 may provide more features or options than are listed for the LittleBoard 800, but some of these chip features/options are not supported on the board and may not function as specified in the chip documentation. |
|---|---|

# CPU (U1)

The LittleBoard 800 offers high performance Intel processors at 1.4GHz Low Voltage (LV) Pentium® M 738, 1.0GHz Ultra Low Voltage (ULV) Celeron® M 373, or 600MHz Ultra Low Voltage (ULV) Celeron M processor.

**Celeron M Processors**

The 600MHz Celeron M processor (Banias core) has 512kB L2 Cache on board, with a 400MHz FSB (front side bus). This Celeron M processor uses 130nm architecture and requires a heatsink, but no fan.

The 1.0GHz Celeron M processor (Dothan core) has 512kB L2 Cache on board with a 400MHz FSB. This Celeron M 373 processor uses 90nm architecture and requires a heatsink, but no fan.

**Pentium M Processor**

The 1.4GHz Pentium M 738 processor (Dothan core) has 2MB L2 Cache on board with a 400MHz FSB. This Pentium M 738 processor uses 90nm architecture and requires a heatsink, but no fan below 70° C..

# Memory

The LittleBoard 800 memory consists of the following elements:

- DDR DIMM RAM
- Flash memory

## DDR DIMM Memory (DIMM1)

The LittleBoard 800 supports a single standard 184-pin DDR DIMM slot.

- DIMM slot can support up to 1GB of memory
- Supports PC2100 (266MHz) or PC2700 (333MHz) DDR RAM
- +2.5V SDRAM

## Flash Memory (U13)

There is an 8-bit wide, 512kB flash device used for system BIOS that is connected to the I/O Hub, 82801DBM (Southbridge), through the LPC bus. The BIOS is re-programmable and the supported features are detailed in Chapter 4, *BIOS Setup*.

## Interrupt Channel Assignments

The channel interrupt assignments are shown in Table 3-1.

**Table 3-1. Interrupt Channel Assignments**

| Device vs IRQ No. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Timer** | X | | | | | | | | | | | | | | | |
| **Keyboard** | | X | | | | | | | | | | | | | | |
| **Secondary Cascade** | | | X | | | | | | | | | | | | | |
| **COM1** | | O | | O | **D** | O | O | O | | O | O | O | O | | O | O |
| **COM2** | | O | | **D** | O | O | O | O | | O | O | O | O | | O | O |
| **COM3** | | O | | O | O | O | O | O | | O | O | **D** | O | | O | O |
| **COM4** | | O | | O | O | O | O | O | | O | **D** | O | O | | O | O |
| **Floppy** | | | | | | | X | | | | | | | | | |
| **Parallel** | | O | | O | O | O | O | **D** | | O | O | O | O | | O | O |
| **RTC** | | | | | | | | | X | | | | | | | |
| **IDE Primary** | | | | | | | | | | | | | | | X | |
| **IDE Secondary** | | | | | | | | | | | | | | | | X |
| **Math Coprocessor** | | | | | | | | | | | | | | X | | |
| **PS/2 Mouse** | | | | | | | | | | | | | X | | | |
| **PCI INTA** | | O | | O | O | **D** | O | O | | O | O | O | O | | O | O |
| **PCI INTB** | | O | | O | O | O | O | O | | **D** | O | O | O | | O | O |
| **PCI INTC** | | O | | O | O | **D** | O | O | | O | O | O | O | | O | O |
| **PCI INTD** | | O | | O | O | O | O | O | | **D** | O | O | O | | O | O |
| **PCI INTE** | | O | | O | O | **D** | O | O | | O | O | O | O | | O | O |
| **PCI INTF** | | O | | O | O | O | O | O | | **D** | O | O | O | | O | O |
| **PCI INTH** | | O | | O | O | **D** | O | O | | O | O | O | O | | O | O |

**Legend:** D = Default, O = Optional, X = Fixed

| **NOTE** | The IRQs for the Ethernet, Video, and Internal Local Bus (ISA) are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices. |
|---|---|

## Memory Map

The following table provides the common PC/AT memory allocations. Memory below 000500h is used by the BIOS.

**Table 3-2. Memory Map**

| Base Address | Function |
|---|---|
| 00000000h - 0009FFFFh | Conventional Memory |
| 000A0000h - 000AFFFFh | Graphics Memory |
| 000B0000h - 000B7FFFh | Mono Text Memory |
| 000B8000h - 000BFFFFh | Color Text Memory |
| 000C0000h - 000C7FFFh | Standard Video BIOS |
| 000F0000h - 000FFFFFh | System BIOS Area (Storage and RAM Shadowing) |
| 00100000h - 04000000h | Extended Memory (If onboard VGA is enabled, then the amount of memory assigned is subtracted from extended memory) |
| FFF80000h - FFFFFFFFh | System Flash |

## I/O Address Map

Table 3-3 shows the I/O address map.

**Table 3-3. I/O Address Map**

| Address (hex) | Subsystem |
|---|---|
| 000-00F | Primary DMA Controller |
| 020-021 | Master Interrupt Controller |
| 040-043 | Programmable Interrupt Timer (Clock/Timer) |
| 060-06F | Keyboard Controller |
| 070-07F | CMOS RAM, NMI Mask Reg, RT Clock |
| 080-09F | DMA Page Registers |
| 092 | Fast A20 gate and CPU reset |
| 094 | Motherboard enable |
| 102 | Video subsystem register |
| 0A0-0BF | Slave Interrupt Controller |
| 0C0-0DF | Slave DMA Controller #2 |
| 0F0-0FF | Math Coprocessor |
| 170-177 | Secondary IDE Hard Disk Controller |
| 1F0-1F8 | Primary IDE Hard Disk Controller |
| 278-27F | Parallel Printer |
| 2E8-2FF | Serial Port 4 (COM4) |
| 2F8-2FF | Serial Port 2 (COM2) |
| 378-37F | Parallel port (Standard and EPP) |
| 3C0-3DF | VGA |
| 3E8-3EF | Serial Port 3 (COM3) |
| 3F0-3F7 | Floppy Disk Controller |
| 3F8-3FF | Serial Port 1 (COM1) |
| 778-77A | Parallel Port (ECP Extensions) (Port 378+400) |
| CF8-CFF | PCI bus Configuration Address and Data |

# PC/104-Plus Interface (J2)

PC/104-*Plus* uses a 120 pin (4x30) 2mm connector interface. This interface connector carries all of the appropriate PCI signals operating at clock speeds up to 33MHz. The Memory Hub (82855GME), integrates a PCI arbiter that supports up to four devices with three external PCI masters. This interface header accepts stackable modules and is located on the top of the board.

Table 3-4 provides the signals and descriptions for the PCI bus pin-outs of 120 pins, 4 rows, consecutive numbering, (A1, B1, C1, D1), 2mm connector.

**Table 3-4. PC/104-Plus Pin/Signal Descriptions (J2)**

| Pin # | Signal | Input/ Output | Description |
|---|---|---|---|
| 1 (A1) | Key/GND | | Key – Ground |
| 2 (A2) | VI/O | | +5 volts ±5% (Reference voltage only) |
| 3 (A3) | AD05 | T/S | PCI Address/Data Bus Line 5 – These signals (AD31 - AD0) are multiplexed on these pins. A bus transaction consists of an address followed by one or more data cycles. |
| 4 (A4) | C/BE0* | T/S | PCI Bus Command/Byte Enable 0 – These signals (C/BE 0 -3) are line multiplexed, so that during the address cycle, the command is defined and during the data cycle, the byte enable is defined. |
| 5 (A5) | GND | | Ground |
| 6 (A6) | AD11 | T/S | Address/Data Bus Line 11 – Refer to pin-A3 for more information. |
| 7 (A7) | AD14 | T/S | Address/Data Bus Line 14 – Refer to pin-A3 for more information. |
| 8 (A8) | +3.3V | | +3.3 volts ±5% power supply input |
| 9 (A9) | SERR* | O/D | System Error – This signal is for reporting address parity errors. |
| 10 (A10) | GND | | Ground |
| 11 (A11) | STOP* | S/T/S | Stop – This signal indicates the current selected device is requesting the master to stop the current transaction |
| 12 (A12) | +3.3V | | +3.3 volts ±5% power supply input |
| 13 (A13) | FRAME* | S/T/S | Frame access – This signal is driven by the current master, indicating a transaction start and will remain active until the final data cycle. |
| 14 (A14) | GND | | Ground |
| 15 (A15) | AD18 | T/S | Address/Data Bus Line 18 – Refer to pin-A3 for more information. |
| 16 (A16) | AD21 | T/S | Address/Data Bus Line 21 – Refer to pin-A3 for more information. |
| 17 (A17) | +3.3V | | +3.3 volts ±5% power supply input |
| 18 (A18) | IDSEL0 | In | Initialization Device Select 0 – These signals (IDSEL 0-3) are used as the chip-selects during configuration read and write transactions. |
| 19 (A19) | AD24 | T/S | Address/Data Bus Line 24 – Refer to pin A3 for more information. |
| 20 (A20) | GND | | Ground |
| 21 (A21) | AD29 | T/S | Address/Data Bus Line 29 – Refer to pin A3 for more information. |
| 22 (A22) | +5V | | +5 volts ±5% power supply input |
| 23 (A23) | REQ0* | T/S | Bus Request 0 – These signals (REQ 0-2) indicate to the arbitrator the device desires use of the bus. |
| 24 (A24) | GND | | Ground |

| Pin # | Signal | Input/ Output | Description |
|---|---|---|---|
| 25 (A25) | GNT1* | T/S | Grant 1 – These signal (GNT 0-2) lines indicate access has been granted to the requesting device (PCI Masters). |
| 26 (A26) | +5V | | +5 volts ±5% power supply input |
| 27 (A27) | CLK2 | In | Clock 2 – These clocks (CLK 0-3) provide timing outputs for four external PCI devices and all timing transactions on the PCI bus. |
| 28 (A28) | GND | | Ground |
| 29 (A29) | +12V | | +12 volts ±5% power supply input |
| 30 (A30) | -12V | | -12 volts (Supplied externally or through PC/104-Plus bus) |
| 31 (B1) | NC | | Not connected (Reset) |
| 32 (B2) | AD02 | T/S | Address/Data Bus Line 2 – Refer to pin A3 for more information. |
| 33 (B3) | GND | | Ground |
| 34 (B4) | AD07 | T/S | Address/Data Bus Line 7 – Refer to pin A3 for more information. |
| 35 (B5) | AD09 | T/S | Address/Data Bus Line 9 – Refer to pin A3 for more information. |
| 36 (B6) | VI/O | | +5 volts ±5% (Reference voltage only) |
| 37 (B7) | AD13 | T/S | Address/Data Bus Line 13 – Refer to pin-A3 for more information. |
| 38 (B8) | C/BE1* | T/S | Command/Byte Enable 1 – Refer to pin-A4 for more information. |
| 39 (B9) | GND | | Ground |
| 40 (B10) | PERR* | | Parity Error – This signal is for reporting data parity errors. |
| 41 (B11) | +3.3V | | +3.3 volts ±5% power supply input |
| 42 (B12) | TRDY* | S/T/S | Target Ready – This signal indicates the selected device's ability to complete the current cycle of transaction. Both IRDY* and TRDY* must be asserted to terminate a data cycle. |
| 43 (B13) | GND | | Ground |
| 44 (B14) | AD16 | T/S | Address/Data Bus Line 16 – Refer to pin-A3 for more information. |
| 45 (B15) | +3.3V | | +3.3 volts ±5% power supply input |
| 46 (B16) | AD20 | T/S | Address/Data Bus Line 20 – Refer to pin-A3 for more information. |
| 47 (B17) | AD23 | T/S | Address/Data Bus Line 23 – Refer to pin-A3 for more information. |
| 48 (B18) | GND | | Ground |
| 49 (B19) | C/BE3* | T/S | Command/Byte Enable 3 – Refer to pin-A4 for more information. |
| 50 (B20) | AD26 | T/S | Address/Data Bus Line 26 – Refer to pin-A3 for more information. |
| 51 (B21) | +5V | | +5 volts ±5% power supply input |
| 52 (B22) | AD30 | T/S | Address/Data Bus Line 30 – Refer to pin-A3 for more information. |
| 53 (B23) | GND | | Ground |
| 54 (B24) | REQ2* | T/S | Bus Request 2 – Refer to pin-A23 for more information. |
| 55 (B25) | VI/O | | +5 volts ±5% (Reference voltage only) |
| 56 (B26) | CLK0 | In | Clock 0 – Refer to pin-A27 for more information |
| 57 (B27) | +5V | | +5 volts ±5% power supply input |
| 58 (B28) | INTD* | O/D | Interrupt D – This signal is used to request interrupts only for multi-function devices. |
| 59 (B29) | INTA* | O/D | Interrupt A – This signal is used to request an interrupt. |

| Pin # | Signal | Input/ Output | Description |
|---|---|---|---|
| 60 (B30) | REQ3* | T/S | Bus Request 3 – Refer to pin-A23 for more information. |
| 61 (C1) | +5V | | +5 volts ±5% power supply input |
| 62 (C2) | AD01 | T/S | Address/Data Bus Line 1 – Refer to pin-A3 for more information. |
| 63 (C3) | AD04 | T/S | Address/Data Bus Lines 4 – Refer to pin-A3 for more information. |
| 64 (C4) | GND | | Ground |
| 65 (C5) | AD08 | T/S | Address/Data Bus Line 8 – Refer to pin-A3 for more information. |
| 66 (C6) | AD10 | T/S | Address/Data Bus Line 10 – Refer to pin-A3 for more information. |
| 67 (C7) | GND | | Ground |
| 68 (C8) | AD15 | T/S | Address/Data Bus Line 15 – Refer to pin-A3 for more information. |
| 69 (C9) | NC | | Not connected (Snoop Backoff) |
| 70 (C10) | +3.3V | | +3.3 volts ±5% power supply input |
| 71 (C11) | LOCK* | S/T/S | Lock – This signal indicates an operation that may require multiple transactions to complete |
| 72 (C12) | GND | | Ground |
| 73 (C13) | IRDY* | S/T/S | Initiator Ready – This signal indicates the master's ability to complete the current data cycle of the transaction |
| 74 (C14) | +3.3V | | +3.3 volts ±5% power supply input |
| 75 (C15) | AD17 | T/S | Address/Data Bus Line 17 – Refer to pin-A3 for more information. |
| 76 (C16) | GND | | Ground |
| 77 (C17) | AD22 | T/S | Address/Data Bus Line 22 – Refer to pin-A3 for more information. |
| 78 (C18) | IDSEL1 | | Initialization Device Select 1 – Refer to pin-A18 for more information |
| 79 (C19) | VI/O | | +5 volts ±5% (Reference voltage only) |
| 80 (C20) | AD25 | T/S | Address/Data Bus Line 25 – Refer to pin-A3 for more information. |
| 81 (C21) | AD28 | T/S | Address/Data Bus Line 28 – Refer to pin-A3 for more information. |
| 82 (C22) | GND | | Ground |
| 83 (C23) | REQ1* | T/S | Bus Request 1 – Refer to pin-A23 for more information. |
| 84 (C24) | +5V | | +5 volts ±5% power supply input |
| 85 (C25) | GNT2* | T/S | Grant 2 – Refer to pin-A25 for more information |
| 86 (C26) | GND | | Ground |
| 87 (C27) | CLK3 | In | Clock 3 – Refer to pin-A27 for more information |
| 88 (C28) | +5V | | +5 volts ±5% power supply input |
| 89 (C29) | INTB* | O/D | Interrupt B – This signal is used to request interrupts only for multi-function devices. |
| 90 (C30) | GNT3* | T/S | Grant 3 – Refer to pin-A25 for more information |
| 91 (D1) | AD00 | T/S | Address/Data Bus Line 0 – Refer to pin-A3 for more information. |
| 92 (D2) | +5V | | +5 volts ±5% power supply input |
| 93 (D3) | AD03 | T/S | Address/Data Bus Line 3 – Refer to pin-A3 for more information. |
| 94 (D4) | AD06 | T/S | Address/Data Bus Line 6 – Refer to pin-A3 for more information. |
| 95 (D5) | GND | | Ground |
| 96 (D6) | M66EN | | Not supported – Reserved for 66MHz on PCI bus. |

| Pin # | Signal | Input/ Output | Description |
|---|---|---|---|
| 97 (D7) | AD12 | T/S | Address/Data Bus Line 12 – Refer to pin-A3 for more information. |
| 98 (D8) | +3.3V | | +3.3 volts ±5% power supply input |
| 99 (D9) | PAR | T/S | Bus Parity bit – This signal is the even parity bit on AD[31:0] and C/BE[3:0]* |
| 100 (D10) | NC | | Not connected (Snoop Done) |
| 101 (D11) | GND | | Ground |
| 102 (D12) | DEVSEL* | S/T/S | Device Select – This signal is driven by the target device when its address is decoded. |
| 103 (D13) | +3.3V | | +3.3 volts ±5% power supply input |
| 104 (D14) | C/BE2* | | Command/Byte Enable 2 – Refer to pin-A4 for more information. |
| 105 (D15) | GND | | Ground |
| 106 (D16) | AD19 | T/S | Address/Data Bus Line 19 – Refer to pin-A3 for more information. |
| 107 (D17) | +3.3V | | +3.3 volts ±5% power supply input |
| 108 (D18) | IDSEL2 | | Initialization Device Select 2 – Refer to pin-A18 for more info. |
| 109 (D19) | IDSEL3 | | Initialization Device Select 3 – Refer to pin-A18 for more info. |
| 110 (D20) | GND | | Ground |
| 111 (D21) | AD27 | T/S | Address/Data Bus Line 27 – Refer to pin-A3 for more information. |
| 112 (D22) | AD31 | T/S | Address/Data Bus Line 31 – Refer to pin-A3 for more information. |
| 113 (D23) | VI/O | | +5 volts ±5% (Reference voltage only) |
| 114 (D24) | GNT0* | T/S | Grant 0 – Refer to pin-A25 for more information. |
| 115 (D25) | GND | | Ground |
| 116 (D26) | CLK1 | In | Clock 1 – Refer to pin-A27 for more information. |
| 117 (D27) | GND | | Ground |
| 118 (D28) | RST* | In | PCI bus reset – This signal is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset. |
| 119 (D29) | INTC* | O/D | Interrupt C – This signal is used to request interrupts only for multi-function devices. |
| 120 (D30) | GND | | Ground |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

The Input/Output signals in this table refer to the input/output signals listed in the *PCI Local Bus Manual*, Revision 2.2, Chapter 2, paragraph 2.1, Signal definitions. The following terms or acronyms are used in this table:

- In – Input is standard input only signal
- Out – Totem Pole output is a standard active driver
- T/S – Tri-State is a bi-directional input output pin
- S/T/S – Sustained Tri-State is an active low tri-state signal driven by one and only one agent at a time
- O/D – Open Drain allows multiple devices to share as a wire-OR.

# PC/104 Interface (J1A,B,C,D)

The PC/104 Bus uses a 104-pin 100 mil header interface. This interface header will carry all of the appropriate PC/104 signals operating at clock speeds up to 8MHz. This interface header accepts stackable modules and is located on the top of the board. The PC/104 connector uses 104-pin, 4 rows, consecutive numbering, (A1, B1, C0, D0), and 0.100" pin spacing.

**Table 3-5. PC/104 Interface Pin/Signal Descriptions (J1A)**

| Pin # | Signal | Description (J1 Row A) |
|---|---|---|
| 1 (A1) | IOCHCHK* | I/O Channel Check – This signal may be activated by ISA boards to request that a non-maskable interrupt (NMI) be generated to the system processor. It is driven active to indicate an uncorrectable error has been detected. |
| 2 (A2) | SD7 | System Data 7 – This signal (0 to 19) provides a system data bit. |
| 3 (A3) | SD6 | System Data 6 – Refer to pin-A2 for more information. |
| 4 (A4) | SD5 | System Data 5 – Refer to pin-A2 for more information. |
| 5 (A5) | SD4 | System Data 4 – Refer to pin-A2 for more information. |
| 6 (A6) | SD3 | System Data 3 – Refer to pin-A2 for more information. |
| 7 (A7) | SD2 | System Data 2 – Refer to pin-A2 for more information. |
| 8 (A8) | SD1 | System Data 1 – Refer to pin-A2 for more information. |
| 9 (A9) | SD0 | System Data 0 – Refer to pin-A2 for more information. |
| 10 (A10) | IOCHRDY | I/O Channel Ready – This signal allows slower ISA boards to lengthen I/O or memory cycles by inserting wait states. This signal's normal state is active high (ready). ISA boards drive the signal inactive low (not ready) to insert wait states. Devices using this signal to insert wait states should drive it low immediately after detecting a valid address decode and an active read, or write command. The signal is released high when the device is ready to complete the cycle. |
| 11 (A11) | AEN | Address Enable – This signal is used to degate the system processor and other devices from the bus during DMA transfers. When this signal is active, the system DMA controller has control of the address, data, and read/write signals. This signal should be included as part of ISA board select decodes to prevent incorrect board selects during DMA cycles. |
| 12 (A12) | SA19 | System Address 19 – This signal (0 to 19) provides a system address bit. |
| 13 (A13) | SA18 | System Address 18 – Refer to pin-A12 , for more information. |
| 14 (A14) | SA17 | System Address 17 – Refer to pin-A12 , for more information. |
| 15 (A15) | SA16 | System Address 16 – Refer to pin-A12 , for more information. |
| 16 (A16) | SA15 | System Address 15 – Refer to pin-A12 , for more information. |
| 17 (A17) | SA14 | System Address 14 – Refer to pin-A12 , for more information. |
| 18 (A18) | SA13 | System Address 13 – Refer to pin-A12 , for more information. |
| 19 (A19) | SA12 | System Address 12 – Refer to pin-A12 , for more information. |
| 20 (A20) | SA11 | System Address 11 – Refer to pin-A12 , for more information. |
| 21 (A21) | SA10 | System Address 10 – Refer to pin-A12 , for more information. |
| 22 (A22) | SA9 | System Address 9 – Refer to pin-A12 , for more information. |
| 23 (A23) | SA8 | System Address 8 – Refer to pin-A12 , for more information. |
| 24 (A24) | SA7 | System Address 7 – Refer to pin-A12 , for more information. |

| Pin # | Signal | Description (J1 Row A) |
|---|---|---|
| 25 (A25) | SA6 | System Address 6 – Refer to pin-A12 , for more information. |
| 26 (A26) | SA5 | System Address 5 – Refer to pin-A12 , for more information. |
| 27 (A27) | SA4 | System Address 4 – Refer to pin-A12 , for more information. |
| 28 (A28) | SA3 | System Address 3 – Refer to pin-A12 , for more information. |
| 29 (A29) | SA2 | System Address 2 – Refer to pin-A12 , for more information. |
| 30 (A30) | SA1 | System Address 1 – Refer to pin-A12 , for more information. |
| 31 (A31) | SA0 | System Address 0 – Refer to pin-A12 , for more information. |
| 32 (A32) | GND | Ground |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

**Table 3-6. PC/104 Interface Pin/Signal Descriptions (J1B)**

| Pin # | Signal | Descriptions (J1 Row B) |
|---|---|---|
| 33 (B1) | GND | Ground |
| 34 (B2) | RSTDRV | Reset Drive – This signal is used to reset or initialize system logic on power up or subsequent system reset. |
| 35 (B3) | +5V | +5 volts ±5% power supply input |
| 36 (B4) | IRQ9 | Interrupt Request 9 – Asserted by a device when it has a pending interrupt request. Only one device may use this request line at a time. |
| 37 (B5) | -5V | -5V volt power (Supplied externally or through PC/104 bus) |
| 38 (B6) | DRQ2 | DMA Request 2 – Used by I/O resources to request DMA service, or to request ownership of the bus as a bus master device. Must be held high until associated DACK2 line is active. |
| 39 (B7) | -12V | -12 volt power (Supplied externally or through PC/104 bus) |
| 40 (B8) | ZWS | Zero Wait State – This signal is driven low by a bus slave device to indicate it is capable of performing a bus cycle without inserting any additional wait states. To perform a 16-bit memory cycle without wait states, this signal is derived from an address decode. |
| 41 (B9) | +12V | +12 volt power supply input (Supplied externally or through PC/104 bus) |
| 42 (B10) | NC | Not connected |
| 43 (B11) | SMEMW* | System Memory Write – This signal is used by bus owner to request a memory device to store data currently on the data bus and only active for the lower 1MB. Used for legacy compatibility with 8-bit cards. |
| 44 (B12) | SMEMR* | System Memory Read – This signal is used by bus owner to request a memory device to drive data onto the data bus and only active for lower 1MB. Used for legacy compatibility with 8-bit cards. |
| 45 (B13) | IOW* | I/O Write – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to capture the write data on the data bus. |
| 46 (B14) | IOR* | I/O Read – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to drive read data onto the data bus. |
| 47 (B15) | DACK3* | DMA Acknowledge 3 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller. |

| Pin # | Signal | Descriptions (J1 Row B) |
|---|---|---|
| 48 (B16) | DRQ3 | DMA Request 3 – Used by I/O resources to request DMA service. Must be held high until associated DACK3 line is active. |
| 49 (B17) | DACK1* | DMA Acknowledge 1 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller. |
| 50 (B18) | DRQ1 | DMA Request 1 – Used by I/O resources to request DMA service. Must be held high until associated DACK1 line is active. |
| 51 (B19) | REFRESH* | Memory Refresh – This signal is driven low to indicate a memory refresh cycle is in progress. Memory is refreshed every 15.6 usec. |
| 52 (B20) | SYSCLK | System Clock – This is a free running clock typically in the 8MHz to 10MHz range, although its exact frequency is not guaranteed. |
| 53 (B21) | IRQ7 | Interrupt Request 7 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 54 (B22) | IRQ6 | Interrupt Request 6 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 55 (B23) | IRQ5 | Interrupt Request 5 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 56 (B24) | IRQ4 | Interrupt Request 4 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 57 (B25) | IRQ3 | Interrupt Request 3 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 58 (B26) | DACK2* | DMA Acknowledge 2 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller. |
| 59 (B27) | TC | Terminal Count – This signal is a pulse to indicate a terminal count has been reached on a DMA channel operation. |
| 60 (B28) | BALE | Buffered Address Latch Enable – This signal is used to latch the LA23 to LA17 signals or decodes of these signals. Addresses are latched on the falling edge of BALE. It is forced high during DMA cycles. When used with AENx, it indicates a valid processor or DMA address. |
| 61 (B29) | +5V | +5 volts ±5% power supply input |
| 62 (B30) | OSC | Oscillator – This clock signal operates at 14.3MHz. This signal is not synchronous with the system clock (SYSCLK). |
| 63 (B31) | GND | Ground |
| 64 (B32) | GND | Ground |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

**Table 3-7. PC/104 Interface Pin/Signal Descriptions (J1C)**

| Pin # | Signal | Descriptions (J1 Row C) |
|---|---|---|
| 1 (C0) | GND | Ground |
| 2 (C1) | SBHE* | System Byte High Enable – This signal is driven low to indicate a transfer of data on the high half of the data bus (D15 to D8). |
| 3 (C2) | LA23 | Latchable Address 23 – This signal must be latched by the resource if the line is required for the entire data cycle. |
| 4 (C3) | LA22 | Latchable Address 22 – Refer to pin-C2, for more information. |

| Pin # | Signal | Descriptions (J1 Row C) |
|---|---|---|
| 5 (C4) | LA21 | Latchable Address 21 – Refer to pin-C2, for more information. |
| 6 (C5) | LA20 | Latchable Address 20 – Refer to pin-C2, for more information. |
| 7 (C6) | LA19 | Latchable Address 19 – Refer to pin-C2, for more information. |
| 8 (C7) | LA18 | Latchable Address 18 – Refer to pin-C2, for more information. |
| 9 (C8) | LA17 | Latchable Address 17 – Refer to pin-C2, for more information. |
| 10 (C9) | MEMR* | Memory Read – This signal instructs a selected memory device to drive data onto the data bus. It is active on all memory read cycles. |
| 11 (C10) | MEMW* | Memory Write – This signal instructs a selected memory device to store data currently on the data bus. It is active on all memory write cycles. |
| 12 (C11) | SD8 | System Data 8 – Refer to pin-A2 for more information. |
| 13 (C12) | SD9 | System Data 9 – Refer to pin-A2 for more information. |
| 14 (C13) | SD10 | System Data 10 – Refer to pin-A2 for more information. |
| 15 (C14) | SD11 | System Data 11 – Refer to pin-A2 for more information. |
| 16 (C15) | SD12 | System Data 12 – Refer to pin-A2 for more information. |
| 17 (C16) | SD13 | System Data 13 – Refer to pin-A2 for more information. |
| 18 (C17) | SD14 | System Data 14 – Refer to pin-A2 for more information. |
| 19 (C18) | SD15 | System Data 15 – Refer to pin-A2 for more information. |
| 20 (C19) | NC | Not connected |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

**Table 3-8. PC/104 Interface Pin/Signal Descriptions (J1D)**

| Pin # | Signal | Descriptions (J1 Row D) |
|---|---|---|
| 21 (D0) | GND | Ground |
| 22 (D1) | MEMCS16* | Memory Chip Select 16 – This is signal is driven low by a memory slave device to indicates it is cable of performing a 16-bit memory data transfer. This signal is driven from a decode of the LA23 to LA17 address lines. |
| 23 (D2) | IOCS16* | I/O Chip Select 16 – This signal is driven low by an I/O slave device to indicate it is capable of performing a 16-bit I/O data transfer. This signal is driven from a decode of the SA15 to SA0 address lines. |
| 24 (D3) | IRQ10 | Interrupt Request 10 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 25 (D4) | IRQ11 | Interrupt Request 11 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 26 (D5) | IRQ12 | Interrupt Request 12 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 27 (D6) | IRQ15 | Interrupt Request 15 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 28 (D7) | IRQ14 | Interrupt Request 14 – Asserted by a device when it has pending interrupt request. Only one device may use this request line at a time. |
| 29 (D8) | DACK0* | DMA Acknowledge 0 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller. |
| 30 (D9) | DRQ0 | DMA Request 0 – Used by I/O resources to request DMA service. Must be held high until associated DACK0 line is active. |

| Pin # | Signal | Descriptions (J1 Row D) |
|---|---|---|
| 31 (D10) | DACK5* | DMA Acknowledge 5 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller. |
| 32 (D11) | DRQ5 | DMA Request 5 – Used by I/O resources to request DMA service. Must be held high until associated DACK5 line is active. |
| 33 (D12) | DACK6* | DMA Acknowledge 6 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller. |
| 34 (D13) | DRQ6 | DMA Request 6 – Used by I/O resources to request DMA service. Must be held high until associated DACK6 line is active. |
| 35 (D14) | DACK7* | DMA Acknowledge 7 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller. |
| 36 (D15) | DRQ7 | DMA Request 7 – Used by I/O resources to request DMA service. Must be held high until associated DACK7 line is active. |
| 37 (D16) | +5V | +5 volts ±5% power supply |
| 38 (D17) | MASTER* | Bus Master Assert – This signal is used by an ISA board along with a DRQ line to gain ownership of the ISA bus. Upon receiving a -DACK a device can pull -MASTER low which will allow it to control the system address, data, and control lines. After -MASTER is low, the device should wait one CLK period before driving the address and data lines, and two clock periods before issuing a read or write command. |
| 39 (D18) | GND | Ground |
| 40 (D19) | GND | Ground |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

# IDE Interface (J6, J7)

The LittleBoard 800 provides two IDE connectors for primary and secondary IDE signals.

The EIDE interface logic supports the following features:

- Bus master IDE transfer rate up to 100Mbps when 80-pin grounded shielded cable is used
- Increase reliability using Ultra DMA 33/66/100 transfer protocols
- Full scatter-gather capability
- Supports ATAPI and DVD compliant devices
- PIO IDE transfers as fast as 14Mbps.
- Single Bus Master EIDE
- Supports two IDE drives per interface (primary or secondary)

Tables 3-9 and 3-10 lists the signals for the two IDE 40 pin connectors, with 2 rows, odd/even, (1, 2), 0.100" pin spacing.

**Table 3-9. Primary IDE Interface Pin/Signal Descriptions (J6)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | RESET* | Low active hardware reset (RSTDRV inverted) |
| 2 | GND | Ground |
| 3 | PD7 | Primary Disk Data 7 – These signals (0 to 15) provide the disk data signals. |
| 4 | PD8 | Primary Disk Data 8 – These signals (0 to 15) provide the disk data signals. |
| 5 | PD6 | Primary Disk Data 6 – These signals (0 to 15) provide the disk data signals. |
| 6 | PD9 | Primary Disk Data 9 – These signals (0 to 15) provide the disk data signals. |
| 7 | PD5 | Primary Disk Data 5 – These signals (0 to 15) provide the disk data signals. |
| 8 | PD10 | Primary Disk Data 10 – These signals (0 to 15) provide the disk data signals. |
| 9 | PD4 | Primary Disk Data 4 – These signals (0 to 15) provide the disk data signals. |
| 10 | PD11 | Primary Disk Data 11 – These signals (0 to 15) provide the disk data signals. |
| 11 | PD3 | Primary Disk Data 3 – These signals (0 to 15) provide the disk data signals. |
| 12 | PD12 | Primary Disk Data 12 – These signals (0 to 15) provide the disk data signals. |
| 13 | PD2 | Primary Disk Data 2 – These signals (0 to 15) provide the disk data signals. |
| 14 | PD13 | Primary Disk Data 13 – These signals (0 to 15) provide the disk data signals. |
| 15 | PD1 | Primary Disk Data 1 – These signals (0 to 15) provide the disk data signals. |
| 16 | PD14 | Primary Disk Data 14 – These signals (0 to 15) provide the disk data signals. |
| 17 | PD0 | Primary Disk Data 0 – These signals (0 to 15) provide the disk data signals. |
| 18 | PD15 | Primary Disk Data 15 – These signals (0 to 15) provide the disk data signals. |
| 19 | GND | Ground |
| 20 | NC/Key | Not Connected - Key pin plug |
| 21 | PDDREQ | Primary Device DMA Channel Request – Used for DMA transfers between host and drive (direction of transfer controlled by DIOR* and DIOW*). Also used in an asynchronous mode with DMACK*. Drive asserts IDRQ0 when ready to transfer or receive data. |
| 22 | GND | Ground |

| Pin # | Signal | Description |
|---|---|---|
| 23 | PDIOW* | Primary I/O Read/Write Strobe – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host. |
| 24 | GND | Ground |
| 25 | PDIOR* | Primary I/O Read/Write Strobe – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host. |
| 26 | GND | Ground |
| 27 | PDIORDY | Primary I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted. |
| 28 | NC | Not connected |
| 29 | PDACK* | Primary Cable Select – Used to configure IDE drives as device 0 or device 1 using a special cable |
| 30 | GND | Ground |
| 31 | IRQ14 | Interrupt Request 14 – Asserted by drive when it has pending interrupt (PIO transfer of data to or from the drive to the host). |
| 32 | NC | Not connected |
| 33 | PDA1 | Primary ATA Disk Address – Used (0 to 2) to indicate which byte in the ATA command block or control block is being accessed |
| 34 | PDIAG | UDMA 33/66 Sense – Senses which DMA mode to use for IDE devices. |
| 35 | PDA0 | Primary ATA Disk Address – Used (0 to 2) to indicate which byte in the ATA command block or control block is being accessed |
| 36 | PDA2 | Primary ATA Disk Address – Used (0 to 2) to indicate which byte in the ATA command block or control block is being accessed |
| 37 | PDCS1 | Primary Slave/Master Chip Select 1 – Used to select the host-accessible Command Block Register. |
| 38 | PDCS3 | Primary Slave/Master Chip Select 3 – Used to select the host-accessible Command Block Register. |
| 39 | NC | Not connected |
| 40 | GND | Ground |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

**Table 3-10. Secondary IDE Interface Pin/Signal Descriptions (J7)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | RESET* | Low active hardware reset (RSTDRV inverted) |
| 2 | GND | Ground |
| 3 | SDD7 | Secondary Disk Data 7 – These signals (0 to 15) provide the disk data signals. |
| 4 | SDD8 | Secondary Disk Data 8 – These signals (0 to 15) provide the disk data signals. |
| 5 | SDD6 | Secondary Disk Data 6 – These signals (0 to 15) provide the disk data signals. |
| 6 | SDD9 | Secondary Disk Data 9 – These signals (0 to 15) provide the disk data signals. |
| 7 | SDD5 | Secondary Disk Data 5 – These signals (0 to 15) provide the disk data signals. |
| 8 | SDD10 | Secondary Disk Data 10 – These signals (0 to 15) provide the disk data signals. |
| 9 | SDD4 | Secondary Disk Data 4 – These signals (0 to 15) provide the disk data signals. |

| Pin # | Signal | Description |
|---|---|---|
| 10 | SDD11 | Secondary Disk Data 11 – These signals (0 to 15) provide the disk data signals. |
| 11 | SDD3 | Secondary Disk Data 3 – These signals (0 to 15) provide the disk data signals. |
| 12 | SD12 | Secondary Disk Data 12 – These signals (0 to 15) provide the disk data signals. |
| 13 | SDD2 | Secondary Disk Data 2 – These signals (0 to 15) provide the disk data signals. |
| 14 | SDD13 | Secondary Disk Data 13 – These signals (0 to 15) provide the disk data signals. |
| 15 | SDD1 | Secondary Disk Data 1 – These signals (0 to 15) provide the disk data signals. |
| 16 | SDD14 | Secondary Disk Data 14 – These signals (0 to 15) provide the disk data signals. |
| 17 | SDD0 | Secondary Disk Data 0 – These signals (0 to 15) provide the disk data signals. |
| 18 | SDD15 | Secondary Disk Data 15 – These signals (0 to 15) provide the disk data signals. |
| 19 | GND | Ground |
| 20 | NC/Key | Not Connected - Key pin plug |
| 21 | SDDREQ | Secondary DMA Channel Request – Used for DMA transfers between host and drive (direction of transfer controlled by DIOR* and DIOW*). Also used in an asynchronous mode with DMACK*. Drive asserts IDRQ0 when ready to transfer or receive data. |
| 22 | GND | Ground |
| 23 | SDIOW* | Secondary I/O Read/Write Strobe – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host. |
| 24 | GND | Ground |
| 25 | SDIOR* | Secondary I/O Read/Write Strobe – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host. |
| 26 | GND | Ground |
| 27 | SIORDY | Secondary I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted. |
| 28 | CSEL | Not connected |
| 29 | SDACK* | Secondary Cable Select – Used to configure IDE drives as device 0 or device 1 using a special cable |
| 30 | GND | Ground |
| 31 | IRQ15 | Interrupt Request 15 – Asserted by drive when it has pending interrupt (PIO transfer of data to or from the drive to the host). |
| 32 | NC | Not connected |
| 33 | SDA1 | Secondary IDE ATA Disk Address 1 – Used (0 to 2) to indicate which byte in the ATA command block or control block is being accessed |
| 34 | SPDIAG | UDMA 33/66 Sense – Senses which DMA mode to use for IDE devices. |
| 35 | SDA0 | Secondary IDE ATA Disk Address 0 – Used (0 to 2) to indicate which byte in the ATA command block or control block is being accessed |
| 36 | SDA2 | Secondary IDE ATA Disk Address 2 – Used (0 to 2) to indicate which byte in the ATA command block or control block is being accessed |
| 37 | SDCS1 | Secondary Slave/Master Chip Select 1 – Used to select the host-accessible Command Block Register. |

| Pin # | Signal | Description |
|---|---|---|
| 38 | SDCS3 | Secondary Slave/Master Chip Select 3 – Used to select the host-accessible Command Block Register. |
| 39 | NC | Not connected |
| 40 | GND | Ground |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

# CompactFlash Socket (J8)

The board contains a Type II PC card socket, which allows for the insertion of a CompactFlash (CF) Card. The CompactFlash Card acts as a standard IDE Drive and is connected to the secondary IDE bus. If a CompactFlash card is installed, only one additional IDE drive may be added to the secondary bus. Jumpers are used to select the Master/Slave mode and the voltage selection (+5V or +3.3V). Refer to Table 2-5, Jumper Settings for more information. The CompactFlash socket has 50 pins, 2 rows, consecutive (1, 26), with 1.27mm pin spacing.

| | |
|---|---|
| **CAUTION** | To prevent system hangs when using older CompactFlash cards, ensure your CompactFlash is compatible with UDMA 100 IDE hard disk drives. Consult your CompactFlash card vendor for UDMA 100 compatibility. |

**Table 3-11. CompactFlash Interface Pin/Signal Descriptions (J8)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | GND | Ground |
| 2 | SD3 | Secondary Disk Data 3 – These signals (D0-D15) carry the Data, Commands, and Status between the host and the controller. D0 is the LSB of the even Byte of the Word. D8 is the LSB of the Odd Byte of the Word. All Task File operations occur in byte mode on the low order bus D0-D7, while all data transfers are 16 bit using D0-D15 to provide the disk data signals. |
| 3 | SD4 | Secondary Disk Data 4 – Refer to SD3 on pin-2 for more information. |
| 4 | SD5 | Secondary Disk Data 5 – Refer to SD3 on pin-2 for more information. |
| 5 | SD6 | Secondary Disk Data 6 – Refer to SD3 on pin-2 for more information. |
| 6 | SD7 | Secondary Disk Data 7 – Refer to SD3 on pin-2 for more information. |
| 7 | SDCS1* | Secondary Chip Select 1 – This signal, along with CE2*, selects the CF and indicates to the CF when a byte or word operation is being performed. This signal accesses the even byte or odd byte of the word depending on A0 and CE2*. |
| 8, 9, 10, 11, 12 | GND | Ground |
| 13 | VCC | Voltage Jumper (JP3) – Selects voltage; pins 1-2 = +5V or pins 2-3 = +3.3V. |
| 14, 15, 16, 17 | GND | Ground |
| 18 | SA2 | Secondary Address Select 2 – One of three signals (0 – 2) used to select one of eight registers in the Task File. The host grounds all remaining address lines. |
| 19 | SA1 | Secondary Address Select 1 – Refer to SA2 on pin-18 for more information. |
| 20 | SA0 | Secondary Address Select 0 – Refer to SA2 on pin-18 for more information. |

| Pin # | Signal | Description |
|---|---|---|
| 21 | SD0 | Secondary Disk Data 0 – Refer to SD3 on pin-2 for more information. |
| 22 | SD1 | Secondary Disk Data 1 – Refer to SD3 on pin-2 for more information. |
| 23 | SD2 | Secondary Disk Data 2 – Refer to SD3 on pin-2 for more information. |
| 24 | NU | Not used (IOIS16*, connected through 10k ohm resistor to VCC) |
| 25 | NU | Not used (CD2*, connected through 10k ohm resistor to VCC) |
| 26 | NU | Not used (CD1*, connected through 10k ohm resistor to VCC) |
| 27 | SD11 | Secondary Disk Data 11 – Refer to SD3 on pin-2 for more information. |
| 28 | SD12 | Secondary Disk Data 12 – Refer to SD3 on pin-2 for more information. |
| 29 | SD13 | Secondary Disk Data 13 – Refer to SD3 on pin-2 for more information. |
| 30 | SD14 | Secondary Disk Data 14 – Refer to SD3 on pin-2 for more information. |
| 31 | SD15 | Secondary Disk Data 15 – Refer to SD3 on pin-2 for more information. |
| 32 | SDCS3* | Secondary Slave/Master Chip Select – This signal, along with CE1*, selects the CompactFlash card and indicates to the card when a byte or word operation is being performed. This signal always accesses the odd byte of the word. |
| 33 | NU | Not used (VS1*, connected through 10k ohm resistor to VCC) |
| 34 | SIOR* | Secondary I/O Read/Write Strobe – This signal is generated by the host and gates the I/O data onto the bus from the CompactFlash card when the card is configured to use the I/O interface. |
| 35 | SIOW* | Secondary I/O Read/Write Strobe – This signal is generated by the host and clocks the I/O data on the Card Data bus into the CompactFlash card controller registers when the card is configured to use the I/O interface. The clock occurs on the negative to positive edge of the signal (trailing edge). |
| 36 | NU | Not used (WE*, connected through 10k ohm resistor to VCC) |
| 37 | IRQ15 | Interrupt Request 15 – IRQ 15 is asserted by drive (CF) when it has a pending interrupt (PIO transfer of data to or from the drive to the host). |
| 38 | VCC | Voltage Jumper (JP3) – Selects voltage; pins 1-2 = +5V or pins 2-3 = +3.3V. |
| 39 | Mas/Slv* | Master/Slave – This pin determines the Master or Slave configuration of the CompactFlash by jumper (JP2) setting. When this pin is grounded (jumper inserted pins 2-3), CF is configured as Master. When this pin is open (jumper inserted pins 1-2), CF is configured as Slave (**Default**). |
| 40 | NU | Not used (VS2*, connected through 10k ohm resistor to VCC) |
| 41 | CFRST* | CF Reset – This input signal is the active low hardware reset from the host. If this pin goes high, it is used as the reset signal. This pin is driven high at power-up, causing a reset, and if left high will cause another reset. |
| 42 | SIORDY | Secondary I/O DMA Channel Ready – When negated, extends the host transfer cycle of any host register access when the CF is not ready to respond to a data transfer request. High impedance if asserted. |
| 43 | NC | Not Connected (InpAck) |
| 44 | NU | Not used (REG*, connected through 10k ohm resistor to VCC) |
| 45 | NU | Not used (ACT/SLV, connected through 10k ohm resistor to VCC) |
| 46 | SPDIAG | Secondary Pass Diagnostic – This input / output signal is used in the Master/Slave handshake protocol. |

| Pin # | Signal | Description |
|---|---|---|
| 47 | SD8 | Secondary Disk Data 8 – Refer to SD3 on pin-2 for more information. |
| 48 | SD9 | Secondary Disk Data 9 – Refer to SD3 on pin-2 for more information. |
| 49 | SD10 | Secondary Disk Data 10 – Refer to SD3 on pin-2 for more information. |
| 50 | GND | Ground |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

# Floppy Drive Interface (J17)

The LPC47B272 chip provides the floppy controller and supports one floppy drive as configured. The floppy signals are provided through the standard 34-pin connector (J17). This connector is separate (not shared with) from the parallel port connector (J16). The floppy controller will support a 360k, 720k, 1.2M, 1.44M, or 2.88M drive.

The floppy drive connector has 34 pins, 2 rows, odd/even, (1, 2) with 0.100" pin spacing.

**Table 3-12. Floppy Drive Interface Pin/Signal Descriptions (J17)**

| Pin # | Signal | Description |
|---|---|---|
| 2 | DRVEN0 | Drive (Floppy) Density Select 0 |
| 4 | NC | Not connected |
| 6 | DRVEN0 | Drive (Floppy) Density Select 0 |
| 8 | INDEX | Index – Sense to detect that the head is positioned over the beginning of a track |
| 10 | MTR0 | Motor Control 0 – Select motor on drive 0. |
| 12 | NC | Not Connected (DS1) |
| 14 | DS0 | Drive Select 0 – Select drive 0. |
| 16 | NC | Not Connected (MTR1) |
| 18 | DIR | Direction – Direction of head movement (0 = inward motion, 1 = outward motion). |
| 20 | STEP | Step – Low pulse for each track-to-track movement of the head. |
| 22 | WDATA | Write Data – Encoded data to the drive for write operations. |
| 24 | WGATE | Write Gate – Signal to the drive to enable current flow in the write head. |
| 26 | TRK0 | Track 0 – Sense detects the head is positioned over track 0. |
| 28 | WRTPRT | Write Protect – Senses the diskette is write protected. |
| 29 | NC | Not Connected (NC1) |
| 30 | RDATA | Read Data – Raw serial bit stream from the drive for read operations. |
| 32 | HDSEL | Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0) |
| 33 | NC | Not Connected (NC2) |
| 34 | DSKCHG | Disk Change – Senses the drive door is open or the diskette has been changed since the last drive selection. |
| 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 31 | GND | Ground |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

# Parallel Port Interface (J16)

Parallel port supports standard parallel, Bi-directional, ECP and EPP protocols. The LPC47B272 provides separate parallel port interface signals not shared with the floppy drive signals.

The parallel connector has 26 pins, 2 rows, odd/even, (1, 2), with 0.100" pin spacing.

**Table 3-13. Parallel Interface Pin/Signal Descriptions (J16)**

| Pin # | Signal | In/Out | Description |
|---|---|---|---|
| 1 | Strobe* | Out | Strobe* – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode. |
| 2 | AFD* | Out | Auto Feed* – This is a request signal into the printer to automatically feed one line after each line is printed. |
| 3 | PD0 | I/O | Parallel Port Data 0 – These pins (0 to 7) provide parallel port data. |
| 4 | ERR* | Out | Error* – This is a status output signal from the printer. A Low State indicates an error condition on the printer. |
| 5 | PD1 | I/O | Parallel Port Data 1 – Refer to pin-3 for more information. |
| 6 | INIT* | Out | Initialize* – This signal used to Initialize printer. Output in standard mode, I/O in ECP/EPP mode. |
| 7 | PD2 | I/O | Parallel Port Data 2 – Refer to pin-3 for more information. |
| 8 | SLIN | Out | Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode. |
| 9 | PD3 | I/O | Parallel Port Data 3 – Refer to pin-3 for more information. |
| 10, 12 | GND | | Ground |
| 11 | PD4 | I/O | Parallel Port Data 4 – Refer to pin-3 for more information. |
| 13 | PD5 | I/O | Parallel Port Data 5 – Refer to pin-3 for more information. |
| 14, 16 | GND | | Ground |
| 15 | PD6 | I/O | Parallel Port Data 6 – Refer to pin-3 for more information. |
| 17 | PD7 | I/O | Parallel Port Data 7 – Refer to pin-3 for more information. |
| 18, 20 | GND | | Ground |
| 19 | ACK* | In | Acknowledge* – This printer output status indicates it has received the data and is ready to accept new data if the signal state is Low. |
| 21 | BUSY | In | Busy – This printer output status indicates the printer is not ready to accept data if the signal state is High. |
| 22, 24 | GND | | Ground |
| 23 | PE | In | Paper End – The printer output status indicates the printer is out of paper if the signal state is High. |
| 25 | SLCT | In | Select – This printer output status indicates the printer is selected and powered on if the signal state is high. |
| 26 | Key/NC | | Key - Not connected |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

# Serial Interfaces (J11, J12)

Two LPC47B272 chips provide the circuitry for the 4 serial ports. One chip provides serial ports 1 and 2 through connector J11 and the second chip provides serial ports 3 and 4 through connector J12. The four serial ports support the following features:

- Four individual 16550-compatible UARTs
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Four individual 16-bit FIFOs
- Serial A Interface (J11)
  - Serial Port 1 (COM1) supports RS232/RS485/RS422 and full modem support
  - Serial Port 2 (COM2) supports RS232/RS485/RS422
- Serial B Interface (J12)
  - Serial Port 3 (COM3) supports RS232/RS485/RS422 and full modem support
  - Serial Port 4 (COM4) supports RS232/RS485/RS422

| NOTE | The RS232 and RS485/RS422 modes can be selected for any serial port in BIOS Setup under the *BIOS and Hardware Settings* menu. However, the RS232 mode is the default selection (Standard) for any serial port. Refer to Table 2-5 for termination jumper settings. |
|---|---|

To implement the two-wire RS485 mode on any serial port, you must tie the equivalent pins together for each port.

For example; on Serial Port 1, tie pin 3 to 5 and pin 4 to 6 at the Serial A interface connector (J11) as shown in Figure 3-1. As an alternate, tie pin 2 to 3 and pin 7 to 8 at the DB9 serial connector for Serial Port 1 as shown in Figure 3-1. Refer also to the following tables for the specific pins for the other ports on each connector. The RS422 mode uses a four-wire interface and does not need any pins tied together, but you must select RS485 in BIOS Setup.

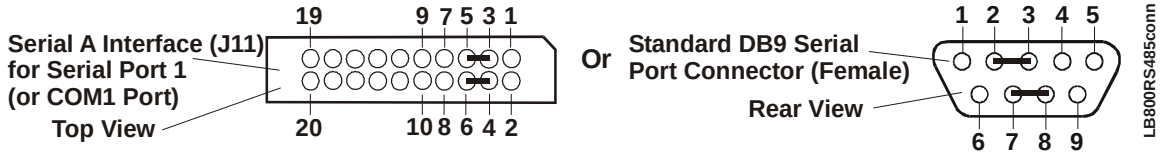



**Figure 3-1. RS485 Serial Port Implementation**

Table 3-14 gives the pins and corresponding signals for the Serial A interface connector (Serial Ports 1 and 2) and Table 3-15 gives the pins and corresponding signals for the Serial B interface connector (Serial Ports 3 and 4).

Both Serial A and B connectors have 20 pins, 2 rows, odd/even, (1, 2), with 0.100” pin spacing.

**Table 3-14. Serial A Interface Pin/Signal Descriptions (J11)**

| Pin # | Pin # DB9 | Signal | Description |
|---|---|---|---|
| 1 | 1 (COM1) | DCD1* | Data Carrier Detect 1 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR1 as part of the DTR/DSR handshake. |
| 2 | 6 | DSR1* | Data Set Ready 1 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate. |
| 3 | 2 | RXD1<br>RX1- | Receive Data 1 – Serial port 1 receive data in.<br>RX1- – If in RS485 or RS422 mode, this pin is Receive Data 1 -. |
| 4 | 7 | RTS1*<br>TX1+ | Request To Send 1 – Indicates Serial port 1 is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.<br>TX1+ – If in RS485 or RS422 mode, this pin is Transmit Data 1 +. |
| 5 | 3 | TXD1<br>TX1- | Transmit Data 1 – Serial port 1 transmit data out.<br>TX1- – If in RS485 or RS422 mode, this pin is Transmit Data 1 -. |
| 6 | 8 | CTS1*<br>RX1+ | Clear to Send 1 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.<br>RX1+ – If in RS485 or RS422 mode, this pin is Receive Data 1 -. |
| 7 | 4 | DTR1* | Data Terminal Ready 1 – Indicates this Serial port is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate. |
| 8 | 9 | RI1* | Ring Indicator 1 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. |
| 9 | 5 | GND | Ground |
| 10 | NC | KEY/ NC | Key<br>Not connected |
| 11 | 1 (COM2) | DCD2* | Data Carrier Detect 2 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR2 as part of the DTR/DSR handshake. |
| 12 | 6 | DSR2* | Data Set Ready 2 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate. |
| 13 | 2 | RXD2<br>RX2- | Receive Data 2 – Serial port 2 receive data in<br>RX1- – If in RS485 or RS422 mode, this pin is Receive Data 1 -. |
| 14 | 7 | RTS2*<br>TX2+ | Request To Send 2 – Indicates Serial port 2 is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.<br>TX2+ – If in RS485 or RS422 mode, this pin is Transmit Data 2 +. |
| 15 | 3 | TXD2<br>TX2- | Transmit Data 2 – Serial port 2 transmit data out<br>TX2- – If in RS485 or RS422 mode, this pin is Transmit Data 2 -. |

| Pin # | Pin # DB9 | Signal | Description |
|---|---|---|---|
| 16 | 8 | CTS2* | Clear To Send 2 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control. |
| | | RX2+ | RX2+ – If in RS485 or RS422 mode, this pin is Receive Data 2 -. |
| 17 | 4 | DTR2* | Data Terminal Ready 2 – Indicates Serial port 1 is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate. |
| 18 | 9 | NC | Not Connected (Ring Indicator 2) |
| 19 | 5 | GND | Ground |
| 20 | NC | NC | Not connected |

**Notes:** The shaded area denotes power or ground. Signals are listed in the table with RS232 first, followed by RS485/RS422.

**Table 3-15. Serial B Interface Pin/Signal Descriptions (J12)**

| Pin # | Pin # DB9 | Signal | Description |
|---|---|---|---|
| 1 | 1 (COM3) | DCD3* | Data Carrier Detect 3 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR3 as part of the DTR/DSR handshake. |
| 2 | 6 | DSR3* | Data Set Ready 3 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR3 for overall readiness to communicate. |
| 3 | 2 | RXD3 | Receive Data 3 – Serial port 3 receive data in |
| | | RX3- | RX3- – If in RS485 or RS422 mode, this pin is Receive Data 3 -. |
| 4 | 7 | RTS3* | Request To Send 3 – Indicates Serial port 3 is ready to transmit data. Used as hardware handshake with CTS3 for low level flow control. |
| | | TX3+ | TX3+ – If in RS485 or RS422 mode, this pin is Transmit Data 3 +. |
| 5 | 3 | TXD3 | Transmit Data 3 – Serial port 3 transmit data out |
| | | TX3- | TX3- – If in RS485 or RS422 mode, this pin is Transmit Data 3 -. |
| 6 | 8 | CTS3* | Clear To Send 3 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS3 for low level flow control. |
| | | RX3+ | RX3+ – If in RS485 or RS422 mode, this pin is Receive Data 3 -. |
| 7 | 4 | DTR3* | Data Terminal Ready 3 – Indicates this Serial port is powered, initialized, and ready. Used as hardware handshake with DSR3 for overall readiness to communicate. |
| 8 | 9 | RI3* | Ring Indicator 3 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. |
| 9 | 5 | GND | Ground |
| 10 | NC | KEY | Not Connected |

| Pin # | Pin # DB9 | Signal | Description |
|---|---|---|---|
| 11 | 1 (COM4) | DCD4* | Data Carrier Detect 4 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR4 as part of the DTR/DSR handshake. |
| 12 | 6 | DSR4* | Data Set Ready 4 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR4 for overall readiness to communicate. |
| 13 | 2 | RXD4<br>RX4- | Receive Data 4 – Serial port 4 receive data in<br>RX4- – If in RS485 or RS422 mode, this pin is Receive Data 4 -. |
| 14 | 7 | RTS4*<br>TX4+ | Request To Send 4 – Indicator to serial output port 4 is ready to transmit data. Used as hardware handshake with CTS4 for low level flow control.<br>TX4+ – If in RS485 or RS422 mode, this pin is Transmit Data 4 +. |
| 15 | 3 | TXD4<br>TX4- | Transmit Data 4 – Serial port 4 transmit data out<br>TX4- – If in RS485 or RS422 mode, this pin is Transmit Data 4 -. |
| 16 | 8 | CTS4*<br>RX4+ | Clear To Send 4 – Indicator to serial port 4 that external serial communications device is ready to receive data. Used as hardware handshake with RTS4 for low level flow control.<br>RX4+ – If in RS485 or RS422 mode, this pin is Receive Data 4 +. |
| 17 | 4 | DTR4* | Data Terminal Ready 4 – Indicates this Serial port is powered, initialized, and ready. Used as hardware handshake with DSR4 for overall readiness to communicate. |
| 18 | 9 | NC | Not connected (Ring Indicator 4) |
| 19 | 5 | GND | Ground |
| 20 | NC | NC | Not connected |

**Notes:** The shaded area denotes power or ground. Signals are listed in the table with RS232 first, followed by RS485/RS422.

# Utility Interfaces

The Utility interfaces consists of three connectors that provide the standard interface signals for the following devices:

- Utility 1 (J15)
  - Keyboard
  - External battery connection
  - Reset Switch
  - Speaker
- Utility 2 (J13)
  - PS/2 Mouse
  - Infrared (IrDA) signals
  - SMBus signals
  - USB signals for USB ports 1 and 2
  - Power button signal
- Utility 3 (J14)
  - USB signals for USB ports 3 (USB0) and 4 (and USB1)

# Utility 1 Interface (J15)

The Utility 1 (J15) interface uses an 18-pin connector and provides the various interface signals to an external I/O board with external connections for the respective connectors, such as, keyboard, speaker, etc. Table 3-17 gives the pin-outs and interface signals for Utility 1 interface and has 16 pins, 2 rows, odd/even, (1, 2) with 0.100" pin spacing.

- Keyboard
- Battery
- Reset Switch
- Speaker
- External voltages (-5V In, -12V In, +3.3V Out to Power On LED)

## Keyboard Interface

The signal lines for a PS/2 keyboard are provided through the Utility 1 interface (J15), which is also fully PC/AT compatible.

## External Battery

An external battery input connection is provided through a Utility 1 interface (J15) for the Real Time Clock's operation in the event the on-board battery is not used.

## Reset Switch

The signal lines for a reset switch (hard or soft) are provided through the Utility 1 interface (J15).

| NOTE | To perform the equivalent of a power-on reset, the reset button must be pressed and held for a minimum of three seconds. |
|---|---|

### Speaker

The signal lines for a speaker port with 0.1-watt drive are provided through a Utility 1 interface (J15).

**Table 3-16. Utility 1 Interface Pin/Signal Descriptions (J15)**

| Pin # | Signal | I/O | Description |
|---|---|---|---|
| 1 | -12V | I | -12 Volts – Supplied from external power source. |
| 2 | GND | I | Ground |
| 3 | -5V | I | -5 Volts – Supplied from external power source. |
| 4 | GND | I | Ground |
| 5 | PwrLED | O | Power On LED – This on-board +3.3 volts is provided through 330 ohm resistor to an external Power-On LED. |
| 6 | NC | - | Not connected (Power Good) |
| 7 | SPKR+ | O | + Speaker Output – This signal drives external PC "Beep" speaker. |
| 8 | GND | I | Ground |
| 9 | RSTSW* | I | Reset Switch – This signal (ground) provided from external reset switch. |
| 10 | NC | - | Not connected (Keyboard Switch) |
| 11 | KBDATA | I/O | Keyboard Data – Data signal provided to external keyboard connector. |
| 12 | KBCLK | I/O | Keyboard Clock – Clock signal provided to external keyboard connector. |
| 13 | GND | I | Keyboard Ground |
| 14 | KBDPWR | O | Keyboard Power – This +5 volts is provided to external keyboard connector. Requires external fuse for keyboard/mouse protection. |
| 15 | BATV+ | I | Backup Battery – This connection provides an additional backup battery from an external source. It can also be used in place of the on-board backup battery, B1, shipped with all LittleBoard 800s. Each RTS battery input is protected with a zener diode. |
| 16 | BATV- | I | Battery - Return (Grounded) |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

# Utility 2 Interface (J13)

The Utility 2 interface consists of a 24-pin connector used to interface various signals to the external board with external connections, or directly to the respective connector such as, the mouse, USB, etc. Table 3-18 gives the pin-outs and interface signals for the Utility 2 interface and it has 24 pins, 2 rows, odd/even, (1, 2) with 0.100" pin spacing.

- PS/2 Mouse signals
- Infrared (IrDA) signals
- SMBus signals
- USB signals for USB ports 1 and 2
- Power button signal

### System Management Bus (SMBus)

The I/O Hub, 82801DBM, (Southbridge) contains both a host and slave SMBus port; but the host cannot access the slave internally. The slave port allows an external master access to the I/O Hub through the connector (J13). The master contained in the 82801DBM is used to communicate with the SDRAM DDR DIMM, 82541(GI/PI) Gigabit Ethernet controller, and the clock generator. Table 3-17 gives the addresses for these devices with the components and corresponding binary addresses of the SMBus.

**Table 3-17. SMBus Reserved Addresses**

| Component | Address Binary |
|---|---|
| SDRAM EPROM | $1010,000x_b$ |
| Clock Generator (ICS950811) | $1101,001x_b$ |
| I/O Hub (82801DBM) | $0000,000x_b$ (default) Programmable Master |

## USB Signals (USB1 and USB2)

The LittleBoard 800 contains one root USB hub with four functional USB ports. This connector (Utility 2) provides two of the four USB ports (USB1 and USB2). The hub is USB V2.0 and Universal UHCI V1.1 compatible.

Features implemented in the USB ports include the following:

- Provides two root USB hubs
- Provides up to four USB ports
- Supports USB v2.0 and Universal UHCI v1.1
- Integrated physical layer transceivers
- Over-current detection status (software) on all four USB ports

| NOTE | Ampro does not recommend connecting a USB boot device to the LittleBoard 800 through an external hub. Instead, connect the USB boot device directly to the LittleBoard 800. Refer to Chapter 4, BIOS Setup for more information. |
|---|---|

## Mouse Interface

The signal lines for a PS/2 mouse are provided through the Utility 2 interface (J13).

## Infrared Port (IrDA)

The Infrared Data Association (IrDA) port provides a two-way wireless communications port using infrared as a transmission medium at the basic level. There are two basic infrared implementations provided; the Hewlett-Packard Serial Infrared (HPSIR) and the Amplitude Shift Keyed Infrared (ASKIR) methods. HPSIR is a serial implementation of infrared developed by Hewlett-Packard. The IrDA (HPSIR and ASKIR) signals are available on the Utility 2 connector.

The HPSIR method allows serial communication at baud rates up to 115k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a single infrared pulse is sent at the beginning of the serial bit time. A one is sent when no infrared pulse is sent during the bit time.

The Amplitude Shift Keyed infrared (ASKIR) allows serial communication at baud rates up to 19.2k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a 500kHz waveform is sent for the duration of the serial bit time. A one is sent when no transmission is sent during the serial bit time.

Both of these methods require an understanding of the timing diagrams provided in the Super I/O-1 controller chip (LPC47B272) specifications available from the manufacture's web site and referenced earlier in this manual. For more information, refer to the SMSC LPC47B272 chip databook and the Infrared Data Association web site at http://www.irda.org.

| NOTE | For faster speeds and infrared applications not covered in this brief description, refer to the LPC47B272 chip specifications by Standard Microsystems Corp. |
|---|---|

**Table 3-18. Utility 2 Interface Pin/Signal Descriptions (J13)**

| Pin # | Signal | I/O | Description |
|---|---|---|---|
| 1 | LIDSW | - | Lid Switch – This signal (Suspend Status on I/O Hub) is asserted by the I/O Hub to indicate the system will be entering a low power state soon. This signal is not shared with other devices on the LittleBoard. This signal is similar to the Lid Switch on laptop computer. |
| 2 | PWRBT* | I | Power Button – This signal from an external switch to the I/O Hub is not used with AT Power supplies. |
| 3 | BATLOW* | | Battery Low – This signal from external battery indicates to the I/O Hub there is insufficient power to boot the system. |
| 4 | NC | O | Not connected (IR Mode select) |
| 5 | IRTX | O | IR Transmit Data – This signal goes to external IrDA Transceiver. |
| 6 | IRRX | I | IR Receive Data – This signal comes from external IrDA Transceiver. |
| 7 | GND | - | Ground |
| 8 | VCC | - | +5 Volts |
| 9 | MDATA | I/O | Mouse Data – Data signal provided to external mouse connector. |
| 10 | MCLK | I/O | Mouse Clock– Clock signal provided to external mouse connector |
| 11 | GND | - | Ground |
| 12 | VCC | - | +5 Volts |
| 13 | SMBCLK | - | SMBus Clock – Clock signal provided to external devices. |
| 14 | SMBDATA | - | SMBus Data – Data signal provided to external devices. |
| 15 | USBPWR1 | - | +5V USB Port Power – Port is disabled if this input is low. |
| 16 | USBPWR2 | - | +5V USB Port Power – Port is disabled if this input is low. |
| 17 | USBP1- | I/O | USB 1 Negative Data Signal |
| 18 | USBP2- | I/O | USB 2 Negative Data Signal |
| 19 | USBP1+ | I/O | USB 1 Positive Data Signal |
| 20 | USBP2+ | I/O | USB 2 Positive Data Signal |
| 21 | USBGND1 | - | USB Port ground |
| 22 | USBGND2 | - | USB Port ground |
| 23 | SHIELD1 | - | USB Port shield (Cable Shield) |
| 24 | SHIELD2 | - | USB Port shield (Cable Shield) |

**Notes:** The shaded area denotes power or ground. The signals marked with * = Negative true logic.

# Utility 3 Interface (J14)

The Utility 3 interface is a 10-pin connector used to provide two of the four USB port signals to an external board with USB connections or directly to the respective USB connector for the USB ports. Table 3-19 gives the pin-outs and interface signals for the Utility 3 interface and it has 24 pins, 2 rows, odd/even, (1, 2) with 0.100" pin spacing.

- USB ports 3 (USB3) and 4 (USB4)

## USB Signals (USB3 and USB4)

The LittleBoard 800 contains one root USB hub with four functional USB ports. This connector (Utility 3) provides two (USB3 and USB4) of the four USB ports. The hub is USB V2.0 and Universal UHCI V1.1 compatible.

Features implemented for the USB ports include the following:

- One root hub and two USB ports on this connector
- USB V2.0 and Universal UHCI V1.1 compatible
- Integrated physical layer transceivers
- Over-current detection status on the USB port (software)

| NOTE | Ampro does not recommend connecting a USB boot device to the LittleBoard 800 through an external hub. Instead, connect the USB boot device directly to the LittleBoard 800. Refer to Chapter 4, BIOS Setup for more information. |
|---|---|

**Table 3-19. Utility 3 Interface Pin/Signal Descriptions (J18)**

| Pin # | Signal | I/O | Description |
|---|---|---|---|
| 1 | USBPWR3 | - | +5V USB Port Power – Port is disabled if this input is low. |
| 2 | USBPWR4 | - | +5V USB Port Power – Port is disabled if this input is low. |
| 3 | USBP3- | I/O | USB 3 Negative Data Signal |
| 4 | USBP4- | I/O | USB 4 Negative Data Signal |
| 5 | USBP3+ | I/O | USB 3 Positive Data Signal |
| 6 | USBP4+ | I/O | USB 4 Positive Data Signal |
| 7 | USBGND3 | - | USB Port ground |
| 8 | USBGND4 | - | USB Port ground |
| 9 | SHIELD3 | - | USB Port shield (Cable Shield) |
| 10 | SHIELD4 | - | USB Port shield (Cable Shield) |

**Note:** The shaded area denotes power or ground.

# Ethernet Interfaces (J10, J23)

The Ethernet solution is provided by two Intel Ethernet controllers, 82541ER, and (Gigabit) 82541GI/PI for Port 1 and Port 2 respectively. Both controllers consist of a Media Access Controller (MAC) and a physical layer (PHY) combined into a single component solution.

## 10/100BaseT Ethernet Controller (U9)

Ethernet Port 1 uses an Intel 82551ER, 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the 82551ER to perform high-speed data transfers over the PCI bus. The 82551ER bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU.

- Backward software compatible to the 82559, 82558, and 82557
- Chained memory structure
- Full duplex or half-duplex support
- Full duplex support at 10Mbps and 100Mbps
- In half-duplex mode, performance is enhanced by a proprietary collision reduction mechanism.
- IEEE 802.3 10BaseT/100BaseT compatible physical layer to wire transformer
- 2 LED support for each port (speed, and link and activity are shared)
- Data transmission with minimum interframe spacing (IFS).
- IEEE 802.3u Auto-Negotiation support
- 3kB transmit and 3kB receive FIFOs (helps prevent data underflow and overflow)
- IEEE 802.3x 100BASE-TX flow control support
- Improved dynamic transmit chaining with multiple priorities transmit queues
- Ethernet port has a RJ-45 connector and the related magnetics integrated on the board.
- Ethernet port controller is connected to PCI bus

Tables 3-20 describes the pin-outs and signals of standard Ethernet port, Ethernet Port 1.

| **CAUTION** | The two Ethernet ports share a common ground, that is floating until you determine how the grounds are connected, to signal ground or chassis ground. |
|---|---|

Tables 3-20 and 3-21 describe the pin-outs and signals of two Ethernet ports 1 and 2, respectively.

**Table 3-20. Ethernet Port 1 Pin/Signal Descriptions (J23)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | TX+ | Analog Twisted Pair Ethernet Transmit Differential Pair – These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair Cable (UTP). These signals interface directly with an isolation transformer. |
| 2 | TX- | |
| 3 | RX+ | Analog Twisted Pair Ethernet Receive Differential Pair – These pins receive the serial bit stream from the isolation transformer. |
| 6 | RX- | |
| 4, 5, 7, 8 | CT_TP | Center Tap – Connected to center tap of transformer and floating ground while isolated from board common ground by 1000pf capacitor. |
| 9 | SPEED | Speed LED – Indicates which transfer rate is being used, 10BaseT or 100BaseT. |
| 10 | VCC3 | +3.3 Volts – Voltage for plus side of LEDs. |
| 11 | LINK | Link LED – Indicates a Link is established between this port and another device. |
| 12 | ACT | Activity LED – Indicates Activity is occurring on the Ethernet link. |
| 13, 14 | SHLD | Shields – Connected to common board ground. |

**Note:** The shaded area denotes power or ground.

## Gigabit Ethernet Controller (U11)

The Intel® 82541(in GI or PI versions) Gigabit Ethernet Controller is 32-bit wide, PCI 2.3 compliant controller capable of transmitting and receiving data rates of 1000 Mbps, 100 Mbps, or 10 Mbps and transferring data over the PCI interface at 33MHz. The 82541GI/PI's gigabit MAC design fully integrates the physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BaseT, 100BaseTX, and 10BaseT applications (802.3, 802.3u, and 802.3ab).

The 82541GI/PI controller delivers high performance, PCI bus efficiency, with wide internal data paths to eliminate performance bottlenecks by efficiently handling large address and data words. This controller includes advanced interrupt handling features to limit PCI bus traffic and a PCI interface that maximizes the use of bursts for efficient bus usage. This controller caches up to 64 packet descriptors in a single burst with a large 64kByte on-chip packet buffer to maintain superior performance with efficient PCI bandwidth use, as available PCI bandwidth changes. In addition, using hardware acceleration, the controller offloads tasks from the host controller, such as TCP/UDP/IP checksum calculations and TCP segmentation. The 82541GI/PI Gigabit Ethernet controller supports or provides the following features:

- Low-latency transmit and receive queues to prevent waiting periods or buffer overflow
- Supports caches of 64 packet descriptors in a signal burst to provide efficient PCI bandwidth use
- Supports programmable host memory receive buffers (256 Bytes to 16kBytes) and cache line sizes (16 to 256 Bytes)
- Supports wide optimized internal data paths for low latency data handling and superior DMA transfer rates
- Supports 64kByte configurable Transmit and Receive FIFO buffers
- Supports simple programming model with descriptor ring transmit and receive management hardware
- Supports jumbo frames of 16kByte transmit and receive packets
- Supports maximized system performance and throughput with interrupt reduction of transmit and receive operations
- Full duplex or half-duplex support at 10Mbps, 100Mbps, and 1000Mbps
- Supports 1000BaseT 4-wire pairs and 10/100BaseT 2-wire pairs
- IEEE 802.3x 10BaseT/100BaseT/1000BaseT compatible physical layer to wire transformer

- IEEE 802.3ab Auto-Negotiation support, includes speed, duplex, and flow control
- IEEE 802.3ab PHY compliance and compatibility with Category-5 twisted pair cabling
- Implements latest DSP architecture with digital adaptive equalization, echo cancellation, and crosstalk cancellation to achieve high performance in noisy environments (high electrical/signal interference impairment)
- Supports transmit and receive IP, TCP, and UDP checksum offloading capabilities for lower CPU utilization
- Supports Transmit TCP segmentation and advanced packet filtering
- Supports system monitoring with industry standard consoles (SNMP and RMON statistic counters)
- Supports remote network management capabilities through DMI 2.0 and SNMP software (SDG 3.0, WfM 2.0, and PC2001 compliance)
- Programmable LED functions for 4 LED support (speed, link, and activity) including blinking
- Supports integrated magnetics in RJ-45 connector
- Supports four-pair, 100 ohm, Category 5 UTP (Unshielded Twisted Pair) wiring

Tables 3-21 describes the pin-outs and signals of Gigabit Ethernet port, Ethernet Port 2.

**Table 3-21. Ethernet Port 2 Pin/Signal Descriptions (J10)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | MDI0+ | Media Dependent Interface [0] |
| 2 | MDI0- | 1000BaseT – In MDI configuration, MDI0± corresponds to BI_DA±, and in MDI-X configuration, MDI0± corresponds to BI_DB±.<br>10/100BaseT – In MDI configuration, MDI0± is used for the transmit pair, and in MDI-X configuration, MDI0± is used for the receive pair. |
| 3 | MDI1+ | Media Dependent Interface [1] |
| 6 | MDI1- | 1000BaseT – In MDI configuration, MDI1± corresponds to BI_DB±, and in MDI-X configuration, MDI1± corresponds to BI_DA±.<br>10/100BaseT – In MDI configuration, MDI1± is used for the transmit pair, and in MDI-X configuration, MDI1± is used for the receive pair. |
| 4 | MDI2+ | Media Dependent Interface [2] |
| 5 | MDI2- | 1000BaseT – In MDI configuration, MDI2± corresponds to BI_DC±, and in MDI-X configuration, MDI2± corresponds to BI_DD±.<br>10/100BaseT – Unused |
| 7 | MDI3+ | Media Dependent Interface [3] |
| 8 | MDI3- | 1000BaseT – In MDI configuration, MDI3± corresponds to BI_DC±, and in MDI-X configuration, MDI3± corresponds to BI_DD±.<br>10/100BaseT – Unused |
| 9 | SPEED_1000 | Speed (1000) LED – Indicates transfer rate at 1000Mbps. |
| 10 | SPEED_100 | Speed (100) LED – Indicates transfer rate at 10Mbps or 100Mbps. |
| 11 | LINKLED | Link LED – Indicates Link established between this port and another device |
| 12 | ACTLED | Activity LED – Indicates Activity is occurring on the Ethernet link. |
| 13, 14 | SHLD | Shields – Connected to center taps of transformer and floating ground while isolated from board common ground by 1000pf capacitor. |

**Note**: The shaded area denotes power or ground.

# Audio Interface (J9)

The audio solution on the LittleBoard 800 is provided by the Realtek ALC202A audio CODEC. The chip is defined by AC97 and is revision 2.2 compliant. The audio interface signals are supplied to the 26-pin 2mm connector (J9). Refer to the following list for the *Audio CODEC* (ALC202A) features.

- Analog Mixer Dynamic Range 97dB (typ)
- D/A Dynamic Range 89dB (typ) and A/D Dynamic Range 90dB (typ)
- AC'97 Rev 2.1 compliant
- High quality Sample Rate Conversion (SRC) from 4kHz to 48kHz
- 3D Sound circuitry and PC-Beep passthrough to Line Out while reset is held active low
- True Line Level Output with volume control independent of Line Out

Table 3-22 describes the pin-outs and signals of the audio interface and it has 26 pins, 2 rows, odd/even, (1, 2) with 2mm pin spacing.

**Table 3-22. Audio Interface Pin/Signal Descriptions (J9)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | VIDEO_L | Video-Audio signal in left channel |
| 2 | VIDEO_GND | Video Audio ground |
| 3 | VIDEO_R | Video-Audio signal in right channel |
| 4 | CD_L | CD-ROM signal left channel |
| 5 | CD_GND | CD-ROM Audio ground |
| 6 | CD_R | CD-ROM signal right channel |
| 7 | LINE_IN_L | Line in signal left channel |
| 8 | LINE_IN_GND | Line in Audio ground |
| 9 | LINE_IN_R | Line in signal right channel |
| 10 | MIC1 | Microphone in signal 1 or left channel |
| 11 | MIC_GND | Microphone Audio ground |
| 12 | MIC2 | Microphone in signal 2 or right channel |
| 13 | MIC_REF | Microphone reference signal |
| 14 | NC/KEY | Not Connected - Key |
| 15 | PHONE_IN | Phone signal in |
| 16 | PHONE_GND | Phone Audio ground |
| 17 | MONO_OUT | Monaural signal out |
| 18 | MONO_GND | Monaural Audio ground |
| 19 | +AOUT_L | - Audio out signal left channel |
| 20 | -AOUT_L | + Audio out Audio ground |
| 21 | +AOUT_R | - Audio out signal right channel |
| 22 | -AOUT_R | + Audio out Audio ground |
| 23 | GND | Audio Ground (tied to all audio grounds) |
| 24 | HP_L | Headphone signal left channel |
| 25 | HP_R | Headphone signal right channel |
| 26 | NC | Not Connected |

**Note:** The shaded area denotes power or ground.

# Video Interfaces (J3, J26)

The 855GME chip provides the graphics control and video signals to the traditional glass CRT monitors and LCD flat panel displays. The chip features are listed below:

*CRT* features:

- Supports a max resolution of 1600 x 1200 with video frame buffer set at 8MB
- Supports a maximum allowable video frame buffer size of 64MB shared memory
- AGP 4X graphics performance (always enabled)

*Flat Panel* features:

- Supports (+3.3V or +5V, and +12V) output to LCD flat panels through a LVDS interface
- Supports panel sizes from VGA (320x480) up to SXGA+ and UXGA+ (1400x1050).
- Supports VGA and SVGA panels with 9-, 12-, or 18-bit (1 Pixel/Clock)
- Supports 1 or 2 channel LVDS outputs

## CRT Interface

Table 3-23 describes the pin-outs and signals of the CRT interface and it has 10 pins, 2 rows, odd/even, (1, 2) with 0.100" pin spacing.

**Table 3-23. CRT Interface Pin/Signal Descriptions (J3)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | RED | Red – This is the Red analog output signal to the CRT. |
| 2 | GND | Ground |
| 3 | GREEN | Green – This is the Green analog output signal to the CRT. |
| 4 | GND | Ground |
| 5 | BLUE | Blue – This is the Blue analog output signal to the CRT. |
| 6 | GND | Ground |
| 7 | HSYNC | Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT. |
| 8 | GND | Ground |
| 9 | VSYNC | Vertical Sync – This signal is used for the digital vertical sync output to the CRT. |
| 10 | PWR | Power – Provided through fuse (F1) to +5 volts +/- 5%. F1 is next to J3 connector on board. |

**Note:** The shaded area denotes power or ground.

## LVDS Interface (J26)

Table 3-24 describes the pin-outs and signals of the LVDS interface and it has 30 pins, 2 rows, odd/even, (1, 2) with 2mm pin spacing header.

**Table 3-24. LVDS Interface Pin/Signal Descriptions (J26)**

| Pin # | Signal | Description | Line | Channel |
|---|---|---|---|---|
| 1 | +12V | +12 volt input | NA | NA |
| 2 | +VCC (+3.3V/+5V) | JP1 determines voltage on pin | | |
| 3 | GND | Ground | | |
| 4 | GND | Ground | | |
| 5 | CLK_LVDS_IYBP | Clock Positive Output | Clock | Channel 2 |
| 6 | CLK_LVDS_IYBM | Clock Negative Output | | |
| 7 | LVDS_IYBP3 | Data Positive Output | 3 | |
| 8 | LVDS_IYBM3 | Data Negative Output | | |
| 9 | LVDS_IYBP2 | Data Positive Output | 2 | |
| 10 | LVDS_IYBM2 | Data Negative Output | | |
| 11 | LVDS_IYBP1 | Data Positive Output | 1 | |
| 12 | LVDS_IYBM1 | Data Negative Output | | |
| 13 | LVDS_IYBP0 | Data Positive Output | 0 | |
| 14 | LVDS_IYBM0 | Data Negative Output | | |
| 15 | LVDS_PANELBKLTCTL | Control Panel Backlight | NA | NA |
| 16 | LVDS_PANELVDDEN | Enable Panel Power | NA | NA |
| 17 | CLK_LVDS_IYAP | Clock Positive Output | Clock | Channel 1 |
| 18 | CLK_LVDS_IYAM | Clock Negative Output | | |
| 19 | LVDS_IYAP3 | Data Positive Output | 3 | |
| 20 | LVDS_IYAM3 | Data Negative Output | | |
| 21 | LVDS_IYAP2 | Data Positive Output | 2 | |
| 22 | LVDS_IYAM2 | Data Negative Output | | |
| 23 | LVDS_IYAP1 | Data Positive Output | 1 | |
| 24 | LVDS_IYAM1 | Data Negative Output | | |
| 25 | LVDS_IYAP0 | Data Positive Output | 0 | |
| 26 | LVDS_IYAM0 | Data Negative Output | | |
| 27 | DDCPCLK | Display Data Channel Clock | NA | NA |
| 28 | DDCPDATA | Display Data Channel Data | NA | NA |
| 29 | LVDS_PANELBKLTEN | Enable Backlight Inverter | NA | NA |
| 30 | NC | Not Connected | NA | NA |

**Note:** The shaded area denotes power or ground.

**NOTE** Pins 5-14 constitute 2nd channel interface of two channels. Pins 15-26 constitute 1st channel interface of two channels, or a single channel interface.

# Miscellaneous

## Real Time Clock (RTC)

The LittleBoard 800 contains a Real Time Clock (RTC). The BIOS (CMOS) RAM is backed up with a Lithium Battery. If the battery is not present, the BIOS has a battery-free boot option to complete the boot process.

## Temperature Monitoring

The ADM1023 performs CPU temperature monitoring. This device has an input connection from the thermal diode in the Intel Celeron M or Pentium M CPU. The SMBus is connected to a dedicated thermal alert pin in the ADM1023 and the other devices on the SMBus.

| NOTE | The LittleBoard 800 requires a heatsink for both Celeron M CPUs and a heatsink for the Pentium M CPU below 70° C. |
|---|---|

## Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event the BIOS settings you've selected prevent you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in the EEPROM from being loaded, forcing the use of the default settings. Connect the DTR pin to the RI pin on serial port 1 (COM 1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and go into BIOS Setup. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

To convert the Serial A interface to an Oops! jumper, short together the DTR (7) and RI (8) pins on Serial A (J11) header for Serial Port 1. As an alternate, short the equivalent pins, 4 and 9, on the Serial Port 1 DB9 connector as shown in Figure 3-2.

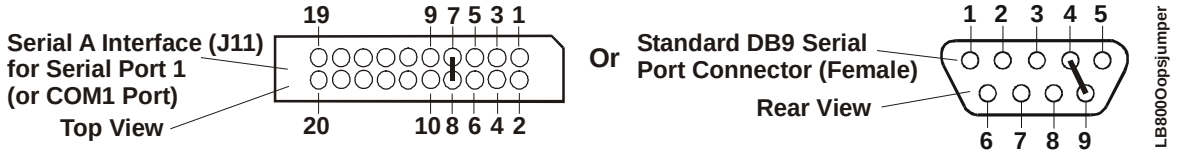



**Figure 3-2. Oops! Jumper Connection**

## Serial Console

The LittleBoard 800 supports the serial console (or console redirection) feature. This I/O function is provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

### Serial Console Setup

The serial console feature is implemented by connecting a standard null modem cable or modified serial cable (or "Hot Cable") between one of the serial ports, such as Serial 1 (J11A) and the serial terminal, or a PC with communications software. The BIOS Setup Utility controls the serial console settings on the LittleBoard 800. Refer to Chapter 4, BIOS Setup for the settings of the serial console option, the serial terminal, or PC with communications software and the connection procedure.

### Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, specific pins must be shorted together at the Serial port connector or at the DB9 connector. For example, short the RTS (7) and RI (9) on the respective DB9 port connector as shown in Figure 3-3.

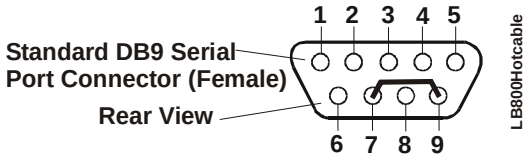



**Figure 3-3. Hot Cable Jumper**

## Watchdog Timer

The watchdog timer (WDT) restarts the system if a mishap occurs, ensuring proper start-up after the interruption. Possible problems include failure to boot properly, the application software's loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (watchdog timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT in the Advanced BIOS Features of BIOS Setup. Set the WDT for a time-out interval in seconds, between 2 and 255, in one-second increments in the Advanced BIOS Features screen. Ensure you allow enough time for the boot process to complete and for the OS to boot. The OS or application must tickle (turnoff) the WDT as soon as it comes up. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some Ampro Board Support Packages provide an API interface to the WDT. The application must tickle (turnoff) the WDT in the time set when the WDT is initialized or the system will be reset. You can use a BIOS call to tickle the WDT or access the hardware directly.

The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

- Watchdog Code examples – Ampro has provided source code examples on the LittleBoard 800 Doc & SW CD-ROM illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file in the Miscellaneous Source Code Examples subdirectory, under the LittleBoard 800 Software menu on the LittleBoard 800 Doc & SW CD-ROM.

# Power Interfaces

## Power Supply Input (J19)

The LittleBoard 800 uses five separate voltages on the board, but only one of the voltages is provided externally (+5 volts) through the external connector, which uses a 7-pin vertical header with 0.156" (3.96mm) spacing. Holes for a right angle mounting header are also available at J19. All the onboard voltages are derived from the externally supplied +5 volts DC +/- 5%. The onboard voltages include the CPU core voltages as well as the other voltages used on the board.

Table 3-25 lists the pin-outs and signals for Power supply input and it has 7 pins, single row, with 0.156" pin spacing..

**Table 3-25. Power Supply Input Pin/Signal Descriptions (J19)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | +5V | +5.0 Volts – This +5.0 volts DC +/- 5% is the only voltage required for operation. |
| 2 | GND | Ground |
| 3 | GND | Ground |
| 4 | +12V | +12 Volts – This +12 volts is for the PC/104, PC/104-Plus, and LVDS power only |
| 5 | +3.3V | +3.3 Volts – This +3.3 volts is for PC/104-Plus Bus power only (optional) |
| 6 | GND | Ground |
| 7 | +5V | +5.0 Volts – This +5.0 volts DC +/- 5% is the only voltage required for operation. |

**Notes:** The shaded area denotes power or ground. The +12V and +3.3V on the Power Supply input connector (J19) are used for the PCI, ISA bus, and LVDS power are supplied externally and not generated on the LittleBoard 800. The -5V and –12V used for the PC/104 bus are supplied through the PC/104 bus or from an external power supply through the Utility 1 connector (J16).

## Optional CPU Fan (J21)

Table 3-26 lists the pin-outs and signals of the optional CPU Fan and it has 3 pins, single row, with 0.100" pin spacing.

**Table 3-26. Optional CPU Fan (J21)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | Fan_Tach | Fan Tachometer – This signal indicates Fan speed |
| 2 | VCC | +5.0 volts DC +/- 5% |
| 3 | GND | Ground |

**Note:** The shaded area denotes power or ground.

# Chapter 4 BIOS Setup

## Introduction

This chapter describes the BIOS Setup Utility menus and the various screens used for configuring the LittleBoard 800. Some features in the Operating System or application software may require configuration in the BIOS Setup screens.

This section assumes the user is familiar with BIOS Setup and does not attempt to describe the inner workings of BIOS functions. Refer to the appropriate PC reference manuals for information about the onboard ROM-BIOS software interface. If Ampro has added to or modified the standard functions, these functions will be described.

The options provided for the LittleBoard 800 are controlled by BIOS Setup Utility. BIOS Setup is used to configure the board, modify the fields in the Setup screens, and save the results in the onboard configuration memory. Configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and the flash memory.

The Setup information is retrieved from configuration memory when the board is powered up or when it is rebooted. Changes made to the Setup parameters, with the exception of the time and date settings, do not take effect until the board is rebooted.

Setup is located in the ROM BIOS and can be accessed, when prompted using the <Del> key, while the board is in the Power-On Self Test (POST) state, just before completing the boot process. The screen displays a message indicating when you can press <Del>.

The LittleBoard 800 BIOS Setup is used to configure items in the BIOS using the following menus:

- BIOS and Hardware Settings
- Reload Initial Settings
- Load Factory Default Settings
- Exit, Saving Changes
- Exit, Discarding Changes

Table 4-1 summarizes the list of BIOS menus and some of the features available for LittleBoard 800. The BIOS Setup menu offers the menu choices listed above and the related topics and screens are described on the following pages.

### Accessing BIOS Setup (VGA Display)

To access BIOS Setup using a VGA display for the LittleBoard 800:

1. Turn on the VGA monitor and the power supply to the LittleBoard 800.
2. Start Setup by pressing the [Del] key, when the following message appears on the boot screen.

```
Hit <Del> if you want to run SETUP
```

| **NOTE** | If the setting for *Memory Test* is set to Fast, you may not see this prompt appear on screen if the monitor is too slow to display it on start up. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup. |
|---|---|

3. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.
4. Follow the instructions at the bottom of each screen to navigate through the selections and modify any settings.

## Accessing BIOS Setup (Serial Console)

Entering the BIOS Setup, in serial console mode, is very similar to the steps you use to enter BIOS Setup with a VGA display, except the actual keys you use.

1. Set the serial terminal, or the PC with communications software to the following settings:
   - 115k baud
   - 8 bits
   - One stop bit
   - No parity
   - No hardware handshake
2. Connect the serial console, or the PC with serial terminal emulation, to Serial Port 1 or Serial Port 2 of the LittleBoard 800.
   - If the BIOS option, *Serial Console* is set to [Enable], use a standard null-modem serial cable.
   - If the BIOS option, *Serial Console* is set to [Hot Cable], use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.
3. Turn on the serial console or the PC with serial terminal emulation and the power supply to the LittleBoard 800.
4. Start Setup by pressing the Ctl–c keys, when the following message appears on the boot screen.

```
Hit ^C if you want to run SETUP
```

5. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.

| **NOTE** | The serial console port is not hardware protected, and is not listed in the COM table within BIOS Setup. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions. |
|---|---|

**Table 4-1. BIOS Setup Menus**

| BIOS Setup Menu | Item/Topic |
|---|---|
| BIOS and Hardware Settings | Date and Time<br>Drive Configuration<br>Boot Order<br>Drive and Boot Options<br>Keyboard & Mouse settings<br>User Interface options<br>Memory settings<br>Power Management<br>Advanced Features<br>On-Board Features (Serial, Parallel, USB, Video, Audio, etc.)<br>PCI and Plug and Play Options |
| Reload Initial Settings | Resets the BIOS (CMOS) to the most recent settings |
| Load Factory Default Settings | Resets BIOS (CMOS) to factory settings |
| Exit, Saving Changes | Writes all changes to BIOS (CMOS) and exits |
| Exit, Discarding Changes | Closes BIOS without saving changes except time and date |

# BIOS Menus

## BIOS Setup Opening Screen

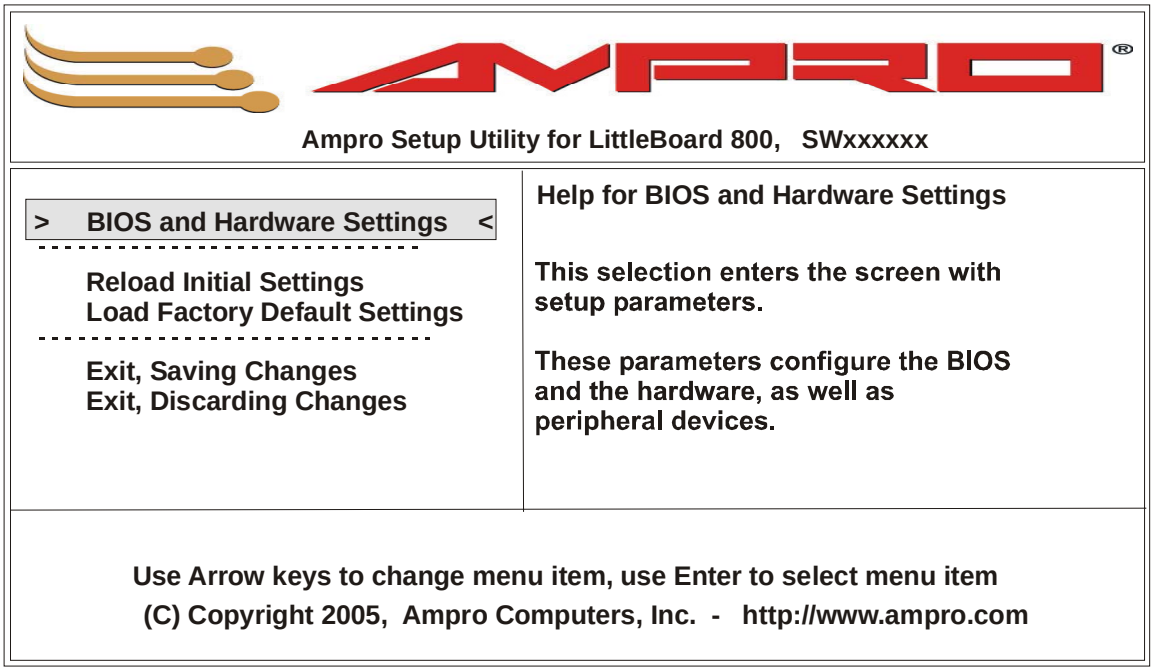



**Figure 4-1. Opening BIOS Screen**

| **NOTE** | For the most current BIOS Information, refer to the Hardware Release Notes provided as hard copy in the shipping container. |
|---|---|

| **NOTE** | The default values or the typical settings are shown highlighted (**bold text**) in the list of options on the following pages.<br><br>Refer to the bottom of the BIOS screens for navigation instructions and when making selections. |
|---|---|

## BIOS Configuration Screen

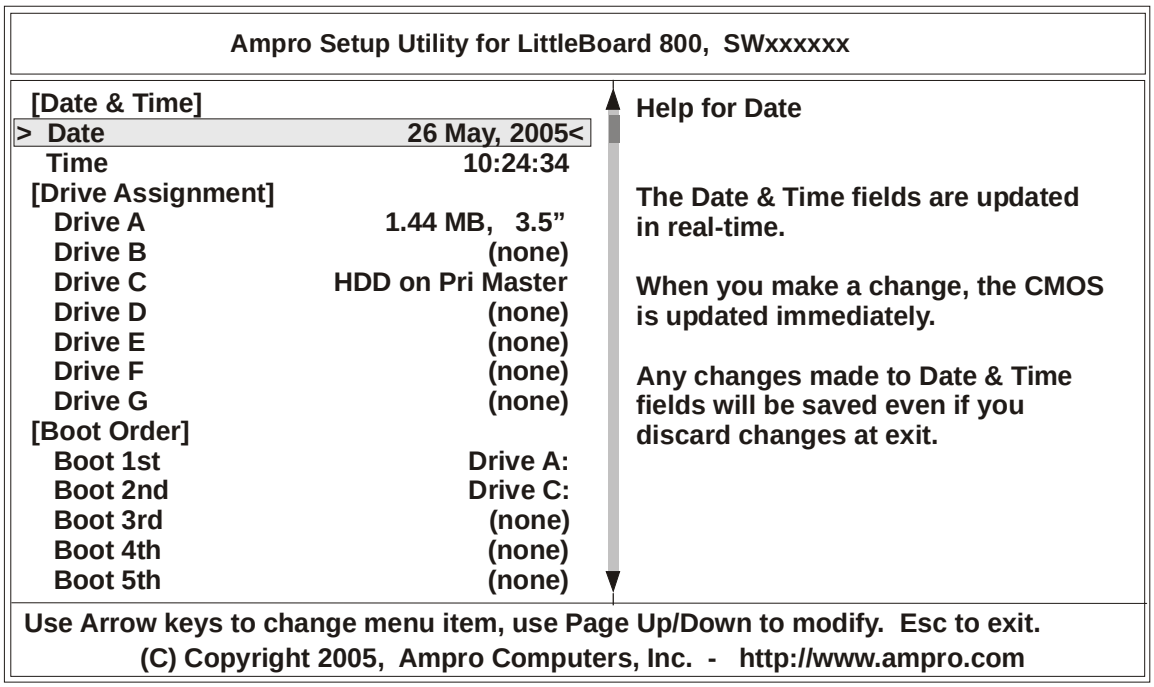



**Figure 4-2. Modifying Setup Parameters Screen**

- **Date & Time**
  - DATE (dd:mmm:yyyy) – This requires the alpha-numeric entry of the calendar month, day of the month, and all 4 digits of the year, including the century plus year (*26 May 2005*).
  - Time (hh:mm:ss) – This requires 24 hour Clock setting in hours, minutes, and seconds

## Drive Configurations and Boot Options

- **Drive Assignment**
  - Drive A – [none], [360kB, 5.25"], [1.2MB, 5.25"], [720kB, 3.5"], [**1.44MB, 3.5"**], [2.88MB, 3.5"], or [USB Floppy]

| NOTE | If USB Boot Support is [Disabled], the USB Floppy selections are invalid and Drive B must be set to [none]. See Table 4-2 Floppy Drive Setting.<br><br>If you want to boot the system using a USB device, you must select the USB device under *Drive Assignments* and enable **USB Boot Support** under *Advanced features* later in the BIOS settings. See USB Notes on next page. |
|---|---|

  - Drive B – [**none**], [360kB, 5.25"], [1.2MB, 5.25"], [720kB, 3.5"], [1.44MB, 3.5"], [2.88MB, 3.5"], or [USB Floppy]

| NOTE | If an on board CompactFlash device is used in the system, it is always configured as [HDD/CF Sec Master or Slave] on Drive C or D. |
|---|---|

  - Drive C – [none], [**HDD on Pri Master**], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]

| NOTE | The BIOS does not support a break in the drive order, that is, Drive C can not be listed as [none] when the boot device is Drive D. |
|---|---|

- Drive D – [**none**], [HDD on Pri Master], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]

**Table 4-2. Floppy Drive BIOS Settings**

| # of Floppy Drive(s) | BIOS Settings |
|---|---|
| None | Set Drives A and B to [None] |
| (1) Non-USB Floppy* | • Configure Drive A to floppy drive type (For example, [1.44MB, 3.5"] )<br>• Set Drive B to [None] |
| (1) USB Floppy | • Set USB Boot Support to [Enable]<br>• Set Drive A to [USB Floppy]<br>• Set Drive B to [None] |
| (2) Floppy drives<br>(1 USB Floppy and 1 non-USB Floppy drive*) | • Set USB Boot Support to [Enable]<br>• Configure one drive (Drive A or B) to floppy drive type (For example, [1.44MB, 3.5"] )<br>• Set one drive (Drive B or A) to [USB Floppy] |

**Table Note**: *A standard 34-pin floppy cable has a twist in the cable wiring between the Floppy A and B connectors, where Floppy B has the straight through cable (non-twist) and is the middle connector. Due to the LittleBoard 800's internal configuration and the cable supplied, there is only one physical connector available (Floppy A connector, because the Floppy B connector is not available).

| NOTE | Ampro does not recommend connecting a USB boot device to the LittleBoard 800 through an external hub. Instead, connect the USB boot device directly to the LittleBoard 800.<br><br>Any USB (block) device that emulates a hard disk drive can be used when [USB HDD] is set as the drive option. This includes various storage media types, such as USB hard disk drives, USB connected CompactFlash™ cards, Secure Digital Memory Card™, and Flash or Thumb drives. Refer also to ***Boot Order*** settings**, USB Boot Support** under ***Advanced features***, and **USB** (device enable) under ***On-Board Controllers*** for USB Drive boot order, USB Boot Enable, and the number of USB ports enabled, respectively. |
|---|---|

- Drive E – [**none**], [HDD on Pri Master], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]
- Drive F – [**none**], [HDD on Pri Master], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]
- Drive G – [**none**], [HDD on Pri Master], [CDROM on Pri Master], [HDD on Pri Slave], [CDROM on Pri Slave], [HDD/CF on Sec Master], [CDROM on Sec Master], [HDD/CF on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]

- **Boot Order**
  - Boot 1st – [none], [**Drive A**], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
  - Boot 2nd – [none], [Drive A], [Drive B], [**Drive C**], [Drive D], [CDROM], [Alarm], or [Reboot]

| **NOTE** | The [Alarm] option sounds beeps on the PC speaker and can be listed, like [Reboot], as the last boot device to indicate no bootable device was found.<br><br>Any of the drives can be listed as a boot drive. |
|---|---|

  - Boot 3rd – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
  - Boot 4th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
  - Boot 5th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
  - Boot 6th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]

| **NOTE** | The default Boot order is A, then C, and the BIOS will start its search for a bootable device in drive A, then C. If no bootable device is found, the screen will display "No Bootable Device Available" and the boot process will stop, allowing you to select:<br><br>R – for Reboot, and Del – for BIOS setup after rebooting<br><br>If you do not choose R, the boot process stops, until you intervene, unless you have set [Reboot] as an option. |
|---|---|

- **Drive and Boot Options**
  - Floppy Seek – [**Disabled**] or [Enabled]
  - Hard disk Seek – [**Disabled**] or [Enabled]
  - Floppy Swap – [**Disabled**] or [Enabled]
  - Boot Method – [**Boot Sector**] or [Windows CE]

    Boot Sector is the traditional method for booting the system. If [Windows CE] is selected, the BIOS attempts to load the NK.BIN file from the root directory of each boot device.
  - Primary IDE Cable – [**Auto**], [40 Wire], or [80 Wire]

    Setting these fields to [Auto], causes the BIOS to query the attached IDE device to determine the type of IDE cable used. If the BIOS detects [40 wire], or you select it, the BIOS will not use UDMA-66 or faster mode when sending signals to/from the IDE device.
  - Secondary IDE Cable – [**Auto**], [40 Wire], or [80 Wire]
  - Seondary Master ATA mode – [**LBA**], [Physical], or [Phoenix]

    This default option (LBA - Logical Block Address) could be used on any IDE device, including CompactFlash cards. However, this option specifically allows you to select between the existing formats used to format your CompactFlash card as the Secondary master device.
  - Secondary Slave ATA mode – [**LBA**], [Physical], or [Phoenix]

    This default option (LBA - Logical Block Address) could be used on any IDE device, including CompactFlash cards. However, this option specifically allows you to select between the existing formats used to format your CompactFlash card as the Secondary slave device.

| NOTE | This feature allows you to use any one of the three common formats available for CompactFlash cards without having to re-format the CompactFlash card before you can use it on the LittleBoard 800. The LBA (Logical Block Address) is set as the default format because it can handle larger drives and is the newest format available, but may not be the one used to format your CompactFlash card. The other common formats that may be encountered are the Physical (below 512MB) or Phoenix (physical above 512MB) formats. |
|---|---|

## User Interface Options

- **Keyboard and Mouse** (Configuration)
  - Numlock – [**Disabled**] or [Enabled]
  - Typematic – [Disabled] or [**Enabled**]

    These fields are used for the keyboard.

    - Delay – [**250ms**], [500ms], [750ms], or [1000ms]

      This field is used for the keyboard and determines how many milliseconds the keyboard controller waits before stating to repeat a key, if the key is held down on the keyboard.

    - Rate – [**30cps**], [24cps], [20cps], [15cps], [12cps], [10cps], [8cps], or [6cps]

      This is a keyboard field and determines the rate, in characters per second, the keyboard controller will repeat a key, if the key is held down on the keyboard.

  - Initialize PS/2 Mouse – [Disabled] or [**Enabled**]
    - If this field is set to [Enabled], the BIOS will initialize the PS/2 mouse.
    - If the PS/2 mouse is [Disabled], the BIOS will not initialize the PS/2 mouse, which may not be recognized by the Operating System.
- **User Interface**
  - Show “Hit <Del>…” – [Disabled] or [**Enabled**]

    This field, if Enabled, will place “Hit Del” on screen during the boot process, to indicate when you may press “Del” to enter the BIOS Setup menus.
  - F1 Error Wait – [**Disabled**] or [Enabled]
    - If this field is [Enabled], the BIOS will display an Error message indicating when an error has occurred during POST (power on self test) and wait for you to respond by hitting the F1 key.
    - If [Disabled], and an error occurs during POST, the BIOS will attempt to continue the boot process.
  - Config Box – [Disabled] or [**Enabled**]

    This field, if Enabled, displays the Configuration Summary Box, which list all of the configuration information for the system, at the completion of POST, but before the Operating System is loaded.

- Splash Screen – [**Disabled**] or [Enabled]

  The Splash Screen is a graphical image displayed as the default (Ampro Splash Screen) or a user customized image on screen. Refer to the Splash Screen Customization topic later in this chapter for instructions on how to customize the splash screen.

  * If Splash Screen is [Enabled] it stays on screen, until the booted Operating System changes it, if the Config Box option is Disabled.
  * If Config Box option is [Enabled], the Splash Screen stays on screen until the Config Box is displayed.

## Memory Control Options

- **Memory**
  - Memory Test – [**Fast**], [Standard], or [Exhaustive]
    * If this field is set to [Fast], only basic memory tests are performed during POST to shorten POST time.
    * If this field is set to [Standard], more than basic tests are performed, but POST time is increased.
    * If this field is set to [Exhaustive], more rigorous tests are performed on memory, but this takes a significant amount of time for POST to complete.
  - Memory Hole – [**Disabled**], or [1MB]

    This field specifies the size of an optional memory hole, below 16MB. Access to the memory addresses inside the memory hole region are forwarded to the PC/104 bus, where memory mapped PC/104 devices have access.
  - Shadow D000-D3FF – [**Disabled**] or [Enabled]

    These Shadow fields specify if BIOS option ROMs in the indicated segments should be shadowed to RAM. Shadowing option ROMs can potentially speed up the operation of the system. The indicated segments are only for option ROMs present on add-on PC/104 and PC/104-Plus cards.
  - Shadow D400-D7FF – [**Disabled**] or [Enabled]
  - Shadow D800-DBFF – [**Disabled**] or [Enabled]
  - Shadow DC00-DFFF – [**Disabled**] or [Enabled]

## Power Management and Advanced User Options

- **Power Management**
  - ACPI – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the Advanced Configuration and Power Interface API is turned on.
  - APM – [**Disabled**] or [Enabled]

    If this field is set to [Enabled], the Advanced Power Management API is turned on.
- **Advanced features**
  - Post Memory Manager – [**Disabled**] or [Enabled]

    If this field is set to [Enabled], the Post Memory Manger API is turned on. The Post Memory Manger can be used by BIOS option ROMs to allocate memory in a well defined way.
  - CPU Serial Number – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the internal serial number in the Intel CPU is accessible by the Operating System and/or Applications that can make use of this information.

- Watchdog Timeout (sec) – [select whole number between 1 and 255 seconds, in 1-second increments] or [**Disabled**]

  If this field is enabled by selecting a time interval (1 to 255 seconds), will direct the watchdog timer to reset the system if it fails to boot the OS properly. Refer to the watchdog timer section in Chapter 3 for more information.

- Serial Console – [**Hot Cable**] or [Enabled]

  * The Hot Cable option only allows console redirection when a Hot Cable is actually connected to COM 1 or 2. Use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.

  * The [Enabled] option instructs the BIOS to operate in the console redirection mode at all times with the serial port selected in the Serial Console > Port field listed below. Use a standard null-modem serial cable.

  * However, connecting a Hot Cable to the other port (port not selected) overrides the setting of this field [Enabled] and the Serial Console > Port field.

  - Port – [**3F8h**], [2F8h], [3E8h], or [2E8h]

    This field selects the COM (Serial) port address used for console redirection when [Enabled] has been selected in Serial Console. Use a standard null-modem serial cable.

    However, connecting a Hot Cable to the other port (port not selected) overrides this field setting and activates the connected port. Connecting a Hot Cable to one of the serial ports only allows console redirection when a Hot Cable is actually connected to Serial 1 or 2. Use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.

- SMM Support – [Disabled] or [**Enabled**]

  This field was created to disable all SMI (System Management Interrupt) activity. This feature should only be used in special cases and then only when SMI activity would degrade realtime response.

  * If this field is set to [Enabled], the default setting, all SMI functions are enabled allowing the Watchdog Timer, ACPI functions and the USB boot features to operate normally.

  * If this field is set to [Disabled], all SMI activity is halted and the Watchdog Timer, ACPI functions, and USB boot features will not operate.

| **CAUTION** | Do not Disable the SMM Support feature, unless you are thoroughly convinced you need it. This feature is only used for special cases when all SMI activity needs to be halted, which will disable many features of your system, including the Watchdog Timer, ACPI functions, and USB boot features. |
|---|---|

- USB Boot Support – [**Disabled**] or [Enabled]

  This field allows you to select any USB device as a boot device. Refer also *to **Drive Assignment*** settings, ***Boot Order*** settings, and **USB** (device enable) under ***On-Board Controllers*** for the USB Drive settings and the number of USB ports enabled, respectively.

  * If this field is set to [Disabled], none of the USB devices connected to the LittleBoard 800 can be used as a boot device.

  * If this field is set to [Enabled], any of the bootable USB devices connected to the LittleBoard 800 can be used as a boot device.

| **NOTE** | Ampro does not recommend connecting a USB boot device to the LittleBoard 800 through an external hub. Instead, connect the USB boot device directly to the LittleBoard 800. |
|---|---|

- LAN Boot – [**Disabled**] or [LAN1]

  This field allows you to boot the system over one of the Ethernet connections (LAN1, J23). Refer to Appendix B, *LAN Boot Feature* and the BIOS settings for the integrated PXE Boot Agent for more information.

  * If this field is set to [LAN 1], the LittleBoard 800 will boot from Ethernet 1 (J23). If you enable LAN Boot [LAN 1], you will need to save changes and reboot the system, before going to the PXE BIOS settings. Refer to Appendix B, *LAN Boot Feature* for more information.

- **On-Board Serial Ports**

| **NOTE** | Serial Ports 1 and 2 can not share the same IRQs, and the IRQs used for Serial Ports 1 and 2 can not be used for Serial Ports 3 and 4 and vice versa. |
|---|---|

- Serial 1 – [Disabled], [**3F8h**], [2F8h], [3E8h], [2E8h], [260h], [3E0h], [2E0h], [200h], [220h], [228h], [238h], or [338h]

  This field specifies the base address used for Serial Port 1.

  - IRQ – [none], [1], [3], [**4**], [5], [6], [7], [9], [10], [11], [12], [14], or [15]

    This field specifies the IRQ used for Serial Port 1. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

  - Mode – [**RS-232**] or [RS-485]

    This field specifies the signal mode, RS232, or RS485, used for Serial Port 1. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

- Serial 2 – [Disabled], [3F8h], [**2F8h**], [3E8h], [2E8h], [260h], [3E0h], [2E0h], [200h], [220h], [228h], [238h], or [338h]

  This field specifies the base address used for Serial Port 2.

  - IRQ – [none], [1], [**3**], [4], [5], [6], [7], [9], [10], [11], [12], [14], or [15]

    This field specifies the IRQ used for Serial Port 2. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

  - Mode – [**RS-232**] or [RS-485]

    This field specifies the signal mode, RS232, or RS485, used for Serial Port 2. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

- Serial 3 – [Disabled], [3F8h], [2F8h], [**3E8h**], [2E8h], [260h], [3E0h], [2E0h], [200h], [220h], [228h], [238h], or [338h]

  This field specifies the base address used for Serial Port 3.

  - IRQ – [none, [1], [3], [4], [5], [6], [7], [9], [10], [**11**], [12], [14], or [15]

    This field specifies the IRQ used for Serial Port 3. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

  - Mode – [**RS-232**] or [RS-485]

    This field specifies the signal mode, RS232, or RS485, used for Serial Port 3. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

- Serial 4 – [Disabled], [3F8h], [2F8h], [3E8h], [**2E8h**], [260h], [3E0h], [2E0h], [200h], [220h], [228h], [238h], or [338h]

  This field specifies the base address used for Serial Port 4.

  - IRQ – [none], [1], [3], [4], [5], [6], [7], [9], [**10**], [11], [12], [14], or [15]

    This field specifies the IRQ used for Serial Port 4. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

  - Mode – [**RS-232**] or [RS-485]

    This field specifies the signal mode, RS232, or RS485, used for Serial Port 4. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

- **On-Board LPT Port**

  - LPT 1 – [Disabled], [**378h**], [278h], or [3BCh]

    This field specifies the base address used for the Parallel Port (LPT 1).

    - IRQ – [none], [1], [3], [4], [5], [6], [**7**], [9], [10], [11], [12], [14], or [15]

      This field specifies the IRQ used for the Parallel Port (LPT 1). If this field is set to [none], then no IRQ is assigned, making it available for other devices.

    - DMA – [**3**], [2], [1], or [0]

      This field specifies the DMA channel used for the Parallel Port (LPT 1). If the LPT 1 field is set to [Disabled], then no DMA channel is assigned, making it available for other devices.

    - Mode – [**Standard**], [SPP (bi-dir)], [EPP 1.9 + SPP], [EPP 1.7 + ECP], [EPP 1.9 + ECP], or [ECP]

      This field specifies the Mode used for the Parallel Port (LPT1).

- **On-Board Controllers**

  - Floppy – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], then the on-board Floppy controller is used.

  - Primary IDE – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], then the on-board Primary IDE controller is used.

  - Secondary IDE – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], then the on-board Secondary IDE controller is used.

  - PS/2 Mouse – [Disabled] or [**Enabled**]

    * If this field is set to [Enabled], then the on-board PS/2 Mouse controller is used and assigned an IRQ by the BIOS, typically IRQ 12.

    * If this field is set to [Disabled], then the on-board PS/2 Mouse controller is not used and IRQ 12 is available for other devices.

  - USB – [Disabled], [2 Ports] or [**4 Ports**]

    * If this field is set to [4 Ports], both on-board USB controllers are used, each one supporting two USB ports.

    * If this field is set to [2 Ports], the first on-board USB controller is used, supporting two USB ports, and the second on-board USB controller is disabled.

  - Audio – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the on-board Audio controller is used.

## Video and Flat Panel Options

- **On-Board Video**
  - Framebuffer Size – [Disabled], [1MB], [4MB], [8MB], [**16MB**], or [32MB]

    This field specifies the amount of system memory used for the on-board Video Framebuffer. The amount of memory used for the Framebuffer of the on-board Video controller is subtracted from the available system memory.
  - AGP Aperture Size – [64MB], [**128MB**], or [256MB]

    This field specifies the size of memory used for the AGP Aperture. The AGP Aperture Size indicates the amount of system memory that can be used for the 3D engine. System memory is still available for system use, unless an application is actually using the AGP Aperture memory.
  - Off-Board Primary – [**Disabled**] or [Enabled]

    This field specifies which video controller is initialized as the primary video controller. This includes the on-board (LittleBoard 800) video controller, or a second video controller (video card on PC/104-Plus bus), initialized as the primary video controller.
    - If this field is set to the default setting, [Disabled], the on-board video controller will always be initialized by the BIOS as the primary video controller. If a second video controller is present, the OS can initialize this video (card) controller as the secondary video controller, allowing you to use two separate video controllers and displays.
    - If this field is set to, [Enabled], the on-board video controller will not be initialized by the BIOS if another controller is present, allowing the OS to initialize an off board video controller as the primary controller. The on-board (LittleBoard 800) video controller will not be recognized by the OS, and therefore, will never be initialized as the secondary controller.
  - Display – [**CRT**], [LCD], [CRT + LCD]

    This field specifies the display type used.
    - If [LCD] or [CRT+LCD] is selected, the panel type selection indicates the configuration of the LCD panel attached. See the Panel Type field and Table 4-3.
    - If the [CRT+LCD] is selected, the same video information is shown on both displays simultaneously.
  - Panel Type – [**none**]

    Refer to Table 4-3 for the list of supported resolutions and flat panel types and the Software Release Notes for the signal pin assignments. Some LCD panels may require video BIOS modifications. If you would like help in setting up your LCD panel, contact Virtual Technician on the web site for assistance with the LCD panel adaptation.

**Table 4-3. LCD Panel Type List**

| # | LCD Resolution | LCD Type |
|---|---|---|
| 1 | **None** | |
| 2 | 640 x 480 x 18 (bit) | LVDS |
| 3 | 800 x 600 x 18 (bit) | LVDS |
| 4 | 1024 x 768 x 24 (bit) | LVDS |
| 5 | 1280 x 1024 x 18 (bit) | LVDS |
| 6 | 1400 x 1050 x 18 (bit) | LVDS |
| 7 | 1024 x 768 x 18 (bit) | LVDS |
| 8 | 1600 x 1200 x 18 (bit) | LVDS |

| # | LCD Resolution | LCD Type |
|---|---|---|
| 9 | | |
| 10 | | |
| 11 | | |
| 12 | | |
| 13 | | |
| 14 | | |
| 15 | | |
| 16 | | |

## PCI, Plug n' Play, and Interrupt/DMA Assignments

- **PCI**
  - INTA IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
  - INTB IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]
  - INTC IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
  - INTD IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]
  - INTE IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
  - INTF IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]
  - INTH IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
- **Plug and Play**
  - PnP BIOS – [Disabled] or [**Enabled**]
    - If this field is set to [Enabled], the BIOS uses Plug and Play adapter initialization and assigns the resources, such as I/O addresses, IRQs, and DMA channels to Plug and Play compatible devices. The resources assigned by the BIOS are based on the settings of the IRQ and DMA channel assignments listed in the following fields.
    - If this field is set to [Disabled], the IRQs and DMA channels listed below can not be assigned to Plug and Play devices.
  - PnP OS – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the BIOS makes the Plug and Play API available for Plug and Play Operating Systems. This allows the Plug and Play OS to get the Plug and Play information by calling the Plug and Play API.
  - Assign IRQ 1 – [**Disabled**] or [Enabled]
    - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
    - If another device in the system is using this IRQ, then this field should be set to [Disabled].
  - Assign IRQ 3 – [Disabled] or [**Enabled**] (Typically COM2)
    - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
    - If another device in the system is using this IRQ, then this field should be set to [Disabled].
  - Assign IRQ 4 – [Disabled] or [**Enabled**] (Typically COM1)
    - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
    - If another device in the system is using this IRQ, then this field should be set to [Disabled].
  - Assign IRQ 5 – [Disabled] or [**Enabled**]
    - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
    - If another device in the system is using this IRQ, then this field should be set to [Disabled].

- Assign IRQ 6 – [**Disabled**] or [Enabled] (Typically Floppy Disk)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 7 – [Disabled] or [**Enabled**] (Typically LPT1)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 9 – [Disabled] or [**Enabled**] (Typically unused)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 10 – [Disabled] or [**Enabled**] (Typically unused)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 11 – [Disabled] or [**Enabled**] (Typically ISA Bridge/Native IDE)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 12 – [**Disabled**] or [Enabled] (Typically PS/2 Mouse)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 14 – [**Disabled**] or [Enabled] (Typically Hard Disk)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 15 – [**Disabled**] or [Enabled] (Typically Hard Disk)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].

- Assign DMA 0 – [**Disabled**] or [Enabled]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 1 – [**Disabled**] or [Enabled]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 2 – [**Disabled**] or [Enabled]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 3 – [Disabled] or [**Enabled**]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 5 – [Disabled] or [**Enabled**]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 6 – [Disabled] or [**Enabled**]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 7 – [Disabled] or [**Enabled**]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].

# Splash Screen Customization

The LittleBoard 800 BIOS supports a graphical splash screen, which can be customized by the user and displayed on screen when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image displayed on screen during the boot process and remain there, depending on the options selected in BIOS Setup, while the OS boots.

## Splash Screen Image Requirements

The user's image may be customized with any bitmap software editing tool, but must be converted into an acceptable format with the tools (files and utilities) provided by Ampro. If the custom image is not converted with the utilities provided, then the image will not display properly when this field is selected in BIOS Setup.

| **NOTE** | Do not use other splash screen conversion tools, as these will render an image that is not compatible with the LittleBoard 800 BIOS. |
|---|---|

The splash screen image supported by the LittleBoard 800 BIOS should be:

- Bitmap image
- Exactly 640x480 pixels
- Exactly 16 colors
- A converted file size of not greater than 55kB

## Converting the Splash Screen File

The following files are provided by Ampro on the LittleBoard 800 Doc & SW CD-ROM and are required for converting a custom splash screen file. Refer to the CD-ROM for the utilities and an example of how to load a custom image in the *lb800\software\examples\splash* directory.

- splash.bmp
- convert.exe
- convert.idf
- resplash.com
- lb800.bin

The process of converting and loading a custom image onto the LittleBoard 800 involves the following sequence of events:

- Prepare directory for conversion (create directory and copy files into it)
- Obtain the LittleBoard 800 BIOS binary
- Prepare the custom image file
- Convert the image to an acceptable BIOS format
- Merge the image with BIOS binary to create new BIOS binary
- Load the new BIOS binary onto the LittleBoard 800

| **NOTE** | You can use any Windows PC to convert the custom image, but your PC must have an internet browser to access, view, and make selections in the main menu of the LittleBoard 800 Doc & SW CD-ROM. For example: Microsoft Internet Explorer 4.x, or greater, Netscape Navigator version 4.x, or greater, or the equivalent. |
|---|---|

Use the following steps to convert and load your custom image onto the LittleBoard 800.

1. Copy the files from the *LB800\software\examples\splash* directory on the CD-ROM to a new directory (conversion directory) on your PC.

   This new conversion directory is where you intend to do the conversion and save the file.

2. Remove the read-only attributes from all the files as part of the file copying process.

3. Copy the LittleBoard 800 BIOS binary file (lb800.bin) to the new conversion directory on your PC where the other files and utilities are located.

   If this file is not on the LittleBoard 800 Doc & SW CD-ROM, you will have to obtain it from Ampro.

| **NOTE** | Ampro recommends keeping a copy of this original lb800.bin file, just in case you encounter problems with your new file or have difficulty updating the BIOS with the new image. |
|---|---|

4. Prepare your custom image file with any Windows bitmap software editing tool.

   - For example, Corel Photo-Paint, Adobe Photoshop, or the Windows Paint program provided with Windows. You can insert a desired graphic image, logo, text, etc. into the file.
   - The custom image must be a bitmap image in .bmp format at 640x480 pixels and it must be 16 colors. The file should be about 153,718 bytes. Refer to the example file splash.bmp.

5. Save your custom image file as splash.bmp at 640x480 pixels by 16 colors.

   - If your custom image file is not approximately 153,718 bytes in size it is probably not in the right format or is too complex to be used in the BIOS. You will have to edit it down in size until you have reached an acceptable file size.
   - If you are doubtful about the conversion process, due to the file size, Ampro recommends making a copy of your new splash.bmp, so that you can edit it later if the conversion does not yield a small enough file. Otherwise, you may have to re-create your custom image before you can edit it down to an acceptable file size.

6. If your custom image file is not on the conversion PC, copy the new splash.bmp file to the conversion directory.

7. Run the following command from DOS, or a Windows DOS pop-up screen to convert your new splash.bmp file.

   ```
   C:\splash>convert convert.idf
   ```

   This conversion should yield a *splash.rle* file of approximately 55kB in size or less, depending on the complexity of your image.

8. If the splash.rle file size is greater than 55kB, go back to the unconverted image file and edit the file.

   You may reduce the file size of the converted image (splash.rle) by reducing the image's complexity.

9. Run the following command to merge the converted image with the BIOS binary file.

   ```
   C:\splash>resplash lb800.bin splash.rle lb800n.bin
   ```

   This creates a new BIOS named lb800n.bin, which has the new splash image. This new BIOS is ready to be loaded onto the LittleBoard 800.

10. Copy the files update.bat, aflash.exe, and lb800n.bin to a DOS boot floppy.

11. Boot the LittleBoard 800 from the floppy and run update.bat.

12. Cycle the power to the LittleBoard 800 and enter BIOS Setup to enable the splash screen.

# Appendix A Technical Support

Ampro Computers, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Requests for support through the Virtual Technician are given the highest priority, and usually will be addressed within one working day.

- Ampro Virtual Technician – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro web site at http://ampro.custhelp.com. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online before you can log in to access this service.
- Personal Assistance – You may also request personal assistance by going to the "Ask a Question" area in the Virtual Technician. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request you can go to the "My Stuff" area and log in to check status, update your request, and access other features.
- Embedded Design Resource Center – This service is also free and available 24 hours a day at the Ampro web site at http://www.ampro.com. However, you must be registered online before you can log in to access this service.

  The Embedded Design Resource Center was created as a resource for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience. This page contains links to White Papers, Specifications, and additional technical information.

**Table A-1. Technical Support Contact Information**

| Method | Contact Information |
|---|---|
| Virtual Technician | http://ampro.custhelp.com |
| Web Site | http://www.ampro.com |
| Standard Mail | Ampro Computers, Incorporated<br>5215 Hellyer Avenue<br>San Jose, CA 95138-1007, USA |

# Appendix B LAN Boot Feature

The LittleBoard 800 provides the LAN Boot feature, which can be Enabled or Disabled in the LittleBoard 800 BIOS Setup Utility. The balance of this appendix describes the LAN Boot feature and briefly describes how to set up LAN Boot using the PXE boot agent BIOS settings.

## Introduction

LAN Boot is only supported by one of the LittleBoard 800 Ethernet ports, the 10/100BaseT LAN 1 port (J23). This feature is based on the Preboot Execution Environment (PXE), an open industry standard. PXE (pronounced “pixie”) was designed by Intel, along with other hardware and software vendors, as part of the Wired for Management (WfM) specification to improve management of desktop systems. This technology can also be applied to the embedded system market place. PXE turns the LittleBoard 800 Ethernet ports into boot devices when connected over a network (LAN).

PXE boots the LittleBoard 800 from the network (LAN) by transferring a "boot image file" from a server. This image file is typically the operating system for the LittleBoard 800, or a pre-OS agent that can perform management tasks prior to loading the image file (OS). A management task could include scanning the hard drive for viruses before loading the image file.

PXE is not operating system-specific, so the image file can load any OS. The most common application of PXE (LAN Boot) is installing an OS on a brand new device (hard disk drive) that has no operating system, (or reinstalling it when the operating system has failed or critical files have been corrupted).

Using PXE prevents the user from having to manually install all of the required software on the storage media device, (typically a hard disk drive) including the OS, which might include a stack of installation CD-ROMs. Installing from the network is as simple as connecting the ReadyBoard to the network and powering it on. The server can be set up to detect new devices and install software automatically, thereby greatly simplifying the management of small to large numbers of systems attached to a network.

If the hard disk drive should crash, the network can be set up to do a hardware diagnostic check, and once a software-related problem is detected, the server can re-install the defective software, or all the ReadyBoard software from the server. Booting from the network also guarantees a "clean" boot, with no boot-time viruses or user-modified files. The boot files are stored on the PXE server, protected from infection and user-modification.

To effectively make use of the Ampro supplied feature (LAN Boot), the LittleBoard 800 requires a PXE boot agent for set up and PXE components on the server side as well. These include a PXE server and TFTP (Trivial File Transfer Protocol) server. The PXE server is designed to work in conjunction with a Dynamic Host Configuration Protocol (DHCP) server. The PXE server can be shared with DHCP server or installed on a different server. This makes it possible to add PXE to an existing network without affecting the existing DHCP server or configuration. Refer to the web sites listed here for sources of PXE boot agents and server components. For a more detailed technical description of how PXE works go to, http://www.pxe.ca. For more detailed information concerning pre-OS agents, go to: http://www.pre-OS.com.

Ampro provides a third party PXE boot agent integrated into the LittleBoard 800 BIOS, but does not provide the PXE server components. You will also need to provide your own PXE server components on a compatible PXE server, before making full use of the LAN Boot feature. If you change the BIOS settings to enable LAN Boot, you will need to exit BIOS Setup, saving your settings, and reboot the system to enter and set the PXE boot agent settings. Refer to Chapter 4, *BIOS Setup* and Appendix B, *PXE Boot Agent BIOS Setup* for more information and configuration information.

# PXE Boot Agent BIOS Setup

This section describes the BIOS settings of the third party PXE Boot agent provided by Ampro and integrated into the LittleBoard 800 firmware. The PXE Boot Agent's BIOS setup menu and screens are used when configuring the LAN boot feature in the LittleBoard 800 BIOS.

The third party PXE Boot agent provided by Ampro supports multiple boot protocols and network environments such as traditional TCP/IP, NetWare, and RPL. It also includes support for all of the most used protocols including DHCP, BOOTP, RPL, NCP/IPX (802.2, 802.3, Ethernet II), and the Wired for Management (WfM) 2.0 specification for Preboot Execution Environment (PXE).

## Accessing PXE Boot Agent BIOS Setup

To access PXE Boot Agent BIOS Setup when LAN Boot has been selected in the LittleBoard 800 BIOS Setup screen, refer to this procedure:

1. Reboot the LittleBoard 800 after selecting LAN 1 in BIOS Setup.

   The default setting for LAN boot is [None].

2. Access the LAN Boot Setup by pressing the Ctrl +Alt + B keys, when the following message appears on the boot screen.

   ```
   Initializing MBA.  Press Ctrl + Alt + B to configure ..
   ```

3. Select from the menu options when the default screen appears as shown in Figure C-1.
4. Follow the instructions at the bottom of the screen to navigate through the selections and modify any settings.

| **NOTE** | The default values are shown highlighted (**bold text**) in the list of options on the following pages.<br><br>Refer to the bottom of the Setup screen for navigation instructions and when making selections. |
|---|---|

## PXE Boot Agent Setup Screen

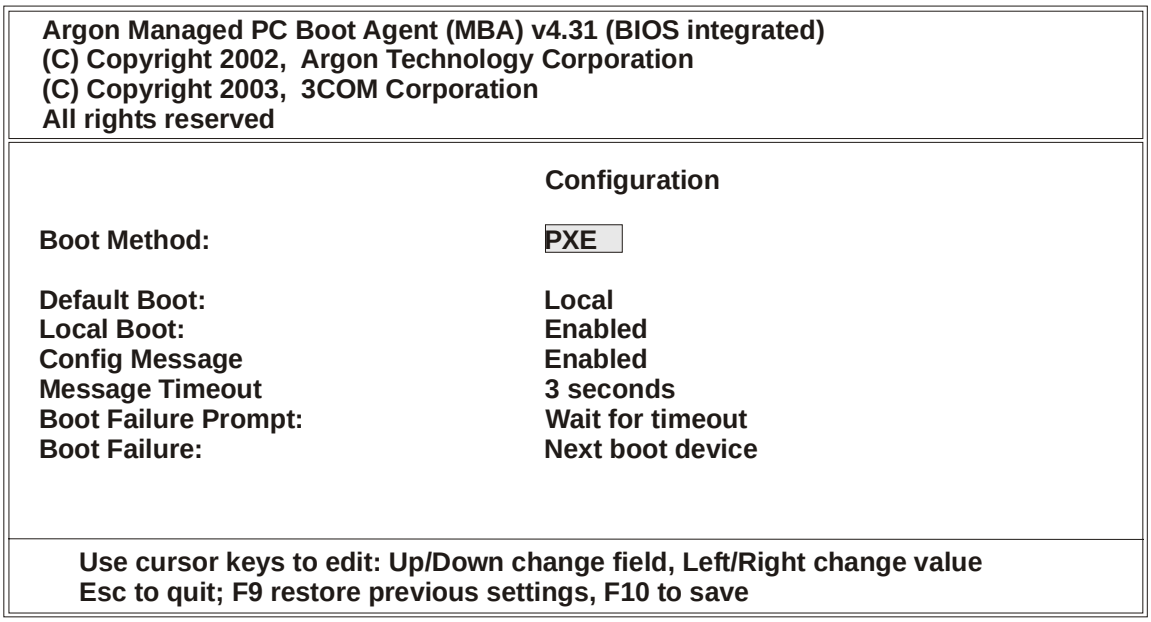



**Figure B-1. PXE Agent Boot Setup Screen**

- **PXE Configuration**
  - Boot Method: – [**PXE**], [TCP/IP], [NetWare], or [RPL]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

- **TCP/IP Configuration**
  - Boot Method: – [PXE], [**TCP/IP**], [NetWare], or [RPL]
  - Protocol: – [**DHCP**] or [BOOTP]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

- **NetWare Configuration**
  - Boot Method: – [PXE], [TCP/IP], [**NetWare**], or [RPL]
  - Protocol: – [802.2], [**802.3**], or [EthII]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

- **RPL Configuration**
  - Boot Method: – [PXE], [TCP/IP], [NetWare], or [**RPL**]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

# Appendix C Connector Part Numbers

The following table provides the connector part numbers, or the equivalent, and if applicable the ribbon-cable part number, used as the mating connector to the referenced connectors on the LittleBoard 800. All connectors use 0.100” (2.54mm) pin spacing unless otherwise indicated.

**Table C-1. Connector and Manufacture’s Part Numbers**

| Connector | Designation | Pin # | Mfg | Part Number |
|---|---|---|---|---|
| J21 | Fan | 3-pin | Molex | Housing 22-01-2037<br>Pins 08-50-0114 (discrete wires) |
| J19 | Power In | 7-pin, 0.156" (3.96mm) | Molex<br>AMP | Housing 09-50-8073<br>Housing 770849-7 |
| | | | Molex<br>AMP | Pins 08-52-0071 (discrete wires)<br>Pins 350980 (discrete wires) |
| J3, J14 | Video (CRT), Utility 3 | 10-pin | MMT<br>PHYCO | Housing IDCA001-F0502GFT<br>Housing 1100-10NP |
| | | | Belden | Flat Cable 9L28010 |
| J15 | Utility 1 | 16-pin | MMT<br>PHYCO | Housing IDCA001-F0802GFT-K<br>Housing 1100-16 |
| | | | Belden | Flat Cable 9L28016 |
| J11, J12 | Serial A & B | 20-pin | MMT<br>PHYCO | Housing IDCA001-F1002GFT-K<br>Housing 1100-20 |
| | | | Belden | 9L28020 |
| J26* | Video (LVDS) | 30-pin, 2mm | Samtec | TMM-115-02-L-D (See Note Below) |
| J13 | Utility 2 | 24-pin | 3M<br>Amphenol | Housing 3626-6600<br>Housing 812-1633-1118H |
| | | | Belden | Flat Cable 9L28024 |
| J16 | Parallel | 26-pin | MMT<br>PHYCO | Housing IDCA001-F1302GFT<br>Housing 1100-26NP |
| | | | Belden | Flat Cable 9L28025 |
| J9 | Audio In/Out | 26-pin, 2mm | MMT<br>FCI | Housing IDCB-F1302GFT<br>Housing 89947-126 |
| | | | Belden | Flat Cable 2L28016 |
| J17 | Floppy | 34-pin | AMP<br>PHYCO | Housing 746285-8<br>Housing 1100-34NP |
| | | | Belden | Flat Cable 9L28034 |
| | | | Molex<br>Samtec | Key Plug 15-04-0292<br>Key Plug PK-01 |
| J6, J7 | Primary & Secondary IDE | 40-pin | 3M | Housing 3417-7040 |
| | | | Belden | Flat Cable 9L28040 |
| | | | 3M | Key Plug 3435-0 |

**Note**: *The LVDS (J26) part number listed in this table is not the mating connector, but the component used by Ampro to stuff the LittleBoard 800. The LVDS cable provided in QuickStart Kit is an unfinished 25" long cable with one connector, which connects to J26 on the LittleBoard. Refer to this web site (http://www.samtec.com) for mating connector information.

# Index