# AR-B1476
# INDUSTRIAL GRADE
# 486DX/DX2/DX4 CPU CARD
# User’ s Guide

Edition: 1.5
Book Number: AR-B1476-02.0801

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# 0.PREFACE

## 0.1 COPYRIGHT NOTICE AND DISCLAIMER

**June 1998**

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## 0.2 WELCOME TO THE AR-B1476 CPU BOARD

This guide introduces the Acrosser AR-B1476 CPU board.

The information provided in this manual describes this card's functions and features. It also helps you start, set up and operate your AR-B1476. General system information can also be found in this publication.

## 0.3 BEFORE YOU USE THIS GUIDE

Please refer to the Chapter 3, "Setting Up the System" in this guide, if you have not already installed this AR-B1476. Check the packing list before you install and make sure the accessories are completely included.

The AR-B1476 diskette provides the newest information regarding the CPU card**. Please refer to the README.DOC file of the enclosed utility diskette**. It contains the modification and hardware & software information, and it has updated to products functions that may not be mentioned here.

## 0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires any services, contact the distributor or sales representative from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.

You can help assure efficient servicing for your product by following these guidelines:

1. Include your name, address, telephone, facsimile number and E-mail.
2. A description of the system configuration and/or software at the time is malfunction.
3. A brief description of the problem occurred.

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## 0.6 ORGANIZATION

This information for users covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview", provides an overview of the system features and packing list.
- Chapter 2, "System Controller" describes the major structure.
- Chapter 3, "Setting Up the System", describes how to adjust the jumper, and the connectors setting.
- Chapter 4, "CRT/LCD Flat Panel Display", describes the configuration and installation procedure using the LCD and CRT display.
- Chapter 5, "Installation", describes setup procedures including information on the utility diskette.
- Chapter 6, "BIOS Console", providing the BIOS options setting.
- Chapter 7, Specifications
- Chapter 8, Placement & Dimensions
- Chapter 9, Programming RS-485 & Index

## 0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.
Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system component, place all materials on an antic static surface.
- Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of every board.

# 1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

## 1.1 INTRODUCTION

The AR-B1476 is a half size industrial grade CPU card that has been designed to withstand continuous operation in harsh environments. The AR-B1476 supports on-board memory 8MB, and extends to 72MB DRAM for using one 72-pin SIMM.

The 8 layers PCB CPU card is equipped with an IDE HDD interface, a floppy disk drive adapter, 1 parallel port, 2 serial ports and a watchdog timer. Its dimensions are as compact as 122mmX185mm. It highly condensed features make it an ideal cost/performance solution for high-end commercial and industrial applications where CPU speeding and mean time between failure is critical.

The AR-B1476 provides 2 bus interfaces, ISA bus and PC/104 compatible expansion bus. Based on the PC/104 expansion bus, you could easy install thousands of PC/104 module from hundreds venders around the world. You could also directly connect the power supply to the AR-B1476 on-board power connector in standalone applications.

A watchdog timer has a software programmable time-out interval, is also provided on this CPU card. It ensures that the system does not hang-up if a program cannot execute normally.

The AR-B1476 is implemented with M1487 and M1489 chipset incorporate a memory controller, parity generation and checking, two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, an address buffer and a data buffer.

A super I/O chip (SMC37C669) is embedded in the AR-B1476 card. It combines functions of a floppy disk drive adapter, a hard disk drive (IDE) adapter, two serial (with 16C550 UART) adapters and 1 parallel adapter. The I/O port configurations can be done by set the BIOS setup program.

As an UART, the chip supports serial to parallel conversion on data characters received from a peripheral device or a MODEM, and parallel to serial conversion on data character received from the CPU. The UART includes a programmable baud rate generator, complete MODEM control capability and a processor interrupt system. As a parallel port, the SMC37C669 provides the user with a fully bi-directional parallel centronics-type printer interface.

## 1.2 PACKING LIST

The accessories are included with the system. Before you begin installing your AR-B1476 board, take a moment to make sure that the following items have been included inside the AR-B1476 package.

- This user's guide
- 1 AR-B1476 CPU card
- 1 Hard disk drive interface cable
- 1 Floppy disk drive interface cable
- 1 Parallel port interface cable & 1 RS-232C interface cable mounted on one bracket
- 1 Software utility CD.

## 1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- All In One designed 486DX/DX2/DX4 CPU card.
- Supports 3.45V/5V CPU with voltage regulator.
- Supports ISA bus and PC/104 bus.
- Supports 512KB cache on board.
- Supports on-board 8MB and extends one 72-pin DRAM SIMM up to 72MB DRAM on board.
- Supports shadow memory and EMS.
- Supports D.O.C. up to 72MB.
- Legal AMI BIOS.
- IDE hard disk drive interface.
- Floppy disk drive interface.
- Bi-direction parallel interface.
- 2 serial ports with 16C550 UART.
- Programmable watchdog timer.
- On-board built-in buzzer.
- 8 layers PCB.

# 2. SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B1476 CPU board. The following topics are covered:

- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Real-Time Clock and Non-Volatile RAM
- Timer
- Serial Port
- Parallel Port

## 2.1 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B1476 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speeding information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

Following is the system information of DMA channels:

| DMA Controller 1 | DMA Controller 2 |
|---|---|
| Channel 0: Spare | Channel 4: Cascade for controller 1 |
| Channel 1: IBM SDLC | Channel 5: Spare |
| Channel 2: Diskette adapter | Channel 6: Spare |
| Channel 3: Spare | Channel 7: Spare |

**Table 2-1 DMA Channel Controller**

## 2.2 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interruption may be used for both send and receive routines.

## 2.3 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B1476 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

Following is the system information of interrupt levels:

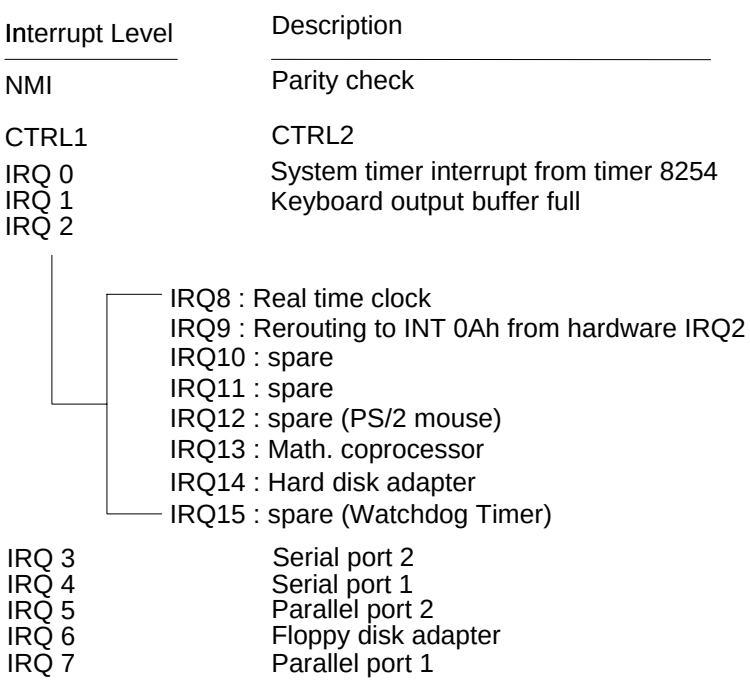



**Figure 2-1 Interrupt Controller**

### *2.3.1 I/O Port Address Map*

| Hex Range | Device |
|---|---|
| 000-01F | DMA controller 1 |
| 020-021 | Interrupt controller 1 |
| 022-023 | ALI M1489/M1487 |
| 040-04F | Timer 1 |
| 050-05F | Timer 2 |
| 060-06F | 8042 keyboard/controller |
| 070-071 | Real-time clock (RTC), non-maskable interrupt (NMI) |
| 080-09F | DMA page registers |
| 0A0-0A1 | Interrupt controller 2 |
| 0C0-0DF | DMA controller 2 |
| 0F0 | Clear Math Co-processor |
| 0F1 | Reset Math Co-processor |
| 0F8-0FF | Math Co-processor |
| 170-178 | Fixed disk 1 |
| 1F0-1F8 | Fixed disk 0 |
| 201 | Game port |
| 208-20A | EMS register 0 |
| 218-21A | EMS register 1 |
| 278-27F | Parallel printer port 2 (LPT 2) |
| 2E8-2EF | Serial port 4 (COM 4) |
| 2F8-2FF | Serial port 2 (COM 2) |
| 300-31F | Prototype card/streaming type adapter |
| 320-33F | LAN adapter |
| 378-37F | Parallel printer port 1 (LPT 1) |
| 380-38F | SDLC, bisynchronous |
| 3A0-3AF | Bisynchronous |
| 3B0-3BF | Monochrome display and printer port 3 (LPT 3) |
| 3C0-3CF | EGA/VGA adapter |
| 3D0-3DF | Color/graphics monitor adapter |
| 3E8-3EF | Serial port 3 (COM 3) |
| 3F0-3F7 | Diskette controller |
| 3F8-3FF | Serial port 1 (COM 1) |

**Table 2-2 I/O Port Address Map**

### *2.3.2 I/O Channel Pin Assignment (Bus1)*

| I/O Pin | Signal Name | Input/Output | I/O Pin | Signal Name | Input/Output |
|---|---|---|---|---|---|
| A1 | -IOCHCK | Input | B1 | GND | Ground |
| A2 | SD7 | Input/Output | B2 | RSTDRV | Output |
| A3 | SD6 | Input/Output | B3 | +5V | Power |
| A4 | SD5 | Input/Output | B4 | IRQ9 | Input |
| A5 | SD4 | Input/Output | B5 | -5V | Power |
| A6 | SD3 | Input/Output | B6 | DRQ2 | Input |
| A7 | SD2 | Input/Output | B7 | -12V | Power |
| A8 | SD1 | Input/Output | B8 | -ZWS | Input |
| A9 | SD0 | Input/Output | B9 | +12V | Power |
| A10 | -IOCHRDY | Input | B10 | GND | Ground |
| A11 | AEN | Output | B11 | -SMEMW | Output |
| A12 | SA19 | Input/Output | B12 | -SMEMR | Output |
| A13 | SA18 | Input/Output | B13 | -IOW | Input/Output |
| A14 | SA17 | Input/Output | B14 | -IOR | Input/Output |
| A15 | SA16 | Input/Output | B15 | -DACK3 | Output |
| A16 | SA15 | Input/Output | B16 | DRQ3 | Input |

| I/O Pin | Signal Name | Input/Output | I/O Pin | Signal Name | Input/Output |
|---|---|---|---|---|---|
| A17 | SA14 | Input/Output | B17 | -DACK1 | Output |
| A18 | SA13 | Input/Output | B18 | DRQ1 | Input |
| A19 | SA12 | Input/Output | B19 | -REFRESH | Input/Output |
| A20 | SA11 | Input/Output | B20 | BUSCLK | Output |
| A21 | SA10 | Input/Output | B21 | IRQ7 | Input |
| A22 | SA9 | Input/Output | B22 | IRQ6 | Input |
| A23 | SA8 | Input/Output | B23 | IRQ5 | Input |
| A24 | SA7 | Input/Output | B24 | IRQ4 | Input |
| A25 | SA6 | Input/Output | B25 | IRQ3 | Input |
| A26 | SA5 | Input/Output | B26 | -DACK2 | Output |
| A27 | SA4 | Input/Output | B27 | TC | Output |
| A28 | SA3 | Input/Output | B28 | BALE | Output |
| A29 | SA2 | Input/Output | B29 | +5V | Power |
| A30 | SA1 | Input/Output | B30 | OSC | Output |
| A31 | SA0 | Input/Output | B31 | GND | Ground |

**Table 2-3 I/O Channel Pin Assignments**

| I/O Pin | Signal Name | Input/Output | I/O Pin | Signal Name | Input/Output |
|---|---|---|---|---|---|
| C1 | -SBHE | Input/Output | D1 | -MEMCS16 | Input |
| C2 | LA23 | Input/Output | D2 | -IOCS16 | Input |
| C3 | LA22 | Input/Output | D3 | IRQ10 | Input |
| C4 | LA21 | Input/Output | D4 | IRQ11 | Input |
| C5 | LA20 | Input/Output | D5 | IRQ12 | Input |
| C6 | LA19 | Input/Output | D6 | IRQ15 | Input |
| C7 | LA18 | Input/Output | D7 | IRQ14 | Input |
| C8 | LA17 | Input/Output | D8 | -DACK0 | Output |
| C9 | -MRD16 | Input/Output | D9 | DRQ0 | Input |
| C10 | -MWR16 | Input/Output | D10 | -DACK5 | Output |
| C11 | SD8 | Input/Output | D11 | DRQ5 | Input |
| C12 | SD9 | Input/Output | D12 | -DACK6 | Output |
| C13 | SD10 | Input/Output | D13 | DRQ6 | Input |
| C14 | SD11 | Input/Output | D14 | -DACK7 | Output |
| C15 | SD12 | Input/Output | D15 | DRQ7 | Input |
| C16 | SD13 | Input/Output | D16 | +5V | Power |
| C17 | SD14 | Input/Output | D17 | -MASTER | Input |
| C18 | SD15 | Input/Output | D18 | GND | Ground |

**Table 2-4 I/O Channel Pin Assignments**

## 2.4 REAL-TIME CLOCK AND NON-VOLATILE RAM

The AR-B1476 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long period of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

| Address | Description |
|---|---|
| 00 | Seconds |
| 01 | Second alarm |
| 02 | Minutes |
| 03 | Minute alarm |
| 04 | Hours |
| 05 | Hour alarm |
| 06 | Day of week |
| 07 | Date of month |
| 08 | Month |
| 09 | Year |
| 0A | Status register A |
| 0B | Status register B |
| 0C | Status register C |
| 0D | Status register D |
| 0E | Diagnostic status byte |
| 0F | Shutdown status byte |
| 10 | Diskette drive type byte, drive A and B |
| 11 | Fixed disk type byte, drive C |
| 12 | Fixed disk type byte, drive D |
| 13 | Reserved |
| 14 | Equipment byte |
| 15 | Low base memory byte |
| 16 | High base memory byte |
| 17 | Low expansion memory byte |
| 18 | High expansion memory byte |
| 19-2D | Reserved |
| 2E-2F | 2-byte CMOS checksum |
| 30 | Low actual expansion memory byte |
| 31 | High actual expansion memory byte |
| 32 | Date century byte |
| 33 | Information flags (set during power on) |
| 34-7F | Reserved for system BIOS |

**Table 2-5 Real-Time Clock & Non-Volatile RAM**

## 2.5 TIMER

The AR-B1476 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

## 2.6 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required handle the communications link.

The following table is summary of each ACE accessible register

| DLAB | Port Address | Register |
|---|---|---|
| 0 | base + 0 | Receiver buffer (read) |
| | | Transmitter holding register (write) |
| 0 | base + 1 | Interrupt enable |
| X | base + 2 | Interrupt identification (read only) |
| X | base + 3 | Line control |
| X | base + 4 | MODEM control |
| X | base + 5 | Line status |
| X | base + 6 | MODEM status |
| X | base + 7 | Scratched register |
| 1 | base + 0 | Divisor latch (least significant byte) |
| 1 | base + 1 | Divisor latch (most significant byte) |

**Table 2-6 ACE Accessible Registers**

### (1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

### (2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

### (3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

### (4) Interrupt Identification Register (IIR)

Bit 0: "0" if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

### (5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

| WLS1 | WLS0 | Word Length |
|---|---|---|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

### (6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

### (7) Line Status Register (LSR)

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

### (8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

### (9) Divisor Latch (LS, MS)

| | LS | MS |
|---|---|---|
| Bit 0: | Bit 0 | Bit 8 |
| Bit 1: | Bit 1 | Bit 9 |
| Bit 2: | Bit 2 | Bit 10 |
| Bit 3: | Bit 3 | Bit 11 |
| Bit 4: | Bit 4 | Bit 12 |
| Bit 5: | Bit 5 | Bit 13 |
| Bit 6: | Bit 6 | Bit 14 |
| Bit 7: | Bit 7 | Bit 15 |

| Desired Baud Rate | Divisor Used to Generate 16x Clock |
|---|---|
| 300 | 384 |
| 600 | 192 |
| 1200 | 96 |
| 1800 | 64 |
| 2400 | 48 |
| 3600 | 32 |
| 4800 | 24 |
| 9600 | 12 |
| 14400 | 8 |
| 19200 | 6 |
| 28800 | 4 |
| 38400 | 3 |
| 57600 | 2 |
| 115200 | 1 |

**Table 2-7 Serial Port Divisor Latch**

## 2.7 PARALLEL PORT

### (1) Register Address

| Port Address | Read/Write | Register |
|---|---|---|
| base + 0 | Write | Output data |
| base + 0 | Read | Input data |
| base + 1 | Read | Printer status buffer |
| base + 2 | Write | Printer control latch |

**Table 2-8 Registers' Address**

### (2) Printer Interface Logic

The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

### (3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

### (4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:

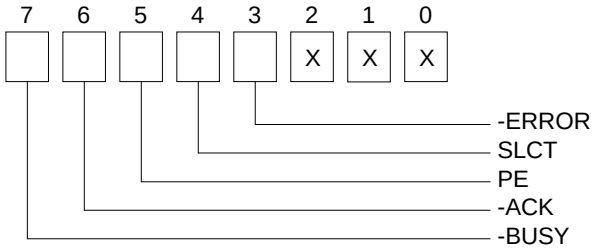



**Figure 2-2 Printer Status Buffer**

**NOTE:** X presents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A1 means the printer has detected the end of the paper.

Bit 4: A1 means the printer is selected.

Bit 3: A0 means the printer has encountered an error condition.

### (5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

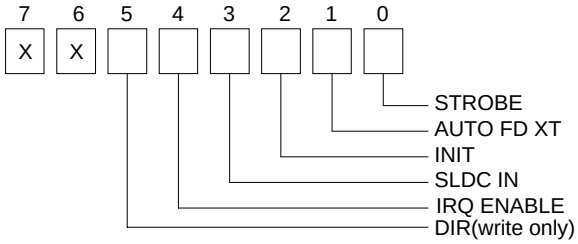



**Figure 2-3 Bit's Definition**

**NOTE:** X presents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is writing only.

Bit 4: A1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A1 in this bit position selects the printer.

Bit 2: A0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A1 causes the printer to line-feed after a line is printed.

Bit 0: A0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

# 3. SETTING UP THE SYSTEM

This section describes pin assignments for system's external connectors and the jumpers setting.

- Overview
- System Setting

## 3.1 OVERVIEW

The AR-B1476 is a half size industrial grade CPU card that has been designed to withstand continuous operation in harsh environments. This section provides hardware's jumpers setting, the connectors' locations, and the pin assignment.

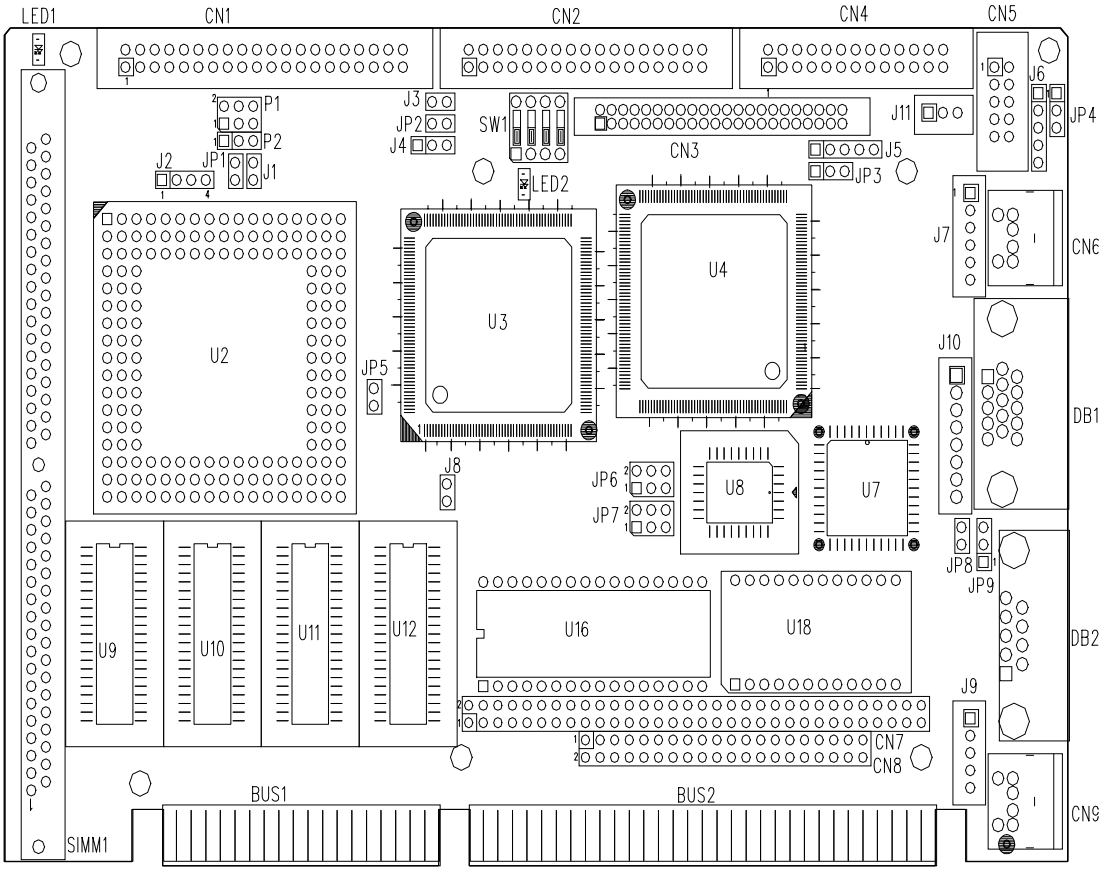



**Figure 3-1 External System Location**

## 3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor [shorting plug] that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B1476 jumper pins, and the factory-default setting.

**CAUTION:** Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

### *3.2.1 Hard Disk (IDE) Connector (CN1)*

A 40-pin header type connector (CN1) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 40-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use the BIOS Setup program. The following table illustrates the pin assignments of the hard disk drive's 40-pin connector.

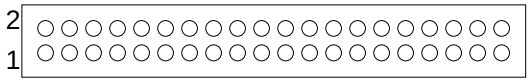



**Figure 3-2 CN1: Hard Disk (IDE) Connector**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | -RESET | 2 | GROUND |
| 3 | DATA 7 | 4 | DATA 8 |
| 5 | DATA 6 | 6 | DATA 9 |
| 7 | DATA 5 | 8 | DATA 10 |
| 9 | DATA 4 | 10 | DATA 11 |
| 11 | DATA 3 | 12 | DATA 12 |
| 13 | DATA 2 | 14 | DATA 13 |
| 15 | DATA 1 | 16 | DATA 14 |
| 17 | DATA 0 | 18 | DATA 15 |
| 19 | GROUND | 20 | NOT USED |
| 21 | NC | 22 | GROUND |
| 23 | -IOW A | 24 | GROUND |
| 25 | -IOR A | 26 | GROUND |
| 27 | -CHRDY A | 28 | NOT USED |
| 29 | NC | 30 | GROUND |
| 31 | -IRQ A | 32 | -IO16 |
| 33 | SA 1 | 34 | NOT USED |
| 35 | SA 0 | 36 | SA 2 |
| 37 | CS 0 | 38 | CS 1 |
| 39 | HD LED A | 40 | GROUND |

**Table 3-1 HDD Pin Assignment**

### *3.2.2 FDD Port Connector (CN2)*

The AR-B1476 provides a 34-pin header type connector for supporting up to two floppy disk drives.

To enable or disable the floppy disk controller, please use the BIOS Setup program.

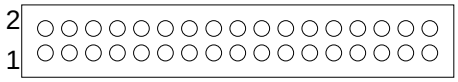



**Figure 3-3 CN2: FDD Port connector**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1-33(odd) | GROUND | 18 | -DIRECTION |
| 2 | DRVEN 0 | 20 | -STEP OUTPUT PULSE |
| 4 | NOT USED | 22 | -WRITE DATA |
| 6 | DRVEN 1 | 24 | -WRITE GATE |
| 8 | -INDEX | 26 | -TRACK 0 |
| 10 | -MOTOR ENABLE 0 | 28 | -WRITE PROTECT |
| 12 | -DRIVE SELECT 1 | 30 | -READ DATA |
| 14 | -DRIVE SELECT 0 | 32 | -SIDE 1 SELECT |
| 16 | -MOTOR ENABLE 1 | 34 | DISK CHANGE |

**Table 3-2 FDD Pin Assignment**

### *3.2.3 Parallel Port Connector (CN4)*

To use the parallel port, an adapter cable has to be connected to the CN4 (26-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B1476 package. The connector for the parallel port is a 25 pin D-type female connector.

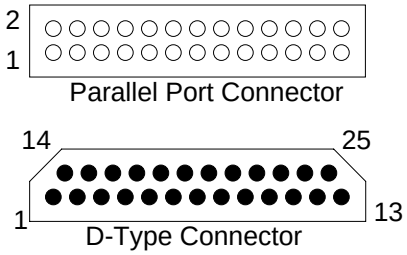



**Figure 3-4 CN4: Parallel Port Connector**

| CN4 | DB-25 | Signal | CN4 | DB-25 | Signal |
|---|---|---|---|---|---|
| 1 | 1 | -Strobe | 2 | 14 | -Auto Form Feed |
| 3 | 2 | Data 0 | 4 | 15 | -Error |
| 5 | 3 | Data 1 | 6 | 16 | -Initialize |
| 7 | 4 | Data 2 | 8 | 17 | -Printer Select In |
| 9 | 5 | Data 3 | 10 | 18 | Ground |
| 11 | 6 | Data 4 | 12 | 19 | Ground |
| 13 | 7 | Data 5 | 14 | 20 | Ground |
| 15 | 8 | Data 6 | 16 | 21 | Ground |
| 17 | 9 | Data 7 | 18 | 22 | Ground |
| 19 | 10 | -Acknowledge | 20 | 23 | Ground |
| 21 | 11 | Busy | 22 | 24 | Ground |
| 23 | 12 | Paper | 24 | 25 | Ground |
| 25 | 13 | Printer Select | 26 | -- | No Used |

**Table 3-3 Parallel Port Pin Assignment**

## *3.2.4 PC/104 Connector*

### (1) 64 Pin PC/104 Connector Bus A & B (CN7)

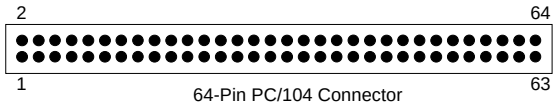



**Figure 3-5 CN7: 64 Pin PC/104 Connector Bus A & B**

CN7

| | 1 | 2 | |
|---|---|---|---|
| -IOCHCK --- | A1 | B1 | --- GND |
| SD7 --- | A2 | B2 | --- RSTDRV |
| SD6 --- | A3 | B3 | --- +5 VDC |
| SD5 --- | A4 | B4 | --- IRQ9 |
| SD4 --- | A5 | B5 | --- -5 VDC |
| SD3 --- | A6 | B6 | --- DRQ2 |
| SD2 --- | A7 | B7 | --- -12 VDC |
| SD1 --- | A8 | B8 | --- -ZWS |
| SD0 --- | A9 | B9 | --- +12 VDC |
| IOCHRDY--- | A10 | B10 | --- GND |
| AEN --- | A11 | B11 | --- -SMEMW |
| SA19 --- | A12 | B12 | --- -SMEMR |
| SA18 --- | A13 | B13 | --- -IOW |
| SA17 --- | A14 | B14 | --- -IOR |
| SA16 --- | A15 | B15 | --- -DACK3 |
| SA15 --- | A16 | B16 | --- DRQ3 |
| SA14 --- | A17 | B17 | --- -DACK1 |
| SA13 --- | A18 | B18 | --- DRQ1 |
| SA12 --- | A19 | B19 | --- -REFRESH |
| SA11 --- | A20 | B20 | --- BUSCLK |
| SA10 --- | A21 | B21 | --- IRQ7 |
| SA9 --- | A22 | B22 | --- IRQ6 |
| SA8 --- | A23 | B23 | --- IRQ5 |
| SA7 --- | A24 | B24 | --- IRQ4 |
| SA6 --- | A25 | B25 | --- IRQ3 |
| SA5 --- | A26 | B26 | --- -DACK2 |
| SA4 --- | A27 | B27 | --- TC |
| SA3 --- | A28 | B28 | --- BALE |
| SA2 --- | A29 | B29 | --- +5 VDC |
| SA1 --- | A30 | B30 | --- OSC |
| SA0 --- | A31 | B31 | --- GND |
| GND --- | A32 | B32 | --- GND |

**Figure 3-6 CN7: 64-Pin PC/104 Connector Bus A & B**

### (2) 40 Pin PC/104 Connector Bus C & D (CN8)

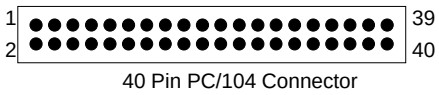



**Figure 3-7 CN8: 40 Pin PC/104 Connector Bus C & D**

CN8

| | 1 | 2 | |
|---|---|---|---|
| GND --- | C1 | D1 | --- GND |
| -BHE --- | C2 | D2 | --- -MEM16 |
| LA23 --- | C3 | D3 | --- -IOCS16 |
| LA22 --- | C4 | D4 | --- IRQ10 |
| LA21 --- | C5 | D5 | --- IRQ11 |
| LA20 --- | C6 | D6 | --- IRQ12 |
| LA19 --- | C7 | D7 | --- IDEIRQA |
| LA18 --- | C8 | D8 | --- IDEIRQB |
| LA17 --- | C9 | D9 | --- -DACK0 |
| -MRD16 --- | C10 | D10 | --- DRQ0 |
| -MWR16 --- | C11 | D11 | --- -DACK5 |
| SD8 --- | C12 | D12 | --- DRQ5 |
| SD9 --- | C13 | D13 | --- -DACK6 |
| SD10 --- | C14 | D14 | --- DRQ6 |
| SD11 --- | C15 | D15 | --- -DACK7 |
| SD12 --- | C16 | D16 | --- DRQ7 |
| SD13 --- | C17 | D17 | --- +5 VDC |
| SD14 --- | C18 | D18 | --- -MASTER |
| SD15 --- | C19 | D19 | --- GND |
| Not Used --- | C20 | D20 | --- GND |

**Figure 3-8 CN8: 40-Pin PC/104 Connector Bus C & D**

### (3) I/O Channel Signal Description

| Name | Description |
|---|---|
| **BUSCLK** [Output] | The BUSCLK signal of the I/O channel is asynchronous to the CPU clock. |
| **RSTDRV** [Output] | This signal goes high during power-up, low line-voltage or hardware reset |
| **SA0 - SA19** [Input / Output] | The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE" |
| **LA17 - LA23** [Input/Output] | The Unlatched Address line run from bit 17 to 23 |
| **SD0 - SD15** [Input/Output] | System Data bit 0 to 15 |
| **BALE** [Output] | The Buffered Address Latch Enable is used to latch SA0 - SA19 onto the falling edge. This signal is forced high during DMA cycles |
| **-IOCHCK** [Input] | The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board |
| **IOCHRDY** [Input, Open collector] | This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address |
| **IRQ 3-7, 9-12, 14, 15** [Input] | The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest) |
| **-IOR** [Input/Output] | The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus |
| **-IOW** [Input/Output] | The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus |
| **-SMEMR** [Output] | The System Memory Read is low while any of the low 1 mega bytes of memory are being used |
| **-MEMR** [Input/Output] | The Memory Read signal is low while any memory location is being read |
| **-SMEMW** [Output] | The System Memory Write is low while any of the low 1 mega bytes of memory is being written |
| **-MEMW** [Input/Output] | The Memory Write signal is low while any memory location is being written |
| **DRQ 0-3, 5-7** [Input] | DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest) |
| **-DACK 0-3, 5-7** [Output] | The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7 |
| **AEN** [output] | The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus |
| **-REFRESH** [Input/Output] | This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel |
| **TC** [Output] | Terminal Count provides a pulse when the terminal count for any DMA channel is reached |
| **SBHE** [Input/Output] | The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus |

| Name | Description |
|---|---|
| **-MASTER** [Input] | The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh |
| **-MEMCS16** [Input, Open collector] | The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation |
| **-IOCS16** [Input, Open collector] | The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation |
| **OSC** [Output] | The Oscillator is a 14.31818 MHz signal used for the color graphic card |
| **-ZWS** [Input, Open collector] | The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle |

**Table 3-4 I/O Channel Signal's Description**

## *3.2.5 LED Header*

### (1) External Power LED & Keyboard Lock Header (J6)

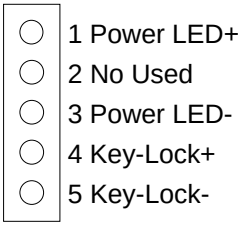



**Figure 3-9 J6: Power LED & Keyboard Lock Header**

### (2) HDD LED Header (J3)

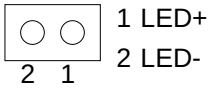



**Figure 3-10 J3: HDD LED Header**

### (3) Watchdog LED Header (J1)

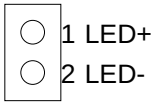



**Figure 3-11 J1: Watchdog LED Header**

## *3.2.6 Serial Port*

### (1) RS-232/RS-485 Select (SW1, JP4 & JP9)

JP4 selects COM B port, and adjusts the CN5 connector is RS-485 or RS-232C. JP9 selects COM A port for using DB2 for RS-232C or connects External RS-485. SW1 adjusts the onboard RS-485.

**(A) COM-A RS-485 Adapter Select (JP9)**

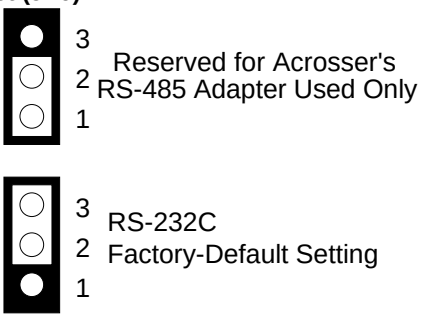



**Figure 3-12 JP9: COM-A RS-485 Adapter Select**

**(B) COM-B RS-485 Adapter Select (JP4)**

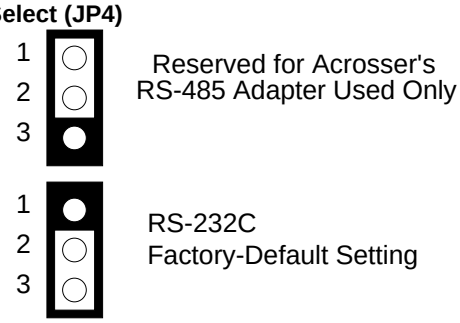



**Figure 3-13 JP4: COM-B RS-485 Adapter Select**

**(C) COM-B RS-232/RS-485 Select (SW1)**

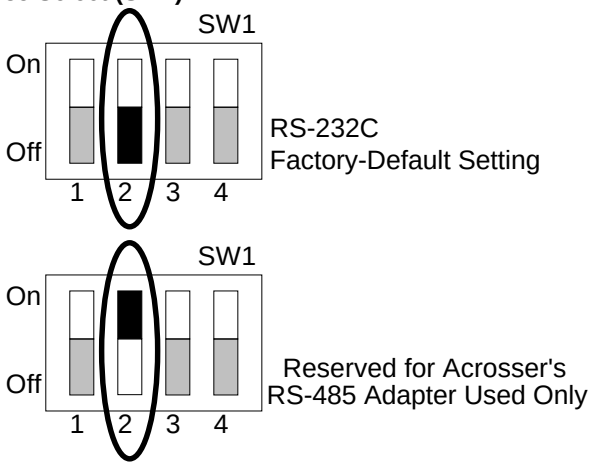



**Figure 3-14 SW1: COM-B RS-232/RS-485 Select**

### (2) RS-485 Terminator Select (JP2)

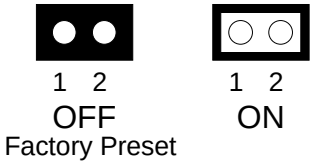



**Figure 3-15 JP2: RS-485 Terminator Select**

### (3) RS-485 Connector (J4)

J4 is onboard RS-485 header, J4 pin assignments are as follows:

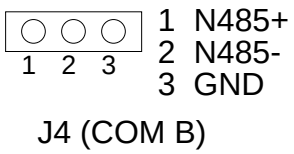



**Figure 3-16 J4: RS-485 Connector**

### (4) RS-232 Connector (CN5 & DB2)

There are two serial ports with EIA RS-232C interface on the AR-B1476. COM A uses one onboard D-type 9 pin male connector (DB2) and COM B uses one 10 pin header (CN5) which are located at the right side of the card. To configure these two serial ports, use the BIOS Setup program, and adjust the jumpers on JP4 and JP9.

The pin assignments of the DB2 and CN5 for serial port A & B are as follows:

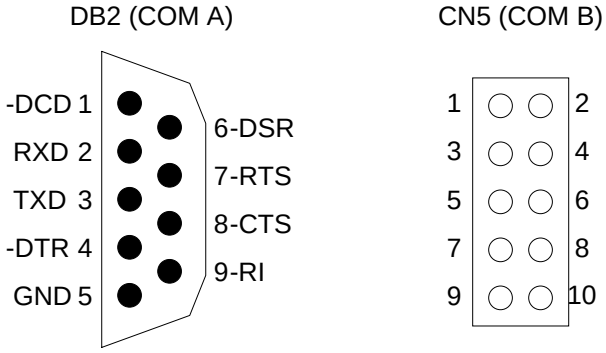



**Figure 3-17 DB2 & CN5: RS-232 Connector**

| CN5 | DB2 | Signal | CN5 | DB2 | Signal |
|---|---|---|---|---|---|
| 1 | 1 | -DCD | 2 | 6 | -DSR |
| 3 | 2 | RXD | 4 | 7 | -RTS |
| 5 | 3 | TXD | 6 | 8 | -CTS |
| 7 | 4 | -DTR | 8 | 9 | -RI |
| 9 | 5 | GND | 10 | -- | Not Used |

**Table 3-5 RS-232 Connector Pin Assignment**

### *3.2.7 Keyboard Connector (CN9 & J9)*

CN9 is a Mini-DIN 6-pin connector. This keyboard connector is a PS/2 type keyboard connector. This connector is also for a standard IBM-compatible keyboard with the keyboard adapter cable. J9 provides another way of connecting a keyboard to the AR-B1476.

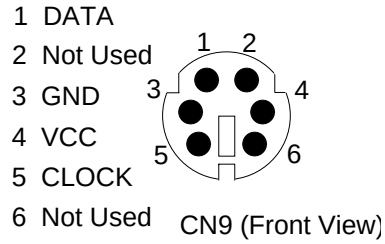



**Figure 3-18 CN9: Keyboard Connector**

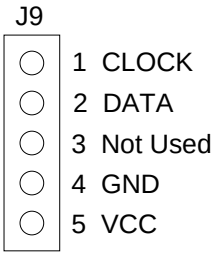



**Figure 3-19 J9: AUX. Keyboard Connector**

### *3.2.8 External Speaker Header (J2)*

Besides the onboard buzzer, you can use an external speaker by connecting to the J2 header.

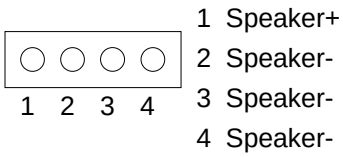



**Figure 3-20 J2: Speaker Header**

### *3.2.9 Power Connector (J10)*

J10 is an 8-pin power connector. You can directly connect the power supply to the onboard power connector for stand-alone applications.

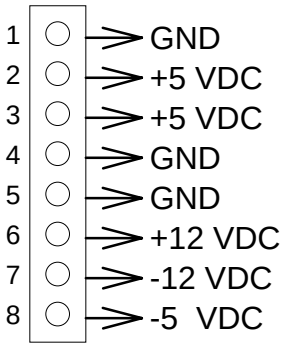



**Figure 3-21 J10: Power Connector**

### *3.2.10 Reset Header (J8)*

J8 is used to connect to an external reset switch. Shorting these two pins will reset the system.


**Figure 3-22 J8: Reset Header**

### *3.2.11 PS/2 Mouse Connector*

**(1) PS/2 Mouse IRQ12 Setting (JP8)**

The default of <Enabled> allows the system detecting a PS/2 mouse on boot. If detected, IRQ12 will be used for the PS/2 mouse. IRQ12 will be reserved for expansion cards and therefore the PS/2 mouse will not function.

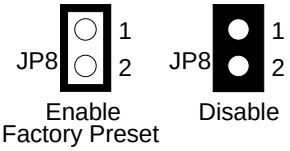



**Figure 3-23 JP8: PS/2 Mouse IRQ12 Setting**

**CAUTION:** After adjusting the JP8 correctly, the user must set the <PS/2 Mouse Support> option to Enabled in the BIOS <Advanced CMOS Setup> Menu. Then the PS/2 mouse can be used.

**(2) PS/2 Mouse Connector (CN6 & J7)**

To use the PS/2 interface, an adapter cable has to be connected to the CN6 and J7 (6-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B1476 package. The connector for the PS/2 mouse is a Mini-DIN 6-pin connector. Pin assignments for the PS/2 port connector are as follows:

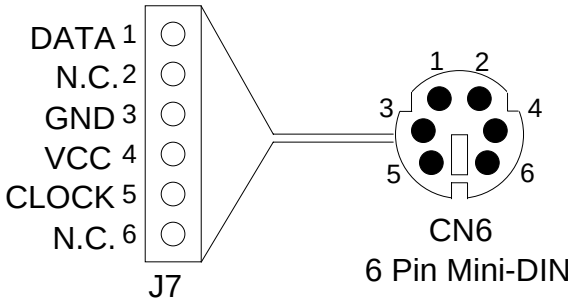



**Figure 3-24 CN6 & J7: PS/2 Mouse Connector**

## *3.2.12 CPU Setting*

The AR-B1476 accepts many types of microprocessors such as Intel/AMD/Cyrix 486DX/DX2/DX4. All of these CPUs include an integer processing unit, floating-point processing unit, memory-management unit, and cache. They can give a two to ten-fold performance improvement in speed over the 386 processor, which is depending on the clock speeds used and specific application. Like the 386 processor, the 486 processor includes both segment-based and page-based memory protection schemes. The instruction of processing time is reduced by on-chip instruction pipelining. By performing fast, on-chip memory management and caching, the 486 processor relaxes requirements for memory response for a given level of system performance.

### (1) CPU Logic Core Voltage Select (P1 & P2)

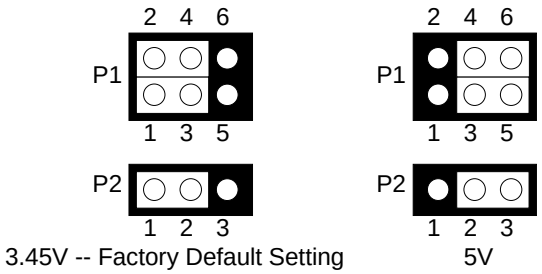



**Figure 3-25 P1 & P2: CPU Logic Core Voltage**

### (2) AMD 3X/4X CPU Select (JP5)

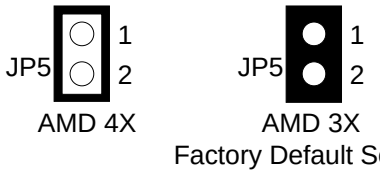



**Figure 3-26 JP5: AMD 3X/4X CPU Select**

### (3) PCI Clock Select (JP7)

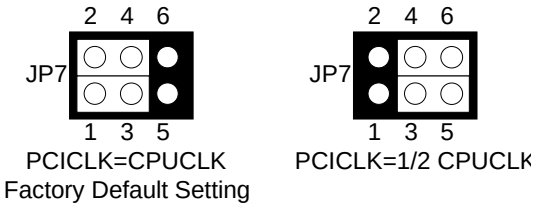



**Figure 3-27 JP7: PCI Clock Select**

### (4) CPU Clock Multiplier Select (JP6)

| A | B | Base Clock | Note |
|---|---|---|---|
| Close | Close | 50MHz | |
| Open | Close | 40MHz | |
| Close | Open | 33.3MHz | Factory Preset |
| Open | Open | 25MHz | |

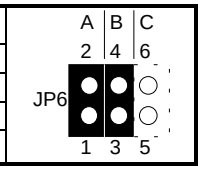



**Table 3-6 JP6: CPU Clock Multiplier Select**

## *3.2.13 Memory Setting*

### (1) DRAM Configuration

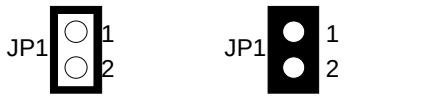
There are two 32-bit memory banks on the AR-B1476 board. It can be one-side or double-side SIMM (Single-Line Memory Modules) which is designed to accommodate 256KX36 bit to 16MX36-bit SIMMs. This provides the user with up to 64MB of main memory. The 32-bit SIMM (without parity bit) also can be used on AR-B1476 board. There are listing on-board memory configurations available. Please refer to the following table for details:

| SIMM1 | Total Memory |
|---|---|
| 256KX32(X36) | 1MB |
| 512KX32(X36) | 2MB |
| 1MX32(X36) | 4MB |
| 2MX32(X36) | 8MB |
| 4MX32(X36) | 16MB |
| 8MX32(X36) | 32MB |
| 16MX32(X36) | 64MB |

**Table 3-7 DRAMs' Configuration**

### (2) Cache RAM (JP1)

The AR-B1476 can be configured to provide a write-back or write-through cache scheme and support 512KB cache systems. A write-back cache system may provide better performance than a write-through cache system. The BIOS Setup program allows you to set the cache scheme either write-back or write-through, either the internal cache selection.




Write-Through Write-Back
Factory Default Setting

**Figure 3-28 JP1: Write-Through/Write-Back CPU Select**

### (3) Cache Size Select (CP1)

The CP1 is located on the back of CPU card. The factory setting is fixed is 512K Byte, this function can't be supplied for user adjusting. The type of setting's table is in following.

| CP1 | Data RAM | TAG RAM | SIZE |
|---|---|---|---|
| OPEN | four 64K x 8 | 32K x 8 | 256KB |
| CLOSE | four 128K x 8 | 32K x 8 | 512KB |

**Table 3-8 Cache Size Selected**

## *3.2.14 DiskOnChip Installation (SW1)*

The DiskOnChip is a new generation of high performance single-chip Flash Disk. It provides a Flash Disk in a standard 32-pin DIP package.

This unique data storage solution offers a better, faster, and more cost-effective Flash Disk for Single Board embedded systems. The DiskOnChip provides a Flash Disk that does not require any bus, slot or connector. Simply insert the DiskOnChip into 32-pin socket U16 position on the CPU board. It is the optimal solution for single board computers, it is a small, fully functional, easy to integrate, plug-and-play Flash Disk with a very low power consumption.

The DiskOnChip is fully tested and formatted before the product is shipped.

### (1) DiskOnChip Hardware Installation

**Step 1:** Make sure the target platform is powered OFF

**Step 2:** Plug the DiskOnChip device into the U16 socket. Verify the direction is correct (pin 1 of the DiskOnChip is aligned with pin 1 of the U16 socket)

**Step 3:** Power up the system

**Step 4:** During power up you may observe the messages displayed by the DiskOnChip when its drivers are automatically loaded into system's memory

**Step 5:** At this stage the DiskOnChip can be accessed as any disk in the system

**Step 6:** If the DiskOnChip is the only disk in the system, it will appear as the first disk (drive C: in DOS)

**Step 7:** If there are more disks besides the DiskOnChip, it will appear by default as the last drive, unless it was programmed as first drive.

**Step 8:** If you want the DiskOnChip to be bootable, copy the operating system files into the DiskOnChip by using the standard DOS command.

### (2) DiskOnChip Memory Address Setting (SW1)

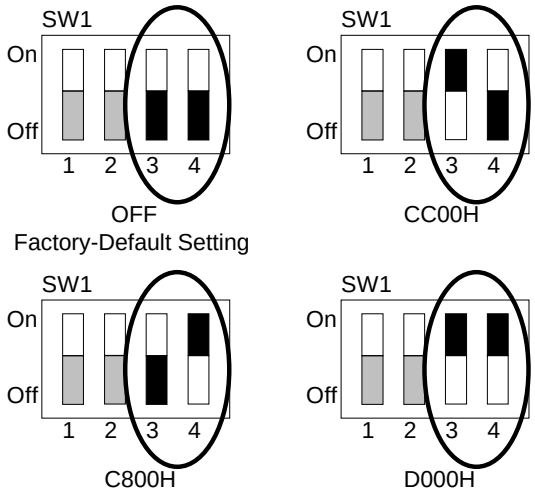



**Figure 3-29 SW1: DiskOnChip Memory Address Setting**

### (3) Configuring the DiskOnChip as a Bootable Disk

The DiskOnChip fully supports the BOOT capability. In order for the DiskOnChip to be bootable, it should be DOS formatted as bootable, like any floppy or hard disk that required to be booted.

| |
|---|
| SYS D:<br><br>Change the disk into bootable (assuming the DiskOnChip is disk D) |

# 4. CRT/LCD FLAT PANEL DISPLAY

This section describes the configuration and installation procedure using LCD and CRT display.

- CRT Connector
- LCD Flat Panel Display
- Supported LCD Panel

## 4.1 CRT CONNECTOR (DB1)

The AR-B1476 supports CRT color monitors. AR-B1476 used onboard VGA chipset and supported 1MB on-board VRAM. For different VGA display modes, your monitor must possess certain characteristics to display the mode you want.

To connect to a CRT monitor, an adapter cable has to be connected to the DB1 connector. DB1 is used to connect with a VGA monitor when you are using the on-board VGA controller as a display adapter. Pin assignments for the DB1 connector are as follows:

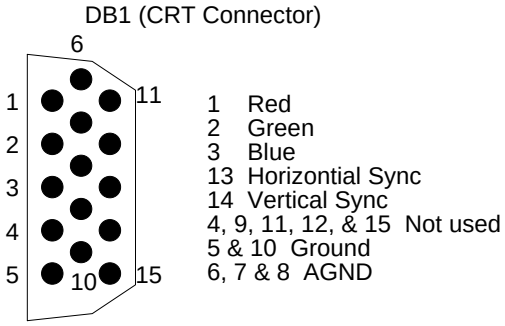



**Figure 4-1 DB1: CRT Connector**

## 4.2 LCD FLAT PANEL DISPLAY

This section describes the configuration and installation procedure for a LCD display. Skip this section if you are using a CRT monitor only.

Use the Flash memory Writer utility to download the new BIOS file into the ROM chip to configure the BIOS default settings for different types of LCD panels. Next, set your system properly and configure the AR-B1476 VGA module for the right type of LCD panel you are using.

The following shows the block diagram of the system when using the AR-B1476 with a LCD display.

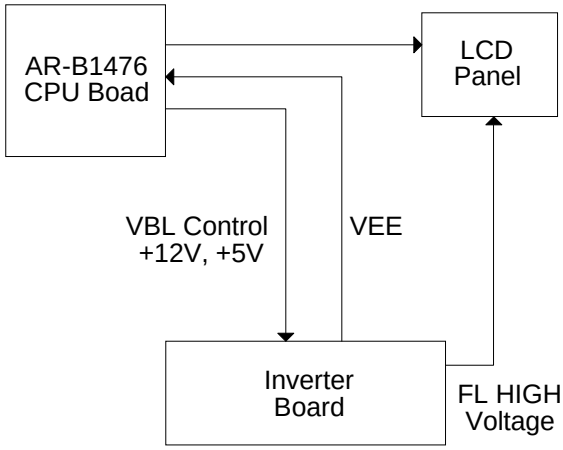



**Figure 4-2 LCD Panel Block Diagram**

The block diagram shows that the AR-B1476 still needs components to use with a LCD panel. The inverter board provides the control for the brightness and the contrast of the LCD panel. The inverter is also the components that supply the high voltage to drive the LCD panel. Each item will be explained further in the section.

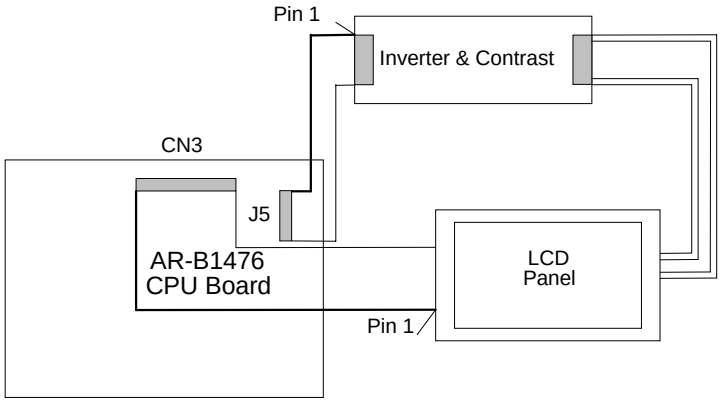



**Figure 4-3 LCD Panel Cable Installation Diagram**

**NOTE:** Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. Pin 1 of the cable connector is indicated with a sticker and pin1 of the ribbon cable is usually has a different color.

### *4.2.1 Inverter Board Description*

The inverter board supplies high voltage signals to drive the LCD panel by converting the 12 volt signal from the AR-B1476 into a high voltage AC signal for LCD panel. It can be installed freely on the space provided over the VR board. If the VR board is installed on the bracket, you have to provide a place to install the inverter board into your system.

### *4.2.2 LCD Connector*

**(1) DE/E Signal from M or LP Select (JP3)**

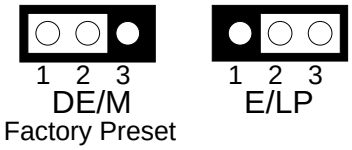



**Figure 4-4 JP3: DE/E Signal from M or LP**

**(2) LCD Control Connector (J5)**

J5 is a 5-pin connector that attaches to the Contrast and Backlight board. Its pin assignment is shown below:

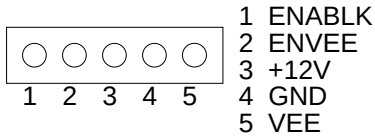



**Figure 4-5 J5: LCD Control Connector**

**(3) Touch Screen Connector (J11)**

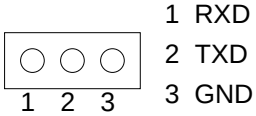



**Figure 4-6 J11: Touch Screen Connector**

### (4) LCD Panel Display Connector (CN3)

Attach a display panel connector to this 44-pin connector with pin assignments as shown below:

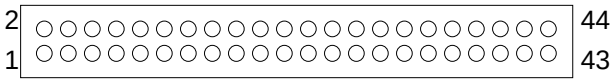



**Figure 4-7 CN3: LCD Display Connector**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GND | 2 | SHFCLK |
| 3 | GND | 4 | LP |
| 5 | FLM | 6 | GND |
| 7 | P0 | 8 | P1 |
| 9 | P2 | 10 | P3 |
| 11 | P4 | 12 | P5 |
| 13 | GND | 14 | P6 |
| 15 | P7 | 16 | P8 |
| 17 | P9 | 18 | P10 |
| 19 | P11 | 20 | GND |
| 21 | P12 | 22 | P13 |
| 23 | P14 | 24 | P15 |
| 25 | P16 | 26 | P17 |
| 27 | GND | 28 | P18 |
| 29 | P19 | 30 | P20 |
| 31 | P21 | 32 | P22 |
| 33 | P23 | 34 | GND |
| 35 | VCC | 36 | VCC |
| 37 | +12V | 38 | +12V |
| 39 | GND | 40 | GND |
| 41 | DE | 42 | ENABLK |
| 43 | GND | 44 | VEE |

**Table 4-1 LCD Display Assignment**

## 4.3 SUPPORTED LCD PANEL

At present, this VGA card can provide a solution with an inverter board for the following list of standard LCD panels. Consult your Acrosser representative for new developments. When using other models of standard LCD panels in the market.

| NO. | Manufacture | Model No. | Description |
|---|---|---|---|
| 1 | NEC | NL-6448AC30-10 | TFT 9.4" |
| 2 | NEC | NL-6448AC32-10 | TFT 10.2" |
| 3 | NEC | NL-6448AC33-10 | TFT 10.4" |
| 4 | HITACHI | LMG5371 | MONO 9.4" Dual Scan |
| 5 | HITACHI | LMG9200 | DSTN 9.4" |
| 6 | HITACHI | LMG9400 | DSTN 10.4" |
| 7 | ORION | OGM-640CN03C-S | DSTN 10.4" |
| 8 | SHARP | LQ10D321 | TFT 10.4" |

**Table 4-2 LCD Panel Type List**

**CAUTION:** 1. If you want to connect the LCD panel, you must update the AR-B1476's BIOS, then you can setup the corrected BIOS. Please contact Acrosser for the latest BIOS update.

2. If user needs to update the BIOS version or connect other LCD, please contact the sales department. The detail supported LCDs are listed in the Acrosser Web site, user can download the suitable BIOS. The address is as follows:

**http:\\www.acrosser.com**

# 5. INSTALLATION

This chapter describes the procedure of the utility diskette installation. The following topics are covered:

- Overview
- Utility Diskette
- Watchdog Timer

## 5.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B1476 CPU board. Please read the details of the CPU board's hardware descriptions before installation carefully, especially jumpers' setting, switch settings and cable connections.

Follow steps listed below for proper installation:

**Step 1 :** Read the CPU card's hardware description in this manual.

**Step 2 :** Install any DRAM SIMM onto the CPU card. (or user can skip this step because that the AR-B1476 embedded on-board DRAM)

**Step 3 :** Set jumpers.

**Step 4 :** Make sure that the power supply connected to your passive CPU board backplane is turned off.

**Step 5 :** Plug the CPU card into a free AT-bus slot or PICMG slot on the backplane and secure it in place with a screw to the system chassis.

**Step 6 :** Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to pin 1 of the related connector.

**Step 7 :** Connect the hard disk/floppy disk flat cables from the CPU card to the drives. Connect a power source to each drive.

**Step 8 :** Plug the keyboard into the keyboard connector.

**Step 9 :** Turn on the power.

**Step 10:** Configure your system with the BIOS Setup program then re-boot your system.

**Step 11:** If the CPU card does not work, turn off the power and read the hardware description carefully again.

**Step 12:** If the CPU card still does not perform properly, return the card to your dealer for immediate service.

## 5.2 UTILITY DISKETTE

AR-B1476 provides two VGA driver diskettes. It supports WIN31, WIN95, WINNT 4.0 and OS/2. If your operating system is the other operating system, please attach Acrosser that will provide the technical supporting for the VGA resolution.

There are two diskettes: disk 1 is for WIN31, WIN95 & WINNT4.0 VGA resolution; disk 2 is for OS/2 VGA resolution. While user extracted the compressed files there is the README.* file in each sub-directories. Please refer to the file of README for any troubleshooting before install the driver.

## *5.2.1 VGA Driver*

### (1) WIN 3.1 Driver

For the WIN31 operating system, user must in the DOS mode decompress the compress file. And then as to the steps:

**Step 1:** Make the new created directory to put the VGA drivers.
`C:\>MD VGAW31`

**Step 2:** Insert the Utility Disk #1 in the floppy disk drive, and then copy the compress file—D54XW31P.ZIP, and the extract program—PKUNZIP.EXE, in the new created directory.
`C:\>COPY A:\ D54XW31P.ZIP C:\VGAW31`
`C:\>COPY A:\PKUNZIP.EXE C:\VGAW31`

**Step 3:** Change directory to the new created directory, and extract the compress file.
`C:\>CD VGAW31`
`C:\VGAW31>PKUNZIP -d D54XW31P.ZIP`

**Step 4:** And then re-name the SET545P.SCP file as SETUP5XX.SCP. Acrosser recommends the method as:
C:\VGAW31>COPY SET545P.SCP SETUP5XX.SCP

**Step 5:** In the DOS mode execute the SETUP.EXE file.
C:\VGAW31>SETUP

**Step 6:** The screen shows the chip type, and presses any key enter the main menu.
CHIPS 655XX - PCI Display Drivers
Preliminary Version 3.3.0

**Step 7:** There are some items for choice to setup. Please choose the <Windows Version 3.1> item, notice the function key defined. Press [ENTER] selected the <All Resolutions>, when this line appears [*] symbol, that means this item is selected. Press [End] starts to install.

**Step 8:** The screen will show the dialog box to demand user typing the WIN31's path. The default is C:\WINDOWS.

**Step 9:** Follow the setup steps' messages execute. As completed the setup procedure will generate the message as follow.

Installation is done!

Change to your Windows directory and type SETUP to run the Windows Setup program. Choose one of the new drivers marked by an *. Please refer to the User's Guide to complete the installation.

**Step 10:** Presses [Esc] return the main menu, and re-press [Esc] return to the DOS mode.

**Step 11:** In the WIN31, you can find the <Chips CPL> icon located in the {CONTROL PANEL} group.

**Step 12:** Adjust the <Refresh Rate>, <Cursor Animation>, <Font size>, <Resolution>, and <Big Cursor>.

### (2) WIN 95 Driver

For the WIN95 operating system, user must in the DOS mode decompress the compress file. And then as to the steps:

**Step 1:** Make the new created directory to put the VGA drivers.
C:\>MD VGAW95

**Step 2:** Insert the Utility Disk #1 in the floppy disk drive, and then copy the compress file—D55XW95.ZIP, and the extract program—PKUNZIP.EXE, in the new created directory.
C:\>COPY A:\D55XW95.ZIP C:\VGAW95
C:\>COPY A:\PKUNZIP.EXE C:\VGAW95

**Step 3:** Change directory to the new created directory, and extract the compress file.
C:\>CD VGAW95
C:\VGAW95>PKUNZIP -d D55XW95.ZIP

**Step 4:** Enter the WIN95 operation system and please choose the <SETTING> item of the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.
C:\VGAW95

**Step 5:** And then you can find the <Chips and Tech 65545 PCI (new)> item, select it and click the <OK> button.

**Step 6:** Finally, user can find the <DISPLAY> icon adds the <Chips> item. You can select this item, and adjust the <Screen Resolution>, <Refresh Rate>, <Font Size>…and other functions. Please refer to the messages during installation.

### (3) WINNT 4.0 Driver

For the WINNT4.0 operating system, user must in the DOS mode decompress the compress file. And then as to the steps:

**Step 1:** Make the new created directory to put the VGA drivers.
C:\>MD VGANT40

**Step 2:** Insert the Utility Disk #1 in the floppy disk drive, and then copy the compress file—D5XXNT4.ZIP, and the PKUNZIP.EXE program—, in the new created directory.
C:\>COPY A:\D5XXNT4.ZIP C:\VGANT40
C:\>COPY A:\PKUNZIP.EXE C:\VGANT40

**Step 3:** Change directory to the new created directory, and extract the compress file.
C:\>CD VGANT40
C:\ VGANT40>PKUNZIP -d D5XXNT4.ZIP

**Step 4:** Enter the WINNT4.0 operation system and please choose the <SETTING> item of the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.
C:\VGANT40

**Step 5:** And then you can find the <Chips and Tech 65545 PCI (new)> item, select it and click the <OK> button.

**Step 6:** Finally, user can find the <DISPLAY> icon adds the <Chips> item. You can select this item, and adjust the <Screen Resolution>, <Refresh Rate>, <Font Size>…and other function. Please refer to the messages during installation.

**(4) OS/2 Warp Driver**

The following steps must be performed before you install the 65545/65548 display's driver:

**CAUTION:**

1. OS/2 DOS Support must be installed.
2. If you previously installed SVGA support, you must do the following:
   a) Close all DOS Full Screen and WIN-OS2 sessions.
   b) Reset the system to VGA mode. VGA is the default video mode enabled when OS/2 is installed. To restore VGA mode, use Selective Install and select VGA for Primary Display. For more information on this procedure, see the section on Changing Display Adapter Support in the OS/2 Users Guide.

To install this driver, do the following steps:

**Step 1:** Open an OS/2 full screen or windowed session.

**Step 2:** Place the 65545/65548 PCI Display Driver Diskette in drive A. (DISK #2)

**Step 3:** Because the diskette enclosed the compress file, to extract file had to as the steps.

**Step 4:** In the OS/2-DOS mode, make the VGA directory for decompress the driver.
C:\>MD VGAOS2
C:\>CD VGAOS2
C:\VGAOS2>COPY A:*.*
C:\VGAOS2>PKUNZIP -d D54XOS2P.ZIP

**Step 5:** At the OS/2 command prompt, type the following commands to copy the files to the OS/2 drive:
C:\VGAOS2> SETUP C:\VGAOS2 C: <ENTER>

**Step 6:** When the Setup Program is completed, you will need to perform a shutdown and then restart the system in order for changes to take effect.

**Step 7:** Please refer to the README.TXT file, there is detail description, user had to according to the installation step by step. When install completed, user can adjust the VGA resolution in the SYSTEM icon <SCREEN> item of the <SYSTEM SETUP>.

## *5.2.2 BIOS FLASH Utility*

The main function of AMIFLASH.COM supports BIOS update. The AR-B1476 can provide FLASH BIOS update function for you to easily upgrade newer BIOS version. Please contact Acrosser engineer to support the modification of the BIOS.

1. Use the AMIFLASH.COM program to update the BIOS setting function.

2. And then refer to the section "BIOS Console", as the steps to modify BIOS.

3. Now the CPU board's BIOS is the newest, user can use this program to modify BIOS function in the future, when the BIOS adding some function.

## 5.3 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, disabled, enabled, and trigger.
The AR-B1476 is equipped with a programmable time-out period watchdog timer. User can use the program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out because of system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be 3 to 42 seconds.

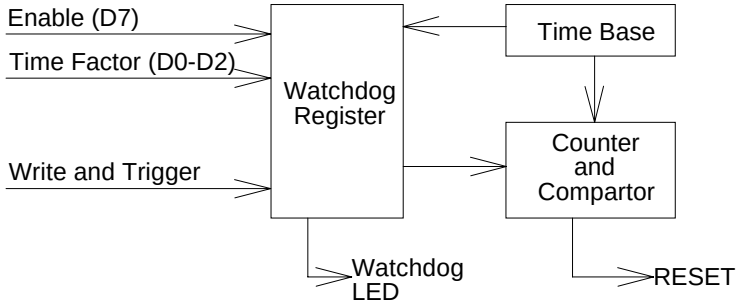



**Figure 5-1 Watchdog Block Diagram**

### *5.3.1 Watchdog Timer Setting*

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.
Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger the IRQ15 signal to tell your program that the watchdog is times out.
The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 7 timer factors.
If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out periods.

| Time Factor | Time-Out Period (Seconds) |
|---|---|
| 80H | 3 |
| 81H | 6 |
| 82H | 12 |
| 83H | 18 |
| 84H | 24 |
| 85H | 30 |
| 86H | 36 |
| 87H | 42 |

**Table 5-1 Time-Out Setting**

If you want to generate IRQ15 signal to warn your program when watchdog times out, the following table listed the relation of timer factors between time-out period. And if you use the IRQ15 signal to warn your program when watchdog timer out, please enter the BIOS Setup the <Peripheral Setup> menu, the <OnBoard PCI IDE> and <IDE Prefetch> these two items must set to ***Primary***.

| Time Factor | Time-Out Period (Seconds) |
|---|---|
| 0C0H | 3 |
| 0C1H | 6 |
| 0C2H | 12 |
| 0C3H | 18 |
| 0C4H | 24 |
| 0C5H | 30 |
| 0C6H | 36 |
| 0C7H | 42 |

**Table 5-2 Time-Out Setting**

**NOTE:** 1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.

2. Before you initial the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously, otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

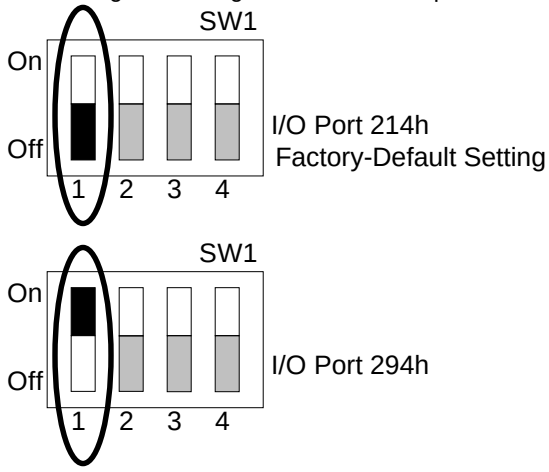



**Figure 5-1 SW1: Watchdog I/O Port Address Select**

## *5.3.2 Watchdog Timer Enabled*

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is 214H or Base Port. The following is a BASICA program, which demonstrates how to enable the watchdog timer and set the time-out period at 24 seconds.

```
1000        REM Points to command register
1010              WD_REG% = 214H
1020        REM Timer factor = 84H (or 0C4H)
1030              TIMER_FACTOR% = %H84
1040        REM Output factor to watchdog register
1050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

## *5.3.3 Watchdog Timer Trigger*

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in next trigger. Below is a BASICA program, which demonstrates how to trigger the watchdog timer:

```
2000        REM Points to command register
2010              WD_REG% = 214H
2020        REM Timer factor = 84H (or 0C4H)
2030              TIMER_FACTOR% = &H84
2040        REM Output factor to watchdog register
2050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

## *5.3.4 Watchdog Timer Disabled*

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
3000        REM Points to command register
3010              WD_REG% = BASE_PORT%
3020        REM Timer factor = 0
3030              TIMER_FACTOR% = 0
3040        REM Output factor to watchdog register
3050              OUT WD_REG%, TIMER_FACTOR%
      ., etc.
```

# 6. BIOS CONSOLE

This chapter describes the AR-B1476 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Peripheral Setup
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit
- BIOS Update

## 6.1 BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer turned on, the BIOS will perform a diagnostics of the system and will display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure the option and configure the functions.

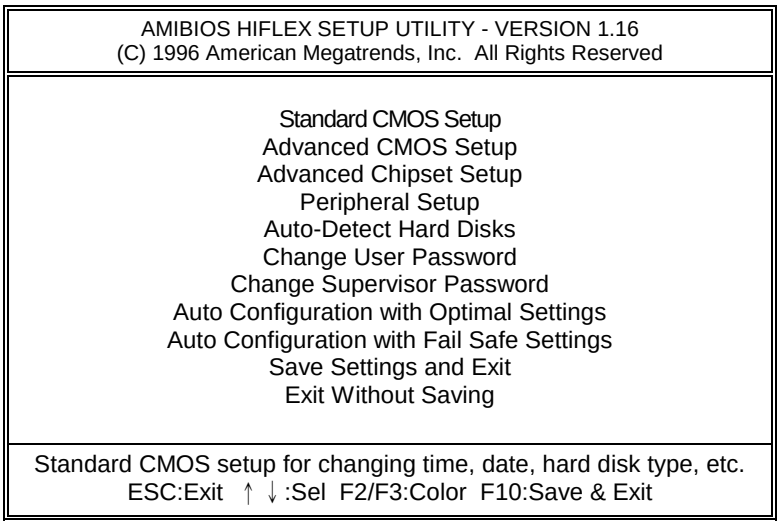



**Figure 6-1 BIOS: Setup Main Menu**

**CAUTION:** 1. AR-B1476 BIOS the factory-default setting is used to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.

2. If the BIOS loss setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section.

## 6.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

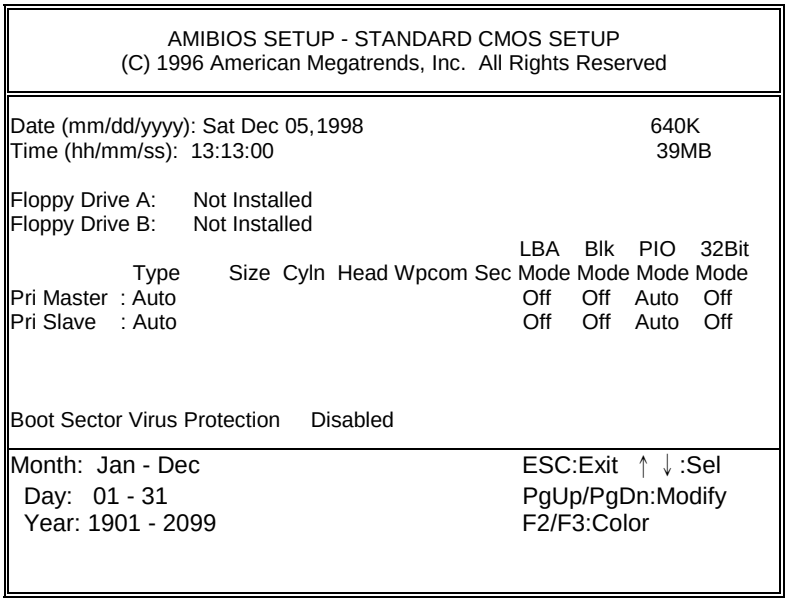



**Figure 6-2 BIOS: Standard CMOS Setup**

### Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

### Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

### Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master> and <Pri Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

### Boot Sector Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <***Disabled***>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

## 6.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board' s design to remain in their default settings.

AMIBIOS SETUP - ADVANCED CMOS SETUP
(C) 1996 American Megatrends, Inc. All Rights Reserved

| | | |
|---|---|---|
| BootUp Sequence | C:,A:,CDROM | Available Options: |
| BootUp Num-Lock | On | C:, A:. CDROM |
| Floppy Drive Swap | Disabled | A:, C:, CDROM |
| Floppy Drive Seek | Disabled | CDROM, A:, C: |
| Mouse Support | Enabled | |
| Typematic Rate | Fast | |
| System Keyboard | Present | |
| Primary Display | VGA/EGA | |
| Password Check | Setup | |
| Wait For 'F1' If Error | Enabled | |
| Hit 'DEL' Message Display | Enabled | |
| Internal Cache | WriteBack | |
| External Cache | WriteThru | |
| System BIOS Cacheable | Enabled | |
| Hard disk Delay | 3 Sec | |
| C000, 16k Shadow | Enabled | |
| C400, 16k Shadow | Enabled | |
| C800, 16k Shadow | Disabled | |
| CC00, 16k Shadow | Disabled | |
| D000, 16k Shadow | Disabled | |
| D400, 16k Shadow | Disabled | ESC:Exit ↑ ↓:Sel |
| D800, 16k Shadow | Disabled | PgUp/PgDn:Modify |
| DC00, 16k Shadow | Disabled | F2/F3:Color |

**Figure 6-3 BIOS: Advanced CMOS Setup**

### BootUp Sequence

The option determines where the system looks first for an operating system.

### BootUp Num-Lock

This item is used to activate the Num-Lock function upon system boot. If the setting is on, after a boot, the Num-Lock light is lit, and user can use the number key.

### Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the setting is <***Enabled>***, the BIOS will be swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

### Floppy Drive Seek

If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time upon boot up.

### Mouse Support

The setting of ***Enabled*** allows the system to detect a PS/2 mouse on boot up. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. ***Disabled*** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

### Typematic Rate

This item specifies the speed at which a keyboard keystroke is repeated.

### System Keyboard

This function specifies that a keyboard would be attached to the computer.

### Primary Display

The option is used to set the type of video display card installed in the system.

### Password Check

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

### Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this option is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

### Hit 'DEL' Message Display

Set this option to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

### Internal Cache

This option specifies the caching algorithm used for L1 internal cache memory. The settings are:

| Setting | Description |
|---|---|
| Disabled | Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled. |
| WriteBack | Use the write-back caching algorithm. |
| WriteThru | Use the write-through caching algorithm. |

**Table 6-1 Internal Cache Setting**

### External Cache

This option specifies the caching algorithm used for L2 secondary (external) cache memory. The settings are:

| Setting | Description |
|---|---|
| Disabled | Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled. |
| WriteBack | Use the write-back caching algorithm. |
| WriteThru | Use the write-through caching algorithm. |

**Table 6-2 External Cache Setting**

### System BIOS Cacheable

When this option is set to ***Enabled***, the contents of the F0000h system memory segment can be read from or written to L2 secondary cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are ***Enabled*** or ***Disabled***. The Optimal default setting is ***Enabled***. The Fail-Safe default setting is ***Disabled***.

### Shadow

These options control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

| SETTING | DESCRIPTION |
|---|---|
| Disabled | The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory. |
| Enabled | The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution. |
| Cached | The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory. |

**Table 6-3 Shadow Setting**

## 6.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

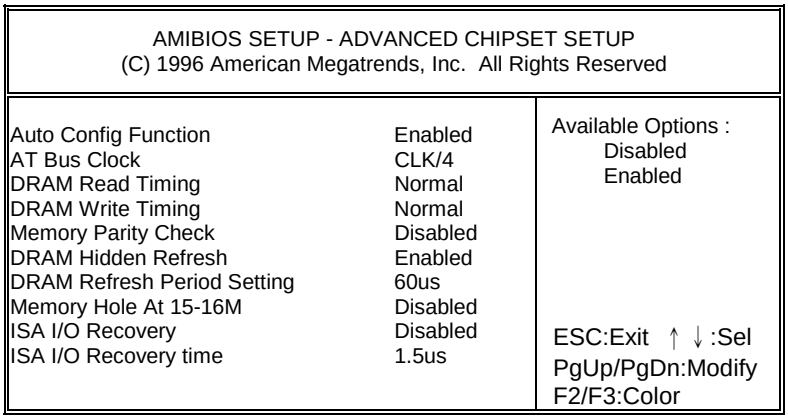



**Figure 6-4 BIOS: Advanced Chipset Setup**

### Automatic Configuration

If selecting a certain setting for one BIOS Setup option determines the settings for one or more other BIOS Setup options, the BIOS automatically assigns the dependent settings and does not permit the end user to modify these settings unless the setting for the parent option is changed. Invalid options are grayed and cannot be selected.

### AT Bus Clock

This option sets the polling clock speed of ISA Bus (PC/104).

**NOTE:** 1. PCLK means the CPU inputs clock.
2. Acrosser recommends user setting at the range of 8MHz to 10MHz.

### Memory Parity Check

This option ***Enables*** or ***Disables*** parity is error checking for all system RAM. This option must be ***Disabled*** if the used DRAM SIMMs are 32-bit but not 36-bit devices.

### Memory Hole at 15-16 M

This option specifies the range 15MB to 16MB in memory that cannot be addressed on the ISA bus.

### ISA I/O Recovery
### ISA I/O Recovery Time

These options specify the length of the delay (in BUSCLK) inserted between consecutive 8-bit/16-bit I/O operations.

## 6.5 PERIPHERAL SETUP

This section is used to configure peripheral features.

| AMIBIOS SETUP - PERIPHERAL SETUP<br>(C) 1996 American Megatrends, Inc. All Rights Reserved | | |
|---|---|---|
| OnBoard FDC | Enabled | Available Options :<br>Auto<br>Disabled<br>Enabled |
| OnBoard Serial Port1 | 3F8 | |
| OnBoard Serial Port1 IRQ | 4 | |
| OnBoard Serial Port2 | 2F8 | |
| OnBoard Serial Port2 IRQ | 3 | |
| OnBoard Parallel Port | 378 | |
| Parallel Port Mode | Normal | |
| EPP Version | N/A | |
| Parallel Port IRQ | 7 | |
| Parallel Port DMA Channel | N/A | ESC:Exit ↑ ↓:Sel<br>PgUp/PgDn:Modify<br>F2/F3:Color |
| OnBoard PCI IDE | Both | |

**Figure 6-5 BIOS: Peripheral Setup**

### OnBoard FDC

This option enables the floppy drive controller on the AR-B1476.

### OnBoard Serial Port

This option enables the serial port on the AR-B1476.

### OnBoard Parallel Port

This option enables the parallel port on the AR-B1476.

### Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.

### Parallel Port DMA Channel

This option is only available if the setting for the parallel Port Mode option is ECP.

### OnBoard PCI IDE/IDE Prefetch

This option specifies the onboard IDE controller channels that will be used.

## 6.6 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

## 6.7 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

### *6.7.1 Setting Password*

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

```
Enter new supervisor password:
```

### *6.7.2 Password Checking*

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter 1-6 character as password. The password does not appear on the screen when typed. Make sure you write it down.

## 6.8 LOAD DEFAULT SETTING

In this section permit user to select a group of setting for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

### *6.8.1 Auto Configuration with Optimal Setting*

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance settings (Y/N) ?
```

### *6.8.2 Auto Configuration with Fail Safe Setting*

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.
The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

## 6.9 BIOS EXIT

This section is used to exit the BIOS main menu in two types situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

### *6.9.1 Save Settings and Exit*

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

### *6.9.2 Exit Without Saving*

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

```
Quit without saving (Y/N) ?
```

## 6.10 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B1476 provides FLASH BIOS update function for you to easily upgrade newer BIOS version. Please follow the operating steps for updating new BIOS:

**Step 1:** Turn on your system and don't detect the CONFIG.SYS and AUTOEXEC.BAT files. Keep your system in the real mode.

**Step 2:** Insert the FLASH BIOS diskette into the floppy disk drive.

**Step 3:** In the MS-DOS mode, you can type the AMIFLASH program.

A:\>AMIFLASH

**Step 4:** The screen will show the message as follow:

Enter the BIOS File name from which Flash EPROM will be programmed. The File name must and with a <ENTER> or press <ESC> to exit.

**Step 5:** And then please enter the file name to the box of <Enter File Name>. And the box of <Message> will show the notice as follow. In the bottom of this window always show the gray statement.

Flash EPROM Programming is going to start. System will not be usable until Programming of Flash EPROM is successfully complete. In case of any error, existing Flash EPROM must be replaced by new program Flash EPROM.

**Step 6:** As the gray statement, press the <Y> key to updating the new BIOS.
And then the <Message> box will show the <Programming Flash EPROM>, and the gray statement shows <Please Wait>.

**Step 7:** The BIOS update is successful, the message will show <Flash Update Completed - Pass>.

**NOTE:** 1. After turn on the computer and the system didn't detect the boot procedure, please press the [F5] key immediately. The system will pass the CONFIG.SYS and AUTOEXEC.BAT files.

2. The BIOS Flash disk is not the standard accessory. Now the onboard BIOS is the newest BIOS, if user needs adding some functions in the future please contact technical supporting engineers, they will provide the newest BIOS for updating.

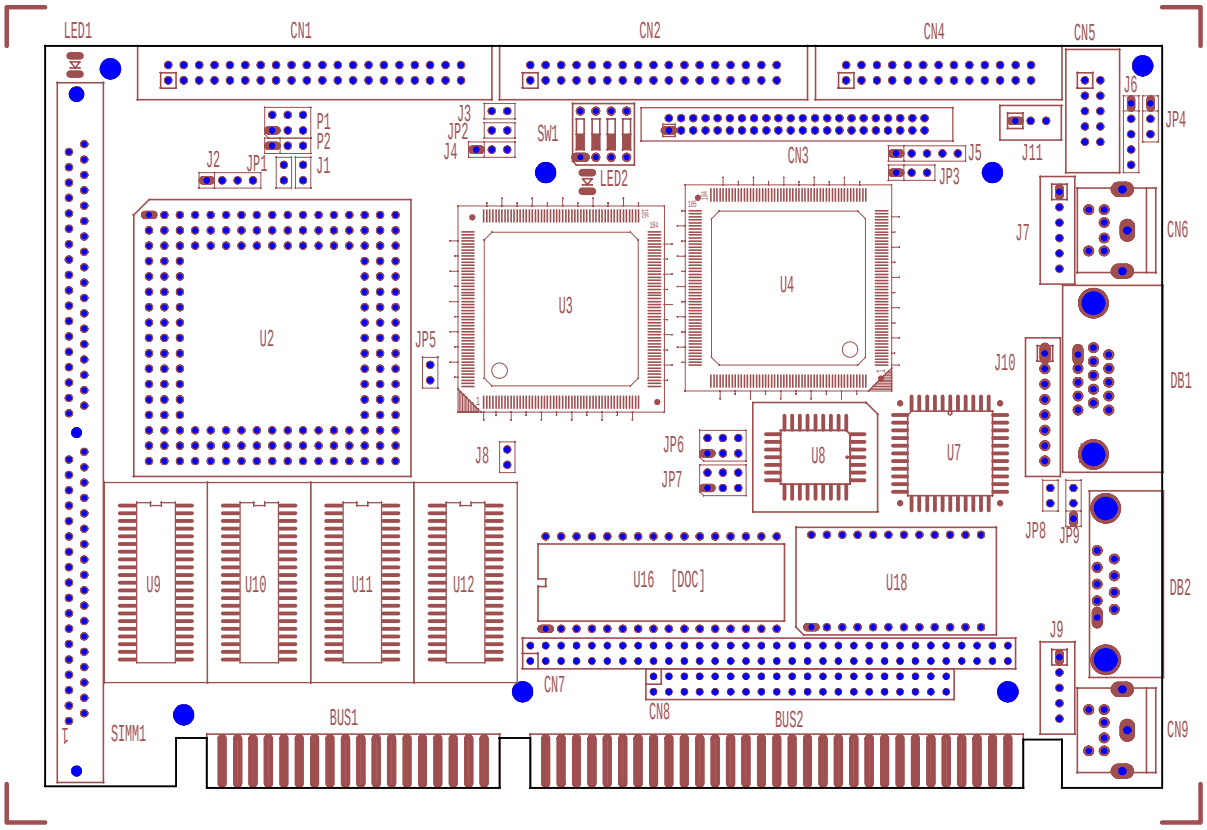
3. The file of AMIFLASH.EXE doesn't attach in the utility diskette. If user needs to update the BIOS version for some reasons please contact the technical supporting engineers, and notices the file of AMIFLASH.EXE has to use the Version 6.31.

# 7. SPECIFICATIONS

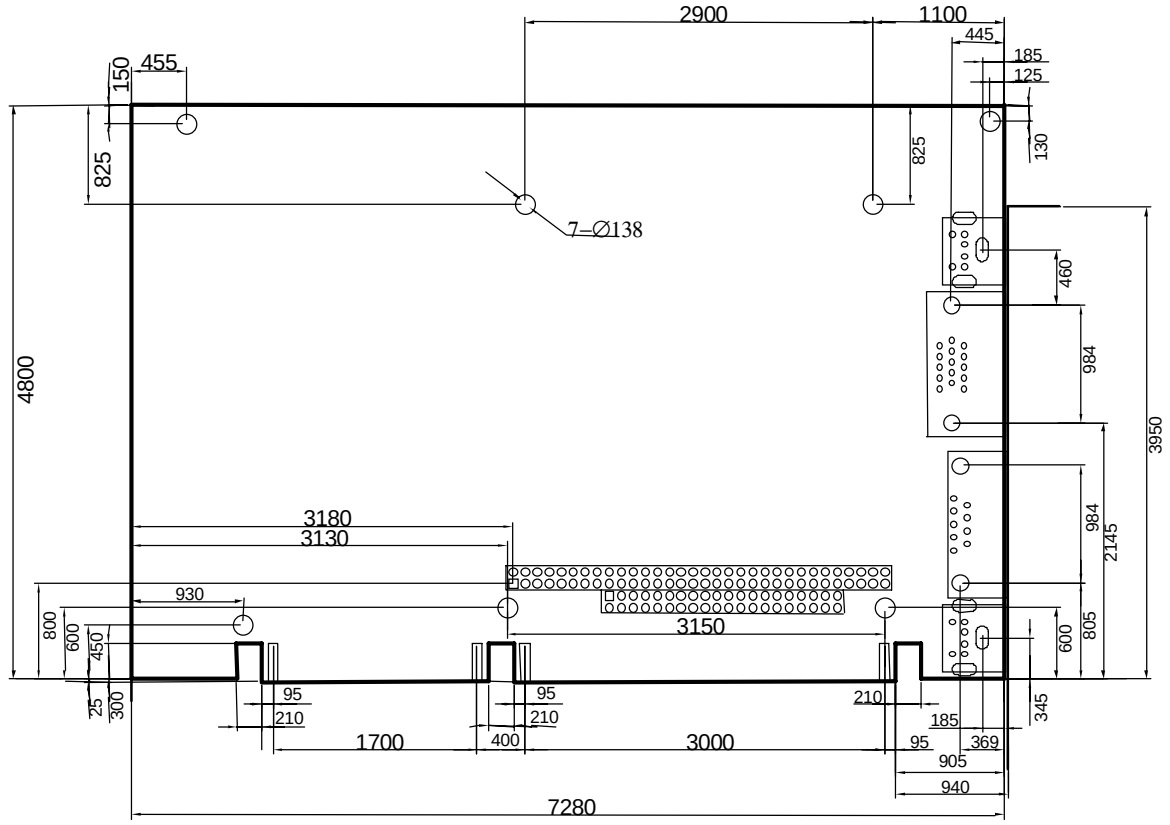
| | |
|---|---|
| **CPU:** | Supports25 to 133 Mhz Intel / AMD / Cyrix / ST / IBM 486 CPU . |
| **Chipset:** | ALI M1489/M1487 and C & T 65545 |
| **Bus Interface:** | ISA (PC/AT) and non-stack through PC/104 bus |
| **RAM Memory:** | Supports FPM/EDO RAM, 72 MB maximum (8MB on-board and one 72-pin SIMMs w/o DRAM) |
| **Cache Size:** | 512KB for standard |
| **VGA/LCD Display:** | 1 MB VRAM (PCI bus, 1024X768/256 colors) |
| **HDC:** | One PCI IDE Supports LBA/Block mode access |
| **FDC:** | Supports two 5.25" or 3.5" floppy disk drives |
| **Parallel Port:** | 1 bi-directional centronics type parallel port<br>Supports SPP/EPP/ECP mode |
| **Serial Port:** | 1 RS-232C and 1 RS-232C/RS-485 |
| **Keyboard:** | PC/AT compatible keyboard |
| **Watchdog:** | Programmable watchdog timer 3 to 42 seconds time interval |
| **Speaker:** | On-board Buzzer and external speaker |
| **Real Time Clock:** | BQ3287MT or compatible chips with 128 bytes data RAM |
| **BIOS:** | AMI Flash BIOS (128KB, including VGA BIOS) |
| **Flash Disk:** | Supports 1 DiskOnChip socket |
| **BUS Drive Cap.:** | 15 TTL level loads maximum |
| **CE Design-In:** | Add EMI components to COM ports, parallel port, CRT, keyboard, and PS/2 mouse |
| **Indicator:** | Power LED, and watchdog LED |
| **Power Req.:** | +5V only, 2.0A maximum (base on Intel DX4-100) |
| **PC Board:** | 8 layers, EMI considered |
| **Dimensions:** | 185 mmX122mm (7.29"X4.80") |

# 8. PLACEMENT & DIMENSIONS

## 8.1 PLACEMENT



## 8.2 DIMENSIONS




Unit: mil (1 inch = 25.4 mm = 1000 mil)

# 9. PROGRAMMING RS-485 & INDEX

## 9.1 PROGRAMMING RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 proceeds the transmission which needs control the TXC signal, and the installing steps are as follows:

**Step 1:** Enable TXC

**Step 2:** Send out data

**Step 3:** Waiting for data empty

**Step 4:** Disable TXC

---

**NOTE:** Please refer to the section of the "Serial Port" in the chapter "System Control" for the detail description of the COM port's register.

### (1) Initialize COM port

**Step 1:** Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

**Step 2:** Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

---

**NOTE:** Control the AR-B1476 CPU card's DTR signal to the RS-485's TXC communication.

### (2) Send out one character (Transmit)

**Step 1:** Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

**Step 2:** Send out the data. (Write this character to the offset+0 of the current COM port address)

**Step 3:** Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

**Step 4:** Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

### (3) Send out one block data (Transmit – the data more than two characters)

**Step 1:** Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

**Step 2:** Send out the data. (Write all data to the offset+0 of the current COM port address)

**Step 3:** Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

**Step 4:** Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

### (4) Receive data

The RS-485's operation of receiving data is in the same of the RS-232's.

### (5) Basic Language Example

***a.) Initial 86C450 UART***

```
10      OPEN "COM1:9600,m,8,1"AS #1 LEN=1
20      REM Reset DTR
30      OUT &H3FC, (INP(%H3FC) AND &HFA)
40      RETURN
```

***b.) Send out one character to COM1***

```
10      REM Enable transmitter by setting DTR ON
20      OUT &H3FC, (INP(&H3FC) OR &H01)
30      REM Send out one character
40      PRINT #1, OUTCHR$
50      REM Check transmitter holding register and shift register
60      IF ((INP(&H3FD) AND &H60) >0) THEN 60
70      REM Disable transmitter by resetting DTR
80      OUT &H3FC, (INP(&H3FC) AND &HEF)
90      RETURN
```

***c.) Receive one character from COM1***

```
10      REM Check COM1: receiver buffer
20      IF LOF(1)<256 THEN 70
30      REM Receiver buffer is empty
40      INPSTR$"
50      RETURN
60      REM Read one character from COM1: buffer
70      INPSTR$=INPUT$(1,#1)
80      RETURN
```

## 9.2 INDEX



Note:
If the content in Setting is inconsistent with CD-ROM. Please refer to the Setting as priority.