EXCALIBUR™

EPXA10 Development Board

Hardware Reference Manual
April 2002
Version 1.1

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About this Manual

This manual provides comprehensive information about the Altera® EPXA10 development board.

Table 1 shows the manual revision history.

Table 1. Revision History

Date	Description
March 2002	First publication as a reference document
April 2002	Change the product codes from EPXA10F1020Cx to EPXA10F1020C2

How to Find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Click on the binoculars icon in the top toolbar to open the Find dialog box.
- Bookmarks serve as an additional table of contents.
- Thumbnail icons, which provide miniature previews of each page, provide a link to the pages.
- Numerous links, shown in green text, allow you to jump to related information.

How to Contact Altera

For the most up-to-date information about Altera products, go to the Altera world-wide web site at http://www.altera.com.

For additional information about Altera products, consult the sources shown in Table 2.

Table 2. How to Contact Altera

Information Type	Access	USA & Canada	All Other Locations
Altera Literature Services	Electronic mail	lit_req@altera.com *(1)*	lit_req@altera.com *(1)*
Non-technical customer service	Telephone hotline	(800) SOS-EPLD	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time)
	Fax	(408) 544-7606	(408) 544-7606
Technical support	Telephone hotline	(800) 800-EPLD (7:00 a.m. to 5:00 p.m. Pacific Time)	(408) 544-7000 *(1)* (7:30 a.m. to 5:30 p.m. Pacific Time)
	Fax	(408) 544-6401	(408) 544-6401 *(1)*
	World-wide web site	http://www.altera.com/mysupport	http://www.altera.com/mysupport
	FTP site	ftp.altera.com	ftp.altera.com
General product information	Telephone	(408) 544-7104	(408) 544-7104 *(1)*
	World-wide web site	http://www.altera.com	http://www.altera.com

Note:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The *EPXA10 Development Board Hardware Reference Manual* uses the typographic conventions shown in Table 3.

Table 3. Conventions

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\QuartusII** directory, **d:** drive, **chiptrip.gdf** file.
Bold italic type	Book titles are shown in bold italic type with initial capital letters. Example: ***1999 Device Data Book***.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75 (High-Speed Board Design).*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <*file name*>, <*project name*>**.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of Quartus II Help topics are shown in quotation marks. Example: "Configuring a FLEX 10K or FLEX 8000 Device with the BitBlaster™ Download Cable."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `_n`, e.g., `reset_n`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\quartusII\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c.,...	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Notes:

Contents

EPXA10 Development Board

Hardware Reference Manual

Features

- Powerful development board for embedded processor PLD designs
  - Features an EPXA10F1020C2 device
  - Supports intellectual property-based (IP-based) designs using a microprocessor
- Industry-standard interconnections
  - 10/100 megabits per second (Mbps) Ethernet with full and half duplexing
  - Two 3.3-V, 32-bit peripheral component interconnect (PCI) connectors

    These features require additional IP blocks; contact Altera for further details.

  - Two RS-232 ports (data terminal equipment (DTE))
- Memory subsystem
  - 16-Mbyte flash memory
  - Up to 512-Mbyte single data rate (SDR) SDRAM in a DIMM socket
- Multiple clocks for communications system design
- Multiple ports for configuration and debugging
  - IEEE Std. 1149.1 Joint Test Action Group (JTAG)
  - Support for configuring the EPXA10 device using flash memory, an EPC2, or a MasterBlaster™ or ByteBlasterMV™ cable
- Expansion headers for greater flexibility and capacity
  - Four expansion headers for daughter-card access
  - 3.3-V/5-V/12-V/–12-V expansion/prototype headers to support up to 502 user I/O pins
- Additional user-interface features
  - One user-definable 9-bit dual in-line package (DIP) switch block
  - Four user-definable push-button switches
  - Eight user-definable LEDs
- Test points and logic analyzer connectors provided to facilitate system development
- Trace port connections

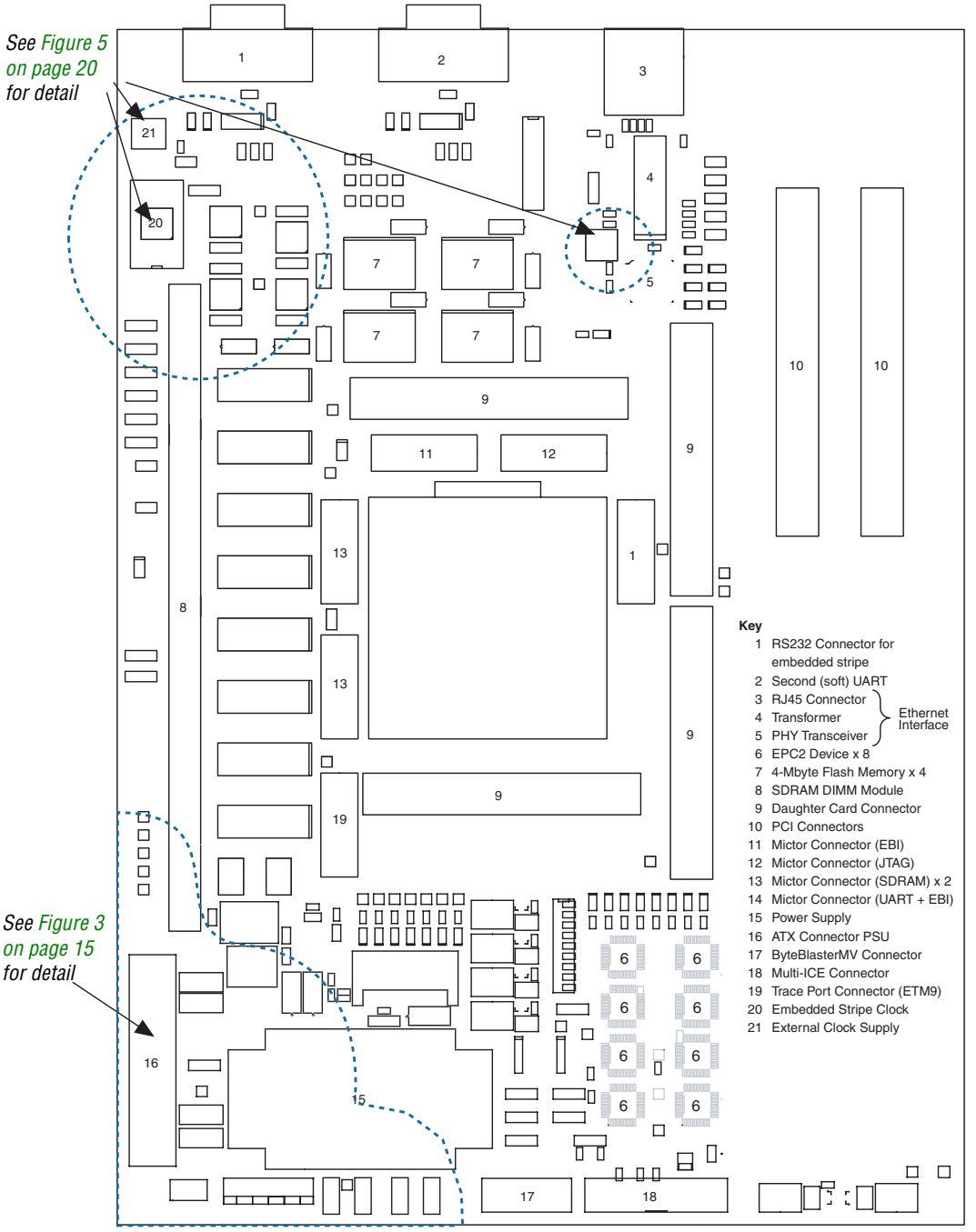
General Description

Designers can use the EPXA10 development board as a desktop development system. It provides a hardware platform to start developing embedded systems immediately; and delivers clocks, debugging, and trace facilities to support the system under development in an ARM®-based EPXA10 embedded processor PLD.

The EPXA10 development board provides a flexible, powerful debug and development environment. Designers can use the board for a variety of purposes, including building and emulating systems for special requirements, and conducting trace and debug investigations.

Figure 1 on page 11 shows a layout diagram of the EPXA10 development board.

Figure 1. EPXA10 Development Board Layout



EPXA10 Embedded Processor PLD

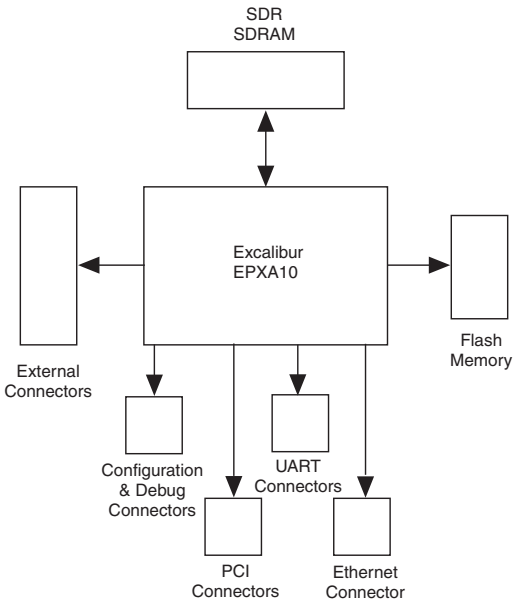
The EPXA10F1020C2 embedded processor PLD features 1,000,000 ASIC-equivalent gates in a 1,020-pin FineLine BGA™ package with 38,400 logic elements and 327,680 ESB RAM bits. Contained in the embedded processor stripe is the ARM922T™ 32-bit RISC microprocessor, a further 3 Mbits of RAM, and the following features:

- SDRAM controller
- System bus bridges
- Reset controller
- Interrupt controller
- Expansion bus interface (EBI)
- ETM9 trace module
- UART
- System status and control registers
- Timers

Refer to the *ARM-Based Embedded Processor PLDs Hardware Reference Manual* for details about the EPXA10 device.

Figure 2 illustrates the relationship between the EPXA10 device and the motherboard peripherals.

Figure 2. EPXA10 Development Board Block Diagram



Board Profile

The development board comprises 14 layers, which are used as follows:

- 10 signal layers
- Full 3.3-V power plane
- 2 ground layers
- Analog ground layer

The board dimensions are 11.5″ × 8″.

Power Supply

The board includes connectors that support both laboratory bench power supplies and commercially-available, PC-style power supplies (ATX). A status LED is provided for each power supply. If you are not using devices attached to the PCI connectors, only the 3.3-V supply is necessary, but to use devices on the PCI connectors, you need an ATX power supply to provide the different voltages.

An ATX supply provides voltage levels of ±12 V, ±5 V, and +3.3 V to the development board, from which it derives the V_{REF}, +2.5 V, and +1.8 V supplies.

Ensure that the voltage setting on the ATX power supply is set to the appropriate voltage based on what your AC power outlet provides.

For a bench supply with connectors, connect only GND and 3.3 V. 1.8 V and 2.5 V are outputs from the board, and should not be connected.

Tables 1 through 4 list the estimated power requirements for the development board.

Table 1. ±12.0-V Supply Requirements

Module	mA (12 V)	mA (–12 V)
PCIs	500	100

Table 2. 5.0-V Supply Requirements

Module	A (5 V)
PCI	Depends on system
CLK_REF	Alternative crystal oscillator

Table 3. 3.3-V Supply Requirements

Module	mA (3.3 V)
EPXA10 I/O *(1)*	Depends on application
SDRAM DIMM module	500
Flash memory	300
PCIs	7.6A (system-dependent)
UARTs	50
Ethernet	-
LEDs	20 × 22
EPC2	50 × 8
Crystal oscillator	15 × 5
Power-on reset	10
Clock buffers	32 × 2

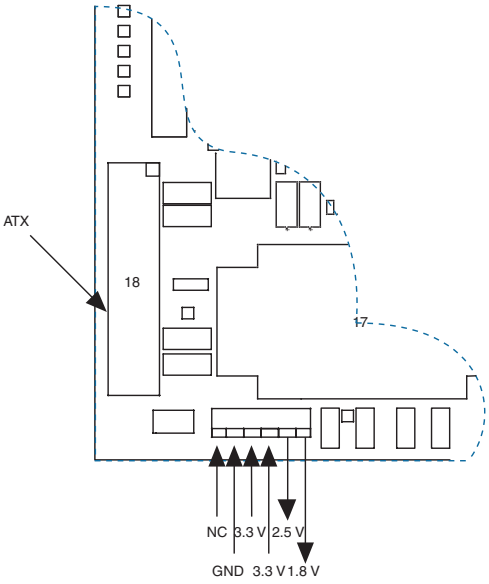
Note:
(1) Jumpers JP58 and JP59 must be set to 3.3 V

Table 4. 1.8-V Supply Requirements

Module	mA (1.8 V)
EPXA10 device core	Depends on application

Figure 3 on page 15 shows the location of the power supply inputs for the EPXA10 development board.

Figure 3. EPXA10 Power Supply Inputs



See Figure 1 on page 11 to locate this subsection on the development board.

Environmental Requirements

The development board must be stored between –40 °C and 100 °C.

Operating Requirements

Operating temperatures must fall between 0 °C and 55 °C. The development board uses commercial grade components and must be convection-cooled.

Anti-static Handling

Before handling the card, you should take proper anti-static precautions, otherwise the board might be damaged.

Clocks

The EPXA10 embedded processor stripe has one clock input, which can be driven from one of three sources as follows:

- A dedicated on-board crystal oscillator
- An alternative crystal oscillator
- A waveform generator using a BNC connector

The EPXA10 PLD has four clock inputs, all using 32-MHz on-board crystal oscillators.

Memory

The EPXA10 development board has the following memory:

- Up to 512 Mbytes 32-bit SDR SDRAM (optional) can be connected via the DIMM socket. The SDRAM interface on the EPXA10 development board is limited to 75 MHz operation
- 16 Mbyte 16-bit flash memory (4 × 4-Mbyte blocks)

Development Board Expansion

The EPXA10 development board supports the EPXA10 device and simultaneously supports flexible expansion:

- Four expansion headers allow the connection of daughter boards
- Two PCI connectors accommodate 3.3-V and universal PCI expansion cards

Interfaces

Table 5 describes the interfaces supported by the board.

Table 5. Development Board Interfaces (Part 1 of 2)

Interface	Description
PCI connectors	The connectors operate at 32-bit, 33 MHz and can be used by designers to connect standard, commercially-available 3.3-V and universal PCI cards
10/100 Ethernet with full- and half-duplexing	This interface consists of a connector, transceiver and transformer. The MAC is implemented in the Altera device as an IP block. The connection between the MAC and the transceiver is a standard MII
Expansion headers	These connectors allow designers to stack multiple daughter boards as required

Table 5. Development Board Interfaces (Part 2 of 2)	
Interface	**Description**
User I/O pins	The expansion header provides up to 502 user I/O pins that connect directly to the EPXA10 device, supporting custom interfaces
IEEE Std. 488 RS-232 serial interfaces	This interface is a 12.0-V transceiver with 235-kbps data rate in a TSSOP package
Debugging/programming ports	The board supports in-circuit debugging by means of the MasterBlaster, ByteBlasterMV, or Multi-ICE cables
MICTOR connectors	This connector provides debugging and monitoring facilities for the UART, EBI, SDRAM, Trace and JTAG

General Information

When power is initially applied to the board, the LEDs flash according to the software test running on the embedded processor. The test suite is programmed directly into flash memory, and when the embedded processor boots it configures the PLD and runs the software using the test PLD image.

Functional Overview

This section gives a brief overview of the EPXA10 development board components. Figure 2 on page 12 shows a functional block diagram of the development board.

EPXA10F1020C2 Device

The main component of the development board is the EPXA10F1020C2 device in a 1,020-pin FineLine BGA package. Table 6 lists the features of the EPXA10 device.

Table 6. EPXA10 Device Features	
Feature	**Capacity**
Maximum system gates	1,772,000
Typical gates	1,000,000
LEs	38,400
ESBs	160
Maximum RAM bits	327,680
Maximum macrocells	2,560
Maximum user I/O pins	708

In addition, the EPXA10 device provides a variety of on- and off-chip peripherals, as listed in Table 7.

Table 7. EPXA10 On- and Off-Chip Peripherals

Peripheral	Description
ARM922T 32-bit RISC processor	For speed grade –1: up to 200 MHz For speed grade –2: up to 166 MHz
ETM9 trace module	Used for software debugging
Interrupt controller	Used for the interrupt system
Internal single-port SRAM	256 Kbytes
Internal dual-port SRAM	128 Kbytes
SDRAM controller	Interfaces between the internal system bus and SDRAM
External SDRAM	Up to 512 Mbytes, 75 MHz
EBI	Interfaces to 16 Mbyte flash memory
External flash memory	Up to 32 Mbytes
Watchdog timer	Protects the system against software failure

For more information about the EPXA10 or other ARM-based embedded processor devices, see the *ARM-Based Embedded Processor PLDs Hardware Reference Manual*

Memory Interfaces

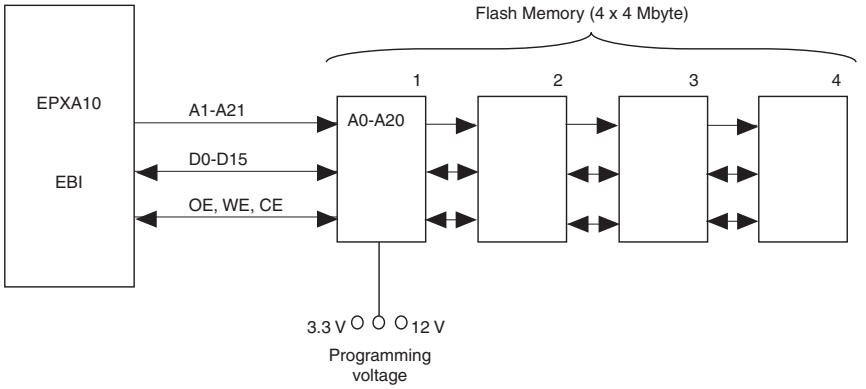
The EPXA10 development board provides on-board memory of the following types and capacities, as listed in Table 8.

Table 8. Development Board Memory Characteristics

Type	Address Lines	Data Lines	Control Lines	Memory Organization	Size
SDR SDRAM	15	32	16	DIMM	Up to 512 Mbytes
Flash	25	16	6	4 × 4 Mbytes	16 Mbyte

Four flash memory chips are connected to the EBI of the EPXA10 development board, to maximize the amount of storage available for the software application. Figure 4 shows this arrangement diagrammatically.

Figure 4. Flash Memory Interface



The EPXA10 development board can be used equally well with either Intel or the AMD flash memory.

Clock Generation & Distribution

There are five clock generators on the EPXA10 development board, connected to crystal oscillators that can be enabled and disabled according to your design requirements. Optionally, the Ethernet clock can be used to drive two of the PLD clocks. The reference clock for the embedded processor stripe (CLK_REF) uses a zero-delay clock buffer to allow a 3.3-V to 5-V interface as well as buffering the clock signal. Refer to "Jumper Configuration" on page 35 for more about configuring the clock options on the development board.

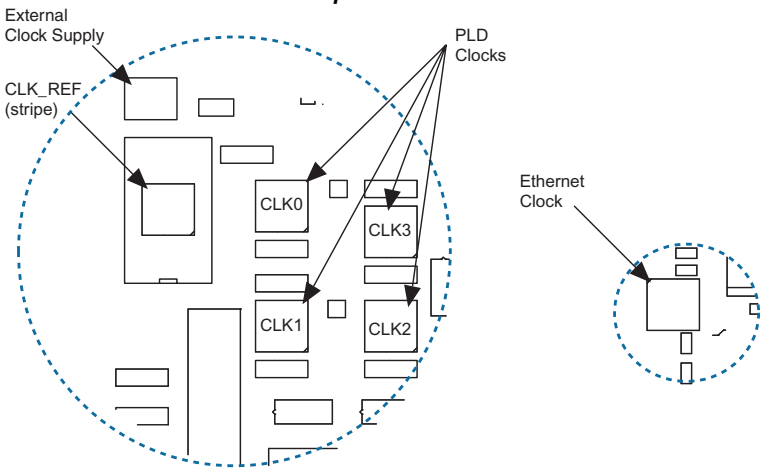
The devices configured on the EPXA10 development board determine which clocks are required. Table 9 gives a comprehensive list of the clocks, assuming that all devices are used.

Table 9. Clock Requirements

Clock	Used In	Speed
CLK_REF	EPXA10 stripe	50 MHz
CLK0	PLD	32.768 MHz
CLK1	PLD	32.768 MHz/tx_clk1
CLK2	PLD	32.768 MHz/rx_clk1
CLK3	PLD	32.768 MHz
CLKIN	Ethernet	25 MHz

Figure 5 on page 20 shows the location of the clocks.

Figure 5. Clock Generators on the EPXA10 Development Board



See Figure 1 on page 11 to locate this subsection on the development board.

Configuration Interfaces

There are two methods of configuring and programming the EPXA10 device:

- Using the flash memory programmer
- Using the Quartus® II software

Using the Flash Memory Programmer

The Altera flash memory programmer (**exc_flash_programmer.exe**) is a utility that allows users to program flash memory on the EBI using the JTAG interface.

With the flash memory programmer, you can program the EPXA10 development board's flash memory with the required hardware and software image. When this phase has finished, the processor boots up and configures the PLD side of the EPXA10, and then loads the PLD with the appropriate software application.

Table 10 shows the board jumper requirements for booting from flash memory; see "Jumper Configuration" on page 35 for more details.

Table 10. Board Configuration for Booting from Flash Memory

BOOT_FLASH	MSEL0	MSEL1	Mode
1 (position 2-3)	0 (position 1-2)	0 (position 1-2)	Boot from 16-bit flash

For further details about booting the device from flash memory, refer to the *ARM-Based Embedded Processor PLDs Hardware Reference Manual*.

Using the Quartus II Software

The Quartus II software can generate a programmer object file (.**pof**) containing both hardware and software, for downloading into the eight EPC2 devices available on the EPXA10 development board. For more details about the EPC2 devices, see "EPC2 Device Configuration" on page 22.

Six of the EPC2 devices are dedicated to the PLD hardware image. The remainder are used for the software image and can be bypassed using jumper JP57. To boot your system from the EPC2 devices, you must configure the EPXA10 development board as defined in Table 11 on page 21.

Table 11. Board Configuration for Booting from a Serial Device

BOOT_FLASH	MSEL0	MSEL1	Mode
0 (position 1-2)	0 (position 1-2)	0 (position 1-2)	Serial

Table 46 on page 58 provides a list of configuration signals. When power is applied to the development board, the EPC2 configuration devices load configuration data into the EPXA10 device, if they have been programmed. If you change the configuration device's programming information, you must turn the board off and on before new information can be loaded into the EPXA10 device.

The EPC2 devices can be programmed through the JTAG interface; see "JTAG Programming Chain" on page 41. The EPC2 device can be programmed with the Quartus II software version 1.1 or higher, using either the MasterBlaster or ByteBlasterMV download cables.

To configure the device using the EPC2 devices, start the Quartus II software, and specify the EPC2 device as an output option to create the required .**pof** files. If the EPC2 devices are not specified, the Quartus II software generates a single file to program the EPXA10 device directly.

Configuration Interfaces

Table 12 shows the data sources for configuration that are available for the EPXA10 device.

Table 12. Supported Configuration Schemes

Configuration Scheme	Data Source
Configuration devices	EPC2 configuration device
JTAG	MasterBlaster/ByteBlasterMV download cable

EPC2 Device Configuration

The EPC2 device section consists of eight EPC2 devices, which are a part of the on-board JTAG chain, to allow in-system programming.

The EPC2 devices contain reprogrammable flash memory to configure the embedded-processor PLD serially. For more details about configuring these devices, refer to the data sheet *Configuration Devices for ACEX, APEX, FLEX & Mercury Devices*.

MasterBlaster/ByteBlasterMV Communications Cable

These cables have a 10-pin header for use with the development board. The cable allows you to download hardware and software configuration data directly to the EPXA10 device or to the EPC2 configuration devices. The development board supports only JTAG download mode, not passive serial download mode. The MasterBlaster and ByteBlasterMV cables also support in-circuit debugging with the SignalTap® embedded logic analyzer.

Two green LEDs are provided on the MasterBlaster cable: one for use with the `CONF_DONE` signal and one for use with the `nSTATUS` signal.

The board header supply voltage is 3.3 V.

The MasterBlaster cable can also be used in conjunction with the ARM debugger to debug your software using JTAG.

Serial I/O Interfaces

The development board contains two RS-232 DTE interfaces. For each, the transceiver and any associated hardware are provided on the board.

Table 13 provides information on the devices used to implement the RS-232 interfaces.

Table 13. RS-232 Interface Device Reference

Reference	Part Number	Manufacturer	Website Address	Description
U35	MAX3241	Maxim	www.maxim-ic.com	RS-232 DTE transceiver (connects to the UART in the stripe using connector P1)
U38	MAX3241	Maxim	www.maxim-ic.com	RS-232 DTE transceiver (connects to the soft UART in the PLD using connector P2)

The transceiver requires a 3.3-V power supply. If the RS-232 input pins are used as outputs, contention occurs because the bus transceiver is always active. If these pins are not used as part of a design, ensure that they remain in the high-impedance state. See Table 33 on page 45 for information on the RS-232 DTE signals.

DTE UART Interface

The EPXA10 device includes a UART core which is directly connected to a device to provide the RS-232 interface levels. A second UART is provided, which is connected to 3.3-V standard EPXA10 I/O. Table 14 shows the DTE UART interface characteristics.

Table 14. DTE UART Interface Characteristics

Features	I/O Pins	Voltage
UART 1 TX, RX & Control	7	3.3 V
UART 2 TX, RX & Control	7	3.3 V

Table 17 lists the UART LEDs on the EPXA10 development board.

Table 15. UART LEDs (Part 1 of 2)

LED Reference	Description
TX_UART1	This blinks to indicate activity on the line
RX_UART1	This blinks to indicate activity on the line
TX_UART2	This blinks to indicate activity on the line

Table 15. UART LEDs (Part 2 of 2)

LED Reference	Description
RX_UART2	This is set on to indicate activity on the line
CONF_DONE	This is set on to indicate that PLD configuration is complete

10/100 Ethernet Parallel Interface

The Ethernet interface consists of a transceiver, or PHY layer, and associated discrete components. You can use the interface to implement an Ethernet media access controller (MAC) in the EPXA10 device. As shown in Table 34 on page 46, the connections consist of the standard media-independent interface (MII) and additional signals. Table 16 provides information on the devices used to implement the Ethernet interface.

Table 16. Ethernet Interface Device Reference

Reference	Part Number	Manufacturer	Website Address	Description
U176	78Q2120-64CGT (TQFP64)	TDK	www.tdk.com	Fast Ethernet MII transceiver
U177	PE-68515L	Pulse	www.pulseeng.com	10/100-BASE T single-port transformer module
U178	AMP 555078-1	AMP	www.amp.com	8-pin PCB RJ45 data socket

Table 17 lists the LEDs used for the Ethernet on the EPXA10 development board.

Table 17. Ethernet LEDs

LED Reference	Description
LEDL	Link LED. This is set on during linkup
LEDTX	Transmit LED. This is set on during transmission
LEDRX	Receive LED. This is set on during receipt
LEDFDX	Full-duplex LED. This set on for full-duplex mode and off for half-duplex
LEDCOL	Collision LED. This is set on in half-duplex mode when a collision occurs, and is held off in full-duplex mode
LEDBTX	100-BASE TX LED. This is set on for 100-BASE T connection, but off otherwise
LEDBT	10-BASE T LED. This is set on for 10-BASE T connection, but is off otherwise

Ethernet Switches

Table 18 lists the switches used for the Ethernet device in the S2 switch bank; and Table 19 shows how the TECH switches are used to set the Ethernet decoding protocol.

Table 18. S2 Switches for PHY

Identifier	Switch	Dip-Switch for Ethernet PHY
ANEGA	1	Auto-negotiation enable
TECH0	2	Used to specify the Ethernet decoding
TECH1	3	
TECH2	4	
PHYAD0	5	Physical Address
PHYAD1	6	
PHYAD2	7	
PHYAD3	8	
PHYAD4	9	

Table 19. Ethernet Protocol Decoding

TECH [2:0]			Function
0	0	0	Advertise no technology capability
1	1	1	Both 10-BASE T and 100-BASE T
0	0	1	10-BASE T, half duplex
0	1	0	100-BASE T, half duplex
0	1	1	Both 10-BASE T and 100-BASE T, half duplex
1	0	0	None
1	0	1	10-BASE T, full/half duplex
1	1	0	100-BASE T, full/half duplex

PCI Interface

Two PCI slots are implemented on the board. The 32-bit interface is capable of 33 MHz and operates at 3.3 V; it complies with *PCI Local Bus Specification, Revision 2.2*. The slots can be used with 3.3-V and universal PCI cards.

User I/O pins are provided for this interface. Table 37 on page 49 lists the PCI signal pin assignments.

EPXA10 Device Signal Definitions for the PCI Card

Table 20 shows the definitions for the EPXA10 device signals required to implement the PCI interface.

Table 20. EPXA10 Device Signal Definitions

Function	Signals	Number
Address and data	AD[31..0] C/BE[3..0]# PAR	37
Interface control	FRAME# TRDY# IRDY# STOP# DEVSEL# LOCK#	6
Error reporting	PERR# SERR#	2
Arbitration	PRSNT1# PRSNT2# REQ1# REQ2# GNT1# GNT2#	6
Interrupts	INTA# INTB# INTC# INTD#	4
System	CLK2 PCI_RST#	2

Some signals are not included in Table 20. IDSEL is a PCI signal used as a device select for configuration cycles and is generally connected to one of the address lines. Table 21 lists the IDSEL signal connections.

Table 21. IDSEL Signal Connections

Board Connector	PCI Slot	EPXA10 Board Reference
U23	1	AD16
U24	2	AD17

Board-Level Issues

The PCI interface requires no devices on the board level if the PCI is implemented as an IP core in the EPXA10 device. All of the power supplies are provided when the ATX power supply is connected on the EPXA10 development board.

Table 22 lists the PCI interface characteristics.

Table 22. PCI Interface Characteristics

Interface Features	I/O Pins	Voltages	Clocks
PCI Interface	55 plus clock	+3.3 V, +5 V, ±12 V	33 MHz

Expansion Headers

Four expansion headers are provided on the EPXA10 development board. The expansion headers are implemented using SAMTEC TOLC 200-pin connectors, as listed in Table 23 on page 27. They are connected to I/O pins on the EPXA10 device. Each header includes +5-V, +3.3-V, ±12-V, and ground signals, as well as I/O signals.

Table 23 provides information on the devices used to implement the expansion header interface.

Table 23. Expansion Header Interface Device Reference

Reference	Part Number	Manufacturer	Website Address	Description
U123	SAMTEC TOLC-150-32-F-Q	Samtec	www.samtec.com	Connector to expansion card
U124				
U125				
U126				

Note:
(1) Altera recommends that you use Samtec SOLC-150-02-F-Q for the daughter board connectors.

Table 24 lists the expansion header interface characteristics.

Table 24. Expansion Header Interface Characteristics

Interface Features	I/O Pins	Signalling Voltage	Clocks	Voltages
Expansion header interface	501	±3.3 V	33 MHz	+3.3 V, +5 V, ±12 V

All LEDs, switches and push buttons are accessible from the expansion headers.

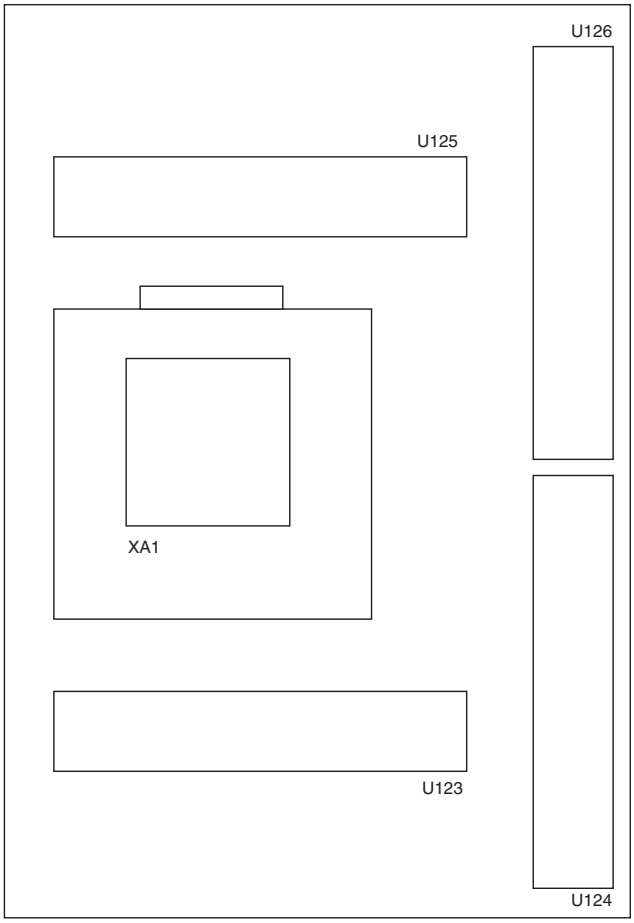
Users can design expansion cards to their specific requirements using the I/O pins on the EPXA10 device and power supplies from the EPXA10 development board.

The connectors are stackable, so more than one card can be plugged on each header, allowing users to develop different cards for individual modules within a complex design.

Refer to Figures 6 to 9 for mechanical drawings of the board expansion headers and Tables 54 through 56 for EPXA10 pin details and their connections on the expansion headers.

Figure 6 on page 29 shows the location of the expansion headers on the EPXA10 development board.

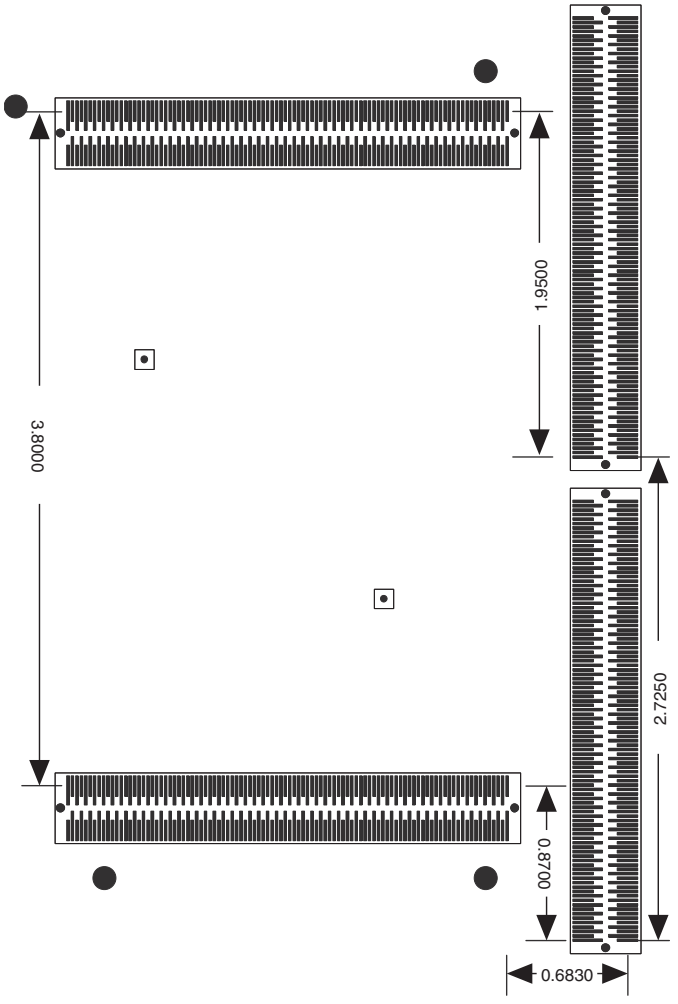
Figure 6. EPXA10 Development Board TOLC Expansion Header Connections



The dimensions given in Figures 7 to 9 are inches, measured from the centre of the pad.

Figure 7 on page 30 gives dimensions for the TOLC expansion headers categorized in Table 23 on page 27.

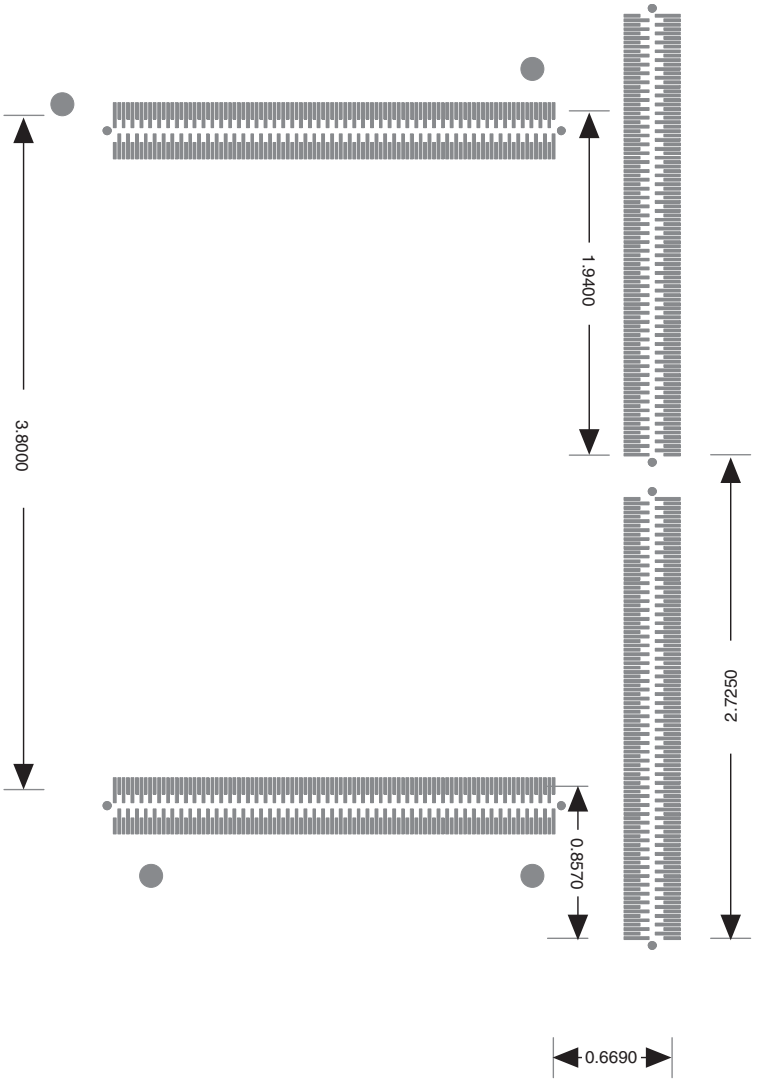
Figure 7. EPXA10 Development Board TOLC Dimensions



All dimensions are in inches.

To connect to the motherboard, a daughter board must use SOLC connectors, for which dimensions are given in Figure 8 on page 31.

Figure 8. Daughter Board SOLC Dimensions

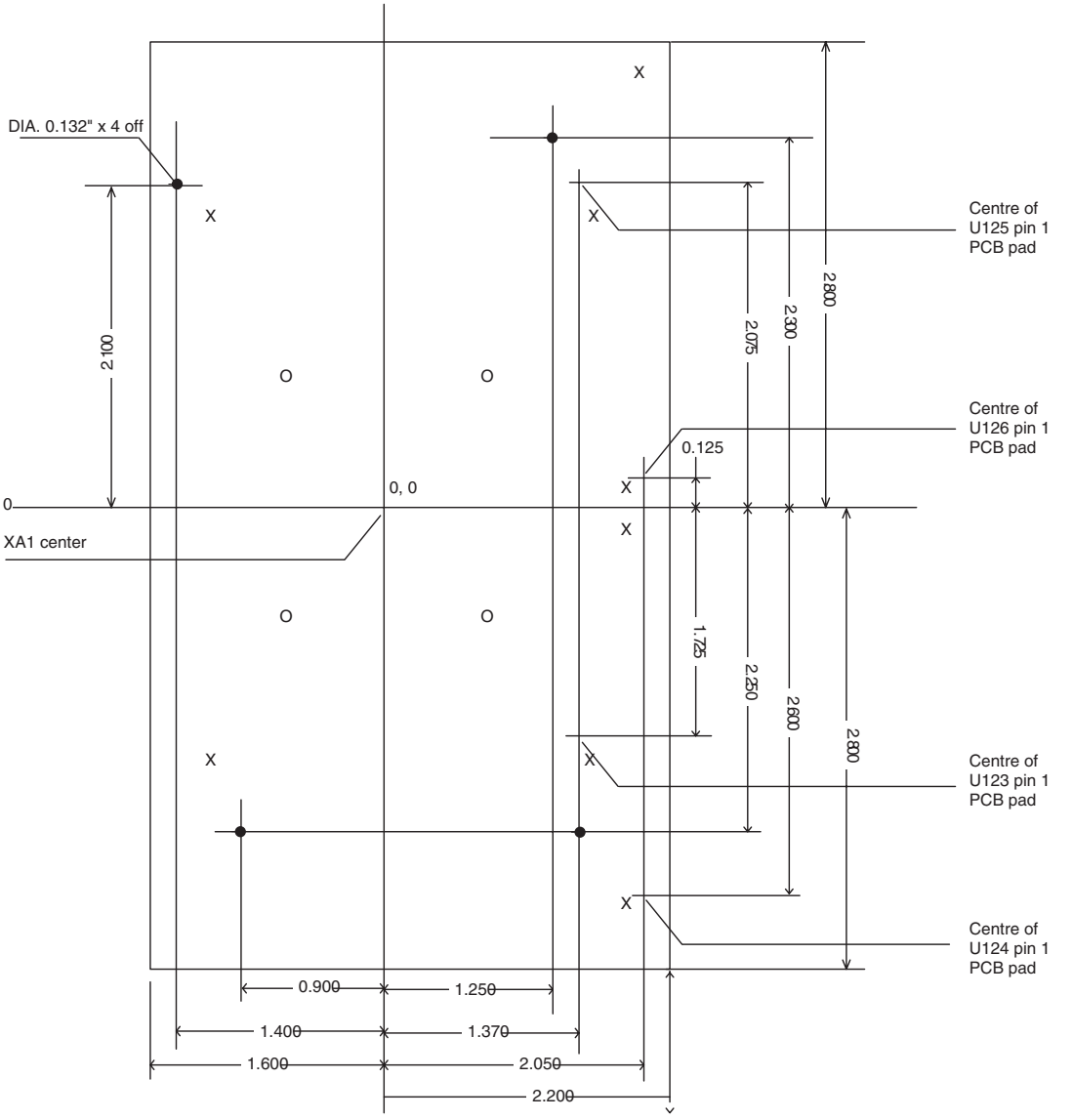


All dimensions are in inches.

Figure 9 on page 32 is a mechanical diagram giving the position of the TOLC connectors on the motherboard layout.

The PCB footprints for TOLC and SOLC connectors differ.

Figure 9. Mechanical Diagram of the EPXA10 Development Board Expansion Headers



All dimensions are in inches.

To design a matching daughter board, designers must do one of the following:

- Base designs on the SOLC expansion header dimensions given in Figure 8 on page 31
- Translate dimensions from the TOLC motherboard dimensions

LED & Switch Interfaces

The EPXA10 development board provides a variety of LED and switch interfaces.

LED Interface

The development board has eight LEDs that are used for application-specific functions on the EPXA10 device. Table 54 on page 63 provides more information on EPXA10 device pins connected to LEDs.

User-Defined LEDs

The EPXA10 development board provides eight user-definable LEDs, which connect directly to the EPXA10 device I/O pins. The LEDs can be used for any kind of application.

Table 25 lists the interface characteristics for the user-defined LED interfaces.

Table 25. LED Interface Characteristics

Feature	Board Name	I/O Pins	Voltage
USER_LED7	U94	T6	3.3 V
USER_LED6	U95	U7	3.3 V
USER_LED5	U96	V8	3.3 V
USER_LED4	U97	V7	3.3 V
USER_LED3	U98	U6	3.3 V
USER_LED2	U99	V5	3.3 V
USER_LED1	U100	U5	3.3 V
USER_LED0	U101	V6	3.3 V

LEDs are also used for specific application functions, such as the configuration, RS-232 and Ethernet interfaces. Table 26 on page 34 lists the application-specific LEDs, their power supply status, and their functions.

Table 26. Application LED Usage

LED Reference	Description
–5V	–5-V power supply indicator
5V	5-V power supply indicator
2.5V	2.5-V power supply indicator
12V	12-V power supply indicator
3.3V	3.3-V power supply indicator
–12V	–12-V power supply indicator
1.8V	1.8-V power supply indicator
LEDL	LED link. This is set on during linkup
LEDTX	LED transmit. This is set on during transmission
LEDRX	LED receive. This is set on during receipt
LEDFDX	LED full duplex. This is set on for full duplex and held off for half duplex
LEDCOL	LED collision. This is set on in half-duplex mode when a collision occurs, and held off in full-duplex mode
LEDBTX	LED 100-BASE TX. This is set on for 100-BASE T connection, and is otherwise held off
LEDBT	LED 10-BASE T. This is set on for 10-BASE T connection, and is otherwise held off
TX_UART1	This blinks to indicate activity on the line
RX_UART1	This blinks to indicate activity on the line
TX_UART2	This blinks to indicate activity on the line
RX_UART2	This is set on to indicate activity on the line
CONF_DONE	This LED is connected to the `INIT_DONE` pin of the EPXA10 device. When `INIT_DONE` is enabled for the design in Quartus II, the `CONF_DONE` LED indicates that the PLD has been configured and is now in user mode

Switch Interfaces

In addition to the dip-switches used for the Ethernet interface, which are listed in Table 18 on page 25, the EPXA10 development board provides nine user-definable switches in another dip-switch block, four push-button switches, and two dedicated reset switches.

The push-button switches and integrated LEDs are connected to the EPXA10 I/O pins. Tables 27 and 28 detail the push-button switches.

Table 27. Push-Button Switches

Push Button Reference	Use	Connected To
SW_RESET	Generates a warm reset	nCONFIG
SW_DEV_CLR_N	Resets the PLD	DEV_CLR_n
SW6	Generates an interrupt on the EBI interface when enabled by the interrupt controller; otherwise connected to user-defined I/O	U10 and G25

Table 28. User-Definable Push-Button Switches

Push Button Reference	I/O Pins	Voltage
SW3	T8	3.3 V
SW4	R5	3.3 V
SW5	U4	3.3 V
SW6	U10	3.3 V

Jumper Configuration

The jumpers on the EPXA10 development board serve several functions:

- Clock distribution
- Enabling clocks
- JTAG configuration
- Enabling the PLL interface

Table 29 lists the jumpers on the EPXA10 development board.

Table 29. Jumpers (Part 1 of 2)

Jumper & Description	Pins 1-2 Connected	Pins 2-3 Connected	Default
JP1 *(1)*	SD_DQS0_SD_CLK_N	N/A	1-2
JP2 *(2)*	TRACE_PORT_TCK (TCK)	TRACE_PORT_TCK (PROC_TCK)	2-3
JP3 *(2)*	TRACE_PORT_TMS (TMS)	TRACE_PORT_TMS (PROC_TMS)	2-3
JP4 *(2)*	TRACE_PORT_TD0 (TD0)	TRACE_PORT_TD0 (PROC_TD0)	2-3
JP5 *(2)*	TRACE_PORT_TD1 (TD1)	TRACE_PORT_TD1 (PROC_TD1)	2-3
JP6 *(2)*	TRACE_PORT_TRST (TRST)	TRACE_PORT_TRST (PROC_TRST)	2-3
JP14 *(3)*	PCI_TDI (PCI_TDIO1)	N/A	None
JP15 *(3)*	PCI_TCK	N/A	None
JP16 *(3)*	PCI_TRST	N/A	None
JP17 *(3)*	PCI_TMS	N/A	None
JP18 *(3)*	PCI_TDI (PCI_TDO)	N/A	None
MSEL0 *(4)*	MSEL0 (0)	MSEL0 (1)	1-2

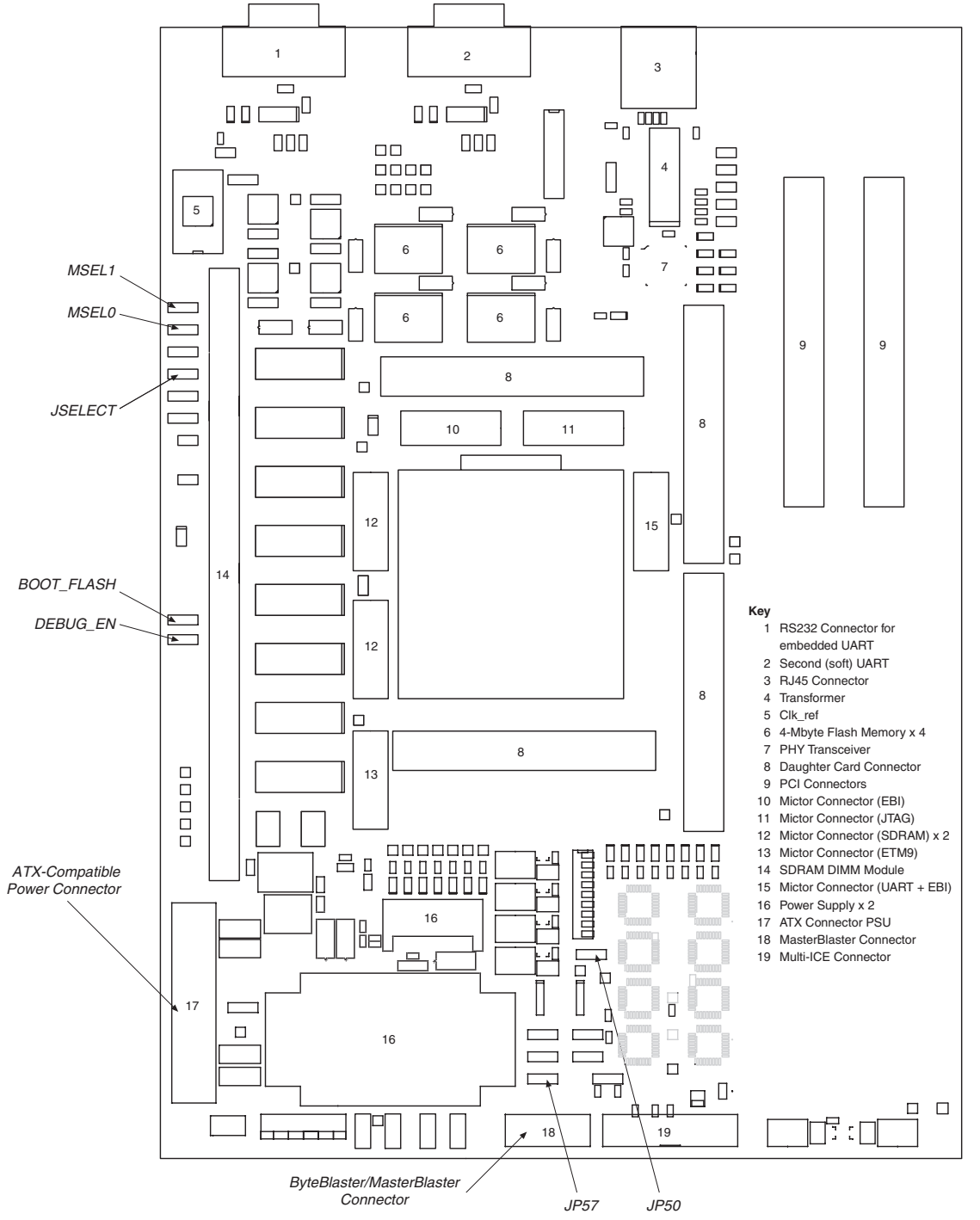
Table 29. Jumpers (Part 2 of 2)

Jumper & Description	Pins 1-2 Connected	Pins 2-3 Connected	Default
MSEL1 *(4)*	MSEL1 (0)	MSEL1 (1)	1-2
JP31 *(5)*	CLK3->LVDSTXINCLK1p	–	None
JP32 *(5)*	nCLK3->LVDSTXINCLK1n	–	None
JP33 *(6)*	CLK_REF 50 Ohms	N/A	None
JSELECT *(7)*	JSELECT=0	JSELECT=1	1-2
DEBUG_EN *(8)*	DEBUG_EN=0	DEBUG_EN=1	2-3
BOOT_FLASH *(4)*	BOOT_FLASH=0	BOOT_FLASH=1	2-3
EN_SELECT (not connected)	EN_SELECT=0	EN_SELECT=1	None
JP40 *(9)*	CLK0=Ext_Osc0	CLK0=TX_CLK	1-2
JP41 *(9)*	CLK1=Ext_Osc1	CLK1=RX_CLK	1-2
JP_VPP	VPP=12 V	VPP=3.3 V	2-3
U179 *(10)*	PHY 25MHz Clock Disabled	PHY 25MHz Clock Enabled	2-3
JP50 (see Table 31 on page 42)	OFF—not to be used	-	1-2
JP51 *(11)*	X7 Osc Disabled	X7 Osc Enabled	2-3
JP52 *(11)*	X8 Osc Disabled	X8 Osc Enabled	2-3
JP53 *(11)*	X9 Osc Disabled	X9 Osc Enabled	2-3
JP54 *(11)*	X10 Osc Disabled	X10 Osc Enabled	2-3
JP55 *(11)*	X11 Osc Disabled	X11 Osc Enabled	2-3
JP57 (see Table 31 on page 42)	ECP2 Bypass	-	1-2
JP58 *(12)*	3.3 V	2.5 V	1-2
JP59 *(12)*	3.3 V	2.5 V	1-2
JP_AGND2GND	Analog to digital GND	-	1-2
JP_PSU_SDR	OFF—not to be used	-	None

Note:
(1) Connects SDRAM DQS0 to SD_CLK_n.
(2) Connects the trace port signals to either JTAG or PROC_JTAG.
(3) Connects the device to the PCI JTAG.
(4) Used to select configuration mode. See "Configuration Interfaces" on page 22.
(5) Connects PLD clock 3 for LVDS. See *AN 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.
(6) Matching load for the embedded processor stripe clock.
(7) Determines whether serial or dual JTAG chains are used for debugging.
(8) Enables/disables debugging.
(9) Connects PLD clocks 0 or 1 to the Ethernet clock.
(10) Enables/disables the Ethernet clock.
(11) Enables/disables clocks.
(12) Set to position 1-2.

Figure 10 on page 37 shows the development board jumper configuration.

Figure 10. Jumper Locations



Clock Distribution

Dedicated inputs on the EPXA10 device are used for clocks. Five are zero-skew; four are global inputs to the PLD and one is a dedicated input providing the embedded processor stripe reference clock. The four PLD clocks service the ClockLock™ and ClockBoost™ circuitry on the Excalibur device. Table 30 lists all the clock sources on the development board.

Table 30. EPXA10 Development Board Clock Sources (Part 1 of 2)

EPXA10 Pin Name	EPXA10 Pin Number	Connection To	Description	Expansion Connector	Board Name Connection
CLK_REF	A28	X7/U147/ J4 *(1)*	50-MHz main clock provided to the synchronous memory and embedded processor. Dedicated input		CLK_REF
CLK1p	N30	X8	Dedicated pin that drives 32.768_MHz clock and inputs		CLK0
CLK2p	Y3	X9	Dedicated pin that drives 32.768_MHz clock and inputs		CLK1
CLK3p	W30	X10	Dedicated pin that drives 32.768_MHz clock and inputs		CLK2
CLK4p	P3	X11	Dedicated pin that drives 32.768_MHz clock and inputs		CLK3
CLK1n	V30	TP_NCLK0*(2)*	Dedicated pin that drives clock and inputs in LVDS mode	U125.199	NCLK0
CLK2n	R3	NCLK1*(2)*	Dedicated pin that drives clock and inputs in LVDS mode	U125.97	NCLK1
CLK3n	Y30	NCLK2*(2)*	Dedicated pin that drives clock and inputs in LVDS mode	U125.87	NCLK2
CLK4n	N3	NCLK3*(2)*	Dedicated pin that drives clock and inputs in LVDS mode	U125.89	NCLK3
CLKLK_FB1N0	AM28	TP_NCLK0FB*(2)*	Dedicated pin that allows external feedback to the PLL in LVDS mode	U125.195	NCLK0_FB
CLKLK_FB2N0	J3	TP_NCLK1FB*(2)*	Dedicated pin that allows external feedback to the PLL in LVDS mode	U125.93	NCLK1_FB
LOCK1	AC30	N/A	Status of ClockLock PLL1	U126.83	AC30
LOCK2	AK4	N/A	Status of ClockLock PLL2	U126.8	AK4
LOCK3	H30	N/A	Status of ClockLock PLL3	U126.85	H30
LOCK4	AK5	N/A	Status of ClockLock PLL4	U126.3	AK5
CLKLK_ENA	P30	N/A	Dedicated pin used for PLL circuitry		PLLENABL
CLKLK_OUT1p	AM29	CLK0_OUT	Dedicated pin that allows the PLL output to be driven off-chip	U125.99	CLK0_OUT
CLKLK_OUT2p	AH3	TP_CLK1_OUT	Dedicated pin that allows the PLL output to be driven off-chip	U125.91	CLK1_OUT

Table 30. EPXA10 Development Board Clock Sources (Part 2 of 2)

EPXA10 Pin Name	EPXA10 Pin Number	Connection To	Description	Expansion Connector	Board Name Connection
CLKLK_FB1p	AL28	CLK0_FBp	Dedicated pin that allows external feedback to the PLL	U125.197	CLK0_FBp
CLKLK_FB2p	K3	TP_CLK1_FBp	Dedicated pin that allows external feedback to the PLL	U125.95	CLK1_FBp

Note:
(1) See "Jumper Configuration for the Clock Input" for details of selecting a source for the stripe clock reference.
(2) Test point.

The clocks on the development board can be configured as required, depending on which devices are used; refer to "Clock Generation & Distribution" on page 19 for a comprehensive list of potential clock requirements.

Jumper Configuration for the Clock Input

Jumpers JP31, JP32, JP40, JP41, and JP51 through JP55 are used to select different clock inputs:.

- JP31 and JP32 can be used to connect CLK3 to lvdstxinclk1p and NCLK3 to lvdstxclk1n, respectively
- JP40 is used to set CLK0 to oscillator 0 (position 1-2) or TX_CLK (position 2-3) and JP41 is used to set CLK1 to oscillator 1 (position 1-2) or RX_CLK (position 2-3)
- JP51to JP55 enable and disable the clocks (X7 to X11, respectively)

During development, if you need to run the clock at a slower rate, you can do so using either the external clock input or a variable oscillator.

The external oscillator is a BNC cable input (J4) that can be used to input a signal from a laboratory signal generator. The variable oscillator is a four-pin socket that supports a variety of 5-V oscillators.

Sources for the Stripe Clock Reference

There are three options for providing a source for the stripe clock reference:

- External clock generator
- Main clock
- An alternative crystal oscillator

Methods of selecting these options are given below.

Using an External Clock Generator

To select an external clock generator, use the following jumper settings:

- Set JP51 to position 1-2 to disable the main clock X7
- Set JP33 to terminate the clock generator at 50Ω

Using the Main Clock

To use the main clock, set JP51 to position 2-3 to enable the crystal oscillator.

Using a Variable Oscillator

To use a variable oscillator as the stripe clock reference, follow the steps below:

1. Plug in the DIL14 crystal oscillator package.
2. Disable the main clock, X7, by connecting pins 1 and 2 at JP51.
3. Provide a 5-V power supply on the board, either by connecting the ATX power supply or by connecting an alternative 5-V input to JP35.

The clock buffer converts 5-V input from the crystal oscillator to the 3.3 V required for the stripe.

Test & Debugging Features

The development board includes the following test features:

- JTAG connectors for use with either the MasterBlaster or ByteBlasterMV, or Multi-ICE
- Test connectors provided for debugging with a logic analyzer
- Matched impedance connectors (MICTORs), which can be used for debugging the individual interfaces

JTAG Programming Chain

There are two JTAG connectors on the EPXA10 development board. Each is connected to a JTAG chain. The MasterBlaster/ByteBlasterMV connector is connected to JTAG and is used to configure the PLD using ByteBlasterMV or MasterBlaster; and the Multi-ICE is connected to JTAG_PROC.

All devices that can be programmed through the JTAG interface are connected to a MasterBlaster/ByteBlasterMV-type connector. The devices connected to the chain are programmed in the following order:

- EPXA10 device
- EPC2 configuration devices
- PCI interface

You can use both JTAG connectors at the same time. A 2 x 5 header, which is used for configuration by the MasterBlaster or ByteBlasterMV, is connected to JTAG. The other JTAG connector is a 2 x 10 header connected to PROC_JTAG, which can only be used by Multi-ICE. The jumper JSELECT is used to specify whether the MasterBlaster/ByteBlasterMV is used in parallel with the Multi-ICE, or alone.

Configuring the JTAG Chain

You can configure the EPXA10 JTAG chain by setting the JSELECT jumper and using the appropriate jumper settings to bypass devices not required in the programming chain.

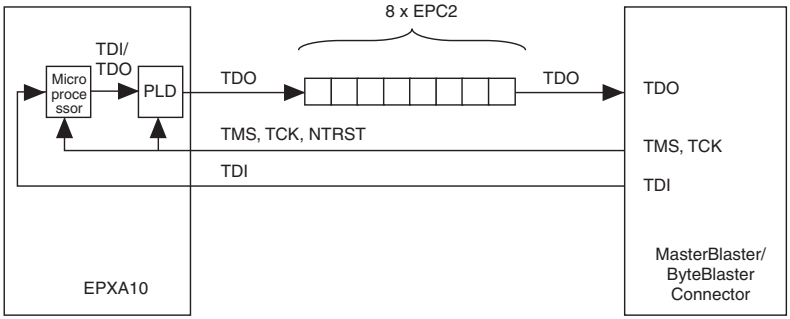
If a device is not included in the programming chain, it must be bypassed to prevent the JTAG chain from being broken. Jumpers JP50 and JP57 determine bypass settings for the EPC2 configuration devices, as shown in Table 31 on page 42.

Table 31. Bypass Settings for EPC2		
	JP57 Pins 1 & 2 Connected	**JP57 Pins 2 & 3 Connected**
JP50 Pins 1 & 2 Connected	Bypass EPC2 (U7-U8)	Bypass all EPC2s (U1-U8)
JP50 Pins 2 & 3 Connected	No bypass	No bypass

Jumper J14 with pins 1-2 connected is used to bypass PCI card 2 (U24) when only one PCI card is required—PCI card 1 (U23) must be used.

By setting JSELECT to 0 (1-2 connected), you can use the MasterBlaster/ByteBlasterMV to debug and download the device software; see Figure 11.

Figure 11. JTAG Chain with JSELECT = 0



The maximum JTAG chain when JSELECT = 0 is as follows:

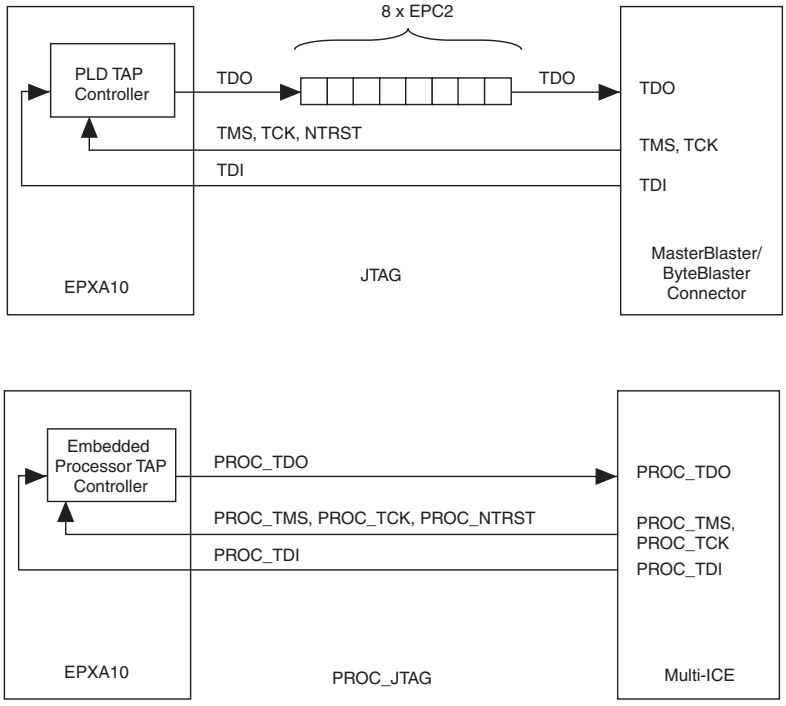
- JTAG connector for MasterBlaster/ByteBlasterMV
- EPXA10 device (both PLD and embedded processor)
- Up to eight EPC2 devices (U1-U8)
- Up to two PCIs (U23 and U24)

When JSELECT = 1 (2-3 connected), there are two JTAG chains, one for the PLD and one for the embedded processor. The maximum JTAG chains are as follows:

- For the PLD
  - JTAG connector for MasterBlaster/ByteBlasterMV or SignalTAP
  - Up to eight EPC2 devices (U1-U8)
  - Up to two PCIs (U23 and U24)
- For the embedded processor
  - JTAG connector for Multi-ICE

By setting JSELECT to 1, you can use Multi-ICE for downloading and debugging the software, and MasterBlaster/ByteBlasterMV for downloading and debugging the hardware. This is shown in Figure 12.

Figure 12. JTAG Chain with JSELECT = 1



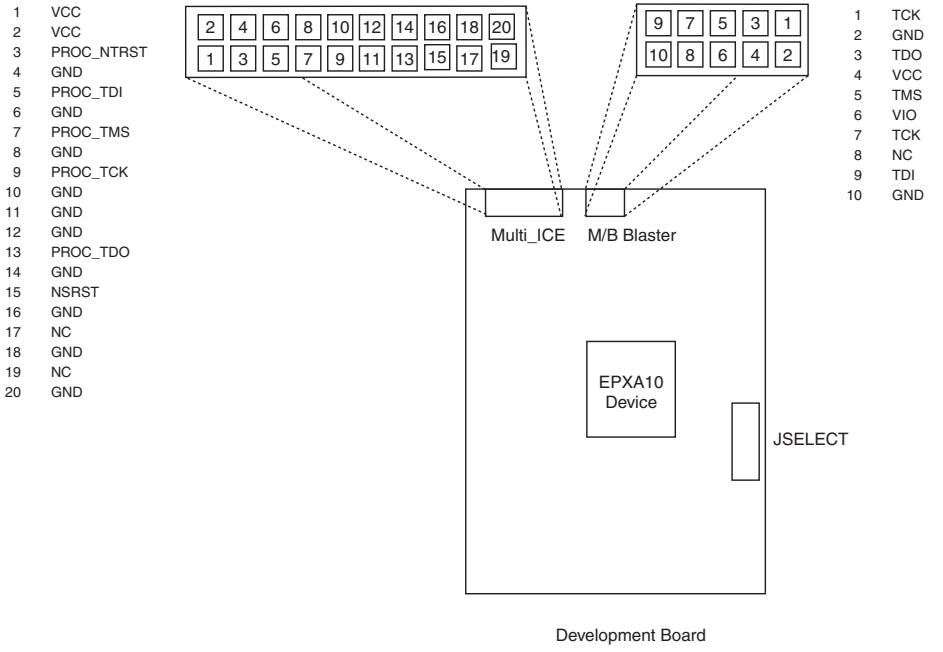
To use SignalTAP to debug the device, JSELECT must be set to 1.

Using MasterBlaster/ByteBlasterMV Cable to Program the EPC2 Devices

The EPC2 devices can be programmed using the Quartus II software, version 1.1, or higher, using either the MasterBlaster or ByteBlasterMV download cable.

Figure 13 on page 44 shows how the MasterBlaster, ByteBlasterMV, and Multi-ICE cables are connected.

Figure 13. Connecting the MasterBlaster, ByteBlasterMV or Multi-ICE Cables



Refer to "Jumpers" on page 35 for details of jumper settings.

Test Connectors

There are various test connectors on the EPXA10 development board, which are documented in Table 55 on page 64.

MICTOR Connectors

A series of six matched impedance connectors (MICTORs) is used to monitor signals from the stripe, specifically from the EBI, UART, SDRAM, and the JTAG chain. Table 32 gives the interface details.

Table 32. MICTOR Interface Device Reference (Part 1 of 2)

Reference	Part Number	Manufacturer	Website Address	Description
U9	AMP ref 2-767004-2	AMP	www.amp.com	EBI
U10	AMP ref 2-767004-2	AMP	www.amp.com	JTAG
U11	AMP ref 2-767004-2	AMP	www.amp.com	SDRAM 1
U12	AMP ref 2-767004-2	AMP	www.amp.com	SDRAM 2

Table 32. MICTOR Interface Device Reference (Part 2 of 2)				
Reference	**Part Number**	**Manufacturer**	**Website Address**	**Description**
TRACE PORT	AMP ref 2-767004-2	AMP	www.amp.com	ETM9
U13	AMP ref 2-767004-2	AMP	www.amp.com	UART and EBI

Debugging

The ETM9 trace module MICTOR connector is used in conjunction with trace tools such as ARM Trace and Lauterbach to debug the software in real time. ETM9 trace tools can either be connected to JTAG or PROC_JTAG signals.

Connector Pin-Outs

Tables 33 through 43 document the pin-outs for the following peripherals:

- DTE UART
- RJ-45 Ethernet
- SDRAM DIMM (for SDR)
- Flash memory
- PCI card
- Trace port
- MICTOR interfaces
- Configuration interfaces

Table 33 lists the UART pin-outs.

Table 33. DTE UART DB9 Male Connector Pin-Outs (1)		
Pin	**Signal**	**Description**
1	DCD	Data carrier detect
2	RXD	Receive data
3	TXD	Transmit data
4	DTR	Data terminal ready
5	GND	Signal ground
6	DSR	Data set ready
7	RTS	Request to send
8	CTS	Clear to send
9	RI	Ring indicator

Note:
(1) The EPXA10 development board has two DB9 male connectors.

Figure 14 shows the UART DB9 male connector.

Figure 14. DTE UART DB9 Male Connector

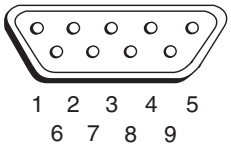


Table 34 lists the Ethernet RJ-45 male connector pin-outs. Figure 15 shows the Ethernet RJ-45 male connector.

Table 34. Ethernet RJ-45 Male Connector Pin-Outs

Pin	Signal	Description
1	TD+	Transmit data +
2	TD–	Transmit data –
3	RD+	Read data +
4	N.C.	No connection
5	N.C.	No connection
6	RD–	Read data –
7	N.C.	No connection
8	N.C.	No connection

Figure 15. Ethernet RJ45 Male Connector

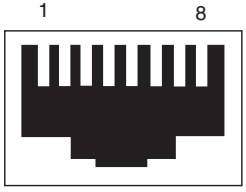


Table 35 lists the SDRAM DIMM socket pin-outs.

Table 35. SDRAM DIMM Socket Pin-Outs (Part 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	SIgnal
1	Vss	2	DQ0	3	DQ1	4	DQ2
5	DQ3	6	Vdd	7	DQ4	8	DQ5
9	DQ6	10	DQ7	11	DQ8	12	Vss
13	DQ9	14	DQ10	15	DQ11	16	DQ12
17	DQ13	18	Vdd	19	DQ14	20	DQ15
21	N.C./CB0	22	N.C./CB1	23	Vss	24	N.C./CB8
25	N.C./CB9	26	Vdd	27	/WE	28	DQMB0
29	DQMB1	30	/S0	31	NU	32	Vss
33	A0	34	A2	35	A4	36	A6
37	A8	38	A10/AP	39	BA1	40	Vdd
41	Vdd	42	CK0	43	Vss	44	NU
45	S2	46	DQMB2	47	DQMB3	48	NU
49	Vdd	50	N.C./CB10	51	N.C./CB11	52	N.C./CB2
53	N.C./CB3	54	Vss	55	DQ16	56	DQ17
57	DQ18	58	DQ19	59	Vdd	60	DQ20
61	/N.C.-MWAIT	62	VREF-N.C.	63	CKE1	64	Vss
65	DQ21	66	DQ22	67	DQ23	68	Vss
69	DQ24	70	DQ25	71	DQ26	72	DQ27
73	Vdd	74	DQ28	75	DQ29	76	DQ30
77	DQ31	78	Vss	79	CK2	80	N.C.
81	N.C.	82	SDA	83	SCL	84	Vdd
85	Vss	86	DQ32	87	DQ33	88	DQ34
89	DQ35	90	Vdd	91	DQ36	92	DQ37
93	DQ38	94	DQ39	95	DQ40	96	Vss
97	DQ41	98	DQ42	99	DQ43	100	DQ44
101	DQ45	102	Vdd	103	DQ46	104	DQ47
105	N.C./CB4	106	N.C./CB5	107	Vss	108	N.C./CB12
109	N.C./CB13	110	Vdd	111	/CAS	112	DQMB4
113	DQMB5	114	/S1	115	/RAS	116	Vss
117	A1	118	A3	119	A5	120	A7
121	A9	122	BA0	123	A11	124	Vdd
125	CK1	126	A12	127	Vss	128	CKE0
129	/S3	130	DQMB6	131	DQMB7	132	A13
133	Vdd	134	N.C.	135	N.C.	136	N.C.
137	N.C.	138	Vss	139	DQ48	140	DQ49

Table 35. SDRAM DIMM Socket Pin-Outs (Part 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	SIgnal
141	DQ50	142	DQ51	143	Vdd	144	DQ52
145	/N.C.-NIRQ	146	VREF-N.C.	147	N.C.	148	Vss
149	DQ53	150	DQ54	151	DQ55	152	Vss
153	DQ56	154	DQ57	155	DQ58	156	DQ59
157	Vdd	158	DQ60	159	DQ61	160	DQ62
161	DQ63	162	Vss	163	CK3	164	N.C.
165	SA0	166	SA1	167	SA2	168	Vdd

Table 36 lists the flash memory pin assignments.

Table 36. Flash Memory Pin-Outs

Pin	Signal	Pin	Signal	Pin	Signal	Pin	SIgnal
1	A15	2	A14	3	A13	4	A12
5	A11	6	A10	7	A9	8	A8
9	N.C.	10	A20	11	WE#	12	RP#
13	VPP	14	WP#	15	A19	16	A18
17	A17	18	A7	19	A6	20	A5
21	A4	22	A3	23	A2	24	A1
25	A0	26	CE#	27	GND	28	OE#
29	DQ0	30	DQ8	31	DQ1	32	DQ9
33	DQ2	34	DQ10	35	DQ3	36	DQ11
37	Vcc	38	DQ4	39	DQ12	40	DQ5
41	DQ13	42	DQ6	43	DQ14	44	DQ7
45	DQ15	46	GND	47	VccQ	48	A16

Table 37 lists the pin assignments on the PCI connectors.

Table 37. PCI Card Connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	SIgnal
A1	–12 V	A2	TCK	B1	TRST#	B2	+12 V
A3	GND	A4	TDO	B3	TMS	B4	TDI
A5	+5 V	A6	+5 V	B5	+5 V	B6	INTA#
A7	INTB#	A8	INTD#	B7	INTC#	B8	+5 V
A9	PRSNT1#	A10	RESERVED	B9	RESERVED	B10	V I/O
A11	PRSNT2#	A12	RESERVED	B11	RESERVED	B12	RESERVED
A13	RESERVED	A14	RESERVED	B13	RESERVED	B14	3.3 V AUX
A15	GND	A16	PCI_CLK	B15	RST#	B16	V I/O
A17	GND	A18	REQ1#	B17	V I/O	B18	GNT1#
A19	V I/O	A20	AD [31]	B19	GND	B20	AD [30]
A21	AD [29]	A22	GND	B21	+ 3.3 V	B22	AD [28]
A23	AD [27]	A24	AD [25]	B23	AD [26]	B24	GND
A25	VCC	A26	C/BE3#	B25	AD[24]	B26	IDSEL
A27	AD[23]	A28	GND	B27	+ 3.3 V	B28	AD[22]
A29	AD[21]	A30	AD[19]	B29	AD[20]	B30	GND
A31	VCC	A32	AD[17]	B31	AD[18]	B32	AD[16]
A33	C/BE2#	A34	GND	B33	+ 3.3 V	B34	FRAME#
A35	IRDY#	A36	+ 3.3 V	B35	GND	B36	TRDY#
A37	DEVSEL#	A38	GND	B37	GND	B38	STOP#
A39	LOCK#	A40	PERR#	B39	+ 3.3 V	B40	RESERVED
A41	+ 3.3 V	A42	SERR#	B41	RESERVED	B42	GND
A43	+ 3.3 V	A44	C/BE1#	B43	PAR	B44	AD[15]
A45	AD[14]	A46	GND	B45	+ 3.3 V	B46	AD[13]
A47	AD[12]	A48	AD[10]	B47	AD[11]	B48	GND
A49	M66EN	A50	GND	B49	AD[9]	B50	GND
A51	GND	A52	AD[8]	B51	GND	B52	C/BE0#
A53	AD[7]	A54	+ 3.3 V	B53	+ 3.3 V	B54	AD[6]
A55	AD[5]	A56	AD[3]	B55	AD[4]	B56	GND
A57	GND	A58	AD[1]	B57	AD[2]	B58	AD[0]
A59	+ 3.3 V	A60	ACK64#	B59	V I/O	B60	REQ64#
A61	+ 5 V	A62	+ 5 V	B61	+ 5 V	B62	+ 5 V

Table 38 lists the pin assignments for the ETM9 trace port.

Table 38. Trace Port Connections

Pin	Signal	Description	Pin	Signal	Description
1	N.C.	No connection	2	N.C.	No connection
3	N.C.	No connection	4	N.C.	No connection
5	GND	Ground	6	TRACECLK	Clock output for the trace port
7	DBGRQ	Not used	8	DBGACK	Output (not used)
9	nSRST	System reset detector	10	EXTTRIG	Output (not used)
11	TDO	Test data input	12	VTRef	Reference voltage input
13	RTCK	Input (not used)	14	VSupply	Power input for the debug equipment
15	TCK	Test clock output	16	TRACEPKT7	Data/address information output on pipeline status
17	TMS	Test mode select output	18	TRACEPKT6	
19	TDI	Test data output	20	TRACEPKT5	
21	nTRST	Reset input/output	22	TRACEPKT4	
23	TRACEPKT15	Data/address information output on pipeline status	24	TRACEPKT3	
25	TRACEPKT14		26	TRACEPKT2	
27	TRACEPKT13		28	TRACEPKT1	
29	TRACEPKT12		30	TRACEPKT0	
31	TRACEPKT11		32	TRACESYNC	
33	TRACEPKT10		34	PIPESTAT2	Processor pipeline status
35	TRACEPKT9		36	PIPESTAT1	
37	TRACEPKT8		38	PIPESTAT0	
39	GND	Ground	40	GND	Ground
41	GND	Ground	42	GND	Ground
43	GND	Ground			

Tables 39 to 43 list the pin assignments for the devices connected to MICTOR interfaces.

Table 39. MICTOR Connector: EBI

Pin	Signal	Description	Pin	Signal	Description
1	N.C.	No connection	2	N.C.	No connection
3	N.C.	No connection	4	N.C.	No connection
5	EBI_A24	EBI address information output	6	EBI_DQ15	EBI data output
7	EBI_A23		8	EBI_DQ14	
9	EBI_A22		10	EBI_DQ13	
11	EBI_A21		12	EBI_DQ12	
13	EBI_A20		14	EBI_DQ11	
15	EBI_A19		16	EBI_DQ10	
17	EBI_A18		18	EBI_DQ9	
19	EBI_A17		20	EBI_DQ8	
21	EBI_A16		22	EBI_DQ7	
23	EBI_A15		24	EBI_DQ6	
25	EBI_A14		26	EBI_DQ5	
27	EBI_A13		28	EBI_DQ4	
29	EBI_A12		30	EBI_DQ3	
31	EBI_A11		32	EBI_DQ2	
33	EBI_A10		34	EBI_DQ1	
35	EBI_A9		36	EBI_DQ0	
37	EBI_A8		38		
39	GND	Ground	40	GND	Ground
41	GND	Ground	42	GND	Ground
43	GND	Ground			

Table 40. MICTOR Connector: SDRAM Part 1

Pin	Signal	Description	Pin	Signal	Description
1	N.C.	No connection	2	N.C.	No connection
3	N.C.	No connection	4	N.C.	No connection
5	SD_DQ16	SDRAM data bus input/output	6	SD_CLK	SDRAM clock
7	SD_DQ15		8	SD_CLKE	SDRAM clock enable
9	SD_DQ14		10	SD_CLK_N	SDRAM clock - inverted
11	SD_DQ13		12	SD_CS1_N	Chip select
13	SD_DQ12		14	SD_CS0_N	Chip select
15	SD_DQ11		16	SD_RAS_N	Row address strobe
17	SD_DQ10		18	SD_CAS_N	Column address strobe
19	SD_DQ9		20	SD_WE_N	Write enable
21	SD_DQ8		22	SD_DQM_ECC	
23	SD_DQ7		24	SD_DQS_ECC	
25	SD_DQ6		26	SD_DQM3	Data byte mask
27	SD_DQ5		28	SD_DQM2	Data byte mask
29	SD_DQ4		30	SD_DQM1	Data byte mask
31	SD_DQ3		32	SD_DQM0	Data byte mask
33	SD_DQ2		34	SD_DQS3	DQS signal
35	SD_DQ1		36	SD_DQS2	DQS signal
37	SD_DQ0		38	SD_DQS1	DQS signal
39	GND	Ground	40	GND	Ground
41	GND	Ground	42	GND	Ground
43	GND	Ground			

Table 41. MICTOR Connector: SDRAM Part 2

Pin	Signal	Description	Pin	Signal	Description
1	N.C.	No connection	2	N.C.	No connection
3	N.C.	No connection	4	N.C.	No connection
5	SD_DQ31	SDRAM data bus input/output	6	SD_DQS0	DQS signal
7	SD_DQ30		8		
9	SD_DQ29		10	SD_ADD14	SDRAM address bus
11	SD_DQ28		12	SD_ADD13	
13	SD_DQ27		14	SD_ADD12	
15	SD_DQ26		16	SD_ADD11	
17	SD_DQ25		18	SD_ADD10	
19	SD_DQ24		20	SD_ADD9	
21	SD_DQ23		22	SD_ADD8	
23	SD_DQ22		24	SD_ADD7	
25	SD_DQ21		26	SD_ADD6	
27	SD_DQ20		28	SD_ADD5	
29	SD_DQ19		30	SD_ADD4	
31	SD_DQ18		32	SD_ADD3	
33	SD_DQ17		34	SD_ADD2	
35			36	SD_ADD1	
37			38	SD_ADD0	
39	GND	Ground	40	GND	Ground
41	GND	Ground	42	GND	Ground
43	GND	Ground	44		

Table 42. MICTOR Connector: Configuration, EBI and UART

Pin	Signal	Description	Pin	Signal	Description
1	N.C.	No connection	2	N.C.	No connection
3	N.C.	No connection	4	N.C.	No connection
5	EBI_A7	EBI address input information output	6	EBI_CLK	EBI clock output
7	EBI_A6		8	EBI_CS3	EBI chip selects
9	EBI_A5		10	EBI_CS2	
11	EBI_A4		12	EBI_CS1	
13	EBI_A3		14	EBI_CS0	
15	EBI_A2		16	EBI_WE_N	EBI write enable - low
17	EBI_A1		18	EBI_OEN	EBI output enable
19	EBI_A0		20	EBI_BE1	
21	UART_CTS_N	Clear to send input	22	EBI_BE0	
23	UART_DSR_N	Data set ready input	24	INT_EXTPIN_N	External interrupt pin
25	UART_RXD	Receive data	26	EBI_ACK	Acknowledge output signal for an asynchronous transaction
27	UART_DCD_N	Data carriage detect input	28	nRESET	Reset input
29	UART_RI_N	Ring indicator input	30	DATA0	Serial data input
31	UART_TXD	Transmit data output	32	CONF_DONE	PLD configuration complete input/output
33	UART_RTS_N	Request to send output	34	nTRST	System reset input
35	UART_DTR_N	Data terminal ready output	36	DCLK	Clock serial configuration input
37	nSTATUS	Configuration error input/output	38	nCONFIG	Initiate configuration input
39	GND	Ground	40	GND	Ground
41	GND	Ground	42	GND	Ground
43	GND	Ground			

Table 43. MICTOR Connector: JTAG, Clocks & I/O

Pin	Signal	Description	Pin	Signal	Description
1	N.C.		2	N.C.	
3	N.C.		4	N.C.	
5	PROC_TDO	JTAG data output (to next device in the chain	6	SD_DQ_ECC6	Standard I/O (not used)
7	PROC_TDI	JTAG data input	8	SD_DQ_ECC5	
9	PROC_TCK	JTAG clock	10	SD_DQ_ECC4	
11	PROC_TMS	JTAG mode select	12	SD_DQ_ECC3	
13	PROC_NTRST	JTAG reset (pulled high)	14	SD_DQ_ECC2	
15	TDO	JTAG data output (to next device in the chain	16	SD_DQ_ECC1	
17	TDI	JTAG data input	18	SD_DQ_ECC0	
19	TCK	JTAG clock	20	NCLK3 *(1)*	Clock
21	TMS	JTAG mode select	22	NCLK2 *(1)*	
23	nPOR		24	NCLK1_FB *(1)*	
25	CLK_REF		26	CLK0_FBp *(1)*	
27	CLK0		28	CLK1_FBp *(1)*	
29	CLK1		30	CLK0_OUT *(1)*	
31	CLK2		32	CLK1_OUT *(1)*	
33	CLK3		34	NCLK1 *(1)*	
35			36	NCLK0_FB *(1)*	
37			38	NCLK0 *(1)*	
39	GND	Ground	40	GND	Ground
41	GND	Ground	42	GND	Ground
43	GND	Ground			

Note:
(1) Board revision 1 only.

Table 44 lists the pin assignments on the MasterBlaster/ByteBlasterMV connector.

Table 44. MasterBlaster/ByteBlasterMV Female Connector

Pin	JTAG Mode	
	Signal	Description
1	TCK	Clock signal
2	GND	Signal ground
3	TDO	Data from device
4	VCC	Power supply
5	TMS	JTAG state machine control
6	VIO	Reference voltage for MasterBlaster/ByteBlasterMV output driver
7	TCK	Clock signal
8	-	No connection
9	TDI	Data to device
10	GND	Signal ground

Table 45 lists the pin assignments on the Multi-ICE connector.

Table 45. Multi-ICE Connector (Part 1 of 2)

Pin	Signal	Description	Direction
1	VCC	Power supply	N/A
2	VCC	Power supply	N/A
3	PROC_NTRTST	Processor reset	O
4	GND	Ground	N/A
5	PROC_TDI	Processor test data input	I
6	GND	Ground	N/A
7	PROC_TMS	Processor test mode select	I
8	GND	Ground	N/A
9	PROC_TCK	Processor test clock input	I
10	GND	Ground	N/A
11	GND	Ground	N/A
12	GND	Ground	N/A
13	PROC_TDO	Processor test data output	O
14	GND	Ground	N/A
15	NSRST	Warm reset	I/O
16	GND	Ground	N/A

Table 45. Multi-ICE Connector (Part 2 of 2)

Pin	Signal	Description	Direction
17	N.C.	No connection	N/A
18	GND	Ground	N/A
19	NA	No connection	N/A
20	GND	Ground	N/A

Development Board Pin-Outs & Signals

The main component of the development board is the EPXA10F1020C2 device. The pins on the EPXA10 device are assigned to functions on the board. When generating IP cores for the EPXA10 device, the pins must be used as defined to avoid damaging the device. The following sections list the interfaces and dedicated pins on the board. Any pins not used for a design should be left in the high-impedance (input) state to avoid contention.

This section details the pins on the EPXA10 device which are assigned to the following purposes:

- Configuration
- SDR SDRAM
- EBI
- UARTs 1 and 2
- Ethernet
- User LEDs, push buttons, and dip-switches
- Fast I/O pins
- Test points.

Pin assignments are grouped into tables for control pins, bank address pins, and data bus pins where appropriate. The tables also detail signals passing across a connection. The remaining I/O pins on the EPXA10 device are listed at the end of this section.

Configuration

The EPXA10 device pins listed in Table 46 on page 58 are used exclusively for configuring the device. Refer to "General Information" on page 17 for more information about EPXA10 configuration.

Refer to the *ARM-Based Embedded Processor PLDs Hardware Reference Manual* for details of the power pins.

Table 46. EPXA10 Device Configuration Pins

Signal Name	EPXA10 Device Pin	Description
MSEL0	J30	Configuration mode select (tied to GND)
MSEL1	K30	Configuration mode select (tied to GND)
NSTATUS	AM14	OE for EPC2s
NCONFIG	R30	INIT for EPC2s
DCLK	W3	Data clock for EPC2s
CONF_DONE	AM13	Configuration complete indicator
INIT_DONE	D14	Initialization complete indicator
nCE	AC3	Not connected
nCEO	D13	
DATA0	V3	Serial input for EPC2 configuration data
DATA1	D10	Serial input for EPC2 configuration data; available for user I/O after configuration
DATA2	A9	
DATA3	B9	
DATA4	C9	
DATA5	D9	
DATA6	A4	
DATA7	B4	
TDI	AD3	JTAG data input
TDO	E11	JTAG data output (to next device in the chain
TCK	AM19	JTAG clock
TMS	AM20	JTAG mode select
TRST	C13	JTAG reset (pulled high)
PROC_TDI	H27	JTAG data input
PROC_TDO	H26	JTAG data output (to next device in the chain
PROC_TCK	D30	JTAG clock
PROC_TMS	E29	JTAG mode select
PROC_TRST	E30	JTAG reset (pulled high)
DEV_CLRn	H3	Global reset for the device
DEV_OE	AE3	Device output enable
nWS	C4	Write strobe
nRS	D4	Read strobe
nCS	D3	Signal providing handshaking between devices
CS	E3	Chip select
RDYnBSY	E14	Ready/busy
CLKUSR	A13	Clock signal

SDR SDRAM Interface

The SDRAM module is 64 bits wide, and the general-purpose memory data bus is 32 bits wide. To allow access to the entire SDRAM memory array, data bus pins are doubled. This means that the upper half of the data bus is connected to the lower half. For example, GPM_D(0) is connected to data pin 0 and data pin 32 on the SDRAM DIMM. Ensure that only 32 bits of the SDRAM data bus are enabled at a time (D[31..0] or D[63..32]) to avoid contention.

The SDRAM_DQM[7:0] lines are used to enable the SDRAM outputs. Because the data bus pins are doubled-up on the SDRAM DIMM, both halves of the data bus may not be enabled at the same time. For example, if SDRAM_DQM[0] is enabled, SDRAM_DQM(4) cannot be enabled or contention will occur.

Table 47 shows the pin-outs for the SDR SDRAM control signals.

Table 47. SDR SDRAM Control Signal Pin-Outs

Signal Name	EPXA10 Device Pin	Description
SD_RAS_N	F17	Row address strobe
SD_CAS_N	F18	Column address strobe
SD_WE_N	G18	Write enable
SD_CS0_N	G14	Chip select
SD_CS1_N	F16	Chip select
SD_CLKE	F14	Clock enable
SD_CLK	F15	SDRAM clock
SD_CLK_N	G13	SDRAM clock - inverted
SD_DQM(0)	H14	Data byte mask
SD_DQM(1)	L14	Data byte mask
SD_DQM(2)	K9	Data byte mask
SD_DQM(3)	H9	Data byte mask
SD_DQS(0)	J14	DQS signal
SD_DQS(1)	K14	DQS signal
SD_DQS(2)	K10	DQS signal
SD_DQS(3)	H10	DQS signal

Table 48 lists the SDRAM data bank and address bus pin-outs.

Table 48. SDR SDRAM Data Bank & Address Bus Pin-Outs

Signal Name	EPXA10 Device Pin	Signal Name	EPXA10 Device Pin
SD_DQ0	H18	SD_DQ1	H17
SD_DQ2	H16	SD_DQ3	J18
SD_DQ4	J17	SD_DQ5	H15
SD_DQ6	J16	SD_DQ7	J15
SD_DQ8	K18	SD_DQ9	K17
SD_DQ10	L18	SD_DQ11	K16
SD_DQ12	L17	SD_DQ13	L16
SD_DQ14	K15	SD_DQ15	L15
SD_DQ16	L13	SD_DQ17	K13
SD_DQ18	L12	SD_DQ19	K12
SD_DQ20	L11	SD_DQ21	K11
SD_DQ22	L10	SD_DQ23	L9
SD_DQ24	H13	SD_DQ25	H12
SD_DQ26	J13	SD_DQ27	J12
SD_DQ28	J11	SD_DQ29	J10
SD_DQ30	J9	SD_DQ31	H11
SD_A0	G12	SD_A1	F13
SD_A2	G11	SD_A3	F12
SD_A4	F11	SD_A5	G10
SD_A6	F10	SD_A7	F9
SD_A8	G9	SD_A9	F8
SD_A10	G8	SD_A11	F7
SD_A12	F6	SD_A13	G7
SD_A14	G6		

EBI

The EBI shares addresses and data with the SDRAM, flash, and configuration devices. Each type of memory has separate control lines.

Table 49 on page 61 shows the EPXA10 pin-outs for the EBI control signals.

Table 49. EBI Control Signal Pin-Outs

Signal Name	EPXA10 Device Pin	Description
EBI_BE0	F27	Byte enable
EBI_BE1	E27	Byte enable
EBI_OE	F26	Output enable
EBI_WE	E26	Write enable
EBI_CS0	A25	Chip select
EBI_CS1	B25	Chip select
EBI_CS2	C25	Chip select
EBI_CS3	D25	Chip select
EBI_CLK	E25	EBI clock
EBI_ACK	F25	EBI acknowledge

Table 50 shows the EBI data bank and address bus pin-outs.

Table 50. EBI Data Bank and Address Bus Pin-Outs

Signal Name	EPXA10 Device Pin	Signal Name	EPXA10 Device Pin
EBI_DQ0	J21	EBI_DQ1	H21
EBI_DQ2	E20	EBI_DQ3	F20
EBI_DQ4	E19	EBI_DQ5	L20
EBI_DQ6	K20	EBI_DQ7	J20
EBI_DQ8	H20	EBI_DQ9	G20
EBI_DQ10	F19	EBI_DQ11	G19
EBI_DQ12	L19	EBI_DQ13	K19
EBI_DQ14	J19	EBI_DQ15	H19
EBI_A0	H25	EBI_A1	D24
EBI_A2	E24	EBI_A3	F24
EBI_A4	G24	EBI_A5	J24
EBI_A6	H24	EBI_A7	E23
EBI_A8	F23	EBI_A9	G23
EBI_A10	K23	EBI_A11	J23
EBI_A12	H23	EBI_A13	E22
EBI_A14	F22	EBI_A15	E21
EBI_A16	L22	EBI_A17	K22
EBI_A18	J22	EBI_A19	H22
EBI_A20	G22	EBI_A21	F21
EBI_A22	G21	EBI_A23	L21
EBI_A24	K21		

UART1 and UART2

Table 51 details the pins used for UARTs 1 and 2.

Table 51. Extension Header UARTs 1 & 2 I/O Pin-Outs

PLD UART			Embedded Stripe UART		
EPXA10 Device Pin	Device Signal	Expansion Board Connector	EPXA10 Device Pin	Device Signal	Expansion Board Connector
J27	UART1_DTR_N	U126.171	G28	UART_CTS_N	N.C.
J29	UART1_TXD	U126.174	D29	UART_RXD	N.C.
K29	UART1_RXD_N	U126.177	E28	UART_RI_N	N.C.
K27	UART1_DSR_N	U126.179	C28	UART_RTS_N	N.C.
J28	UART1_RTS_N	U126.173	F28	UART_DSR_N	N.C.
J26	UART1_RI_N	U126.175	G27	UART_DCD_N	N.C.
K28	UART1_DCD_N	U126.178	D28	UART_TXD	N.C.
K26	UART1_CTS_N	U126.181	G26	UART_DTR_N	N.C.

Ethernet

Table 51 details the pins used for the Ethernet interface.

Table 52. Extension Header Ethernet Pin-Outs

EPXA10 Device Pin	Device Signal	Expansion Board Connector	EPXA10 Device Pin	Device Signal	Expansion Board Connector
R23	RXD1	U126.155	R24	TXD3	U126.153
R25	TXD0	U126.149	M19	MDC	U126.145
M20	RST_N	U126.146	M21	TX_ER	U126.161
M22	TX_EN	U126.162	M23	RXD2	U126.157
N19	CRS	U126.166	N20	COL	U126.163
N21	RX_DV	U126.167	N22	MDIO	U126.169
N23	RXD0	U126.154	P20	INTR	U126.147
P21	RX_ER	U126.165	P22	RX_D3	U126.158
N25	TXD1	U126.150	P25	TXD2	U126.151

Fast I/O Pins

Table 53 details the pins used for the EPXA10 fast I/O pins.

Table 53. EPXA10 Fast I/O Pins

EPXA10 Pin Name	Description	Pin	Board Connector	Board Name
FAST0	Dedicated fast I/O pins	E13	U126.133	FAST0
FAST1	Dedicated fast I/O pins	E12	U126.134	FAST1
FAST2	Dedicated fast I/O pins	AM18	U126.135	FAST2
FAST3	Connected to PCI to provide IRDY#	AM15		IRDY#

User LEDs, Switches and Push Button LEDs

Table 54 details the pins used for the user-defined LEDs, push-button switches and dip-switches.

Table 54. Expansion Header LED, Switch and Push Button I/O Pin-Outs

EPXA10 Device	Device Signal	Board Connector	EPXA10 Device	Device Signal	Board Connector
V6	USER_LED0	U123.1	U5	USER_LED1	U123.3
V5	USER_LED2	U123.4	U6	USER_LED3	U123.5
V7	USER_LED4	U123.7	V8	USER_LED5	U123.8
U7	USER_LED6	U123.9	T6	USER_LED7	U123.11
U8	USER_SW0	U123.12	T5	USER_SW1	U123.13
V4	USER_SW2	U123.15	V10	USER_SW3	U123.16
T7	USER_SW4	U123.17	W12	USER_SW5	U123.17
U9	USER_SW6	U123.20	V11	USER_SW7	U123.21
R6	USER-SW8	U123.23	T8	USER_PB0	U123.24
R5	USER_PB1	U123.25	U4	USER_PB2	U123.27
U10	USER_PB3	U123.28			

List of Test Points

Table 55 on page 64 lists the test points on the EPXA10 development board.

Table 55. EPXA10 Development Board Test Points

Test Point	Connected To
GND1	GND
GND2	GND
GND3	GND
GND4	GND
GND5	GND
GND6	GND
GND7	GND
TP_NSTATUS	NSTATUS
TP_TCK1	TCK1
TP_TDI1	TDI1
TP_TDO1	TDO1
TP_TMS1	TMS1
CLK0_FBP	CLK0_FBP
CLK0_OUT	CLK0_OUT
CLK2	CLK2
CLK3	CLK3
CLK_REF	CLK_REF
NCLK1	NCLK1
NCLK2	NCLK2
NCLK3	NCLK3
TP_CLK0	CLK0
TP_CLK1	CLK1
TP_CLK1_FBP	CLK1_FBP
TP_CLK1_OUT	CLK1_OUT
TP_EBI_CLK	EBI_CLK
TP_NCLK0	NCLK0
TP_NCLK0_FB	NCLK0_FB
TP_NCLK1_FB	NCLK1_FB
TP_CS0_N	CS0_N
TP_CS1_N	CS1_N
TP_CS2_N	CS2_N
TP_CS3_N	CS3_N
TP_OE_N	OE_N
TP_WE_N	WE_N

Table 55. EPXA10 Development Board Test Points

Test Point	Connected To
–12V	Test points for input power supply
–5V	
1.8V	
12V	
2.5V	
3.3V	
5V	
U155	ATX POWER_OK
TP1	I2C Test Points for DIMM Socket
TP2	
TP3	
TP4	
TP5	

Expansion Header I/O Pins

Table 56 lists the remaining I/O pins on the EPXA10 development board daughter cards, and their assignments on the EPXA10 device. Some of these pins can optionally be dedicated to the Ethernet, UART, user LEDs, push-button switches, and dip-switches.

Table 56. Development Board Expansion Header I/O Pin-Outs (Part 1 of 5)

EPXA10 Device	Board Connector	EPXA10 Device	Board Connector	EPXA10 Device	Board Connector
A14	U125.191	A15	U125.188	A18	U125.175
A19	U125.174	A20	U125.168	A23	U125.163
A24	U125.158	A29	U126.63	A5	U123.183
A8	U123.171	AA10	U125.132	AA11	U125.126
AA12	U125.119	AA21	U124.128	AA22	U124.135
AA23	U124.142	AA24	U124.148	AA25	U124.158
AA26	U124.168	AA28	U124.154	AA5	U125.136
AA6	U125.104	AA27	U124.180	AA7	U125.148
AA8	U125.143	AB10	U124.16	AB11	U124.3
AB12	U123.168	AB13	U123.154	AB14	U123.140
AB15	U123.127	AB16	U123.114	AB23	U125.49
AB24	U125.1	AB25	U125.32	AB26	U124.156
AB27	U124.167	AB28	U124.164	AB5	U125.130
AB6	U125.150	AB7	U125.144	AB8	U125.139
AB9	U125.131	AC1	U126.47	AC10	U124.15

Table 56. Development Board Expansion Header I/O Pin-Outs (Part 2 of 5)

EPXA10 Device	Board Connector	EPXA10 Device	Board Connector	EPXA10 Device	Board Connector
AC11	U124.1	AC12	U123.166	AC13	U123.147
AC14	U123.139	AC15	U123.126	AC16	U123.112
AC2	U126.48	AC23	U125.51	AC24	U125.40
AC25	U125.31	AC26	U124.144	AC27	U124.155
AC28	U124.143	AC29	U124.134	AC30	U126.83
AC31	U126.78	AC32	U126.77	AC4	U125.115
AC5	U125.123	AC7	U125.138	AC6	U125.146
AC8	U125.128	AC9	U125.120	AD1	U126.50
AD10	U124.13	AD11	U123.170	AD12	U123.162
AD13	U123.148	AD14	U123.138	AD15	U123.124
AD16	U123.111	AD2	U126.51	AD23	U125.52
AD24	U125.41	AD25	U125.29	AD26	U124.130
AD27	U124.136	AD28	U124.138	AD29	U124.132
AD30	U124.131	AD31	U126.74	AD32	U126.75
AD4	U125.114	AD5	U125.122	AD6	U125.135
AD7	U125.124	AD8	U125.118	AD9	U124.28
AE1	U126.53	AE10	U124.12	AE11	U123.167
AE12	U123.156	AE13	U123.150	AE14	U123.136
AE15	U123.123	AE16	U123.110	AE2	U126.54
AE23	U125.53	AE24	U125.43	AE25	U125.28
AE26	U124.122	AE27	U124.123	AE28	U124.127
AE29	U124.126	AE3	U126.2	AE30	U124.124
AE31	U126.72	AE32	U126.71	AE4	U125.112
AE5	U125.116	AE6	U124.49	AE7	U124.44
AE8	U124.39	AE9	U124.27	AF10	U124.11
AF11	U123.163	AF12	U123.158	AF13	U123.151
AF14	U123.135	AF15	U123.122	AF16	U123.108
AF24	U125.44	AF25	U125.27	AF26	U125.17
AF27	U124.119	AF28	U124.120	AF5	U125.111
AF6	U124.48	AF7	U124.41	AF8	U124.37
AF9	U124.25	AG10	U124.9	AG11	U123.160
AG12	U123.159	AG13	U123.152	AG14	U123.134
AG15	U123.120	AG16	U123.107	AG20	U125.57
AG24	U125.45	AG25*(1)*	U125.25	AG26	U125.16
AG27	U124.116	AG28	U124.114	AG5	U124.56
AG6	U124.47	AG7	U124.43	AG8	U124.36
AG9	U124.24	AH1	U126.56	AH10	U124.4

Table 56. Development Board Expansion Header I/O Pin-Outs (Part 3 of 5)

EPXA10 Device	Board Connector	EPXA10 Device	Board Connector	EPXA10 Device	Board Connector
AH11	U123.164	AH12	U123.155	AH13	U123.146
AH14	U123.132	AH15	U123.119	AH16	U123.106
AH2	U126.57	AH23	U125.48	AH24	U125.39
AH25*(1)*	U125.24	AH26	U125.15	AH27	U125.13
AH28	U125.9	AH29	U124.115	AH30	U124.118
AH31	U126.68	AH32	U126.69	AH4	U124.55
AH5	U124.52	AH6	U124.45	AH7	U124.40
AH8	U124.35	AH9	U124.17	AJ1	U126.59
AJ10	U124.5	AJ13	U123.144	AJ31	U126.66
AJ14	U123.131	AJ15	U123.118	AJ16	U123.104
AJ2	U126.60	AJ20	U125.56	AJ23	U125.47
AJ24	U125.37	AJ25*(1)*	U125.23	AJ28	U125.11
AJ29	U125.7	AJ3	U126.9	AJ30	U125.59
AJ32	U126.65	AJ4	U124.53	AJ5	U124.51
AJ8	U124.33	AJ9	U124.19	AK10	U124.7
AK13	U123.143	AK14	U123.130	AK15	U123.116
AK16	U123.103	AK17	U123.102	AK24	U125.36
AK25	U125.21	AK28	U125.12	AK29	U125.8
AK4	U126.8	AK5	U126.3	AK8	U124.32
AK9	U124.20	AL10	U124.8	AL13	U123.142
AL14	U123.128	AL15	U123.115	AL20	U125.55
AL24	U125.35	AL25	U125.20	AL29	U126.84
AL4	U126.11	AL5	U126.6	AL8	U124.31
AL9	U124.21	AM24	U125.33	AM25	U125.19
AM4	U126.12	AM5	U126.5	AM8	U124.29
AM9	U124.23	B14	U125.190	B15	U125.187
B18	U125.176	B19	U125.172	B20	U125.167
B23	U125.162	B24	U125.156	B29	U126.62
B5	U123.182	B8	U123.176	C14	U125.194
C19	U125.171	C20	U125.166	C23	U125.160
C8	U123.175	D1	U126.14	D15	U125.186
D16	U125.183	D17	U125.180	D18	U125.178
D19	U125.170	D2	U126.15	D20	U125.164
D23	U125.159	D31	U126.130	D32	U126.131
D5	U123.85	D8	U123.180	E1	U126.17
E10	U123.184	E15	U125.192	E16	U125.184
E17	U125.182	E18	U125.179*(1)*	E2	U126.18

Table 56. Development Board Expansion Header I/O Pin-Outs (Part 4 of 5)

EPXA10 Device	Board Connector	EPXA10 Device	Board Connector	EPXA10 Device	Board Connector
E31	U126.128	E32	U126.127	E4	U123.77
E5	U123.84	E6	U123.172	E7	U123.174
E8	U123.179	E9	U123.178	F5	U123.83
G5	U123.81	H1	U126.20	H2	U126.21
H30	U126.85	H31	U126.124	H32	U126.125
H4	U123.75	H5	U123.80	J1	U126.23
J2	U126.24	J26	U126.170	J27	U126.171
J28	U127.173	J29	U126.174	J31	U126.122
J32	U126.121	J4	U123.73	J5	U123.79
K1	U126.26	K2	U126.27	K26	U126.181
K27	U126.179	K28	U126.178	K29	U126.177
K31	U126.118	K32	U126.119	K4	U123.72
K5	U123.76	L23	U126.183	L24	U125.3*(1)*
L26	U125.4	L27	U125.5*(1)*	L28	U126.182
L5	U123.71	M19	U126.145*(1)*	M20	U126.146*(1)*
M21	U126.161	M22	U126.162	M23	U126.157
M25	U125.80				
M26	U125.80	M28	U125.83	M5	U123.69
N1	U126.30	N11	U123.65	N12	U123.67
N13	U123.68	N19	U126.166	N2	U126.29
N20	U126.163	N21	U126.167	N22	U126.169
N23	U126.154	N25	U126.150	N26	U125.69*(1)*
N29	U125.71*(1)*	N31	U126.116	N32	U126.115
N4	U123.64	N5	U123.51	P1	U126.32
P10	U123.57	P11	U123.59	P12	U123.60
P13	U123.61	P2	U126.33	P20	U126.147*(1)*
P21	U126.165	P22	U126.158	P25	U126.151
P27	U125.81*(1)*	P28	U126.142*(1)*	P29	U126.143*(1)*
P31	U126.112	P32	U126.113	P4	U123.63
P5	U123.37	P6	U123.35	P7	U123.43
P8	U123.48	R1	U126.35	R10	U123.52
R11	U123.53	R12	U123.55	R13	U123.56
R2	U126.36	R20	U124.178	R21	U124.83
R22	U124.75	R23	U126.155	R24	U126.153
R25	U126.149	R26	U126.137*(1)*	R27	U126.138*(1)*
R28	U126.139*(1)*	R29	U126.141*(1)*	R31	U126.110
R32	U126.109	R4	U123.49	R5	U123.25

Table 56. Development Board Expansion Header I/O Pin-Outs (Part 5 of 5)

EPXA10 Device	Board Connector	EPXA10 Device	Board Connector	EPXA10 Device	Board Connector
R6	U123.23	R7	U123.29	R8	U123.33
R9	U123.44	T5	U123.13	T6	U123.11
T7	U123.17	T8	U123.24	T10	U123.39
T11	U123.41	T12	U123.45	T13	U123.47
T21	U124.174	T22	U124.179	T23	U124.81
T25	U124.69	T26	U124.65	T27	U124.57
T28	U124.64	T29	U124.63	T4	U123.36
U10	U123.28	U11	U123.32	U12	U123.40
U21	U124.163	U22	U124.172	U23	U124.184
U24	U124.80	U25	U124.71	U26	U124.67
U27	U124.59	U28	U124.73	U29	U124.72
U4	U123.27	U5	U123.3	U6	U123.5
U7	U123.9	U8	U123.12	U9	U123.20
V1	U126.38	V10	U123.16	V11	U123.21
V12	U123.31	V2	U126.39	V21	U124.152
V22	U124.162	V23	U124.171	V25	U124.79
V26	U124.61	V27	U124.60	V28	U124.85
V29	U124.84	V31	U126.106	V32	U126.107
V4	U123.15	V5	U123.4	V6	U123.1
V7	U123.7	V8	U123.8	W1	U126.41
W10	U125.147	W11	U125.142	W12	U123.17
W2	U126.42	W21	U124.147	W22	U124.151
W23	U124.160	W25	U124.183	W26	U124.77
W27	U124.68	W28	U124.175	W29	U124.176
W31	U126.104	W32	U126.103	W4	U125.102
W5	U125.103	W6	U125.110	W7	U125.108
W8	U125.106	Y1	U126.45	Y10	U125.140
Y11	U125.134	Y12	U125.127	Y2	U126.44
Y21	U124.140	Y22	U124.146	Y23	U124.150
Y24	U124.159	Y25	U124.170	Y26	U124.182
Y27	U124.76	Y28	U124.166	Y29	U124.139
Y31	U126.80	Y32	U126.81	Y4	U125.155
Y5	U125.151	Y6	U125.107	Y7	U125.154
Y8	U125.152				

Note:
(1) Board Revision 1.1.

General Usage Guidelines

To use the development board properly, and to avoid damage to it, follow the guidelines in this section.

Anti-static Handling

Before handling the card, you should take proper anti-static precautions, otherwise the board can be damaged.

SDR SDRAM to DIMM Data Bus Connections

To avoid conflict between the 64-bit SDRAM bus and the 32-bit general purpose memory data bus, ensure that only the desired portion of the bus is enabled at any one time. See "SDR SDRAM Interface" on page 59 for details.

Unused EPXA10 Device Pins

All unused general-purpose I/O EPXA10 device pins have been allocated to the expansion headers. To avoid unnecessary power consumption and possible contention, unused pins must be left in the high impedance (input) state. Follow the steps below to put the unused EPXA10 device pins into a high-impedance state:

1. Run the Quartus II software.
2. Choose **Compiler Settings** (**Processing** menu).
3. Click the **Chips & Devices** tag.
4. Click the **Device & Pin Options** button.
5. Click the **Unused Pins** tag.
6. Under **Reserve all unused pins**, select **As inputs, tri-stated**.

   All the critical control lines for the interfaces on the board are pulled to the inactive state.

If a device is not used, it can be ignored and the EPXA10 device interface pins left as inputs.

Power Consumption

Power consumption issues need to be addressed only if the board is powered from a terminal strip and not the provided ATX power supply adaptor. Altera recommends that you monitor the input current to ensure that sufficient power is supplied. The power required by the board is directly related to the following:

- Number of interfaces used
- Density and speed of the device
- Population of the interfaces

The typical maximum current is 5.0 A, which can be exceeded if the board is heavily loaded with many interfaces running at high-clock speeds.

PCI Cards

Do not use 5-V-only PCI cards.

The PCI slots on the development board are suitable only for 3.3-V and universal PCI cards. The keying slots on 5-V only PCI cards are not designed to mate with the motherboard connectors, because the signalling voltage on 5-V cards is incorrect for the development board.

Test Core Functionality

For implementing a test plan, Altera provides test cores with the development board, which can be programmed onto the EPXA10 device using the JTAG chain. Each test core tests one or more interfaces (push-buttons, LEDs, switches, etc.). Diagnostic software is also provided to test the board, the EPXA10 device, and its test cores, with results displayed on a terminal.

Notes: