CONFIDENTIAL

SAMSUNG

TFT-LCD TV/MONITOR

Chassis	Model
NK15N*	LTM1575W
NK17N*	LTM1775W

Training Manual

TFT-LCD TV/MONITOR

CONTENTS

Visual Media Division Global CS Team

Quality Assurance Group

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2. Product Specifications

1 Specifications

Item	Description	
	LTM1575W	LTM1775W
LCD Panel	TFT-LCD panel, RGB vertical stripe, normaly white, 15-Inch viewable, 0.2895 mm pixel pitch	TFT-LCD panel, RGB vertical stripe, normaly white, 17-Inch viewable, 0.2895 mm pixel pitch
Scanning Frequency	Horizontal : 30 kHz ~ 61 kHz (Automatic) Vertical : 56 Hz ~ 75 Hz (Automatic)	
Display Colors	16.2 Million colors	
Maximum Resolution	Horizontal : 1280 Pixels Vertical : 768 Pixels	
Input Video Signal	Analog 0.7 Vp-p ± 5% positive at 75 Ω, internally terminated	
Input Sync Signal	Type : Seperate H/V Level : TTL level	
Maximum Pixel Clock rate	80 MHz	80 MHz
Active Display Horizontal/Vertical	368.0 mm / 236.0 mm	370.560 mm / 222.336 mm
AC power voltage & Frequency	AC 90 ~ 264 Volts, 60 / 50 Hz ± 3 Hz	
Power Consumption	50 W (Max)	53 W (Max)
Dimensions Unit (W x D x H) Carton (W x D x H)	 19.6 x 8.0 x 14.7 Inches (498 x 204.5 x 374 mm) 22.5 x 17.4 x 10.6 Inches (571 x 441 x 269 mm)	 21.1 x 8.0 x 15.8 Inches (536 x 204.5 x 402 mm) 24.0 x 18.3 x 10.6 Inches (609 x 465 x 269 mm)
Weight	3.95 Kg (8.7 lbs)	4.8 Kg (10.6 lbs)
Environmental Considerations	Operating Temperature : 50 °F ~ 104 °F (10 °C ~ 40 °C) Humidity : 10 % ~ 80 % Storage Temperature : -4 °F ~ 113 °F (-20 °C ~ 45 °C) Humidity : 5 % ~ 95 %	
TV System	Tunning	Frequency Synthesize
	System	NTSC-M
	Sound	STEREO
Antena Input	75Ω, Coaxial Cable	
Sound Characteristic	– MAX Internal speaker Out : Right => 3W Left => 3W	Right => 5W Left => 5W
	– BASS Control Range : -12 dB~ + 12 dB – TREBLE Control Range : -12 dB~ + 12 dB – Headphone Out: 5mW max (400m Vrms) – Output Frequency : RF => 80 Hz ~ 15 kHz A/V => 80 Hz ~ 15 kHz	

2 Pin Assignments

2-1 D-SUB

Pin	Separate
1	Red
2	Green
3	Blue
4	GND
5	GND (DDC Return)
6	GND-Red
7	GND-Green
8	GND-Blue
9	No Connection
10	GND-Sync./Self Test
11	GND
12	DDC Data
13	H-Sync.
14	V-Sync.
15	DDC Clock

2-2 DVD, DTV

RCA Green	Y
	GND
RCA Blue	Pb (Cb)
	GND
RCA Red	Pr (Cr)
	GND
RCA White	Audio L
	GND
RCA Red	Audio R
	GND

2-3 S-Video

Pin	Separate
1	GND
2	Y
3	C
4	GND
5	GND

2-4 A/V

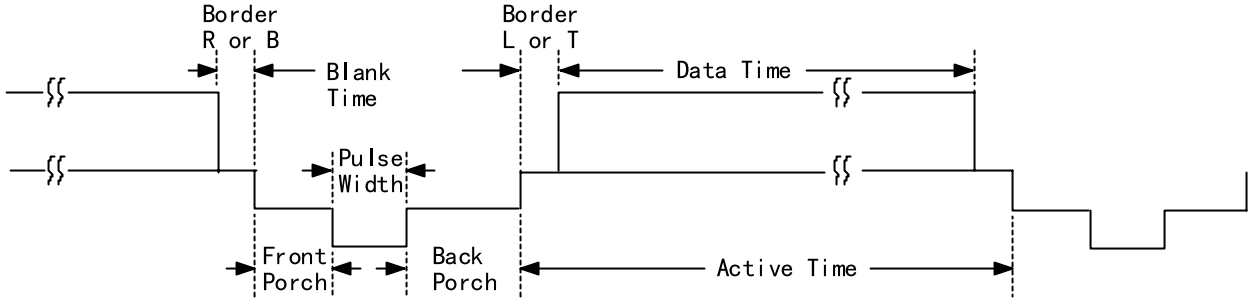
RCA Yellow	CVBS
RCA White	Audio L
	GND
RCA Red	Audio R
	GND

3 Timing Chart

This section of the service manual describes the timing that the computer industry recognizes as standard for computer-generated video signals.

3-1 LCD Panel Mode : 1 mode

Timing No. Originator Mode Name Resolution (HxV)	 1280/60Hz 1280x768
HORIZONTAL Frequency Total time Active time Blank time Border (L / R) Data time Front porch Sync. width Back porch Sync. polarity	 47.700kHz 20.964μs 15.973μs 4.992μs 0.000μs 15.964μs 0.799μs 1.697μs 2.496μs Negative
VERTICAL Frequency Total time Active time Blank time Border (T / B) Data time Front porch Sync. width Back porch Sync. polarity	 60Hz 16.667ms 16.101ms 0.566ms 0.000ms 16.101ms 20.964ms 62.893ms 482.180 Positive
Dot Clock	80.136MHz
Sync. Type Scan Type*	Separate N/I



3-2 Supported Modes (1)

Timing No.	2	3	11	17	32
Originator	IBM	IBM	VESA	VESA	MAC
Mode Name	VGA2	VGA3	640/72Hz	640/75Hz	640/67Hz
Resolution (HxV)	720x400	640x480	640x480	640x480	640x480
HORIZONTAL					
Frequency	31.469kHz	31.469kHz	37.861kHz	37.500kHz	35.000kHz
Total time	31.777µs	31.778µs	26.413µs	26.667µs	28.571µs
Active time	26.058µs	26.058µs	20.825µs	20.317µs	21.164µs
Blank time	5.720µs	5.720µs	5.588µs	6.350µs	7.407µs
Border (L / R)	0.318µs	0.318µs	0.254µs	0.000µs	0.000µs
Data time	25.422µs	25.422µs	20.317µs	20.317µs	21.164µs
Front porch	0.318µs	0.318µs	0.508µs	0.508µs	2.116µs
Sync. width	3.813µs	3.813µs	1.270µs	2.032µs	2.116µs
Back porch	1.589µs	1.589µs	3.810µs	3.810µs	3.175µs
Sync. polarity	Negative	Negative	Negative	Negative	Negative
VERTICAL					
Frequency	70.087Hz	59.940Hz	72.809Hz	75.000Hz	66.667Hz
Total time	14.268ms	16.683ms	13.735ms	13.333ms	15.000ms
Active time	13.155ms	15.761ms	13.100ms	12.800ms	13.714ms
Blank time	1.113ms	0.922ms	0.635ms	0.533ms	1.286ms
Border (T / B)	0.222ms	0.254ms	0.211ms	0.000ms	0.000ms
Data time	12.711ms	15.253ms	12.678ms	12.800ms	13.714ms
Front porch	0.191ms	0.064ms	0.026ms	0.027ms	0.086ms
Sync. width	0.064ms	0.064ms	0.079ms	0.080ms	0.086ms
Back porch	0.858ms	0.794ms	0.528ms	0.427ms	1.114ms
Sync. polarity	Positive	Negative	Negative	Negative	Negative
Dot Clock	28.322MHz	25.175MHz	31.500MHz	31.500MHz	30.240MHz
Sync. Type	Separate	Separate	Separate	Separate	Separate
Scan Type*	N/I	N/I	N/I	N/I	N/I

3-2 Supported Modes (2)

Timing No.	13	14	18	33	15
Originator	VESA	VESA	VESA	MAC	VESA
Mode Name	800/60Hz	800/72Hz	800/75Hz	832/75Hz	1024/60Hz
Resolution (HxV)	800x600	800x600	800x600	832x624	1024x768
HORIZONTAL					
Frequency	37.879kHz	48.077kHz	46.875kHz	49.726kHz	48.363kHz
Total time	26.400µs	20.800µs	21.333µs	20.110µs	20.677µs
Active time	20.000µs	16.000µs	16.162µs	14.524µs	15.754µs
Blank time	6.400µs	4.800µs	5.171µs	5.171µs	4.923µs
Border (L / R)	0.000µs	0.000µs	0.000µs	0.000µs	0.000µs
Data time	20.000µs	16.000µs	16.162µs	14.524µs	15.754µs
Front porch	1.000µs	1.120µs	0.323µs	0.559µs	0.369µs
Sync. width	3.200µs	2.400µs	1.616µs	1.117µs	2.092µs
Back porch	2.200µs	1.280µs	3.232µs	3.910µs	2.462µs
Sync. polarity	Positive	Positive	Positive	Positive	Negative
VERTICAL					
Frequency	60.317Hz	72.188Hz	75.000Hz	74.551Hz	60.004Hz
Total time	16.579ms	13.853ms	13.333ms	13.414ms	16.666ms
Active time	15.840ms	12.480ms	12.800ms	12.549ms	15.880ms
Blank time	0.739ms	1.373ms	0.533ms	0.864ms	0.786ms
Border (T / B)	0.000ms	0.000ms	0.000ms	0.000ms	0.000ms
Data time	15.840ms	12.480ms	12.800ms	12.549ms	15.880ms
Front porch	0.026ms	0.770ms	0.021ms	0.020ms	0.062ms
Sync. width	0.106ms	0.125ms	0.064ms	0.060ms	0.124ms
Back porch	0.607ms	0.478ms	0.448ms	0.784ms	0.600ms
Sync. polarity	Positive	Positive	Positive	Positive	Negative
Dot Clock	40.000MHz	50.000MHz	49.500MHz	49.500MHz	65.000MHz
Sync. Type	Separate	Separate	Separate	Separate	Separate
Scan Type*	N/I	N/I	N/I	N/I	N/I

3-2 Supported Modes (3)

Timing No.	16	19
Originator	VESA	VESA
Mode Name	1024/70Hz	1024/75Hz
Resolution (HxV)	1024x768	1024x768
HORIZONTAL		
Frequency	56.476kHz	60.023kHz
Total time	17.707µs	16.660µs
Active time	13.653µs	13.003µs
Blank time	4.053µs	3.777µs
Border (L / R)	0.000µs	0.000µs
Data time	13.653µs	13.003µs
Front porch	0.320µs	0.323µs
Sync. width	1.813µs	1.219µs
Back porch	1.920µs	2.235µs
Sync. polarity	Negative	Positive
VERTICAL		
Frequency	70.069Hz	75.029Hz
Total time	14.272ms	13.328ms
Active time	13.599ms	12.795ms
Blank time	0.672ms	0.533ms
Border (T / B)	0.000ms	0.000ms
Data time	13.599ms	12.795ms
Front porch	0.053ms	0.017ms
Sync. width	0.106ms	0.050ms
Back porch	0.513ms	0.466ms
Sync. polarity	Negative	Positive
Dot Clock	75.000MHz	78.750MHz
Sync. Type	Separate	Separate
Scan Type*	N/I	N/I

3. Factory Mode Adjustments

1 Entering Factory Mode

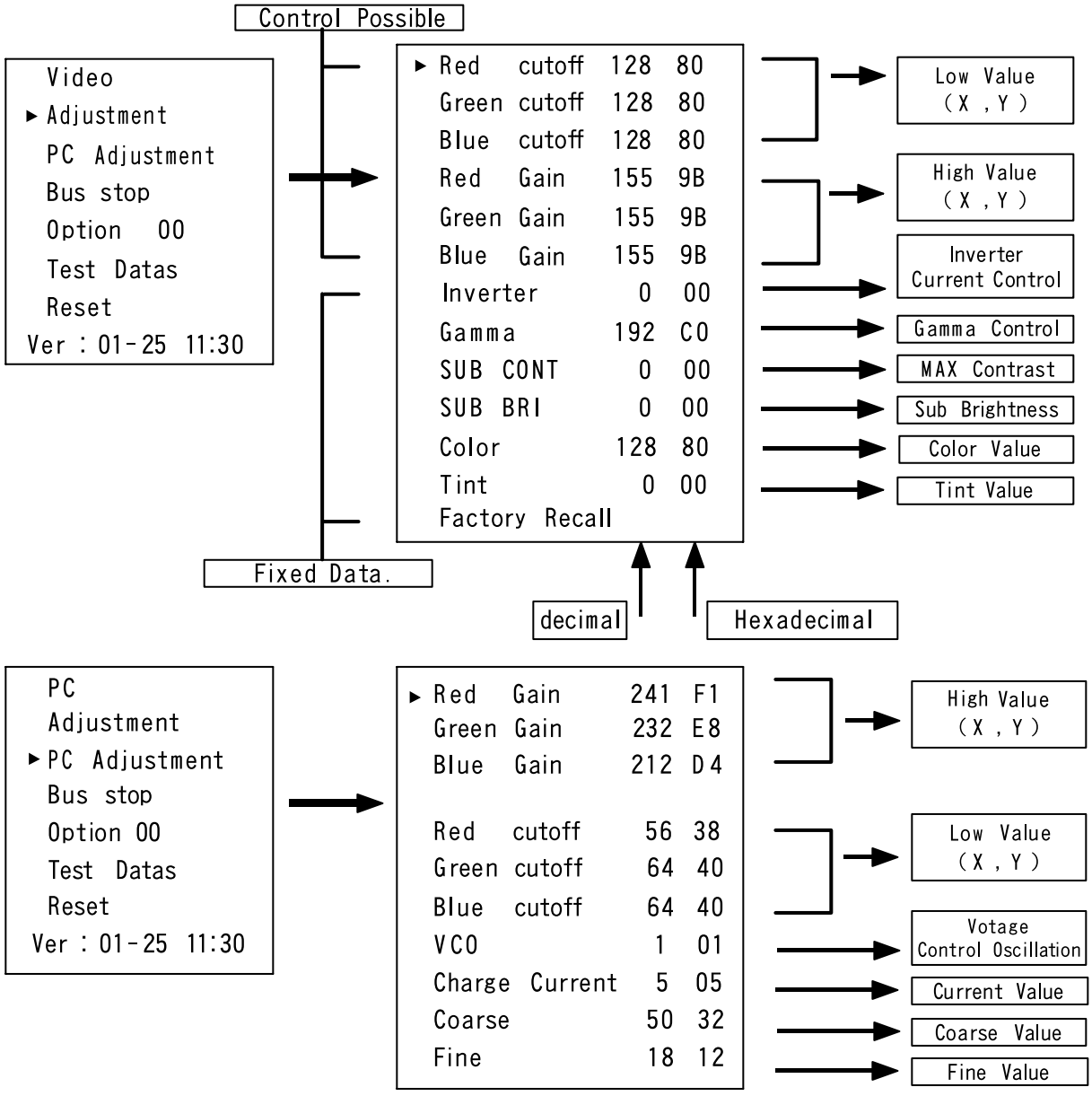
1. To enter “Service Mode” Press the remote -control keys in this sequence :
   - If you do not have Factory remote - control

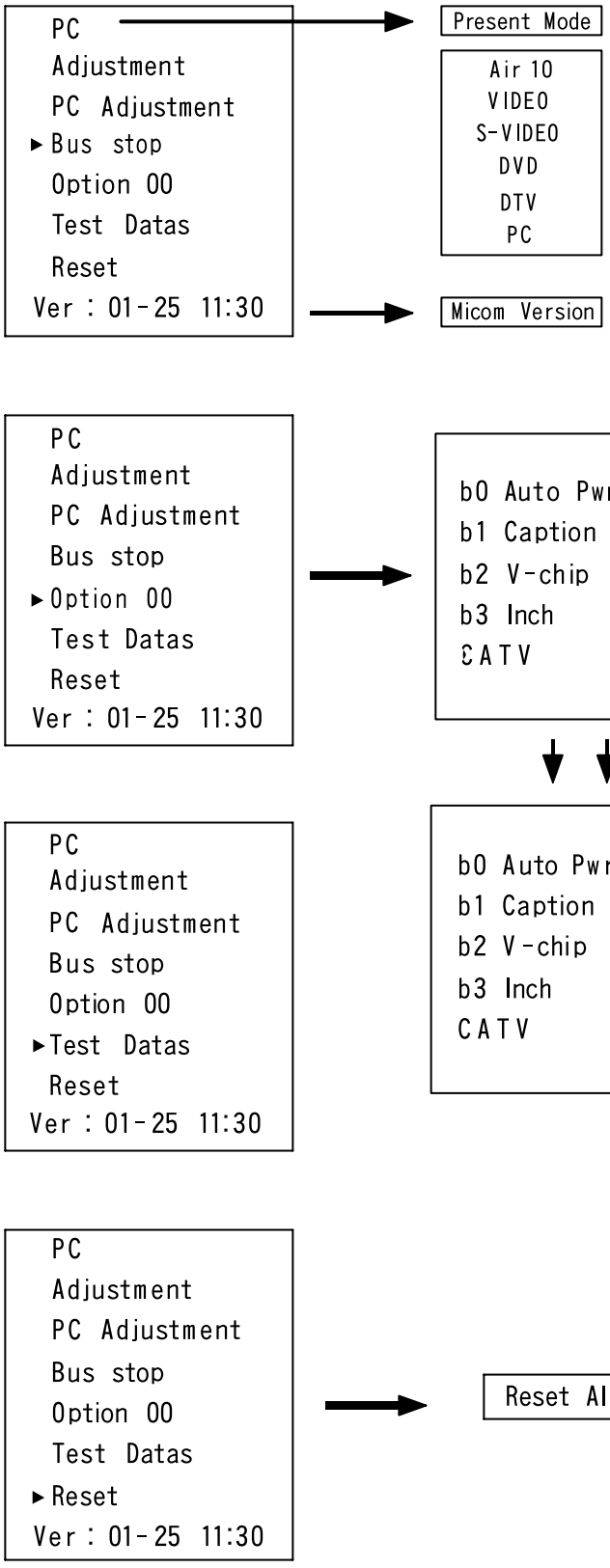
PICTURE OFF → MUTE → 1 → 8 → 2 → Power ON

   - If you have Factory remote - control

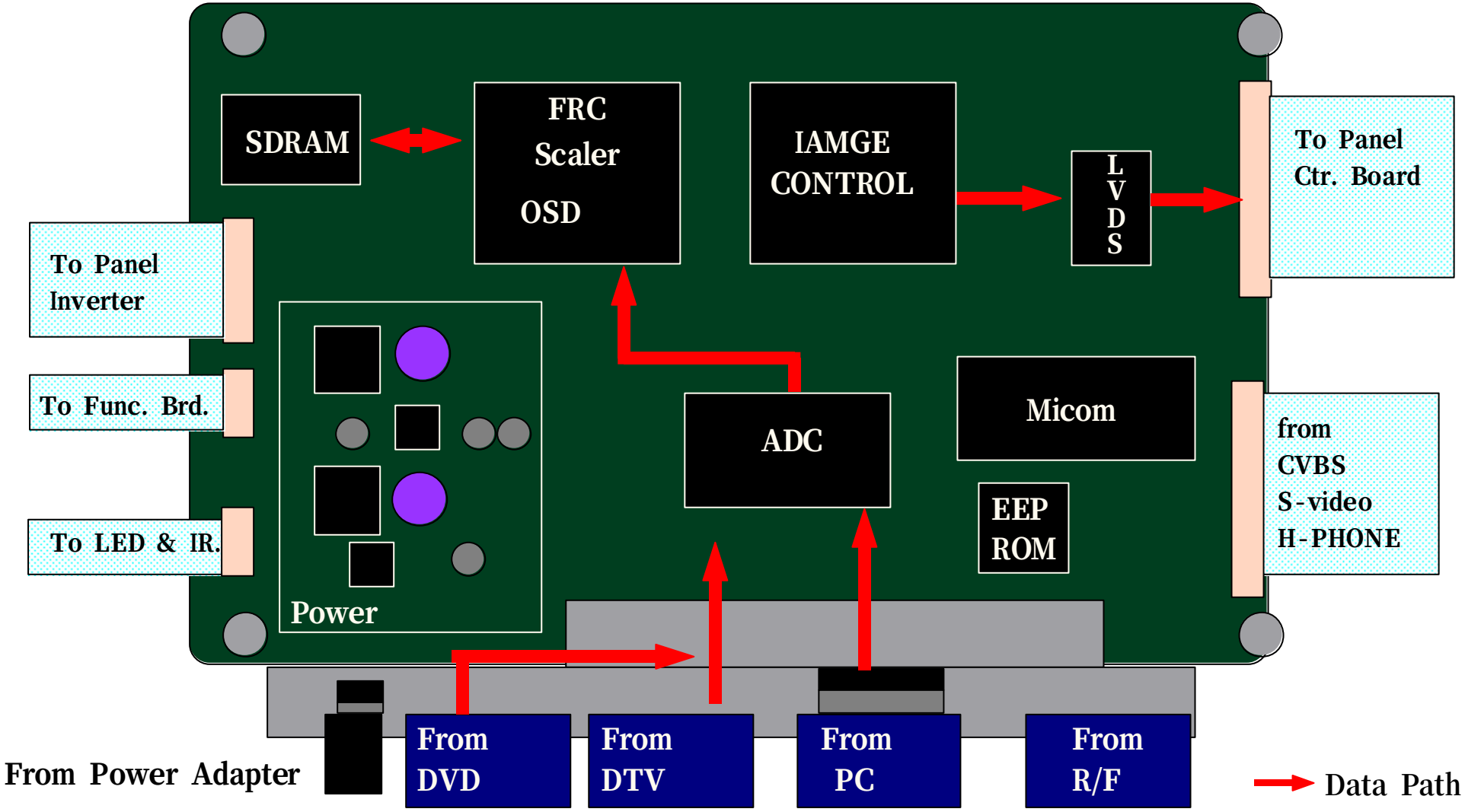
PICTURE ON → DISPLAY → FACTORY

2 Factory Mode Tree

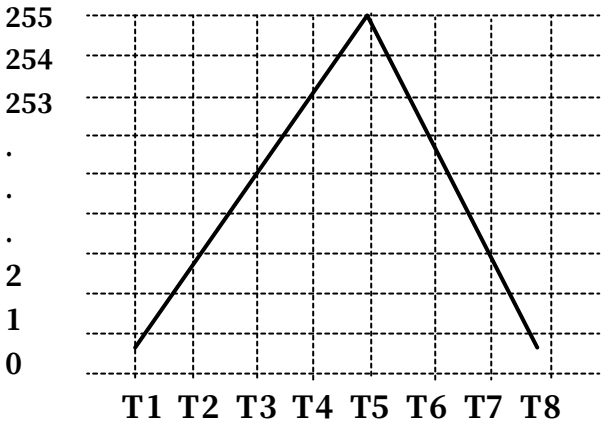



PC
Adjustment
PC Adjustment
▶Bus stop
Option 00
Test Datas
Reset
Ver : 01-25 11:30
Present Mode
Air 10
VIDEO
S-VIDEO
DVD
DTV
PC
Micom Version
PC
Adjustment
PC Adjustment
Bus stop
▶Option 00
Test Datas
Reset
Ver : 01-25 11:30
b0 Auto Pwr : Off
b1 Caption : On
b2 V-chip : Off
b3 Inch : 17 Inch
CATV : STD/HRC/IRC
b0 Auto Pwr : On or Off
b1 Caption : On or Off
b2 V-chip : On or Off
b3 Inch : 17 Inch or 15 Inch
CATV : STD/HRC/IRC or STD/HRC/AFN
PC
Adjustment
PC Adjustment
Bus stop
Option 00
▶Test Datas
Reset
Ver : 01-25 11:30
PC
Adjustment
PC Adjustment
Bus stop
Option 00
Test Datas
▶Reset
Ver : 01-25 11:30
Reset All Mode Data

■ The Block diagram of TFT-LCD Monitor Main Board



■ Analog To Digital Converting



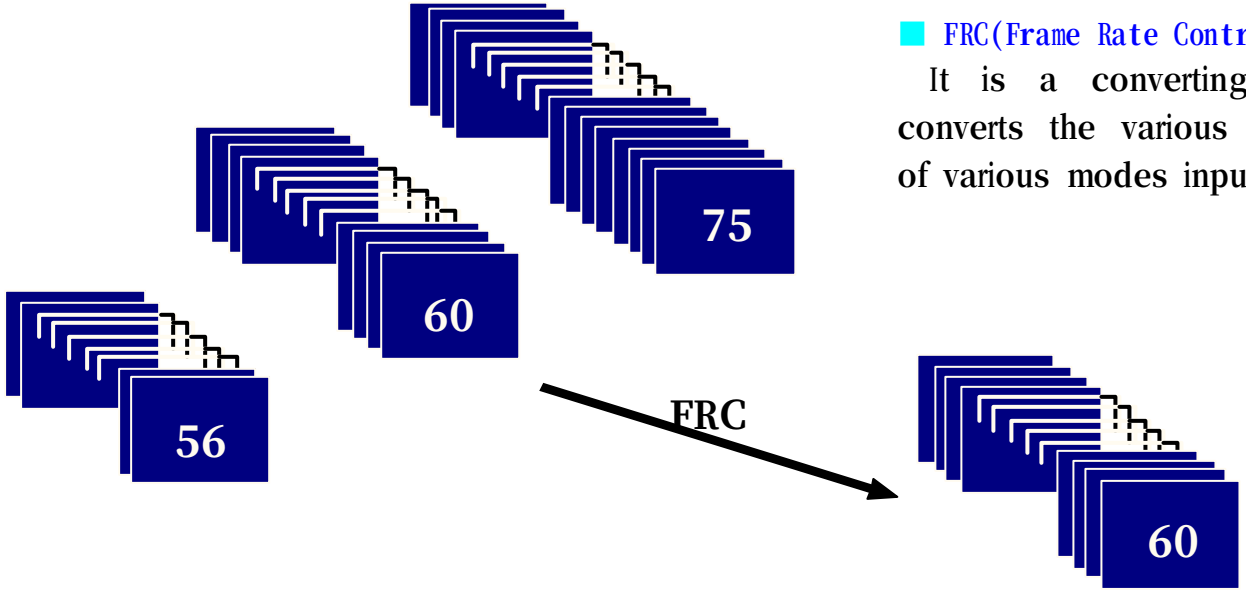
ADC

T1 : 0
T2 : 2
.
.
T5 : 255
.
.
T7 : 2

■ ADC(Analog to Digital Converter)

It is a device to convert analog signal to digital signal and applied 80MHz-120MHz

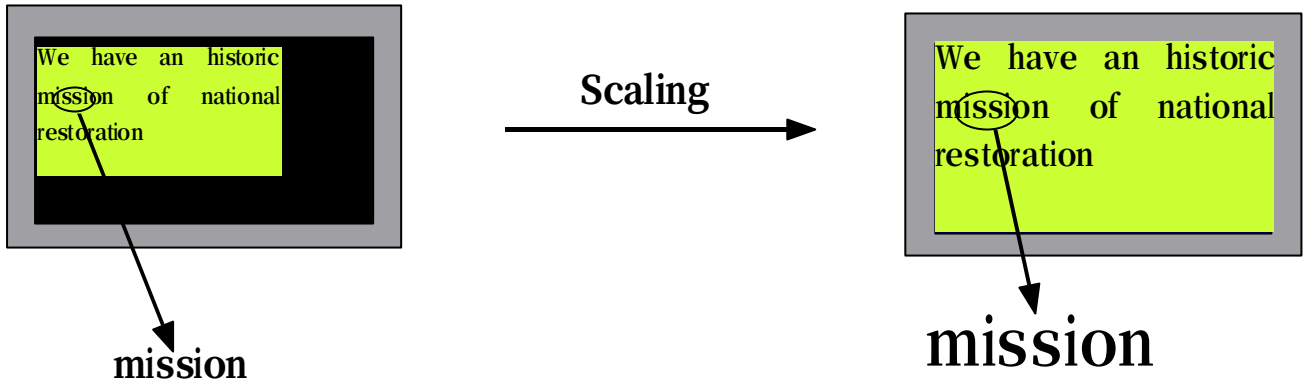
■ FRC(Frame Rate Conversion):



■ FRC(Frame Rate Controller) :

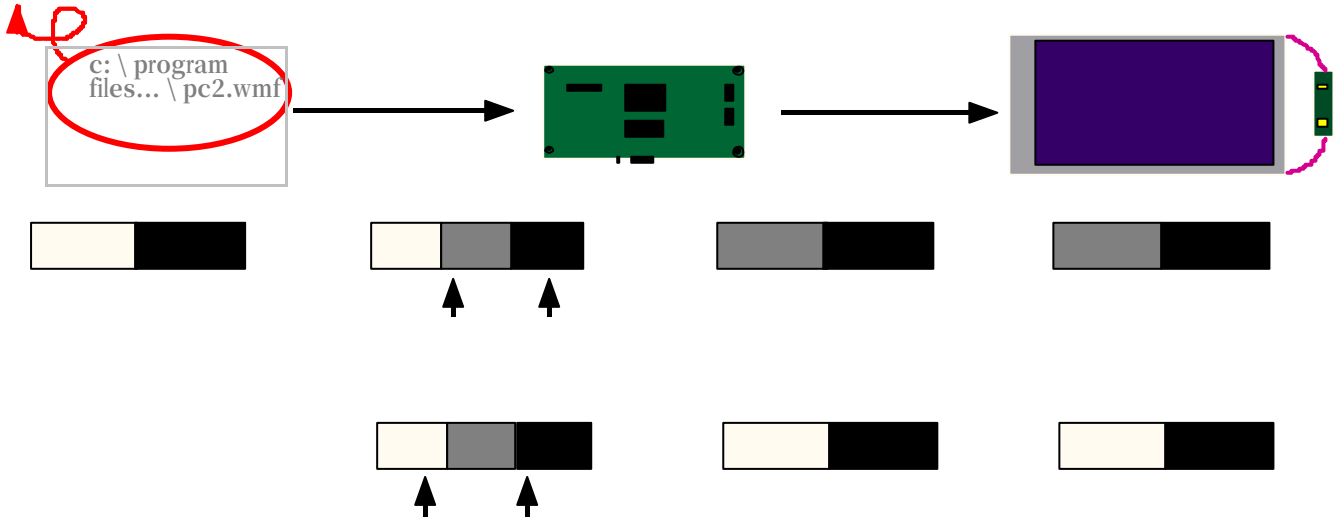
It is a converting part/method that constantly converts the various vertical frequencies (50-95Hz) of various modes inputted in diversity.

■ **Scaling concept: It converts the resolution signal inputted in various forms to WXGA 1280x768**



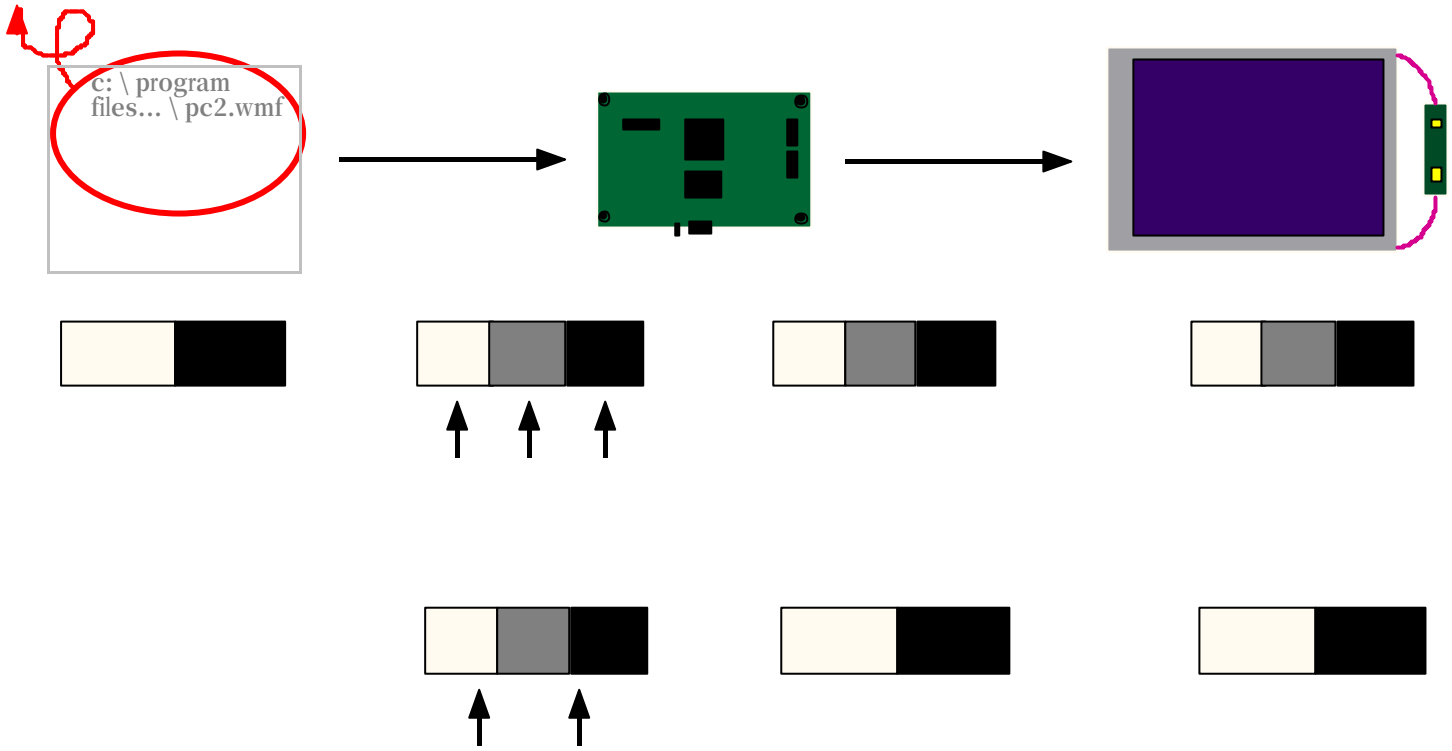
■ Image Scaler :
A technique to change the inputted resolution to the other resolution.
(EX. 640x480 → 1024x768)

■ **Fine adjustment**



■ FINE :
Adjustment of the monitor's distinction by adjusting the positional difference between video signal and video clock.

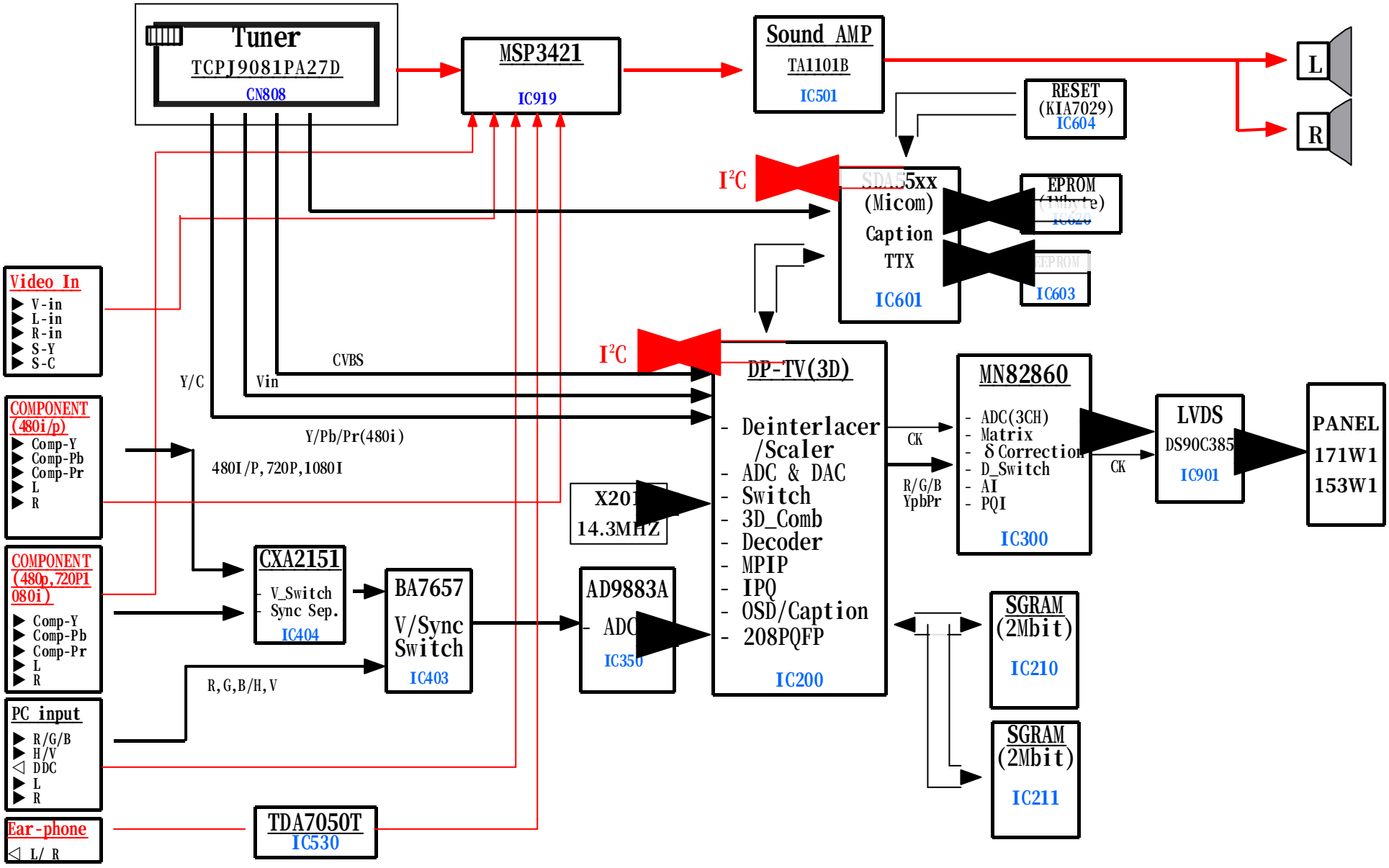
■ Adjustment of Coarse

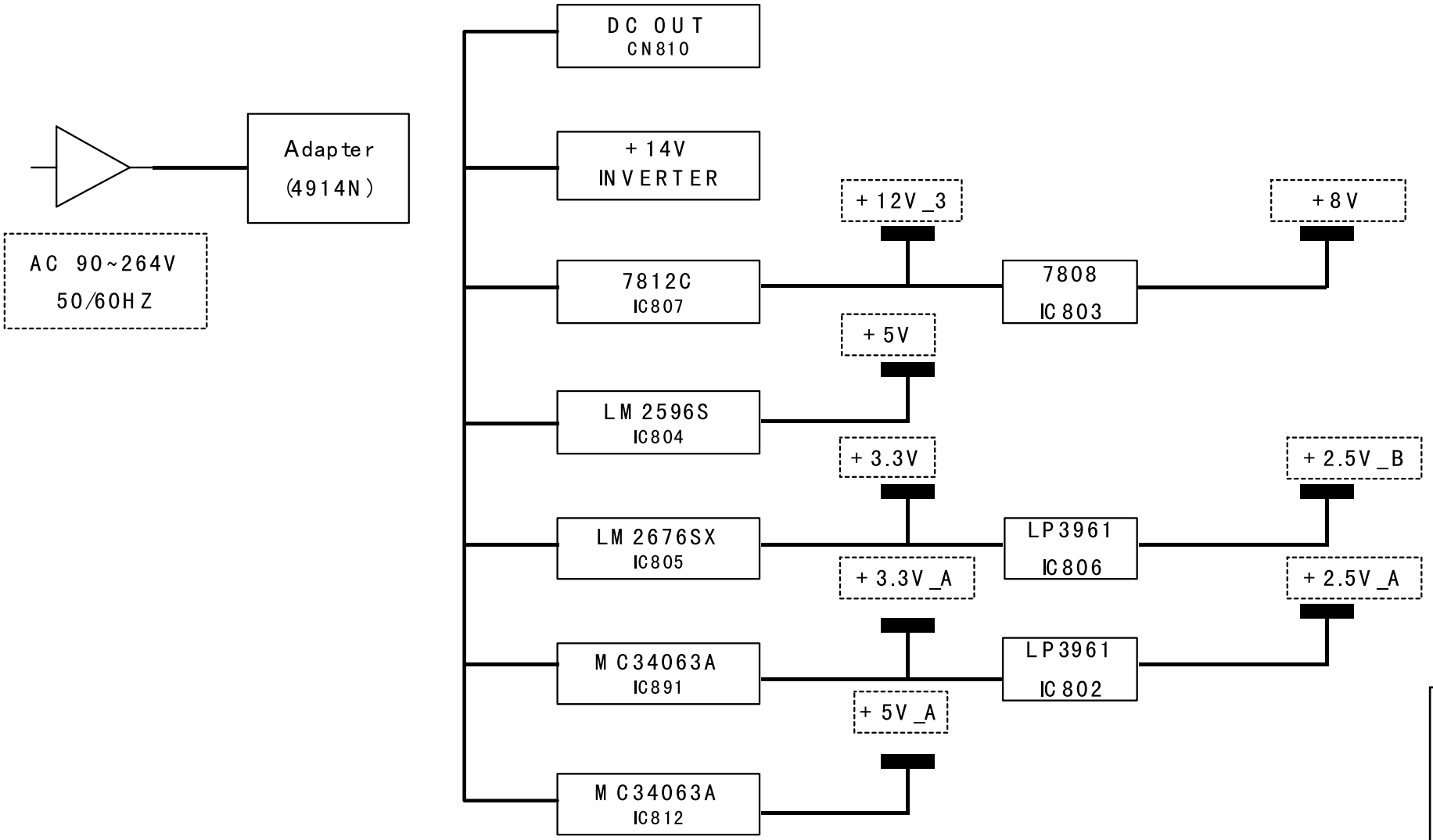


■ COARSE :

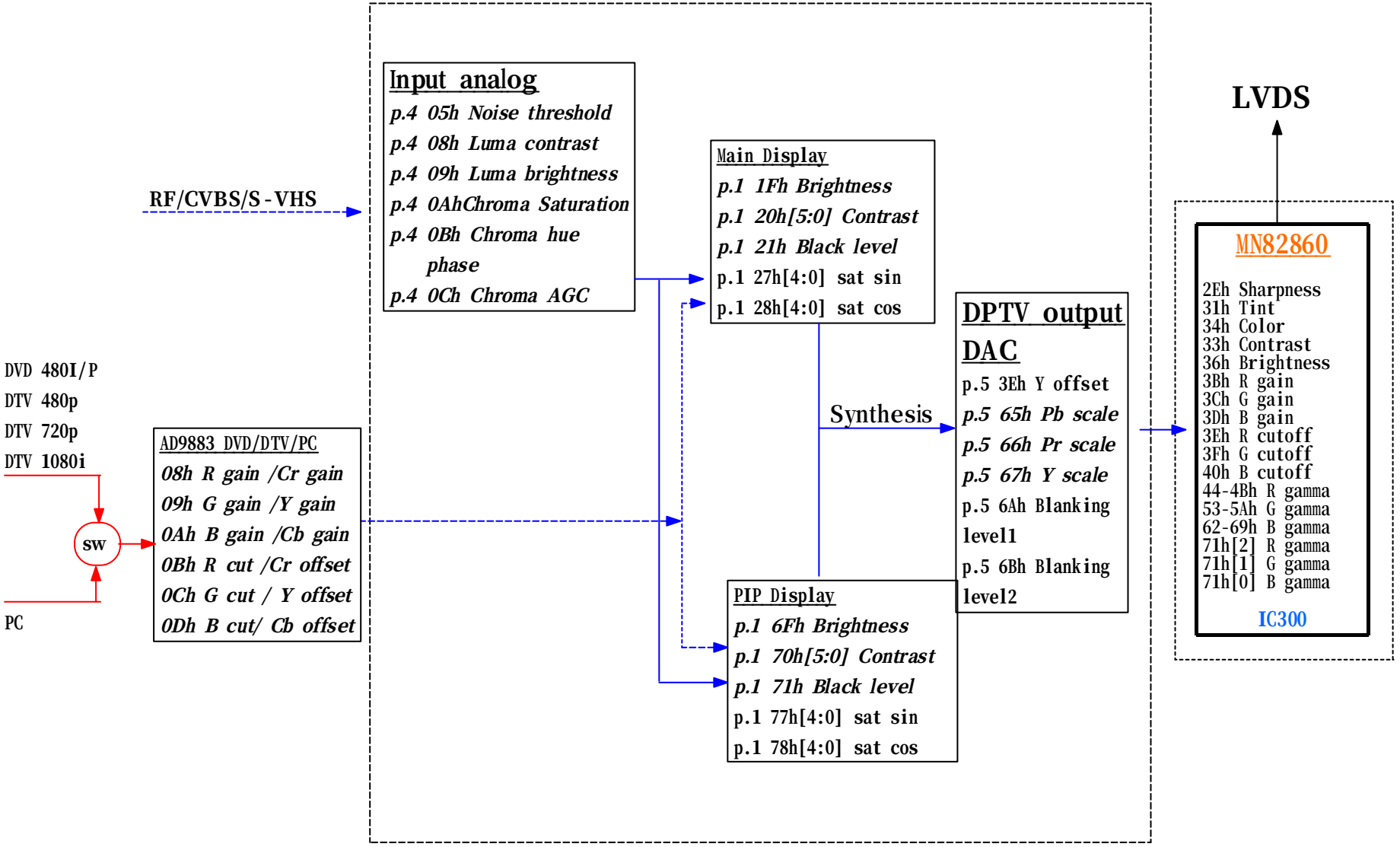
(Fine adjustment of a video clock for matching video clocks occurred between inputted video band and PLL)

NIKE-LCD TV NTSC BLOCK DIAGRAM




AC 90~264V
50/60HZ
Adapter
(4914N)
DC OUT
CN810
+14V
INVERTER
7812C
IC807
+12V_3
7808
IC803
+8V
LM2596S
IC804
+5V
LM2676SX
IC805
+3.3V
LP3961
IC806
+2.5V_B
+3.3V_A
MC34063A
IC891
LP3961
IC802
+2.5V_A
+5V_A
MC34063A
IC812

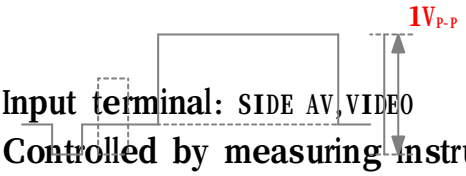
■ NIKE LCD-TV NTSC adjustment RESISTOR



1. Full white level setting

1) Pattern in use: full white (100% IRE)

(1) CVBS (Measured at AV JECK)



(2) Input terminal: SIDE AV, VIDEO

(3) Controlled by measuring instrument : video gain 140%(100%IRE)

-When video gain is 100%, it is 70%IRE.

(TOCHIBA PATTERN)

2) MN82860 GAMMA : OFF

(1) iw dc 71 07 — GAMMA DATA(GAMMA OFF)

iw dc 71 00 — GAMMA ON

Order — MN82860 SLAVE ADRESS

MN82860 SUB ADRESS

3) Highlight adjustment (x:282 y:283 T:10,000K)

(1) Pattern adjustment : FULL WHITE PATTERN (VIDEO GAIN 140%)

-.After it is inputted at chassis to panel with RGB Full Gain, it can be adjusted to the coordinates where you wish by using CA110.

(2) Adjustment address and adjustment

iw dc 3e ?? -->RED GAIN (X value adjustment)

iw dc 3f ?? -->GREEN GAIN (Y value adjustment)

iw dc 40 FF -->BLUE GAIN (Y value adjustment) -->FIX

-.The ratio of input/output is outputted 1:1 at MN82860 when RGB gain value is FF.

-.Among characters of the RGB reproduction, a character of blue reproduction is the lowest. If you want to have white coordinates, you must output the blue higher at chassis.

(3) The reason why gamma has to be off at 2)

-The RGB Gain has to be adjusted in the state of gamma-Off because the MN82860 gamma correction is located at the end of column after adjustment of RGB cut-off and gain.

-.After the gamma correction is set finally, the RGB Gain has to be adjusted in the state of gamma-On for production.

2. Set the low light level

1) Pattern in use: Toshiba ABL pattern Low Light Area

(1)Turn On the gamma correction of NM82860.(iw dc 71 00)

-There was a trial and error. In the state of gamma-off, the Toshiba pattern's cut-off is broken down because the gray pattern touches the gamma.

Therefore, it is necessary to align the Cut-off of the Toshiba pattern to the first/second row of the gray pattern. However, do not touch the data of cut-off when you adjust the gray pattern. (Please, refer to the previous page for data address of cut-off)

Therefore, for the adjustment, turn on the gamma.

(2)Adjustment of Low-light(x:282 y:283 Y: about 4.5 (10.000k)-->

Until the 6th row of the Toshiba pattern can be seen)

iw dc 3b ?? -->RED CUT-OFF (x value adjustment)

iw dc 3c ?? -->GREEN CUT-OFF (y value adjustment)

iw dc 3d 80 -->BLUE CUT-OFF (Y value adjustment) -->FIX

-Set the blue to maximum due to its low reproduction.

(3)Adjustment with ignoring the highlight data

- The maximum luminance is determined with IRE 100% full white pattern.

-The highlight luminance of the Toshiba ABL pattern cannot be maximum luminance due to its luminance is IRE 70%.

3.Final Adjustment Method

1)Repeat the adjustment of 1 and 2 till it is matched with adjustment spec. Nevertheless, the output voltage [1V~0.9V] has to be measured with scope when moving to the full white, and then adjust the gain. (Refer to the 1.)

Method of the panel gamma setting

1)Set the maximum value not to occur the white saturation in panel by using out sources such as DVD, etc.

(1)17": A0

(2)15": D0

4.Method of the RGB gamma setting

1)Pattern in use : 100%IRE의 GREY-SCALE PATTERN

2)Adjustment of sub address : MN82860

(1)GREEN GAMMA GAIN FIX : ALL 40

(2) R, G, and B data about the sub address (Green is fixed, so adjust read and blue)

SUB ADDRESS	RED	SUB ADDRESS	BLUE	SUB ADDRESS	GREEN
44		62		53	40
45		63		54	40
46		64		55	40
47		65		56	40
48		66		57	40
49		67		58	40
4A		68		59	40
4B		69		5A	40

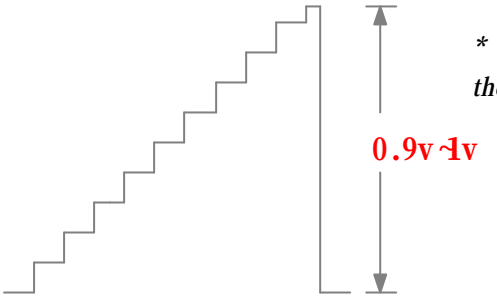
FIX

3)The adjustment sequence of the gray scale

(1) Drive the 11 gray patterns

(2) Measured the input/output gain voltage (Adjust the video gain to 100%)

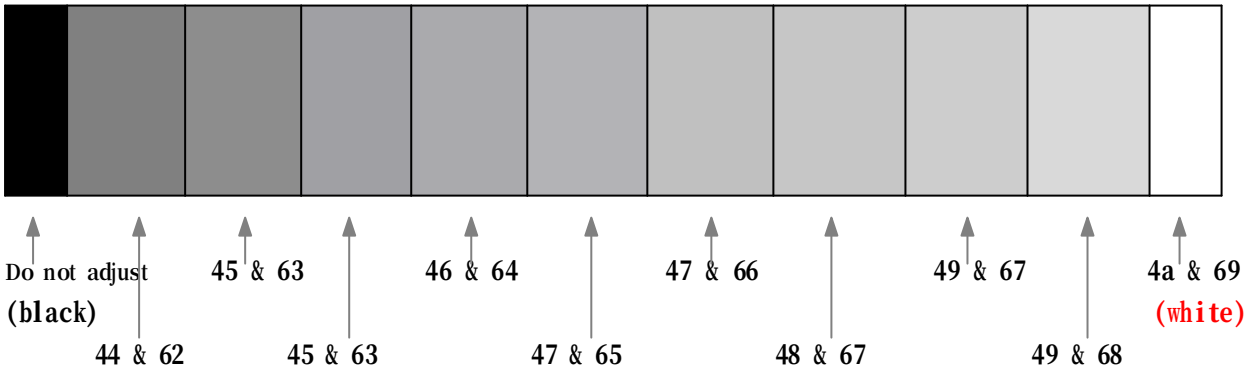
-->point :dptv의 G-OUT (R315)



** As mentioned above, check the gain voltage when you change the pattern, then adjust. **

(3)After perform the factory mode, spread the gamma data.(iw dc 71 00) (4)Adjust the each steps to match with the adjustment spec (x:282, y:283)

-Adjust by using the sub address in the above.



-When you adjust the each step, do not affect to the next steps.

(Example: When adjusting the cut-off row, the flowing rows get effects. You may know when you give ff to the data.)

(5) Confirm whether the cut-off is matched or not in Toshiba pattern.

- It has to be confirmed because the cut-off is a little bit twisted when adjusting the gray scale. If it is not matched to the adjustment spec, repeat the step (2) of 2. After adjustment, return to the gray scale and perform the fine adjustment for each step.

(The values are already adjusted, so there will not be big differences.)

-Adjust the Toshiba pattern and gray scale pattern repeatedly.

-After finished the adjustment, check it in the Full-white pattern.

(Do not forget to measure the gain voltage.)

If white is twisted, repeat the above. (Gamma off in full white)

3.FACTORY MODE시 MICOM SETTING

-MODE:DYNAMIC MODE / COOL

BLUE FIX

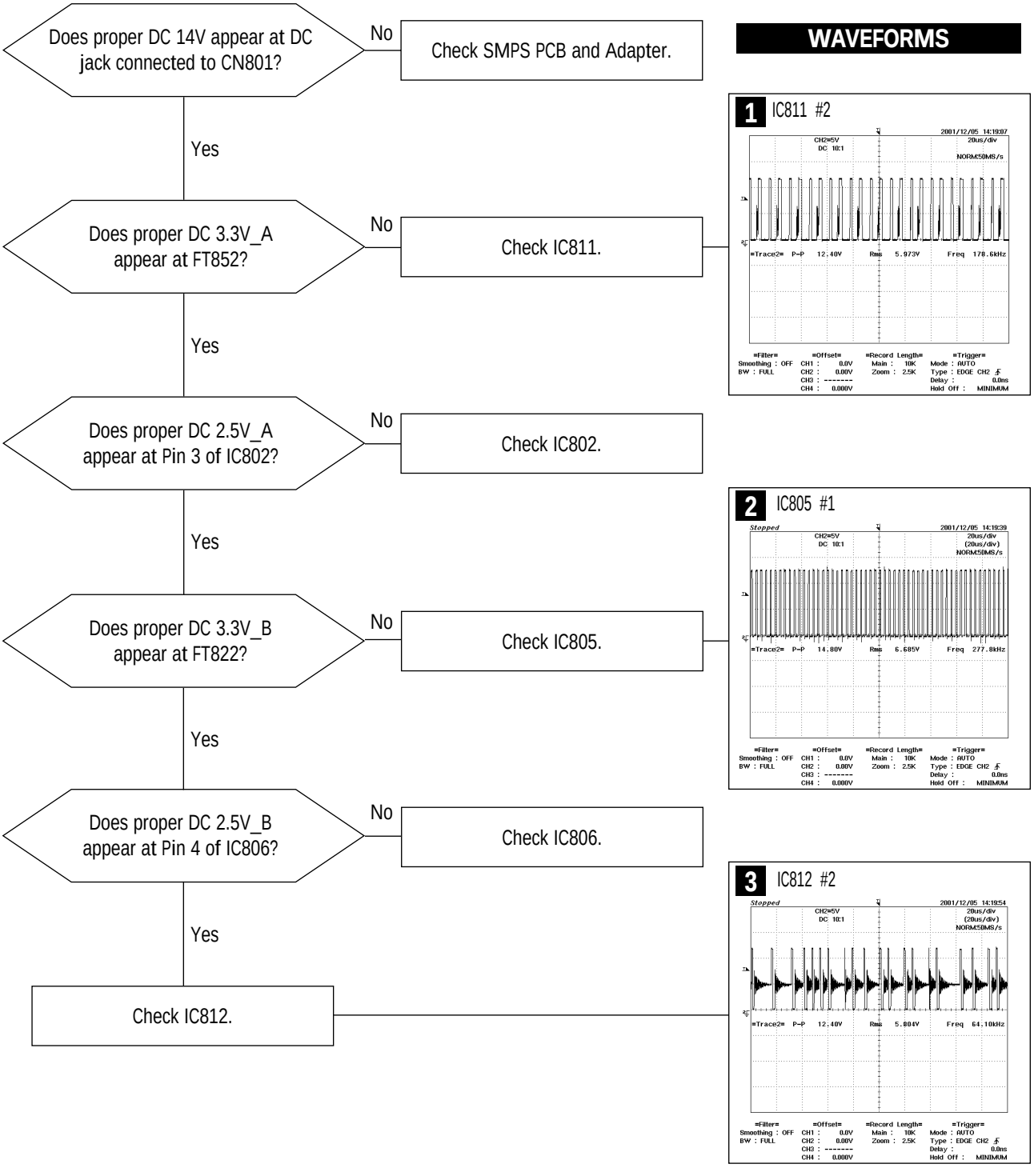
CONTRAST:80 ,BRIGHTNESS:50

2.Gamma Correction Setting
1)MN82860 Gamma Correction Setting

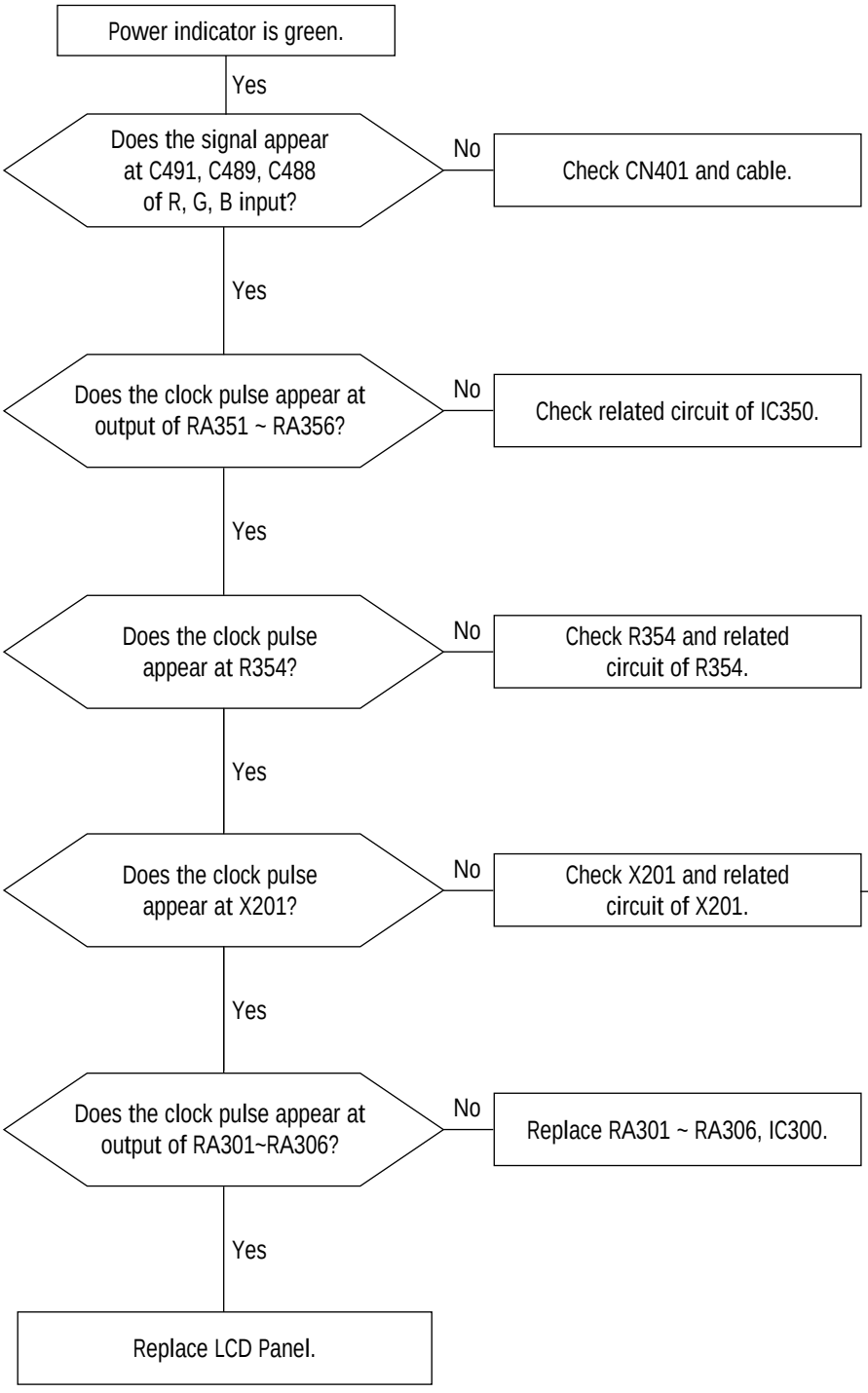
Sub-address	Gamma Correction (17")					Gamma Correction (15")						Remarks
	Spl1	Spl2	Spl3	Spl4	Spl5	Spl1	Spl2	Spl3	Spl4	Spl5		
33h'	95					A0						Contrast control
36h'	1C					10						Brightness Control
3Bh'	E1					DD						Red Gain
3Ch'	C7					C8					RGB Gain Control	Green Gain
3Dh'	FF					FF						Blue Gain
Y cd/m2	98.1											Condition of the full white gamma off
3Eh'	7E					86						Red Cut-off
3Fh'	75					77					RGB Cut-off Control	Green Cut-off
40h'	80					80						Blue Cut-off
Y cd/m	2.0					3.5						Low light condition of Toshiba ABL pattern
44h'	44					44						Bit[7-0] RTANA R static Gamma gradient setting 1 (=40h' for 1x)
45h'	45					47						Bit[7-0] RTANB R static Gamma gradient setting 2 (=40h' for 1x)
46h'	44					41						Bit[7-0] RTANC R static Gamma gradient setting 3 (=40h' for 1x)
47h'	33					37						Bit[7-0] RTAND R static Gamma gradient setting 4 (=40h' for 1x)
48h'	40					4D					Red Gamma Correction	Bit[7-0] RTANE R static Gamma gradient setting 5 (=40h' for 1x)
49h'	3B					2E						Bit[7-0] RTANF R static Gamma gradient setting 6 (=40h' for 1x)
4Ah'	3D					25						Bit[7-0] RTANG R static Gamma gradient setting 7 (=40h' for 1x)
4Bh'	40					40						Bit[7-0] RTANH R static Gamma gradient setting 8 (=40h' for 1x)
53h'	40					40						
54h'	40					40						
55h'	40					40						
56h'	40					40					Green Gamma Correction	
57h'	40					40						
58h'	40					40						
59h'	40					40						
62h'	37					3F						
63h'	3A					3F						
64h'	40					39						
65h'	33					34						
66h'	42					42					Blue Gamma Correction	
67h'	48					44						
68h'	4F					5F						
69h'	50					3F						

5. Troubleshooting

1 No Power

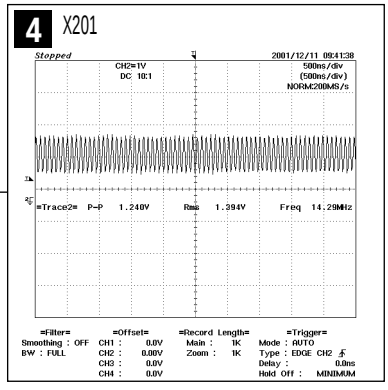


2 No Video (PC Signal)

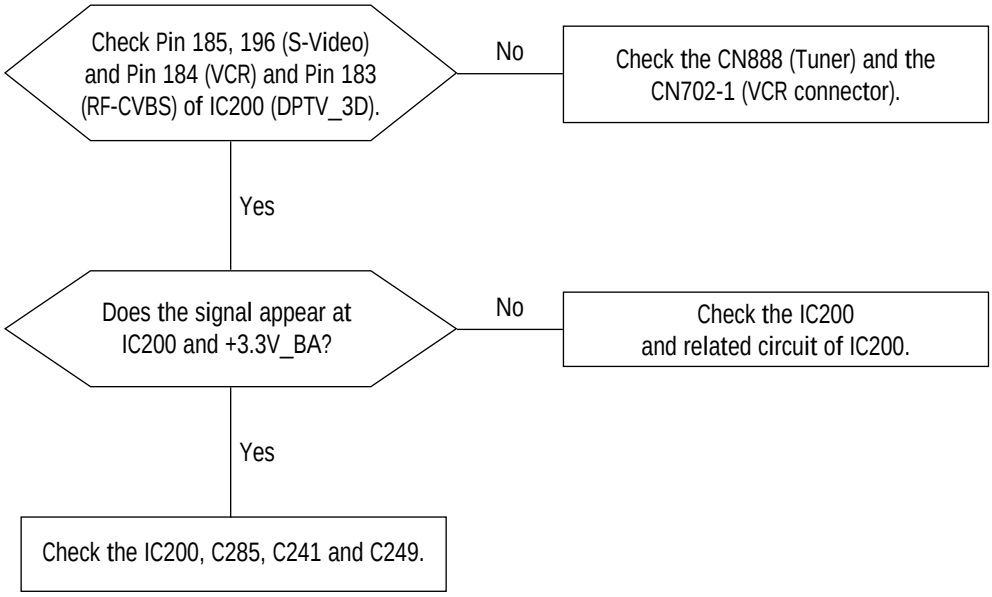


WAVEFORMS

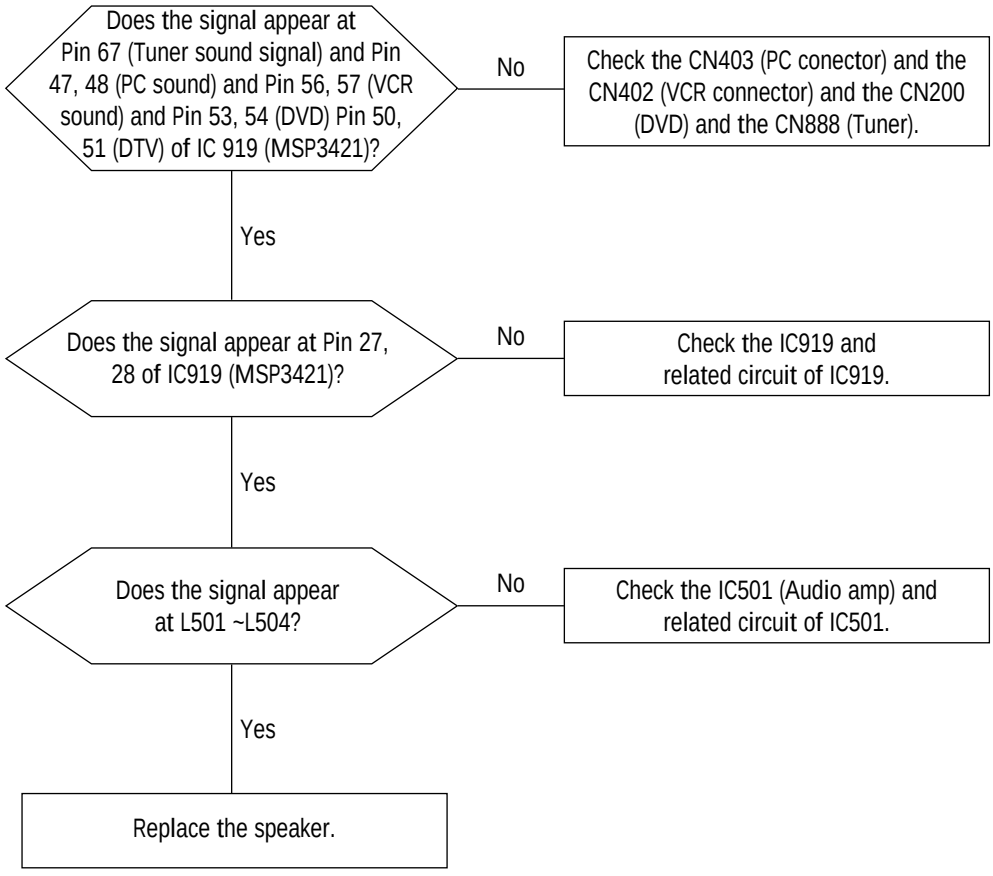
4 X201



3 No Picture (TV, Video, S-Video, DVD, DTV)



4 No Sound


Does the signal appear at Pin 67 (Tuner sound signal) and Pin 47, 48 (PC sound) and Pin 56, 57 (VCR sound) and Pin 53, 54 (DVD) Pin 50, 51 (DTV) of IC 919 (MSP3421)?
No
Check the CN403 (PC conector) and the CN402 (VCR connector) and the CN200 (DVD) and the CN888 (Tuner).
Yes
Does the signal appear at Pin 27, 28 of IC919 (MSP3421)?
No
Check the IC919 and related circuit of IC919.
Yes
Does the signal appear at L501 ~L504?
No
Check the IC501 (Audio amp) and related circuit of IC501.
Yes
Replace the speaker.

Extra

TROUBLESHOOTING

If the TV seems to have a problem, first try this list of possible problems and solutions. If none of these troubleshooting tips apply, call your nearest service center.

Identifying Problems

Problem	Possible Solution
Poor picture	Try another channel. Adjust the antenna. Check all wire connections.
Poor sound quality.	Try another channel. Adjust the antenna.
No picture or sound.	Try another channel. Press the TV/VIDEO button. Make sure the TV is plugged in. Check the antenna connections.
No color, wrong colors or tints.	Make sure the program is broadcast in color. Adjust the picture settings. If the set is moved or turned in a different direction, the power should be OFF for at least 30 minutes. Adjust the antenna.
Picture rolls vertically.	Check all wire connections.
The TV operates erratically.	Unplug the TV for 30 seconds, then try operating it again.
The TV won't turn on.	Make sure the wall outlet is working.
Blurred or snowy picture, distorted sound	Check the direction, location and connections of your aerial. This interference is often due to the use of an indoor aerial.
Remote control malfunctions	Replace the remote control batteries. Clean the upper edge of the remote control (transmission window). Check the battery terminals.
“Check Signal Cable” message.	Ensure that the signal cable is firmly connected to the PC or video sources. Ensure that the PC or video sources are turned on.

TROUBLESHOOTING

Problem	Possible Solution
"Not Supported Mode!" message.	Check the maximum resolution and the frequency of the video Adapter. Compare these values with the data in the Display Modes Timing Chart.
The image is too light or too dark.	Adjust the Brightness and Contrast. Adjust the Fine function.
Horizontal bars appear to flicker, jitter or shimmer on the image.	Adjust the Coarse function and then adjust the Fine function.
Vertical bars appear to flicker, jitter or shimmer on the image.	The TV is using its power management system. Move the computer's mouse or press a key on the keyboard.
Screen is black and power indicator light blinks steadily.	Check that the display resolution and frequency from your PC or video board is an available mode for your TV. On your computer check: Control Panel, Display, Settings.
Image is not stable and may appear to vibrate.	If the setting is not correct, use your computer utility program to change the display settings. NOTE: Your TV supports multiscan display functions within the following frequency domain: • Horizontal frequency: 30 kHz ~ 61 kHz • Vertical frequency: 56 Hz ~ 75 Hz • Maximum refresh rate: 1280 x 768 @ 60 Hz
Image is not centered on the screen.	Adjust the horizontal and vertical position.
You need the Monitor driver software.	Download the driver from WWW pages: http://www.samsungusa.com/monitor

8. General Informations of LCD

1. History of the LCD (Liquid Crystal Display)

LCD, a display device, has been started to adapt for a calculator, display part of watch, and electronic note-book, and nowadays, it is adapted for a PC, Workstation, Liquid crystal color TV, monitor, game device, and so on with a tendency of larger size, larger capacity, and colorization.

Liquid crystal has been starting to use as a display device since R. Williams at RCA co. in 1963 stated that the liquid crystal has the electro-optics effect in the science magazine, "Nature".

After the G. H Heilmeier group of the Sharp presented the first possibility of LCD's practical use in 1968, the first segment type of the DSM style LCD electronic calculator, 'EL-805', was commercialized in 1973. But, it has several problems such as black-and-white display, responding speed, narrow viewing angle, high power consumption for portability, and so on.

☞ Responding speed: It is taking time that LCD element becomes On or Off. When voltage signal from external changes it On to Off or Off to On, a LCD is changed due to the signal. But, it cannot be changed immediately because of the viscosity of the liquid crystal, so time delay for reaching the liquid crystal to equilibrium state is occurred. Such transformational characteristic shows up as an optical characteristic, and the delay time for the optic is called responding time. The responding time is proportional to the viscosity of the liquid crystal and inversely proportional to the cell spacing. When the electronic signal is converted to On/Off, the responding time can be measured from the transmission characteristic in contrast with the time.

☞ Viewing angle: The LCD has a characteristic that the contrast ratio is changed by angle of the viewing point. The changing degree is shown by the viewing angle. The viewing angle is expressed as an angle over than certain value of the contrast ratio according to top, bottom, right, and left position. In a LCD cell, the transmissivity is sharply changed due to the angle of the incoming light. Therefore, in the driving process for turning it On/Off, the contrast ratio is changed because of such change of the transmissivity.

The measuring method of the viewing angle is that determine 0° where eye and a screen become a front view, and measure the gray level (gray1~gray16) at every 25° while rotate a panel to top, bottom, (-60°, +60°) left, and right (-60°, +60°). If you draw the luminance curve due to the viewing angle, the angle from an inversion of the gray scale can be found. The viewing angle range is settled when the C/R value is over 10:1. Generally, the points to decide the picture quality of the LCD are not only the viewing angle, but also the angel of the inverted gray scale.

* LCD electronic calculator of the segment type *

Enterprises of the display market acknowledge the unlimited potential power of the LCD and have needed to develop better LCD with dot matrix display for informational device, which can obtain letter, figure, and various information.

* Segment display and Dot matrix display *

Afterward, TN (Twisted Nematic) style LCD is developed for reducing consumption power. It has weaknesses of contrast, viewing angle, and display grade. Especially, it is not proper for the larger

screen. Therefore, the STN (Super TN) LCD is developed. STN LCD has several merits compare to TN such as higher productive efficiency, suitable for lager screen, wider viewing angle, and higher contrast. The Sharp presented the word processor "WD-250" with STN LCD in 1986. It was the beginning to rapidly distribute the LCD and to develop the word processor and PC.

Nevertheless, the STN LCD uses two display colors, yellow and blue, to get enough luminosity for high contrast. The LCD needs clean white-and-black display color to be regularly substituted for CRT instead of OA. With the reason, DSTN (Double STN) style LCD, displays beautiful black-and-white, is developed in 1987, and it is commercialized.

* STN Color Word processor and DSTN color LCD notebook *

The materialization of the black and white display is opened the way of the gray scale and color display period, and it helps to access to PC following word processor. Afterward, LCD is developed for better conditions such as lighter weight, thinner thickness, higher resolution for larger screen, higher contrast, and wider viewing angle.

☞ The gray scale: It is a display method that the different state exists except On/Off state. The huge amount of information such as color display cannot be displayed with only On/Off drive. In the gray scale display, several middle states exist between an On and Off state. For example, there is gray state between black and white to display information. The gray scale is made by applying middle power between On and Off power in LCD. There are several methods to get a middle value: control the strength of the power, adjust the rage of the power pulse, and so on. The color display is determined by the degree of

the gray scale. With the only On and Off state, just 8 colors can be displayed, but with the gray scale, more colors can be displayed.

The capacity of it is still not as good as CRT.
Because LCD has passive matrix construction, it is not suitable for moving pictures in fact of high quality picture, high contrast, and high-speed response.

Development of the high capacity color LCD is needed for emulating the existing screen. With the reason, TFT (Thin film transistor) LCD of the Active matrix drive method, which is totally different to the passive matrix drive method, is developed.
The new method puts a switch element (TFT) into a picture element to control each picture element. As a result, the TFT LCD has been gotten excellent construction to develop the display quality, contrast, and viewing angle.

After 3" color TV with the TFT_LCD is developed in 1986, LCD has been larger, and technique suitable for the larger size has been developed. At the present, 40" LCD is developed.

Through the continuous efforts for developing LCD for 4 and half centuries, the flat display is made at present.

The strong parts of TFT_LCD compared to CRT are lighter weight, thinner style, and lower power consumption. In the efficiency aspect, the viewing angle, luminance, and contrast are near or even better than CRT. But, price and responding speed is still not so good as the CRT. In case of the viewing angle, if it is 15", left and right is 110° ~160°, top and bottom is 90°~160° which is no problem to watch. The luminance is maximum 200~250cd, and the contrast ratio is 200:1~300:1 which is better than CRT. The responding speed for TFT_LCD is several tens ms (15": 30ms~50ms) and for the STN_LCD is several hundreds ms. For display a moving picture, the frequency of the frame is 60Hz, so it must be 16ms. But, the frequency of

TFT_LCD has to be twice more than STN_LCD to make differences between the signals (On/Off), so it must be under 8ms. Nevertheless, it is a just theoretical numerical value. For driving moving picture, actually it has to be 2 or 3 times faster than that.

☞ Contrast ratio: The contrast ratio(C/R) is the scale to decide whether the image is clearly appeared or not. It will be clearer when the difference of the luminance is bigger. It is defined by dividing the luminance with all pixels white by luminance with all pixels black in the middle front view.
C/R = (Luminance with all pixels white) / (Luminance with all pixels black)
Luminance with all pixels black has lower value than luminance with all pixels white. The value of the contrast ratio has mainly affected by luminance of the black pixels.

In the fact of the industrial economic (another fact to rise the price), the investment efficiency and productivity problem have to be overcome. By developing responding speed of TFT_LCD and productivity, the cost competitive power can be gotten, which makes possibility to outdo the CRT market easily.

2. Principle of the driving LCD monitor

* Principle outline*

Among display parts such as LED, PDP, EL and so on, TFT_LCD has been the most widely used together with LED. The configuration of the LC cell is as follow. Liquid crystal is located in between two tip-enclosed glass plates, and electrodes exist inside of each glass plate to display an image. These electrodes are electrically contacted to external terminal.

☞ LC cell: It consists of two glass plates, and it is a construction part of LCD element inserted between the plates. Inside of the plates, transparent electrodes exist to construct picture element, and above it, an alignment film plate exists for aligning LC molecule in one direction. The active procession LCD is formed at the lower substrate, and the active elements (diode and transistor) are formed at the side of the picture element. The Color LCD is formed at the upper substrate, and a color filter is mounted for displaying colors. The color filter is located between transparent electrode and glass substrate, and it is made by pigment dispersion method, staining techniques, and etc. on the glass substrate.

The space between the grass substrates is maintained for inserting the liquid crystal, and the spacer maintains the space for the wider display element. In the space, the liquid crystal is inserted and aligned. At the side of the cell, electrode pattern connected to the transparent electrode exists, and external voltage reaches to the liquid crystal through the pattern. In the active procession LCD, pattern for driving active element is formed. The active element is driven by patterns, and external voltage is applied to the liquid crystal through the patterns.

* Why TFT_LCD*

Display is requested the display efficiencies such as high contrast ratio, high luminance, high revolution (display capacity on the dialogue screen), gradation display ability, color display ability, high-speed response ability, wide angle of visual field, and so on. Picture, letter, or figure information can be displayed by single passive matrix type, but the characteristics are in the relation of trade-off. In other

words, making one characteristic better would make other characteristic worth. Therefore, there is a limit to make all characteristics highly efficient. The worst weakness is a problem of cross-talking, but active matrix can enhance the ability of display by adding a switch element into each picture element.

☞ Cross Talk: It is a signal interruption between elements. For example, the display signal is distorted in the unselected picture element row, and it makes low C/R value. Active matrix method has low cross talk value contrast with simple matrix. But, the active matrix method still occurs the cross talk because the TFT element cannot drive the switch well. Also, the simple matrix method occurs the cross talk because of the signal delay due to the resistance of the electrode. Therefore, it is needed making a low resistance of ITO or driving it by given a same signal from the both side of the electrodes.

? Liquid Crystal

Liquid crystal seems like a liquid at a glance, but it is in a unique state showing anisotropy like a crystal. It is an organic compound called "Thermotropic liquid crystal" becomes a liquid crystal in certain temperature range.
There are reflection type and backlit type of LCD. The reflective LCD reflects the incoming light from the front side of the LCD panel to the reflection board mounted to the backside of the panel. The backlit LCD expresses an image by taking surrounding light or fluorescence from rear side.

? Driving principle

The liquid crystal is contacted to the aligned surface for inducting the direction of the liquid crystal, and the liquid crystal molecules are arranged in parallel with the alignment film hollow. All liquid crystal

molecules are arranged in parallel near to the both substrate surfaces, and both substrates are twisted 90 degree against each other (called 'twisted molecule arrangement'). Therefore, the liquid crystal molecules are twisted 90 degree between both substrates in succession, and the light advances in the same direction with the molecules. As shown in the figure, if the molecules are twisted 90 degrees, the light takes same direction with the molecules in twisted 90 degrees.

☞ Liquid crystal: There is a mesophase exists in the natural world with three common states, solid, liquid, and gas. The mesophase is called liquid crystal phase. It has characteristics, fluidity of liquid and positional system of crystal, in the certain temperature range.
The liquid crystal phase is divided into Nematic, Smectic, and columnar phase. The phase of 온도 전이형 액정 is changed by temperature, and phase of 농도 전이형 액정 is changed by density.

그림 삽입 [Liquid crystal molecules are arranged in parallel to the aligned film hollow.]
그림 삽입 [Liquid crystal molecules are twisted 90 degree between both substrates.]

By adding voltage or external force with TFT, the direction of the liquid crystal is coming undone from the state of twisted in 90 degree. The direction is arranged in one direction to the panel surface vertically, and the light goes straight.

Consequently, the matter of passing the incoming light is depending on the conditions (twisted or untwisted) of liquid crystal. By adding the polarizing to the both glass boards, the light passed through the liquid crystal is collected in one direction again, and it is entered into the picture element to be appeared on the screen finally.

☞ Polarizing film: Light is vibrated by electromagnetic wave, and the electronic field and magnetic field are vibrated vertically to the operating direction. The vibrating direction of the light from the backlight of the LCD module has same probability to the all direction. The polarizing film transmits the light vibrated same direction of the polarizing axis, and it absorbs with proper medium or reflects the rest of the light vibrated to other directions to make the light in specific direction. While it is passing the liquid cell, the strength of transmitting light is controlled by rotation of the polarizing axis, and it makes the expression of gray in between black and white. In the LCD application, it is important not only polarizing degree but also management of the low reflected surface. When using the LCD in brightening place, the contrast becomes low, and the acknowledgment is reduced as a result. Therefore, the technique to reduce the reflecting ratio for the surface of the polarizing film is needed for developing picture quality.

[Shows how liquid crystal molecules are arranged when voltage is given.]

[Shows how liquid crystal molecules are arranged when voltage is off.]

[Shows how light go through when voltage is on or off.]

? Principle of expressing colors

In the beginning, LCD supports only black color. Nevertheless, as the application range of LCD is getting wider, and the display market is getting changed toward to the color, the LCD has developed to support colors.

LCD uses the color filter, which has three primary colors of red,

green and blue, to express colors. The RGB color filters are arranged closely to each other, and each color signal is applied to the color filter for controlling the brightness to express colors. The voltage applied to the element is controlled for managing the brightness to express various colors.

If the liquid crystal has only two functions such as cutting off light and passing light completely (red, green, blue = 1bit respectively), 8 colors (2 to the third power) can be expressed. In other words, if filter has a function to open and close, each of three colors can be controlled with 1 bit data. If each color is controlled by 2 bits, 64 colors (2 to the sixth power) can be expressed. It is expressed in equation as below.

Consequently, the quantity of colors to be expressed by LCD is depending on the bits of image data.
In other words, the quantity of light passing through the color filter is controlled by liquid crystal. The voltage for operating the liquid crystal is output from the source driver IC and supplied through the pixel TFT. The voltage supplied to the liquid crystal changes the permeability of liquid crystal. The possible quantity of colors to be expressed is determined by number of steps for controlling the liquid crystal. For example, if the liquid crystal is twisted, the color will be black, and if the liquid crystal is released, the color will be white. The combination of medium gray scales expresses other various colors.

? Resolution

The resolution is another primary characteristic of display. The resolution is a measurement to express an image in detail. As resolution is higher, the quantities of picture elements are getting more. It means that the amount of data treated by drive IC during unit of time is larger; therefore, the processing speed reaches near to

the limit.
Due to the fact, there are more possibilities of creating signal distortion and EMI. In addition, as vertical resolution is getting higher, time allowed for one horizontal line becomes shorter. Time for charging data voltage into picture element is the same as time for one horizontal line. If the time gets shorter than a certain level, charging process cannot be achieved completely which leads to bad picture quality. Study and research to solve the problems has been processed in many aspects, and technology has made much advance.

☞ EMI : Electro-magnetic interference. It is an electronic interruption by a mutual induction of electromagnetic frequency. It is not proved its harmfulness, but its harmfulness is proved in statistics and dynamic research indirectly. It drops off immunity and outbreaks of VDT symptom. Therefore, every country has standard for limitation of EMI emission. For preventing serious problem, electromagnetic interference is basically standardized not to interrupt other machine's operation such as instrument or communication facility of airplane, pulse generator of hospital, etc. Recently, Korea government also processes to establish the restriction low due to the studies.

? Construction of color TFT_LCD module

Color TFT_LCD is divided into a-Si (amorphous silicon) TFT and p-Si (polysilicon) TFT. The direct view TFT_LCD using a-Si TFT is the most widely used.

TFT_LCD is roughly divided into the following 3 units.
First, panel with liquid crystal implanted between substrates.
Second, driving circuit includes Driver LSI for driving panel and PCB (printed circuit board) with circuit element.
Third, chassis structure with backlight.

Assembly composed of these units is called TFT_LCD module.

☞ Backlight: Light is sent from backside. Liquid crystal cannot make light itself, so it controls the amount of light from backlight to display various colors. Therefore, the backlight function has deep relation with luminance. As backlight is better, luminance is higher.
Two tubes looks like fluorescent lamp are installed horizontally, and send light over the screen evenly. The light is controlled light to display liquid crystal and display various color.

The backlight of a surface light source type, which maintains even luminosity of whole screen, is needed because liquid crystal cannot make light itself and just modulates the amount of transmitted light. The requesting performance of the backlight for LCD is having even luminance of whole display surface, and maintaining enough luminance in considering transmissivity of panel, less than 10%. In case of portable LCD, it has to be lighter, thinner, and has low consumption power. CCFL (cold cathode fluorescent lamp) used as light source of backlight unit is consisted of fluorescent lamp (heat cathode shape), light guide panel, prism sheet, diffusion plate, reflection sheet, etc.
The fluorescent substance of the CCFL is mainly the rare earth (Y, Ce, Tb, etc), which has high efficiency. For LCD, fluorescent substance is consisted of 3 frequency types of white system, which is mixture of red, green, and blue fluorescent. The light guide plate takes the light from the side of acrylic plate. The light processes to the inside of the acrylic plate, and it is coming out to the front of panel by reflection plate. The reflection plate, dot type gradation pattern, controls the amount of reflection to make the backlight to have even luminance over its surface by applying less light in where close to the lamp or more light in where far from the lamp.

TFT_LCD module has display function, and it is a subsystem of the systems such as a notebook PC, TV, or monitor.

[Construction of the TFT-LCD module]

* Principle of LCD drive*

1)

a) Black Matrix: It cuts off the light from the R,G, and B element. It is formed in among pixels of color filters and absorbs the light coming from the outside to prevent the reflection.

b) Color Filter: It is a resin film containing dyeing stuff or pigments of primary colors (red, green, and blue). Eventually, it makes the passed light through liquid crystal to have colors.

c) Over Coat Film: It is used for making a flat surface of the color filter. It is also used for improving adhesiveness with ITO (Indium Tin Oxide), which is a material of transparent electrode due to its great transmissivity, conductivity, and chemical/thermal stability.

d) Common Electrode: It is an electrode made of ITO, the transparent electric conductor, and adds voltage to liquid crystal cell.

e) Alignment Film: It is a thin organic film consists of Polimide, and is formed for aligning liquid crystal.

f) Liquid Crystal: Its thickness is normally about 5㎛, and it has arrangement of twisted Nematic letters.

g) Sealant: It is located on the edge of panel and works as an adhesive to fix TFT array substrate and color filter substrate. It makes active cell area.

h) Picture element electrode: It is transparent and made of electric-conductive ITO. It adds the signal voltage given by TFT to liquid crystal cells.

i) TFT: It is a switching element to give or cut off the signal voltage to liquid crystal.

j) Storage Capacitor: It maintains the signal voltage given to pixel ITO more than a certain time.

2) Backlight unit

It makes a plane light with even luminosity from a fluorescent lamp used as the light resource. The thickness of module and consumption of electricity are depending on making thinner thickness of the unit and improving coefficient of utilization of light. The light from backlight gradually decreases in brightness immediately after penetrating the display module unit. Only 5% of light coming into the backlight penetrates the front Polarizer.

3) Driving circuit and Chassis unit

The TFT LCD panel consists of TFT array and color filter substrates. The drive circuit including driver IC must be installed in the peripheral part. The drive circuit takes multi layer PCB type. For the circuit part, SMT (surface mounting technology) is used for having a thinness and high density. Driver IC is made in the form of TCP (Tape carrier package) and connected between PCB and panel.

The drive circuits, TFT LCD panel, and backlight unit made as above are completed with chassis unit, and become assembled parts. It is called TFT module.

Manufacturing processes for TFT LCD panel is briefly described as

follows.

1) TFT array process to make switch elements, which give pixel unit signal.
2) Color filter process to make color array of red, green, and blue for expression of colors.
3) Liquid crystal process to make liquid crystal cells in between TFT substrate and color filter substrates.

The STN LCD is adopted for the LC cellular phone or car navigation, monitors, and so on, and the TFT LCD is adopted for Note PC monitor, desktop monitor, and so on. The 15" and 18" LC desktop monitors are the most popular in the world. For increasing the market share in the display field, the technique for larger size screen has to be developed.
In the technical aspect, it is difficult to maintain the LC space equally because the LC weight gets together into the middle if it is larger size. The picture quality becomes low due to the distribution of the unequal space.
Due to the weakness, PDP is developed for the 20", but its market share is small because of its expensiveness. Therefore, it is expected the lots of technical developments of the LCD for the flat display device with its high market share.

3. CRT monitor and LCD monitor

◆ The weakness of the LCD compare to the CRT
  ☞ Viewing angle, after image, quantity of display color, responding speed
◆ The strong point of the LCD
  ☞ Consumption power, electromagnetic wave, size (saving space), picture quality (focus, GD, CG)
◆ Equivalence (no problem to use and possible compensation):
  ☞ Maximum luminance, contrast, flicker

☞ Viewing angle: It is one of LCD's weakness. It is no problem to watch the 120 ° of right and left and 110 ° of top and bottom. But, if many people watch one screen, the color is turning over due to the changing viewing point with moving a head little bit to the top, bottom, right, or left. Especially, as size is larger, the viewing angle must be bigger; therefore, the technical development is necessary for larger screen.

☞ Responding speed: The responding speed is slow because of the LD's characteristic of the molecules. Generally, it is no problem doing word process and moving picture not to fast, but for the game and real movie, the picture quality is getting worth due to short on/off time of the LC.

☞ After image: When trying to express another image after certain image is stoppage in long time, the first image pattern reminds on it called after image.

☞ Number of colors: If the sub-pixels (red, green, blue = 6 bits each) adopt the panel consists of 18 bits, various colors can be expressed by controlling the luminance of the sub-pixel in several level even though the number of sub-pixel is 18. The possible expressing numbers of colors are 16,700,000 (2 to 6^{th} power = 256 levels).

It is the same case as the sub-pixel is 24 bit (2 to 24^{th} power). CRT has analog signal. It means that CRT supports all colors with graphic card. In comparison with the CRT, the possible expressing color numbers of the LCD is still deficiency.

☞ Consumption power: If CRT has 105w and LCD has 35w, the LCD's consumption power is 33% of the CRT's. For example, If PC is used 8 hours per a day for year, the consumption power of the CRT monitor will be 306,600w (105x8x365=306,600w), and the consumption power of the LCD monitor will be 102,200w (35x8x365=102,200w).

If the average electric charge is 75won per 1kw/h, the consumption power for year will be 22,995won (306,600x75=22,995) for CRT and 7,665won (102,200x75=7,665) for LCD. The difference, 15,330 won, is small amount for person, but nation. The low consumption power is good aspect for the TFT-LCD monitor mounted to the note PC due to portability and battery waiting time (time to use for one charge), but for the TFT_LCD mounted to Desktop monitor. But the advantage of the LCD monitor cannot be ignored due to the environmental protection tendency of the current time.

☞ Electromagnetic frequency: In comparison with the LCD, the CRT monitor (certified TC099) makes high frequency, which affects to human body. Therefore, the LCD monitor is used in hospital, laboratory, and so on because precision machine could be malfunctioned by electromagnetic frequency.

☞ Weight: The CRT is 20kg and the LCD is 5.5kg, which means the weight of the LCD monitor is 28%(1/4) of the CRT monitor. It is a great advantage for the note PC monitor and desktop monitor. But the flat CRT monitor

has thicker glass of panel. It means that the weight is heavier for the female user and children user.

☞ Size: It is a just numeric value.
CRT monitor: 420x443x466=86,703,960
LCD monitor: 405x182x361=26,609,310
The size ratio of the LCD monitor is about 30% of the CRT monitor, so it saves a space as much as the percentage.

[The side view of the general TFT LCD and flat CRT]

☞ Visible picture: The CRT has different sizes of the visible picture when being a Braun tube and a monitor by inserting the cabinet. There is no certain theory why size is not standardized when it is a monitor. The size of the visible picture for the CRT 17" is actually 16". Nevertheless, the actual size of the TFT LCD is same as spec. The visible picture size of CRT 17" is 310x230, and LCD 15.1" is 307x230. There is just 3mm difference horizontally. In other word, 17" CRT monitor and 15.1" LCD monitor is almost same size.

☞ Picture quality: The problems, luminance, contrast, etc, in the developing process of the LCD, are almost solved. About the picture quality, the pixel concept of the CRT is unclear, and the CRT adopts the polarizing device to scan a beam physically. As a result, there can be differences of focus, cg, gd, etc. between every products and even fine products. Nevertheless, because the pixel position of the LCD is fixed, there are no differences of the focus, cg, gd, etc. between products. If

there are some problems, it could be about the unequal brightness or unequal white, or missing pixel due to inferiority of TFT at each picture element.

☞ Managing surface: The general management of CRT surface is anti reflection and anti static management. There are two methods, coating and attaching film. The coating method is difficult to coat over the flat evenly, so film method is invented. The surface of the Samtron 75DF is treated with Multi-layer film with ARAS. It means it is prevented from the refection and static by attaching the multi layer film. For the LCD, the anti glare treatment is applied to prevent the glance of the surface. The CRT surface consists of thick glass, so it is very strong from impact or scratches. Nevertheless, the surface of LCD consists of the thin polarizing film, so it is very weak. Therefore, hard coating is applied additionally for protecting the surface. If LCD is used in carefulness with acknowledgment of the weakness, it is not a serious problem.

☞ Comparative superiority of the TFT-LCD monitor and CRT monitor.

▶ Slim design for space saving

- In comparison with CRT monitor, it supports the fine environment for taking small space (less than 1/3 of CRT).
- User can get nice interior effect.

▶ Clean image at every part of the screen. (Even at the edge)

- In comparison with CRT monitor, it expresses an image vividly.
- It is comfortable to use visually for long time use.

▶ No screen flickering

- There is no flickering screen because individual active elements exist in each picture element.
- There is no tiredness of eyes for long-term work.

▶ Almost no electron wave is occurred.

- In comparison with the CRT monitor, almost no electron wave, which may harm human body, is occurred.
- It doesn't affect to other device with electron wave. (It is suitable for hospital, military, laboratory, etc.)
- In the future, TFT_LCD monitor will be dealing with all application devices instead of CRT.

▶ Low consumption power

- It is low-consumption-power monitor, 32w, so it is suitable monitor for bank, office, stock market, telemarketing, control devices, etc.
- It minimizes the calorific value to supply fine work environment.

* DCT monitor is basically driven by RGB signal, and it has construction that the electron from the electron layer is polarized by crushing to the glass of fluorescent materials for creating light.
TFT_LCD monitor drives the liquid crystal panel to display an image. The TFT_LCD has construction different to the CDT. Liquid crystal is filled in between two glasses, and electrode is connected into each liquid crystal cell. By applying voltage, the construction of the liquid crystal's molecule is changed for controlling light coming from backlight. The TFT_LCD has several advantages in comparison with

CDT such as thinner thickness, no flickering screen, etc.

4. Analog monitor and Digital monitor

▶ The trend of the monitor market in the world

Desktop monitor is divided into two big parts, CRT monitor and TFT_LCD monitor.
According to the statistics in 1999, CRT monitor owns 95% of market share, and the LCD owns only 5%. According to the statistics, the 15% (which is not small percentage) of reason to choose it is for digital interface. Nevertheless, the CRT monitor, which controls the market, is analog, so LCD takes analog method mainly for considering interface.

▶ Difference between CRT monitor and LCD monitor

Originally, the CRT displays information with analog method, so the output signal has to be analog method. But, all information from the PC is digital data. For displaying the digital data onto the monitor with analog method, the data is converted to analog at graphic board. As a result, the RAMDAC (digital to analog converter) is needed in the graphic board, and the signal from the board is transmitted to monitor via cable. Therefore, signal loss and noise are occurred which make low picture quality.

Primarily, LCD monitor is display device with digital method. Therefore, there are no signal loss or noise, and unnecessary part such as ADC (Analog to digital converter) is not needed because it takes the digital data from PC directly. Nevertheless, for considering marketability, it is impossible to produce only the TFT_LCD with digital input. Therefore, TFT_LCD monitor with a built-in ADC (analog to digital converter) is mostly produced. Also, companies for graphic board adopt the DAC (digital to analog converter) because the most of monitor takes the analog input method.

▶ Relationship in changing signals between Digital monitor and analog monitor.

The LCD monitor with analog input method converts the data from PC to analog at the graphic board, and coverts it to the digital to the LCD monitor. Such processes occur the information loss and make to adopt unnecessary parts, which is the fact to raise its price. It is reasonable that low demand of LCD due to such additional cost.

	Digital Monitor	Analog Monitor
Advantage	- There is no signal conversion between digital and analog, so no signal loss is occurred. Better picture quality. - It doesn't need ADC and DAC. Low price.	- Generally, it has nice interface with graphic board. - It doesn't need to buy a new graphic board.
Disadvantage	- There is no defined standardization. (P&D, DFP, and DVI) - Interface problem - The graphic board with digital interface is needed additionally. Also, it is difficult to find it.	- There is signal loss during signal conversion, digital to analog, and analog to digital. - Cable gets effect from external. - ADC or DAC is needed. High price.

[Comparison between digital monitor and analog monitor]

▶ Digital era

All the information is getting digitalized. For example, the information from the Internet is digital. Also, TV programs from the North America, Europe, and Japan are broadcasted in digital. In the near future, all TV programs will be broadcasted in digital, and it has been prepared. In Korea, some digital programs are already introduced, and DVD movies are increased in number. With the

trend, the digital monitor is introduced from North America, Japan, and Europe. Domestic manufacturing companies also make digital monitors. The digital monitor's market share will be expanded in the future.

▶ Why aren't there many digital monitors?

The reasons that the digital monitor cannot be popular are: first, as mentioned above, the analog market is too big, and the manufacturing companies don't invest for it. Second, there is no standardization for wider use. The VGA interface for digital method is not standardized, so the monitor manufacturing companies or graphic board manufacturing companies are unwilling to produced it.

▶ What kind of VGA interfaces exist?

Mainly, P&D, DTP, DVI, etc. are adopted recently.
P&D (digital plug & play) was adopted by VESA in 1997, and it is transfer protocol with TMDS method, called panel link. The digital connector with P&D method transfers both of analog and digital. But, price is raised by attaching the solution (combination of USB and IEEE 1394/Flrewire signal) to achieve the transmission. Any of graphic board manufacturing companies doesn't have interested in such expensive connector, so it couldn't be standardized. The Compaq makes DFP (digital flat panel), which has similar function with P&D, but price is lower. The functions are almost same as P&D except analog signal, USB, and IEEE 1394 which are dropped off due to high price. The transfer protocol is same as P&D and TMDS method. The weak point of the DPF is that the maximum resolution is limited at SXGA (1280x1024), and it can't take the graphic board and analog monitor because it transmits only digital. It is expected that the DFP connector can't be stand longer with the weaknesses.

▶ What is the DVI?

Recently, to make up for such weaknesses, DVI (Digital Video Interface) is being watched for VGA interface and counting on for marketability. DVI is developed by DWG (digital display working group), which includes many companies related in DFP. DVI has possibility to be a standard due to its interface using TMDS protocol as P&D and DFP. The maximum resolution of the P&D and DFP, which have one link, is limited to 1,280x1,024, but DVI supports over 1,280x1,024 with 2 links by increasing the maximum pixel speed twice. Also, it transmits analog signal, so it can be connected to the CRT. With the reasons, DVI is expected to be a standard of VGA interface.

▶ Does what kind of graphic board be chose?

Graphic board problem cannot be missing for the digital monitor. Now, graphic boards are expensive because they support either of analog and digital in considering the interface with analog monitor. As the demand of digital monitor is less, it is not a good idea to make user individually to buy an additional high price graphic board for digital monitor. The local manufacturing companies produce graphic boards for their digital monitors and sell it to buyers who buy their company's digital monitor.

▶ The advantage when the DVI is adopted

The main problem of the analog VGA standard is quality difference of output signal among the manufacturing companies and graphic board companies. But if DVI standard is standardized, the quality difference among companies will be reduced. As the results, the technical gaps of products, CDT monitor, will be raised clearly among companies. Also, the DAC is attached to CDT, which is the fact to raise price. In the quality aspect, there is no unnecessary process in comparison with analog method, so the picture quality will be improved.
The price of the digital monitor will be down because it doesn't need to attach the ADC (analog to digital converter), and its picture quality

will be improved by skipping two signal conversions.

▶ Products with DVI

Let's see digital monitors introduced in Comdex show on Nov., 1999.
All prices are standardization on Nov., 1999. The digital CRT monitor produced by Samsung is 21 Syncmaster 990 DVI. The 21 Syncmaster 990 DVI is CRT monitor, and it supports high resolution (UXGA level (1600x1280)) and either of digital signal and analog signal. Price is about 1,450,000 won. The ViewSonic introduces OptiSync PF77, 17" flat CRT monitor, and OptiSync PF97, 19" flat CRT monitor. They support either of analog signal and digital signal. Price of PF97 is $625, and PF77 is $429.

Let's see digital TFT LCD monitor.
Hewlett Packard introduces 15" Pavilion FX70. It supports DFP, P&D, DVI, and analog. Price is $1,099. The ViewSonic has VP181, 18" digital TFT LCD, and VP151, 15" digital TFT LCD.
They have video input, two digital inputs, and two analog inputs. Price of the VP181 is $3,795, and VP151 is $1,795. The maximum resolution of VP181 is 1600x1200 and VP151 is 1280x1024.
NEC has 15" MultiSync LCD1525X and 18" MultiSync LCD1810X. They support combining connection of analog and digital and analog exclusive port. The Hankook computer company, local company, introduces SlimWin 15D with DFP graphic interface, and a new model with DVI will be introduced in this year.

▶ Future of Digital monitor

Even though digital monitor has lots of advantages, it seems to be far from us.
In Japan, The TFT LCD monitor takes over 50% of market share in desktop monitor market, but the analog method for VGA interface takes more percents in it. It may be that the CRT monitor takes much part, so its effect is still reminded over the industry.

Nevertheless, the importance of digital monitor is getting serious as all information is getting digitalized.
The demand of monitor for digital interface is getting bigger over the world.

5. Summery of TFT_LCD monitor terms

TFT-LCD (Thin film transistor liquid crystal display) is a display method of that liquid crystal is filled in between two glass plates. When light is passing the liquid crystal's molecules, direction of light is defined with alignment of the molecules, and polarizing film controls direction of the passing light. After applying voltage, the liquid crystal molecules are aligned in curved angle for passing the polarizing filter. The applying voltage drives the liquid crystal as a shutter of camera for making the light to block or pass the filter. TFT LCD has cost efficiency due to using low power and glass, and it doesn't create noxious frequency.

☞ Sync Signal

- It is a standard signal to give a regular hue signal to monitor. Basically, the signal is divided into horizontal and vertical Sync signal. According to the Sync signal, monitor expresses the normal hue signal by resolution and frequency.

☞ Kinds of Sync signal

- Separate: It is a method to delivery the horizontal and vertical Sync signal to monitor.
- Composite: It is a method to synthesize horizontal and vertical Sync signal and to delivery the combination signal to monitor. The signal is separated inner side of the monitor and express the hue signal on monitor.
- Sync on green: It doesn't use additional Sync signal line. It is a method to delivery the signal to monitor by synthesizing the

horizontal and vertical Sync to the green among the hue signals. It is mainly used for workstation.

☞ Saturation

- It is a degree of difference determined from white (standard) to own color. As the saturation is bigger, color is getting near to its own color.

☞ Hue

- Red, green and blue

☞ Vertical frequency

- Monitor repeats the same picture several tens in a second like fluorescent lamp. The repeating degree to express picture in a second is called vertical frequency or reflash rate. Unite is Hz.

  Example) People can feel the flickering when the light is shown 60 times in a second. It is became a Flicker-free mode by using over 70Hz of vertical frequency to prevent such happening.

☞ Horizontal frequency

- Horizontal cycle is a taking time to express one horizontal line. Horizontal frequency divides the horizontal cycle by 1 to express how many horizontal lines can be express in a second, and use kHz.

☞ Plug & Play

- It is automatically set up the best picture by exchanging the information between monitor and computer. Monitor takes the VESA DOC method (international standard) for plug and play function.

☞ Resolution

- It is a number of vertical and horizontal dots consisted monitor, and tells detailed degree of picture. As the resolution is larger, lots of information can be gotten on the monitor.

Example) If resolution is 1,024x768, it is consisted of 1,024 dots (horizontal resolution) and 768 lines (vertical resolution).

☞ Back Light

- LCD cannot make light itself, so it needs light from external. It is a light source located in the backside of liquid crystal panel.

☞ Aperture Ratio

- It tells possible area ratio of LCD for displaying information out of whole screen. As the aperture ratio is larger, picture elements take more area, so luminosity becomes better.

☞ Viewing Angle

- Contrast ratio is changed by angle of the viewing point. The changing degree is shown by the viewing angle.

☞ Cross talk

- Signal interruption among picture elements.

☞ Luminance

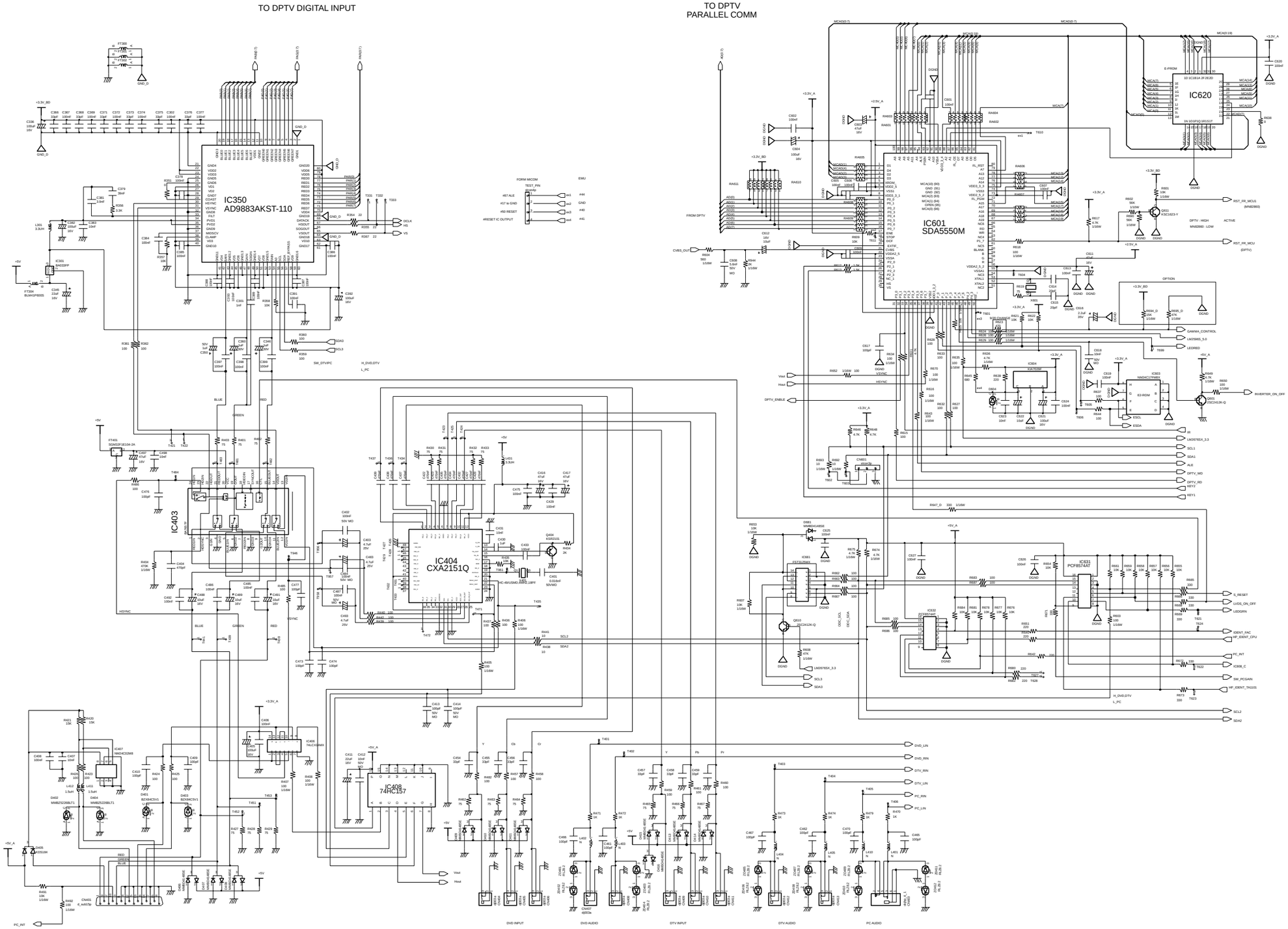
- It is about the luminosity, and its units are NIT, F/L, Cd/m^2, etc.

☞ Function of Image scaling

- Because 14" and 15" TFT panels are made up of basic pixel numbers, 1,024x786 mode, a special function is needed to expand an image in a beeline for watching the whole screen of the SVGA and VGA.

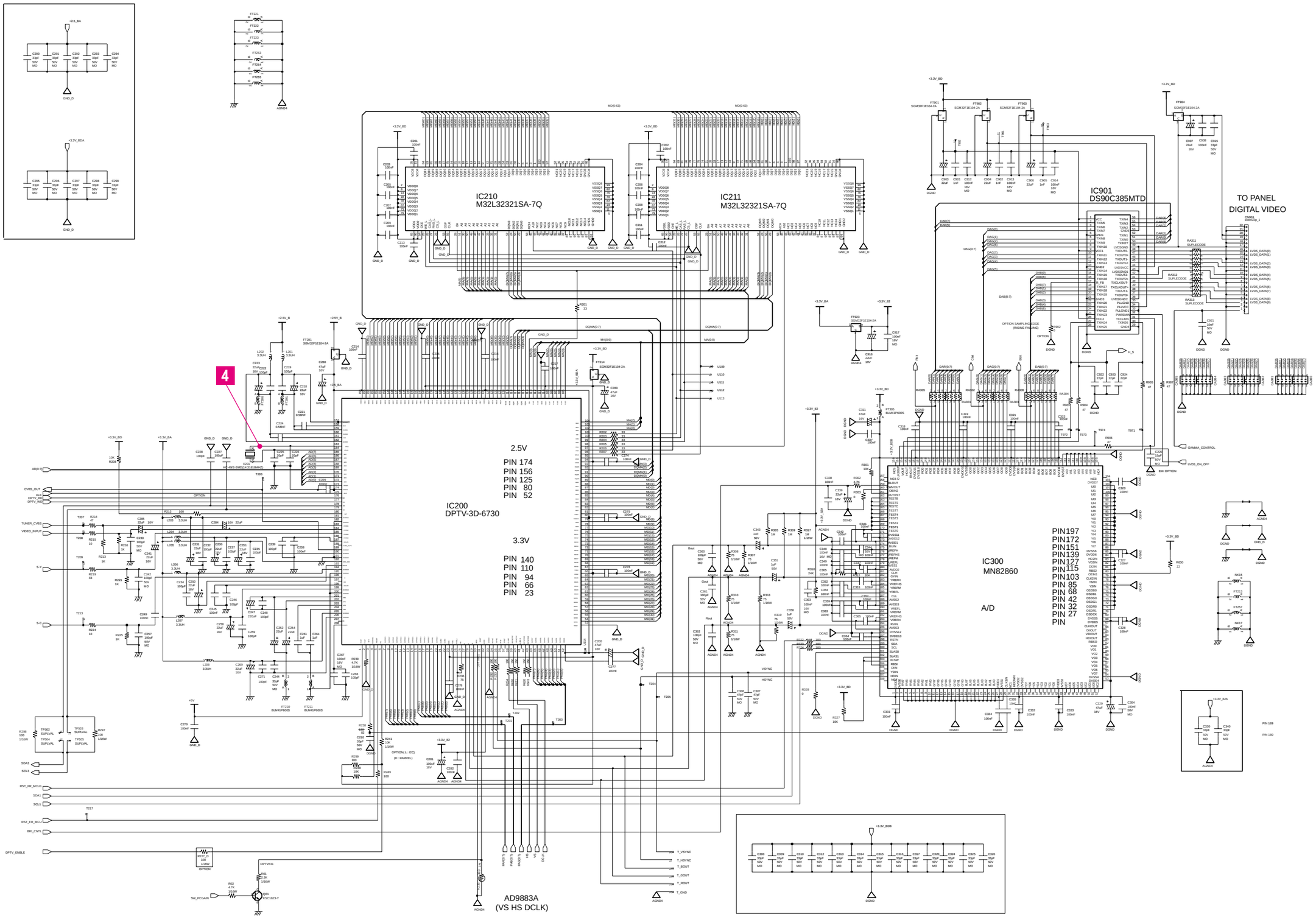
9. Schematic Diagrams

1 CPU Block & Signal Processing Part Schematic Diagram



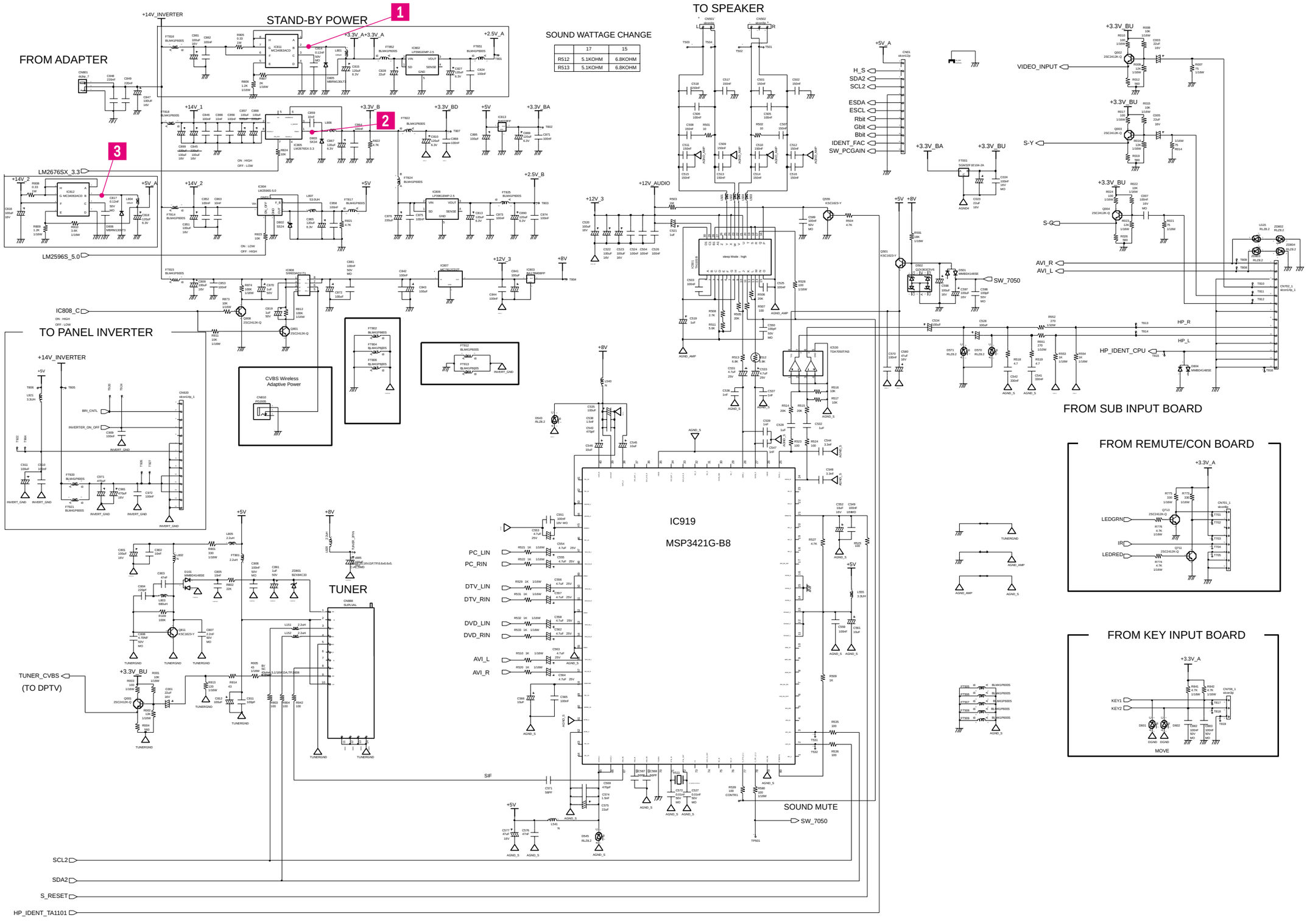
CONFIDENTIAL

2 LCDTV DPTV & 82860 Part Schematic Diagram

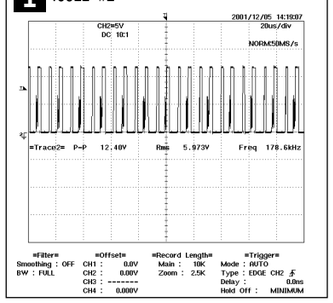


CONFIDENTIAL

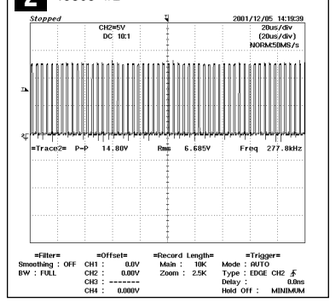
3 LCDTV DC Power Input, Sound, Tuner, ETC Part Schematic Diagram



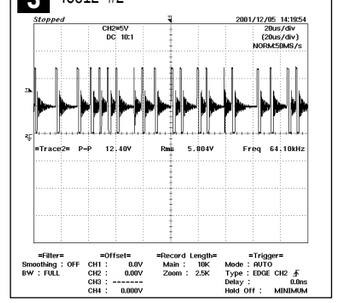
1 IC811 #2



2 IC805 #1



3 IC812 #2



24C02C

2K 5.0V I²C™ Serial EEPROM

FEATURES

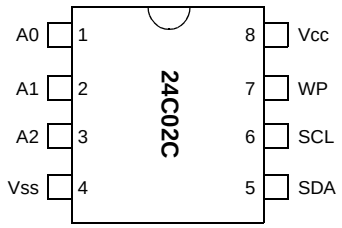
- Single supply with operation from 4.5 to 5.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Organized as a single block of 256 bytes (256 x 8)
- Hardware write protection for upper half of array
- 2-wire serial interface bus, I²C compatible
- 100 kHz and 400 kHz compatibility
- Page-write buffer for up to 16 bytes
- Self-timed write cycle (including auto-erase)
- Fast 1 mS write cycle time for byte or page mode
- Address lines allow up to eight devices on bus
- 1,000,000 erase/write cycles guaranteed
- ESD protection > 4,000V
- Data retention > 200 years
- 8-pin PDIP, SOIC or TSSOP packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

DESCRIPTION

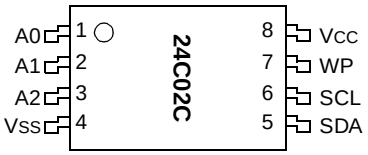
The Microchip Technology Inc. 24C02C is a 2K bit Serial Electrically Erasable PROM with a voltage range of 4.5V to 5.5V. The device is organized as a single block of 256 x 8-bit memory with a 2-wire serial interface. Low current design permits operation with typical standby and active currents of only 10 µA and 1 mA respectively. The device has a page-write capability for up to 16 bytes of data and has fast write cycle times of only 1 mS for both byte and page writes. Functional address lines allow the connection of up to eight 24C02C devices on the same bus for up to 16K bits of contiguous EEPROM memory. The device is available in the standard 8-pin PDIP, 8-pin SOIC (150 mil), and TSSOP packages.

PACKAGE TYPES

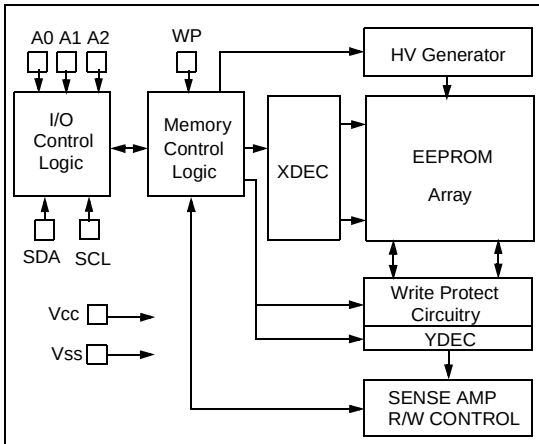
PDIP/SOIC



TSSOP



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
A0, A1, A2	Chip Selects
WP	Hardware Write Protect

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	VIH	0.7 VCC	—	V	
Low level input voltage	VIL	—	0.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 VCC	—	V	(Note)
Low level output voltage	VOL	—	0.40	V	IOL = 3.0 mA, Vcc = 4.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to 5.5V, WP = Vss
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, f = 1 MHz
Operating current	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Write	—	3	mA	VCC = 5.5V
Standby current	ICCS	—	50	µA	VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Vcc = 4.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Tamb > +85°C		-40°C ≤ Tamb ≤ +85°C		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 + 0.1 C_B	250	ns	(Note 1), $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	1.5	—	1	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

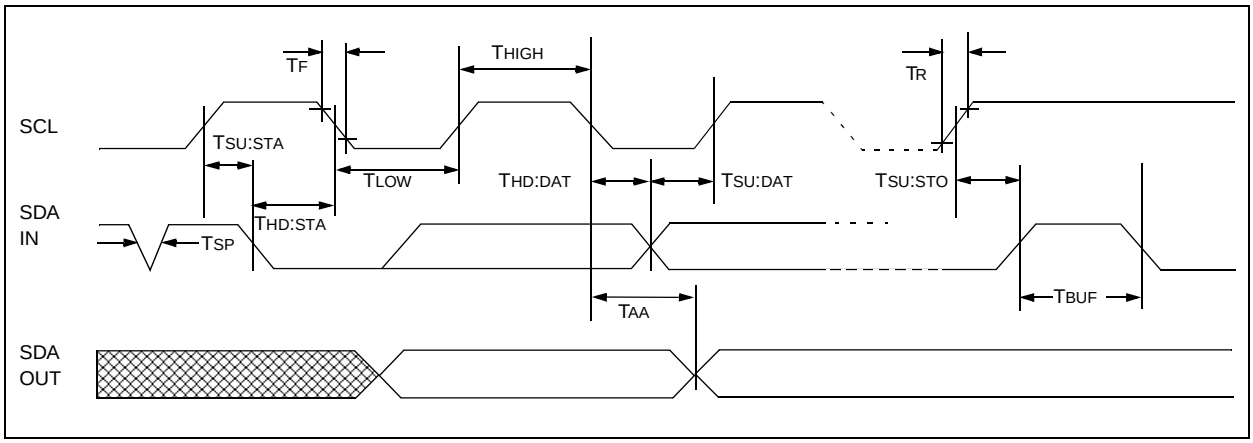
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-1: BUS TIMING DATA



Input selector switch for high definition displays

BA7657F / BA7657S

The BA7657F and BA7657S are for high definition displays, and have internal switches for switching between broadband RGB signals and HD / VD signals, as well as an internal synchronization separator. These ICs simplify the designing of input units for deluxe displays.

●Applications

CRT display, HDTV, video board for personal computer, etc.

●Features

1) Operates on a single 5V power supply.
2) Internal broadband RGB switch (frequency characteristics: 230MHz, – 3dB).
3) Internal HD / VD switch.
4) Internal synchronization separator for synchronizing signals superimposed onto G signals.

●Absolute maximum ratings (Ta = 25°C)

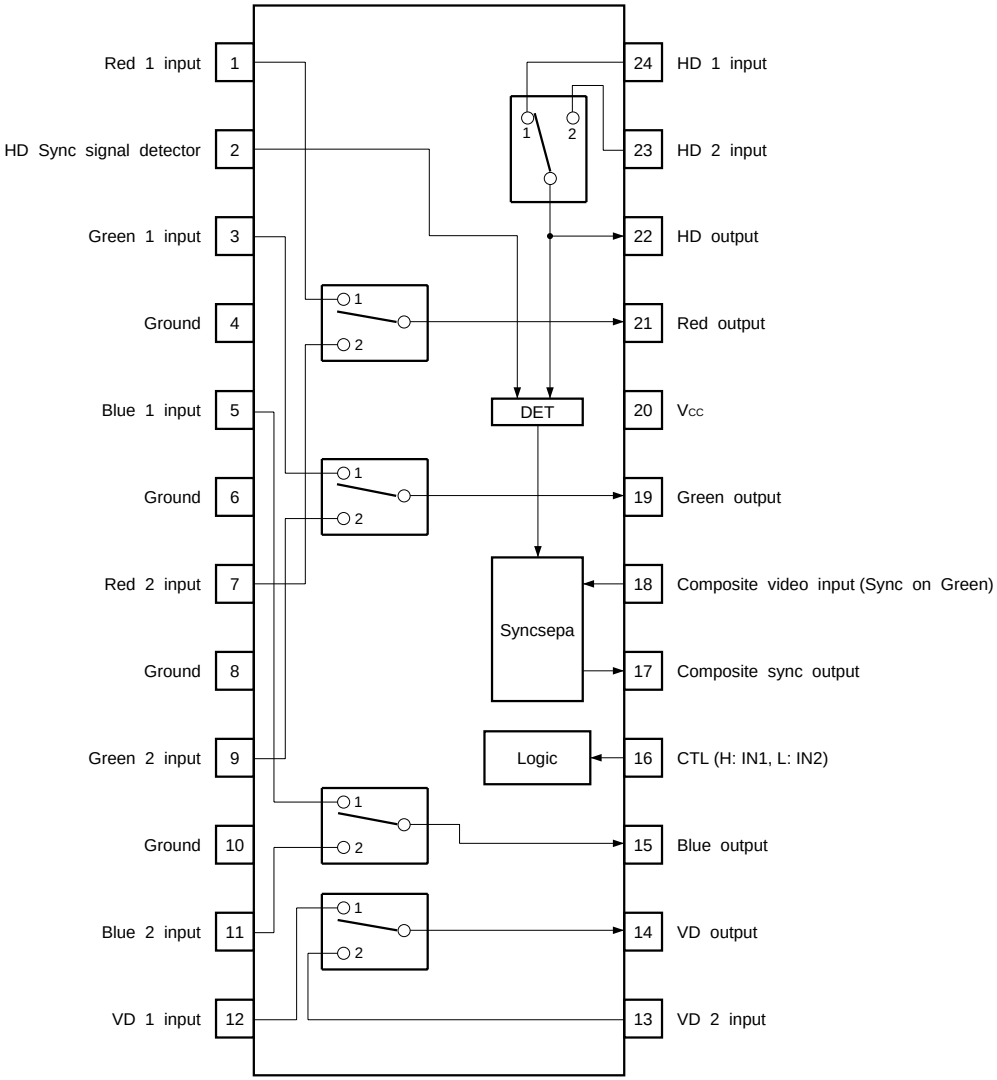
Parameter		Symbol	Limits	Unit
Power supply voltage		V_{CC}	8.0	V
Power dissipation	BA7657F	Pd	550*	mW
	BA7657S		1200*	
Operating temperature		Topr	– 25 ~ + 75	°C
Storage temperature		Tstg	– 55 ~ + 125	°C

* Reduced by 5.5mW (BA7657F) or 12mW (BA7657S) for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V

●Block diagram



●Pin descriptions

Pin No.	Pin name	Function
1	Red 1 input	Color signal R1 input
2	HD Sync signal detector	Detecting phase of the synchronization signal detector circuit
3	Green 1 input	Color signal G1 input
4	Ground	Ground
5	Blue 1 input	Color signal B1 input
6	Ground	Ground
7	Red 2 input	Color signal R2 input
8	Ground	Ground
9	Green 2 input	Color signal G2 input
10	Ground	Ground
11	Blue 2 input	Color signal B2 input
12	VD 1 input	Vertical synchronization signal VD1 input
13	VD 2 input	Vertical synchronization signal VD2 input

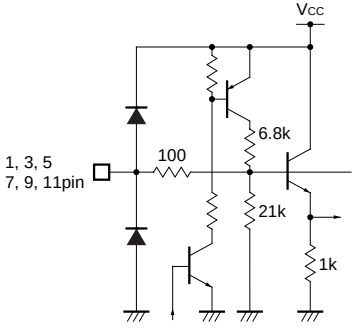
Pin No.	Pin name	Function
14	VD output	Vertical synchronization signal VD output
15	Blue output	Color signal B output
16	Control	Control (high = IN1, low = IN2)
17	Composite sync output	Synchronization signal output
18	Composite video input	Composite signal input (Sync on Green)
19	Green output	Color signal G output
20	V_{CC}	Power supply
21	Red output	Color signal R output
22	HD output	Horizontal synch. signal HD output
23	HD 2 input	Horizontal synch. signal HD2 input
24	HD 1 input	Horizontal synch. signal HD1 input

●Output selection setting table

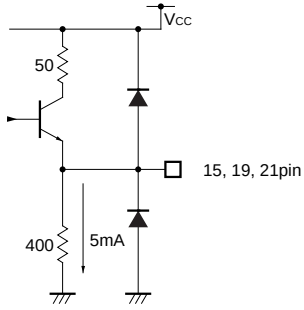
CTL	R	G	B	HD	VD
H	IN1	IN1	IN1	IN1	IN1
L	IN2	IN2	IN2	IN2	IN2

●Input / output circuits

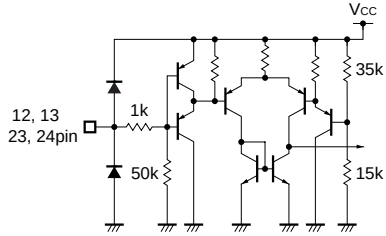
R. G. B input



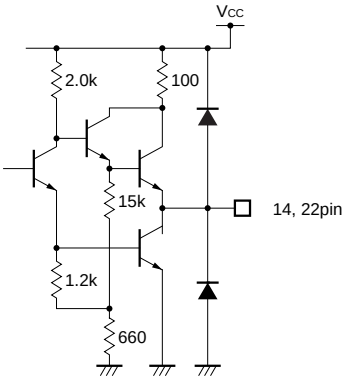
R. G. B output



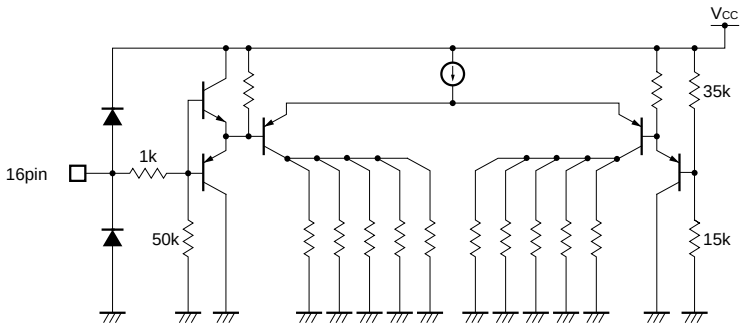
HD. VD input



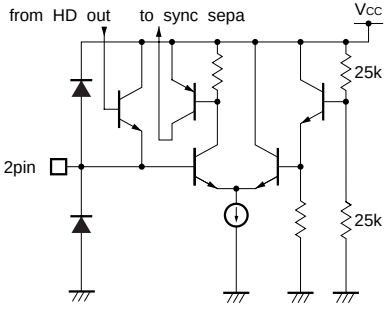
HD. VD output



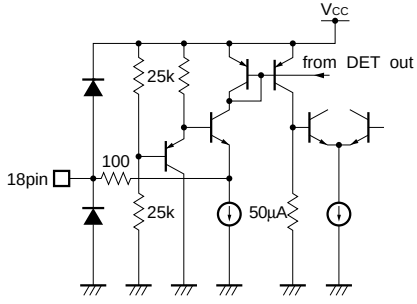
Control



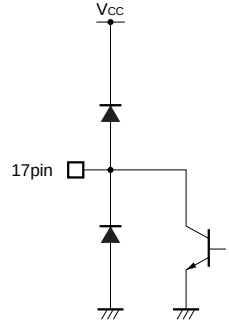
HD sync signal detector



Composite Video input



Composite Sync output



FAIRCHILD SEMICONDUCTOR™

August 1997
Revised January 2001

FST3125
4-Bit Bus Switch

General Description

The Fairchild Switch FST3125 provides four high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as four 1-bit switches with separate $\overline{OE}$ inputs. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

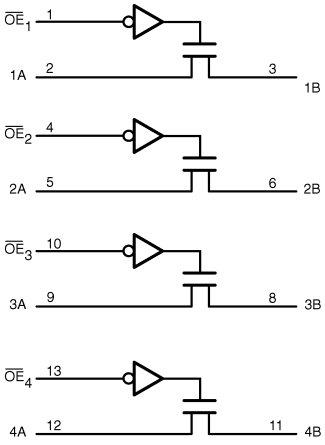
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

Order Number	Package Number	Package Description
FST3125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
FST3125QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

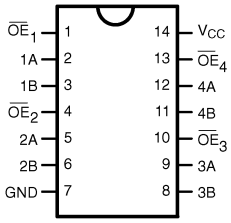
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram

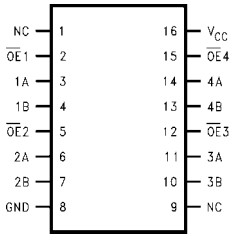


Connection Diagrams

Pin Assignment for SOIC and TSSOP



Pin Assignment for QSOP



Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$, $\overline{OE}_4$	Bus Switch Enables
1A, 2A, 3A, 4A	Bus A
1B, 2B, 3B, 4B	Bus B
NC	Not Connected

Truth Table

Inputs	Inputs/Outputs
$\overline{OE}$	A,B
L	A = B
H	Z

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_{IN})(Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0ns/V to 5ns/V
Switch I/O	0ns/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held high or low. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	High Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	Low Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance (Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V. Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\ °C$ to $+85\ °C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figures 1, 2
t_{PZH}, t_{PZL}	Output Enable Time	1.0	5.0		5.5	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figures 1, 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	5.3		5.6	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figures 1, 2

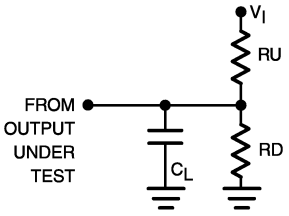
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	5		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500ns

FIGURE 1. AC Test Circuit

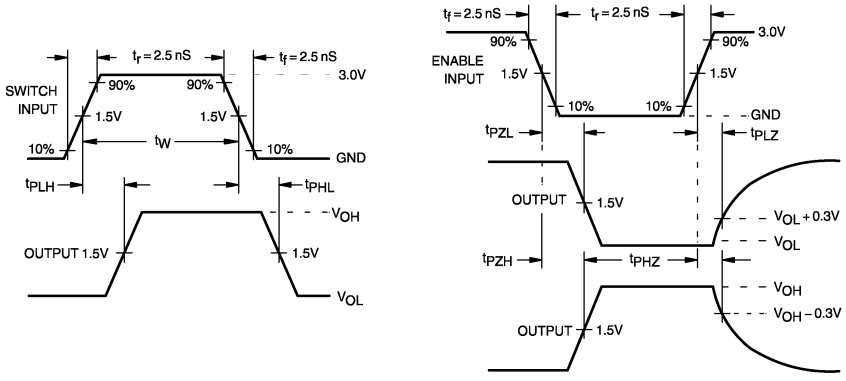


FIGURE 2. AC Waveforms

November 2000

National Semiconductor

DS90C385/DS90C365
+3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-85 MHz, +3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link-85 MHz

DS90C385/DS90C365 +3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-85 MHz, +3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link-85 MHz

General Description

The DS90C385 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 85 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 297.5 Mbytes/sec. Also available is the DS90C365 that converts 21 bits of LVCMOS/LVTTL data into three LVDS (Low Voltage Differential Signaling) data streams. Both transmitters can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge or Falling edge strobe transmitter will interoperate with a Falling edge strobe Receiver (DS90CF386/DS90CF366) without any translation logic.

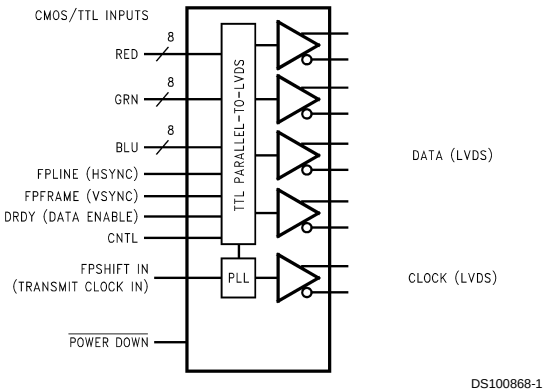
The DS90C385 is also offered in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package which provides a 44 % reduction in PCB footprint compared to the TSSOP package. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Features

- 20 to 85 MHz shift clock support
- Best–in–Class Set & Hold Times on TxINPUTs
- Tx power consumption <130 mW (typ) @85MHz Grayscale
- Tx Power-down mode <200µW (max)
- Supports VGA, SVGA, XGA and Single/Dual Pixel SXGA.
- Narrow bus reduces cable size and cost
- Up to 2.38 Gbps throughput
- Up to 297.5 Megabytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead or 48-lead TSSOP package
- DS90C385 also available in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package

Block Diagrams

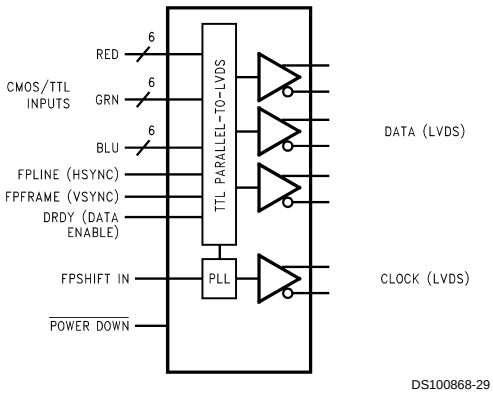
DS90C385



DS100868-1

Order Number DS90C385MTD or DS90C385SLC
See NS Package Number MTD56 or SLC64A

DS90C365



DS100868-29

Order Number DS90C365MTD
See NS Package Number MTD48

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.5V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec)	+260˚C
Solder reflow Temperature (20 sec for FBGA)	+220˚C
Maximum Package Power Dissipation Capacity @ 25˚C	
MTD56 (TSSOP) Package: DS90C385MTD	1.63 W
MTD48 (TSSOP) Package: DS90C365MTD	1.98 W
SLC64 (FBGA) Package:	
DS90C385SLC	2.0 W
Package Derating: DS90C385MTD	12.5 mW/˚C above +25˚C
Package Derating: DS90C365MTD	16 mW/˚C above +25˚C
DS90C385SLC	10.2 mW/˚C above +25˚C
ESD Rating	
(HBM, 1.5kΩ, 100pF)	> 7 kV
(EIAJ, 0Ω, 200 pF)	> 500V
Latch Up Tolerance @ 25˚C	> ±300mA

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Supply Noise Voltage (V_{CC})			100	mV_{PP}
TxCLKIN frequency	20		85	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}			+1.8	+10	µA
		V_{IN} = GND		−10	0		µA
LVDS DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states					35	mV
V_{OS}	Offset Voltage (Note 4)			1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between complimentary output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case DS90C385	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		31	45	mA
			f = 40 MHz		32	50	mA
			f = 65 MHz		37	55	mA
			f = 85 MHz		42	60	mA
ICCTG	Transmitter Supply Current 16 Grayscale DS90C385	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		29	38	mA
			f = 40 MHz		30	40	mA
			f = 65 MHz		35	45	mA
			f = 85 MHz		39	50	mA
ICCTW	Transmitter Supply Current Worst Case DS90C365	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		28	42	mA
			f = 40 MHz		29	47	mA
			f = 65 MHz		34	52	mA
			f = 85 MHz		39	57	mA

SGRAM 512K x 32 Bit x 2 Banks

Synchronous Graphic RAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual bank / Pulse $\overline{RAS}$
- MRS cycle with address key programs
  - CAS Latency (2, 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- DQM 0-3 for byte masking
- Auto & self refresh
- 32ms refresh period (2K cycle)
- 100 pin QFP / TQFP

Graphic Features

- SMRS cycle
  - Load mask register
  - Load color register
- Write Per Bit (Old Mask)
- Block Write (8 Columns)

GENERAL DESCRIPTION

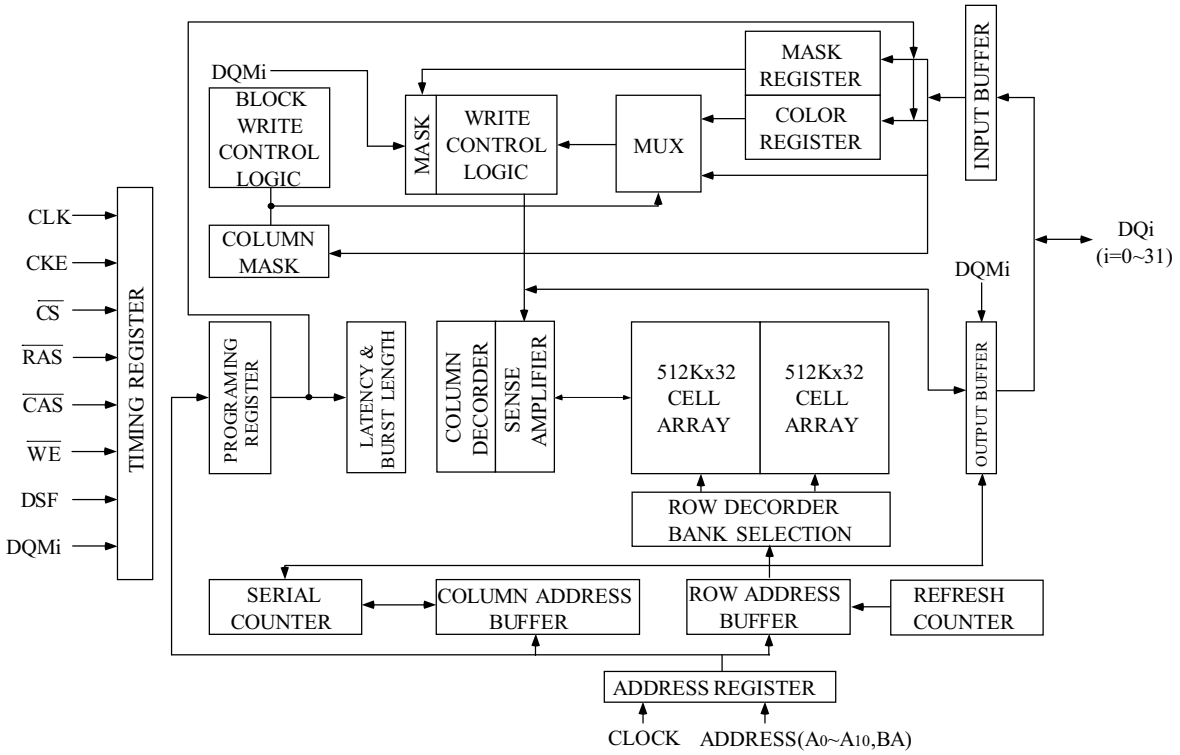
The M32L32321SA is 33, 554, 432 bits synchronous high data rate Dynamic RAM organized as 2 x 524, 288 words by 32 bits, fabricated with ESMT's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies , programmable burst length, and programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Write per bit and 8 columns block write improves performance in graphic systems.

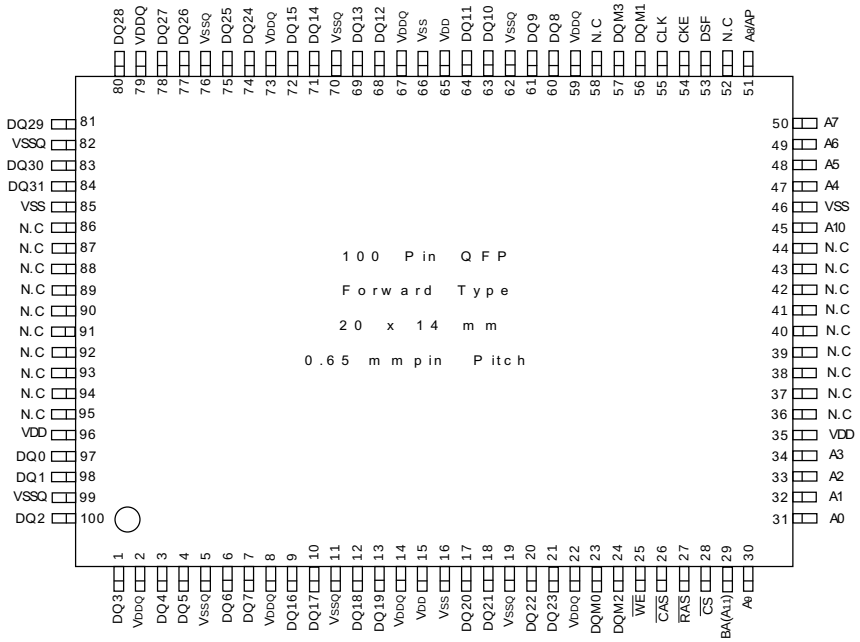
ORDERING INFORMATION

Part NO.	Cycle time	Clock Frequency	Access time@CL=3
M32L32321SA -5Q/-5F	5ns	200MHz	4.5ns
M32L32321SA -5.5Q/-5.5F	5.5ns	183MHz	5ns
M32L32321SA -6Q/-6F	6ns	166MHz	5.5ns
M32L32321SA -7Q/-7F	7ns	143MHz	6.0ns
M32L32321SA -8Q/-8F	8ns	125MHz	6.5ns

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enable device operation by masking or enabling all inputs except CLK, CKE and DQMi
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock+ tss prior to new command. Disable input buffers for power down in standby.
A0 ~ A10	Address	Row / column addresses are multiplexed on the same pins. Row address : RA0~RA10, column address : CA0~CA7
BA	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK With $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and Row precharge.
DQMi	Data Input/Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DQi	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
DSF	Define Special/ Function	Enables write per bit, block write and special mode register set.
V_{DD}/V_{SS}	Power Supply/ Ground	
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	

ABSOLUTE MAXIMUM RATINGS (Voltage referenced to V_{SS})

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

SGRAM 512K x 32 Bit x 2 Banks

Synchronous Graphic RAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual bank / Pulse $\overline{RAS}$
- MRS cycle with address key programs
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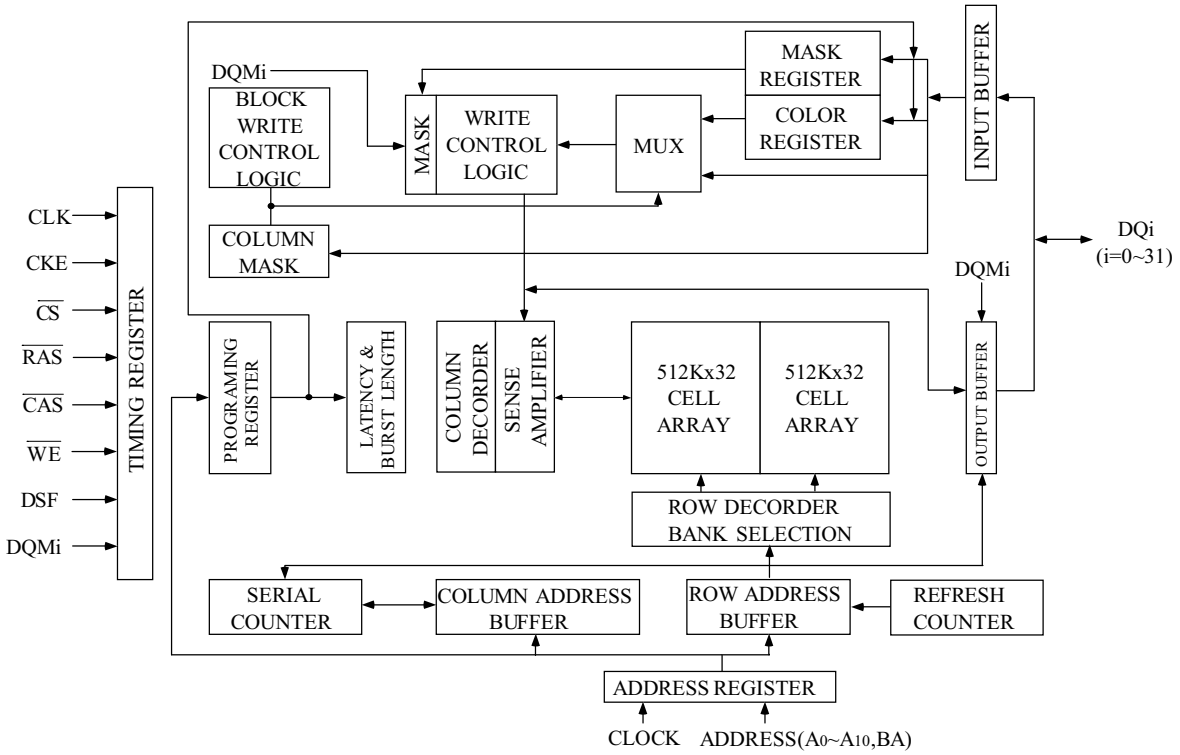
Write per bit and 8 columns block write improves performance in graphic systems.

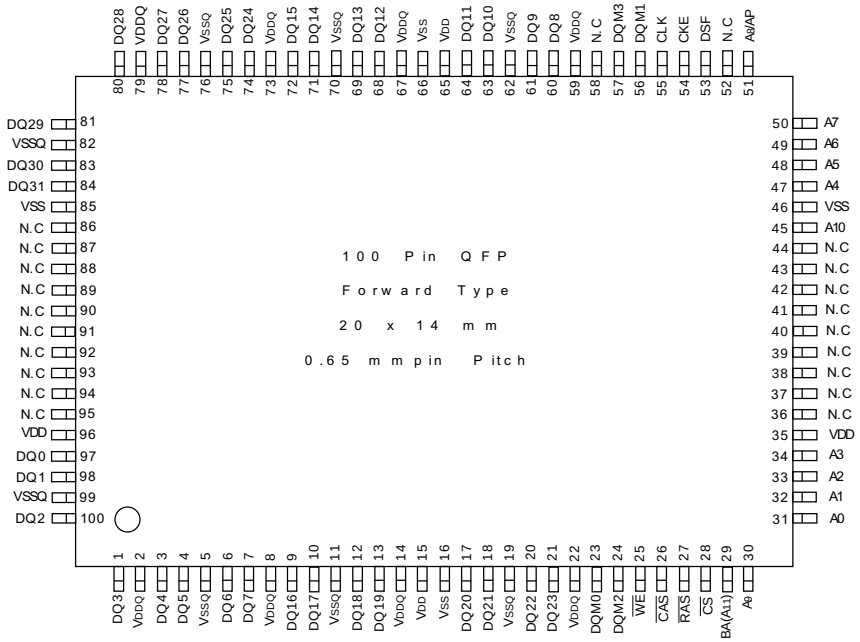
ORDERING INFORMATION

Part NO.	Cycle time	Clock Frequency	Access time@CL=3
M32L32321SA -5Q/-5F	5ns	200MHz	4.5ns
M32L32321SA -5.5Q/-5.5F	5.5ns	183MHz	5ns
M32L32321SA -6Q/-6F	6ns	166MHz	5.5ns
M32L32321SA -7Q/-7F	7ns	143MHz	6.0ns
M32L32321SA -8Q/-8F	8ns	125MHz	6.5ns

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enable device operation by masking or enabling all inputs except CLK, CKE and DQMi
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock+ tss prior to new command. Disable input buffers for power down in standby.
A0 ~ A10	Address	Row / column addresses are multiplexed on the same pins. Row address : RA0~RA10, column address : CA0~CA7
BA	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK With $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and Row precharge.
DQMi	Data Input/Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DQi	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
DSF	Define Special/ Function	Enables write per bit, block write and special mode register set.
V_{DD}/V_{SS}	Power Supply/ Ground	
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	

ABSOLUTE MAXIMUM RATINGS (Voltage referenced to V_{SS})

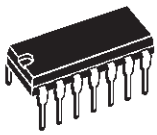
Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

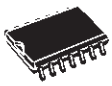
M74HC32

QUAD 2-INPUT OR GATE

- HIGH SPEED:
  t_{PD} = 8ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 1µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 32



DIP



SOP

TSSOP

ORDER CODES

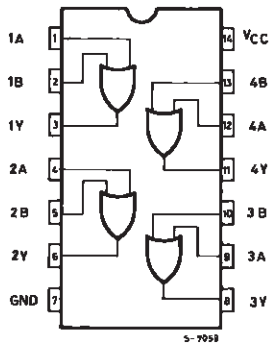
PACKAGE	TUBE	T & R
DIP	M74HC32B1R	
SOP	M74HC32M1R	M74HC32RM13TR
TSSOP		M74HC32TTR

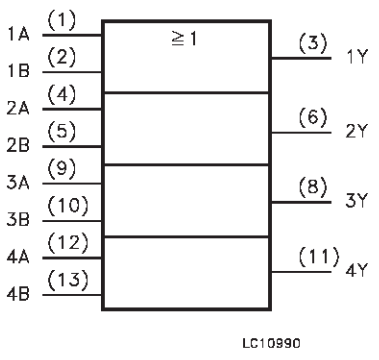
DESCRIPTION

The M74HC32 is an high speed CMOS QUAD 2-INPUT OR GATE fabricated with silicon gate C^2MOS technology.
The internal circuit is composed of 2 stages including buffer output, which enables high noise immunity and stable output.

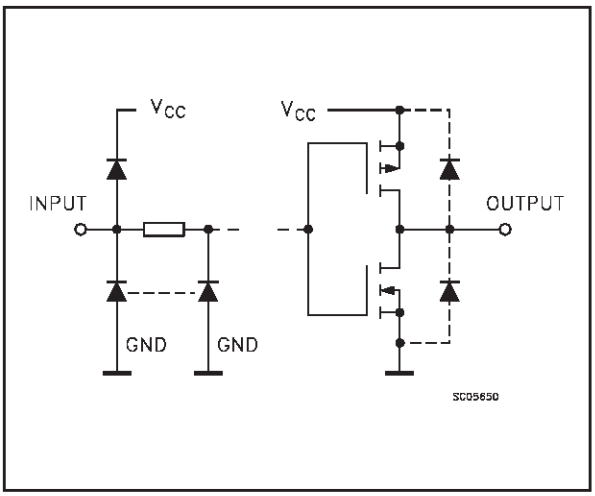
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			24	75		95		110	ns
		4.5			9	15		19		22	
		6.0			8	13		16		19	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			21						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per gate)

Remote 8-bit I/O expander for I²C-bus PCF8574

1 FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 µA maximum
- I²C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, or space-saving SO16 or SSOP20 packages.

2 GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C).

The device consists of an 8-bit quasi-bidirectional port and an I²C-bus interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address as shown in Fig.9.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

4 BLOCK DIAGRAM

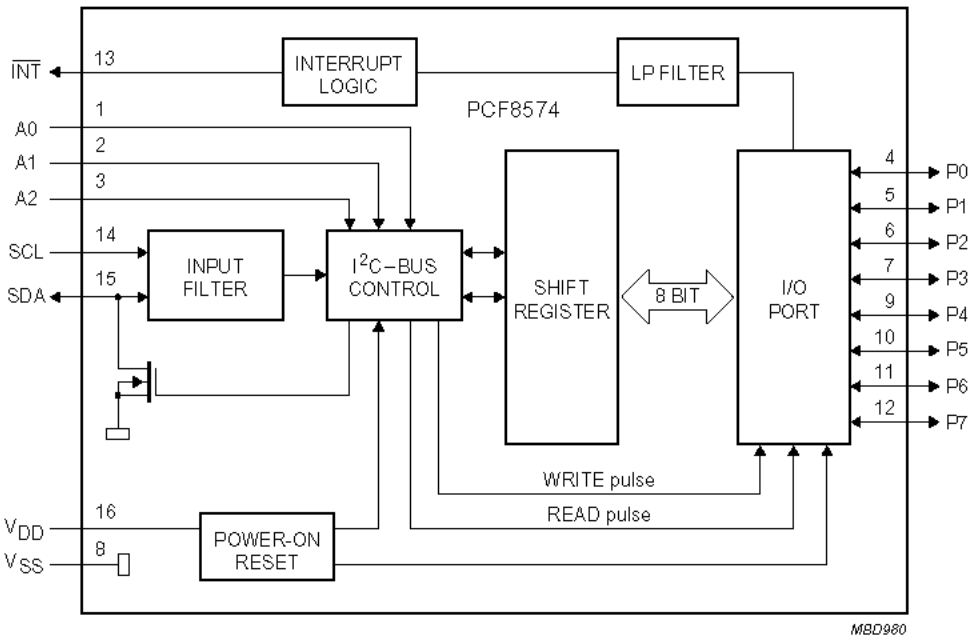
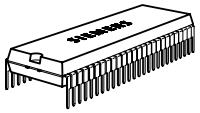


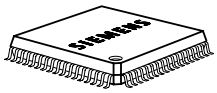
Fig.1 Block diagram (SOT38-1 and SOT162-1).

CMOS

1.5 Features



P-SDIP-52



P-MQFP-64

General

- Feature selection via special function register
- Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
- Supply Voltage 2.5 and 3.3 V
- ROM version package P-SDIP 52, P-MQFP64
- Romless version package P-MQFP100,P-LCC84

External Crystal and Programmable clock speed

- Single external 6MHz crystal, all necessary clocks are generated internally
- CPU clock speed selectable via special function registers.
- Normal Mode 33.33 Mhz CPU clock, Power Save mode 8.33 Mhz

Microcontroller Features

- 8bit 8051 instruction set compatible CPU.
- 33.33-MHz internal clock (max.)
- 0.360 µs (min.) instruction cycle
- Two 16-bit timers
- Watchdog timer
- Capture compare timer for infrared remote control decoding
- Pulse width modulation unit (2 channels 14 bit, 6 channels 8 bit)
- ADC (4 channels, 8 bit)
- UART

Type	Package
TVTEXT PRO (ROM)	P-SDIP-52, P-MQFP-64
TVTEXT PRO (ROMless)	P-MQFP-100, P-LCC-84

Memory

- Non-multiplexed 8-bit data and 16 … 20-bit address bus (ROMless Version)
- Memory banking up to 1Mbyte (Romless version)
- Up to 128 Kilobyte on Chip Program ROM
- Eight 16-bit data pointer registers (DPTR)
- 256-bytes on-chip Processor Internal RAM (IRAM)
- 128bytes extended stack memory.
- Display RAM and TXT/VPS/PDC/WSS-Acquisition-Buffer directly accessible via MOVX
- UP to 16KByte on Chip Extended RAM(XRAM) consisting of;
  - 1 Kilobyte on-chip ACQ-buffer-RAM (access via MOVX)
  - 1 Kilobyte on-chip extended-RAM (XRAM, access via MOVX) for user software
  - 3 Kilobyte Display Memory

Display Features

- ROM Character Set Supports all East and West European Languages in single device
- Mosaic Graphic Character Set
- Parallel Display Attributes
- Single/Double Width/Height of Characters
- Variable Flash Rate
- Programmable Screen Size (25 Rows x 33...64 Columns)
- Flexible Character Matrixes (HxV) 12 x 9...16
- Up to 256 Dynamical Redefinable Characters in standard mode; 1024 Dynamical Redefinable Characters in Enhanced Mode
- CLUT with up to 4096 color combinations
- Up to 16 Colors per DRCS Character
- One out of Eight Colors for Foreground and Background Colors for 1-bit DRCS and ROM Characters
- Shadowing
- Contrast Reduction
- Pixel by Pixel Shiftable Cursor With up to 4 Different Colors
- Support of Progressive Scan and 100 Hz.
- 3 X 4Bits RGB-DACs On-Chip
- Free Programmable Pixel Clock from 10 MHZ to 32MHz
- Pixel Clock Independent from CPU Clock
- Multinorm H/V-Display Synchronization in Master or Slave Mode

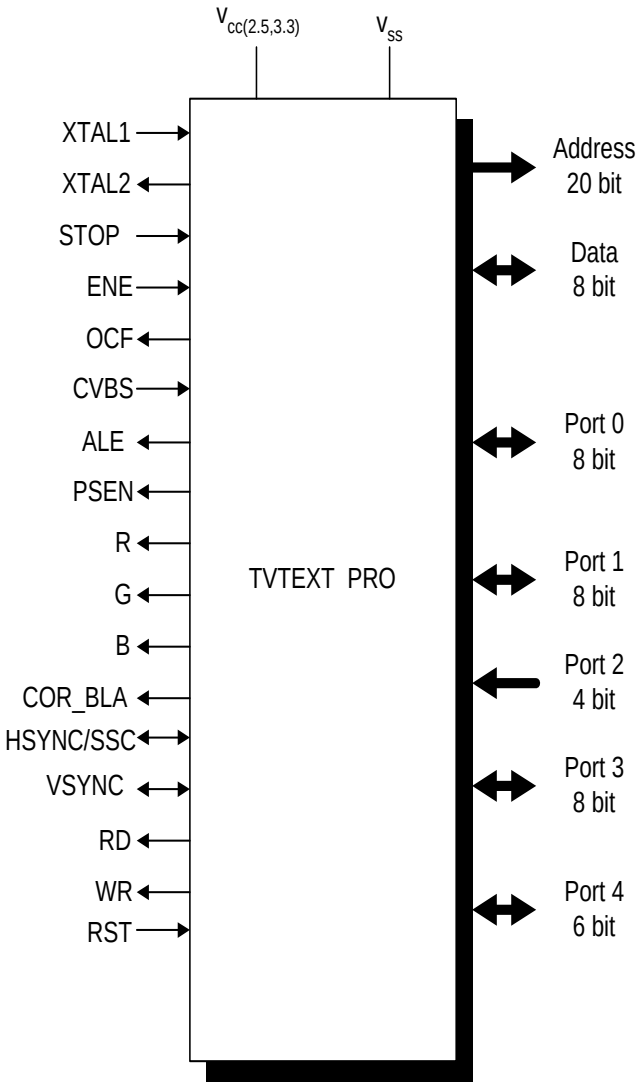
Acquisition Features

- Multistandard Digital Data Slicer
- Parallel Multi-norm Slicing (TTX, VPS, WSS, CC, G+)
- Four Different Framing Codes Available
- Data Caption only Limited by available Memory
- Programmable VBI-buffer
- Full Channel Data Slicing Supported
- Fully Digital Signal Processing
- Noise Measurement and Controlled Noise Compensation
- Attenuation Measurement and Compensation
- Group Delay Measurement and Compensation
- Exact Decoding of Echo Disturbed Signals

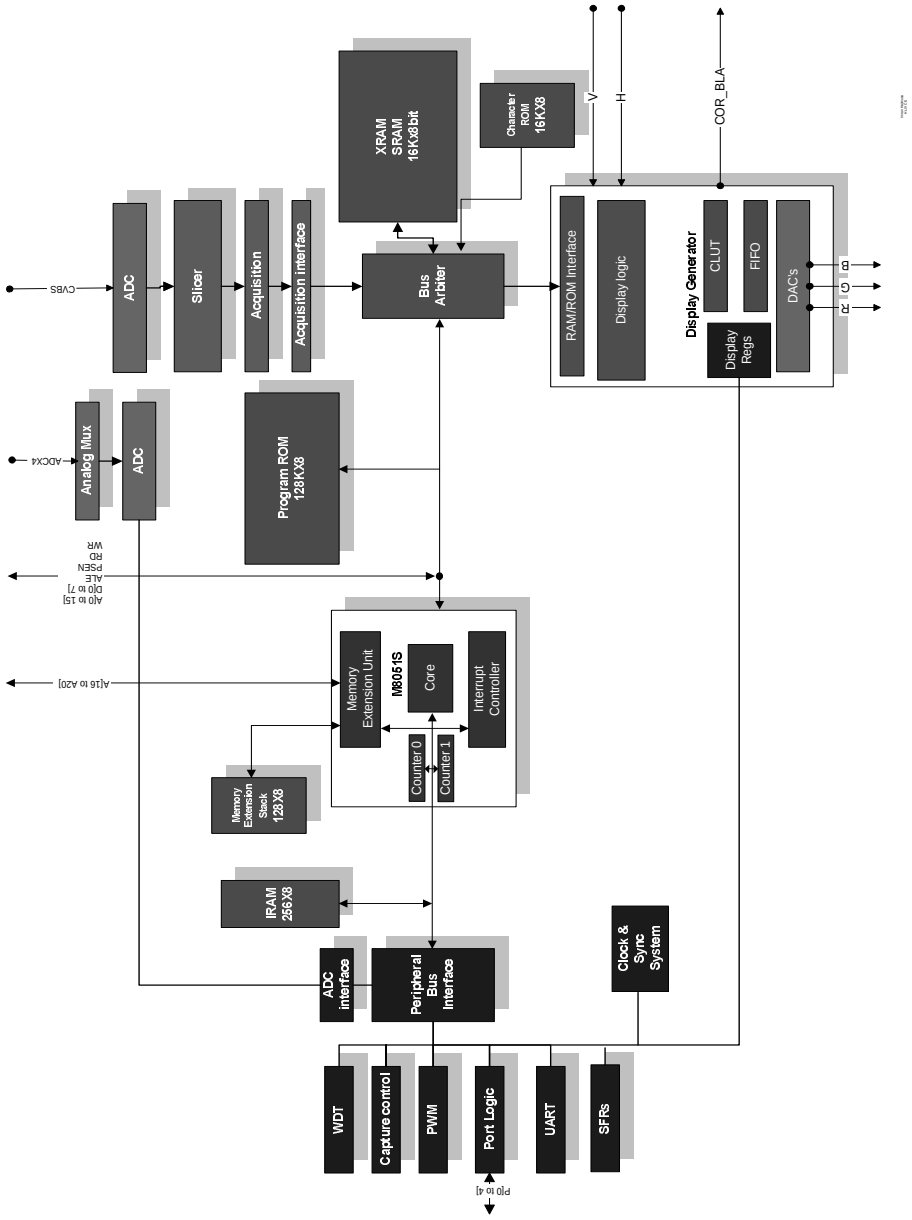
Ports

- One 8-bit I/O-port with open drain output and optional I^2C Bus emulation suport(Port0)
- Two 8-bit multifunction I/O-ports (Port1, Port3)
- One 4-bit port working as digital or analog inputs for the ADC (Port2)
- One 2-bit I/O port with secondary functions (P4.2, 4.3, 4.7)
- One 4-bit I/O-port with secondary function (P4.0, 4.1, 4.4) (Not available in P-SDIP 52)

1.6 Logic Symbol



1.7 Block diagram

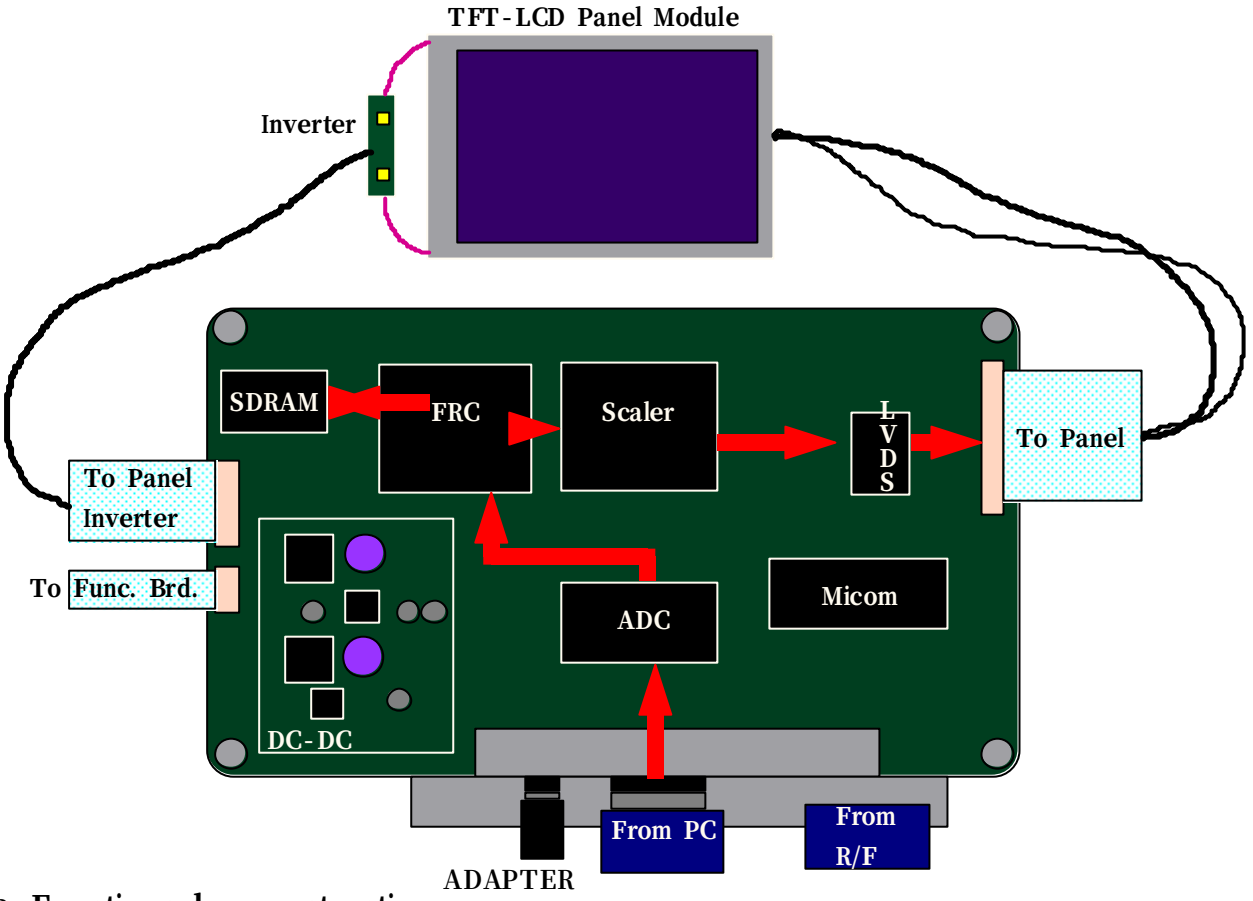


TFT-LCD Monitor

1. What is TFT-LCD TV (Monitor)?

It is a TV (Monitor) with display element of TFT-LCD. It is a new concept TV (Monitor) compared to the existing CRT TV (Monitor) in the fact of reducing space and consumption power.

2. Construction of the TFT-LCD TV (Monitor)



3. Functions by construction

■ TFT-LCD Panel Module

-The color TFT-LCD is divided in a-Si (amorphous silicon) TFT and Si (Polysilicon) TFT by the kind of TFT elements. The flat TFT-LCD with a-Si TFT is the most widely used.

- **The TFT-LCD can be determined by 3 units.**

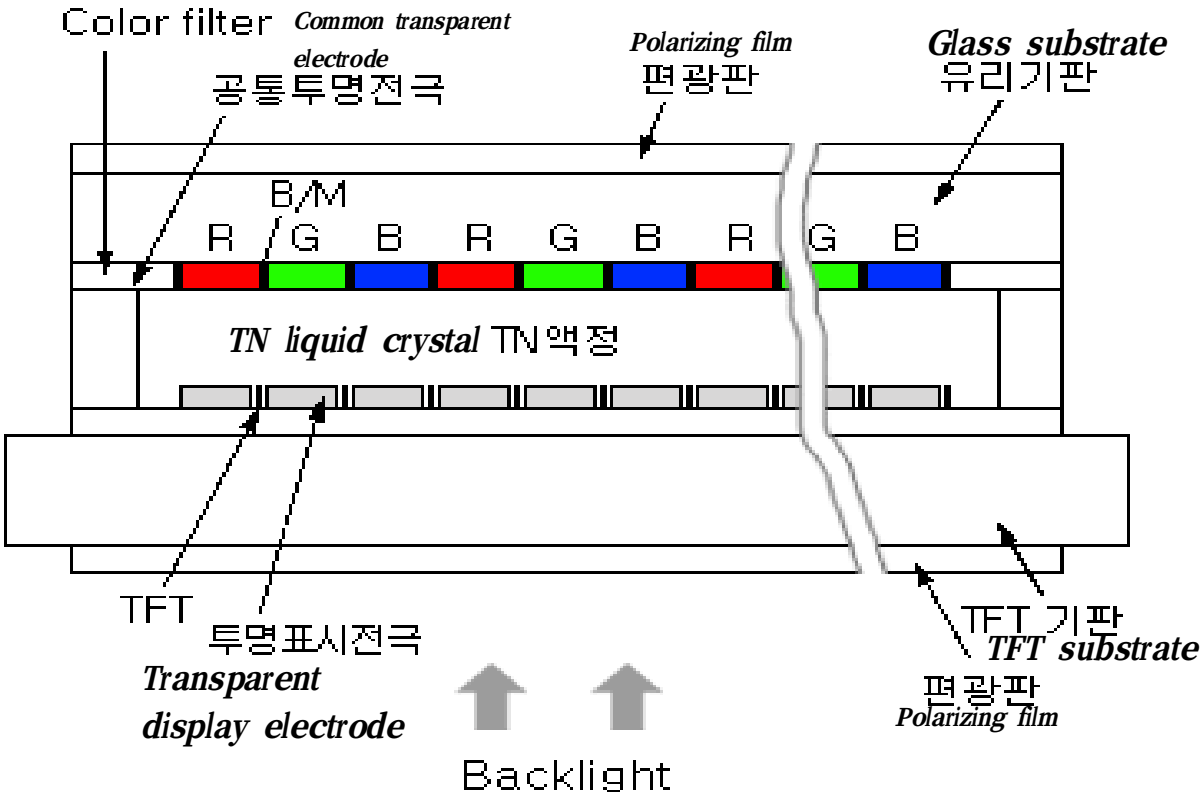
-The first, a panel with inserting liquid crystal between substrates.

-The seconds, Driver LSI for driving the panel and Drive circuit unit with PCB (Printed Circuit Board) to where various circuit elements are attached.

- The third, Chassis including the backlight.

☞ The assembly consists of the above is called TFT-LCD Module.

- TFT-LCD is one of a subsystem to charge the display function in the system such as Notebook PC, TV, and Monitor.



1) Panel의 기능은 Backlignt Unit에서 입사된 백색 평면관을 구동 회로 Unit으로부터 입력된 개개 화소의 신호전압에 따라 화소에 투과되는 빛을 제어하여 Color영상을 표현하는 역할을 한다.

2)BackLight Unit

It makes a plane light, which has even luminosity, from a fluorescent lamp used as the light resource. The thickness of module and consumption of electricity depends on making thinner thickness of the unit and improving coefficient of utilization of light. The light from backlight gradually decreases in brightness immediately after penetrating the display module unit. Only 5% of light coming into the backlight penetrates the front polarizer.

3)Driving circuit and Chassis unit

The TFT LCD panel consists of TFT array and color filter substrates. The drive circuit including driver IC must be installed in the peripheral part. The drive circuit takes multi layer PCB type and for the circuit part, SMT (surface mounting technology) is used for thinness and high density. Driver IC is made in the form of TCP (Tape carrier package) and connected between PCB and panel.

The drive circuits of TFT LCD panel and backlight unit made as above are completed with chassis unit and has a type of assembled parts. It is called TFT module.

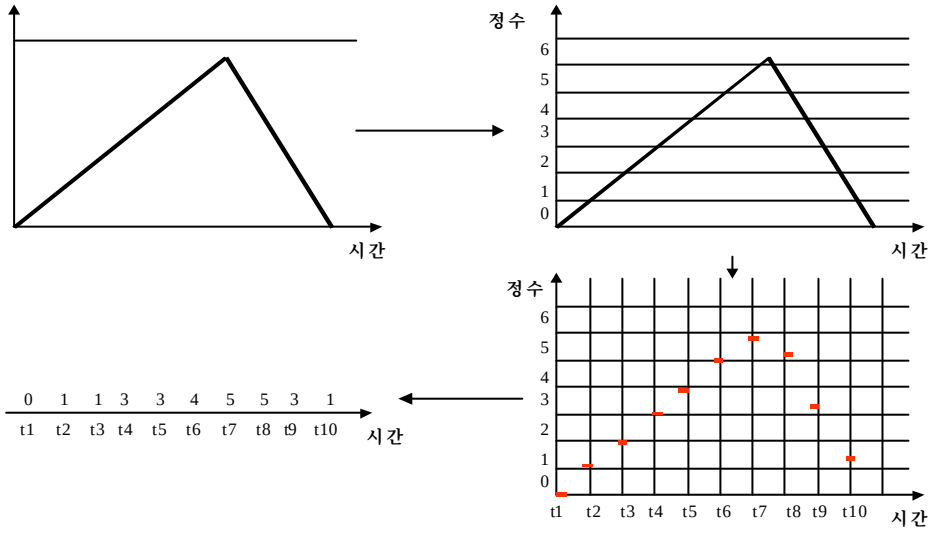
■ *Inverter*

It is a supplying device of current to supply power to backlight, and it controls luminosity of the backlight by supplying amount of power to the backlight.

■ ADC (Analog to Digital Converter)

It is a circuit to covert the inputted analog signal from PC to the digital signal for using it at the end of ADC. It is important to determine a picture quality. ADC consists of three parts: AMP unit, AD unit, and PLL unit. AMP unit amplifies the inputted analog signal to adjust the gain. AMP is necessary for expressing the precise gray because the difference of gain among PCs is existed. When AD unit converts analog signal to digital signal, the signal with adjusted gain through AMP is divided in 256 by voltage from bottom reference to top reference, and the digital signal (0~255) is given to each section to convert analog signal to digital signal. PLL makes a clock, which determines the time to convert analog to digital.

There is an importance to convert analog signal to digital signal: convert exact number of data in exact time. The transmitted data from PC is a data converted digital signal to analog signal. Therefore, a display without picture noise is possible by getting the exact digital signal from PC.



■ Scaler

It converts the resolution of the inputted signal of TV (Monitor) to the resolution, which you wish. Please refer to the attachment for technical part of the scaling.

■ LVDS (Low Voltage Differential Signal)

It is for interface of panel. It is a data type to transmit the Vp-p by 345mV. It is transmitted at least 28 times faster than the speed of output clock, and it reduces the number of connectors at least 1/3 in comparison with the TTL signal. The EMI character is improved by transmitting the Vp-p to low.