C141-E203-01EN

MHT2080BH, MHT2060BH, MHT2040BH

DISK DRIVES

PRODUCT MANUAL

FUJITSU

FOR SAFE OPERATION

Handling of This Manual

This manual contains important information for using this product. Read thoroughly before using the product. Use this product only after thoroughly reading and understanding especially the section “Important Alert Items” in this manual. Keep this manual handy, and keep it carefully.

FUJITSU makes every effort to prevent users and bystanders from being injured or from suffering damage to their property. Use the product according to this manual.

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The contents of this manual may be revised without prior notice.

Revision History

Edition	Date	Revised section (*1) (Added/Deleted/Altered)	Details
01	2004-02-27		

*1 Section(s) with asterisk (*) refer to the previous edition when those were deleted.

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Preface

This manual describes MHT2080BH/ MHT2060BH/ MHT2040BH models of the MHT Series, 2.5-inch hard disk drives. These drives have a built-in controller that is compatible with the Serial-ATA interface.

This manual describes the specifications and functions of the drives and explains in detail how to incorporate the drives into user systems. This manual assumes that the reader has a basic knowledge of hard disk drives and their implementations in computer systems.

This manual consists of seven chapters and sections explaining the special terminology and abbreviations used in this manual:

Overview of Manual

CHAPTER 1 Device Overview

This chapter gives an overview of the disk drive and describes their features.

CHAPTER 2 Device Configuration

This chapter describes the internal configurations of the disk drive and the configuration of the systems in which they operate.

CHAPTER 3 Installation Conditions

This chapter describes the external dimensions, installation conditions, and switch settings of the disk drive.

CHAPTER 4 Theory of Device Operation

This chapter describes the operation theory of the disk drive.

CHAPTER 5 Interface

This chapter describes the interface specifications of the disk drive.

CHAPTER 6 Operations

This chapter describes the operations of the disk drive.

Glossary

The glossary describes the technical terms that need to be understood to read this manual.

Acronyms and Abbreviations

This section gives the meanings of the definitions used in this manual.

Conventions for Alert Messages

This manual uses the following conventions to show the alert messages. An alert message consists of an alert signal and alert statements. The alert signal consists of an alert symbol and a signal word or just a signal word.

The following are the alert signals and their meanings:

⚠CAUTION	This indicates a hazardous situation *could* result in *minor* or *moderate personal injury* if the user does not perform the procedure correctly. This alert signal also indicates that damages to the product or other property *may* occur if the user does not perform the procedure correctly.
IMPORTANT	This indicates information that could help the user use the product more efficiently.

In the text, the alert signal is centered, followed below by the indented message. A wider line space precedes and follows the alert message to show where the alert message begins and ends. The following is an example:

(Example)

⚠CAUTION

Data corruption: Avoid mounting the disk drive near strong magnetic sources such as loud speakers. Ensure that the disk drive is not affected by external magnetic fields.

The main alert messages in the text are also listed in the “Important Alert Items.”

Operating Environment

This product is designed to be used in offices or computer rooms.

Conventions

An MHT series device is sometimes simply referred to as a "hard disk drive," "HDD," "drive," or "device" in this document.

Decimal numbers are represented normally.

Hexadecimal numbers are represented as shown in the following examples: X'17B9', 17B9h, 17B9H, or 17B9H.

Binary numbers are represented as shown in the following examples: 010 or 010b.

Serial-ATA may be referred to as "SATA."

Attention

Please forward any comments you may have regarding this manual.

To make this manual easier for users to understand, opinions from readers are needed. Please write your opinions or requests on the Comment at the back of this manual and forward it to the address described in the sheet.

Liability Exception

"Disk drive defects" refers to defects that involve adjustment, repair, or replacement.

Fujitsu is not liable for any other disk drive defects, such as those caused by user misoperation or mishandling, inappropriate operating environments, defects in the power supply or cable, problems of the host system, or other causes outside the disk drive.

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Important Alert Items

Important Alert Messages

The important alert messages in this manual are as follows:

⚠CAUTION

A hazardous situation *could* result in *minor* or *moderate personal injury* if the user does not perform the procedure correctly. Also, damage to the product or other property, *may* occur if the user does not perform the procedure correctly.

Task	Alert message	Page
Normal Operation	**Data corruption:** Avoid mounting the disk drive near strong magnetic sources such as loud speakers. Ensure that the disk drive is not affected by external magnetic fields. **Damage:** Do not press the cover of the disk drive. Pressing it too hard, the cover and the spindle motor contact, which may cause damage to the disk drive. **Static:** When handling the device, disconnect the body ground (500 kΩ or greater). Do not touch the printed circuit board, but hold it by the edges.	3-7

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Manual Organization

MHT2080BH, MHT2060BH, MHT2040BH DISK DRIVES PRODUCT MANUAL (C141-E203) <This manual>	• Device Overview • Device Configuration • Installation Conditions • Theory of Device Operation • Interface • Operations
MHT2080BH, MHT2060BH, MHT2040BH DISK DRIVES MAINTENANCE MANUAL (C141-F068)	• Maintenance and Diagnosis • Removal and Replacement Procedure

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CHAPTER 1 Device Overview

Overview and features are described in this chapter, and specifications and power requirement are described.

The disk drive is 2.5-inch hard disk drives with built-in disk controllers. These disk drives use the SATA interface protocol which has a high-speed interface data transfer rate.

1.1 Features

1.1.1 Functions and performance

The following features of the disk drive is described.

(1) Compact

The disk drive has 1 disk or 2 disks of 65 mm (2.5 inches) diameter, and its height is 9.5 mm (0.374 inch).

(2) Large capacity

The disk drive can record up to 40 GB (formatted) on one disk using the RLL recording method and 30 recording zone technology. The disk drive has a formatted capacity of 80 GB (MHT2080BH), 60 GB (MHT2060BH), 40 GB (MHT2040BH) respectively.

(3) High-speed Transfer rate

The disk drive (the MHT Series) has an internal data rate up to 53.9 MB/s. The disk drive supports an external data rate up to 1.5Gbps (Serial-ATA Generation-1).

(4) Average positioning time

Use of a rotary voice coil motor in the head positioning mechanism greatly increases the positioning speed. The average positioning time is 12 ms (at read).

1.1.2 Adaptability

(1) Power save mode

The disk drive is ideal for applications since it supports the power save mode function that works in each of the Idle, Standby and Sleep modes and has the Partial and Slumber interface power management functions.

(2) Wide temperature range

The disk drive can be used over a wide temperature range (5 °C to 55 °C).

(3) Low noise and vibration

In Ready status (while the device is waiting for any commands), the Sound Power level of the disk drives in idle mode is 2.2 Bels [MHT2040BH]/2.8 Bels [MHT2080BH, MHT2060BH]. The Sound Pressure level is 25.0 dB [MHT2040BH]/34.0 dB [MHT2080BH, MHT2060BH] as measured 0.3 m from the drive in Idle mode.

(4) High resistance against shock

The Load/Unload mechanism is highly resistant against non-operation shock up to 8820 m/s^2 (900G).

1.1.3 Interface

(1) Connection to SATA interface

The disk drive has built-in controllers compatible with the SATA interface.

(2) Data buffer

The disk drive use a 2MB or 8MB data buffer to transfer data between the host and the disk media.

In combination with the read-ahead cache system described in item (3) and the write cache described in item (6), the buffer contributes to efficient I/O processing.

(3) Read-ahead cache system

After the execution of a disk read command, the disk drive automatically reads the subsequent data block and writes it to the data buffer (read ahead operation). This cache system enables fast data access. The next disk read command would normally cause another disk access. But, if the read ahead data corresponds to the data requested by the next read command, the data in the buffer can be transferred instead.

(4) Error correction and retry by ECC

If a recoverable read error occurs, the disk drive itself attempt error recovery. The ECC has improved buffer error correction for correctable data errors.

(5) Self-diagnosis

The disk drive has a diagnostic function to check operation of the controller and disk drive. Executing a diagnostic function of the smart command invokes self-diagnosis.

(6) Write cache

When the disk drive receives a write command, the disk drive posts the command completion at completion of transferring data to the data buffer completion of writing to the disk media. This feature reduces the access time at writing.

1.2 Device Specifications

1.2.1 Specifications summary

Table 1.1 shows the specifications of the disk drives.

Table 1.1 Specifications (1/2)

	MHT2080BH	MHT2060BH	MHT2040BH
Format Capacity (*1, *2)	80 GB	60 GB	40 GB
Number of Sectors (User)	156,301,488 sectors	117,210,240 sectors	78,140,160 sectors
Bytes per Sector	512 bytes		
Rotational Speed	5,400 rpm ± 1%		
Average Latency	5.56 ms		
Positioning time (read and seek) • Minimum (Track-Track) • Average • Maximum (Full)	 1.5 ms (typ.) Read: 12ms (typ.) 22 ms (typ.)		
Start time	4.0 sec (typ.)		
Interface	Compliant with ATA/ATAPI-7, SATA1.0a, and SATA II 1.0 [Cable length: less than 1.0m (39.37 inchs)]		
Data Transfer Rate (*2) • To/From Media • To/From Host	 53.9 MB/s Max. 1.5Gbps Max (Serial-ATA Generation-1)		
Data Buffer Size (*3)	8MB		
Physical Dimensions (Height × Depth × Width)	9.5 mm × 100.0 mm × 70.0 mm (*4)		
Weight	99 g (max)		

*1: Capacity under the LBA mode.

*2: 1GB = 1,000,000,000 bytes, and 1 MB = 1,000,000 bytes.

*3: 1MB = 1,048,576 bytes.

*4: The value of Depth (=100.0 mm) does not include PCBA (Printed Circuit Board Assembly). Refer to Section 3.1.

Table 1.1 lists the formatted capacity, number of logical cylinders, number of heads, and number of sectors of every model for which the CHS mode has been selected using the BIOS setup utility on the host.

Table 1.1 Specifications (2/2)

Model	Capacity (*1)	No. of Cylinder	No. of Heads	No. of Sectors
MHT2080BH	8.45 GB	16,383	16	63
MHT2060BH	8.45 GB	16,383	16	63
MHT2040BH	8.45 GB	16,383	16	63

*1 Indicates the storage capacity when the numbers of logical cylinders, heads, and sectors are specified as shown in this table.

1.2.2 Model and product number

Table 1.2 lists the model names and product numbers of the disk drive.

The model name does not necessarily correspond to the product number as listed in Table 1.2 since some models have been customized and have specifications that are different from those for the standard model.

If a disk drive is ordered as a replacement drive, the product number must be the same as that of the drive being replaced.

Table 1.2 Examples of model names and product numbers

Model Name	Capacity (user area)	Mounting screw	Order No.
MHT2080BH	80 GB	M3 depth 3	CA06500-B048
MHT2060BH	60 GB	M3 depth 3	CA06500-B046
MHT2040BH	40 GB	M3 depth 3	CA06500-B024

1.3 Power Requirements

(1) Input Voltage

- + 5 V ± 5 %
- It is unnecessary for this drive to supply +3.3V and +12V power supplies.

(2) Ripple

	+5 V
Maximum	100 mV (peak to peak)
Frequency	DC to 1 MHz

(3) A negative voltagelike the bottom figure isn't to occur at +5 V when power is turned off and, a thing with no ringing.

Permissible level: −0.2 V

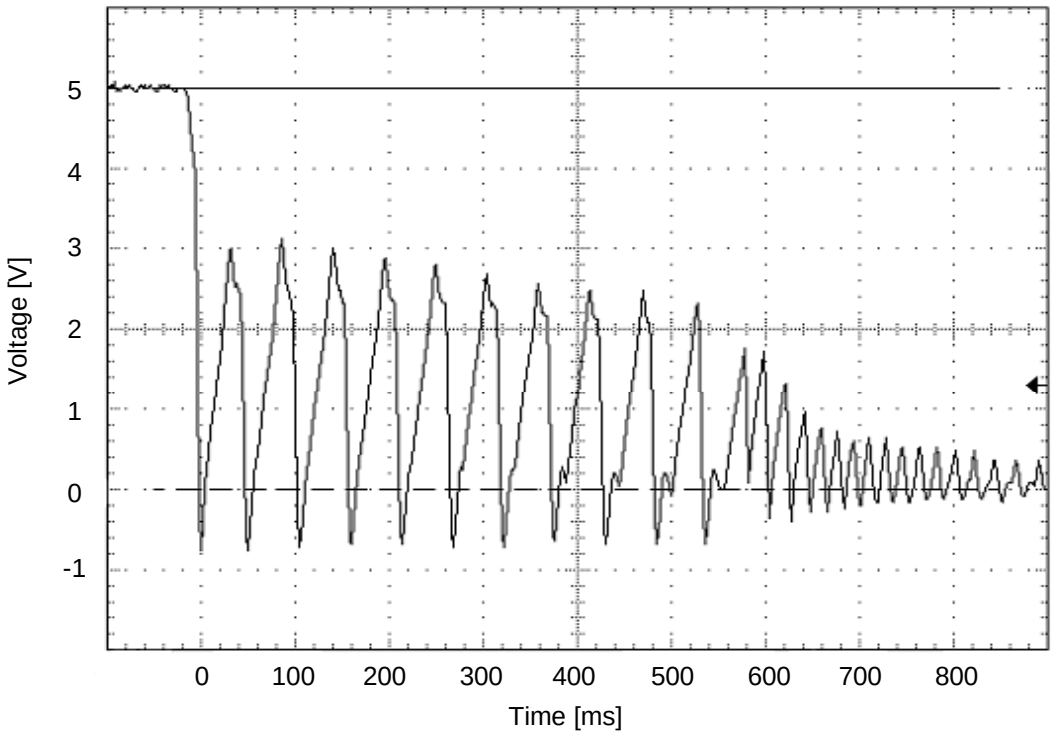

Figure 1.1 Negative voltage at +5 V when power is turned off

(4) Current Requirements and Power Dissipation

Table 1.3 lists the current and power dissipation (typical).

Table 1.3 Current and power dissipation

	Typical RMS Current	Typical Power (*3)
	MHT2080BH, MHT2060BH, MHT2040BH	MHT2080BH, MHT2060BH, MHT2040BH
Spin up (*1)	1.0 A	5.0 W
Idle (*6)	170 mA	0.85 W
R/W (on track) (*2)	Read 460 mA / Write 460mA	Read 2.3 W / Write 2.3 W
Seek (*5)	500 mA	2.5 W
Standby (*6)	50 mA	0.25 W
Sleep (*6)	20 mA	0.1 W
Energy Efficiency (*4)	—	0.011 W/GB (rank E / MHT2080BH) 0.014 W/GB (rank E / MHT2060BH) 0.021 W/GB (rank D / MHT2040BH)

*1 Maximum current and power at starting spindle motor.

*2 Current and power level when the operation (command) that accompanies a transfer of 63 sectors is executed 3 times in 100 ms.

*3 Power requirements reflect nominal values for +5 V power.

*4 Energy efficiency based on the Law concerning the Rational Use of Energy indicates the value obtained by dividing power consumption by the storage capacity. (Japan only)

*5 The seek average current is specified based on three operations per 100 msec.

*6 IPM mode: Slumber mode.

(5) Current fluctuation (Typ.) at +5 V when power is turned on

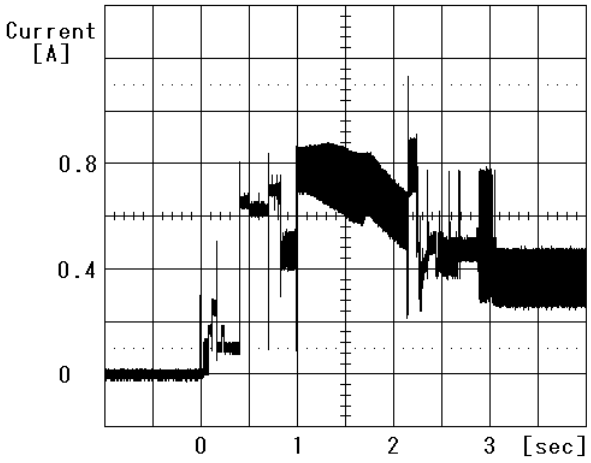

Figure 1.2 Current fluctuation (Typ.) at +5 V when power is turned on

(6) Power on/off sequence

The voltage detector circuits monitor +5 V. The circuits do not allow a write signal if either voltage is abnormal. These prevent data from being destroyed and eliminates the need to be concerned with the power on/off sequence.

1.4 Environmental Specifications

Table 1.4 lists the environmental specifications.

Table 1.4 Environmental specifications

Item	Specification
Temperature	
• Operating	5 °C to 55 °C (ambient) 5 °C to 60 °C (disk cover surface)
• Non-operating	–40 °C to 65 °C
• Thermal Gradient	20 °C/h or less
Humidity	
• Operating	8 % to 90 % RH (Non-condensing)
• Non-operating	5 % to 95 % RH (Non-condensing)
• Maximum Wet Bulb	29 °C (Operating) 40 °C (Non-operating)
Altitude (relative to sea level)	
• Operating	–300 to 3,000 m
• Non-operating	–300 to 12,000 m

1.5 Acoustic Noise

Table 1.5 lists the acoustic noise specification.

Table 1.5 Acoustic noise specification

Item	Specification (typical)
• Idle mode (DRIVE READY)	
Sound Power	2.2 Bels [MHT2040BH] 2.8 Bels [MHT2080BH/MHT2060BH]
Sound Pressure (at 0.3m)	25.0 dB [MHT2040BH] 34.0 dB [MHT2080BH/MHT2060BH]

1.6 Shock and Vibration

Table 1.6 lists the shock and vibration specification.

Table 1.6 Shock and vibration specification

Item	Specification
Vibration (Swept sine, 1/4 octave per minute)	
• Operating	5 to 500 Hz, 9.8m/s^2 0-peak (1G 0-peak) (without non-recovered errors)
• Non-operating	5 to 500 Hz, 49m/s^2 0-peak (5G 0-peak) (no damage)
Shock (half-sine pulse)	
• Operating	2205 m/s^2 0-peak (225G 0-peak) 2ms duration (without non-recovered errors)
• Non-operating	8820 m/s^2 0-peak (900G 0-peak) 1ms duration 1176 m/s^2 0-peak (120G 0-peak) 11ms duration (no damage)

1.7 Reliability

(1) Mean time between failures (MTBF)

Conditions of 300,000 h	Power-on time	250H/month or less 3000H/years or less
	Operating time	20 % or less of power-on time
	Environment	5 to 55 °C/8 to 90 % But humidity bulb temperature 29 °C or less

MTBF is defined as follows:

$$\text{MTBF} = \frac{\text{Total operation time in all fields}}{\text{number of device failure in all fields (*1)}} \text{ (H)}$$

*1 "Disk drive defects" refers to defects that involve repair, readjustment, or replacement. Disk drive defects do not include failures caused by external factors, such as damage caused by handling, inappropriate operating environments, defects in the power supply host system, or interface cable.

(2) Mean time to repair (MTTR)

The mean time to repair (MTTR) is 30 minutes or less, if repaired by a specialist maintenance staff member.

(3) Service life

In situations where management and handling are correct, the disk drive requires no overhaul for five years when the DE surface temperature is less than 48 °C. When the DE surface temperature exceeds 48 °C, the disk drives requires no overhaul for five years or 20,000 hours of operation, whichever occurs first. Refer to item (3) in Subsection 3.2 for the measurement point of the DE surface temperature. Also the operating conditions except the environment temperature are based on the MTBF conditions.

(4) Data assurance in the event of power failure

Except for the data block being written to, the data on the disk media is assured in the event of any power supply abnormalities. This does not include power supply abnormalities during disk media initialization (formatting) or processing of defects (alternative block assignment).

1.8 Error Rate

Known defects, for which alternative blocks can be assigned, are not included in the error rate count below. It is assumed that the data blocks to be accessed are evenly distributed on the disk media.

(1) Unrecoverable read error

Read errors that cannot be recovered by maximum read retries of drive without user's retry and ECC corrections shall occur no more than 10 times when reading data of 10^{14} bits. Read retries are executed according to the disk drive's error recovery procedure, and include read retries accompanying head offset operations.

(2) Positioning error

Positioning (seek) errors that can be recovered by one retry shall occur no more than 10 times in 10^{7} seek operations.

1.9 Media Defects

Defective sectors are replaced with alternates when the disk drive is formatted prior to shipment from the factory (low level format). Thus, the hosts see a defect-free devices.

Alternate sectors are automatically accessed by the disk drive. The user need not be concerned with access to alternate sectors.

1.10 Load/Unload Function

The Load/Unload function is a mechanism that loads the head on the disk and unloads the head from the disk.

The product supports a minimum of 300,000 normal Load/Unload cycles. Normal Unload is a normal head unloading operation and the commands listed below are executed.

- COMRESET signal asserted
- STANDBY command issued
- STANDBY IMMEDIATE command issued
- SLEEP command issued
- IDLE command issued
- SLUMBER signal transferred
  (PMREQ_S signal is transferred from the host or the drive, and the host responds with PMACK signal.)

Emergency Unload other than Normal Unload is performed when the power is shut down while the heads are still loaded on the disk.
The product supports the Emergency Unload a minimum of 20,000 times.
When the power is shut down, the controlled Normal Unload cannot be executed. Therefore, the number of Emergency other than Normal Unload is specified.

Remark:

We recommend cutting the power supply of the HDD for this device after the Head Unload operation completes. The recommended power supply cutting sequence for this device is as follows:

1) Disk Flush

   Flush Cache command execution.

2) Head Unload

   Standby Immediate command execution.

3) Wait Status

   Checking whether bit 7 of the status register was set to '0'.
   (wait to complete STANDBY IMMEDIATE command)

4) HDD power supply cutting

1.11 Advanced Power Management

The disk drive shifts to the three kinds of APM modes automatically under the Idle condition.

The APM mode can be chosen with a Sector Count register of the SET FEATURES(EF) command.

In APM Mode-1, which is the APM default mode, the operation status shifts till it finally reaches "Low Power Idle."

The disk drive complies with the three kinds of APM modes that a command from the host is required.

FR = 05h : Enable APM

SC = C0h - FEh : Mode-0 Active Idle → Low Power Idle

SC = 80h - BFh : Mode-1 Active Idle → Low Power Idle (Default)

SC = 01h - 7Fh : Mode-2 Active Idle → Low Power Idle → Standby

FR = 85h : Disable APM (Set Mode-0)

Active Idle:	The head is in a position of extreme inner in disk medium.
Low Power Idle:	The head is unloaded from disk. The spindle motor rotates.
Standby:	The spindle motor stops.

Table 1.7 Advanced power management

APM Mode	Active Idle	Low Power Idle (Unload)	Standby (Spin Off)
Mode-0	0.2-1.2 sec	15 min.	N/A
Mode-1	0.2-1.2 sec	10.0-40.0 sec	N/A
Mode-2	0.2-1.2 sec	10.0-40.0 sec	10.0-40.0 sec

When the maximum time that the HDD is waiting for commands has been exceeded:

Mode-0: Mode shifts from Active condition to Active Idle in 0.2-1.2, and to Low Power Idle in 15 minutes.

Mode-1: Mode shifts from Active condition to Active Idle in 0.2-1.2 seconds and to Low Power Idle in 10.0-40.0 seconds.

Mode-2: Mode shifts from Active condition to Active Idle in 0.2-1.2 seconds and to Low Power Idle in 10.0-40.0 seconds. After 10.0-40.0 seconds in Low Power Idle, the mode shifts to standby.

* The default values of these settings are reflected in the WORD 91 values of the IDENTIFY DEVICE command. Also, the APM mode is initialized to Mode-1 (default value) by a hardware reset and at power-off.

1.12 Interface Power Management (IPM)

1.12.1 Host-initiated Interface Power Management (HIPM)

When the disk drive is waiting for commands, it can enter one of three IPM modes as requested by the host. The three IPM modes are:

1) Partial mode: PMREQ_P is sent when the host requests the Partial mode.

2) Slumber mode: PMREQ_S is sent when the host requests the Slumber mode.

3) Active mode: When the serial ATA interface is in active state.

There are three interface (I/F) power states: Active, Partial, and Slumber. As requested by the host, the disk drive switches its I/F power state from the Active state to the Partial state, or from the Active state to the Slumber state.

1.12.2 Device-initiated Interface Power Management (DIPM)

If this function is enabled by Set Features command, the disk drive shifts to two kinds of IPM modes automatically under the Idle condition.

1) Partial mode: PMREQ_P is sent when the disk drive requests the Partial mode.

2) Slumber mode: PMREQ_S is sent when the disk drive requests the Slumber mode.

I/F power states

1) Active state

   The SATA interface is active, and data can be sent and received.

2) Partial state

   The SATA interface is in the Power Down state. In this state, the interface is switched to the Partial state when a PMREQ_P signal is received from or sent to host. Because the return time to the Active state from the Partial state is specified as within 10 μs, the degree of the I/F Power Save mode is shallow so that this recovery time is satisfied.

3) Slumber state

   The SATA interface is in the Power Down state. In this state, the interface is switched to the Slumber state when a PMREQ_S signal is received from or sent to host. Because the return time to the Active state from the Slumber state is specified as within 10 ms, the degree of the I/F Power Save mode is deep so that this recovery time is satisfied.

Table 1.8 Interface power management

IPM Mode	I/F power state	Return time to active	I/F condition
Active	Active State	–	Active
Partial	Partial State	5 to 10 μs maximum	Power Down
Slumber	Slumber State	5 to 10 ms maximum	Power Down

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CHAPTER 2 Device Configuration

This chapter describes the internal configurations of the hard disk drives and the configuration of the systems in which they operate.

2.1 Device Configuration

Figure 2.1 shows the disk drive. The disk drive consists of a disk enclosure (DE), read/write preamplifier, and controller PCA. The disk enclosure contains the disk media, heads, spindle motors, actuators, and a circulating air filter.

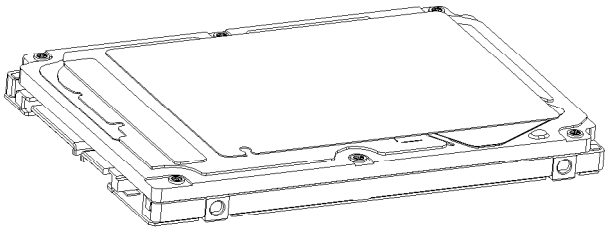

Figure 2.1 Disk drive outerview

(1) Disk

The outer diameter of the disk is 65 mm. The inner diameter is 20 mm.

(2) Head

The heads are of the load/unload (L/UL) type. The head unloads the disk out of while the disk is not rotating and loads on the disk when the disk starts.

(3) Spindle motor

The disks are rotated by a direct drive Sensor-less DC motor.

(4) Actuator

The actuator uses a revolving voice coil motor (VCM) structure which consumes low power and generates very little heat. The head assembly at the edge of the actuator arm is controlled and positioned by feedback of the servo information read by the read/write head. If the power is not on or if the spindle motor is stopped, the head assembly stays on the ramp out of the disk and is fixed by a mechanical lock.

(5) Air circulation system

The disk enclosure (DE) is sealed to prevent dust and dirt from entering. The disk enclosure features a closed loop air circulation system that relies on the blower effect of the rotating disk. This system continuously circulates the air through the circulation filter to maintain the cleanliness of the air within the disk enclosure.

(6) Read/write circuit

The read/write circuit uses a LSI chip for the read/write preamplifier. It improves data reliability by preventing errors caused by external noise.

(7) Controller circuit

The controller circuit consists of an LSI chip which includes Serial-ATA core to achieve a high-performance native Serial-ATA controller.

2.2 System Configuration

2.2.1 SATA interface

Figure 2.2 shows the SATA interface system configuration. The disk drive complies with ATA/ATAPI-7, SATA 1.0a and SATA II 1.0 standards.

2.2.2 Drive connection

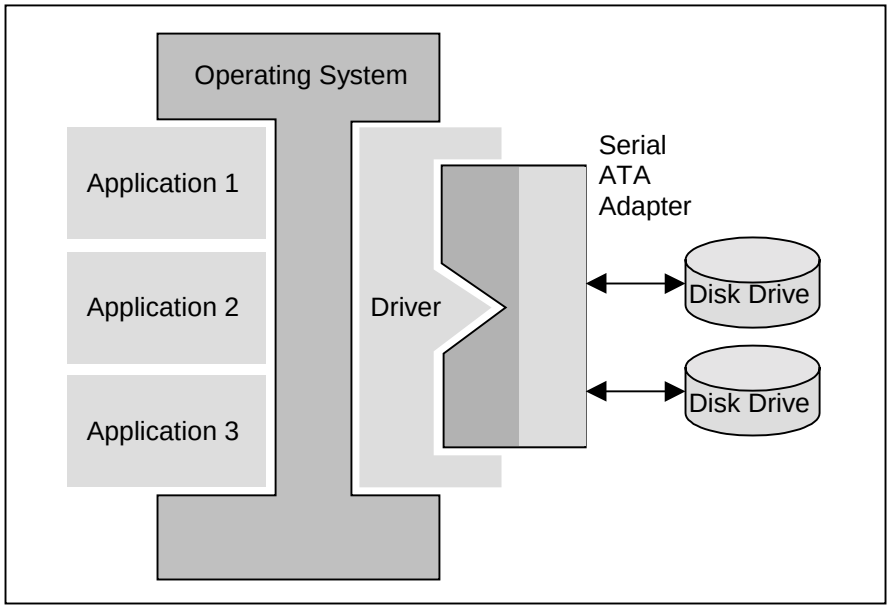

Figure 2.2 Drive system configuration

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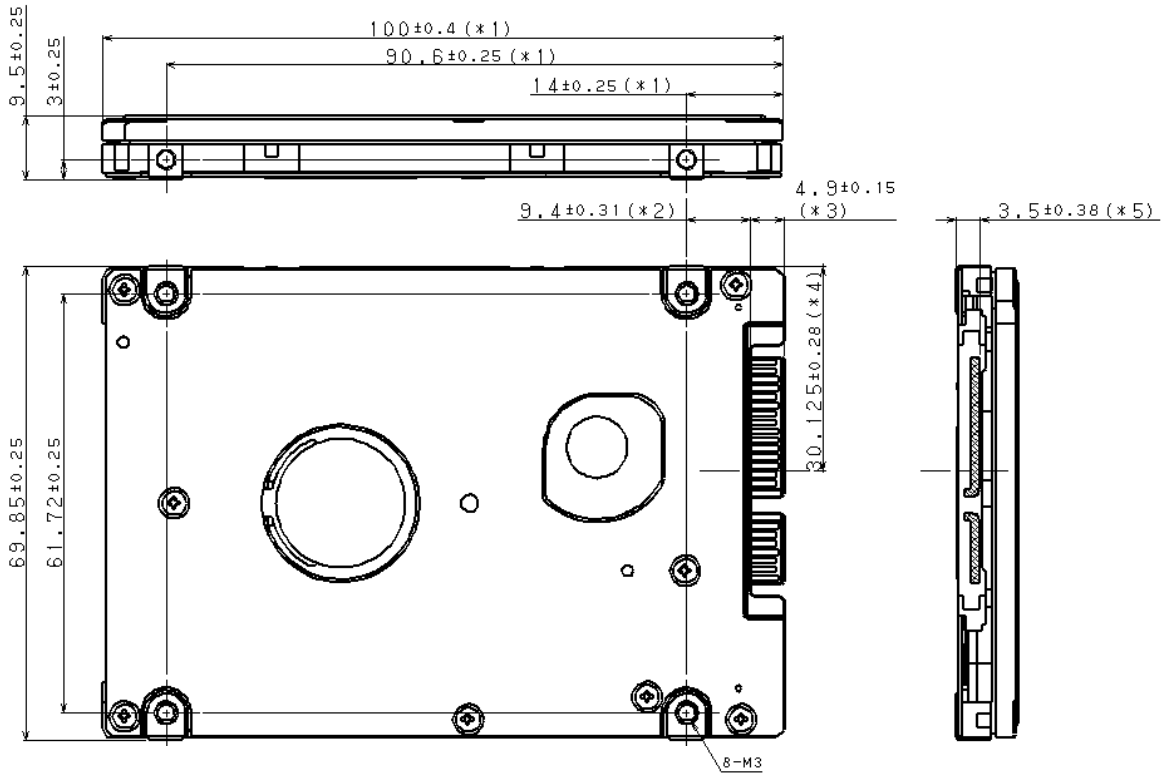
CHAPTER 3 Installation Conditions

This chapter gives the external dimensions, installation conditions, surface temperature conditions, cable connections, and switch settings of the hard disk drives.

3.1 Dimensions

Figure 3.1 illustrates the dimensions of the disk drive. All dimensions are in mm.



*1 The PCA and connectors are not included in these dimensions.

*2 Dimension from the center of the user tap to the base of the connector pins

*3 Length of the connector pins

*4 Dimension from the outer edge of the user tap to the center of the connector pins

*5 Dimension from the outer edge of the user tap to the innermost edge of the connector pins

Figure 3.1 Dimensions

3.2 Mounting

For information on mounting, see the "FUJITSU 2.5-INCH HDD INTEGRATION GUIDANCE (C141-E144)."

(1) Orientation

Figure 3.2 illustrates the allowable orientations for the disk drive.

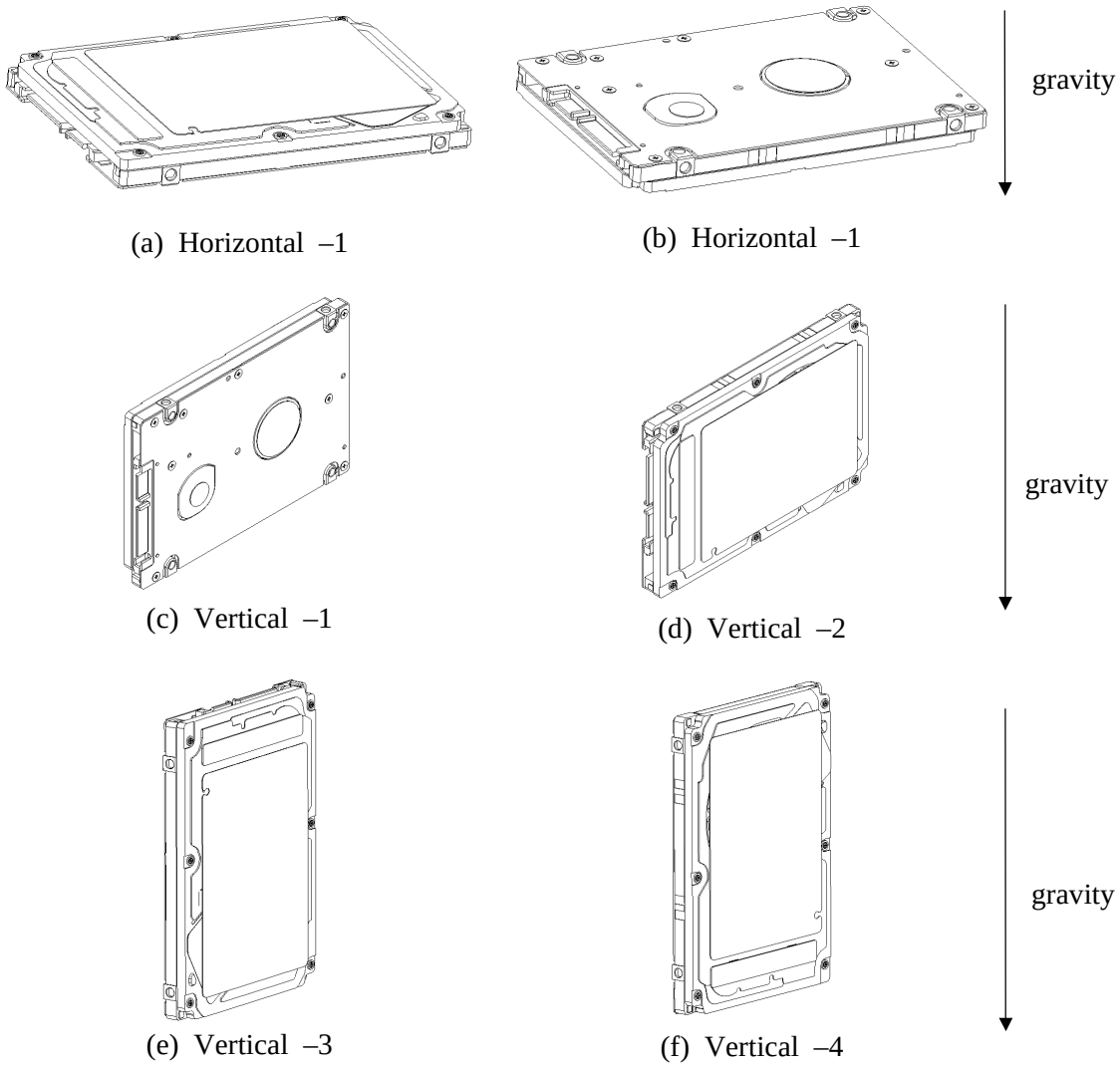


Figure 3.2 Orientation

(2) Frame

The MR head bias of the HDD disk enclosure (DE) is zero. The mounting frame is connected to Signal Ground (SG).

IMPORTANT

Use M3 screw for the mounting screw and the screw length should satisfy the specification in Figure 3.3.

The tightening torque must be 0.49N•m (5kgf•cm).

When attaching the HDD to the system frame, do not allow the system frame to touch parts (cover and base) other than parts to which the HDD is attached.

(3) Limitation of mounting

Note) These dimensions are recommended values; if it is not possible to satisfy them, contact us.

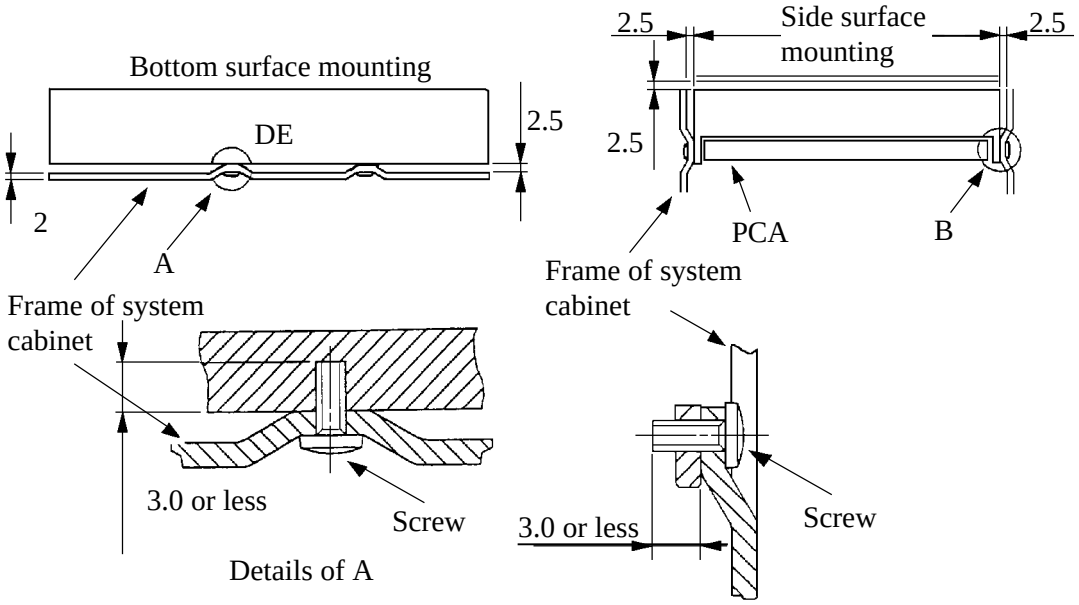


Figure 3.3 Mounting frame structure

IMPORTANT

Because of breather hole mounted to the HDD, do not allow this to close during mounting.

Locating of breather hole is shown as Figure 3.4.

For breather hole of Figure 3.4, at least, do not allow its around ϕ 2.4 to block.

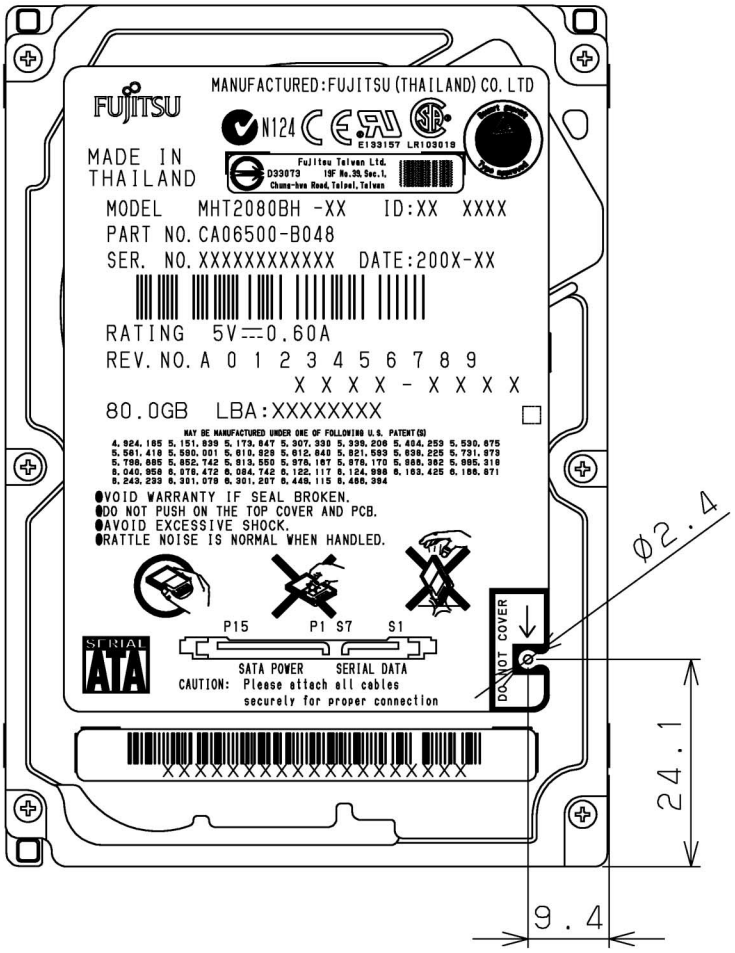


Figure 3.4 Location of breather

(4) Ambient temperature

The temperature conditions for a disk drive mounted in a cabinet refer to the ambient temperature at a point 3 cm from the disk drive. The ambient temperature must satisfy the temperature conditions described in Section 1.4, and the airflow must be considered to prevent the DE surface cover temperature from exceeding 60 °C.

Provide air circulation in the cabinet such that the PCA side, in particular, receives sufficient cooling. To check the cooling efficiency, measure the surface cover temperatures of the DE. Regardless of the ambient temperature, this surface cover temperature must meet the standards listed in Table 3.1. Figure 3.5 shows the temperature measurement point.

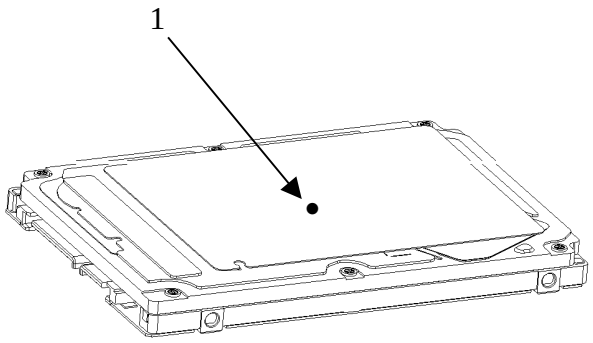


Figure 3.5 Surface cover temperature measurement points

Table 3.1 Surface temperature measurement points and standard values

No.	Measurement point	Temperature
1	DE cover	60 °C max

(5) Service area

Figure 3.6 shows how the drive must be accessed (service areas) during and after installation.

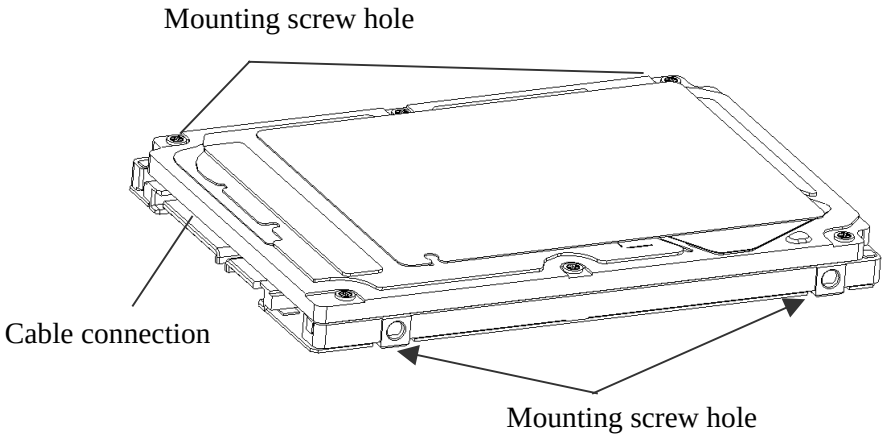


Figure 3.6 Service area

⚠CAUTION

Data corruption: Avoid mounting the disk drive near strong magnetic sources such as loud speakers. Ensure that the disk drive is not affected by external magnetic fields.

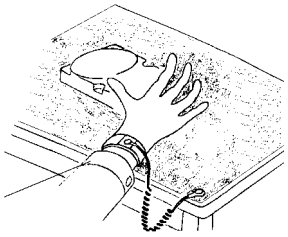
Damage: Do not press the cover of the disk drive. Pressing it too hard, the cover and the spindle motor contact, which may cause damage to the disk drive.

Static: When handling the device, disconnect the body ground (500 kΩ or greater). Do not touch the printed circuit board, but hold it by the edges.

(6) Handling cautions

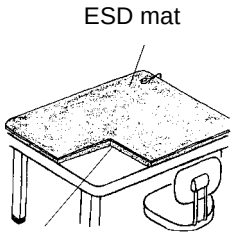
Please keep the following cautions, and handle the HDD under the safety environment.

- **General notes**



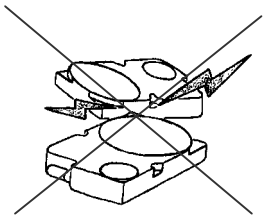
Wrist strap

Use the Wrist strap.

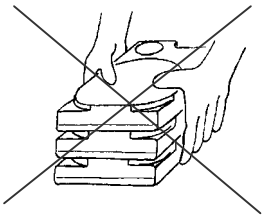


Shock absorbing mat

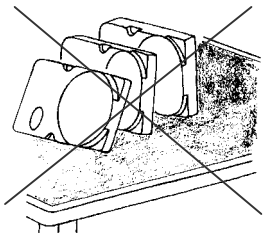
Place the shock absorbing mat on the operation table, and place ESD mat on it.



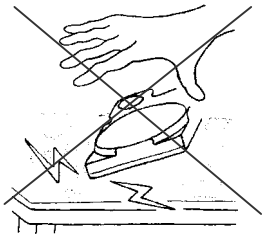
Do not hit HDD each other.



Do not stack when carrying.



Do not place HDD vertically to avoid falling down.



Do not drop.

Figure 3.7 Handling cautions

- **Installation**

(1) Please use the driver of a low impact when you use an electric driver.
HDD is occasionally damaged by the impact of the driver.

(2) Please observe the tightening torque of the screw strictly.
M3 ……0.49N•m (5 kgf•cm).

- **Recommended equipments**

Contents		Model	Maker
ESD	Wrist strap	JX-1200-3056-8	SUMITOMO 3M
	ESD mat	SKY-8A (Color Seiden Mat)	Achilles
Shock	Low shock driver	SS-6500	HIOS

3.3 Connections with Host System

3.3.1 Device connector

The disk drive has the SATA interface connectors listed below for connecting external devices. Figure 3.8 shows the locations of these connectors and terminals.

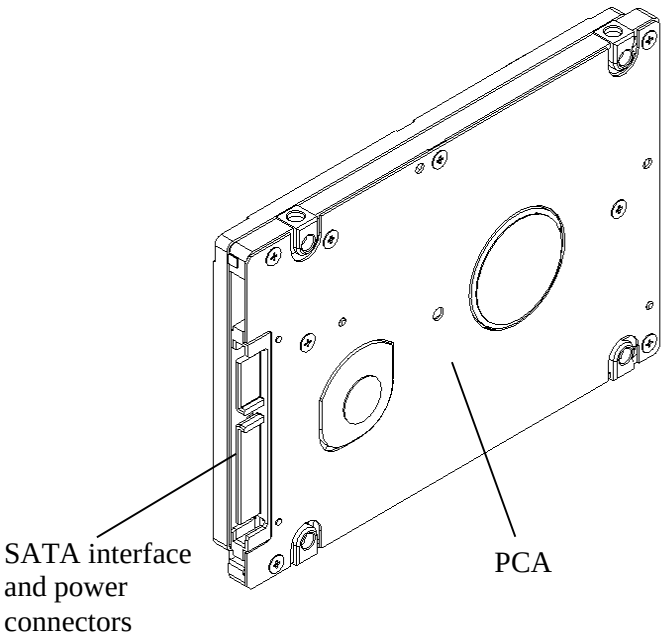


Figure 3.8 Connector locations

3.3.2 Signal segment and power supply segment

Figure 3.9 shows each segment of the SATA interface connector and pin numbers.

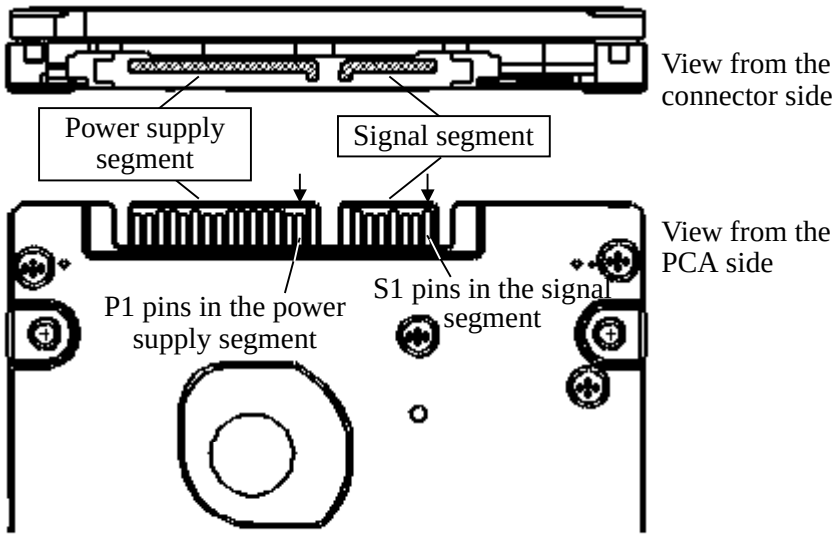


Figure 3.9 Power supply pins (CN1)

3.3.3 Connector specifications for host system

Table 3.2 lists the recommended specifications for the host interface connectors.

Table 3.2 The recommended connector specifications for the host system

Segment	Name	Model (Manufacturer)
SATA interface and power supply	Host receptacle	67492-0220 (Molex) or compatibles

3.3.4 SATA interface cable connection

The cable that connects the disk drive to the host system must be compliant with the Serial ATA 1.0a specification.

3.3.5 Note about SATA interface cable connection

Take note of the following precaution about plugging a SATA interface cable into the SATA interface connector of the disk drive and plugging the connector into a host receptacle:

- When plugging together the disk drive SATA interface connector and the host receptacle or SATA interface cable connector, do not apply more than 10 kgf of force in the connection direction once they are snugly and securely in position.

Note: Hot Plug

These drives support the serial ATA interface and Hot Plug (hot-pluggable). However, the disk drive installation and removal procedures and notes on safety precautions with regard to hot-plugging vary depending on the specific requirements and environment-related conditions of the system to which the drive is connected by hot-plugging.

When using the drive under general conditions of use (i.e., without hot-plugging), observe the important alert messages and notes on safety precautions given in this manual.

For the conditions of use and notes on using the drive with a system that supports hot-plugging, contact our sales representative at one of our offices.

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CHAPTER 4 Theory of Device Operation

This chapter explains basic design concepts of the disk drive. Also, this chapter explains subassemblies of the disk drive, each sequence, servo control, and electrical circuit blocks.

4.1 Outline

This chapter consists of two parts. First part (Section 4.2) explains mechanical assemblies of the disk drive. Second part (Sections 4.3 through 4.7) explains a servo information recorded in the disk drive and drive control method.

4.2 Subassemblies

The disk drive consists of a disk enclosure (DE) and printed circuit assembly (PCA).

The DE contains all movable parts in the disk drive, including the disk, spindle, actuator, read/write head, and air filter. For details, see Subsections 4.2.1 to 4.2.4.

The PCA contains the control circuits for the disk drive. The disk drive has one PCA. For details, see Sections 4.3.

4.2.1 Disk

The DE contains disks with an outer diameter of 65 mm and an inner diameter of 20 mm.

Servo data is recorded on each cylinder (total 124). Servo data written at factory is read out by the read head. For servo data, see Section 4.7.

4.2.2 Spindle

The spindle consists of a disk stack assembly and spindle motor. The disk stack assembly is activated by the direct drive sensor-less DC spindle motor, which has a speed of 5,400 rpm ±1%. The spindle is controlled with detecting a PHASE signal generated by counter electromotive voltage of the spindle motor at starting.

4.2.3 Actuator

The actuator consists of a voice coil motor (VCM) and a head carriage. The VCM moves the head carriage along the inner or outer edge of the disk. The head carriage position is controlled by feeding back the difference of the target position that is detected and reproduced from the servo information read by the read/write head.

4.2.4 Air filter

There are two types of air filters: a breather filter and a circulation filter.

The breather filter makes an air in and out of the DE to prevent unnecessary pressure around the spindle when the disk starts or stops rotating. When disk drives are transported under conditions where the air pressure changes a lot, filtered air is circulated in the DE.

The circulation filter cleans out dust and dirt from inside the DE. The disk drive cycles air continuously through the circulation filter through an enclosed loop air cycle system operated by a blower on the rotating disk.

4.3 Circuit Configuration

Figure 4.1 shows the power supply configuration of the disk drive, and Figure 4.2 shows the disk drive circuit configuration.

(1) Read/write circuit

The read/write circuit consists of two circuits; read/write preamplifier (PreAMP) and read channel (RDC).

The PreAMP consists of the write current switch circuit, that flows the write current to the head coil, and the voltage amplifier circuit, that amplitudes the read output from the head.

The RDC is the read demodulation circuit using the Modified Extended Partial Response (MEEPR), and contains the Viterbi detector, programmable filter, adaptable transversal filter, times base generator, data separator circuits, RLL (Run Length Limited) encoder and servo demodulation circuit.

(2) Servo circuit

The position and speed of the voice coil motor are controlled by 2 closed-loop servo using the servo information recorded on the data surface. The servo information is an analog signal converted to digital for processing by a MPU and then reconverted to an analog signal for control of the voice coil motor.

The MPU precisely sets each head on the track according on the servo information on the media surface.

(3) Spindle motor driver circuit

The circuit measures the interval of a PHASE signal generated by counter-electromotive voltage of a motor and controls the motor speed comparing target speed.

(4) Controller circuit

Major functions are listed below.

- Serial-ATA interface control and data transfer control
- Data buffer management
- Sector format control
- Defect management
- ECC control
- Error recovery and self-diagnosis

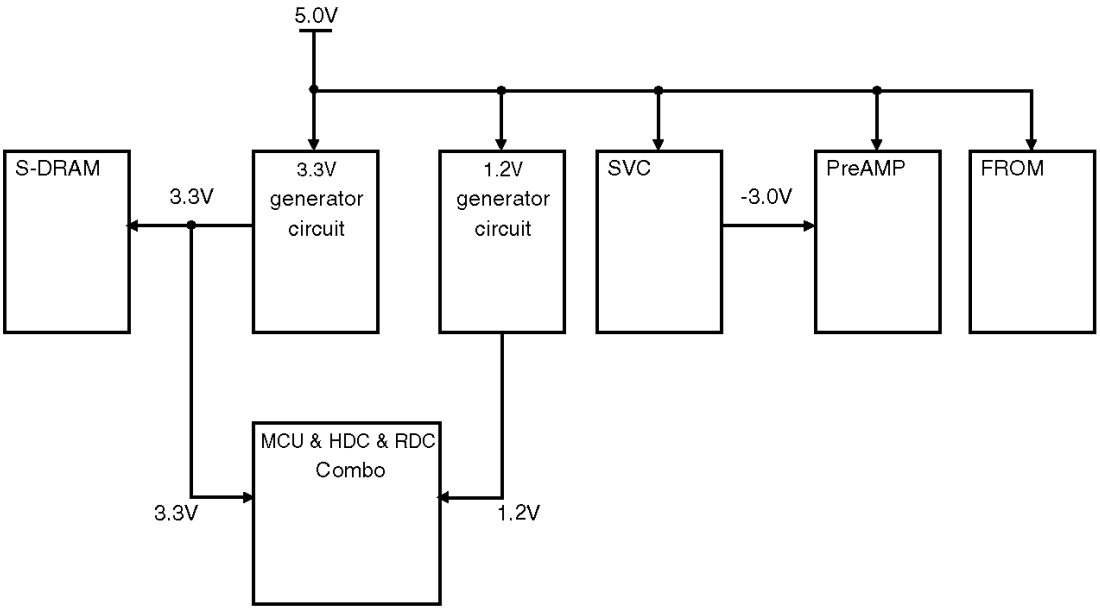

Figure 4.1 Power Supply Configuration

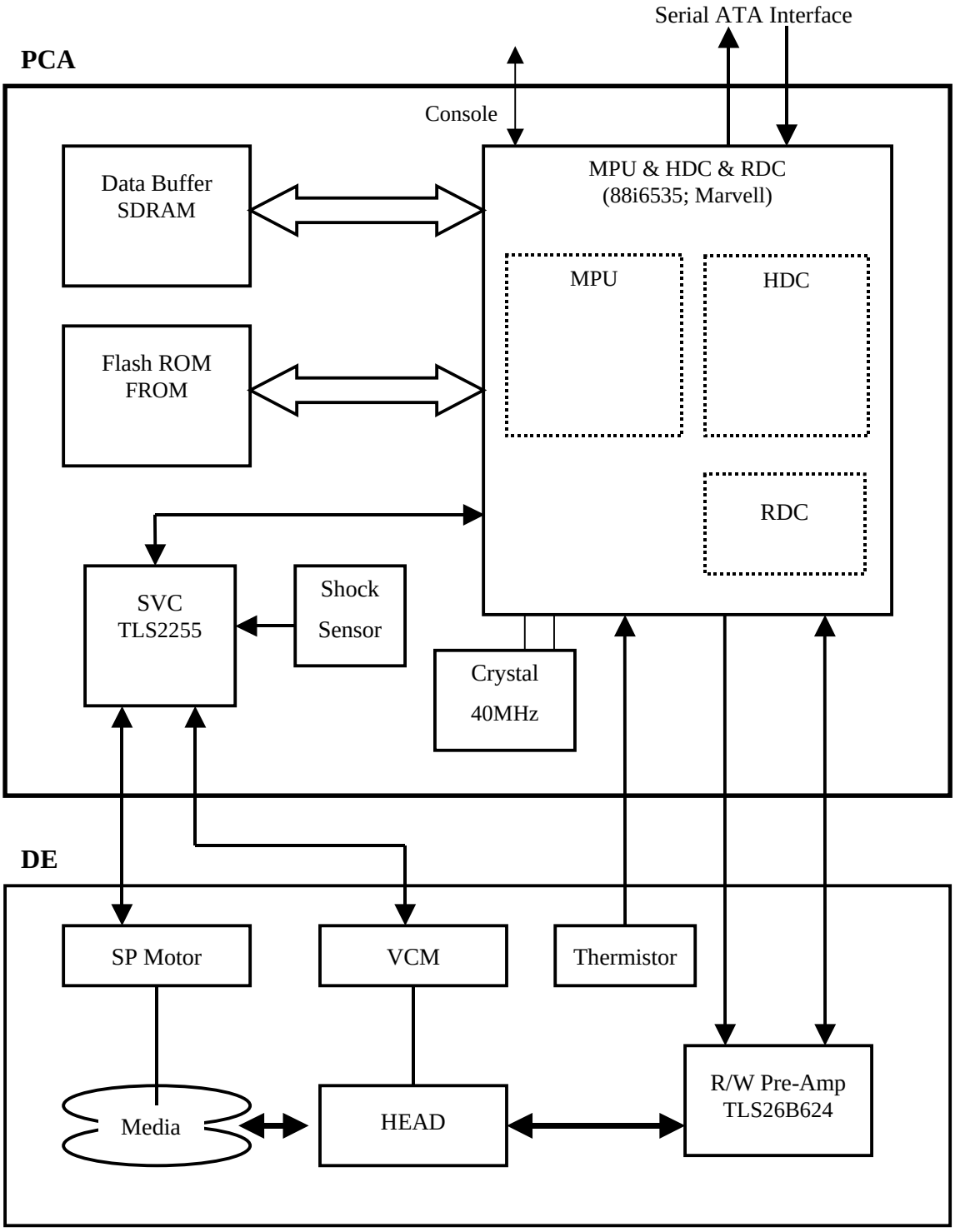

Figure 4.2 Circuit Configuration

4.4 Power-on Sequence

Figure 4.3 describes the operation sequence of the disk drive at power-on. The outline is described below.

a) After the power is turned on, the disk drive executes the MPU bus test, internal register read/write test, and work RAM read/write test. When the self-diagnosis terminates successfully, the disk drive starts the spindle motor.

b) The disk drive executes self-diagnosis (data buffer read/write test) after enabling response to the SATA interface.

c) After confirming that the spindle motor has reached rated speed, the head assembly is loaded on the disk.

d) The disk drive positions the heads onto the SA area and reads out the system information.

e) The disk drive sets up a requirement for execution of self -calibration. This collects data for VCM torque and mechanical external forces applied to the actuator, and updates the calibrating value.

f) The drive becomes ready. The host can issue commands.

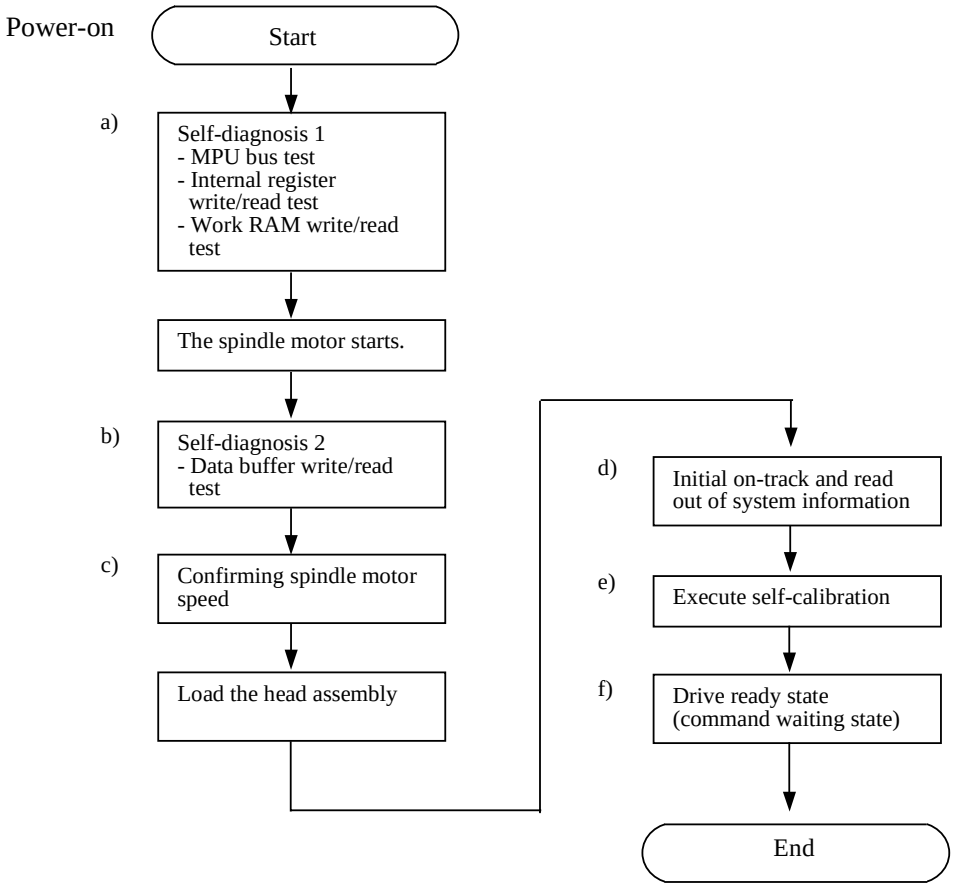

Figure 4.3 Power-on operation sequence

4.5 Self-calibration

The disk drive occasionally performs self-calibration in order to sense and calibrate mechanical external forces on the actuator, and VCM torque. This enables precise seek and read/write operations.

4.5.1 Self-calibration contents

(1) Sensing and compensating for external forces

The actuator suffers from torque due to the FPC forces and winds accompanying disk revolution. The torque vary with the disk drive and the cylinder where the head is positioned. To execute stable fast seek operations, external forces are occasionally sensed.

The firmware of the drive measures and stores the force (value of the actuator motor drive current) that balances the torque for stopping head stably. This includes the current offset in the power amplifier circuit and DAC system.

The forces are compensated by adding the measured value to the specified current value to the power amplifier. This makes the stable servo control.

To compensate torque varying by the cylinder, the disk is divided into 13 areas from the innermost to the outermost circumference and the compensating value is measured at the measuring cylinder on each area at factory calibration. The measured values are stored in the SA cylinder. In the self-calibration, the compensating value is updated using the value in the SA cylinder.

(2) Compensating open loop gain

Torque constant value of the VCM has a dispersion for each drive, and varies depending on the cylinder that the head is positioned. To realize the high speed seek operation, the value that compensates torque constant value change and loop gain change of the whole servo system due to temperature change is measured and stored.

For sensing, the firmware mixes the disturbance signal to the position signal at the state that the head is positioned to any cylinder. The firmware calculates the loop gain from the position signal and stores the compensation value against to the target gain as ratio.

For compensating, the direction current value to the power amplifier is multiplied by the compensation value. By this compensation, loop gain becomes constant value and the stable servo control is realized.

To compensate torque constant value change depending on cylinder, whole cylinders from most inner to most outer cylinder are divided into 13 partitions at calibration in the factory, and the compensation data is measured for representative cylinder of each partition. This measured value is stored in the SA area. The compensation value at self-calibration is calculated using the value in the SA area.

4.5.2 Execution timing of self-calibration

Self-calibration is performed once when power is turned on. After that, the disk drive does not perform self-calibration until it detects an error.

That is, self-calibration is performed each time one of the following events occur:

- When it passes from the power on for about 7 or 8 seconds except that the disk drive shifts to Low Power Idle mode, Standby mode and Sleep mode by execution of any commands.
- The number of retries to write or seek data reaches the specified value.
- The error rate of data reading, writing, or seeking becomes lower than the specified value.

4.5.3 Command processing during self-calibration

This enables the host to execute the command without waiting for a long time, even when the disk drive is performing self-calibration. The command execution wait time is about maximum 72 ms.

When the error rate of data reading, writing, or seeking becomes lower than the specified value, self-calibration is performed to maintain disk drive stability.

If the disk drive receives a command execution request from the host while performing self-calibration, it stops the self-calibration and starts to execute the command. In other words, if a disk read or write service is necessary, the disk drive positions the head to the track requested by the host, reads or writes data, and then restarts calibration after about 3 seconds.

If the error rate recovers to a value exceeding the specified value, self-calibration is not performed.

4.6 Read/write Circuit

The read/write circuit consists of the read/write preamplifier (PreAMP), the write circuit, the read circuit, and the time base generator in the read channel (RDC). Figure 4.4 is a block diagram of the read/write circuit.

4.6.1 Read/write preamplifier (PreAMP)

PreAMP equips a read preamplifier and a write current switch, that sets the bias current to the MR device and the current in writing. Each channel is connected to each data head, and PreAMP switches channel by serial I/O. In the event of any abnormalities, including a head short-circuit or head open circuit, the write unsafe signal is generated so that abnormal write does not occur.

4.6.2 Write circuit

The write data is output from the hard disk controller (HDC) with the NRZ data format, and sent to the encoder circuit in the RDC. The NRZ write data is converted to RLL (Run Length Limited) code data by the encoder circuit then sent to the PreAMP, and the data is written onto the media.

(1) RLL code MEEPRML

This device converts data using the RLL (Run Length Limited) algorithm.

(2) Write precompensation

Write precompensation compensates, during a write process, for write non-linearity generated at reading.

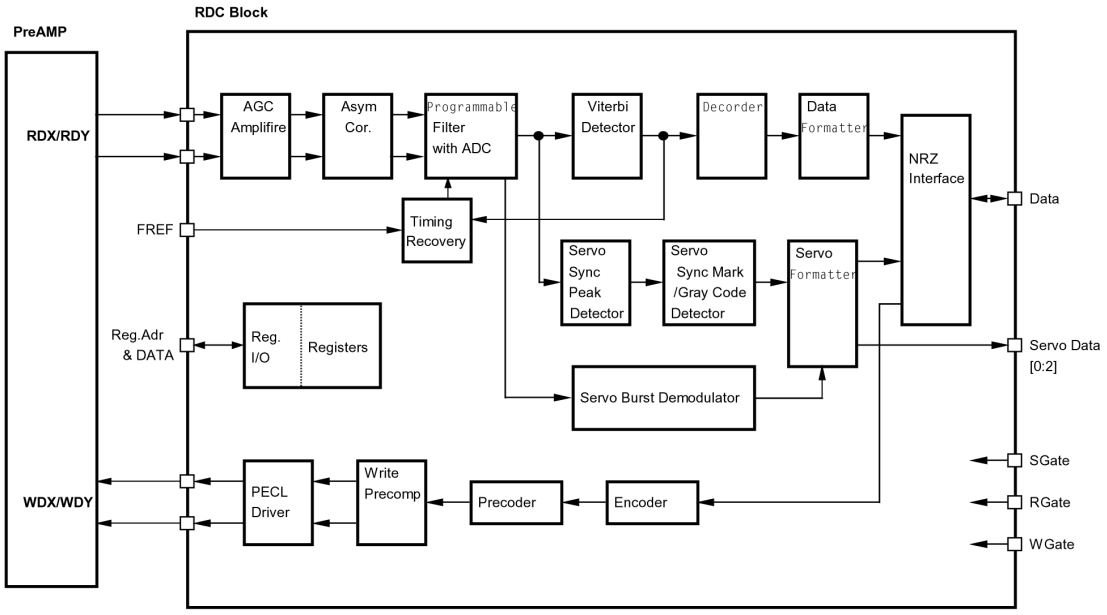

Figure 4.4 Read/write circuit block diagram

4.6.3 Read circuit

The head read signal from the PreAMP is regulated by the automatic gain control (AGC) circuit. Then the output is converted into the sampled read data pulse by the programmable filter circuit and the flash digitizer circuit. This clock signal is converted into the NRZ data by the ENDEC circuit based on the read data maximum-likelihood-detected by the Viterbi detection circuit, then is sent to the HDC.

(1) AGC circuit

The AGC circuit automatically regulates the output amplitude to a constant value even when the input amplitude level fluctuates. The AGC amplifier output is maintained at a constant level even when the head output fluctuates due to the head characteristics or outer/inner head positions.

(2) Programmable filter circuit

The programmable filter circuit has a low-pass filter function that eliminates unnecessary high frequency noise component and a high frequency boost-up function that equalizes the waveform of the read signal.

Cut-off frequency of the low-pass filter and boost-up gain are controlled from the register in read channel by an instruction of the serial data signal from MPU (M5). The MPU optimizes the cut-off frequency and boost-up gain according to the transfer frequency of each zone.

Figure 4.5 shows the frequency characteristic sample of the programmable filter.

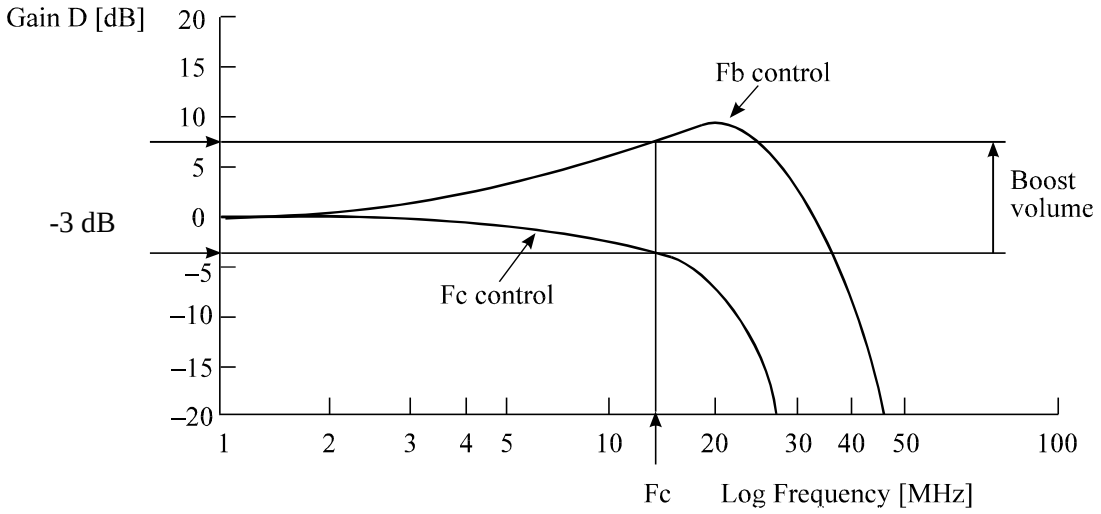

Figure 4.5 Frequency characteristic of programmable filter

(3) FIR circuit

This circuit is 10-tap sampled analog transversal filter circuit that equalizes the head read signal to the Modified Extended Partial Response (MEEPR) waveform.

(4) A/D converter circuit

This circuit changes Sampled Read Data Pulse from the FIR circuit into Digital Read Data.

(5) Viterbi detection circuit

The sample hold waveform output from the flash digitizer circuit is sent to the Viterbi detection circuit. The Viterbi detection circuit demodulates data according to the survivor path sequence.

(6) ENDEC

This circuit converts the read data into the NRZ data.

4.6.4 Digital PLL circuit

The drive uses constant density recording to increase total capacity. This is different from the conventional method of recording data with a fixed data transfer rate at all data area. In the constant density recording method, data area is divided into zones by radius and the data transfer rate is set so that the recording density of the inner cylinder of each zone is nearly constant. The drive divides data area into 30 zones to set the data transfer rate.

The MPU transfers the data transfer rate setup data (SD/SC) to the RDC that includes the Digital PLL circuit to change the data transfer rate.

4.7 Servo Control

The actuator motor and the spindle motor are submitted to servo control. The actuator motor is controlled for moving and positioning the head to the track containing the desired data. To turn the disk at a constant velocity, the actuator motor is controlled according to the servo data that is written on the data side beforehand.

4.7.1 Servo control circuit

Figure 4.6 is the block diagram of the servo control circuit. The following describes the functions of the blocks:

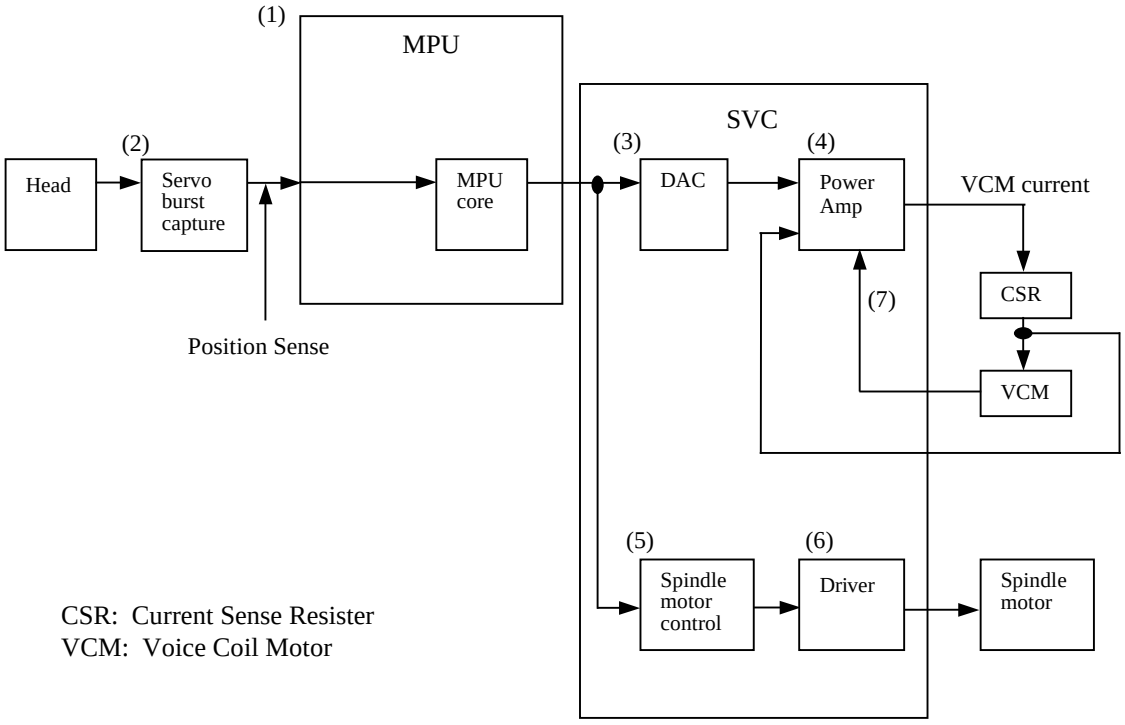

Figure 4.6 Block diagram of servo control circuit

(1) Microprocessor unit (MPU)

The MPU executes startup of the spindle motor, movement to the reference cylinder, seek to the specified cylinder, and calibration operations. Main internal operation of the MPU are shown below.

The major internal operations are listed below.

a. Spindle motor start

Starts the spindle motor and accelerates it to normal speed when power is applied.

b. Move head to reference cylinder

Drives the VCM to position the head at the any cylinder in the data area. The logical initial cylinder is at the outermost circumference (cylinder 0).

c. Seek to specified cylinder

Drives the VCM to position the head to the specified cylinder.

d. Calibration

Senses and stores the thermal offset between heads and the mechanical forces on the actuator, and stores the calibration value.

(2) Servo burst capture circuit

The servo burst capture circuit reproduces signals (position signals) that indicate the head position from the servo data on the data surface. From the servo area on the data area surface, via the data head, the burst signal of SERVO A, SERVO B, SERVO C, and SERVO D is output as shown in Figure 4.9 in subsequent to the servo mark, gray code that indicates the cylinder position, and index information. The servo signals do A/D-convert by Fourier-demodulator in the servo burst capture circuit. At that time the AGC circuit is in hold mode. The A/D converted data is recognized by the MPU as position information with A-B and C-D processed.

(3) D/A converter (DAC)

The control program calculates the specified data value (digital value) of the VCM drive current, and the value is converted from digital-to-analog so that an analog output voltage is sent to the power amplifier.

(4) Power amplifier

The power amplifier feeds currents, corresponding to the DAC output signal voltage to the VCM.

(5) Spindle motor control circuit

The spindle motor control circuit controls the sensor-less spindle motor. A spindle driver IC with a built-in PLL(FLL) circuit that is on a hardware unit controls the sensor-less spindle motor.

(6) Driver circuit

The driver circuit is a power amplitude circuit that receives signals from the spindle motor control circuit and feeds currents to the spindle motor.

(7) VCM current sense resistor (CSR)

This resistor controls current at the power amplifier by converting the VCM current into voltage and feeding back.

4.7.2 Data-surface servo format

Figure 4.7 describes the physical layout of the servo frame. The three areas indicated by (1) to (3) in Figure 4.7 are described below.

(1) Inner guard band (IGB)

This area is located inside the user area, and the rotational speed of the VCM can be controlled on this cylinder area for head moving.

(2) Data area

This area is used as the user data area and the SA cylinder.

(3) Outer guard band (OGB)

This area is located at outer position of the user data area, and the rotational speed of the spindle can be controlled on this cylinder area for head moving.

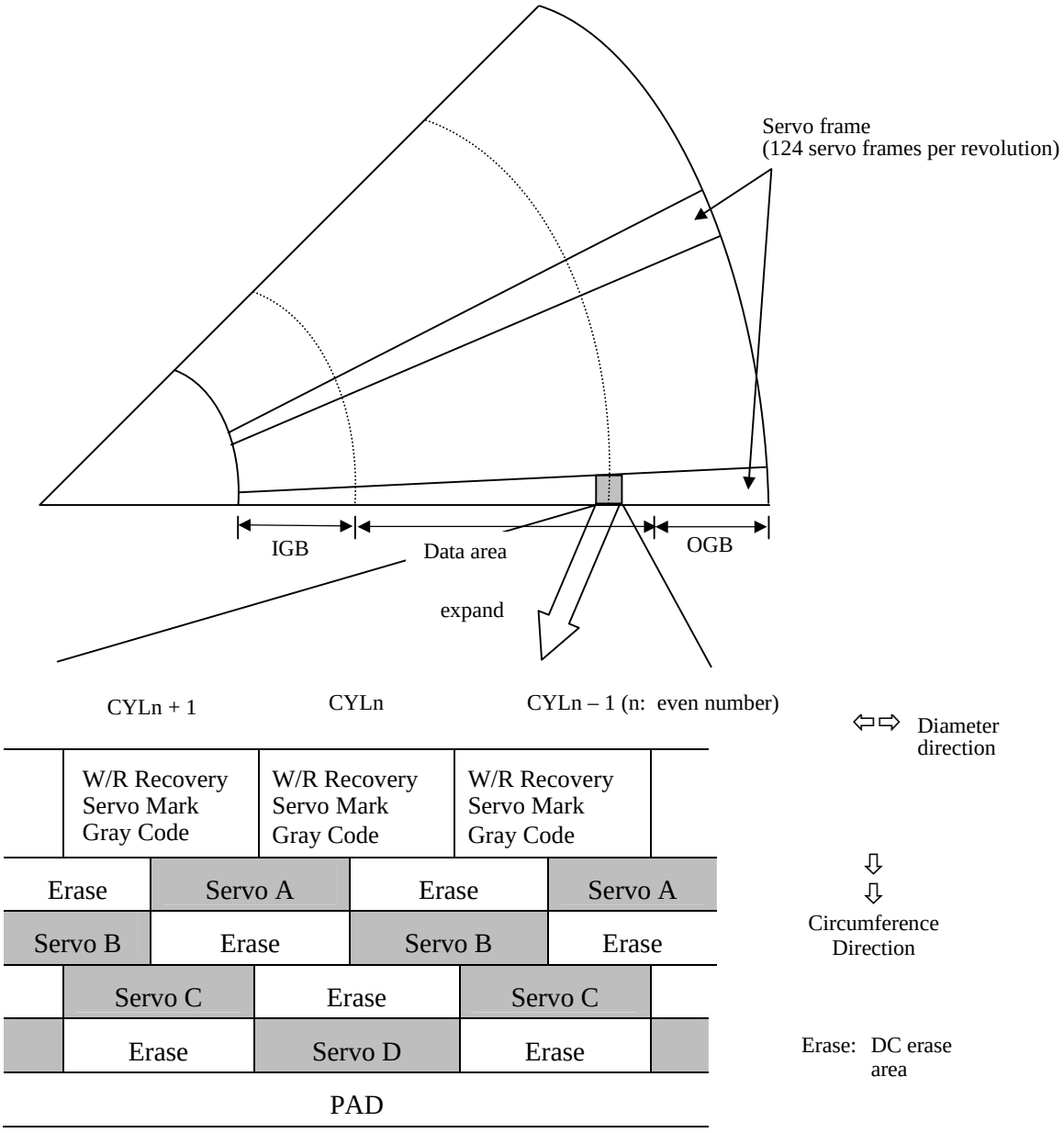

Figure 4.7 Physical sector servo configuration on disk surface

4.7.3 Servo frame format

As the servo information, the IDD uses the two-phase servo generated from the gray code and servo A to D. This servo information is used for positioning operation of radius direction and position detection of circumstance direction.

The servo frame consists of 6 blocks; write/read recovery, servo mark, gray code, servo A to D, and PAD. Figure 4.8 shows the servo frame format.

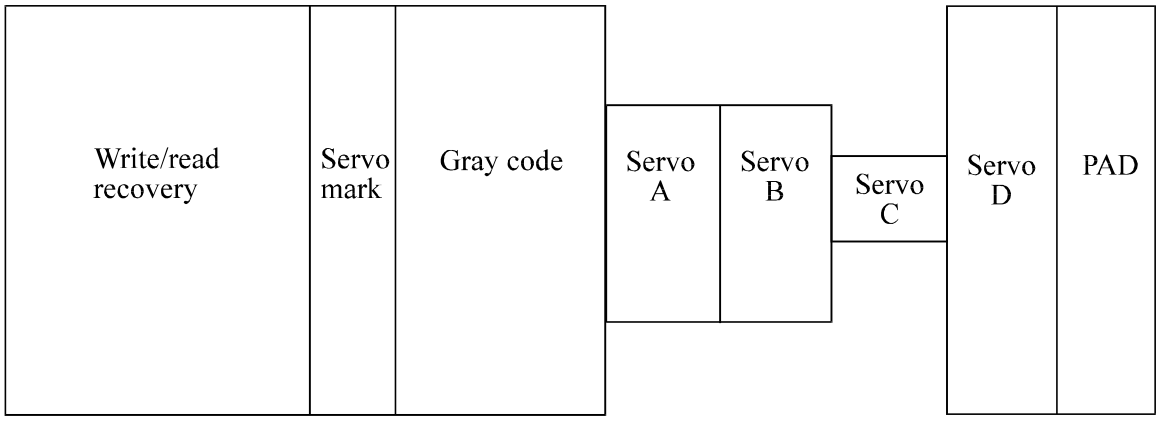

Figure 4.8 Servo frame format

(1) Write/read recovery

This area is used to absorb the write/read transient and to stabilize the AGC.

(2) Servo mark

This area generates a timing for demodulating the gray code and position-demodulating the servo A to D by detecting the servo mark.

(3) Gray code (including sector address bits)

This area is used as cylinder address. The data in this area is converted into the binary data by the gray code demodulation circuit

(4) Servo A, servo B, servo C, servo D,

This area is used as position signals between tracks and the IDD control at on-track so that servo A level equals to servo B level.

(5) PAD

This area is used as a gap between servo and data.

4.7.4 Actuator motor control

The voice coil motor (VCM) is controlled by feeding back the servo data recorded on the data surface. The MPU fetches the position sense data on the servo frame at a constant interval of sampling time, executes calculation, and updates the VCM drive current.

The servo control of the actuator includes the operation to move the head to the reference cylinder, the seek operation to move the head to the target cylinder to read or write data, and the track-following operation to position the head onto the target track.

(1) Operation to move the head to the reference cylinder

The MPU moves the head to the reference cylinder when the power is turned. The reference cylinder is in the data area.

When power is applied the heads are moved from the outside of media to the normal servo data zone in the following sequence:

a) Micro current is fed to the VCM to press the head against the outer direction.

b) The head is loaded on the disk.

c) When the servo mark is detected the head is moved slowly toward the inner circumference at a constant speed.

d) If the head is stopped at the reference cylinder from there. Track following control starts.

(2) Seek operation

Upon a data read/write request from the host, the MPU confirms the necessity of access to the disk. If a read/write instruction is issued, the MPU seeks the desired track.

The MPU feeds the VCM current via the D/A converter and power amplifier to move the head. The MPU calculates the difference (speed error) between the specified target position and the current position for each sampling timing during head moving. The MPU then feeds the VCM drive current by setting the calculated result into the D/A converter. The calculation is digitally executed by the firmware. When the head arrives at the target cylinder, the track is followed.

(3) Track-following operation

Except during head movement to the reference cylinder and seek operation under the spindle rotates in steady speed, the MPU does track following control. To position the head at the center of a track, the DSP drives the VCM by feeding micro current. For each sampling time, the VCM drive current is determined by filtering the position difference between the target position and the position clarified by the detected position sense data. The filtering includes servo compensation. These are digitally controlled by the firmware.

4.7.5 Spindle motor control

Hall-less three-phase twelve-pole motor is used for the spindle motor, and the 3-phase full/half-wave analog current control circuit is used as the spindle motor driver (called SVC hereafter). The firmware operates on the MPU manufactured by Fujitsu. The spindle motor is controlled by sending several signals from the MPU to the SVC. There are three modes for the spindle control; start mode, acceleration mode, and stable rotation mode.

(1) Start mode

When power is supplied, the spindle motor is started in the following sequence:

a) After the power is turned on, the MPU sends a signal to the SVC to charge the charge pump capacitor of the SVC. The charged amount defines the current that flows in the spindle motor.

b) When the charge pump capacitor is charged enough, the MPU sets the SVC to the motor start mode. Then, a current (approx. 0.3 A) flows into the spindle motor.

c) A phase switching signal is generated and the phase of the current flowed in the motor is changed in the order of (V-phase to U-phase), (W-phase to U-phase), (W-phase to V-phase), (U-phase to V-phase), (U-phase to W-phase), and (V-phase to W-phase) (after that, repeating this order).

d) During phase switching, the spindle motor starts rotating in low speed, and generates a counter electromotive force. The SVC detects this counter electromotive force and reports to the MPU using a PHASE signal for speed detection.

e) The MPU is waiting for a PHASE signal. When no phase signal is sent for a specific period, the MPU resets the SVC and starts from the beginning. When a PHASE signal is sent, the SVC enters the acceleration mode.

(2) Acceleration mode

In this mode, the MPU stops to send the phase switching signal to the SVC. The SVC starts a phase switching by itself based on the counter electromotive force. Then, rotation of the spindle motor accelerates. The MPU calculates a rotational speed of the spindle motor based on the PHASE signal from the SVC, and waits till the rotational speed reaches 5,400 rpm. When the rotational speed reaches 5,400 rpm, the SVC enters the stable rotation mode.

(3) Stable rotation mode

The SVC calculates a time for one revolution of the spindle motor based on the PHASE signal. The MPU takes a difference between the current time and a time for one revolution at 4,200 rpm that the MPU already recognized. Then, the MPU keeps the rotational speed to 4,200 rpm by charging or discharging the charge pump for the different time. For example, when the actual rotational speed is 4,000 rpm, the time for one revolution is 15.000 ms. And the time for one revolution at 4,200 rpm is 14.286 ms. Therefore, the MPU charges the charge pump for 0.714 ms $\times$ k (k: constant value). This makes the flowed current into the motor higher and the rotational speed up. When the actual rotational speed is faster than 4,200 rpm, the MPU discharges the pump the other way. This control (charging/discharging) is performed every 1 revolution.

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CHAPTER 5 Interface

This chapter gives details about the interface, and the interface commands and timings.

5.1 Physical Interface

5.1.1 Interface signals

Figure 5.1 shows the interface signals.

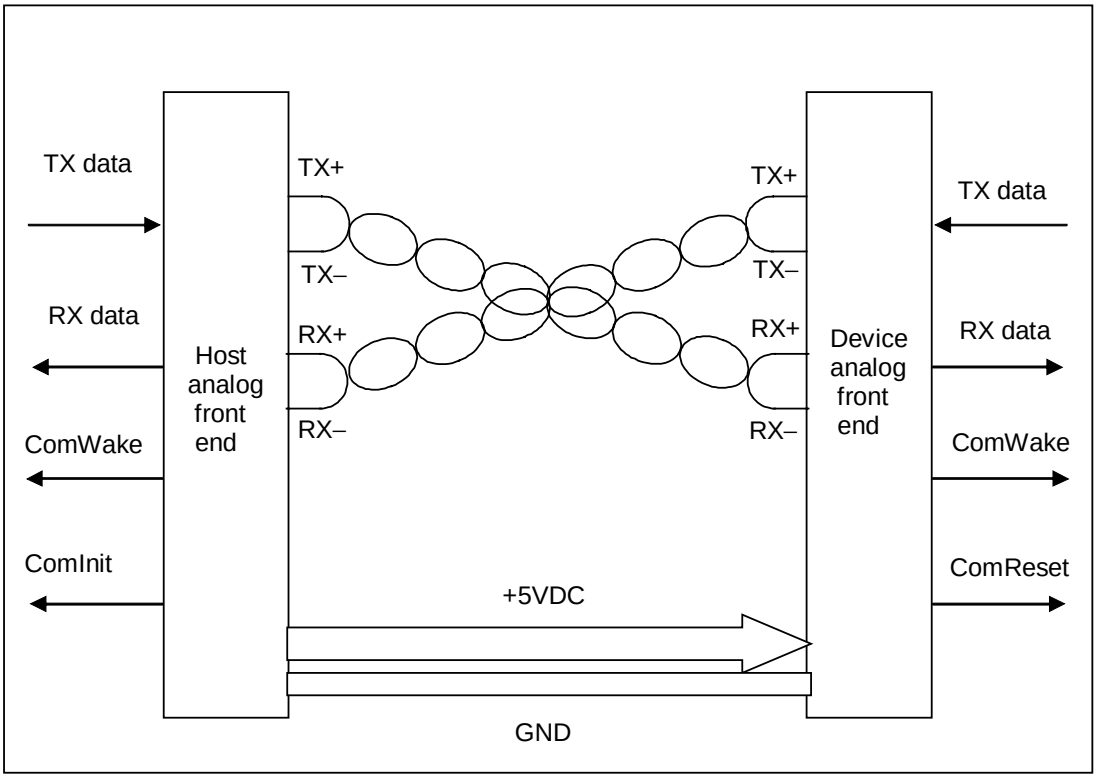


Figure 5.1 Interface signals

An explanation of each signal is provided below.

TX + / TX -

These signals are the outbound high speed differential signals that are connected to the serial ATA cable.

RX + / RX -

These signals are the inbound high speed differential signals that are connected to the serial ATA cable.

TxData

Serially encoded 10b data attached to the high speed serial differential line driver

RxData

Serially encoded 10b data attached to the high speed serial differential line receiver

COMWAKE

Signal from the out of band detector that indicates the COMWAKE out of band signal is being detected.

COMRESET / COMINIT

Host: Signal from the out of band detector that indicates the COMINIT out of band signal is being detected.

Device: Signal from the out of band detector that indicates the COMRESET out of band signal is being detected.

5VDC/GND

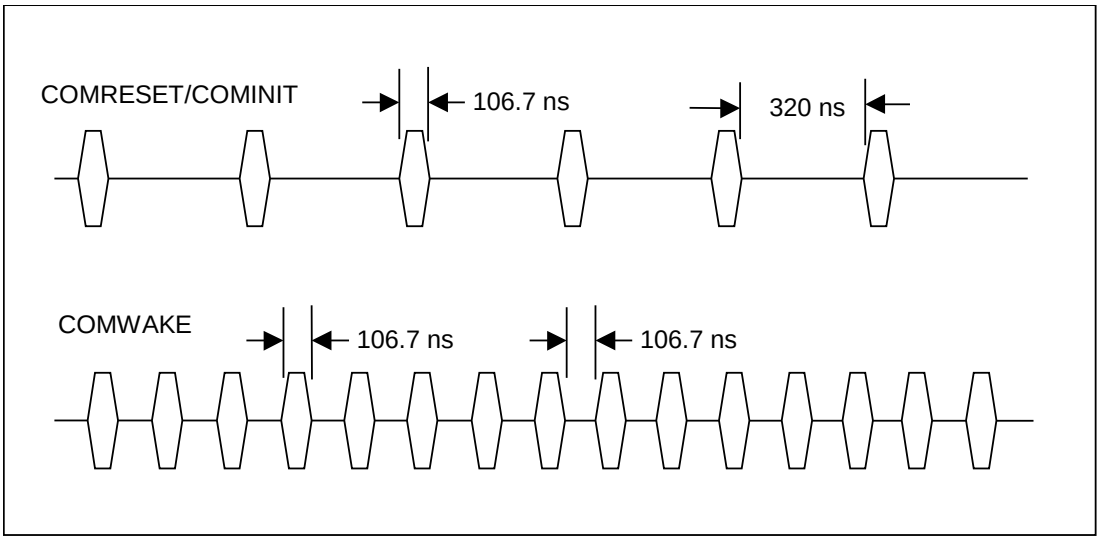
5VDC: +5 V power supply to the disk drive

GND: Ground signal for each signal

5.1.2 Signal interface regulation

5.1.2.1 Out of band signaling

During OOB signaling transmissions, the differential and common mode levels of the signal lines shall comply with the same electrical specifications as for in-band data transmission, specified as follows.



5.1.2.2 Primitives descriptions

The following table contains the primitive mnemonics and a brief description of each.

Primitive	Name	Description
ALIGN	Physical layer control	Upon receipt of an ALIGN, the physical layer readjusts internal operations as necessary to perform its functions correctly.
EOF	End of frame	EOF marks the end of a frame.
PMACK	Power management acknowledge	Sent in response to a PMREQ_S or PMREQ_P when a receiving node is prepared to enter a power mode state.
PMNAK	Power management denial	Sent in response to a PMREQ_S or PMREQ_P when a receiving node is not prepared to enter a power mode state or when power management is not supported.
PMREQ_P	Power management request to partial	This primitive is sent continuously until PMACK or PMNAK is received. When PMACK is received, current node (host or device) will stop PMREQ_P and enters the Partial power management state.
PMREQ_S	Power management request to Slumber	This primitive is sent continuously until PMACK or PMNAK is received. When PMACK is received, current node (host or device) will stop PMREQ_S and enters the Slumber power management state.
R_ERR	Reception error	Current node (host or device) detected error in received payload.
R_OK	Reception with no error	Current node (host or device) detected no error in received payload.
R_RDY	Receiver ready	Current node (host or device) is ready to receive payload.
SOF	Start of frame	Start of a frame. Payload and CRC follow to EOF.
SYNC	Synchronization	Synchronizing primitive - always idle.
X_RDY	Transmission data ready	Current node (host or device) has payload ready for transmission.

5.1.3 Electrical specifications

Table 5.1 Physical Layer Electrical Requirements (1/2)

	Nom	Min	Max	Units	Comments
T,UI		666.43	670.12	ps	Operating data period (nominal value architecture specific)
t_{rise}	0.3	0.15	0.41	UI	20%-80% at transmitter
t_{fall}	0.3	0.15	0.41	UI	80%-20% at transmitter
$V_{cm,dc}$	250	200	450	mV	Common mode DC level measured at receiver connector
$V_{cm,ac\ coupled\ TX}$		0	2.0	V	Transmitter common mode DC level measured at TX pins
$V_{cm,ac\ coupled\ RX}$		0	2.0	V	Receiver common mode DC level measured at RX pins
F_{CM}		2	200	MHz	Sinusoidal common-mode noise components inside this frequency range with an amplitude of Vcm,ac.
$T_{settle,CM}$			10	ns	Maximum time for common-mode transients to and from the idle bus condition
$V_{diff,tx}$	500	400	600	mV_{p-p}	+/- 250 mV differential nominal. Measured at Serial ATA connector on transmit side
$V_{diff,rx}$	400	325	600	mV_{p-p}	+/- 200 mV differential nominal. Measured at Serial ATA connector on receive side
Tx pair differential impedance	100	85	115	Ohm	As seen by a differential TDR with 100 ps (max) edge looking into connector (20%-80%). Measured with TDR in differential mode.
Rx pair differential impedance	100	85	115	Ohm	As seen by a differential TDR with 100 ps (max) edge looking into connector (20%-80%). Measured with TDR in differential mode.
Tx single-ended impedance		40		Ohm	As seen by TDR with 100 ps (max) edge looking into connector (20%-80%). TDR set to produce simultaneous positive pulses on both signals of the Tx pair.

Table 5.1 Physical Layer Electrical Requirements (2/2)

	Nom	Min	Max	Units	Comments
Rx single-ended impedance		40		Ohm	As seen by TDR with 100 ps (max) edge looking into connector (20%-80%). TDR set to produce simultaneous positive pulses on both signals of the Rx pair.
$C_{ACcoupling}$			12	nF	Coupling capacitance value for AC coupled TX and RX pairs
TX DC clock frequency skew		-350	+350	ppm	Specifies the allowed ppm tolerance for TX DC frequency variations around the nominal 1.5GHz
TX AC clock frequency skew		-5000	+0	ppm	Specifies the allowed ppm tolerance for TX AC frequency variations around the nominal 1.5GHz
TX differential skew			20	ps	Nominal value architecture specific
Squelch detector threshold	100	50	200	mV_{p-p}	Minimum differential signal amplitude
COMRESET/COMINIT detector off threshold		175	525	ns	Detector shall reject all bursts with spacings outside this spec
COMRESET/COMINIT detector on threshold	320	304	336	ns	Detector shall detect all bursts with spacings meeting this period
COMRESET/COMINIT transmit spacing	320.0	310.4	329.6	ns	Differential crosspoints of last and first edges of bursts
COMWAKE detector off threshold		55	175	ns	Detector shall reject all bursts with spacings outside this spec
COMWAKE detector on threshold	106.7	101.3	112	ns	Detector shall detect all burst spacings meeting this period
COMWAKE transmit spacing	106.7	103.5	109.9	ns	Differential crosspoints from last to first edges of bursts
UI_{OOB}		646.67	686.67	ps	Operating data period during OOB burst transmission

5.1.4 Connector pinouts

The pin definitions are shown in Table 5.2.

Table 5.2 Connector pinouts

Signal segment key			
Signal segment	S1	Gnd	2nd mate
	S2	A+	Differential signal pair A from Phy
	S3	A-	
	S4	Gnd	2nd mate
	S5	B-	Differential signal pair B from Phy
	S6	B+	
	S7	Gnd	2nd mate
Signal segment “L”			
Central connector polarizer			
Power segment “L”			
Power segment	P1	V33	3.3 V power *1
	P2	V33	3.3 V power *1
	P3	V33	3.3 V power, pre-charge, 2nd mate *1
	P4	Gnd	1st mate
	P5	Gnd	2nd mate
	P6	Gnd	2nd mate
	P7	V5	5 V power, pre-charge, 2nd mate
	P8	V5	5 V power
	P9	V5	5 V power
	P10	Gnd	2nd mate
	P11	Reserved	The pin corresponding to P11 in the backplane receptacle connector is also reserved The corresponding pin to be mated with P11 in the power cable receptacle connector shall be grounded
	P12	Gnd	1st mate
	P13	V12	12 V power, pre-charge, 2nd mate *1
	P14	V12	12 V power *1
	P15	V12	12 V power *1
Power segment key			
Notes:			

*1 Since applying a single external supply voltage of 5V enables this drive to operate it is unnecessary to supply +3.3V and +12V power supplies.

5.2 Logical Interface

The host system and the device communicate with each other by sending and receiving serial data.

The host and the device have several dedicated communication layers between them. These layers have different functions, enabling communication between the different levels of layers within the host or device and between layers at the same level that link the host and device.

Figure 5.2 is a conceptual diagram of the communication layers.

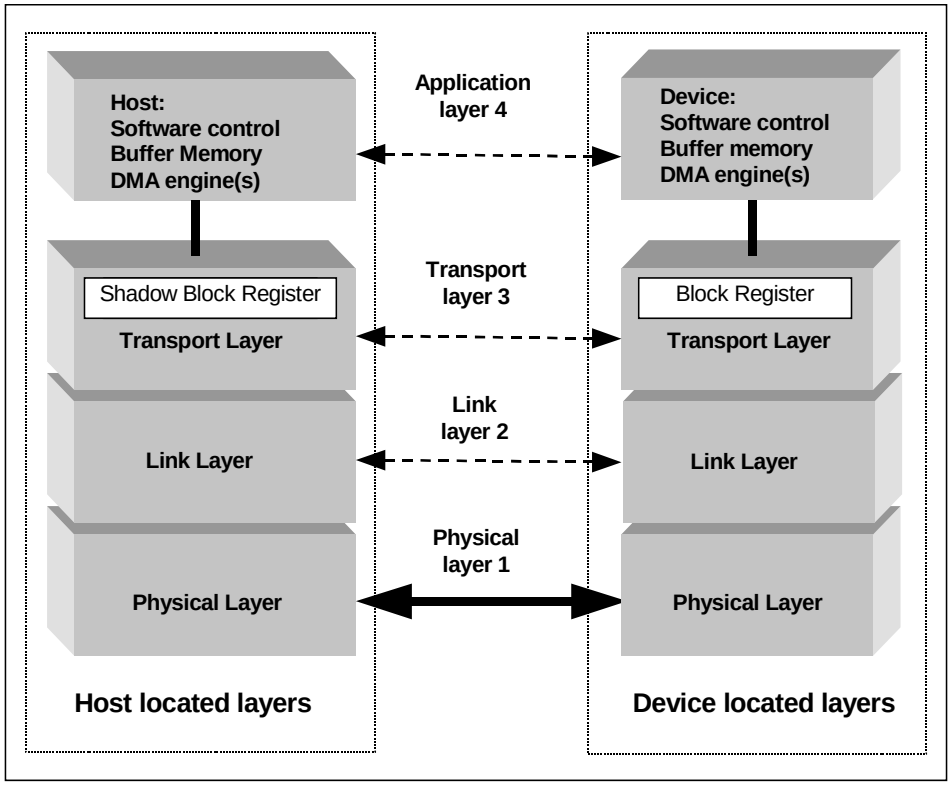


Figure 5.2 Conceptual diagram of communication layers

5.2.1 Communication layers

Each of the layers is outlined below.

Physical layer

- Detects, sends, and receives band signals.
- Sends serial data to and receives it from the link layer.

Link layer

- Negotiates against mutual transfer requests between the host system and device.
- Encodes serial data as 10- or 8-bit data, then converts it into DWORD data.
- Inserts auxiliary signals (SOF, CRC, and EOF), deletes auxiliary signals, and communicates with the transport and physical layers.

Transport layer

- Exchanges data in communication with the link layer, and builds the frame information structure (FIS).
- Contains a (Shadow) Block Register.
- Reflects the FIS contents to the Block Register.

5.2.2 Outline of the Shadow Block Register

Each transport layer in the host system and device has a block register, which is called a Shadow Block Register in the host system, and a Block Register in the device.

These registers are used when the host system issues a command to the device.

Table 5.3 Shadow Block Register

<table>
<tr><td colspan="4">Command Block registers</td></tr>
<tr><td colspan="2">Read</td><td colspan="2">Write</td></tr>
<tr><td colspan="4">Data Port</td></tr>
<tr><td colspan="2">Error</td><td colspan="2">Features</td></tr>
<tr><td>Sector Count (exp)</td><td>Sector Count</td><td>Sector Count (exp)</td><td>Sector Count</td></tr>
<tr><td>Sector Number (exp)</td><td>Sector Number</td><td>Sector Number (exp)</td><td>Sector Number</td></tr>
<tr><td>Cylinder Low (exp)</td><td>Cylinder Low</td><td>Cylinder Low (exp)</td><td>Cylinder Low</td></tr>
<tr><td>Cylinder High (exp)</td><td>Cylinder High</td><td>Cylinder High (exp)</td><td>Cylinder High</td></tr>
<tr><td colspan="4">Device / Head</td></tr>
<tr><td colspan="2">Status</td><td colspan="2">Command</td></tr>
<tr><td colspan="4">Control Block registers</td></tr>
<tr><td colspan="2">Alternate Status</td><td colspan="2">Device Control</td></tr>
</table>

Note: Each of the Sector Count, Sector Number, Cylinder Low, and Cylinder High fields has a higher-order field used for issuing the Ext command. The fields are called Sector Count exp, Sector Number exp, Cylinder Low exp, and Cylinder High exp, respectively. For information on writing data to these fields, see "Device Control Field."

5.2.3 Outline of the frame information structure (FIS)

The transport layer converts data written in a Block Register into the FIS, and sends it to the upper layer.

The FIS, which is generated in the transport layer, is explained below.

5.2.3.1 FIS types

The types of FIS are as follows:

- Register- Host to Device
- Register- Device to Host
- DMA Active – Device to Host
- DMA Setup – Device to Host or Host to Device (Bidirectional)
- Set Device Bits – Device to Host
- BIST Active – Bidirectional
- PIO Setup – Device to Host
- Data – Host to Device or Device to Host (Bidirectional)

5.2.3.2 Register - Host to Device

The Register - Host to Device FIS has the following layout:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Features								Command								C	R	R	Reserved (0)					FIS Type (27h)							
1	Device								LBA High								LBA Mid								LBA Low							
2	Features (exp)								LBA High (exp)								LBA Mid (exp)								LBA Low (exp)							
3	Control								Reserved (0)								Sector Count (exp)								Sector Count							
4	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							

Figure 5.3 Register - Host to Device FIS layout

The host system uses the Register - Host to Device FIS when information in the Register Block is transferred from the host system to the device. This is the mechanism for issuing the ATA command from the host system to the device.

C - To update the Command field, "1" would be set in this field; and to update the Device Control field, "0" would be set in the field.

If both C = 1 and SRST = 1 are set, operation is not guaranteed.

5.2.3.3 Register - Device to Host

The Register - Device to Host FIS has the following layout:

	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12 11 10 9 8	7 6 5 4 3 2 1 0
0	Error	Status	R	I	R	Reserved (0)	FIS Type (34h)
1	Device	LBA High	LBA Mid				LBA Low
2	Reserved (0)	LBA High (exp)	LBA Mid (exp)				LBA Low (exp) (0)
3	Reserved (0)	Reserved (0)	Sector Count (exp)				Sector Count
4	Reserved (0)	Reserved (0)	Reserved (0)				Reserved (0)

Figure 5.4 Register - Device to Host FIS layout

The Register - Device to Host FIS is used when information concerning the Shadow Register Block in the host adapter is updated. This FIS indicates that the device has completed a command operation. Furthermore, this is a mechanism for changing information concerning the Shadow Register Block of the host adapter.

I - If this bit is set, an interrupt request is issued to the host system.

5.2.3.4 DMA Active - Device to Host

The DMA Active - Device to Host FIS has the following layout:

	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12 11 10 9 8	7 6 5 4 3 2 1 0
0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (39h)

Figure 5.5 DMA Active - Device to Host FIS layout

The host uses the DMA Active - Device to Host FIS layout. This FIS instructs the host to continue transferring DMA data from the host to the device.

5.2.3.5 DMA Setup - Device to Host or Host to Device (Bidirectional)

The DMA Setup - Device to Host or Host to Device FIS has the following layout:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved (0)								Reserved (0)								A	I	D	Reserved (0)					FIS Type (41h)							
1	0																											TAG				
2	0																															
3	Reserved (0)																															
4	DMA Buffer Offset																															
5	DMA Transfer Count																															
6	Reserved (0)																															

Figure 5.6 DMA Setup - Device to Host or Host to Device FIS layout

The DMA Setup - Device to Host or Host to Device FIS communicates the start of a first-party DMA access to the host system. This FIS is used to request the host system or device to set up the DMA controller before the start of a DMA data transfer.

A - Auto Active bit. If this bit is cleared ("0" is set for the bit), it indicates that a DMA Active FIS transfer is required before a Data FIS transfer.

D - Direction bit. If this bit is set ("1" is set for the bit), it indicates that the data transfer direction is from the device to the host system.

5.2.3.6 BIST Active - Bidirectional

The BIST Active - Bidirectional FIS has the following layout:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved (0)								Pattern definition T	A	S	L	F	P	R	V	R	R	R	Reserved (0)								FIS Type (58h)								
1	Data [31:24]								Data [23:16]								Data [23:16]								Data [7:0]							
2	Data [31:24]								Data [23:16]								Data [23:16]								Data [7:0]							

Figure 5.7 BIST Active - Bidirectional FIS layout

The BIST Active - Bidirectional FIS is used to set the receiver to Loop Back mode. This FIS can be sent by either the host system or device.

The following combinations of pattern definitions are supported:

Table 5.4 BIST combinations

T	A	S	L	F	P	V	SC Reg	Contents
-	-	-	1	-	-	1	09h	SATA Phy Analog Loopback Mode
-	-	-	1	-	-	-	10h	Far End Retimed Loopback Mode
1	1	-	-	-	-	-	C0h	No ALIGN Transmit_only Mode (Scramble ON) (*1)
1	1	1	-	-	-	-	E0h	No ALIGN Transmit_only Mode (Scramble OFF)
1	1	-	-	-	1	-	C4h	No ALIGN Transmit_only with primitive Mode (Scramble ON) (*1)
1	1	1	-	-	1	-	E4h	No ALIGN Transmit_only with primitive Mode (Scramble OFF)
1	-	-	-	-	-	-	80h	ALIGN Transmit_only Mode (Scramble ON) (*1)
1	-	1	-	-	-	-	A0h	ALIGN Transmit_only Mode (Scramble OFF)
1	-	-	-	-	1	-	84h	ALIGN Transmit_only with primitive Mode (Scramble ON) (*1)
1	-	1	-	-	1	-	A4h	ALIGN Transmit_only with primitive Mode (Scramble OFF)

5.2.3.7 Data - Host to Device or Device to Host (Bidirectional)

This Data FIS has the following layout:

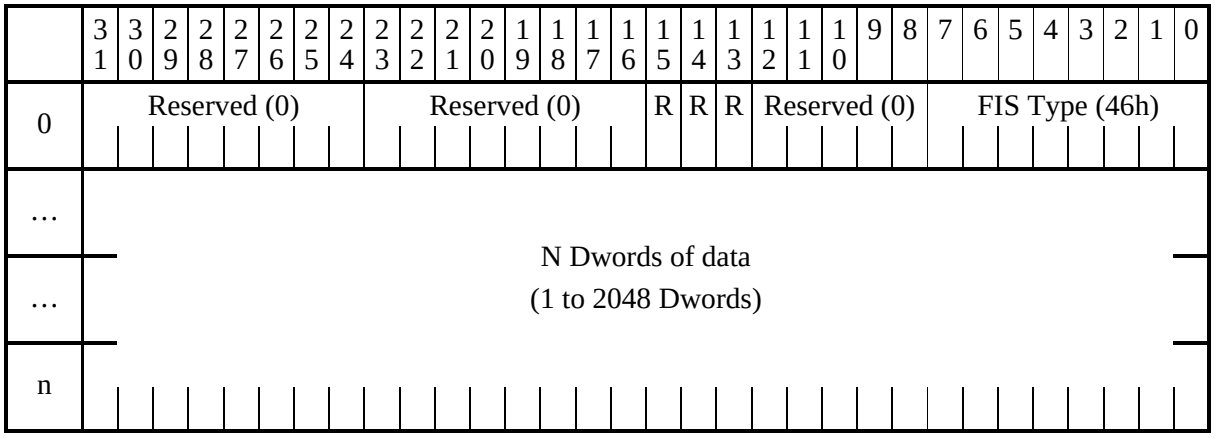


Figure 5.8 Data FIS (Bidirectional) layout

The Data FIS is used for data transfers between the host system and device.

5.2.4 Shadow block registers

(1) Error Field

The Error Field indicates the status of the command executed by the device. The fields are valid when the ERR bit of the Status field is 1.

This register contains a diagnostic code after power is turned on, the Com Reset, or the EXECUTIVE DEVICE DIAGNOSTIC command is executed.

- [Status at the completion of command execution other than diagnostic command]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	UNC	X	IDNF/ SFRW	SFRR	ABRT	TK0NF	AMNF

X: Unused

- Bit 7: Unused
- Bit 6: Uncorrectable Data Error (UNC). This bit indicates that an uncorrectable data error has been encountered.

  SATA Frame Error Write (SF RW). This bit indicates that a SATA communication error has been encountered during the write process.
- Bit 5: Unused
- Bit 4: ID Not Found (IDNF). This bit indicates an error except for bad sector, uncorrectable error and SB not found.

  Or, SATA Frame Error Write (SFRW) This bit indicates that a SATA communication error has been encountered during the write process. In this case, bit4 and bit2 are set both.
- Bit 3: SATA Frame Error Read (SF RR). This bit indicates that a SATA communication error has been encountered during the read process. In this case, bit3 and bit2 are set both.
- Bit 2: Aborted Command (ABRT). This bit indicates that the requested command was aborted due to a device status error (e.g. Not Ready, Write Fault) or the command code was invalid.
- Bit 1: Track 0 Not Found (TK0NF). This bit indicates that track 0 was not found during RECALIBRATE command execution.
- Bit 0: Address Mark Not Found (AMNF). This bit indicates that the SB Not Found error occurred.

[Diagnostic code]

- X'00': Format Unit is not completed.
- X'01': No Error Detected.
- X'02': HDC Diagnostic Error

- X’03’: Data Buffer Diagnostic Error.
- X’04’: Memory Diagnostic Error.
- X’05’: Reading the system area is abnormal.
- X’06’: Calibration is abnormal.

(2) Features Field (exp)

The Features Field provides specific feature to a command. For instance, it is used with SET FEATURES command to enable or disable caching.

(3) Sector Count Field (exp)

The Sector Count Field indicates the number of sectors of data to be transferred in a read or write operation between the host system and the device. When the value in this field is X’00’, the sector count is 256. With the EXT system command, the sector count is 65536 when value of the Sector Count Field is X'00' and that of the Sector Count Field (exp) is X’00’.

When this field indicates 0 at the completion of the command execution, this indicates that the command is completed successfully. If the command is not completed successfully, this field indicates the number of sectors to be transferred to complete the request from the host system. That is, this field indicates the number of remaining sectors that the data has not been transferred due to the error. However, as of the last sector of PIO transfer, SC=1 indicates the normal completion.

The contents of this field also have other definitions (Refer to 5.4)

(4) Sector Number Field (exp)

The contents of this field indicates the starting sector number for the subsequent command. The sector number should be between X’01’ and [the number of sectors per track defined by INITIALIZE DEVICE PARAMETERS command.

Under the LBA mode, this field indicates LBA bits 7 to 0. Under the LBA mode of the EXT system command, LBA bits 31 to 24 are set in the Sector Number Field, and LBA bits 7 to 0 are set in the Sector Number Field (exp).

(5) Cylinder Low Field (exp)

The contents of this field indicates low-order 8 bits of the starting cylinder address for any disk-access.

At the end of a command, the contents of this field are updated to the current cylinder number.

Under the LBA mode, this field indicates LBA bits 15 to 8. Under the LBA mode of the EXT system command, LBA bits 39 to 32 are set in the Cylinder Low Field, and LBA bits 15 to 8 are set in the Cylinder Low Field (exp).

(6) Cylinder High Field (exp)

The contents of this field indicates high-order 8 bits of the disk-access start cylinder address.

At the end of a command, the contents of this field are updated to the current cylinder number. The high-order 8 bits of the cylinder address are set to the Cylinder High Register.

Under the LBA mode, this field indicates LBA bits 23 to 16. Under the LBA mode of the EXT system command, LBA bits 47 to 40 are set in the Cylinder High Field, and LBA bits 23 to 16 are set in the Cylinder High Field (exp).

(7) Device/Head Field

The contents of this field indicate the device and the head number.

When executing INITIALIZE DEVICE PARAMETERS command, the contents of this field defines “the number of heads minus 1” (a maximum head No.).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	L	X	X	HS3	HS2	HS1	HS0

- Bit 7: Unused
- Bit 6: L. 0 for CHS mode and 1 for LBA mode.
- Bit 5: Unused
- Bit 4: Unused
- Bit 3: HS3 CHS mode head address 3 (2^3). bit 27 for LBA mode. Unused under the LBA mode of the EXT command.
- Bit 2: HS2 CHS mode head address 2 (2^2). bit 26 for LBA mode. Unused under the LBA mode of the EXT command.
- Bit 1: HS1 CHS mode head address 1 (2^1). bit 25 for LBA mode. Unused under the LBA mode of the EXT command.
- Bit 0: HS0 CHS mode head address 0 (2^0). bit 24 for LBA mode. Unused under the LBA mode of the EXT command.

(8) Status field

The contents of this field indicate the status of the device. The contents of this field are updated at the completion of each command. When the BSY bit is 1, other bits of this field, are invalid.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BSY	DRDY	DF	DSC	DRQ	0	0	ERR

- Bit 7: Busy (BSY) bit.

  This bit is set whenever the Command filed of the shadow block registers for the host system is accessed.

  Then this bit is cleared when the command is completed. However, even if a command is being executed, this bit is cleared during the PIO data transfer request.

  When BSY bit is 1, the host system should not write the shadow block registers. This bit is set by the device under following conditions:

  (a) After COMRESET or SRST is set in the Device Control Field, the BSY bit is set, then the BSY bit is cleared, when the COMRESET process is completed.

  The BSY bit is set for no longer than 15 seconds after the IDD accepts reset.

- Bit 6: Device Ready (DRDY) bit.

  This bit indicates that the device is capable to respond to a command.

  The IDD checks its status when it receives a command. If an error is detected (not ready state), the IDD clears this bit to 0. This is cleared to 0 at power-on and it is cleared until the rotational speed of the spindle motor reaches the steady speed.

- Bit 5: Device Write Fault (DF) bit.

  This bit indicates that a device fault (write fault) condition has been detected.

  If a write fault is detected during command execution, this bit is latched and retained until the device accepts the next command or reset.

- Bit 4: Device Seek Complete (DSC) bit.

  This bit indicates that the device heads are positioned over a track.

  In the IDD, this bit is always set to 1 after the spin-up control is completed.

- Bit 3: Data Request (DRQ) bit.

  This bit indicates that the device is ready to transfer PIO data of word unit or byte unit between the host system and the device.

- Bit 2: Always 0.

- Bit 1: Always 0.

- Bit 0: Error (ERR) bit.

  This bit indicates that an error was detected while the previous command was being executed. The Error field indicates the additional information of the cause for the error.

(9) Command Field

The Command Field contains a command code being sent to the device. After this field is written, the command execution starts immediately.

Table 5.3 lists the executable commands and their command codes. This table also lists the necessary parameters for each command which are written to certain fields before the Command register is written.

(10) Device Control Field

The Device Control Field contains software reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	SRST	X	0

- Bit 2: Software Reset (SRST)

This is the host software reset bit. When this bit is set, the device is held reset state.

The slave device is not required to execute the DASP- handshake.

(11) E_Status Field

This field is in the PIO Setup FIS. The field contents are the same as those described in (8), "Status Field." However, the values in the Status field are those before a PIO data transfer, and the values in the E_Status field are those when a PIO data transfer is completed.

(12) DMA Buffer Offset Field

This field is in the DMA Setup FIS, representing byte offset. Since this device does not support byte offset, 0 is always set for the field.

(13) DMA Transfer Count Field

This field is in the DMA Setup FIS, representing the number of bytes to be transferred.

(14) Active Field

This field is in the Set Device Bits FIS. Each bit number corresponds to the tag number of one of 32 commands that can be placed in a queue, and the bit setting of "1" indicates that the corresponding command is completed.

5.3 Host Commands

The host system issues a command to the device by writing necessary parameters in related fileds in the shadow block registers and writing a command code in the Command field of the shadow block registers.

The device can accept the command when the BSY bit is 0 (the device is not in the busy status).

The host system can halt the uncompleted command execution only at execution of hardware or software reset.

When the BSY bit is 1 or the DRQ bit is 1 (the device is requesting the PIO data transfer) and the host system writes to the command field of the shadow block register, the correct device operation is not guaranteed.

5.3.1 Command code and parameters

Table 5.5 lists the supported commands, command code and the related fields to be written necessary parameters at command execution.

Table 5.5 Command code and parameters (1/3)

COMMAND NAME	COMMAND CODE (Bit)								PARAMETER USED				
	7	6	5	4	3	2	1	0	FR	SC	SN	CY	DH
RECALIBRATE	0	0	0	1	X	X	X	X	N	N	N	N	D
READ SECTOR(S)	0	0	1	0	0	0	0	R	N	Y	Y	Y	Y
READ LONG	0	0	1	0	0	0	1	R	N	Y	Y	Y	Y
WRITE SECTOR(S)	0	0	1	1	0	0	0	R	N	Y	Y	Y	Y
WRITE LONG	0	0	1	1	0	0	1	R	N	Y	Y	Y	Y
WRITE VERIFY	0	0	1	1	1	1	0	0	N	Y	Y	Y	Y
READ VERIFY SECTOR(S)	0	1	0	0	0	0	0	R	N	Y	Y	Y	Y
SEEK	0	1	1	1	X	X	X	X	N	N	Y	Y	Y
EXECUTE DEVICE DIAGNOSTIC	1	0	0	1	0	0	0	0	N	N	N	N	N
INITIALIZE DEVICE PARAMETERS	1	0	0	1	0	0	0	1	N	Y	N	N	Y
DOWNLOAD MICROCODE	1	0	0	1	0	0	1	0	Y	Y	Y	N	D
STANDBY IMMEDIATE	1 1	0 1	0 1	1 0	0 0	1 0	0 0	0 0	N	N	N	N	D
IDLE IMMEDIATE	1 1	0 1	0 1	1 0	0 0	1 0	0 0	1 1	Y	N	Y	Y	D
STANDBY	1 1	0 1	0 1	1 0	0 0	1 0	1 1	0 0	N	Y	N	N	D

Table 5.5 Command code and parameters (2/3)

COMMAND NAME	COMMAND CODE (Bit)								PARAMETER USED				
	7	6	5	4	3	2	1	0	FR	SC	SN	CY	DH
IDLE	1 1	0 1	0 1	1 0	0 0	1 0	1 1	1 1	N	Y	N	N	D
CHECK POWER MODE	1 1	0 1	0 1	1 0	1 0	0 1	0 0	0 1	N	N	N	N	D
SLEEP	1 1	0 1	0 1	1 0	1 0	0 1	0 1	1 0	N	N	N	N	D
SMART	1	0	1	1	0	0	0	0	Y	Y	Y	Y	D
DEVICE CONFIGURATION	1	0	1	1	0	0	0	1	Y	N	N	N	D
READ MULTIPLE	1	1	0	0	0	1	0	0	N	Y	Y	Y	Y
WRITE MULTIPLE	1	1	0	0	0	1	0	1	N	Y	Y	Y	Y
SET MULTIPLE MODE	1	1	0	0	0	1	1	0	N	Y	N	N	D
READ DMA	1	1	0	0	1	0	0	R	N	Y	Y	Y	Y
WRITE DMA	1	1	0	0	1	0	1	R	N	Y	Y	Y	Y
READ BUFFER	1	1	1	0	0	1	0	0	N	N	N	N	D
FLUSH CACHE	1	1	1	0	0	1	1	1	N	N	N	N	D
WRITE BUFFER	1	1	1	0	1	0	0	0	N	N	N	N	D
IDENTIFY DEVICE	1	1	1	0	1	1	0	0	N	N	N	N	D
IDENTIFY DEVICE DMA	1	1	1	0	1	1	1	0	N	N	N	N	D
SET FEATURES	1	1	1	0	1	1	1	1	Y	N*	N	N	D
SECURITY SET PASSWORD	1	1	1	1	0	0	0	1	N	N	N	N	D
SECURITY UNLOCK	1	1	1	1	0	0	1	0	N	N	N	N	D
SECURITY ERASE PREPARE	1	1	1	1	0	0	1	1	N	N	N	N	D
SECURITY ERASE UNIT	1	1	1	1	0	1	0	0	N	N	N	N	D
SECURITY FREEZE LOCK	1	1	1	1	0	1	0	1	N	N	N	N	D
SECURITY DISABLE PASSWORD	1	1	1	1	0	1	1	0	N	N	N	N	D
READ NATIVE MAX ADDRESS	1	1	1	1	1	0	0	0	N	N	N	N	D
SET MAX	1	1	1	1	1	0	0	1	N	Y	Y	Y	Y
READ SECTOR(S) EXT	0	0	1	0	0	1	0	0	N	Y	Y	Y	D
READ DMA EXT	0	0	1	0	0	1	0	1	N	Y	Y	Y	D
READ NATIVE MAX ADDRESS EXT	0	0	1	0	0	1	1	1	N	N	N	N	D
READ MULTIPLE EXT	0	0	1	0	1	0	0	1	N	Y	Y	Y	D

Table 5.5 Command code and parameters (3/3)

COMMAND NAME	COMMAND CODE (Bit)								PARAMETER USED				
	7	6	5	4	3	2	1	0	FR	SC	SN	CY	DH
READ LOG EXT	0	0	1	0	1	1	1	1	N	Y	Y	Y	D
WRITE SECTOR(S) EXT	0	0	1	1	0	1	0	0	N	Y	Y	Y	D
WRITE DMA EXT	0	0	1	1	0	1	0	1	N	Y	Y	Y	D
SET MAX ADDRESS EXT	0	0	1	1	0	1	1	1	N	Y	Y	Y	Y
WRITE MULTIPLE EXT	0	0	1	1	1	0	0	1	N	Y	Y	Y	D
WRITE LOG EXT	0	0	1	1	1	1	1	1	N	Y	Y	Y	D
READ VERIFY SECTOR(S) EXT	0	1	0	0	0	0	1	0	N	Y	Y	Y	D
FLUSH CACHE EXT	1	1	1	0	1	0	1	0	N	N	N	N	D
WRITE MULTIPLE FUA EXT	1	1	0	0	1	1	1	0	N	Y	Y	Y	D
WRITE DMA FUA EXT	0	0	1	1	1	1	0	1	N	Y	Y	Y	D
READ FP DMA QUEUED	0	1	1	0	0	0	0	0	Y	Y	Y	Y	D
WRITE FP DMA QUEUED	0	1	1	0	0	0	0	1	Y	Y	Y	Y	D

CY: cylinder field

DH: device/head field

FR: features field

SC: sector count field

SN: sector number field

R: Retry at error
1 = Without retry
0 = With retry

Y: Necessary to set parameters

Y*: Necessary to set parameters under the LBA mode.

N: Not necessary to set parameters (The parameter is ignored if it is set.)

N*: May set parameters

D: The device parameter is valid, and the head parameter is ignored.

X: Do not care

5.3.2 Command descriptions

The contents of the shadow block registers to be necessary for issuing a command and the example indication of the shadow block registers at command completion are shown as following in this subsection.

Example: READ SECTOR (S)

At command issuance (Shadow Block Registers setting contents)								
Bit	7	6	5	4	3	2	1	0
CM	0	0	1	0	0	0	0	0
DH	x	L	x	x	HD No./LBA			
CH EXP	LBA(47-40)							
CH	Start cylinder address [MSB] / LBA(23-16)							
CL EXP	LBA(39-32)							
CL	Start cylinder address [LSB] / LBA(15-8)							
SN EXP	LBA(31-24)							
SN	Start sector No. / LBA (7-0)							
SC EXP	Transfer sector count (15-8)							
SC	Transfer sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers to be read)								
Bit	7	6	5	4	3	2	1	0
ST	Status information							
DH	x	L	x	x	HD No./LBA			
CH EXP	LBA(47-40)							
CH	End cylinder address [MSB] / LBA(23-16)							
CL EXP	LBA(39-32)							
CL	End cylinder address [LSB] / LBA(15-8)							
SN EXP	LBA(31-24)							
SN	End sector No. / LBA (7-0)							
SC EXP	X ' 00 '							
SC	X ' 00 '							
ER	Error information							

CH (EXP): Cylinder High Field (EXP)
CL (EXP): Cylinder Low Field (EXP)
CM: Command Field
DH: Device/Head Field
ER: Error Field
FR (EXP): Features Field (EXP)
L: LBA (Logical Block Address) setting bit
SN (EXP): Sector Number Field (EXP)
SC (EXP): Sector Count Field (EXP)
ST: Status Field
x, xx: Don't care (setting is not necessary)

Note:

1. When the L bit is specified to 1, the lower 4 bits of the DH field and all bits of the CH field, CL and SN fields indicate the LBA bits (bits of the DH filed are the MSB (most significant bit) and bits of the SN field are the LSB (least significant bit).
2. At error occurrence, the SC field indicates the remaining sector count of data transfer.
3. Bit indication is omitted in each command description.

(1) RECALIBRATE (X'10' to X'1F')

This command performs the calibration. When the device completes the calibration, the device reports the status to the host system.

This command can be issued in the LBA mode.

- Error reporting conditions

  (1) An error was detected during head positioning (ST = 51h, ER = 02h).

  (2) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	0	1	x	x	x	x
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

Note:

Also executable in LBA mode.

(2) READ SECTOR(S) (X'20' or X'21')

This command reads data of sectors specified in the Sector Count field from the address specified in the Device/Head, Cylinder High, Cylinder Low and Sector Number fields. Number of sectors can be specified from 1 to 256 sectors. To specify 256 sectors reading, '00' is specified. For the protocols related to data transfer, see Subsection 5.4.1.

If the head is not on the track specified by the host, the device performs an implied seek. After the head reaches to the specified track, the device reads the target sector.

If an error occurs, retry reads are attempted to read the target sector before reporting an error, irrespective of the R bit setting.

If an error does not occur, PIO Setup is always transferred prior to the data transfer.

Upon the completion of the command execution, shadow block registers contain the cylinder, head, and sector addresses (in the CHS mode) or logical block address (in the LBA mode) of the last sector read.

If an unrecoverable disk read error occurs in a sector, the read operation is terminated at the sector where the error occurred. Shadow block registers contain the cylinder, the head, and the sector addresses of the sector (in the CHS mode) or the logical block address (in the LBA mode) where the error occurred, and remaining number of sectors of which data was not transferred (including sector when the error occurred).

- Error reporting conditions

  (1) A specified address exceeds the range where read operations are allowed (ST = 51h, ER = 10h).

  (2) The range where read operations are allowed will be exceeded by an address during a read operation (ST = 51h, ER = 10h).

  (3) An uncorrectable disk read error occurred (ST = 51h, ER = 40h).

  (4) The sync byte indicating the beginning of a sector was not found (ST = 51h, ER = 01h).

  (5) A communication error occurred (ST = 51h, ER = 0Ch).

  (6) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	0	0	0	0	R
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	Transfer sector count							
FR	xx							

(R: Retry)

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	L	x	x	HD No. / LBA
CH	End cylinder No. [MSB] / LBA				
CL	End cylinder No. [LSB] / LBA				
SN	End sector No. / LBA [LSB]				
SC	01 (*1)				
ER	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors of which data was not transferred.

(3) READ LONG (X'22' or X'23')

This command operates similarly to the READ SECTOR(S) command except that the device transfers the data in the requested sector and the ECC bytes to the host system. The ECC error correction is not performed for this command. This command is used for checking ECC function by combining with the WRITE LONG command. The READ LONG command supports only single sector operation.

Number of ECC bytes to be transferred is fixed to 4 bytes and cannot be changed by the SET FEATURES command.

- Error reporting conditions

  (1) A specified address exceeds the range where read operations are allowed (ST = 51h, ER = 10h).

  (2) A value other than 01h is specified in the SC field (ST = 51h, ER = 04h).

  (3) The sync byte indicating the beginning of a sector was not found (ST = 51h, ER = 01h).

  (4) A SATA communication error occurred (ST = 51h, ER = 0Ch).

  (5) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	0	0	0	1	R
DH	x	L	x	x	HD No. /LBA			
CH	Cylinder No. [MSB] / LBA							
CL	Cylinder No. [LSB] / LBA							
SN	Sector No. / LBA [LSB]							
SC	01							
FR	xx							

(R: Retry)

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	L	x	x	HD No. /LBA
CH	Cylinder No. [MSB] / LBA				
CL	Cylinder No. [LSB] / LBA				
SN	Sector No. / LBA [LSB]				
SC	xx				
ER	Error information				

(4) WRITE SECTOR(S) (X'30' or X'31')

This command writes data of sectors from the address specified in the Device/Head, Cylinder High, Cylinder Low, and Sector Number fields to the address specified in the Sector Count field. Number of sectors can be specified from 1 to 256 sectors. A sector count of 0 requests 256 sectors. Data transfer begins at the sector specified in the Sector Number field. For the protocols related to data transfer, see Subsection 5.4.3.

If the head is not on the track specified by the host, the device performs an implied seek. After the head reaches to the specified track, the device writes the target sector.

If an error occurs when writing to the target sector, retries are attempted irrespectively of the R bit setting.

The data stored in the buffer, and CRC code and ECC bytes are written to the data field of the corresponding sector(s).

Upon the completion of the command execution, the shadow block registers contain the cylinder, head, and sector addresses of the last sector written.

If an disk error occurs during multiple sector write operation, the write operation is terminated at the sector where the error occurred. Shadow block registers contain the cylinder, the head, the sector addresses (in the CHS mode) or the logical block address (in the LBA mode) of the sector where the error occurred.

- Error reporting conditions

  (1) A specified address exceeds the range where write operations are allowed (after a transfer of dummy data, ST = 51h, ER = 10h).

  (2) The range where write operations are allowed will be exceeded by an address during a write operation (after a transfer of dummy data, ST = 51h, ER = 10h).

  (3) A write fault was detected when the write cache was disabled (ST = 71h, ER = 10h).

  (4) While the write cache is enabled, if the status indicating a completed transfer (STS = 50h) is returned and a data write operation failed because a write fault was detected during the data write operation, Abort will be returned for all subsequent ATA commands (ST = 71h, ER = 04h). This state is cleared the next time that the device is turned on.

  (5) A SATA communication error occurred (ST = 51h, ER = 14h).

  (6) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	1	0	0	0	R
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	Transfer sector count							
FR	xx							

(R: Retry)

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	L	x	x	HD No. / LBA
CH	End cylinder No. [MSB] / LBA				
CL	End cylinder No. [LSB] / LBA				
SN	End sector No. / LBA [LSB]				
SC	00 (*1)				
ER	Error information				

*1 If the command was terminated because of an error, the number of sectors for which data has not been written is set in this field.

(5) WRITE LONG (X'32' or X'33')

This command operates similarly to the WRITE SECTOR(S) command except that the device writes the data and the ECC bytes transferred from the host system to the disk medium. The device does not generate ECC bytes by itself. The WRITE LONG command supports only single sector operation.

The number of ECC bytes to be transferred is fixed to 4 bytes and can not be changed by the SET FEATURES command.

This command is operated under the following conditions:

- READ LONG issued → WRITE LONG (Same address) issues sequence (After READ LONG is issued, WRITE LONG can be issued consecutively.)

If the above condition is not satisfied, WRITE LONG Data becomes an uncorrectable error for subsequent READ command.

- Error reporting conditions

(1) A specified address exceeds the range where write operations are allowed (after a transfer of dummy data, ST = 51h, ER = 10h).

(2) The range where write operations are allowed will be exceeded by an address during a write operation (after a transfer of dummy data, ST = 51h, ER = 10h).

(3) A write fault was detected when the write cache was disabled (ST = 71h, ER = 10h).

(4) While the write cache is enabled, if the status indicating a completed transfer (STS = 50h) is returned and a data write operation failed because a write fault was detected during the data write operation, Abort will be returned for all subsequent ATA commands (ST = 71h, ER = 04h). This state is cleared the next time that the device is turned on.

(5) A SATA communication error occurred (ST = 51h, ER = 14h).

(6) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	1	0	0	1	R
DH	x	L	x	x	HD No. /LBA			
CH	Cylinder No. [MSB] / LBA							
CL	Cylinder No. [LSB] / LBA							
SN	Sector No. / LBA [LSB]							
SC	01							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	L	x	x	HD No. /LBA
CH	Cylinder No. [MSB] / LBA				
CL	Cylinder No. [LSB] / LBA				
SN	Sector No. / LBA [LSB]				
SC	xx				
ER	Error information				

(6) WRITE VERIFY (X'3C')

This command operates similarly to the WRITE SECTOR(S) command except that the device verifies each sector immediately after being written. The verify operation is a read and check for data errors without data transfer. Any error that is detected during the verify operation is posted.

After all sectors are verified, device reports the status to the host system.

- Error reporting conditions

(1) A specified address exceeds the range where write operations are allowed (after a transfer of dummy data, ST = 51h, ER = 10h).

(2) The range where write operations are allowed will be exceeded by an address during a write operation (after a transfer of dummy data, ST = 51h, ER = 10h).

(3) A write fault was detected when the write cache was disabled (ST = 71h, ER = 10h).

(4) While the write cache is enabled, if the status indicating a completed transfer (STS = 50h) is returned and a data write operation failed because a write fault was detected during the data write operation, Abort will be returned for all subsequent ATA commands (ST = 71h, ER = 04h). This state is cleared the next time that the device is turned on.

(5) An uncorrectable read error occurred disk (ST = 51h, ER = 40h).

(6) A SATA communication error occurred (ST = 51h, ER = 14h).

(7) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	1	1	1	0	0
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	Transfer sector count							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	L	x	x	HD No. / LBA
CH	Start cylinder No. [MSB] / LBA				
CL	Start cylinder No. [LSB] / LBA				
SN	Start sector No. / LBA [LSB]				
SC	00 (*1)				
ER	Error information				

*1 If the command is terminated because of an error, the number of remaining sectors for which data has not been written or verified is set in this register.

(7) READ VERIFY SECTOR(S) (X'40' or X'41')

This command operates similarly to the READ SECTOR(S) command except that the data is not transferred to the host system.

After all requested sectors are verified, the device reports the status to the host system.

Upon the completion of the command execution, the shadow block registers contain the cylinder, head, and sector number of the last sector verified.

If an unrecoverable disk error occurs, the verify operation is terminated at the sector where the error occurred. The shadow block registers contain the cylinder, the head, and the sector addresses (in the CHS mode) or the logical block address (in the LBA mode) of the sector where the error occurred. The Sector Count field indicates the number of sectors that have not been verified.

- Error reporting conditions

  (1) A specified address exceeds the range where read operations are allowed (ST = 51h, ER = 10h).

  (2) The range where read operations are allowed will be exceeded by an address during a read operation (ST = 51h, ER = 10h).

  (3) An uncorrectable disk read error occurred (ST = 51h, ER = 40h).

  (4) The sync byte indicating the beginning of a sector was not found (ST = 51h, ER = 01h).

  (5) A SATA communication error occurred (ST = 51h, ER = 01h).

  (6) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	1	0	0	0	0	0	R
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	Transfer sector count							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	L	x	x	HD No. / LBA
CH	Start cylinder No. [MSB] / LBA				
CL	Start cylinder No. [LSB] / LBA				
SN	Start sector No. / LBA [LSB]				
SC	00 (*1)				
ER	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors of which data was not transferred is set in this register.

(8) SEEK (X'70' to X'7F')

This command performs a seek operation to the track and selects the head specified in the command block registers. After completing the seek operation, the device reports the status to the host system.

In the LBA mode, this command performs the seek operation to the cylinder and head position in which the sector is specified.

- Error reporting conditions

(1) A specified address exceeds the range where the head can be positioned (ST = 51h, ER = 10h).

(2) Head positioning is not possible because an error occurred (ST = 51h, ER = 10h).

(3) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	1	1	1	x	x	x	x
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)								
ST	Status information							
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	xx							
ER	Error information							

(9) EXECUTE DEVICE DIAGNOSTIC (X'90')

This command performs an internal diagnostic test (self-diagnosis) of the device.

The device reports the diagnostic result and status to the host.

Table 5.6 lists the diagnostic code written in the Error field which is 8-bit code.

Table 5.6 Diagnostic code

Code	Result of diagnostic
X'00'	Format Unit is not completed.
X'01'	No error detected.
X'02'	HDC diagnostic error
X'03'	Data buffer diagnostic error
X'04'	Memory diagnostic error
X'05'	Reading the system area is abnormal
X'06'	Calibration abnormal

Note: The device responds to this command with the result of power-on diagnostic test.

- Error reporting conditions

(1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	0	0	1	0	0	0	0
DH	x	x	x	x	HD No. /LBA			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	HD No. /LBA
CH)	xx				
CL	xx				
SN	01H				
SC	01H				
ER	Diagnostic code				

(10) INITIALIZE DEVICE PARAMETERS (X'91')

The host system can set the number of sectors per track and the maximum head number (maximum head number is "number of heads minus 1") per cylinder with this command. Upon receipt of this command, the device sets the parameters. Then the device reports the status to the host system.

When the SC field is specified to X'00', an ABORTED COMMAND error is posted. Other than X'00' is specified, this command terminates normally.

The parameters set by this command are retained even after soft reset issuance or power save operation regardless of the setting of disabling the reverting to default setting, however, the COMRESET is not retained.

The operation is always performed in CHS mode, with the command ignoring any setting of LBA mode.

- Error reporting conditions

  (1) "00h" is specified in the SC field (ST = 51h, ER = 04h).

  (2) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	0	0	1	0	0	0	1
DH	x	x	x	x	Max. head No.			
CH	xx							
CL	xx							
SN	xx							
SC	Number of sectors/track							
FR	xx							

At command completion (Shadow Block Registers contents to be read)								
ST	Status information							
DH	x	x	x	x	Max. head No.			
CH	xx							
CL	xx							
SN	xx							
SC	Number of sectors/track							
ER	Error information							

(11) DOWNLOAD MICROCODE (X'92')

At command issuance (Shadow Block Registers setting contents)								
CM	1	0	0	1	0	0	1	0
DH	1	x	1	x	0	0	0	0
CH	00							
CL	00							
SN	Sector count (15-8)							
SC	Sector count (7-0)							
FR	Subcommand code							

At command completion (Shadow Block Registers contents to be read)								
ST	Status information							
DH	1	x	1	x	0	0	0	0
CH	00							
CL	00							
SN	xx							
SC	xx							
ER	Error information							

This command rewrites the microcode of the device (firmware).

When this command is accepted, the device does beginning the data transfer of the microcode or the microcode rewriting according to Subcommand code (Rewriting is also possible simultaneously with the data transfer). Refer to Table 5.7.

In the data transfer of Subcommand code:01h, transfer by which data is divided into multiple times is possible. Refer to Table 5.8.

After the designation of rewriting by Subcommand code:07h, reactivates in the device for the update of the rewriting microcode of the microcode.

Table 5.7 Operation of DOWNLOAD MICROCODE

Host Command		Movement of device	
Subcommand code (FR Field)	Sector count (SN, SC Field)	Data transfer	Microcode rewriting execution
01h	0000h	Non	Rewriting execution reservation
	xxxxh	It is.	Rewriting execution reservation
07h	0000h	Non	Execution. **
	xxxxh	It is.	Execution. **
Excluding 01h and 07h	–	Abort	

**: In the following cases, Subcommand code=07h returns Abort as an error though becomes Microcode rewriting execution specification.

1) Abnormality of the transmitted Microcode data is detected.

2) The data transfer is not done (The number of transfer: 0).

3) The DOWNLOAD MICROCODE command is not continuously issued when the transfer has been divided into multiple transfers.

Table 5.8 Example of rewriting procedure of data 384K Bytes (30000h Bytes) of microcode

Transfer example 1:	
1) CMD = 92h SN, SC = 0100h FR = 0lh	Transfer of 127 KB from the first
2) CMD = 92h SN, SC = 0100h FR = 0lh	Transfer from 128 to 255 KB
3) CMD = 92h SN, SC = 0100h FR = 0lh	Transfer from 256 to 383 KB
4) CMD = 92h SN, SC = 0000h FR = 07h	Firmware rewriting execution
Transfer example 2:	
1) CMD = 92h SN, SC = 0300h FR = 0lh	Transfer of 384 KB
2) CMD = 92h SN, SC = 0000h FR = 07h	Firmware rewriting execution
Transfer example 3:	
1) CMD = 92h SN, SC = 0300h FR = 07h	Transfer of 384 KB and Firmware rewriting execution
Transfer example 4:	
1) CMD = 92h SN, SC = 0100h FR = 0lh	Transfer of 127 KB from the first
2) CMD = 92h SN, SC = 0100h FR = 0lh	Transfer from 128 to 255 KB
3) CMD = 92h SN, SC = 0100h FR = 07h	Transfer from 256 to 383 KB and Firmware rewriting execution

The Aborted Command error is reported if any of the following conditions is satisfied: transferred microcode data is incorrect, firmware rewriting is specified before microcode data is transferred, or the DOWNLOAD MICROCODE command is not issued continuously when the transfer has been divided into multiple transfers.

- Error reporting conditions

(1) When the transferred Micro code data error occurs (ST = 51h, ER = 04h).

(2) When writing is specified though the data has not transferred yet. (ST = 51h, ER = 04h).

(3) When the SATA frame error occurs. (ST = 51h, ER = 14h).

(4) When detect the error other than the above mentioned. (ST = 51h, ER = 04h).

(12) STANDBY IMMEDIATE (X'94' or X'E0')

Upon receipt of this command, the device enters the standby mode. The device then reports the status to the host system. This command does not support the APS timer function.

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)					
CM	X'94' or X'E0'				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
FR	xx				

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(13) IDLE IMMEDIATE (X'95' or X'E1')

Upon receipt of this command, the device enters the idle mode. Then, the device reports the status to the host system. This command does not support the APS timer function.

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)					
CM	X'95' or X'E1'				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
FR	xx				

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(14) STANDBY (X'96' or X'E2')

Upon receipt of this command, the device enters the standby mode. If the device has already spun down, the spin-down sequence is not implemented.

If the Sector Count field has a value other than "0," the APS timer is set when the command is received. In this event, the device enters the command waiting state, and the timer starts to count down. If a command is not received within the period specified as the APS timer value, the device automatically enters Standby mode. If the Sector Count field value is "0" the APS timer is disabled when the command is received.

Under the standby mode, the spindle motor is stopped. Thus, when the command involving a seek such as READ SECTOR(s) command is received, the device processes the command after driving the spindle motor.

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)					
CM	X'96' or X'E2'				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	Period of timer				
FR	xx				

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(15) IDLE (X'97' or X'E3')

Upon receipt of this command, the device enters the idle mode. The device report the status even if the device has not fully entered the idle mode. If the spindle of the device is already rotating, the spin-up sequence shall not be implemented.

By using this command, the APS (Automatic Power Standby) timer function is enabled and the timer immediately starts the countdown. When the timer reaches the specified value, the device enters standby mode. The APS timer is set to prohibition if the Sector Count field's value was "0" when device has received this command.

The period of timer count is set depending on the value of the Sector Count register as shown below.

Sector Count field value		Point of timer
0	[X'00']	Timeout disabled
1 to 240	[X'01' to X'F0']	(Value × 5) seconds
241 to 251	[X'F1' to X'FB']	((Value-240) × 30) min
252	[X'FC']	21 minutes
253	[X'FD']	8 hrs
254 to 255	[X'FE' to X'FF']	21 minutes 15 seconds

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)						
CM	X'97' or X'E3'					
DH	x	x	x	x	xx	
CH	xx					
CL	xx					
SN	xx					
SC	Period of timer					
FR	xx					

At command completion (Shadow Block Registers contents to be read)						
ST	Status information					
DH	x	x	x	x	xx	
CH	xx					
CL	xx					
SN	xx					
SC	xx					
ER	Error information					

(16) CHECK POWER MODE (X'98' or X'E5')

The host checks the power mode of the device with this command.

The host system can confirm the power save mode of the device by the contents of the Sector Count field after executing this command.

The device sets the following field value. After that, the device reports the status to the host system.

Power save mode	Sector Count field
• During moving to Standby mode • Standby mode	X'00'
• Idle mode	X'FF'
• Active mode	X'FF'

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)						
CM	X'98' or X'E5'					
DH	x	x	x	x	xx	
CH	xx					
CL	xx					
SN	xx					
SC	xx					
FR	xx					

At command completion (Shadow Block Registers contents to be read)						
ST	Status information					
DH	x	x	x	x	xx	
CH	xx					
CL	xx					
SN	xx					
SC	X'00' or X'FF'					
ER	Error information					

(17) SLEEP (X'99' or X'E6')

This command is the only way to make the device enter the sleep mode.

Upon receipt of this command, the device enters the sleep mode, then reports the status to the host system. The device report the status even if the device has not fully entered the sleep mode.

In the sleep mode, the spindle motor is stopped.

The only way to release the device from sleep mode is to execute a software or COMRESET.

- Error reporting conditions

(1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)					
CM	X'99' or X'E6'				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
FR	xx				

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(18) SMART (X'B0')

This command predicts the occurrence of device failures depending on the subcommand specified in the Features field. If the Features field contains values that are not supported with the command, the Aborted Command error is issued.

Before issuing the command, the host must set the key values in the Cylinder Low and Cylinder High field (4Fh in the Cylinder Low field and C2h in the Cylinder High field). If the key values are incorrect, the Aborted Command error is issued.

If the failure prediction function is disabled, the device returns the Aborted Command error to subcommands other than those of the SMART Enable Operations (with the Features field set to D8h).

If the failure prediction function is enabled, the device collects and updates data on specific items. The values of items whose data is collected and updated by the device in order to predict device failures are hereinafter referred to as attribute values.

Table 5.9 Features Field values (subcommands) and functions (1/3)

Features Field	Function
X'D0'	SMART READ DATE: A device that received this subcommand saves all the updated attribute values. The device then transfers 512-byte attribute value information to the host after transferring PIOSU. * For information about the format of the attribute value information, see Table 5.10.
X'D1'	SMART READ ATTRIBUTE THRESHOLDS: This subcommand is used to transfer 512-byte guarantee failure threshold value data to the host. * For information about the format of the guarantee failure threshold value data, see Table 5.11.
X'D2'	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE: Enables (by setting the Sector Count field to a value other than 00h) or disables (by setting the Sector Count field to 00h) a function that automatically saves device attribute values ("automatic attribute save function"). This setting is held regardless of whether the device is turned on or off. If the automatic attribute save function is enabled and more than 15 minutes has elapsed since the last time that attributes were saved, then the attributes are saved. However, if the automatic attribute save function is disabled, the attributes are not saved. Upon receiving this subcommand, a device enables or disables the automatic attribute save function, and transfers the RegDH, then reports the status.
X'D3'	SMART SAVE ATTRIBUTE VALUES: When the device receives this subcommand, if saves device attribute value data, and transfers the RegDH, then reports the status.
X'D4'	SMART EXECUTIVE OFF-LINE IMMEDIATE: A device which receives this command starts collecting the off-line data specified in the Sector Number field, or stops. In the off-line mode, after transferring the RegDH, off-line data are collected. In the captive mode, it collects off-line data then transfers the RegDH when collection of data is completed. SN Off-line data collection mode 00h: Off-line diagnosis (off-line mode) 01h: Simple self-test (off-line mode) 02h: Comprehensive self-test (off-line mode) 03h: Conveyance self-test (off-line mode) 04h: Selective self-test (off-line mode) 7Fh: Self-test stop 81h: Simple self-test (captive mode) 82h: Comprehensive self-test (captive mode) 83h: Conveyance self-test (captive mode) 84h: Selective self-test (captive mode)

Table 5.9 Features Field values (subcommands) and functions (2/3)

<table>
<tr><th>Features Field</th><th>Function</th></tr>
<tr><td>X’D5’</td><td>SMART READ LOG:
A device which receives this sub-command reads the log sector specified in the Sector Number Field. Next, it transfers the PIOSU and transmits the log sector to the host computer.

<table>
<tr><th>SN:</th><th>SC:</th><th>Log sector</th></tr>
<tr><td>00h:</td><td>01h:</td><td>SMART log directory</td></tr>
<tr><td>01h:</td><td>01h:</td><td>SMART summary error log</td></tr>
<tr><td>02h:</td><td>33h:</td><td>SMART comprehensive error log</td></tr>
<tr><td>06h:</td><td>01h:</td><td>SMART self-test log</td></tr>
<tr><td>09h:</td><td>01h:</td><td>SMART selective self-test log</td></tr>
<tr><td>80h-9Fh:</td><td>01h-10h:</td><td>Host vendor log</td></tr>
</table>
* See Table 5.18 concerning the SMART error log data format.
See Table 5.20 concerning the SMART self-test log data format.
See Table 5.21 concerning the SMART selective self-test log data format.</td></tr>
<tr><td>X’D6’</td><td>SMART WRITE LOG:
A device which receives this sub-command, when it has prepared to receive data from the host computer, it transfers the PIOSU. Next, it receives data from the host computer and writes the specified log sector in the Sector Number Field.

<table>
<tr><th>SN:</th><th>SC:</th><th>Log sector</th></tr>
<tr><td>09h:</td><td>01h:</td><td>SMART selective self-test log</td></tr>
<tr><td>80h-9Fh:</td><td>01h-10h</td><td>Host vendor log</td></tr>
</table>
* The host can write any desired data in the host vendor log.</td></tr>
<tr><td>X’D8’</td><td>SMART ENABLE OPERATIONS:
This subcommand enables SMART. The setting is maintained even when the device is turned off and then on.
When the device receives this subcommand, it enables SMART, then transfers the RegDH.</td></tr>
<tr><td>X’D9’</td><td>SMART DISABLE OPERATIONS:
This subcommand disables SMART. The setting is maintained even when the device is turned off and then on.
When the device receives this subcommand, it disables SMART, then transfers the RegDH..</td></tr>
</table>

Table 5.9 Features Field values (subcommands) and functions (3/3)

Features Field	Function
X'DA'	SMART RETURN STATUS: When the device receives this subcommand, it saves the current device attribute values. Then the device compares the device attribute values with guarantee failure threshold values. If there is an attribute value exceeding the threshold, F4h and 2Ch are loaded into the Cylinder Low and Cylinder High field. If there are no attribute values exceeding the thresholds, 4Fh and C2h are loaded into the Cylinder Low and Cylinder High field. After the settings for the Cylinder Low and Cylinder High field have been determined, the device transfers the RegDH.
X'DB'	SMART ENABLE/DISABLE AUTO OFF-LINE: This sets automatic off-line data collection in the enabled (when the Sector Count field specification ≠ 00h) or disabled (when the Sector Count field specification = 00) state. This setting is preserved whether the drive's power is switched on or off. If 24 hours have passed since the power was switched on, or since the last time that off-line data were collected, off-line data collection is performed without relation to any command from the host computer.

The host must regularly issue the SMART READ DATA subcommand (Features field = D0h), SMART SAVE ATTRIBUTE VALUES subcommand (Features field = D3h), or SMART RETURN STATUS subcommand (Features field = DAh) to save the device attribute value data on a medium.

Alternative, the device must issue the SMART ENABLE-DISABLE ATTRIBUTE AUTOSAVE subcommand (Features field = D2h) to use a feature which regularly save the device attribute value data to a medium.

The host can predict failures in the device by periodically issuing the SMART RETURN STATUS subcommand (Features field = DAh) to reference the Cylinder Low and Cylinder High field.

If an attribute value is below the guarantee failure threshold value, the device is about to fail or the device is nearing the end of its life. In this case, the host recommends that the user quickly backs up the data.

At command issuance (Shadow Block Registers setting contents)								
CM	1	0	1	1	0	0	0	0
DH	x	x	x	x	xx			
CH	Key (C2h)							
CL	Key (4Fh)							
SN	xx							
SC	xx							
FR	Subcommand							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	Key-failure prediction status (C2h/2Ch)				
CL	Key-failure prediction status (4Fh/F4h)				
SN	xx				
SC	xx				
ER	Error information				

The attribute value information is 512-byte data; the format of this data is shown the following Table 5.10. The host can access this data using the SMART READ DATE subcommand (Features field = D0h). The guarantee failure threshold value data is 512-byte data; the format of this data is shown the following Table 5.11. The host can access this data using the SMART READ ATTRIBUTE THRESHOLDS subcommand (Features field = D1h).

Table 5.10 Format of device attribute value data

Byte	Item	
00 01	Data format version number	
02	Attribute 1	Attribute ID
03 04		Status flag
05		Current attribute value
06		Attribute value for worst case so far
07 to 0C		Raw attribute value
0D		Reserved
0E to 169	Attribute 2 to attribute 30	(The format of each attribute value is the same as that of bytes 02 to 0D.)
16A	Off-line data collection status	
16B	Self-test execution status	
16C, 16D	Off-line data collection execution time [sec.]	
16E	Reserved	
16F	Off-line data collection capability	
170, 171	Trouble prediction capability flag	
172	Error logging capability	
173	(Self-test error detection point)	
174	Simple self-test (Quick Test) execution time [min.]	
175	Comprehensive self-test (Comprehensive Test) execution time [min.]	
176	Conveyance self-test execution time [min.]	
177 to 181	Reserved	
182 to 1FE	Vendor unique	
1FF	Check sum	

Table 5.11 Format of guarantee failure threshold value data

Byte	Item	
00 01	Data format version number	
02	Threshold 1	Attribute ID
03		Guarantee failure threshold
04 to 0D		Reserved
0E to 169	Threshold 2 to Threshold 30	(The format of each threshold value is the same as that of bytes 02 to 0D.)
16A to 17B	Reserved	
17C to 1FE	Vendor unique	
1FF	Check sum	

- Data format version number

  The data format version number indicates the version number of the data format of the device attribute values or guarantee failure thresholds. The data format version numbers of the device attribute values and guarantee failure thresholds are the same. When a data format is changed, the data format version numbers are updated.

- Attribute ID

  The attribute ID is defined as follows:

Attribute ID	Attribute name
0	(Indicates unused attribute data.)
1	Read Error Rate
2	Throughput Performance
3	Spin Up Time
4	Start/Stop Count
5	Reallocated Sector Count
7	Seek Error Rate
8	Seek Time Performance
9	Power-On Hours Count
10	Spin Retry Count
12	Drive Power Cycle Count
192	Emergency Retract Cycle Count
193	Load/Unload Cycle Count
194	HDA Temperature
195	ECC On the Fly Count
196	Reallocated Event Count
197	Current Pending Sector Count
198	Off-Line Scan Uncorrectable Sector Count
(199)	(Ultra ATA CRC Error Count)
200	Write Error Rate
203	Run Out
240	Communication Error Rate

- Status Flag

Bit	Meaning
0	If this bit is 1, it indicates normal operations are assured with the attribute when the attribute value exceeds the threshold value.
1	If this bit is 1 (0), it indicates the attribute only updated by an on-line test (off-line test).
2	If this bit 1, it indicates the attribute that represents performance.
3	If this bit 1, it indicates the attribute that represents an error rate.
4	If this bit 1, it indicates the attribute that represents the number of occurrences.
5	If this bit 1, it indicates the attribute that can be collected/saved even if SMART is disabled.
6 to 15	Reserve bit

- Current attribute value

  It indicates the normalized value of the original attribute value. The value deviates in a range of 01h to 64h (range of 01h to C8h for the Ultra ATA CRC error rate and communication error rate). It indicates that the closer the value is to 01h, the higher the possibility of a failure. The host compares the attribute value with the threshold value. If the attribute value is larger than the threshold value, the drive is determined to be normal.

- Attribute value for the worst case so far

  This is the worst attribute value among the attribute values collected to date. This value indicates the state nearest to a failure so far.

- Raw attribute value

  Raw attributes data is retained.

- Off-line data collection status

Table 5.12 Off-line data collection status

Status Byte	Meaning
00h or 80h	Off-line data collection is not executed.
02h or 82h	Off-line data collection has ended without an error.
04h or 84h	Off-line data collection is interrupted by a command from the host.
05h or 85h	Off-line data collection has ended before completion because of a command from the host.
06h or 86h	Off-line data collection has ended before completion because of an error that makes collection impossible. (Not used)
40 to 7Fh C0h to FFh	Vendor unique (Not used)
01h or 81h 03h or 83h 07h or 3Fh 87h to BFh	Reserved

- Self-test execution status

Table 5.13 Self-test execution status

Bit	Meaning
0 to 3:	Remainder of the self-test is indicated as a percentage in a range of "0h to 9h" (corresponding to 0 to 90 %).
4 to 7:	Self-test execution status
= 0h:	Self-test has ended successfully, or self-test has not been executed.
= 1h:	Self-test is suspended by the host.
= 2h:	Self-test is interrupted by a soft/COMRESET from the host.
= 3h:	Self-test cannot be executed.
= 4h:	Self-test has ended with an abnormality because of unknown contents.
= 5h:	Self-test has ended with "Write/Read Test" error.
= 6h:	Self-test has ended with "Servo Check," error.
= 7h:	Self-test has ended with "SMART Drive Error Log Check," "Random Read Test," or "Read Scan Test" error.
= 8h:	Self-test has ended with "Pre-SMART Check," or "Post-SMART Check" error.
= 9h to Eh:	Reserved
= Fh:	Self-test is in progress.

- Off-line data collection capability

  Indicates the method of off-line data collection carried out by the drive. If the off-line data collection capability is 0, it indicates that off-line data collection is not supported.

Table 5.14 Off-line data collection capability

Bit	Meaning
0	If this bit is 1, it indicates that the SMART EXECUTE OFF-LINE IMMEDATE sub-command (Features field = D4h) is supported.
1	Vendor unique
2	If this bit is 1, it indicates that offline data collection under execution is aborted when a new command is received.
3	If this bit is 1, it indicates that the SMART Off-line Read Scanning Technology is supported.
4	If this bit is 1, it indicates that the SMART Self-test function is supported.
5	If this bit is 1, it indicates that the SMART Conveyance Self-test is supported.
6	If this bit is 1, it indicates that the SMART Selective Self-test is supported.
7	Reserved bits

- Failure prediction capability flag

Table 5.15 Failure prediction capability flag

Bit	Meaning
0	If this bit is 1, it indicates that the attribute value is saved on media before the drive enters the power save mode.
1	If this bit is 1, it indicates that the attribute value is saved automatically after the pre-set operation of the drive.
2 to 15	Reserved bits

- Error logging capability

Table 5.16 Drive error logging capability

Bit	Meaning
0	If this bit is 1, it indicates that the drive error logging function is supported.
1 to 7	Reserved bits

- Checksum

  Two's complement of the lower byte, obtained by adding 511-byte data one byte at a time from the beginning.

- Guarantee failure threshold

  The limit of a varying attribute value. The host compares the attribute values with the thresholds to identify a failure.

Table 5.17 Log Directory Data Format

<table>
<tr><th>Byte</th><th colspan="2">Item</th></tr>
<tr><td>00
01</td><td colspan="2">SMART Logging Version</td></tr>
<tr><td>02</td><td colspan="2">Number of sectors of Address "01h"</td></tr>
<tr><td>03</td><td colspan="2">Reserved</td></tr>
<tr><td>04</td><td colspan="2">Number of sectors of Address "02h"</td></tr>
<tr><td>05 to 0B</td><td colspan="2">Reserved</td></tr>
<tr><td>0C</td><td colspan="2">Number of sectors of Address "06h"</td></tr>
<tr><td>0D to 11</td><td colspan="2">Reserved</td></tr>
<tr><td>12</td><td colspan="2">Number of sectors of Address "09h"</td></tr>
<tr><td>13 to FF</td><td colspan="2">Reserved</td></tr>
<tr><td>100</td><td rowspan="2">Address 80h</td><td>Number of sector</td></tr>
<tr><td>101</td><td>Reserved</td></tr>
<tr><td>102 to 13F</td><td>Address 81h
to
Address 9Fh</td><td>"102" and "13F" are both the same format as "100-101"</td></tr>
<tr><td>140 to 1FF</td><td colspan="2">Reserved</td></tr>
</table>

- SMART error logging

  If the device detects an unrecoverable error during execution of a command received from the host, the device registers the error information in the SMART Summary Error Log (see Table 5.18) and the SMART Comprehensive Error Log (see Table 5.19), and saves the information on media.

  The host issues the SMART Read Log Sector sub-command (Features field = D5h, Sector Number field = 01h, Sector Count field = 01h) and can read the SMART Summary Error Log.

  The host issues the SMART Read Log Sector sub-command (Features field = D5h, Sector Number field = 02h, Sector Count field = 33h) and can read the SMART Comprehensive Error Log.

Table 5.18 Data format of SMART Summary Error Log (1/2)

Byte	Item		
00	Version of this function		
01	Pointer for the latest “Error Log Data Structure”		
02 to 0D	Error log data structure	Forth last command data structure	
0E to 19		Third last command data structure	
1A to 25		Second last command data structure	
26 to 31		Last command data structure	
32		Command data structure	Device Control field value
33			Features field value
34			Sector Count field value
35			Sector Number field value
36			Cylinder Low field value
37			Cylinder High field value
38			Drive/Head field value
39			Command field value
3A to 3D			Elapsed time after the power-on sequence (unit: ms)
3E		Error data structure	Reserved
3F			Error field value
40			Sector Count field value
41			Sector Number field value
42			Cylinder Low field value
43			Cylinder High field value
44			Drive/Head field value
45			Status field value
46 to 58			Vendor unique
59			State
5A, 5B			Power-on time (unit: h)

Table 5.18 Data format of SMART Summary Error Log (2/2)

Byte	Item
5C to 1C3	Error log data structure 2 to Error log data structure 5
1C4, 1C5	Total number of drive errors
1C6 to 1FE	Reserved
1FF	Check sum

- Command data structure

  Indicates the command received when an error occurs.

- Error data structure

  Indicates the status register when an error occurs.

- Total number of drive errors

  Indicates total number of errors registered in the error log.

- Checksum

  Two's complement of the lower byte, obtained by adding 511-byte data one byte at a time from the beginning.

- Status

  Bits 0 to 3: Indicates the drive status when received error commands according to the following table.

  Bits 4 to 7: Vendor unique

Status	Meaning
0	Unclear status
1	Sleep status
2	Standby status
3	Active status (BSY bit = 0)
4	Off-line data collection being executed
5 to F	Reserved

Table 5.19 Data format of SMART Comprehensive Error Log

Byte	First sector	Next sector
00	SMART Error Logging 01h	Reserved
01	Index Pointer Latest Error Data Structure	Reserved
02…5B	1st Error Log Data Structure	Error Log Data Structure 5n+1
5C…B5	2nd Error Log Data Structure2	Error Log Data Structure 5n+2
B6…10F	3rd Error Log Data Structure3	Error Log Data Structure 5n+3
110…169	4th Error Log Data Structure4	Error Log Data Structure 5n+4
16A…1C3	5thError Log Data Structure5	Error Log Data Structure 5n+5
1C4…1C5	Total number of drive errors	Reserved
1C6…1FE	Reserved	Reserved
1FF	Check sum	Check sum
“n” indicates sector number in the Error Log. The first sector is 0.		

- SMART Self-Test

  The host computer can issue the SMART Execute Off-line Immediate sub-command (Features field = D4h) and cause the device to execute a self-test. When the self-test is completed, the device saves the SMART self-test log to the disk medium.

  The host computer can issue the SMART Read Log Sector sub-command (Features field = D5h, Sector Number field = 06h, Sector Count field = 01h) and can read the SMART self-test log.

Table 5.20 SMART self-test log data format

Byte	Item	
00, 01	Self-test log data structure	
02	Self-test log 1	Self-test number (Sector Number field Value)
03		Self-test execution status
04, 05		Life time. Total power-on time [hours]
06		Self-test error No.
07 to 0A		Error LBA
0B to 19		Vendor unique
1A to 1F9	Self-test log 2 to 21	(Each log data format is the same as that in byte 02 to 19.)
1FA, 1FB	Vendor unique	
1FC	Self-test index	
1FD, 1FE	Reserved	
1FF	Check sum	

- Self-test number

  Indicates the type of self-test executed.

- Self-test execution status

  Same as byte 16Bh of the attribute value.

- Self-test index

  If this is "00h", it indicates the status where the self-test has never been executed.

- Checksum

  Two's complement of the lower byte, obtained by adding 511-byte data one byte at a time from the beginning.

Table 5.21 Selective self-test log data structure

Byte	Item	
00h, 01h	Data Structure Revision Number	
02h...09h	Test Span 1	Starting LBA
0Ah...11h		Ending LBA
12h...19h	Test Span 2	Starting LBA
1Ah...21h		Ending LBA
22h...29h	Test Span 3	Starting LBA
2Ah...31h		Ending LBA
32h...39h	Test Span 4	Starting LBA
3Ah...41h		Ending LBA
42h...49h	Test Span 5	Starting LBA
4Ah...51h		Ending LBA
52h...151h	Reserved	
152h...1EBh	Vender Unique	
1Ech...1F3h	Current LBA under test	
1F4h...1F5h	Current Span under test	
1F6h...1F7h	Feature Flags	
1F8h	Vender Unique	Offline Execution Flag
1F9h		Selective Offline Scan Number
1FAh, 1FBh		Reserved
1FCh, 1FDh	Selective Self-test pending time [min]	
1FEh, 1FFh	Checksum	

- Test Span

  Selective self-test log provides for the definition of up to five test spans. If the starting and ending LBA values for a test span are both zero, a test span is not defined and not tested.

- Current LBA under test

  As the self-test progress, the device shall modify this value to contain the LBA currently being tested.

- Current Span under test

  As the self-test progress, the device shall modify this value to contain the test span number currently being tested.

- Feature Flags

Table 5.22 Selective self-test feature flags

Bit	Description
0	Vendor specific (unused)
1	When set to one, perform off-line scan after selective test
2	Vendor specific (unused)
3	When set to one, off-line scan after selective test is pending.
4	When set to one, off-line scan after selective test is active.
5...15	Reserved

Bit [l] shall be written by the host and returned unmodified by the device. Bit [3:4] shall be written as zeros by the host and the device shall modify them as the test progress.

- Selective Self-test pending time [min]

  The selective self-test pending time is the time in minutes from power-on to the resumption of the off-line testing if the pending bit is set.

(19) DEVICE CONFIGURATION (X'B1')

Individual Device Configuration Overlay feature sub commands are identified by the value placed in the Features field. The following table shows these Features field values. If this command sets with the reserved value of Features field, an aborted command error is posted.

FR field	Command
C0h	DEVICE CONFIGURATION RESTORE
C1h	DEVICE CONFIGURATION FREEZE
C2h	DEVICE CONFIGURATION IDENTIFY
C3h	DEVICE CONFIGURATION SET
00h-BFh, C4h-FFh	Reserved

At command issuance (Shadow Block Registers setting contents)								
CM	1	0	1	1	0	0	0	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	C0h/C1h/C2h/C3h							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

- DEVICE CONFIGURATION RESTORE (Features Field = C0h)

  The DEVICE CONFIGURATION RESTORE command disables any setting previously made by a DEVICE CONFIGURATION SET command and returns the content of the IDENTIFY DEVICE command response to the original settings as indicated by the data returned from the execution of a DEVICE CONFIGURATION IDENTIFY command. After execution of this command, the settings are kept regardless of the power-on or COMRESET execution.

- Error reporting conditions

  (1) The device is in the Device Configuration Freeze Lock state (ST = 51h, ER = 04h).

  (2) The command was received before the DEVICE CONFIGURATION SET command was issued (ST = 51h, ER = 04h).

  (3) The SET MAX ADDRESS (EXT) command (F9h, 37h) has been specified with a value in the Host Protected Area (ST = 51h, ER = 04h).

  (4) A SATA communication error occurred (ST = 51h, ER = 14h).

- DEVICE CONFIGURATION FREEZE LOCK (Features Field = C1h)

  The DEVICE CONFIGURATION FREEZE LOCK command prevents accidental modification of the Device Configuration Overlay settings. After successful execution of a DEVICE CONFIGURATION FREEZE LOCK command, all DEVICE CONFIGURATION SET, DEVICE CONFIGURATION FREEZE LOCK, DEVICE CONFIGURATION IDENTIFY, and DEVICE CONFIGURATION RESTORE commands are aborted by the device. The DEVICE CONFIGURATION FREEZE LOCK condition is cleared by a power-down, not cleared by a COMRESET or software reset.

- Error reporting conditions

  (1) The device is in the Device Configuration Freeze Lock state (ST = 51h, ER = 04h).

  (2) The command was received before the DEVICE CONFIGURATION SET command was issued (ST = 51h, ER = 04h).

  (3) A SATA communication error occurred (ST = 51h, ER = 14h).

- DEVICE CONFIGURATION IDENTIFY (Features Field = C2h)

  The DEVICE CONFIGURATION IDENTIFY command returns information shown in Table 5.23. The content of this data structure indicates the selectable commands, modes, and feature sets that the device is capable of supporting. If a DEVICE CONFIGURATION SET command has been issued reducing the capabilities, the response to an IDENTIFY DEVICE command will reflect the reduced set of capabilities, however, the DEVICE CONFIGURATION IDENTIFY command will not be changed.

- Error reporting conditions

  (1) The device is in the Device Configuration Freeze Lock state (ST = 51h, ER = 04h).

  (2) A SATA communication error occurred (ST = 51h, ER = 14h).

- DEVICE CONFIGURATION SET (Features Field = C3h)

  The DEVICE CONFIGURATION SET command allows to reduce the set of optional commands, modes, or feature sets supported by a device as indicated by a DEVICE CONFIGURATION IDENTIFY command. The format of the overlay transmitted by the device is described in Table 5.23. As a result to the limitation of the function by the DEVICE CONFIGURATION SET command, is reflected in IDENTIFY information. When the bits in these words are cleared, the device no longer supports the indicated command, mode, or feature set. If a bit is set in the overlay transmitted by the device that is not set in the overlay received from a DEVICE CONFIGURATION IDENTIFY command, no action is taken for that bit. After execution of this command, the settings are kept regardless of the power-on, COMRESET, or soft reset

  If the restriction of Multiword DMA modes or Ultra DMA modes is executed, a SET FEATURES command should be issued for the modes restriction prior the DEVICE CONFIGURATION SET command is issued. When the Automatic Acoustic Management function is assumed to be a unsupport, Automatic Acoustic Management is prohibited beforehand by SET FEATURES command (FR=C2h).

- Error reporting conditions

  (1) The device is in the Device Configuration Freeze Lock state (ST = 51h, ER = 04h).

  (2) The SET MAX ADDRESS (EXT) command (F9h, 37h) has been specified with a value in the Host Protected Area (ST = 51h, ER = 04h).

  (3) A SATA communication error occurred (ST = 51h, ER = 14h).

Table 5.23 DEVICE CONFIGURATION IDENTIFY data structure

Word	Value	Content
0	X'0001'	Data structure revision
1	X'0007'	Multiword DMA modes supported Reflected in IDENTIFY information "WORD63". Bit 15-3: Reserved Bit 2: 1 = Multiword DMA mode 2 and below are supported Bit 1: 1 = Multiword DMA mode 1 and below are supported Bit 0: 1 = Multiword DMA mode 0 is supported
2	X'003F'	Ultra DMA modes supported Reflected in IDENTIFY information "WORD88". Bit 15-6: Reserved Bit 5: 1 = Ultra DMA mode 5 and below are supported Bit 4: 1 = Ultra DMA mode 4 and below are supported Bit 3: 1 = Ultra DMA mode 3 and below are supported Bit 2: 1 = Ultra DMA mode 2 and below are supported Bit 1: 1 = Ultra DMA mode 1 and below are supported Bit 0: 1 = Ultra DMA mode 0 is supported
3 to 6	-	Maximum LBA address Reflected in IDENTIFY information "WORD60-61". (WORD100-103) *
7	X'00CF' (X'01CF') *	Command set/feature set supported Reflected in IDENTIFY information "WORD82-87". Bit 15-9: Reserved Bit 8: 1 = 48-bit Addressing feature set supported Bit 7: 1 = Host Protected Area feature set supported Bit 6: 1 = Automatic acoustic management supported Bit 5: 1 = READ/WRITE DMA QUEUED commands supported Bit 4: 1 = Power-up in Standby feature set supported Bit 3: 1 = Security feature set supported Bit 2: 1 = SMART error log supported Bit 1: 1 = SMART self-test supported Bit 0: 1 = SMART feature set supported
8	X ' 0005 '	Serial-ATA command set/function → Reflected in IDENTIFY information ”Word 76 to 79. Bit15-4: Reserved Bit3: 1 = Asynchronous Notification supported Bit2: 1 = Interface power management supported Bit1: 1 = Non-zero buffer offsets in DMA Setup FIS supported Bit0: 1 = Native command queuing supported
9	X ' 0000 '	Reserved for Serial-ATA
10 to 254	X'0000'	Reserved
255	X'xxA5'	Bit 15-8: Check sum code (This is obtained by calculating the sum of all upper bytes and lower bytes in WORD 0 to 256 and the byte consisting of bits 7 to 0 in WORD 255, and then calculating the two's complement of the lowest byte of that sum.) Bit 7 - 0:

(20) READ MULTIPLE (X'C4')

The READ MULTIPLE command performs the same tasks as the READ SECTOR(S) command except that this command sends the PIO Setup FIS before sending data blocks of multiple sectors. The PIO Setup FIS is sent only before the first data block is transferred, and it is not sent before any subsequent transfer of sector blocks.

The number of sectors per block is defined by a successful SET MULTIPLE MODE Command. The SET MULTIPLE MODE command should be executed prior to the READ MULTIPLE command.

If the number of requested sectors is not divided evenly (having the same number of sectors [block count]), as many full blocks as possible are transferred, then a final partial block is transferred. The number of sectors in the partial block to be transferred is n where n = remainder of ("number of sectors"/"block count").

If the READ MULTIPLE command is issued when the READ MULTIPLE command is disabled, the device rejects the READ MULTIPLE command with an ABORTED COMMAND error.

If an uncorrectable disk read error occurs, the read operation stops at the sector where the error occurred (even if the read operation has not reached the end of the block). At this time, the number of sectors that have not been transferred (including the error sector), and either the cylinder, head, and sector addresses of the error sector (CHS mode) or the logical block address of the error sector (LBA mode) are set in the Shadow Block Register.

Figure 5.2 shows an example of the execution of the READ MULTIPLE command.

- Block count specified by SET MULTIPLE MODE command = 4 (number of sectors in a block)
- READ MULTIPLE command specifies;
  Number of requested sectors = 9 (Sector Count register = 9)

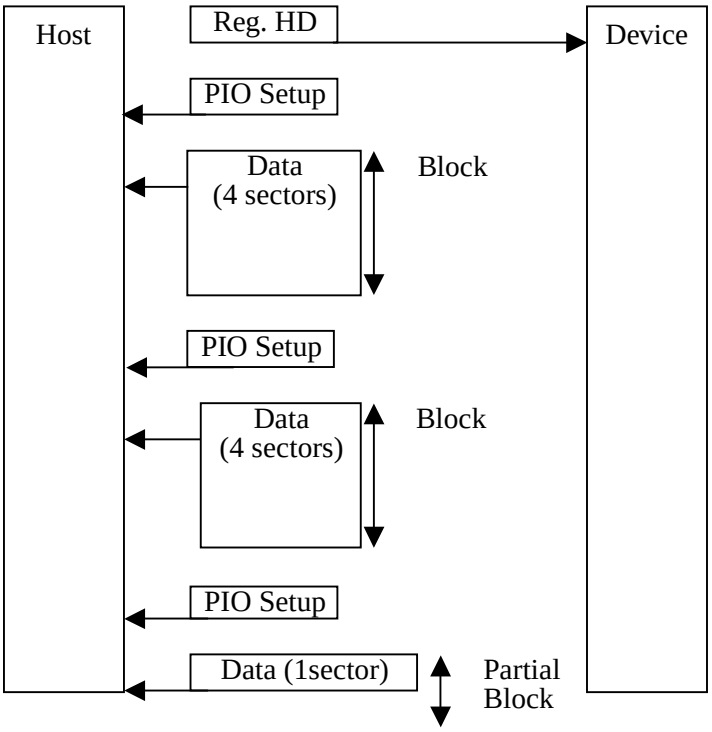


Figure 5.9 Execution example of READ MULTIPLE command

- Error reporting conditions

  (1) A specified address exceeds the range where read operations are allowed (ST = 51h, ER = 10h).

  (2) The range where read operations are allowed will be exceeded by an address during a read operation (ST = 51h, ER = 10h).

  (3) An uncorrectable disk read error occurred (ST = 51h, ER = 40h).

  (4) The sync byte indicating the beginning of a sector was not found (ST = 51h, ER = 01h).

  (5) The READ MULTIPLE command is disabled (ST = 51h, ER = 04h).

  (6) A SATA communication error occurred (ST = 51h, ER = 0Ch).

  (7) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	0	0	0	1	0	0
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	Transfer sector count							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	L	x	x	HD No. / LBA
CH	End cylinder No. [MSB] / LBA				
CL	End cylinder No. [LSB] / LBA				
SN	End sector No. / LBA [LSB]				
SC	(*1)				
ER	Error information				

*1 If the command is completed normally, the number of remaining sectors is set in this field.
If the command is terminated because of an error, the number of sectors for which data has not been transferred is set in the field.

(21) WRITE MULTIPLE (X'C5')

The WRITE MULTIPLE command performs the same tasks as the WRITE SECTOR(S) command except that this command sends the PIO Setup FIS before sending data blocks of multiple sectors. The PIO Setup FIS is sent only before the first data block is transferred, and it is not sent before any subsequent transfer of sector blocks.

The number of sectors per block is defined by a successful SET MULTIPLE MODE command. The SET MULTIPLE MODE command should be executed prior to the WRITE MULTIPLE command.

If the number of requested sectors is not divided evenly (having the same number of sectors [block count]), as many full blocks as possible are transferred, then a final partial block is transferred. The number of sectors in the partial block to be transferred is n where n = remainder of ("number of sectors"/"block count").

If the WRITE MULTIPLE command is issued before the SET MULTIPLE MODE command is executed or when WRITE MULTIPLE command is disabled, the device rejects the WRITE MULTIPLE command with an ABORTED COMMAND error.

A disk write error that occurs during execution of the WRITE MULTIPLE command will be reported after a disk write operation has been attempted for the transferred blocks and partial block. The write operation stops at the sector where the error occurred (even if the write operation has not reached the end of the block). At this time, the number of remaining sectors (the error sector and subsequent sectors) and either cylinder, head, and sector addresses of the error sector (CHS mode) or the logical block address of the error sector (LBA mode) are set in the Shadow Block Register.

- Error reporting conditions

  (1) A specified address exceeds the range where write operations are allowed (after a transfer of dummy data, ST = 51h, ER = 10h).

  (2) The range where write operations are allowed will be exceeded by an address during a write operation (after a transfer of dummy data, ST = 51h, ER = 10h).

  (3) A write fault was detected when the write cache was disabled (ST = 71h, ER = 10h).

  (4) While the write cache is enabled, if the status indicating a completed transfer (STS = 50h) is returned and a data write operation failed because a write fault was detected during the data write operation, Abort will be returned for all subsequent ATA commands (ST = 71h, ER = 04h). This state is cleared the next time that the device is turned on.

  (5) The WRITE MULTIPLE command is disabled (ST = 51h, ER = 04h).

  (6) A SATA communication error occurred (ST = 51h, ER = 14h).

  (7) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	0	0	0	1	0	1
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	Transfer sector count							
FR	xx							

(R: Retry)

At command completion (Shadow Block Registers contents to be read)								
ST	Status information							
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	00 (*1)							
ER	Error information							

*1 If the command was terminated because of an error, the number of sectors for which data has not been written is set in this field.

(22) SET MULTIPLE MODE (X'C6')

This command enables the device to perform the READ MULTIPLE and WRITE MULTIPLE commands. The block count (number of sectors in a block) for these commands are also specified by the SET MULTIPLE MODE command.

The number of sectors per block is written into the Sector Count field. The IDD supports block sizes of 2, 4, 8, and 16 sectors.

Upon receipt of this command, the device checks the contents of the Sector Count field. If the contents of the Sector Count field is valid and is a supported block count, the value is stored for all subsequent READ MULTIPLE and WRITE MULTIPLE commands. Execution of these commands is then enabled. If the value of the Sector Count register is not a supported block count, an ABORTED COMMAND error is posted and the READ MULTIPLE and WRITE MULTIPLE commands are disabled.

If the contents of the Sector Count field is 0, when the SET MULTIPLE MODE command is issued, the READ MULTIPLE and WRITE MULTIPLE commands are disabled.

When the SET MULTIPLE MODE command operation is completed, the device reports the status to the host.

In the default mode that is entered at power-on, the READ MULTIPLE and WRITE MULTIPLE commands are enabled (block count = 10h).

- Error reporting conditions

  (1) A value other than 00h, 02h, 04h, 08h, or 10h is specified in the SC field (ST = 51h, ER = 04h).

  (2) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	0	0	0	1	1	0
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	Sector count/block							
FR	xx							

At command completion (Shadow Block Registers contents to be read)						
ST	Status information					
DH	x	x	x	x	xx	
CH	xx					
CL	xx					
SN	xx					
SC	Sector count/block					
ER	Error information					

(23) READ DMA (X'C8' or X'C9')

The READ DMA command reads data from sectors, starting from the sectors specified in the Device/Head, Cylinder High, Cylinder Low, and Sector Number fields and continuing for as many sectors as specified in the Sector Count field. A value ranging from 1 to 256 can be specified for the number of sectors. In order to specify 256, "00" must be set in the Sector Count field. For the protocol concerning data transfers, see Section 5.4.4.

When the command is completed, either cylinder, head, and sector addresses (CHS mode) or the logical block address (LBA mode) of the last sector is stored in the Shadow Block Register.

If an error such as an uncorrectable disk read error is detected during execution of the READ DMA command and continued operation not possible, the data transfer stops after all data, including the data of the sector where the error was detected, is transferred. The device notifies the host of the status by sending the Register DH FIS. At this time, the number of remaining sectors including the sector where the error was detected, and either cylinder, head, and sector addresses (CHS mode) or the logical block address (LBA mode) of the sector where the error was detected are stored in the Shadow Block Register.

The host system can select the DMA transfer mode by using the SET FEATURES command, however, the transfer speed does not change.

- Multiword DMA transfer mode 0 to 2
- Ultra DMA transfer mode 0 to 5

- Error reporting conditions

  (1) A specified address exceeds the range where read operations are allowed (ST = 51h, ER = 10h).

  (2) The range where read operations are allowed will be exceeded by an address during a read operation (ST = 51h, ER = 10h).

  (3) An uncorrectable disk read error occurred (ST = 51h, ER = 40h).

  (4) The sync byte indicating the beginning of a sector was not found (ST = 51h, ER = 01h).

  (5) A SATA communication error occurred (ST = 51h, ER = 0Ch).

  (6) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	0	0	1	0	0	R
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	Transfer sector count							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	L	x	x	HD No. / LBA
CH	Start cylinder No. [MSB] / LBA				
CL	Start cylinder No. [LSB] / LBA				
SN	Start sector No. / LBA [LSB]				
SC	00 (*1)				
ER	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors of which data was not transferred is set in this register.

(24) WRITE DMA (X'CA' or X'CB')

The WRITE DMA command writes data to sectors starting from the sectors specified in the Device/Head, Cylinder High, Cylinder Low, and Sector Number fields and continuing for as many sectors as specified in the Sector Count field. A value ranging from 1 to 256 can be specified for the number of the sectors. In order to specify 256, "00" must be set in the Sector Count field. For the protocol concerning data transfers, see Section 5.4.5.

When the command is completed, cylinder, head, and sector addresses (CHS mode) of the last sector to which data was written is stored in the Shadow Block Register.

If a disk write error is detected during execution of the WRITE DMA command and continued operation is not possible, command processing is terminated after all data, including the data of the sector where the error was detected, is transferred. The device notifies the host of the status by sending the Register DH FIS. At this time, the number of remaining sectors including the sector where the error was detected, and either cylinder, head, and sector addresses (CHS mode) or the logical block address (LBA mode) of the sector where the error was detected are stored in the Shadow Block Register.

A host system can select the following transfer mode using the SET FEATURES command, however, the transfer speed does not change.

- Multiword DMA transfer mode 0 to 2
- Ultra DMA transfer mode 0 to 5

- Error reporting conditions

  (1) A specified address exceeds the range where write operations are allowed (after a transfer of dummy data, ST = 51h, ER = 10h).

  (2) The range where write operations are allowed will be exceeded by an address during a write operation (after a transfer of dummy data, ST = 51h, ER = 10h).

  (3) A write fault was detected when the write cache was disabled (ST = 71h, ER = 10h).

  (4) While the write cache is enabled, if the status indicating a completed transfer (STS = 50h) is returned and a data write operation failed because a write fault was detected during the data write operation, Abort will be returned for all subsequent ATA commands (ST = 71h, ER = 04h). This state is cleared the next time that the device is turned on.

  (5) A SATA communication error occurred (ST = 51h, ER = 14h).

  (6) An error other than the above errors occurred (ST = 51h, ER = 04h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	0	0	1	0	1	R
DH	x	L	x	x	HD No. / LBA			
CH	Start cylinder No. [MSB] / LBA							
CL	Start cylinder No. [LSB] / LBA							
SN	Start sector No. / LBA [LSB]							
SC	Transfer sector count							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	L	x	x	HD No. / LBA
CH	Start cylinder No. [MSB] / LBA				
CL	Start cylinder No. [LSB] / LBA				
SN	Start sector No. / LBA [LSB]				
SC	00 (*1)				
ER	Error information				

*1 If the command was terminated because of an error, the number of sectors for which data has not been written is set in this field.

(25) READ BUFFER (X'E4')

The host system can read the current contents of the data buffer of the device by issuing this command.

Upon receipt of this command, the device transfers the PIO Setup. After that, the host system can read up to 512 bytes of data from the buffer.

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 0Ch).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	0	0	1	0	0
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(26) FLUSH CACHE (X'E7')

This command is used to write every write cache data stored by the device into the medium. When the device completes all the data writing, it reports the status to the host system. The device performs every error recovery so that the data are read correctly.

When executing this command, the writing of the data may take several seconds if much data are to be written.

In case a non-recoverable disk write error has occurred while the data is being read, the error generation address is put into the shadow block register before ending the command. This error sector is deleted from the write cache data.

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	0	0	1	1	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(27) WRITE BUFFER (X'E8')

The host system can overwrite the contents of the data buffer of the device with a desired data pattern by issuing this command. Upon receipt of this command, the device transfers the PIO Setup. After that, 512 bytes of data is transferred from the host and the device writes the data to the buffer, then reports the status .

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	0	1	0	0	0
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(28) IDENTIFY DEVICE (X'EC')

The host system issues the IDENTIFY DEVICE command to read parameter information from the device. When it receives the command, the device prepares the parameter information to be sent to the host. Next, the device sends the PIO Setup FIS to the host, then sends the parameter information including a 512-byte date. Table 5.24 shows the values of the parameter words and the meaning in the buffer.

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 0Ch).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	0	1	1	0	0
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(29) IDENTIFY DEVICE DMA (X'EE')

When this command is not used to transfer data to the host in DMA mode, this command functions in the same way as the Identify Device command.

- Error reporting conditions

(1) A SATA communication error occurred (ST = 51h, ER = 0Ch).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	0	1	1	1	0
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

t command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

Table 5.24 Information to be read by IDENTIFY DEVICE command (1/3)

Word	Value	Description
0	X'045A'	General Configuration *1
1	X'3FFF'	Number of Logical cylinders *2
2	X'C837'	Detailed Configuration *3
3	X'0010'	Number of Logical Heads *2
4-5	X'0000'	Undefined
6	X'003F'	Number of Logical sectors per Logical track *2
7-9	X'0000'	Undefined
10-19	Set by a device	Serial number (ASCII code, 20 characters, right)
20	X'0003'	Undefined
21	X'xxxx'	Buffer Size (1 LSB: 512 Bytes) ex. Buffer Size=8MBytes: X'4000'
22	X'0004'	Number of ECC bytes transferred at READ LONG or WRITE LONG command
23-26	–	Firmware revision (ASCII code, 8 characters, left)
27-46	Set by a device	Model name (ASCII code, 40 characters, left)
47	X'8010'	Maximum number of sectors per block on READ/WRITE MULTIPLE command
48	X'0000'	Reserved
49	X'2F00'	Capabilities *4
50	X'4000'	Capabilities *5
51	X'0200'	PIO data transfer mode *6
52	X'0200'	Reserved
53	X'0007'	Enable/disable setting of words 54-58 and 64-70, 88 *7
54	(Variable)	Number of current Cylinders
55	(Variable)	Number of current Head
56	(Variable)	Number of current sectors per track
57-58	(Variable)	Total number of current sectors
59	*8	Transfer sector count currently set by READ/WRITE MULTIPLE command *8
60-61	*2	Total number of user addressable sectors (LBA mode only) *2
62	X'0000'	Reserved
63	X'xx07'	Multiword DMA transfer mode *9
64	X'0003'	Advance PIO transfer mode support status *10

Table 5.24 Information to be read by IDENTIFY DEVICE command (2/3)

Word	Value	Description
65	X’0078’	Minimum multiword DMA transfer cycle time per word: 120 [ns]
66	X’0078’	Manufacturer’s recommended DMA transfer cycle time: 120 [ns]
67	X’00F0’	Minimum PIO transfer cycle time without IORDY flow control: 240 [ns]
68	X’0078’	Minimum PIO transfer cycle time with IORDY flow control: 120 [ns]
69-74	X’0000’	Reserved
75	X'001F'	Queue depth *11
76	X'0302'	Serial ATA capabilities *12
77	X'0000'	Reserved for Serial ATA
78	X'0004'	Support of Serial ATA function *13
79	X'0000'	Valid of Serial ATA function *14
80	X’00F8’	Major version number *11
81	X’001A’	Minor version number
82	X’346B’	Support of command sets *12
83	X’7F09’	Support of command sets *13
84	X’60xx’	Support of command sets/function *14
85	*15	Valid of command sets/function *15
86	*16	Valid of command sets/function *16
87	*17	Default of command sets/function *17
88	X’xx3F’	Ultra DMA transfer mode *18
89	Set by a device	Security Erase Unit execution time (1 LSB: 2 min.) *19
90	X’0000’	Enhanced Security Erase Unit execution time (1 LSB: 2 min.)
91	(Variable)	Advance power management level
92	(Variable)	Master password revision
93	X’0000’	COMRESET Result
94	(Variable)	Acoustic Management level *21
95-99	X’0000’	Reserved
100-103	X’xx’	Total number of sectors accessible by users in the 48-bit LBA mode *22
104-105	X’00’	Reserved
106	*26	Logical sector size per logical sector
107-116	X'0000'	Reserved

Table 5.24 Information to be read by IDENTIFY DEVICE command (3/3)

Word	Value	Description
117-118	X ' 0100 '	Number of words for logical sectors
119-127	X ' 0000 '	Reserved
128	X’0xxx’	Security status *23
129-159	X’xxxx’	Undefined
160-254	X’0000’	Reserved
255	X’xxA5’	Check sum (The 2 complement of the lower order byte resulting from summing bits 7 to 0 of word 0 to 254 and word 255, in byte units.)

*1 Word 0: General configuration

Bit 15: ATA device = 0, ATAPI device = 1

Bit 14-8: Undefined

Bit 7: Removable disk drive = 1

Bit 6: Fixed drive = 1

Bit 5-3: Undefined

Bit 2: IDENTIFY DEVICE Valid = 0

Bit 1-0: Reserved

*2 Word 1, 3, 6, 60-61

Word	MHT2080BH	MHT2060BH	MHT2040BH
1	X ' 3FFF '	X ' 3FFF '	X ' 3FFF '
3	X ' 10 '	X ' 10 '	X ' 10 '
6	X ' 3F '	X ' 3F '	X ' 3F '
60-61	X ' 950F8B0 '	X ' 6FC7C80 '	X '4A85300 '

*3 Status of the Word 2 Identify information is shown as follows:

37C8h The device requires the SET FEATURES sub-command after the power-on sequence in order to spin-up. The Identify information is incomplete.

738Ch The device requires the SET FEATURES sub-command after the power-on sequence in order to spin-up. The Identify information is incomplete.

8C73h The device requires the SET FEATURES sub-command after the power-on sequence in order to spin-up. The Identify information is incomplete.

C837h The device requires the SET FEATURES sub-command after the power-on sequence in order to spin-up. The Identify information is incomplete.

Others Reserved

*4 Word 49: Capabilities

Bit 15-14: Reserved

Bit 13: Standby timer value. ATA spec is '1.'

Bit 12: Reserved

Bit 11: '1' = IORDY supported

Bit 10: '1' = IORDY inhibition supported

Bit 9: '1' = DMA supported

Bit 8: '1' = LBA supported

Bit 7-0: Undefined

*5 Word 50: Device capability

Bit 15: 0

Bit 14: 1

Bit 13 to 1 Reserved

Bit 0 Standby timer value '1' = Standby timer value of the device is the smallest value.

*6 Word 51: PIO data transfer mode

Bit 15-8: PIO data transfer mode X'02'=PIO mode 2 supported

Bit 7-0: Undefined

*7 Word 53: Enable/disable setting of word 54-58 and 64-70

Bit 15-3: Reserved

Bit 2: '1' = Enable the word 88

Bit 1: '1' = Enable the word 64-70

Bit 0: '1' = Enable the word 54-58

*8 Word 59: Transfer sector count currently set by READ/WRITE MULTIPLE command

Bit 15-9: Reserved

Bit 8: '1' = Enable the multiple sector transfer

Bit 7-0: Transfer sector count currently set by READ/WRITE MULTIPLE command without interrupt supports 2, 4, 8 and 16 sectors.

*9 Word 63: Multiword DMA transfer mode

Bit 15-11: Reserved

Bit 10: '1' = multiword DMA mode 2 is selected.

Bit 9: '1' = multiword DMA mode 1 is selected.

Bit 8: '1' = multiword DMA mode 0 is selected.

Bit 7-3: Reserved

Bit 2: '1' = Multiword DMA mode 2, 1, and 0 supported (Bit 1 = 0 = '1')

Bit 1: '1' = Multiword DMA mode 1, and 0 supported (Bit 0 = '1')

Bit 0: '1' = Mode 0

*10 Word 64: Advance PIO transfer mode support status

Bit 15-8: Reserved

Bit 7-0: Advance PIO transfer mode

Bit 1: '1' = Mode 4 supported

Bit 0: '1' = Mode 3 supported

*11 WORD 75: X ' 001F ' (32)

*12 WORD 76

Bit15-10: Reserved

Bit 9: '1' = Supports the Power Management initiation request from the host system.

Bit 8: '1' = Supports the Native command queueing.

Bit 7-4: Reserved

Bit 3: Reserved for SATA

Bit 2: '1' = Supports the Gen-2 signaling rete.

Bit 1: '1' = Supports the Gen-1 signaling rete.

Bit 0: Reserved

*13 WORD 78

Bit15-5: Reserved

Bit 4: '1'= Supports the in-order data delivery.

Bit 3: '1'= Supports the Power Management initiation from the device to the host system.

Bit 2: '1' = Supports the DMA Setup FIS Auto-Activate optimization.

Bit 1: '1' = Supports the non-zero buffer offset in the DMA Setup FIS.

Bit 0: Reserved

*14 WORD 79

Bit15-5: Reserved

Bit 4: '1' = Enables the in-order data delivery.

Bit 3: '1' = Enables the Power Management initiation function from Bit 2:

'1' = Enables the Auto-Activate optimization function in the DMA Setup FIS.

Bit 1: '1' = Enables the non-zero buffer offset function in the DMA Setup FIS.

Bit 0: Reserved

*15 WORD 80

Bit 15-8: Reserved

Bit 7: '1' = ATA/ATAPI-7 supported

Bit 6: '1' = ATA/ATAPI-6 supported

Bit 5: '1' = ATA/ATAPI-5 supported

Bit 4: '1' = ATA/ATAPI-4 supported

Bit 3: '1' = ATA-3 supported

Bit 2: '1' = ATA-2 supported

Bit 1-0: Undefined

*16 WORD 82

Bit 15: Undefined

Bit 14: '1' = Supports the NOP command.

Bit 13: '1' = Supports the READ BUFFER command.

Bit 12: '1' = Supports the WRITE BUFFER command.

Bit 11: Undefined

Bit 10: '1' = Supports the Host Protected Area feature set.

Bit 9: '1' = Supports the DEVICE RESET command.

Bit 8: '1' = Supports the SERVICE interrupt.

Bit 7: '1' = Supports the release interrupt.

Bit 6: '1' = Supports the read cache function.

Bit 5: '1' = Supports the write cache function.

Bit 4: '1' = Supports the PACKET command feature set.

Bit 3: '1' = Supports the power management feature set.

Bit 2: '1' = Supports the Removable Media feature set.

Bit 1: '1' = Supports the Security Mode feature set.

Bit 0: '1' = Supports the SMART feature set.

*17 WORD 83

Bit 15: = 0

Bit 14: = 1

Bit 13: * '1' = Supports the FLUSH CACHE EXT command.

Bit 12: '1' = Supports the FLUSH CACHE command.

Bit 11: '1' = Supports the Device Configuration Overlay feature set.

Bit 10:* '1' = 48 bit LBA feature set.

Bit 9: '1' = Automatic Acoustic Management feature set.

Bit 8: '1' = Supports the SET MAX Security extending command.

Bit 7: Reserved

Bit 6: '1' = When the power is turned on, spin is started by the SET FEATURES sub-command.

Bit 5: '1' = Supports the Power-Up In Standby set.

Bit 4: '1' = Supports the Removable Media Status Notification feature set.

Bit 3: '1' = Supports the Advanced Power Management feature set.

Bit 2: '1' = Supports the CFA (Compact Flash Association) feature set.

Bit 1: '1' = Supports the READ/WRITE DMA QUEUED command.

Bit 0: '1' = Supports the DOWNLOAD MICROCODE command.

*: Option (customizing)

*18 WORD 84

Bit 15: = 0 The device always returns the fixed value indicated on the left.

Bit 14: = 1 The device always returns the fixed value indicated on the left.

Bit 13: '1' = Support the Unload Immediate command.

Bit 12-9 Reserved

Bit 8 '1' = Support the World wide name.

Bit 7 '1' = Support the WRITE DMA QUEUED FUA EXT command. *

Bit 6 '1' = Support the WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands. *

Bit 5 '1'= Support the General Purpose Logging feature.

Bit 4-2 Reserved

Bit 1: '1' = Supports the SMART SELF-TEST.

Bit 0: '1' = Supports the SMART Error Logging.

* Option (customizing)

*19 WORD 85

Bit 15: Undefined.

Bit 14: '1' = Supports the NOP command.

Bit 13: '1' = Supports the READ BUFFER command.

Bit 12: '1' = Supports the WRITE BUFFER command.

Bit 11: Undefined.

Bit 10: '1' = Supports the Host Protected Area function.

Bit 9: '1' = Supports the DEVICE RESET command.

Bit 8: '1' = Enables the SERVICE interrupt. From the SET FEATURES command

Bit 7: '1' = Enables the release interrupt. From the SET FEATURES command

Bit 6: '1' = Enables the read cache function. From the SET FEATURES command

Bit 5: '1' = Enables the write cache function.

Bit 4: '1' = Enables the P PACKET command set.

Bit 3: '1' = Supports the Power Management function.

Bit 2: '1' = Supports the Removable Media function.

Bit 1: '1' = From the SECURITY SET PASSWORD command

Bit 0: '1' = From the SMART ENABLE OPERATION command

*20 WORD 86

Bits 15: Reserved

Bit 13-10: Same definition as WORD 83.

Bit 9: '1' = Enables the Automatic Acoustic Management function from the SET FEATURES command

Bit 8: '1' = From the SET MAX SET PASSWORD command

Bits 7-6: Same definition as WORD 83.

Bit 5: '1' = Enables the Power-Up In Standby function.

Bit 4: '1' = Enables the Removable Media Status Notification function.

Bit 3: '1' = Enables the Advanced Power Management function.

Bits 2-0: Same definition as WORD 83.

*21 WORD 87

Bit 15: = 0 The device always returns the fixed value indicated on the left.

Bit 14: = 1 The device always returns the fixed value indicated on the left.

Bits 13-0: Same definition as WORD 84.

*22 WORD 88

Bit 15-14: Currently used Ultra DMA transfer mode

Bit 13: '1' = Mode 5 is selected.

Bit 12: '1' = Mode 4 is selected.

Bit 11: '1' = Mode 3 is selected.

Bit 10: '1' = Mode 2 is selected.

Bit 9: '1' = Mode 1 is selected.

Bit 8: '1' = Mode 0 is selected.

Bit 7-0: Supportable Ultra DMA transfer mode

Bit 5: '1' = Supports the Mode 5

Bit 4: '1' = Supports the Mode 4

Bit 3: '1' = Supports the Mode 3

Bit 2: '1' = Supports the Mode 2

Bit 1: '1' = Supports the Mode 1

Bit 0: '1' = Supports the Mode 0

*23 WORD 89

MHT2080BH = X'28': 80 minutes

MHT2060BH = X'1E': 60 minutes

MHT2040BH = X'14': 40 minutes

*24 WORD 94

Bit 15-8: X'FE' Recommended acoustic management value.

Bit 7-0: X'XX' Current set value.

FE-C0: Performance mode

BF-80: Acoustic mode

00: Acoustic management is unused it. (It is same as "FE-CO")

*25 WORD 100-103

When "48 bit LBA" of the option (customize) is supported, same number of LBA as WORD 60-61 is displayed.

*26 WORD 106

Bit 15: = 0 The device always returns the fixed value indicated on the left.

Bit 14: = 1 The device always returns the fixed value indicated on the left.

Bit13: '1' = Each device has several logical sectors per physical sector.

Bit12: '1' = Logical sector of the device is grater than 256 Words.

Bit11-4: Reserved

Bit3-0: Logical sector size per physical sector

*27 WORD 128

Bit 15-9: Reserved

Bit 8: Security level. 0: High, 1: Maximum

Bit 7-6: Reserved

Bit 5: '1' = Enhanced security erase supported

Bit 4: '1' = Security counter expired

Bit 3: '1' = Security frozen

Bit 2: '1' = Security locked

Bit 1: '1' = Security enabled

Bit 0: '1' = Security supported

(30) SET FEATURES (X'EF')

The host system issues the SET FEATURES command to set parameters in the Features field for the purpose of changing the device features to be executed.

Upon receipt of this command, the device sets the parameters in the Features field, then reports the status to the host system.

If the value in the Features field is not supported or it is invalid, the device posts an ABORTED COMMAND error.

Table 5.25 lists the available values and operational modes that may be set in the Features field.

Table 5.25 Features field values and settable modes (1/2)

Features Field	Drive operation mode
X ' 02 '	Enables the write cache function.
X ' 03 '	Set the data transfer mode. *1
X ' 04 '	Enables the automatic reassign. (Note)
X ' 05 '	Enables the advanced power management function. *2
X ' 06 '	Enables the Power-Up In Standby function. (Note)
X ' 07 '	Spin up the Power-Up In Standby status device. (Note)
X ' 10 '	Enables the Serial ATA function. *3
X ' 33 '	Undefined (Note)
X ' 42 '	Enables the Acoustic management function. *4
X ' 54 '	Undefined (Note)
X ' 55 '	Disables the read cache function.
X ' 66 '	Disables the reverting to power-on default settings after software reset. (Note)
X ' 77 '	Undefined (Note)
X ' 81 '	Prohibit the 8-bit data transfer. (Note)
X ' 82 '	Disables the write cache function.
X ' 84 '	Enables the automatic shift. (Note)
X ' 85 '	Set the advanced power management mode to Mode-0.
X ' 86'	Prohibit the Power-Up In Standby function. (Note)
X ' 88'	Undefined (Note)
X ' 90'	Disables the Serial ATA function.

Table 5.25 Features field values and settable modes (2/2)

Features Field	Drive operation mode
X ' AA '	Enables the read cache function.
X ' BB '	Specifies the transfer of 4-byte ECC for READ LONG and WRITE LONG commands. (Note)
X ' C2 '	Disables the Acoustic management function.
X ' CC '	Enables the reverting to power-on default settings after software reset. (Note)
Note: Although there is a response to the command, nothing is done.	

At power-on or after COMRESET, the default mode is set as follows.

Write cashe function : Enabled

Transfer mode : PIO Mode-4, Multiworld DMA Mode-2

Advanced power management function : Enabled (Mode-1)

Acoustic management function : State keeping

Read cashe function : Enabled

Serial ATA function : Prohibited

- Error reporting conditions

(1) An undefined code is specified in the FR or SC field (ST = 51h, ER = 04h).

(2) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block O registers setting contents)								
CM	1	1	1	0	1	1	1	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx or *1~3							
FR	[See Table 5.6]							

At command completion (Shadow Block Registers contents to be read)						
ST	Status information					
DH	x	x	x	x	xx	
CH	xx					
CL	xx					
SN	xx					
SC	xx					
E	Error information					

*1) Data Transfer Mode

The host sets X'03' to the Features field. By issuing this command with setting a value to the Sector Count field, the transfer mode can be selected. Upper 5 bits of the Sector Count register defines the transfer type and lower 3 bits specifies the binary mode value.

The IDD supports following values in the Sector Count field value. If other value than below is specified, an ABORTED COMMAND error is posted.

Note: For a serial ATA device, the setting of a data transfer mode is reflected in WORD 63 and 88 in IdentifyDevice information. However, the actual data transfer rate depends on the serial ATA signaling rate in WORD 76 in IdentifyDevice information.

Transfer mode	Sector Count file
• PIO default transfer mode	00000 000 (X'00')
• PIO flow control transfer mode X	00001 000 (X'08': Mode 0)
	00001 001 (X'09': Mode 1)
	00001 010 (X'0A': Mode 2)
	00001 011 (X'0B': Mode 3)
	00001 100 (X'0C': Mode 4)
• Single word DMA Mode X	00010 000 (X ' 10 ' : Mode 0)
	00010 001 (X ' 11 ' : Mode 1)
	00010 010 (X ' 12 ' : Mode 2)

Transfer mode	Sector Count file
• Multiword DMA transfer mode X	00100 000 (X'20': Mode 0)
	00100 001 (X'21': Mode 1)
	00100 010 (X'22': Mode 2)
• Ultra DMA transfer mode X	01000 000 (X'40': Mode 0)
	01000 001 (X'41': Mode 1)
	01000 010 (X'42': Mode 2)
	01000 011 (X'43': Mode 3)
	01000 100 (X'44': Mode 4)
	01000 101 (X'45': Mode 5)

*2) Advanced Power Management (APM)

The host writes the Sector Count field with the desired power management level and executes this command with the Features field X'05', and then Advanced Power Management is enabled.

The drive automatically shifts to power saving mode up to the specified APM level when the drive does not receive any commands for a specific time. The sequence in which the power management level shifts is from Active Idle to Low Power Idle to Standby. The Mode-2 level requires the longest shifting time, depending on the APM level settings. The settings of the APM level revert to their default values (Mode-1) when power-on or a hardware reset occurs for the drive.

APM Level	Sector Count Field
Mode 0 Active Idle → Low Power Idle	C0h-FEh
Mode 1 Active Idle → Low Power Idle	80h-BFh
Mode 2 Active Idle → Low Power Idle → Standby	01h-7Fh
Reserve (State Keep)	00h, FFh

Active Idle: The spindle motor rotates, and the head is loaded on the most inner position on media.

Low Power Idle: The spindle motor rotates, and the head is unloaded.

Standby: The spindle motor stops, and the head is unloaded.

*3) Serial ATA Functions

The host can enable and disable the following Serial ATA functions by issuing this command after setting X'10/90' in the Features field and an applicable value in the Sector Count field:

Serial ATA function	Sector Count field
Non-zero buffer offset in DMA Setup FIS	01h (*1)
DMA Setup FIS Auto-Activate optimization	02h (*2)
Device-initiated interface power state Transitions	03h (*3)
Guaranteed In-Order Data Deliverry	04h (*1)
Asynchronous Notification	05h (*1)

*1 The device normally responds to the command but performs no operation.

*2 This feature is prohibited when power is on. While this function is enabled, the device does not return the DMA Activate FIS for the first data sector after the WRITE FP DMA QUEUED command is issued.

*3 This specification is prohibited when power on. While this function is enabled, the device perform interface power save.

*4) Automatic Acoustic Management (AAM)

The host writes to the Sector Count filed with the requested acoustic management level and executes this command with subcommand code 42h, and then Automatic Acoustic Management is enabled. The AAM level setting is preserved by the drive across power on and COMRESET.

AAM Level	Sector Count Filed
Performance mode (Fast Seek)	C0h-FEh
Acoustic mode (Slow Seek)	80h-BFh
Abort	01h-7Fh
Non Operate	00h, FFh

High-speed seek to which gives priority to the performance operates as for "Performance mode", and low-speed seek by which the seek sound is suppressed operates as for "Acoustic mode".

Setting the seek mode by this command is applied to the seek operation in all command processing.

(31) SECURITY SET PASSWORD (X'F1')

This command enables a user password or master password to be set.

The host transfers the 512-byte data shown in Table 5.26 to the device. The device determines the operation of the lock function according to the specifications of the Identifier bit and Security level bit in the transferred data. (Table 5.27)

Issuing this command in LOCKED MODE or FROZEN MODE returns the Aborted Command error.

Table 5.26 Contents of SECURITY SET PASSWORD data

Word	Contents
0	Control word Bit 0 Identifier 0 = Sets a user password. 1 = Sets a master password. Bits 1 to 7 Reserved Bit 8 Security level 0 = High 1 = Maximum Bits 9 to 15 Reserved
1 to 16	Password (32 bytes)
17	Master password version number
18 to 255	Reserved

Table 5.27 Relationship between combination of Identifier and Security level, and operation of the lock function

Identifier	Level	Description
User	High	The specified password is set as a new user password. The lock function is enabled after the device is turned off and then on. LOCKED MODE can be canceled using the user password or the master password already set.
Master	High	The specified password is set as a new master password. The lock function is not enabled.
User	Maximum	The specified password is set as a new user password. The lock function is enabled after the device is turned off and then on. LOCKED MODE can be canceled using the user password only. The master password already set cannot cancel LOCKED MODE.
Master	Maximum	The specified password is set as a new master password. The lock function is not enabled.

- Error reporting conditions

  (1) The device is in Security Locked mode (ST = 51h, ER = 04h).

  (2) The device is in Security Frozen mode (ST = 51h, ER = 04h).

  (3) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	0	0	0	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Register contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(32) SECURITY UNLOCK(X'F2')

This command cancels LOCKED MODE.

The host transfers the 512-byte data shown in Table 5.28 to the device. Operation of the device varies as follows depending on whether the host specifies the master password.

- When the master password is selected

  When the security level is LOCKED MODE is high, the password is compared with the master password already set. If the passwords are the same, LOCKED MODE is canceled. Otherwise, the Aborted Command error is returned. If the security level in LOCKED MODE is set to the highest level, the Aborted Command error is always returned.

- When the user password is selected

  The password is compared with the user password already set. If the passwords are the same, LOCKED MODE is canceled. Otherwise, the Aborted Command error is returned.

  If the password comparison fails, the device decrements the UNLOCK counter. The UNLOCK counter initially has a value of five. When the value of the UNLOCK counter reaches zero, this command or the SECURITY ERASE UNIT command causes the Aborted Command error until the device is turned off and then on, or until a COMRESET is executed. Issuing this command with LOCKED MODE canceled (in UNLOCK MODE) has no affect on the UNLOCK counter.

- Error reporting conditions

  (1) An incorrect password is specified (ST = 51h, ER = 04h).

  (2) The device is in Security Frozen mode (ST = 51h, ER = 04h).

  (3) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	0	0	1	0
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Register contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(33) SECURITY ERASE PREPARE (X'F3')

The SECURITY ERASE UNIT command feature is enabled by issuing the SECURITY ERASE PREPARE command and then the SECURITY ERASE UNIT command. The SECURITY ERASE PREPARE command prevents data from being erased unnecessarily by the SECURITY ERASE UNIT command.

- Error reporting conditions

  (1) An incorrect password is specified (ST = 51h, ER = 04h).

  (2) The device is in Security Frozen mode (ST = 51h, ER = 04h).

  (3) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	0	0	1	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(34) SECURITY ERASE UNIT (X'F4')

This command erases all user data. This command also invalidates the user password and releases the lock function.

The host transfers the 512-byte data shown in Table 5.28 to the device. The device compares the user password or master password in the transferred data with the user password or master password already set. The device erases user data, invalidates the user password, and releases the lock function if the passwords are the same.

Although this command invalidates the user password, the master password is retained.

To recover the master password, issue the SECURITY SET PASSWORD command and reset the user password.

- Error reporting conditions

  (1) An incorrect password is specified (ST = 51h, ER = 04h).

  (2) The Security Erase Prepare command did not complete normally beforehand (ST = 51h, ER = 04h).

  (3) The device is in Security Frozen mode (ST = 51h, ER = 04h).

  (4) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	0	1	0	0
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(35) SECURITY FREEZE LOCK (X'F5')

This command puts the device into FROZEN MODE. The following commands used to change the lock function return the Aborted Command error if the device is in FROZEN MODE.

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

FROZEN MODE is canceled when the power is turned off, or when COMRESET is reseted.

If this command is reissued in FROZEN MODE, the command is completed and FROZEN MODE remains unchanged.

The following medium access commands return the Aborted Command error when the device is in LOCKED MODE:

- READ DMA (EXT)
- READ LONG
- READ MULTIPLE (EXT)
- READ SECTORS
- READ VERIFY SECTORS
- WRITE DMA (EXT)
- WRITE LONG
- WRITE MULTIPLE (EXT)
- WRITE SECTORS (EXT)
- WRITE VERIFY
- SECURITY DISABLE PASSWORD
- SECURITY FREEZE LOCK
- SECURITY SET PASSWORD
- SET MAX ADDRESS (EXT)

- FLUSH CACHE (EXT)
- DCO RESTORE
- DCO SET
- WRITE MULTIPLE FUA EXT
- WRITE DMA FUA EXT
- READ FP DMA QUEUED
- WRITE FP DMA QUEUED

- Error reporting conditions

  (1) The device is in Security Locked mode (ST = 51h, ER = 04h).

  (2) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	0	1	0	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(36) SECURITY DISABLE PASSWORD (X'F6')

This command invalidates the user password already set and releases the lock function.

The host transfers the 512-byte data shown in Table 5.28 to the device. The device compares the user password or master password in the transferred data with the user password or master password already set, and releases the lock function if the passwords are the same.

Although this command invalidates the user password, the master password is retained. To recover the master password, issue the SECURITY SET PASSWORD command and reset the user password.

If the user password or master password transferred from the host does not match, the Aborted Command error is returned.

Issuing this command while in LOCKED MODE or FROZEN MODE returns the Aborted Command error.

(The section about the SECURITY FREEZE LOCK command describes LOCKED MODE and FROZEN MODE.)

Table 5.28 Contents of security password

Word	Contents
0	Control word Bit 0: Identifier 0 = Compares the user passwords. 1 = Compares the master passwords. Bits 1 to 15: Reserved
1 to 16	Password (32 bytes)
17 to 255	Reserved

- Error reporting conditions

  (1) An incorrect password is specified (ST = 51h, ER = 04h).

  (2) The device is in Security Locked mode (ST = 51h, ER = 04h).

  (3) The device is in Security Frozen mode (ST = 51h, ER = 04h).

  (4) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents))								
CM	1	1	1	1	0	1	1	0
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	xx				
CL	xx				
SN	xx				
SC	xx				
ER	Error information				

(37) READ NATIVE MAX ADDRESS (X'F8')

This command posts the maximum address intrinsic to the device, which can be set by the SET MAX ADDRESS command. Upon receipt of this command, the device indicates the maximum address in the DH, CH, CL and SN field. Then reports the status to the host system.

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	1	0	0	0
DH	x	L	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	Max head/LBA [MSB]
CH	CYL No. [MSB] / LBA				
CL	CYL No. [LSB] / LBA				
SN	SCT No. / LBA[LSB]				
SC	xx				
ER	Error information				

(38) SET MAX (X'F9')

SET MAX Features Register Values

Value	Command
00h	Obsolete
01h	SET MAX SET PASSWORD
02h	SET MAX LOCK
03h	SET MAX UNLOCK
04h	SET MAX FREEZE LOCK
05h - FFh	Reserved

- SET MAX ADDRESS

A successful READ NATIVE MAX ADDRESS command shall immediately precede a SET MAX ADDRESS command.

This command allows the maximum address accessible by the user to be set in LBA or CHS mode. Upon receipt of the command, the device saves the maximum address specified in the DH, CH, CL and SN field then, reports the status to the host.

The new address information set by this command is reflected in Words 1, 54, 57, 58, 60 and 61 of IDENTIFY DEVICE information. If an attempt is made to perform a read or write operation for an address beyond the new address space, an ID Not Found error will result.

When SC field bit 0, VV (Value Volatile), is 1, the value set by this command is held even after power on and the occurrence of a hard reset. When the VV bit is 0, the value set by this command becomes invalid when the power is turned on or a ComRest occurs, and the maximum address returns to the value most lately set when VV bit = 1. (The value by VV bit = 0 is held in case that this command with VV bit = 1 has not been issued or had set the default value, and ComRest occurs.)

When the READ NATIVE MAX ADDRESS command has been issued immediately preceding this command, this command operates normally as the SET MAX ADDRESS command. Otherwise, this command operates as one of the SET MAX subcommands depending on the value in the Features field. The subcommands are explained below.

After power on and the occurrence of a ComRest, the host can issue this command only once when VV bit = 1. If this command with VV bit = 1 is issued twice or more, any command following the first time will result in an Aborted Command error.

When the SET MAX ADDRESS EXT command is executed, all SET MAX ADRESS commands are aborted. The address value returns to the origin when the SET MAX ADDRESS EXT command is executed using the address value returned by the READ NATIVE MAX ADDRESS command.

- Error reporting conditions

  (1) The command has been issued more than twice (ST = 51h, ER = 10h).

  (2) The READ NATIVE MAX ADDRESS command has not been issued prior to the SET MAX ADDRESS command. (ST = 51h, ER = 04h).

  (3) The SET MAX ADDRESS (EXT) command has been issued (ST = 51h, ER = 04h).

  (4) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	1	0	0	1
DH	x	L	x	x	HD No./LBA			
CH	CYL No. [MSB] / LBA							
CL	CYL No. [LSB] / LBA							
SN	SCT No. / LBA[LSB]							
SC	xx							VV
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH	CYL No. [MSB] / LBA				
CL	CYL No. [LSB] / LBA				
SN	SCT No. / LBA[LSB]				
SC	xx				
ER	Error information				

- SET MAX SET PASSWORD (Features Field = 01h)

  This command requests a transfer of 1 sector of data from the host, and defines the contents of SET MAX password. The password is retained by the device until the next power cycle.

- Error reporting conditions

  (1) The device is in Set Max Locked mode or Set Max Freeze Locked mode (ST = 51h, ER =04h).

  (3) The SET MAX ADDRESS (EXT) command has been issued (ST = 51h, ER = 04h).

  (4) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	1	0	0	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	01							

At command completion (Shadow Block Registers contents to be read)	
ST	Status information
DH	xx
CH	xx
CL	xx
SN	xx
SC	xx
ER	Error information

Password information

Words	Contents
0	Reserved
1 to 16	Password (32 bytes)
17 to 255	Reserved

- SET MAX LOCK (Features Field = 02h)

  The SET MAX LOCK command sets the device into SET_MAX_LOCK state. After this command is completed, any other SET MAX commands except SET MAX UNLOCK and SET MAX FREEZE LOCK commands are rejected. And the device returns command aborted.

  The device remains in the SET MAX LOCK state until a power cycle or the acceptance of SET MAX UNLOCK or SET MAX FREEZE LOCK command.

- Error reporting conditions

  (1) The device is in Set Max Locked mode or Set Max Freeze Locked mode (ST = 51h, ER = 04h).

  (2) The SET MAX ADDRESS (EXT) command has been issued (ST = 51h, ER = 04h).

  (3) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	1	0	0	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	02							

At command completion (Shadow Block Registers contents to be read)	
ST	Status information
DH	xx
CH	xx
CL	xx
SN	xx
SC	xx
ER	Error information

- SET MAX UNLOCK (Features Field = 03h)

  This command requests a transfer of single sector of data from the host, and defines the contents of SET MAX ADDRESS password.

  The password supplied in the sector of data transferred shall be compared with the stored password.

  If the password compare fails, the device returns command aborted and decrements the Unlock counter, and remains in the Set Max Lock state. On the acceptance of the SET MAX LOCK command, the Unlock counter is set to a value of five. When this counter reaches zero, then SET MAX UNLOCK command returns command aborted until a power cycle.

  If the password compare matches, then the device makes a transition to the Set Max Unlocked state and all SET MAX commands will be accepted.

- Error reporting conditions

  (1) The device is in Set Max Locked mode or Set Max Freeze Locked mode (ST = 51h, ER = 04h).

  (2) The device is in Set Max Unlocked mode (ST = 51h, ER = 04h).

  (3) The SET MAX ADDRESS (EXT) command has been issued (ST = 51h, ER = 04h).

  (4) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	1	0	0	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	03							

At command completion (Shadow Block Registers contents to be read)	
ST	Status information
DH	xx
CH	xx
CL	xx
SN	xx
SC	xx
ER	Error information

- SET MAX FREEZE LOCK (Features Field = 04h)

  The Set MAX FREEZE LOCK command sets the device to SET_MAX_Frozen state.
  After the device made a transition to the Set Max Freeze Lock state, the following SET MAX commands are rejected, then the device returns command aborted:

  – SET MAX ADDRESS

  – SET MAX SET PASSWORD

  – SET MAX LOCK

  – SET MAX UNLOCK

- Error reporting conditions

  (1) The device is in Set Max Locked mode or Set Max Freeze Locked mode (ST = 51h, ER = 04h).

  (2) The SET MAX ADDRESS (EXT) command has been issued (ST = 51h, ER = 04h).

  (3) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	1	1	0	0	1
DH	x	x	x	x	xx			
CH	xx							
CL	xx							
SN	xx							
SC	xx							
FR	04							

At command completion (Shadow Block Registers contents to be read)	
ST	Status information
DH	xx
CH	xx
CL	xx
SN	xx
SC	xx
ER	Error information

(39) READ SECTOR (S) EXT (X'24')

- Description

  This command is the extended command of the READ SECTOR (S) command. The LBA specification is increased from 28 bits to 48 bits, and the maximum number of sectors that can be transferred by a single command is changed from 100h to 10000h. Other command controls are the same as those of the READ SECTOR (S) command.

- Error reporting conditions

  (1) The command was issued in CHS mode (ST = 51h, ER = 04h).
  The other error reporting conditions are the same as those of the READ SECTOR(S) command.

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	0	0	1	0	0
DH	1	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	LBA (47-40)				
CH	LBA (23-16)				
CL EXP	LBA (39-32)				
CL	LBA (15-8)				
SN EXP	LBA (31-24)				
SN	LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(40) READ DMA EXT (X'25')

- Description

  This command is the extended command of the READ DMA command. The LBA specification is increased from 28 bits to 48 bits, and the maximum number of sectors that can be transferred by a single command is changed from 100h to 10000h. Other command controls are the same as those of the READ DMA command.

- Error reporting conditions

  (1) The command was issued in CHS mode (ST = 51h, ER = 04h).
  The other error reporting conditions are the same as those of the READ DAM command.

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	0	0	1	0	1
DH	1	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	LBA (47-40)				
CH	LBA (23-16)				
CL EXP	LBA (39-32)				
CL	LBA (15-8)				
SN EXP	LBA (31-24)				
SN	LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(41) READ NATIVE MAX ADDRESS EXT (X'27')

- Description

  This command is used to assign the highest address that the device can initially set with the SET MAX ADDRESS EXT command. The maximum address is displayed in the CH(EXP), CL(EXP), SN(EXP) filed of the device shadow block registers.

- Error reporting conditions

  (1) This command is issued with LBA = 0. (ST = 51h, ER= 04h)

  (2) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	0	0	1	1	1
DH	1	L	1	x	xx			
CH EXP	xx							
CH	xx							
CL EXP	xx							
CL	xx							
SN EXP	xx							
SN	xx							
SC EXP	xx							
SC	xx							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	Native max address LBA (47-40)				
CH	Native max address LBA (23-16)				
CL EXP	Native max address LBA (39-32)				
CL	Native max address LBA (15-8)				
SN EXP	Native max address LBA (31-24)				
SN	Native max address LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(42) READ MULTIPLE EXT (X'29')

- Description

  This command is the extended command of the READ MULTIPLE command. The LBA specification is increased from 28 bits to 48 bits, and the maximum number of sectors that can be transferred by a single command is changed from 100h to 10000h. Other command controls are the same as those of the READ MULTIPLE command.

- Error reporting conditions

  (1) The command was issued in CHS mode (ST = 51h, ER = 04h).
  The other error reporting conditions are the same as those of the READ MULTIPLE command.

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	0	1	0	0	1
DH	1	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	LBA (47-40)				
CH	LBA (23-16)				
CL EXP	LBA (39-32)				
CL	LBA (15-8)				
SN EXP	LBA (31-24)				
SN	LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(43) READ LOG EXT (X'2F')

The READ LOG EXTEND command reads versatile log data. Versatile log data includes the Extended SMART Comprehensive Error log, the Extended SMART Self-test log, and the SMART Selective log. The effectiveness of the log types depends on customization. All types of versatile log data except Read Log Ext log page 10h are customizable. For the protocol concerning data transfers, see Section 5.4.

The number of the log to be read is specified as the Log address. For log data consisting of multiple sectors, a sector offset can be specified as an instruction so that data transfer starts from the specified sector. The number of sectors to be transferred is specified as the Sector count.

If an error occurs in the FP Queued protocol, Read Log Ext log page 10h containing the error information is transferred. This Read Log Ext log page can be read by specifying Sector offset = 00h, Sector count = 01h, and Log address = 10h. For the data format of Read Log Ext log page 10h, see Table 5.29.

If this command is not supported, or if an invalid value is specified for the Log address, Sector count, or Sector offset, the Aborted Command error occurs.

- Error reporting conditions

  (1) An error was detected during power-on processing (ST = 51h, ER = 04h).

  (2) An error was detected during wake-up processing (in cases where wake-up processing is required before execution of this command) (ST = 51h, ER = 04h).

  (3) An error that cannot be corrected with ECC occurred (ST = 51h, ER = 40h).

  (4) The sync byte indicating the beginning of a sector was not found (ST = 51h, ER = 01h).

  (5) An invalid log sector address or invalid Sector count (number of sectors to be transferred) is specified (ST = 51h, ER = 04h).

  (6) A SATA communication error occurred (ST = 51h, ER = 0Ch).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	0	1	1	1	1
DH	x	x	x	x	xx			
CH EXP	xx							
CH	xx							
CL EXP	Sector offset (15-8)							
CL	Sector offset (7-0)							
SN EXP	xx							
SN	Log address							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH EXP	xx				
CH	xx				
CL EXP	xx				
CL	xx				
SN EXP	xx				
SN	xx				
SC EXP	xx				
SC	xx				
ER	Error information				

Table 5.29 Data format of Read Log Ext log page 10h

Byte	Item
00	Tag field
01	Reserved
02	Status field value
03	Error field value
04	Sector Number field value
05	Cylinder Low field value
06	Cylinder High field value
07	Dev/Head field value
08	Sector Number Exp field value
09	Cylinder Low Exp field value
0A	Cylinder High Exp field value
0B	Reserved
0C	Sector Count field value
0D	Sector Count Exp field value
0E to FF	Reserved
100 to 1FE	Vendor Unique
1FF	Check sum

Table 5.30 Tag field information

Bit	Description
0 … 4	If bit 7 is 0, this field has an error tag number.
5 6	Reserved
7	If this bit is 0, the field consisting of bits 0 to 4 has an error tag number.

(44) WRITE SECTOR (S) EXT (X'34')

- Description

  This command is the extended command of the WRITE SECTOR (S) command. The LBA specification is increased from 28 bits to 48 bits, and the maximum number of sectors that can be transferred by a single command is changed from 100h to 10000h. Other command controls are the same as those of the WRITE SECTOR (S) command.

- Error reporting conditions

  (1) The command was issued in CHS mode (ST = 51h, ER = 04h).
  The other error reporting conditions are the same as those of the WRITE SECTOR(S) command.

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	1	0	1	0	0
DH	1	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	LBA (47-40)				
CH	LBA (23-16)				
CL EXP	LBA (39-32)				
CL	LBA (15-8)				
SN EXP	LBA (31-24)				
SN	LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(45) WRITE DMA EXT (X'35')

- Description

  This command is the extended command of the WRITE DMA command. The LBA specification is increased from 28 bits to 48 bits, and the maximum number of sectors that can be transferred by a single command is changed from 100h to 10000h. Other command controls are the same as those of the WRITE DMA command.

- Error reporting conditions

  (1) The command was issued in CHS mode (ST = 51h, ER = 04h).
  The other error reporting conditions are the same as those of the WRITE DMA command.

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	1	0	1	0	1
DH	1	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	LBA (47-40)				
CH	LBA (23-16)				
CL EXP	LBA (39-32)				
CL	LBA (15-8)				
SN EXP	LBA (31-24)				
SN	LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(46) SET MAX ADDRESS EXT (X'37')

- Description

  This command limits specifications so that the highest address that can be accessed by users can be specified only in LBA mode.

  The address information specified with this command is set in words 1, 54, 57, 58, 60, 61, and 100 to 103 of the IDENTIFY DEVICE command response. If read or write processing is executed for an address that is outside of the new address space, an ID Not Found error occurs.

  If the SC field bit is 0 and the value volatile (VV) bit is 1 when this command is executed, the specified values are maintained after a power-on or a COMRESET. If the VV bit is 0 when the command is executed, the specified values are invalidated during the power-on sequence. If the VV bit is 1, the highest address value is defined as the last value specified. (If the VV bit is not set to 1, the highest address is the default value.)

  After a power-on reset is performed, a host can issue the SET MAX ADDRESS (EXT) command only once if the VV bit is 1. If the SET MAX ADDRESS (EXT) command is issued twice or more, an ID Not Found error occurs.

  When the SET MAX ADDRESS EXT command is executed, all SET MAX ADDRESS commands are aborted. The address value returns to the origin when the SET MAX ADDRESS EXT command is executed using the address value returned by the READ NATIVE MAX ADDRESS command.

- Error reporting conditions

  (1) This command is issued twice or more in an operation sequence. (ST = 51h, ER = 10h)

  (2) The READ NATIVE MAX ADDRESS EXT command (27h) is not issued immediately before this command (ST = 51h, ER = 04h) is issued.

  (3) This command is issued in CHS mode (ST = 51h, ER = 04h)

  (4) The SET MAX ADDRESS command has already been issued. (ST = 51h, ER = 04h)

  (5) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	1	0	1	1	1
DH	1	L	1	x	xx			
CH EXP	SET MAX LBA (47-40)							
CH	SET MAX LBA (23-16)							
CL EXP	SET MAX LBA (39-32)							
CL	SET MAX LBA (15-8)							
SN EXP	SET MAX LBA (31-24)							
SN	SET MAX LBA (7-0)							
SC EXP	xx							
SC	xx							VV
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	SET MAX LBA (47-40)				
CH	SET MAX LBA (23-16)				
CL EXP	SET MAX LBA (39-32)				
CL	SET MAX LBA (15-8)				
SN EXP	SET MAX LBA (31-24)				
SN	SET MAX LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(47) WRITE MULTIPLE EXT (X'39')

- Description

  This command is the extended command of the WRITE MULTIPLE command. The LBA specification is increased from 28 bits to 48 bits, and the maximum number of sectors that can be transferred by a single command is changed from 100h to 10000h. Other command controls are the same as those of the WRITE MULTIPLE command.

- Error reporting conditions

  (1) The command was issued in CHS mode (ST = 51h, ER = 04h).
  The other error reporting conditions are the same as those of the WRITE MULTIPLE command.

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	1	1	0	0	1
DH	1	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	LBA (47-40)				
CH	LBA (23-16)				
CL EXP	LBA (39-32)				
CL	LBA (15-8)				
SN EXP	LBA (31-24)				
SN	LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(48) WRITE LOG EXT (X'3F')

The WRITE LOG EXTEND command writes versatile log data. Versatile log data includes the Extended SMART Comprehensive Error log, the Extended SMART Self-test log, and the SMART Selective log; and each log can be partially written with this command. The effectiveness of the log types depends on customization. For the protocol concerning data transfers, see Section 5.4.

The number of a log to be written is specified as the Log address. For log data consisting of multiple sectors, a sector offset can be specified as an instruction so that data transfer starts from the specified sector. The number of sectors to be transferred is specified as the Sector count.

If this command is not supported, or if an invalid value is specified for the Log address, Sector count, or Sector offset, the Aborted Command error occurs.

- Error reporting conditions

  (1) An error was detected during power-on processing (ST = 51h, ER = 04h).

  (2) An error was detected during wake-up processing (in cases where wake-up processing is required before execution of this command) (ST = 51h, ER = 04h).

  (3) A write fault was detected while the write cache was disabled (ST = 71h, ER = 10h).

  (4) While the write cache is enabled, if the status indicating a completed transfer (STS = 50h) is returned and a data write operation failed because a write fault was detected during the data write operation, Abort will be returned for all subsequent ATA commands (ST = 71h, ER = 04h). This state is cleared the next time that the device is turned on.

  (5) An invalid log sector address or invalid Sector count (number of sectors to be transferred) is specified (ST = 51h, ER = 04h).

  (6) The failure prediction capability is disabled (ST = 51h, ER = 04h).

  (7) A check sum error was detected in the data transferred (ST = 51h, ER = 04h).

  (8) A SATA communication error occurred (ST = 51h, ER = 0Ch).

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	1	1	1	1	1
DH	x	x	x	x	xx			
CH EXP	xx							
CH	xx							
CL EXP	Sector offset (15-8)							
CL	Sector offset (7-0)							
SN EXP	xx							
SN	Log address							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	x	x	x	x	xx
CH EXP	xx				
CH	xx				
CL EXP	xx				
CL	xx				
SN EXP	xx				
SN	xx				
SC EXP	xx				
SC	xx				
ER	Error information				

(49) READ VERIFY SECTOR (S) EXT (X'42')

- Description

  This command is the extended command of the READ VERIFY SECTOR (S) command. The LBA specification is increased from 28 bits to 48 bits, and the maximum number of sectors that can be transferred by a single command is changed from 100h to 10000h. Other command controls are the same as those of the READ VERIFY SECTOR (S) command.

- Error reporting conditions

  (1) The command was issued in CHS mode (ST = 51h, ER = 04h).
  The other error reporting conditions are the same as those of the READ VERIFY SECTOR(S) command.

At command issuance (Shadow Block Registers setting contents)								
CM	0	1	0	0	0	0	1	0
DH	1	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	LBA (47-40)				
CH	LBA (23-16)				
CL EXP	LBA (39-32)				
CL	LBA (15-8)				
SN EXP	LBA (31-24)				
SN	LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(50) FLUSH CACHE EXT (X'EA')

- Description

  This command executes the same operations as the FLUSH CACHE command (E7h). However, only LBA=1 can be specified in the command.

- Error reporting conditions

  (1) A SATA communication error occurred (ST = 51h, ER = 14h).

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	1	0	1	0	1	0
DH	1	L	1	x	xx			
CH EXP	xx							
CH	xx							
CL EXP	xx							
CL	xx							
SN EXP	xx							
SN	xx							
SC EXP	xx							
SC	xx							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	xx				
CH	xx				
CL EXP	xx				
CL	xx				
SN EXP	xx				
SN	xx				
SC EXP	xx				
SC	xx				
ER	Error information				

(51) WRITE MULTIPLE FUA EXT (X'CE')

- Description

The WRITE MULTIPLE FUA EXT command reports the status of a command after user data is written to a medium, regardless of whether the write cache feature is enabled or disabled. The other command control and error reporting conditions are the same as those of the WRITE MULTIPLE EXT command.

At command issuance (Shadow Block Registers setting contents)								
CM	1	1	0	0	1	1	1	0
DH	1	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	LBA (47-40)				
CH	LBA (23-16)				
CL EXP	LBA (39-32)				
CL	LBA (15-8)				
SN EXP	LBA (31-24)				
SN	LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(52) WRITE DMA FUA EXT (X'3D')

- Description

The WRITE DMA FUA EXT command reports the status of a command after user data is written to a medium, regardless of whether the write cache feature is enabled or disabled. The other command control and error reporting conditions are the same as those of the WRITE DMA EXT command.

At command issuance (Shadow Block Registers setting contents)								
CM	0	0	1	1	1	1	0	1
DH	1	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	Sector count (15-8)							
SC	Sector count (7-0)							
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	LBA (47-40)				
CH	LBA (23-16)				
CL EXP	LBA (39-32)				
CL	LBA (15-8)				
SN EXP	LBA (31-24)				
SN	LBA (7-0)				
SC EXP	xx				
SC	xx				
ER	Error information				

(53) READ FP DMA QUEUED (X'60')

- Description

For details about control of the READ FP DMA QUEUED command, see Section 5.4.6.

At command issuance (Shadow Block Registers setting contents)								
CM	0	1	1	0	0	0	0	0
DH	FUA	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	xx							
SC	TAG				xx			
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	xx				
CH	xx				
CL EXP	xx				
CL	xx				
SN EXP	xx				
SN	xx				
SC EXP	xx				
SC	xx				
ER	Error information				

FUA: If this bit is 1, the device always reads data from media regardless of whether the data requested by the host is in the cache.

TAG: Number of a TAG specified by the host

(54) WRITE FP DMA QUEUED (X'61')

- Description

For details about control of the WRITE FP DMA QUEUED command, see Section 5.4.6.

At command issuance (Shadow Block Registers setting contents)								
CM	0	1	1	0	0	0	0	1
DH	FUA	L	1	x	xx			
CH EXP	LBA (47-40)							
CH	LBA (23-16)							
CL EXP	LBA (39-32)							
CL	LBA (15-8)							
SN EXP	LBA (31-24)							
SN	LBA (7-0)							
SC EXP	xx							
SC	TAG				xx			
FR EXP	xx							
FR	xx							

At command completion (Shadow Block Registers contents to be read)					
ST	Status information				
DH	1	L	1	x	xx
CH EXP	xx				
CH	xx				
CL EXP	xx				
CL	xx				
SN EXP	xx				
SN	xx				
SC EXP	xx				
SC	xx				
ER	Error information				

FUA: If this bit is 1, the device always reports the status after data is written to a medium.

TAG: Number of a TAG specified by the host

5.3.3 Error posting

Table 5.31 lists the defined errors that are valid for each command.

Table 5.31 Command code and parameters (1/2)

COMMAND NAME	Error Field						Status Field		
	SFRW	SFRR	UNC	IDNF	ABRT	TK0NF	DRDY	DWF	ERR
RECALIBRATE	V				V	V	V	V	V
READ SECTOR(S)		V	V	V	V		V	V	V
READ LONG		V		V	V		V	V	V
WRITE SECTOR(S)	V			V	V		V	V	V
WRITE LONG	V			V	V		V	V	V
WRITE VERIFY	V		V	V	V		V	V	V
READ VERIFY SECTOR(S)		V	V	V	V		V	V	V
SEEK	V			V	V		V	V	V
EXECUTE DEVICE DIAGNOSTIC	V		*1	*1	*1	*1			
INITIALIZE DEVICE PARAMETERS	V				V		V	V	V
DOWNLOAD MICROCODE	V				V		V	V	V
STANDBY IMMEDIATE	V				V		V	V	V
IDLE IMMEDIATE	V				V		V	V	V
STANDBY	V				V		V	V	V
IDLE	V				V		V	V	V
CHECK POWER MODE	V				V		V	V	V
SLEEP	V				V		V	V	V
SMART	V	V		V	V		V	V	V
DEVICE CONFIGURATION	V	V			V		V	V	V
READ MULTIPLE		V	V	V	V		V	V	V
WRITE MULTIPLE	V			V	V		V	V	V
SET MULTIPLE MODE	V				V		V	V	V
READ DMA		V	V	V	V		V	V	V
WRITE DMA	V			V	V		V	V	V
READ BUFFER		V			V		V	V	V
FLUSH CACHE	V			V	V		V	V	V
WRITE BUFFER	V				V		V	V	V
IDENTIFY DEVICE		V			V		V	V	V
IDENTIFY DEVICE DMA		V			V		V	V	V
SET FEATURES	V				V		V	V	V
SECURITY SET PASSWORD	V				V		V	V	V

Table 5.31 Command code and parameters (2/2)

COMMAND NAME	Error Field						Status Field		
	SFRW	SFRR	UNC	IDNF	ABRT	TK0NF	DRDY	DWF	ERR
SECURITY UNLOCK	V				V		V	V	V
SECURITY ERASE PREPARE	V				V		V	V	V
SECURITY ERASE UNIT	V				V		V	V	V
SECURITY FREEZE LOCK	V				V		V	V	V
SECURITY DISABLE PASSWORD	V				V		V	V	V
READ NATIVE MAX ADDRESS	V				V		V	V	V
SET MAX	V			V	V		V	V	V
READ SECTOR(S) EXT		V	V	V	V		V	V	V
READ DMA EXT		V	V	V	V		V	V	V
READ NATIVE MAX ADDRESS EXT	V				V		V	V	V
READ MULTIPLE EXT		V	V	V	V		V	V	V
WRITE LOG EXT	V			V	V		V	V	V
WRITE SECTOR(S) EXT	V			V	V		V	V	V
WRITE DMA EXT	V			V	V		V	V	V
SET MAX ADDRESS EXT	V			V	V		V	V	V
WRITE MULTIPLE EXT	V			V	V		V	V	V
READ LOG EXT		V	V	V	V		V	V	V
READ VERIFY SECTOR(S) EXT		V	V	V	V		V	V	V
FLUSH CACHE EXT	V			V	V		V	V	V
WRITE MULTIPLE FUA EXT	V			V	V		V	V	V
WRITE DMA FUA EXT	V			V	V		V	V	V
READ FP DMA QUEUED		V	V	V	V		V	V	V
WRITE FP DMA QUEUED	V			V	V		V	V	V

V: Valid on this command

*1: See the command descriptions.

* For a description of each bit in the Error field and Status field, see Section 5.2.4.

5.4 Command Protocol

The host should confirm that the BSY bit of the Shadow Block Status register of the device is 0 prior to issue a command. If BSY bit is 1, the host should wait for issuing a command until BSY bit is cleared to 0.

Commands can be executed only when the DRDY bit of the Status register is 1. However, the following commands can be executed even if DRDY bit is 0.

- EXECUTE DEVICE DIAGNOSTIC
- INITIALIZE DEVICE PARAMETERS

5.4.1 Non-data command protocol

Execution of the following commands does not involve data transfer between the host and the device.

- RECALIBRATE
- SEEK
- READ VERIFY SECTOR(S) (EXT)
- EXECUTE DEVICE DIAGNOSTIC
- INITIALIZE DEVICE PARAMETERS
- SET FEATURES
- SET MULTIPLE MODE
- SET MAX ADDRESS (EXT)
- READ NATIVE MAX ADDRESS (EXT)
- IDLE
- IDLE IMMEDIATE
- STANDBY
- STANDBY IMMEDIATE
- CHECK POWER MODE
- SMART DISABLE OPERATION
- SMART ENABLE/DISABLE AUTOSAVE
- SMART ENABLE OPERATION

- SMART EXECUTE OFFLINE IMMEDIATE
- SMART RETURN STATUS
- SECURITY ERASE PREPARE
- SECURITY FREEZE LOCK
- FLUSH CACHE (EXT)
- SLEEP
- DEVICE CONFIGRATION RESTORE (FREEZE LOCK)

The following is the protocol for command execution without data transfer:

1) The device receives a non-data command with the Register HD FIS.
2) The device executes the received command.
3) Command execution is completed.
4) The device reports the completion of command execution by sending to the host the Register DH FIS with 1 set in the I bit.

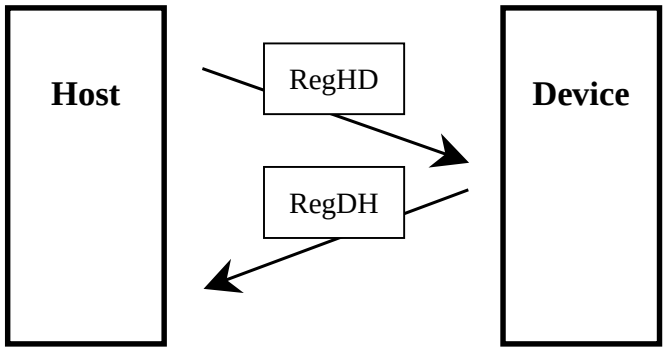


Figure 5.10 Non-data command protocol

5.4.2 PIO data-in command protocol

Execution of the following commands involves data transfers from the device to the host system:

- IDENTIFY DEVICE
- READ SECTOR(S) (EXT)
- READ MULTI (EXT)
- READ LONG
- READ BUFFER
- SMART READ DATA
- SMATR READ LOG SECTOR
- READ LOG EXT
- DEVICE CONFIGRATION IDENTIFY

Data of one or more sectors is transferred from the device to the host. With the READ LONG command, data of 516 bytes is transferred.

An outline of this protocol is as follows:

1) The device receives a PIO data-in command with the Register HD FIS.
2) If an error remaining in the device prevents command execution, the device sends the Register DH FIS with 1 set in the I bit.
3) When the device is ready to send data, it sets 0 in the BSY bit, 1 in the DRQ bit, and 1 in the I bit of the Status field of the PIO Setup FIS, then sends this FIS to the host. At this time, if the requested data is read from the last sector to be processed, the device sets 0 in both the BSY bit and DRQ bit of the E_Status field. Otherwise, the device sets 1 in the BSY bit and 0 in the DRQ bit of the E_Status field.
4) The device sends the DATA FIS to the host.
5) When all data has been transferred, command execution is completed. If any data remains to be transferred, this protocol is repeated starting from step 3). (The maximum data size is 8 KB.)

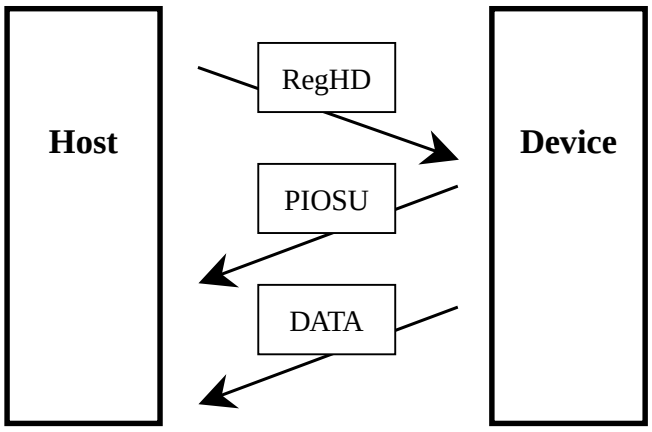


Figure 5.11 PIO data-in command protocol

5.4.3 PIO data-out command protocol

Execution of the following commands involves data transfers from the host system to the device:

- WRITE SECTOR(S) (EXT)
- WRITE MULTI (EXT) (FUA EXT)
- WRITE LONG
- WRITE BUFFER
- WRITE VERIFY
- SMART WRITE LOG SECTOR
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- DOWNLOAD MICROCODE
- WRITE LOG EXT
- DEVICE CONFIGRATION SET

Data of one or more sectors is transferred from the host to the device. With the WRITE LONG command, data of 516 bytes is transferred.

An outline of this protocol is as follows:

1) The device receives a PIO data-out command with the Register HD FIS.
2) If an error remaining in the device prevents command execution, the device sends the Register DH FIS with 1 set in the I bit.
3) When the device is ready to receive data, it sets 0 in the BSY bit and 1 in the DRQ bit of the Status field of the PIO Setup FIS. At this time, the device sets 0 in the I bit of the Status field of the PIO Setup FIS for a data transfer to the first sector, while it sets 1 in the I bit for a data transfer to any sector other than the first sector. Then, it sends this FIS to the host. In the E_Status field, the device sets 1 in the BSY bit and 0 in the DRQ bit.
4) The device receives the DATA FIS from the host.
5) When all data has been transferred, the device sends the Register DH FIS (with 1 set in the I bit) to complete execution of the command. If the device has an error, it reports the error. If any data remains to be received by the device, this protocol is repeated starting from step 3). (The maximum data size is 8 KB.)

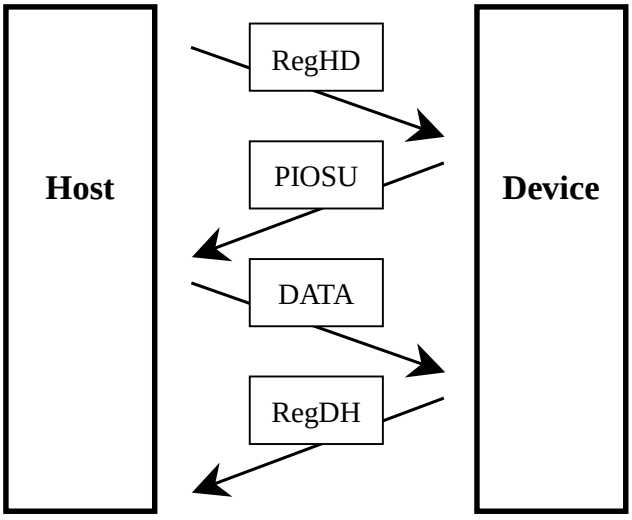


Figure 5.12 PIO data-out command protocol

5.4.4 DMA data-in command protocol

DMA data-in commands include the following commands:

- READ DMA (EXT)
- IDENTFY DMA

The DMA mechanism transfers data of more than one block from the device to the host. The completion of a command is reported by an interruption.

An outline of this protocol is as follows:

1) The device receives a DMA data-in command with the Register HD FIS.
2) If an error remaining in the device prevents command execution, the device sends the Register DH FIS with 1 set in the I bit.
3) When the device is ready to send data, it sends the Data FIS to the host.
4) When all data has been transferred, the device sends the Register DH FIS (with 1 set in the I bit) to complete execution of the command. If any data remains to be sent by the device, this protocol is repeated starting from step 3). (The maximum data size is 8 KB.)

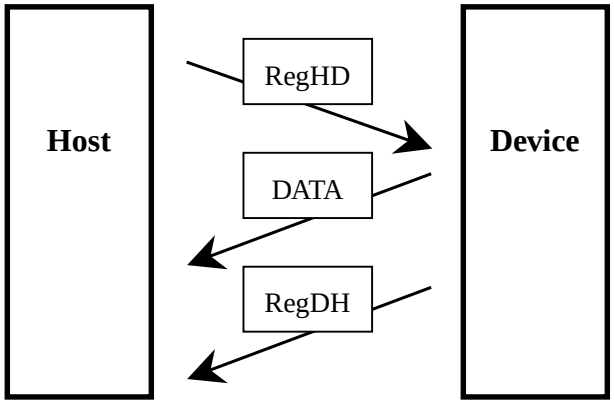


Figure 5.13 DMA data-in command protocol

5.4.5 DMA data-out command protocol

The DMA data-out command is the following command:

- WRITE DMA (EXT) (FUA EXT)

The DMA mechanism transfers data of more than one block from the host to the device. The completion of the command is reported by an interruption.

An outline of this protocol is as follows:

1) The device receives the DMA data-out command with the Register HD FIS.
2) If an error remaining in the device prevents command execution, the device sends the Register DH FIS with 1 set in the I bit.
3) When the device is ready to receive data, it sends the DMA Activate FIS to the host.
4) The device receives the Data FIS from the host.
5) When all data has been transferred, the device sends the Register DH FIS (with 1 set in the I bit) to complete execution of the command. If any data remains to be received by the device, this protocol is repeated starting from step 3). (The maximum data size is 8 KB.)

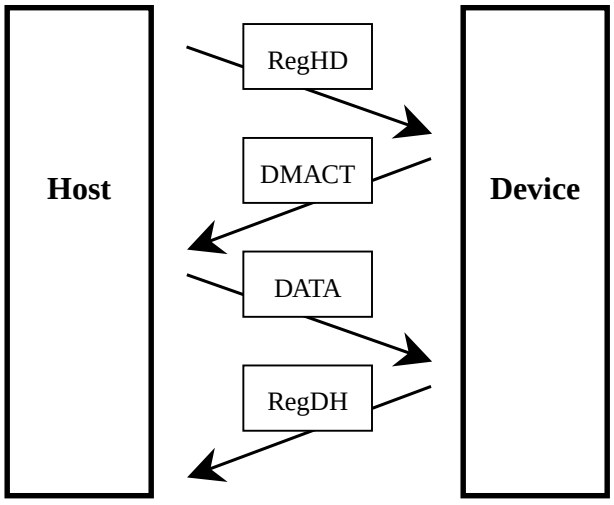


Figure 5.14 DMA data-out command protocol

5.4.6 Native Command Queuing protocol

Native Queued commands include the following commands:

READ FP DMA QUEUED

WRITE FP DMA QUEUED

An outline of the command queuing protocol is as follows:

1) After the device receives a Native Queued command, if the command is executable, the device sends to the host the Register DH FIS with the settings of I bit = 0, BSY bit = 0, and DRQ bit = 0, and it places the command in the command queue. Otherwise, the device sends the Register DH FIS to the host to report an error.
2) If the device receives a command that is not a Native Queued command during command queuing, the device sends to the host the Register DH FIS with the settings of ERR bit = 1, I bit = 1, BSY bit = 0, DRQ bit = 0, and Error register = 0x04 to report an abort.
3) When the device is ready to send data for the data transfer of the READ FP DMA QUEUED command, it sends to the host the DMA Setup FIS with the settings of TAG = #, D bit = 1, I bit = 0, and A bit = 0, and it then sends the Data FIS to the host. (The Data FIS is transferred in units of up to 8 KB).
4) When the read data transfer requested by the command is completed and the command is completed normally, the bit in the SActive field in the Set Device Bits FIS corresponding to the tag number of the completed command is set by the device, and the device sets 0 in the Err bit and 0 in the Error register in the Set Device Bits FIS. Then, it sends the Set Device Bits FIS to the host.
5) For the data transfer of the WRITE FP DMA QUEUED command, if the DMA Setup Auto Activate function is disabled, the device sends to the host the DMA Setup FIS with the settings of TAG = #, D bit = 0, A bit = 0, and I bit = 0, and it sends the DMA Activate FIS before it receives the Data FIS from the host. (The Data FIS is transferred in units of up to 8 KB, with the actual length of the Data FIS varying depending on the host).
6) If the DMA Setup AutoActivate function is enabled, the device sends to the host the DMA Setup FIS with the settings of TAG = #, D bit = 0, A bit = 1, and I bit = 0, and it then receives the Data FIS from the host (in units of 8 KB, 16 sectors).
7) When the write data transfer requested by the command is completed and the command is completed normally, the bit in the SActive field in the Set Device Bits FIS corresponding to the tag number of the completed command is set by the device, and the device sets 0 in the Err bit and 0 in the Error register in the Set Device Bits FIS. Then, it sends the Set Device Bits FIS to the host. (The DMA Setup AutoActivate function can be enabled and disabled by the SET FEATURES command. The function is disabled by default.)

8) If an uncorrectable error occurs during command queuing, the device sends to the host the Set Device Bits FIS with the settings of ERR bit = 1, ERRReg = ATAErrCode, I bit = 1, and SActive = 0 to report an error.

9) After reporting the error, the device accepts only the READ LOG EXT command with page 10h specified and the reset requests (SoftReset and COMRESET). The device reports abort for other commands.

10) If the device receives the READ LOG EXT command with page 10h specified, queued commands are aborted. Then, after the device sends to the host the Set Device Bits FIS (ERR = 0, ERRReg = 0, I = 0, and SActive =0xFFFFFFFF), it sends to the host the log data for the READ LOG EXT command with page 10h specified and reports the status of this command. Next, the command queuing function is enabled, and commands can be accepted again.

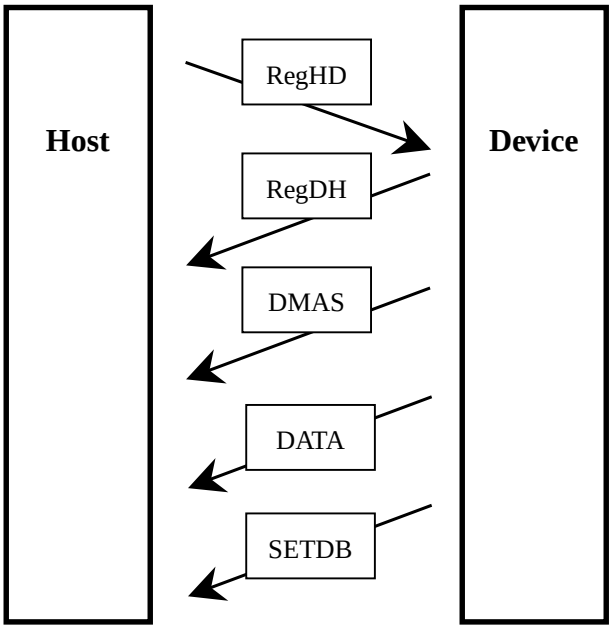


Figure 5.15 READ FP DMA QUEUED command protocol

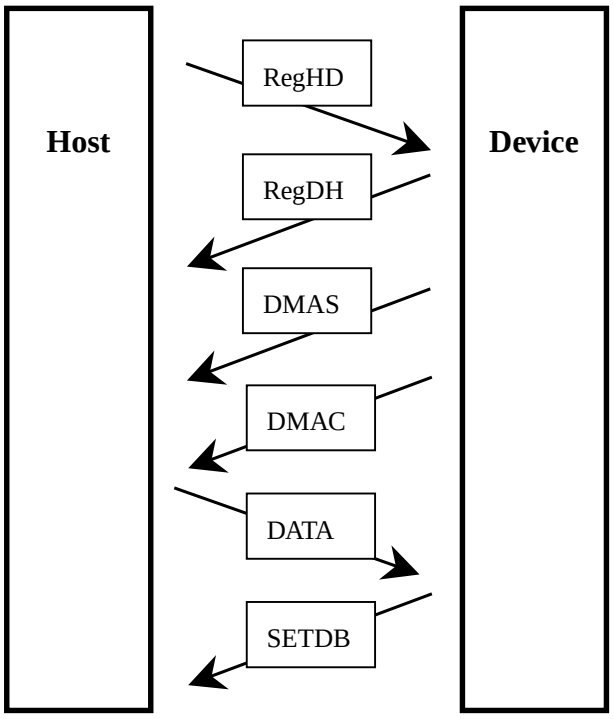


Figure 5.16 WRITE FP DMA QUEUED command protocol

5.5 Power-on and COMRESET

Figure 5.17 shows the power-on sequence, and Figure 5.18 shows the COMRESET sequence.

Immediately after power-on or COMRESET, the host sets 0x7Fh in the Status field of the Shadow Block Register and 0xFFh in other fields. After the power-on sequence shown below and after communication with the SATA interface is established, the host sets 0xFFh in the Status field of the Shadow Block Register. The device completes the power-on sequence within 10 ms so that communication with the SATA interface can be established.

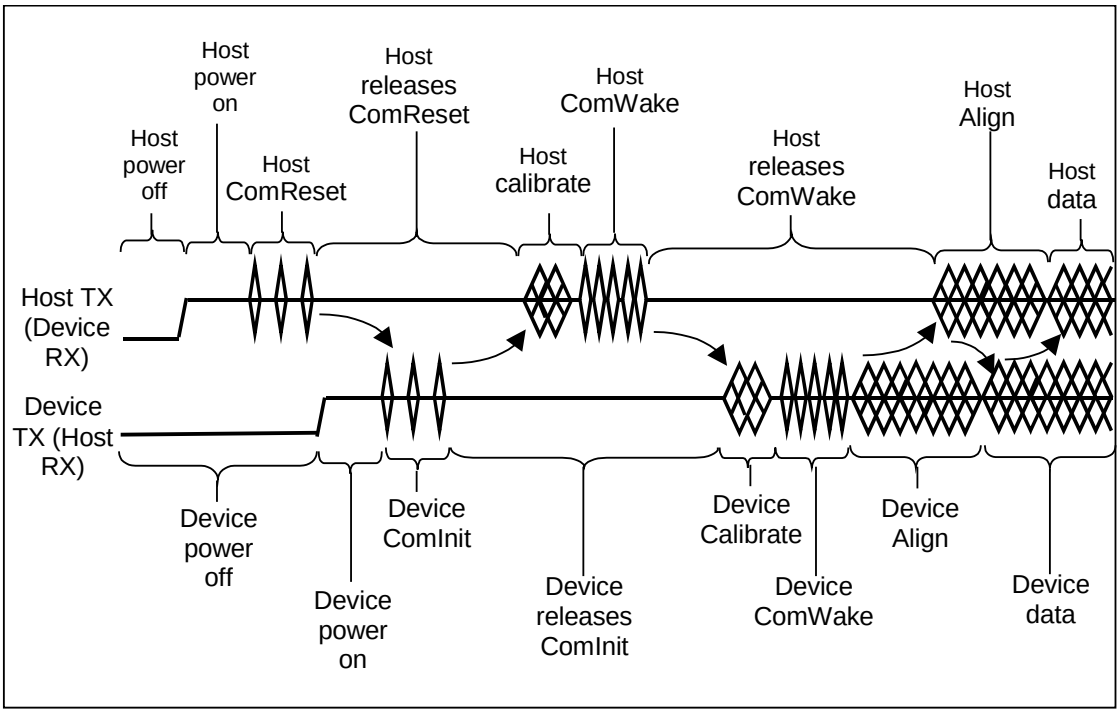


Figure 5.17 Power-on sequence

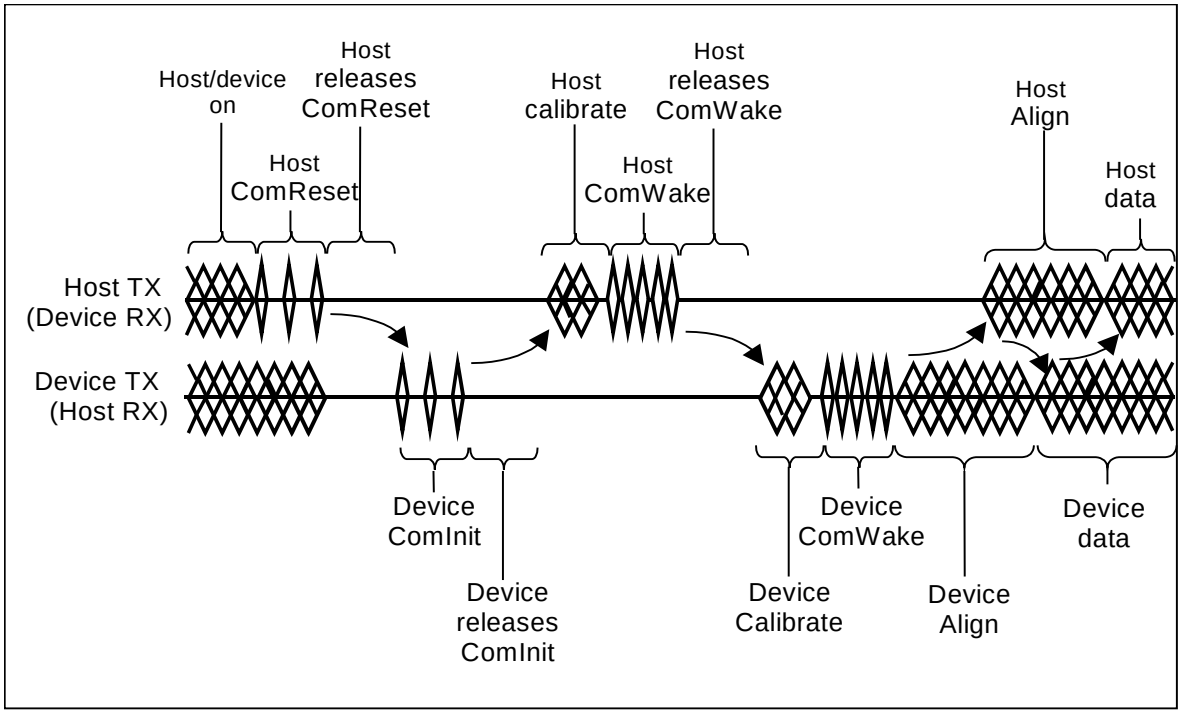


Figure 5.18 COMRESET sequence

CHAPTER 6 Operations

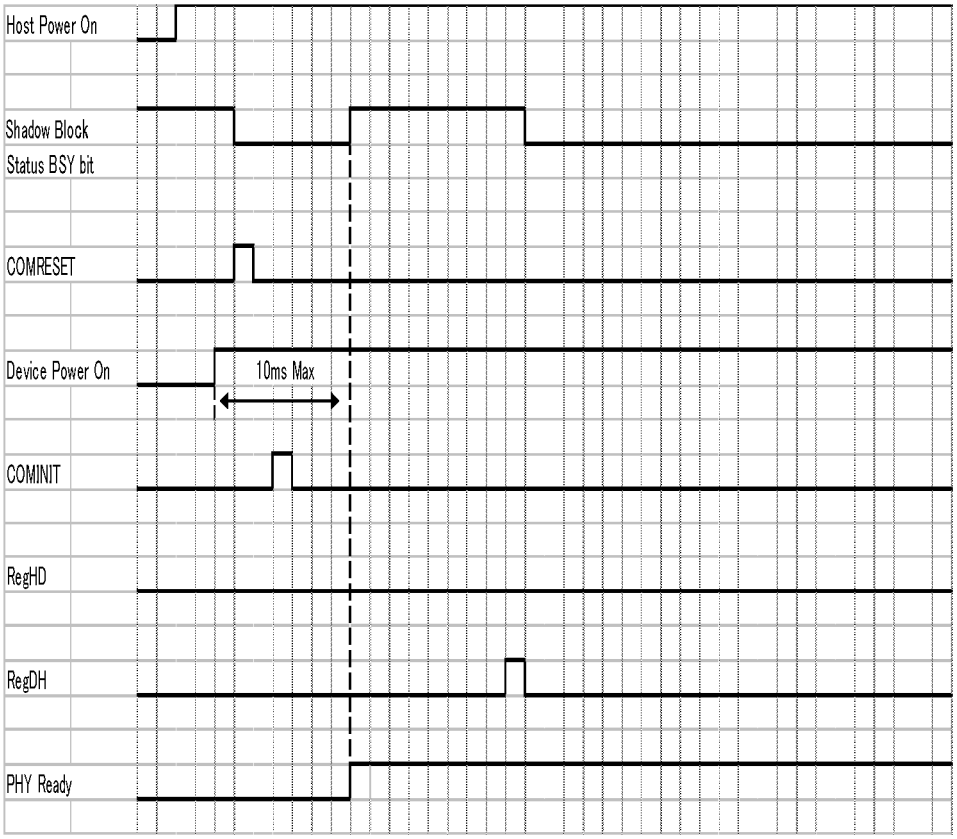
This chapter explains each of the above operations.

6.1 Reset and Diagnosis

This section explains the device responses to power-on and an accepted reset.

6.1.1 Response to power-on

Immediately after power is turned on, the host sets 0x7Fh in the Status field of the Shadow Block and 0xFFh in other fields. After communication with the SATA interface is established, the host sets 0xFFh in the Status field of the Shadow Block. The device establishes communication with the SATA interface (PHY Ready) within 10 ms. The device sends the FIS (STS = 50h) to notify the host that the device is ready.



Note: Figure 6.1 assumes that power is turned on after the power-off state continued for more than five seconds.

Figure 6.1 Response to power-on (when the host is powered on earlier than the device)

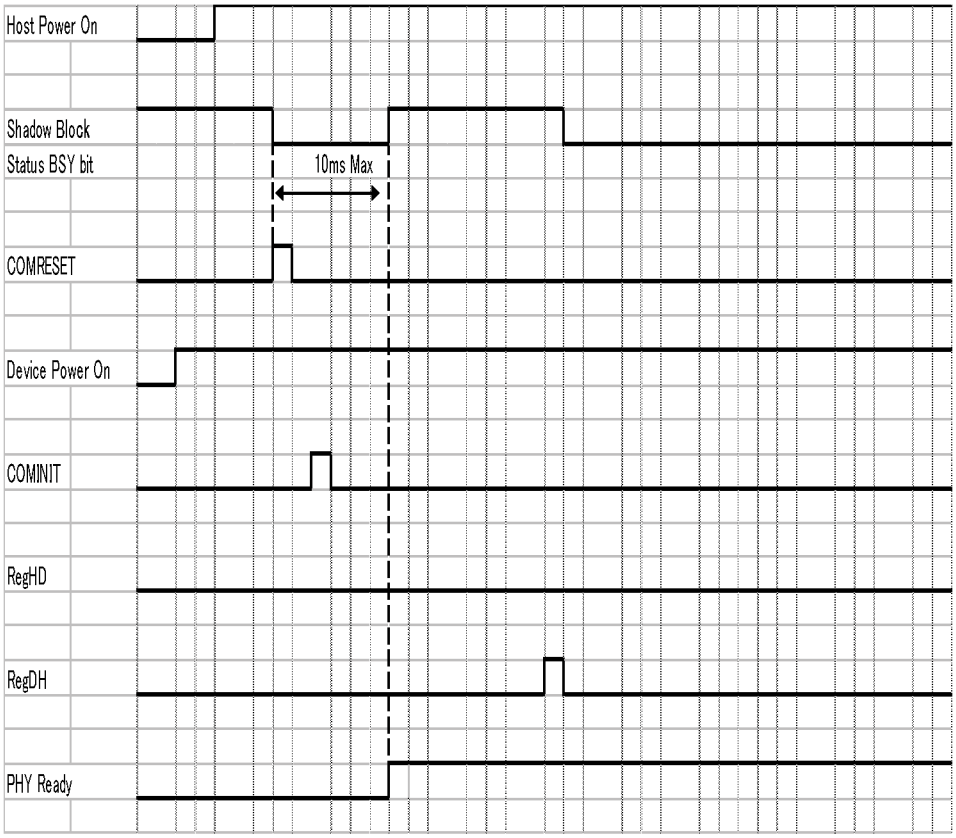


Figure 6.2 Response to power-on (when the device is powered on earlier than the host)

6.1.2 Response to COMRESET

The response to COMRESET is almost the same as the response when power is turned on and a power-on reset is then cancelled. The device establishes communication with the SATA interface (PHY Ready) and sends the Register DH FIS (STS = 50h) to notify the host that the device is ready. Then, the COMRESET sequence is completed.

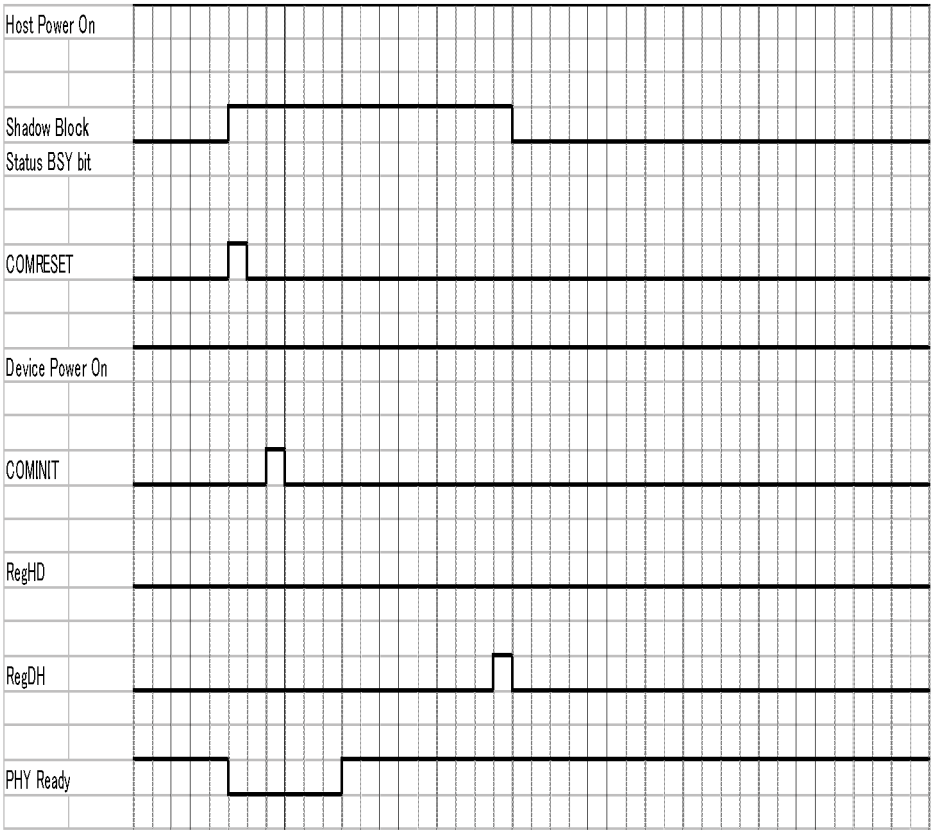


Figure 6.3 Response to COMRESET

6.1.3 Response to a software reset

When a software reset is accepted, the device performs a self-diagnosis, and it sends the Register DH FIS (STS = 50h) to notify the host that the device is ready. Then, the software reset sequence is completed.

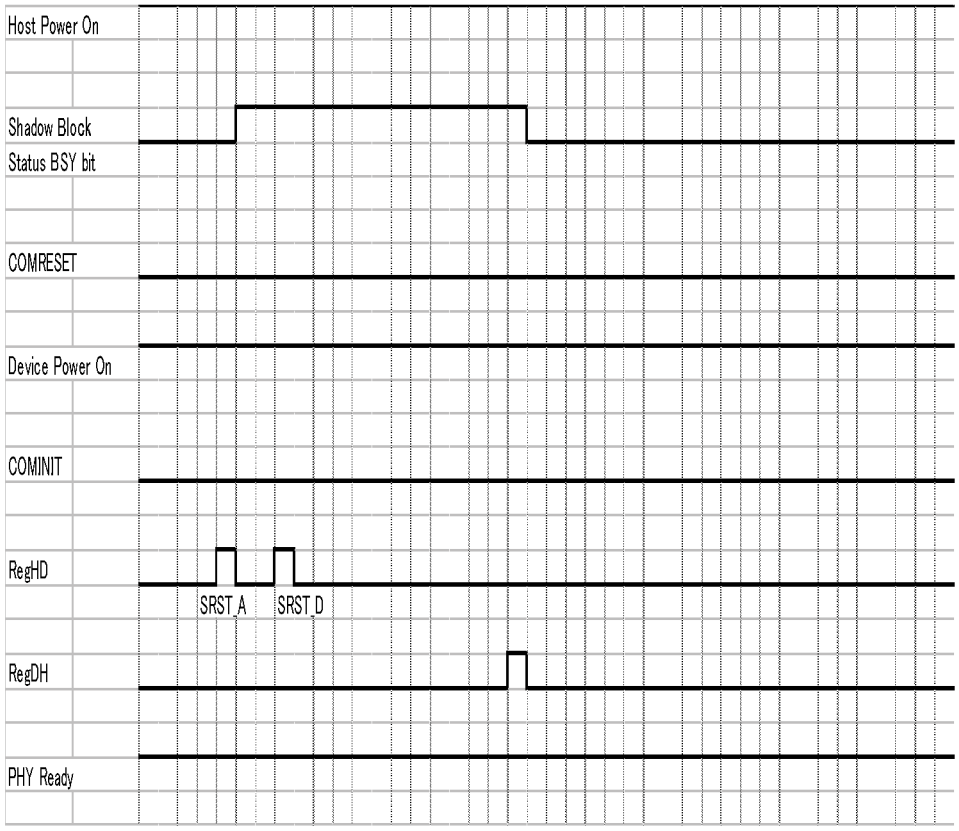


Figure 6.4 Response to a software reset

6.2 Power Save

The host can change the power consumption state of the device by issuing a power command to the device.

6.2.1 Power save mode

There are five types of power consumption state of the device including active mode where all circuits are active.

- Active mode
- Active idle mode
- Low power idle mode
- Standby mode
- Sleep mode

The device enters the active idle mode by itself. The device also enters the idle mode in the same way after power-on sequence is completed. The subsequent mode transition changes depending on the APM setting.

(1) Active mode

In this mode, all the electric circuit in the device are active or the device is under seek, read or write operation.

A device enters the active mode under the following conditions:

- The media access system is received.

(2) Active idle mode

In this mode, circuits on the device is set to power save mode.

The device enters the Active idle mode under the following conditions:

- After completion of the command execution other than SLEEP and STANDBY commands.

(3) Low power idle mode

Sets circuits on the device to the power save mode. The heads are disabled in the safe state.

The device enters the low power mode under the following conditions:

- After certain amount of time has elapsed in the active idle state (APM Mode 0, Mode 1 and Mode 2)
- Upon completion of the power-on sequence

- Upon receipt of a COMRESET
- Upon receipt of Idle/Idle Intermediate

(4) Standby mode

In this mode, the spindle motor has stopped from the low power idle state.

The device can receive commands through the interface. However if a command with disk access is issued, response time to the command under the standby mode takes longer than the active, active idle, or low power idle mode because the access to the disk medium cannot be made immediately.

The drive enters the standby mode under the following conditions:

- A STANDBY or STANDBY IMMEDIATE command is issued.
- A certain amount of time has elapsed in the low power idle state. (APM Mode 2)
- The time specified by the STANDBY or IDLE command has elapsed after completion of the command.
- A reset is issued in the sleep mode.

When one of following commands is issued, the command is executed normally and the device is still stayed in the standby mode.

- Reset (hardware or software)
- STANDBY command
- STANDBY IMMEDIATE command
- INITIALIZE DEVICE PARAMETERS command
- CHECK POWER MODE command

(5) Sleep mode

The power consumption of the drive is minimal in this mode. The drive enters only the standby mode from the sleep mode. The only method to return from the standby mode is to execute a software or COMRESET.

The drive enters the sleep mode under the following condition:

- A SLEEP command is issued.

In this mode, the device does not accept the command. (It is ignored.)

6.2.2 Power commands

The following commands are available as power commands.

- IDLE
- IDLE IMMEDIATE
- STANDBY
- STANDBY IMMEDIATE
- SLEEP
- CHECK POWER MODE
- SET FEATURES (APM setting)

6.3 Interface Power Save

The host system can change the power consumption status of the interface by issuing the PARTIAL or SLUMBER request to the device.

6.3.1 Power save mode of the interface

The interface power consumption states of this device can be separated into the following three modes, including the Active mode where the device is in the active state:

- Active mode
- Partial mode (shallow Interface Power Down)
- Slumber mode (deep Interface Power Down)

* The relationship of amount of power consumption in each mode is: Active mode > Partial mode > Slumber mode. The following table specifies a rule about the period in which the device must switch to Active mode from the Interface Power Down state:

	Period in which the device must switch to Active mode
Partial mode	Maximum 10 μs
Slumber mode	Maximum 10 ms

(1) Active mode

The interface is in the Active state and commands can be accepted.

(2) Partial mode

In this mode, (shallow) Power Save mode is set for the interface circuit.

The device switches to Partial mode when the following occurs:

- The device receives the PMREQ_P signal from the host and responds with the PMACK signal
- The device sends the PMREQ_P signal and the host responds with PMACK signal.

The device cannot switch to Partial mode if the following condition is satisfied:

- The device responds with the PMNAK signal because it is not waiting for commands.

The device returns to Active mode from Partial mode when the following condition is satisfied:

- The device receives the COMRESET or ComWake signal from the host.

(3) Slumber mode

In this mode, the (deep) Power Save mode is set for the interface circuit.

The device switches to Slumber mode when the following occurs:

- The device receives the PMREQ_P signal from the host and responds with the PMACK signal
- The device sends the PMREQ_S signal and the host responds with PMACK signal.

The device cannot switch to Slumber mode if the following condition is satisfied:

- The device responds with the PMNAK signal because it is not waiting for commands.

The device returns to Active mode from Slumber mode when the following condition is satisfied:

- The device receives the COMRESET or ComWake signal from the host.

6.4 Read-ahead Cache

Read-ahead Cache is the function for automatically reading data blocks upon completion of the read command in order to read data from disk media and save data block on a data buffer.

If a subsequent command requests reading of the read-ahead data, data on the data buffer can be transferred without accessing the disk media. As the result, faster data access becomes possible for the host.

6.4.1 Data buffer structure

This device contains a data buffer. This buffer is divided into two areas: one area is used for MPU work, and the other is used as a read cache for another command. (See Figure 6.5)

8MB buffer

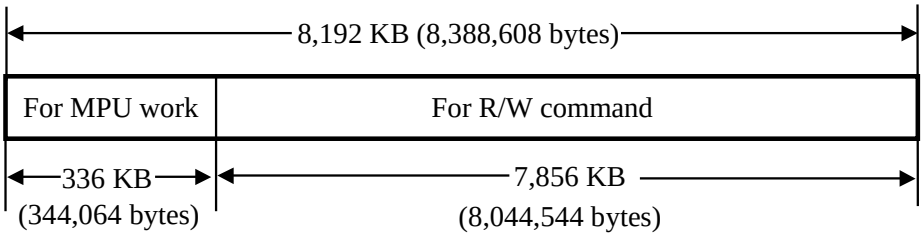


Figure 6.5 Data buffer structure

The read-ahead operation is done by the following commands.

- READ SECTOR (s) (EXT)
- READ MULTIPLE (EXT)
- READ DMA (EXT)
- READ FP DMA QUEUED

6.4.2 Caching operation

The caching operation is performed only when the commands listed below are received. If any of the following data are stored on the data buffer, the data is sent to the host system.

- All of the sector data that this command processes.
- A part of the sector data including the start sector, that this command processes.

If part of the data to be processed is stored on the data buffer, the remaining data is read from disk media and sent to the host system.

(1) Commands that are targets of caching

The commands that are targets of caching are as follows:

- READ SECTOR (S) (EXT)
- READ MULTIPLE (EXT)
- READ DMA (EXT)
- READ FP DMA QUEUED

However, if the caching function is prohibited by the SET FEATURES command, the caching operation is not performed.

(2) Data that is a target of caching

The data that is a target of caching are as follows:

1) Read-ahead data that is read from disk media and saved to the data buffer upon completion of execution of a command that is a target of caching.
2) Pre-read data that is read from disk media and saved to the data buffer before execution of a command that is a target of caching.
3) Data required by a command that is a target of caching and has been sent to the host system one. If the sector data requested by the host has not been completely stored in the read cache portion of the buffer, this data does not become a target of caching. Also, If sequential hits occur continuously, the caching-target data required by the host becomes invalid because that data is overwrited by new data.

(3) Invalidating caching-target data

Data that is a target of caching on the data buffer is invalidated under the following conditions:

1)-1 Any command other than the following commands is issued. (All caching-target data is invalidated.)

READ LONG

READ BUFFER

WRITE LONG

WRITE BUFFER

RECALIBRATE

FORMAT TRACK

SET FEATURES

SECURITY ERASE UNIT

DEVICE CONFIGURATION

DOWNLOAD MICROCODE

UNSUPPORT COMMAND (INVALID COMMAND)

1)-2 Commands that partially invalidate caching data

READ DMA/READ MULTIPLE/READ SECTOR(S)

READ DMA EXT/READ MULTIPLE EXT/READ SECTOR(S) EXT

READ FP DMA QUEUED

WRITE DMA/WRITE MULTIPLE/WRITE SECTOR(S)

WRITE DMA EXT/WRITE MULTIPLE EXT/WRITE SECTOR(S) EXT

WRITE DMA FUA EXT/WRITE MULTIPLE FUA EXT

WRITE FP DMA QUEUED

SMART

2) A COMRESET is issued or the power is turned off.

3) When HOST CRC ERROR has occurred.

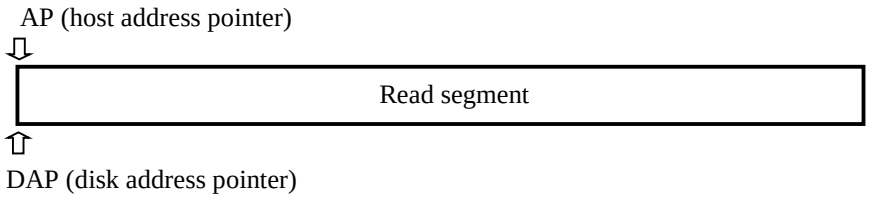
6.4.3 Using the read segment buffer

Methods of using the read segment buffer are explained for following situations.

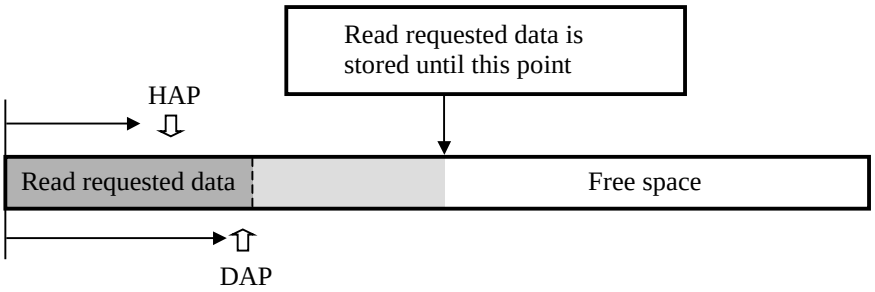
6.4.3.1 Miss-hit

In this situations, the top block of read requested data is not stored at all in the data buffer. As a result, all of the read requested data is read from disk media.

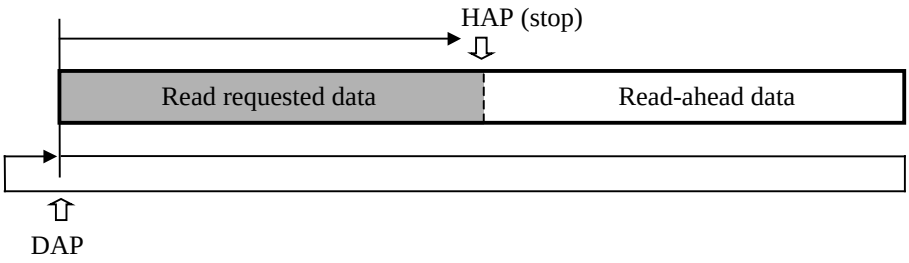
1) HAP (host address pointer) and DAP (disk address pointer) are defined in the head of the segment allocated from Buffer. (If pre-read is executed, HAP is set at the requested data reading position.)



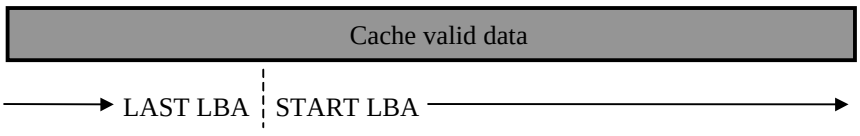
2) During reading of read requested data, the request data that has already been read is sent to the host system.



3) When reading of read requested data is completed and transfer of the read requested data to the host system is completed, reading of the disk continues until a certain amount of data is stored.



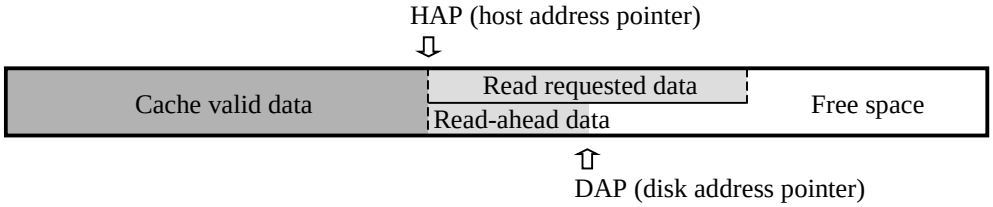
4) The following cache valid data is for the read command that is executed next:



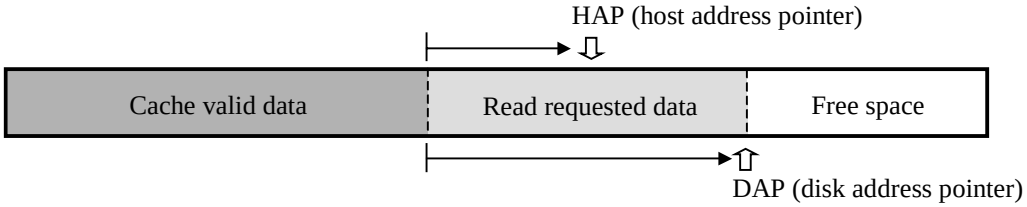
6.4.3.2 Sequential hit

When the read command that is targeted at a sequential address is received after execution of the read commands is completed, the read command transmits the Read requested data to the host system continuing read-ahead without newly allocating the buffer for read.

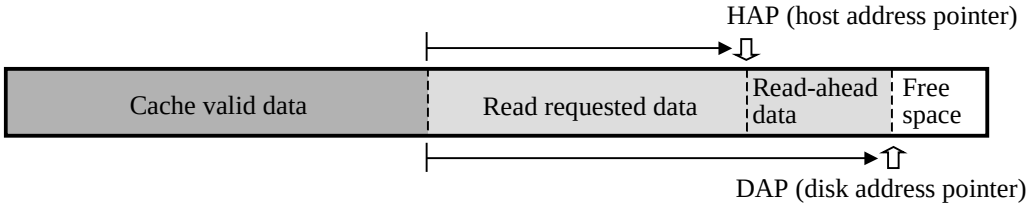
1) When the sequential read command is received, HAP is set in the sequential address of the last read command, and DAP is set at a present read position as it is.



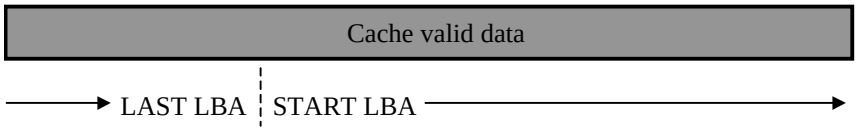
2) During reading of read requested data, the request data that has already been read is sent to the host system.



3) When reading of read requested data is completed and transfer of the read requested data to the host system is completed, the read-ahead operation continues until a certain amount of data is stored.



4) The following cache valid data is for the read command that is executed next:

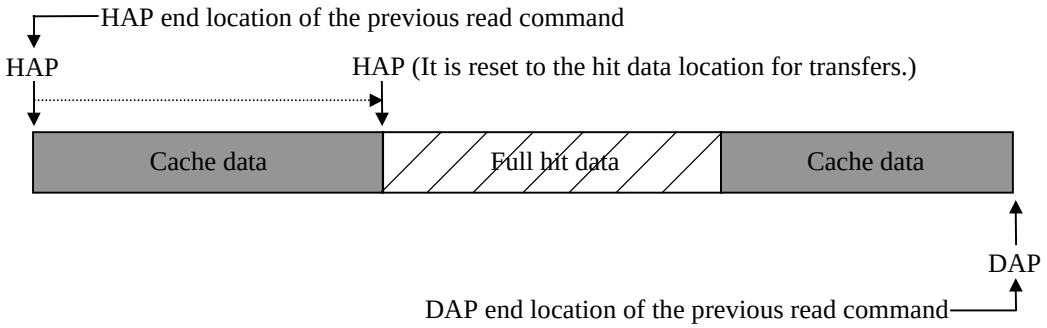


6.4.3.3 Full hit

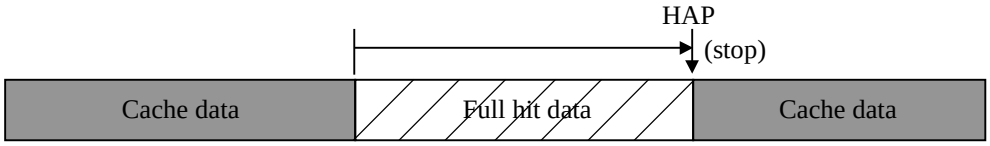
In this situation, all read requested data is stored in the data buffer. Transfer of the read requested data is started from the location where hit data is stored. For

data that is a target of caching and remains before a full hit, the data is retained when execution of the command is completed. This is done so that a new read-ahead operation is not performed. If the full hit command is received during the read-ahead operation, a transfer of the read requested data starts while the read-ahead operation is in progress.

1) An example is the state shown below where the previous read command is executing sequential reading. First, HAP is set at the location where hit data is stored.



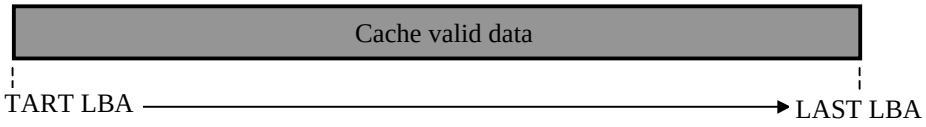
2) The read requested data is transferred, and a new read-ahead operation is not performed.



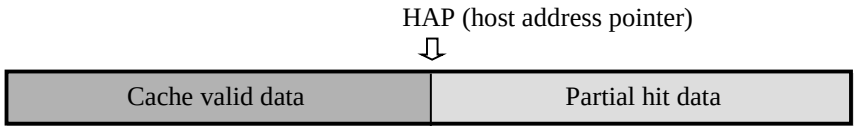
6.4.3.4 Partial hit

In this situation, a part of read requested data including the top sector is stored in the data buffer. A transfer of the read requested data starts from the address where the data that is hit is stored until the top sector of the read requested data. Remaining part of insufficient data is read then.

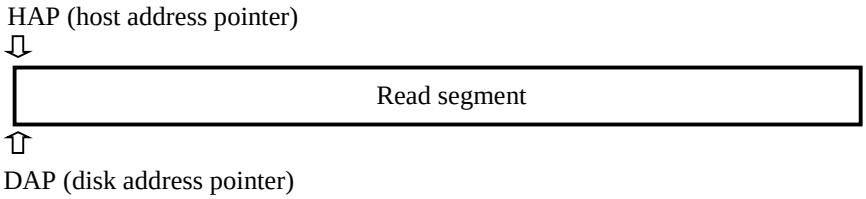
An example is a case where a partial hit occurs in cache data, as shown below.



1) HAP is set at the address where partial hit data is stored, and Transfer is started.

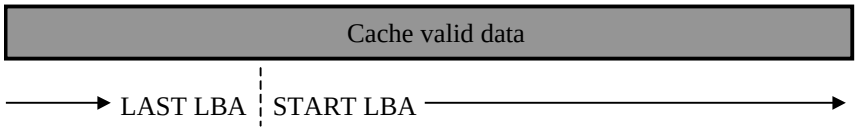


2) DAP and HAP are set at the head of Buffer newly allocated, and insufficient data is read.



3) When reading the read requested data ends and the transmission of the read requested data to the host system ends, the read-ahead operation continues until a certain amount of data is stored.

   The method of storing the read-ahead data at Partial hit is the same as the Miss hit.



6.5 Write Cache

Write Cache is the function for reducing the command processing time by separating command control to disk media from write control to disk media. When Write Cache is permitted, the write command can be keep receiving as long as the space available for data transfers remains free on the data buffer. Because of this function, command processing appears to be completed swiftly from the viewpoint of the host. It improves system throughput.

6.5.1 Cache operation

(1) Command that are targets of caching

The Commands that are targets of caching are as follows:

- WRITE SECTOR(S) (EXT)
- WRITE MULTIPLE (EXT) (FUA)
- WRITE DMA (EXT) (FUA)
- WRITE FP DMA QUEUED

However, the caching operation is not performed when the caching function is prohibited by the SET FEATURES command.

(2) Invalidation of cached data

If an error occurs during writing onto media, write processing is repeated up to as many times as specified for retry processing. If retry fails for a sector because the retry limit is reached, automatic alternate sector processing is executed for the sector. If the automatic alternate sector processing fails, the data in the sector for which automatic alternate sector processing failed is invalidated without being guaranteed.

Moreover, when the command (clause 6.4.2(3)) is accepted and HOST CRC Error is generated, the cashing data is invalidated.

<Exception>

- If a COMRESET, a software reset or command is received while a transfer of one sector of data is in progress, data is not written in the sector of the media where the interruption occurred, and sectors accepted before interruption occurred is written in the medium.

(3) Status report in the event of an error

The status report concerning an error occurring during writing onto media is created when the next command is issued. Where the command reporting the error status is not executed, only the error status is reported. Only the status of an error that occurs during write processing is reported.

<Exceptions>

The error status is not reported in the following case:

- The COMRESET or software reset is received after an error has occurred during writing to media.
  → The COMRESET or software reset processing is performed as usual. The error status that has occurred during writing to media is not reported.

(4) Enabling and disabling

Enabling and disabling of the Write Cache function can be set only with the SET FEATURES command. The setting does not changed even when the error status is reported.

The initial setting is stored in the system area of media. System area information is loaded whenever the power is turned on.

(5) COMRESET and software reset response

When a COMRESET or software reset is received while cached data is stored on the data buffer, data of the data buffer is written on the media, and reset processing is then performed. This is true for both a hard reset and soft reset.

(6) Cashing function when power supply is turned on

The cashing function is invalid until Calibration is done after the power supply is turned on.(about 10 sec) It is effective in Default after that as long as the cashing function is not invalidly set by the SET FEATURES command.

IMPORTANT

If Write Cache is enabled, there is a possibility that data transferred from the host with the Write Cache enable command is not completely written on disk media before the normal end interrupt is issued.

If an unrecoverable error occurs while multiple commands that are targets of write caching are received, the host has difficulty determining which command caused the error. (An error report is not issued to the host if automatic alternating processing for the error is performed normally.) Therefore, the host cannot execute a retry for the unrecoverable error while Write Cache is enabled. Be very careful on this point when using this function.

If a write error occurs, an abort response is sent to all subsequent commands.

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Glossary

Actuator

Head positioning assembly. The actuator consists of a voice coil motor and head arm. If positions the read-write (R-W) head.

AT bus

A bus between the host CPU and adapter board

ATA (AT Attachment) standard

The ATA standard is for a PC AT interface regulated to establish compatibility between products manufactured by different vendors. Interfaces based on this standard are called ATA interfaces.

BIOS standard for drives

The BIOS standard collectively refers to the parameters defined by the host, which, for example, include the number of cylinders, the number of heads, and the number of sectors per track in the drive. The physical specifications of the drive do not always correspond to these parameters.

The BIOS of a PC AT cannot make full use of the physical specifications of these drivers. To make the best use of these drives, a BIOS that can handle the standard parameters of these drives is required.

Command

Commands are instructions to input data to and output data from a drive. Commands are written in command registers.

Data block

A data block is the unit used to transfer data. A data block normally indicates a single sector.

DE

Disk enclosure. The DE includes the disks, built-in spindle motor, actuator, heads, and air filter. The DE is sealed to protect these components from dust.

MTBF

Mean time between failures. The MTBF is calculated by dividing the total operation time (total power-on time) by the number of failures in the disk drive during operation.

MTTR

Mean time to repair. The MTTR is the average time required for a service person to diagnose and repair a faulty drive.

PIO (Programmed input-output)

Mode to transfer data under control of the host CPU

Positioning

Sum of the seek time and mean rotational delay

Power save mode

The power save modes are idle mode, standby mode, and sleep mode.

In idle mode, the drive is neither reading, writing, nor seeking data. In standby mode, the spindle motor is stopped and circuits other than the interface control circuit are sleeping. The drive enters sleep mode when the host issues the SLEEP command.

Reserved

Reserved bits, bytes, and fields are set to zero and unusable because they are reserved for future standards.

Rotational delay

Time delay due to disk rotation. The mean delay is the time required for half a disk rotation. The mean delay is the average time required for a head to reach a sector after the head is positioned on a track.

Seek time

The seek time is the time required for a head to move from the current track to another track. The seek time does not include the mean rotational delay.

Status

The status is a piece of one-byte information posted from the drive to the host when command execution is ended. The status indicates the command termination state.

VCM

Voice coil motor. The voice coil motor is excited by one or more magnets. In this drive, the VCM is used to position the heads accurately and quickly.

Acronyms and Abbreviations

A

ABRT	Aborted command
AIC	Automatic idle control
AMNF	Address mark not found
ATA	AT attachment
AWG	American wire gage

B

BBK	Bad block detected
BIOS	Basic input-output system

C

CORR	Corrected data
CH	Cylinder high register
CL	Cylinder low register
CM	Command register
CSR	Current sense register
CSS	Current start/stop
CY	Cylinder register

D

dBA	dB A-scale weighting
DE	Disk enclosure
DH	Device/head register
DRDY	Drive ready
DRQ	Ddata request bit
DSC	Drive seek complete
DWF	Drive write fault

E

ECC	Error checking and correction
ER	Error register
ERR	Error

F

FR	Feature register

H

HA	Host adapter
HDD	Hard disk drive

I

IDNF	ID not found
IRQ14	Interrupt request 14

L

LED	Light emitting diode

M

MB	Mega-byte
MB/S	Mega-byte per seconds
MPU	Micro processor unit

P

PCA	Printed circuit assembly
PIO	Programmed input-output

R

RLL	Run-length-limited

S

SA	System area
SC	Sector count register
SG	Signal ground
SN	Sector number register
ST	Status register

T

TPI	Track per inches
TRONF	Track 0 not found
Typ	Typical

U

UNC	Uncorrectable ECC error

V

VCM	Voice coil motor

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We would appreciate your comments and suggestions regarding this manual.

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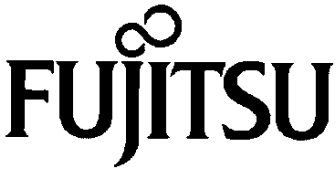
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