Intel® IXP43X Product Line of Network Processors

Hardware Design Guidelines

April 2007

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Revision History

Date	Revision	Description
April 2007	001	Initial release

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1.0 Introduction

This design guide provides recommendations for hardware and system designers who are developing with the Intel® IXP43X Product Line of Network Processors. This document should be used in conjunction with the *Intel® IXP43X Product Line of Network Processors Datasheet* and sample schematics provided for the Intel® IXP435 Multi-Service Residential Gateway Reference Platform.

Design recommendations are necessary to meet the timing and signal quality specifications. The guidelines recommended in this document are based on experience and simulation work done at Intel while developing the Intel® IXP435 Multi-Service Residential Gateway Reference Platform. These recommendations are subject to change.

Note: This document discusses all features supported on the IXP43X product line of network processors. A subset of these features is supported by certain processors in the IXP43X network processors, such as the Intel® IXP432 Network Processor. Refer to the *Intel® IXP43X Product Line of Network Processors Datasheet* for detailed information on various features listed by processor.

1.1 Content Overview

Chapter Name	Description
Chapter 1.0, “Introduction”	Conventions used in this manual and related documentation
Chapter 2.0, “System Architecture”	System architectural block diagram and system memory map
Chapter 3.0, “General Hardware Design Considerations”	Graphical representation of most common peripheral interfaces
Chapter 4.0, “General PCB Guide”	General PCB design practice and layer stack-up description
Chapter 5.0, “General Layout and Routing Guide”	More specific layout and routing recommendations for board designers
Chapter 6.0, “PCI Interface Design Considerations”	Board-design recommendations when implementing PCI interface
Chapter 7.0, “DDRII / DDRI SDRAM”	Board-design recommendations when implementing DDRII/I memory interface

1.2 Related Documentation

The reader of this design guide should also be familiar with the material and concept presented in the following documents:

Title	Document #
Intel® IXP43X Product Line of Network Processors Datasheet	316842
Intel® IXP43X Product Line of Network Processors Developer's Manual	316843
Intel® IXP43X Product Line of Network Processors: Migrating from the Intel® IXP42X Product Line	316845
Intel® IXP400 Software Programmer's Guide	252539
Intel® IXP400 Software Specification Update	273795
Intel® XScale™ Core Developer's Manual	273473
Intel StrataFlash® *Embedded Memory (P30) Application Note*	__
Intel XScale® Microarchitecture Technical Summary	—
Double Data Rate (DDR) SDRAM Specification, 2004; JEDEC Solid State Technology Association	JESD79D
IEEE 802.3 Specification	N/A
PCI Local Bus Specification, Rev. 2.2	N/A
Universal Serial Bus Specification, Revision 2.0	N/A
UTOPIA Level 2 Specification, Revision 1.0	N/A

1.3 Acronyms

Table 1 lists the acronyms and abbreviations used in this guide.

Table 1. List of Acronyms and Abbreviations (Sheet 1 of 2)

Term	Explanation
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
ATM	Asynchronous Transfer Mode
DDR	Double Data Rate
EMI	Electro-Magnetic Interference
GPIO	General Purpose Input/Output
HSS	High Speed Serial
IP	Internet Protocol
ISA	Instruction Set Architecture
LAN	Local Area Network
MII	Media-Independent Interface
NPE	Network Processor Engine
PCB	Printed Circuit Board
PCI	Peripheral Component Interface
PHY	Physical Layer Interface
PLL	Phase-Locked Loop

Table 1. List of Acronyms and Abbreviations (Sheet 2 of 2)

Term	Explanation
PMU	Performance Monitoring Unit
SME	Small-to-Medium Enterprise
SSP	Synchronous Serial Protocol
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
VTT	Termination Voltage Supply

1.4 Overview

The Intel® IXP43X Product Line of Network Processors is a highly integrated device, capable of interfacing with most common industry standard peripherals, required for high-performance control applications.

Note: This document discusses all features supported on the IXP43X network processors. Refer to the *Intel® IXP43X Product Line of Network Processors Datasheet* for details on feature support listed by processor.

Some of the key features of the IXP43X network processors, when used as a single-chip solution for embedded applications are as follows:

- Intel XScale® Processor (compliant with Intel® StrongARM* architecture) up to 667 MHz
- 32-bit PCI interface Master/Target 33 MHz
- Two Universal Serial Bus (USB) V2.0 Host Controller
- DDRI-266 SDRAM or DDRII-400 SDRAM—
  - — Support for 16 MB, minimum for DDR II/I, 32 MB minimum for DDRII-400; 1 GB, maximum for DDR II/I, 512 MBs maximum for DDRII-400
  - — User-enabled ECC.
- 16bit Data / 24bit Address Expansion Bus Interface
- One UART interface
- Two NPEs
- UTOPIA Level 2 Interface
- Synchronous Serial Port Interface (SSP)
- One High-Speed Serial Port Interfaces (HSS)
- Network interfaces that can be configured in the following manner: **Note 1**
  - — Two MII interfaces
  - — One MII interface + 1 UTOPIA Level 2 interface
- MII interfaces are: **Note 1**
  - — 802.3 MII interfaces
  - — Single MDIO interface to control the MII interfaces
- UTOPIA Level 2 Interface is: **Note 1**
  - — Eight-bit interface
  - — Up to 33-MHz clock speed
  - — Five transmit and five receive address lines

- 16 GPIO (General Purpose Input Output)
- Packaging
  - — 460-pin PBGA
  - — 31 mm by 31 mm
  - — Commercial temperature (0° to 70° C)
  - — Lead free support

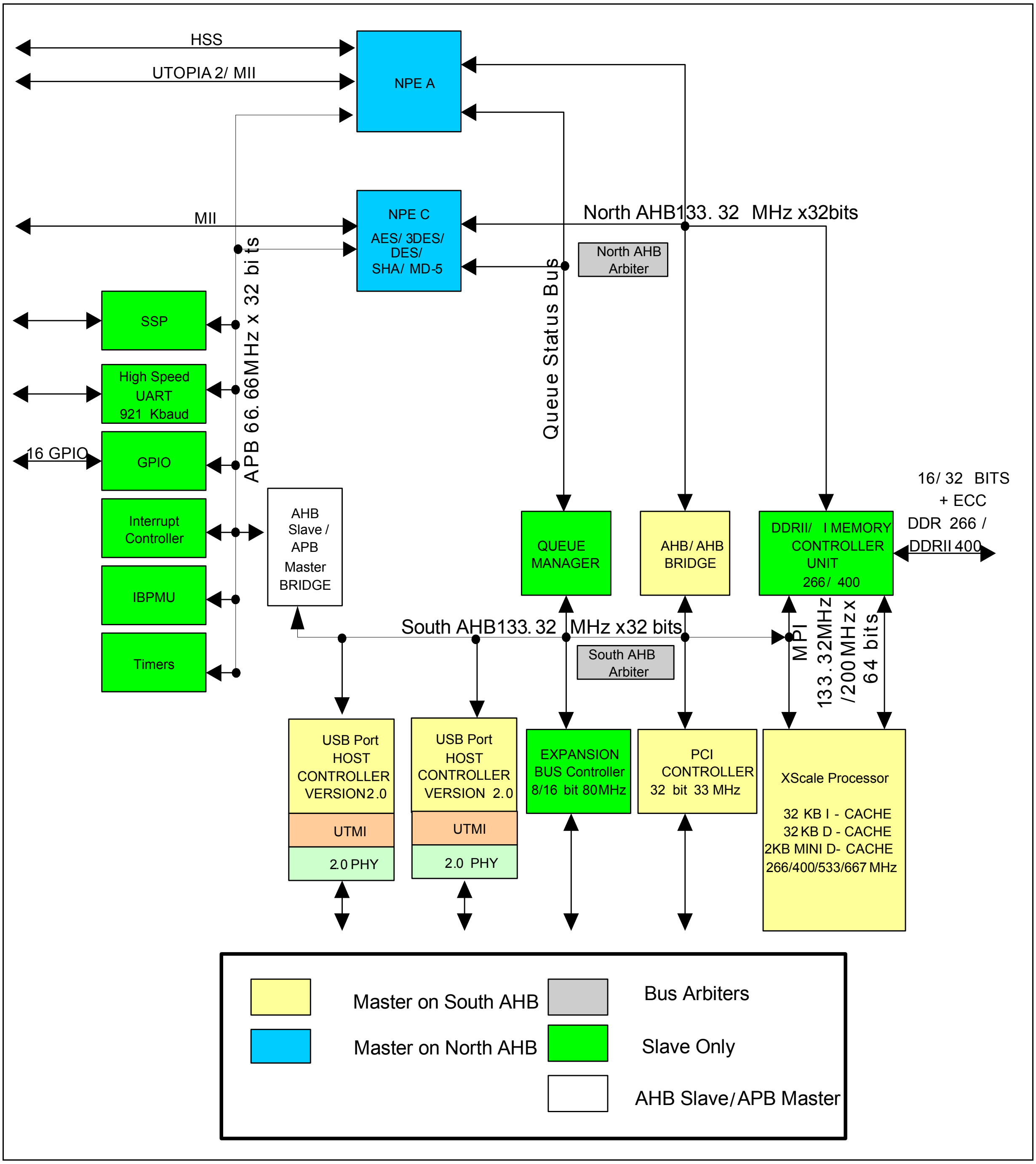
Refer to the *Intel® IXP43X Product Line of Network Processors Datasheet* for complete feature list and block diagram description.

Note:

1. This feature requires Intel-supplied software. To determine if this feature is enabled in a particular software release, refer to the *Intel® IXP400 Software Programmer's Guide*.

A block diagram of all major internal hardware components of IXP43X network processors is shown in Figure 1. The illustration also shows how the components interface with each other through the various bus interfaces such as the North AHB, South AHB, and APB.

Figure 1. Intel® IXP435 Network Processor Block Diagram



Note: Figure 1 shows the Intel® IXP435 Network Processor. For details on feature and SKU support listed by processor, see the *Intel® IXP43X Product Line of Network Processors Datasheet*.

1.5 Typical Applications

- SOHO-Small Business/Residential
- Modular Router
- Wireless Gateway(802.11a/b/g)
- Network-Attached Storage
- Wired/Wireless RFID Readers
- Digital Media Adapter
- Digital Media Player
- VoIP Router
- Video Phone
- Secure Gateway/Router
- Network Printer
- Wireless Media Gateway
- IP Set Top box

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2.0 System Architecture

2.1 System Architecture Description

The Intel® IXP43X Product Line of Network Processors is a multifunction processor that integrates the Intel XScale® Processor (ARM* architecture compliant) with highly integrated peripheral controllers and network processor engines.

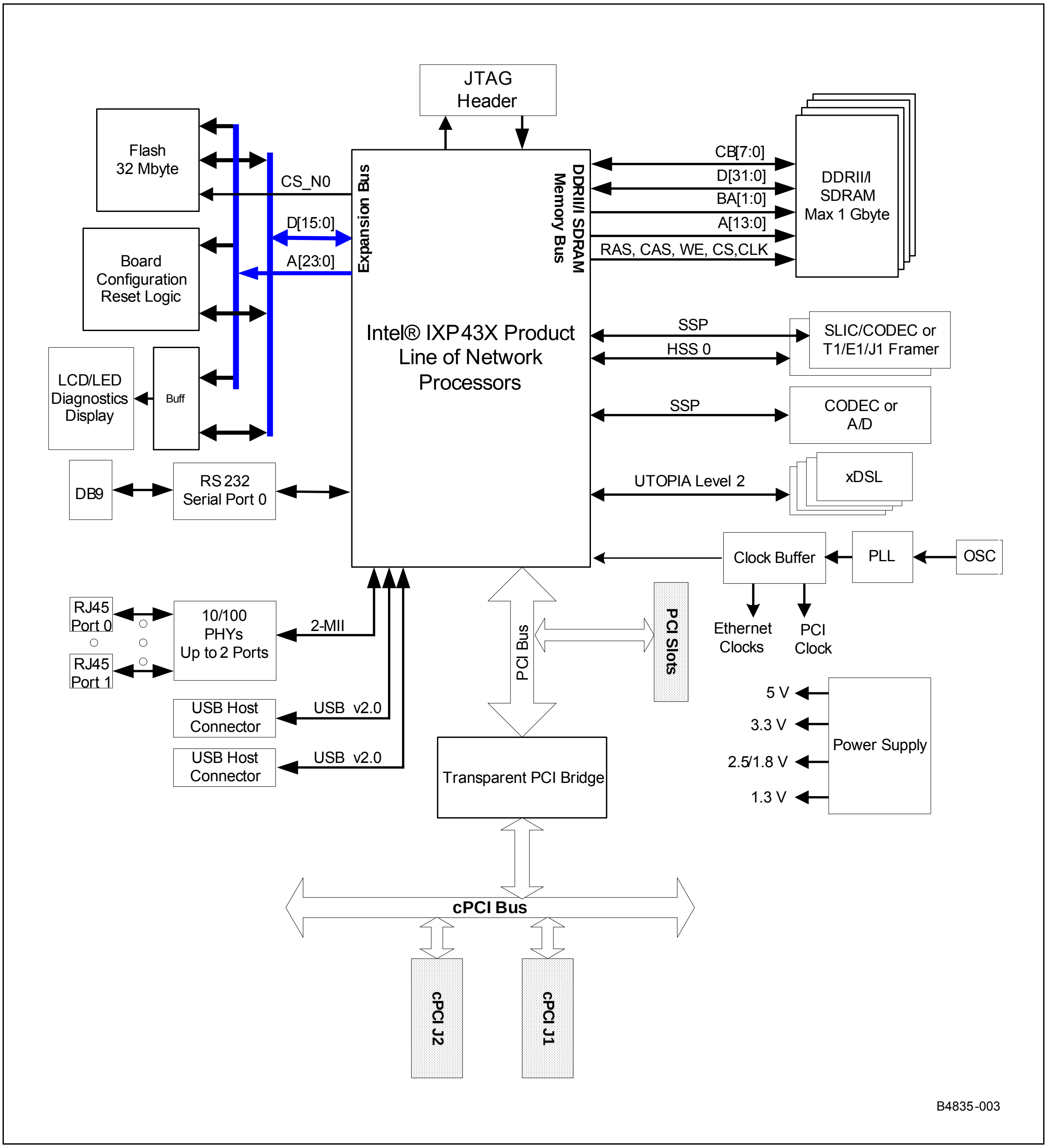
The processor is a highly integrated design, manufactured with Intel's 0.13-µm production semiconductor process technology. This process technology, along with numerous, dedicated function peripheral interfaces and many features with the Intel XScale processor, addresses the needs of many system applications and helps reduce system costs. The processors can be configured to meet many system application and implementation needs.

Figure 2 illustrates one of the many applications for which the IXP43X network processors can be implemented. For detailed functional description, see the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

2.2 System Memory Map

Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for a complete memory map and register description of each individual module.

Figure 2. Example: Intel® IXP43X Product Line of Network Processors System Block Diagram



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3.0 General Hardware Design Considerations

This chapter contains information for implementing and interfacing with major hardware blocks of the Intel® IXP43X Product Line of Network Processors. Such blocks include DDRII/I SDRAM, Flash, Ethernet PHYs, UART and other peripherals interfaces. Signal definition tables list resistor recommendations for pull-ups and pull-downs.

Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected. Features enabled by a specific part number and required to be Soft Fuse-disabled, only require pull-ups or pull-downs in the **clock-input signals.** Other conditions can require pull-up or pull-down resistors for configuration purposes at power on or reset. In the same way, open-drain outputs must be pulled high.

Warning: With the exception of USB_V5REF all other I/O pins of the IXP43X network processors are not 5.0-V tolerant.

Table 2 gives the legend for interpreting the **Type** field used in the signal-definition tables that are covered in this chapter.

Table 2. Signal Type Definitions

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be an input or output
OD	Open-drain pin
TRI	Tri-State pin
PWR	Power pin
GND	Ground pin

3.1 Soft Fusible Features

Soft Fuse Enable/Disable is a method to enable or disable features in hardware, virtually disconnecting the hardware modules from the processor.

Some of the features offered in the IXP43X product line of network processors can be Soft Fuse Enabled/Disabled during boot. It is recommended that if a feature is not used in the design, the feature be soft disabled. This helps reduce power and maintain the part running at a cooler temperature. When Soft Fuse Disabled, a pull-up resistor must be connected to each clock input pins of the disabled feature interface. All other signals can be left unconnected.

Soft Fuse Enable/Disable can be done by writing to EXP_UNIT_FUSE_RESET register. For more information refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* and review the register description.

Table 3. Soft Fusible Features (Sheet 1 of 2)

Name	Description
PCI	The complete bus must be enabled or disable.
HSS0	Can only be disable as a pair.
UTOPIA	while enabling UTOPIA, MACs on NPE A is disabled. while enabling MACs on NPE A, UTOPIA is disabled.

Table 3. Soft Fusible Features (Sheet 2 of 2)

Name	Description
ETHERNET	Can enable MII MACs. Enable of MACs can be separately done per each NPE.
USB Host	Each USB can be Enable separately.
DDR ECC	ECC can be enabled or disabled separately from the rest of the DDR interface.

3.2 DDRII/I SDRAM Interface

The IXP43X network processors support unbuffered, DDRI-266 or DDRII-400 SDRAM technology, capable of addressing two memory banks (one bank per CS). Each bank can be configured to support 32/64/128/256/512-Mbyte for a total combined memory support of 1 Gbyte.

The IXP43X network processors integrate a high-performance, multi-ported Memory Controller Unit (MCU) to provide a direct interface with its local memory subsystem. The MCU supports:

- DDR II/I or DDRII-400 SDRAM
- 128/256/512-Mbit, 1-Gbit DDRI SDRAM technology support
- Supports 256/512-Mbit technologies for the DDRII-400
- Only unbuffered DRAM support (No registered DRAM support)
- Dedicated port for Intel XScale processor to the DDRII/DDRI SDRAM
- Between 32 MBs and 1-GB of 32-bit DDRI SDRAM
- Between 64MBs and 512 MBs of 32-bit DDRII SDRAM
- 16MB for 16-bit memory systems for DDRI SDRAM (non-ECC) supporting 128-Mbit technology only
- 32MB for 16-bit memory systems for DDRII SDRAM (non-ECC) supporting 256-Mbit technology only
- Single-bit error correction, multi-bit detection support (ECC)
- 32-bit, 40-bit wide memory interfaces (non-ECC and ECC support), and 16-bit wide memory interfaces (non-ECC)

The DDRII/DDRI SDRAM interface provides a direct connection to a high-bandwidth and reliable memory subsystem. The DDRII/DDRI SDRAM interface is a 16 or 32-bit-wide data path.

The device supports non-ECC and ECC for error correction, which can be enable or disable by software as required. Banks have a bus width of 32 bits for non ECC or 40 bits for ECC enable (32-bit data + 8-bit ECC).

An 8-bit Error Correction Code (ECC) across each 32-bit word improves system reliability. It is important to note that ECC is also referred to as CB in many DIMM specifications. The pins on the IXP43X network processors are called DDR_CB[7:0]. ECC is only implemented in the 32-bit mode of operation, while the algorithm used to generate the 8-bit ECC is implemented over 64-bit.

The ECC circuitry is designed to operate always on a 64-bit data and when operating in 32-bit mode, the upper 32 bits are driven to zeros internally. To summarize the impact to the customer, the full 8 bits of ECC is stored and read from a memory array for the ECC logic to work. An 8-bit-wide memory is used when implementing ECC.

The memory controller only corrects single bit ECC errors on read cycles. The ECC is stored into the DDRII/DDRI SDRAM array along with the data and is checked when the data is read. If the code is incorrect, the MCU corrects the data before reaching the initiator of the read. ECC error scrubbing is done with software. User-defined fault correction software is responsible for The value written back into the memory location contains the 32-bit word with the modified byte and the new ECC value.

Refer to the *Intel® IXP43X Product Line of Network Processors Datasheet* for a detailed list of features.

General DDRII/I SDRAM routing guidelines can be found in Section 7.3.3, "Routing Guidelines" on page 82. For more detailed information, see the PC266 and PC400 DDR SDRAM specification.

3.2.1 Signal Interface

Table 4. DDRII/I SDRAM Interface Pin Description (Sheet 1 of 2)

Name	Type Field	Device-Pin Connection	VTT Termination	Description
D_CK[2:0] / DDR_CK[2:0]	O	Connect a pair of differential clock signals to every device; When using both banks, daisy chain devices with same data bit sequence.	No	DDRII/I SDRAM Clock Out — Provides the positive differential clocks to the external SDRAM memory subsystem.
D_CK_N[2:0] / DDR_CK_N[2:0]	O	Same as above	No	DDRII/I SDRAM Clock Out — Provides the negative differential clocks to the external SDRAM memory subsystem.
D_CS_N[1:0] / C_CS_N[1:0]	O	Use the same CS to control 32-bit data + 8-bit ECC, per bank	Yes	Chip Select — Must be asserted for all transactions to the DDRII/I SDRAM device. One per bank.
D_RAS_N / DDR_RAS_N	O	The RAS signal must be connected to each device in a daisy chain manner	Yes	Row Address Strobe — Indicates that the current address on D_MA[13:0] / DDR_MA[13:0] is the row.
D_CAS_N / DDR_CAS_N	O	The CAS signal must be connected to each device in a daisy chain manner	Yes	Column Address Strobe — Indicates that the current address on D_MA[13:0] / DDR_MA[13:0] is the column.
D_WE_N / DDR_WE_N	O	The WE signal must be connected to each device in a daisy chain manner	Yes	Write Strobe — Defines whether or not the current operation by the DDRII/I SDRAM is to be a read or a write.
D_DM[4:0] / DDR_DM[4:0]	O	Connect to each DM device pin. For the 8-bit devices connect one DM signal per device. For the 16-bit devices connect two DM signal per device (depending on how many data bits are being used).	Yes	Data Bus Mask — Controls the DDRII/I SDRAM data input buffers. Asserting D_WE_N/ DDR_WE_N causes the data on D_DQ[31:0]/ DDR_DQ[31:0] and D_CB[7:0]/DDR_CB[7:0] to be written into the DDRII/I SDRAM devices. D_DM[4:0]/DDR_DM[4:0] controls this operation on a per-byte basis. D_DM[3:0]/ DDR_DM[3:0] are intended to correspond to each byte of a word of data. D/DM[4]/ DDR_DM[4] is intended to be utilized for the ECC byte of data.
D_BA[1:0] / DDR_BA[1:0]	O	The BA signals must be connected to each device in a daisy chain manner.	Yes	DDRII/I SDRAM Bank Selects — Controls which of the internal DDRII/I SDRAM banks to read or write. D_BA[1:0]/DDR_BA[1:0] are used for all technology types supported.
D_MA[13:0] / DDR_MA[13:0]	O	All address signals must be connected to each device in a daisy chain manner.	Yes	Address bits 13 through 0 — Indicates the row or column to access depending on the state of D_RAS_N/DDR_RAS_N and D_CAS_N/ DDR_CAS_N.
D_DQ[31:0] / DDR_DQ[31:0]	I/O	Must be connected in parallel to achieve a 32-bit bus width.	Yes	Data Bus — 32-bit wide data bus.

Table 4. DDRII/I SDRAM Interface Pin Description (Sheet 2 of 2)

Name	Type Field	Device-Pin Connection	VTT Termination	Description
D_CB[7:0] / DDR_CB[7:0]	I/O	Connect to ECC memory devices.	Yes	ECC Bus — Eight-bit error correction code which accompanies the data on D_DQ[31:0]/ DDR_DQ[31:0]. When ECC is disabled and not being used in a system design, these signals can be left un-connected.
D_DQS[4:0] / DDR_DQS[4:0]	I/O	Connect DQS[3:0] to devices with data signals and DQS[4] to devices with ECC signals.	Yes	Data Strobes Differential — Strobes that accompany the data to be read or written from the DDRII/I SDRAM devices. Data is sampled on the negative and positive edges of these strobes. D_DQS[3:0]/DDR_DQS[3:0] are intended to correspond to each byte of a word of data. D_DQS[4]/DDR_DQS[4] is intended to be utilized for the ECC byte of data.
D_CKE[1:0] / DDR_CKE[1:0]	O	Use one CKE per bank, never mix the CKE on the same bank. Use CKE[0] for bank0 and CKE[1] for bank1	Yes	Clock enables — One clock after D_CKE[1:0]/ DDR_CKE[1:0] is de-asserted, data is latched on D_DQ[31:0]/DDR_DQ[31:0] and D_CB[7:0]/DDR_CB[7:0]. Burst counters within DDRII/I SDRAM device are not incremented. De-asserting this signal places the DDRII/I SDRAM in self-refresh mode. For normal operation, D_CKE[1:0]/DDR_CKE[1:0] must be asserted.
D_ODT[1:0]				On Die Termination Control — Turns on DDR II SDRAM termination during writes.
D_RES[2:1]		Refer to Figure 27		Compensation for DDR OCD (analog) DDRII mode only. This function is not enable and special connection is required.
D_SLWCRES		Refer to Figure 27		Compensation Voltage Reference (analog) for DDR driver slew rate control connected through a resistor to D_CRES0.
D_IMPCRES		Refer to Figure 27		Compensation Voltage Reference (analog) for DDR driver impedance control connected through a resistor to D_CRES0.
D_CRES0	O	Tied off to a resistor	Tied off to a resistor	Analog VSS Ref Pin (analog) both D_SLWCRES and D_IMPCRES signals connect to this pin through a reference resistor. For DDRII/I respectively: - 285 / 387Ohm Resistor connected to DDR_IMPCRES used for process and temperature adjustments. - 825 / 845Ohm Resistor connected to DDR_SLWCRES used for process and temperature adjustments.
D_VREF / DDR_VREF	I	VCCDDR/2	VCCDDR/2	DDRII/IDDRII/I SDRAM Voltage Reference — is used to supply the reference voltage to the differential inputs of the memory controller pins.

3.2.2 DDRII/I SDRAM Initialization

For instructions on DDRII/I SDRAM initialization, refer to **DDR SDRAM Initialization** subsection in the Memory Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

3.3 Expansion Bus

The Expansion Bus of the IXP43X network processors is specifically designed for compatibility with Intel-and Motorola* style microprocessor interfaces.

The expansion bus controller includes a 24-bit address bus and a 16-bit wide data path, running at a maximum speed of 80 MHz from an external clock oscillator. The bus can be configure to support the following target devices:

- Intel multiplexed
- Intel StrataFlash®
- Motorola non multiplexed
- Intel non-multiplexed
- Synchronous Intel StrataFlash® Memory
- Motorola multiplexed

The expansion bus controller also has an arbiter that supports up to four external devices that can master the expansion bus. External masters can be used to access external slave devices that reside on the expansion bus, including access to internal memory mapped regions within the IXP43X network processors.

All supported modes are seamless and no additional glue logic is required. Other cycle types can be supported by configuring the Timing and Control Register for Chip Select.

The expansion interface functions support 8-bit or 16-bit data operation and allows an address range of 512 bytes to 16 MBs, using 24 address lines for each of the four independent chip selects.

Access to the expansion-bus interface is completed in five phases. Each of the five phases can be lengthened or shortened by setting various configuration registers on a per-chip-select basis. This feature allows the IXP43X network processors to connect to a wide variety of peripheral devices with varying speeds.The expansion interface supports Intel or Motorola* microprocessor style bus cycles. The bus cycles can be configured to be multiplexed address/data cycles or separate address/data cycles for each of the four chip-selects.

The expansion interface is an asynchronous interface to externally connected chips. A clock is supplied to the IXP43X network processors expansion interface for the interface to operate. This clock can be driven from GPIO 15 or an external source. Devices on the expansion bus can be clocked by an external clock at a rate of up to 80 MHz. If GPIO 15 is used as the clock source, the Expansion Bus interface can only be clocked at a maximum of 33.33 MHz. GPIO 15’s maximum clock rate is 33.33 MHz.

3.3.1 Signal Interface

Table 5. Expansion Bus Signal Recommendations (Sheet 1 of 2)

Name	Type Field	Pull Up Down	Recommendations
EX_CLK	I	No	Use series termination resistor, 10Ω to 33Ω at the source.
EX_ALE	TRI O	No	Use series termination resistor, 10Ω to 33Ω at the source.
EX_ADDR[23:0]	I/O	Yes	Use 470Ω resistors for pull-downs; required for boot strapping for initial configuration of Configuration Register 0. Pull-ups are not required as for when the system comes out of reset, all bits are initially set HIGH. For more details, see Table 6. For additional details on address strapping, see the *Intel® IXP43X Product Line of Network Processors Developer’s Manual*.
EX_WR_N	I/O	No	Use series termination resistor, 10Ω to 33Ω at the source.
EX_RD_N	I/O	No	Use series termination resistor, 10Ω to 33Ω at the source.

Table 5. Expansion Bus Signal Recommendations (Sheet 2 of 2)

Name	Type Field	Pull Up Down	Recommendations
EX_CS_N[3:0]	I/O	Yes	Use series termination resistor, 10Ω to 33Ω at the source. Use 10KΩ resistors pull-ups to ensure that the signal remains de-asserted.
EX_DATA[15:0]	I/O	No	Expansion-bus, bidirectional data.
EX_IOWAIT_N	I	Yes	Should be pulled high through a 10-KΩ resistor when *not* being utilized in the system.

3.3.2 Reset Configuration Straps

At power up or whenever RESET_IN_N is asserted, the Expansion-bus address outputs are switched to inputs and the state of the inputs are captured and stored in Configuration Register 0, bits 23 through 0. This occurs when PLL_LOCKED is de-asserted.

The strapping of Expansion-bus address pins can be done by placing external pull-down resistors at the required address pin. It is not required to use external pull-up resistors, by default upon reset all bits on Configuration Register 0 are set High, unless an external pull down is used to set them Low. For example to register a bit low or high in the Configuration Register 0, do the following:

Place an external 470Ω pull-down resistor to register a bit LOW in the Configuration Register 0.

No external pull-up is required; upon reset, bits are set high by default.

The state of the boot-strapping resistor is registered on the first cycle after the synchronous de-assertion of the reset signal. These bits can be read or written as needed for desired configurations. It is recommended that only Bit 31, Memory Map, be changed from 1 to 0 after execution of boot code from external flash.

Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for a complete bit description of Configuration Register 0.

Table 6. Boot/Reset Strapping Configuration (Sheet 1 of 2)

Name	Function	Description
EX_ADDR[23:21]	Intel XScale® Processor Clock Set[2:0]	Allow a slower Intel XScale® Processor clock speed to override device fuse settings. But cannot be used to over clock core speed. Refer to Table 7 for additional information.
EX_ADDR[20:17]	Customer	Customer-defined bits. (Might be used for board revision.)
EX_ADDR[16:12]	(Reserved)	(Reserved)
EX_ADDR[11]	DDR_MODE	DDRI or DDRII mode selection: 0 - DDRII mode (400MHz) 1 - DDRI mode (266MHz) DDR_mode or DDR clock speed selection bit is read only and strapped in from exp address bit 11 upon activation of reset_early_n and reset_cold_n.

Table 6. Boot/Reset Strapping Configuration (Sheet 2 of 2)

Name	Function	Description
EX_ADDR[10]	IOWAIT_CS0	1 = EX_IOWAIT_N is sampled during the read/write expansion bus cycles for Chip Select 0. 0 = EX_IOWAIT_N is ignored for read and write cycles to Chip select 0 if EXP_TIMING_CS0 is configured to Intel mode that is mentioned in *Intel® IXP43X Product Line of Network Processors Datasheet* and *Intel® IXP43X Product Line of Network Processors Developer's Manual.* Typically, IOWAIT_CS0 must be pulled down to Vss when attaching a Synchronous Intel StrataFlash® on Chip Select 0 since the default mode for EXP_TIMING_CS0 is Intel mode and EX_IOWAIT_N is an unknown value for Synchronous Intel StrataFlash. If the board does not connect the Synchronous Intel StrataFlash WAIT pin to EX_WAIT_N (and the board guarantees EX_IOWAIT_N is pulled up), the value of IOWAIT_CS0 is a don't-care, since EX_IOWAIT_N will not be asserted. When EXP_TIMING_CS0 is reconfigured to Intel Synchronous mode during boot-up (for synchronous Intel chips), the expansion bus controller ignores EX_IOWAIT_N during read and write cycles since the WAIT functionality is determined from the EXP_SYNCINTEL_COUNT and EXP_TIMING_CS registers.
EX_ADDR[9]	EXP_MEM_DRIVE	Refer to table found in EX_ADDR[5].
EX_ADDR[8]	USB Clock	Controls the USB clock select. 1 = USB Host/Device clock is generated internally 0 = USB Device clock is generated from GPIO[0]. When generating a spread spectrum clock on OSC_IN, GPIO[1] can be driven from the system board to generate a 48 MHz clock for the USB Host.
EX_ADDR[7]	32_FLASH	Selects the data bus width of the FLASH memory device found on Chip Select 0. Refer to 8/16_FLASH bit (Bit 0) of this register as well. 0 = 8 or 16-bit data bus size (must be pulled down during address strapping) 1 = not supported
EX_ADDR[6]	(Reserved)	(Reserved)
EX_ADDR[5]	EXP_DRIVE	Expansion bus low/medium/high drive strength. The drive strength depends on EXP_DRIVE and EXP_MEM_DRIVE configuration bits. EXP_MEM_DRIVE EXP_DRIVE Expansion drive strength --- 0 0 Reserved 0 1 Medium Drive 1 0 Low Drive 1 1 High Drive
EX_ADDR[4]	PCI_CLK	Sets the clock speed of the PCI Interface 0 = 33 MHz (must be pulled down during address strapping) 1 = not supported
EX_ADDR[3]	(Reserved)	(Reserved). EX_ADDR[3] must not be pulled down during address strapping. This bit must be written to '1' if performing a write to this register.
EX_ADDR[2]	PCI_ARB	Enables the PCI Controller Arbiter 0 = PCI arbiter disabled 1 = PCI arbiter enabled
EX_ADDR[1]	PCI_HOST	Configures the PCI Controller as PCI Bus Host 0 = PCI as non-host 1 = PCI as host
EX_ADDR[0]	8/16_FLASH	Specifies the data bus width of the FLASH memory device found on Chip Select 0. 8/16_FLASH Data bus size 0 16-bit 1 8-bit

Table 7. Setting Intel XScale® Processor Operation Speed

Intel XScale® Processor Speed (Factory Part Speed)	Cfg0 EX_ADDR[21]	Cfg1 EX_ADDR[22]	Cfg_en_n EX_ADDR[23]	Actual Core Speed (MHz)
667 MHz	X	X	1	667 MHz
667 MHz	0	0	0	667 MHz
667 MHz	1	0	0	533 MHz
667 MHz	0	1	0	266 MHz
667 MHz	1	1	0	400 MHz
533 MHz	X	X	1	533 MHz
533 MHz	0	0	0	533 MHz
533 MHz	1	0	0	533 MHz
533 MHz	0	1	0	266 MHz
533 MHz	1	1	0	400 MHz
400 MHz	X	X	1	400 MHz
400 MHz	0	0	0	400 MHz
400 MHz	1	0	0	400 MHz
400 MHz	0	1	0	266 MHz
400 MHz	1	1	0	400 MHz
266 MHz	X	X	X	266 MHz

Note: The Intel XScale processor can operate at slower speeds than the factory programmed speed setting. This is done by placing a value on Expansion bus address bits 23,22,21 when PLL_LOCK is deasserted and knowing the speed grade of the part from the factory. Column 1 above denotes the speed grade of the part from the factory. Column 2, 3, and 4 denotes the values captured on the Expansion Bus address bits when PLL_LOCK is deasserted. Column 5 represents the speed at which the Intel XScale processor speed is operating at.

3.3.3 8-Bit Device Interface

The IXP43X network processors support 8-bit-wide data bus devices (byte mode). For interface cycles, the data lines and control signals can be connected as shown in Figure 3 on page 26. During byte mode accesses, the remaining data signals not being used EX_DATA[15:8], are driven by the processor to an unpredictable state on WRITE cycles and tri-stated during READ cycles.

When booting an 8-bit flash device, the expansion bus must be configured during reset to the 8-bit mode, bit 0 and 7 of Configuration Register 0 must be set as follows (see Table 6):

Bit 0 = 1. By default this bit is set high when coming off reset or any time reset is asserted.

Bit 7 = 0. This can be done by placing an external 470 ohm pull-down resistor to the pin EX_ADDR[7].

Boot-strapping is required in certain address pins of the Expansion bus. If it is required to change access mode, after the system has booted, and during normal operation; the Timing and Control Register for Chip Select must be configured to perform the desired mode access. For a complete description on accomplishing this refer to the **Expansion Bus** chapter in the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

3.3.4 16-Bit Device Interface

The IXP43X network processors support 16-bit wide data bus devices (16-bit word mode). For Intel interface cycles, the data lines and control signals can be connected as shown in Figure 3 on page 26.

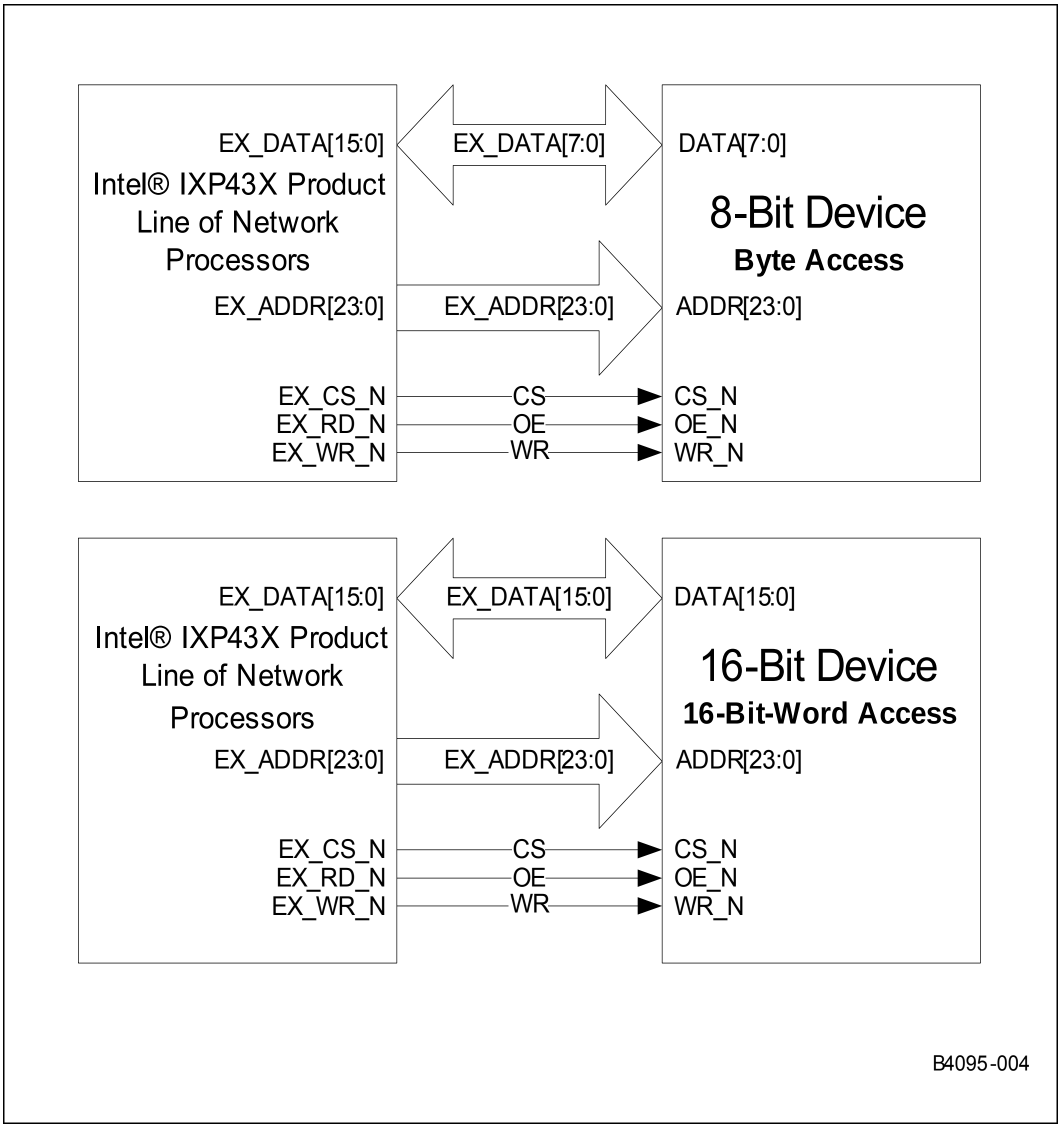
When booting a 16-bit flash device, the expansion bus must be configured during reset to the 16-bit mode (see Configuration Register 0).

Bit 0 = 0. This can be done by placing an external 470 ohm pull-down resistor to the pin EX_ADDR[0].

Bit 7 = 0. This can be done by placing an external 470 ohm pull-down resistor to the pin EX_ADDR[7].

Boot-strapping is required in certain address pins of the Expansion bus.To change to access mode after booting the system and during normal operation, the Timing and Control Register for Chip Select must be configured to perform the desired mode access. For a complete description on how to accomplish this refer to the **Expansion Bus** chapter in the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

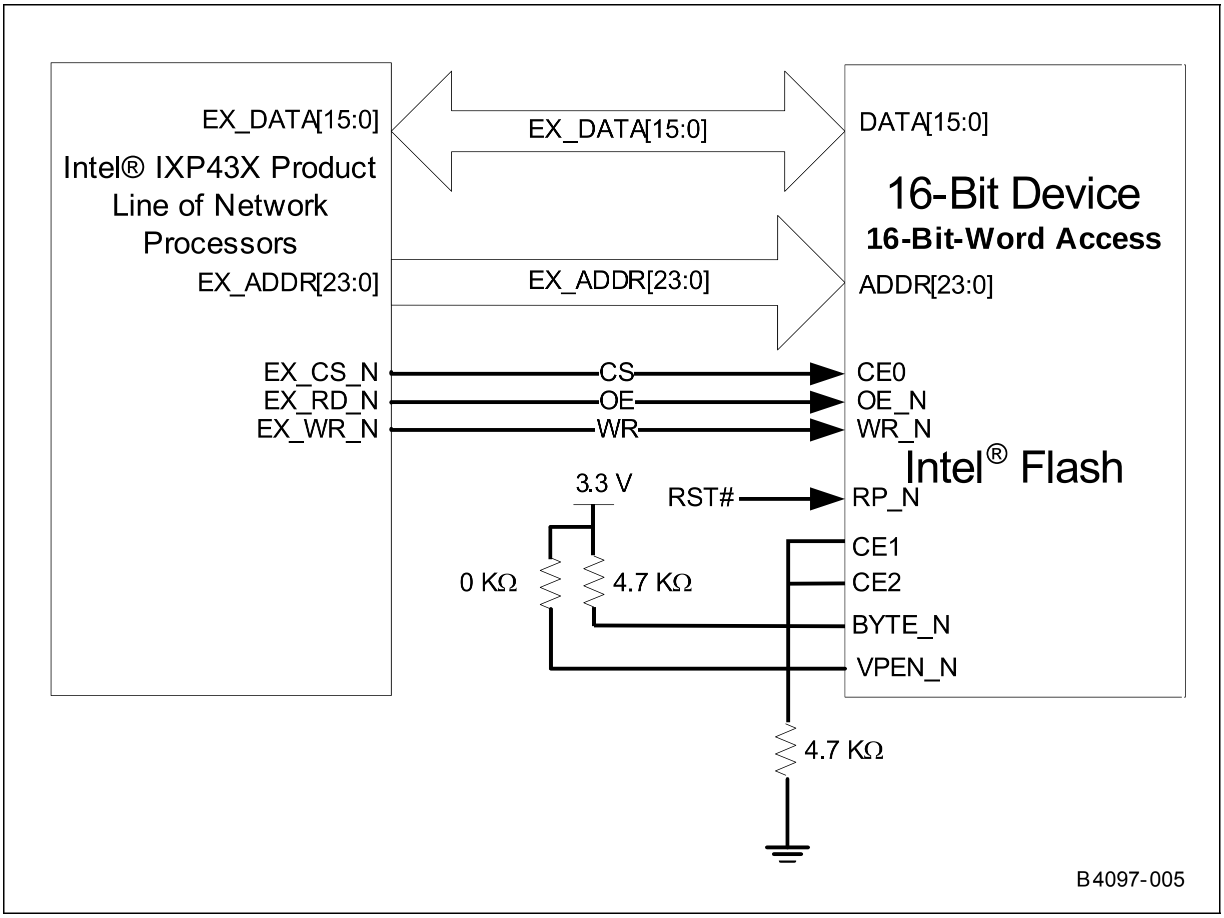
Figure 3. 8/16-Bit Device Interface



3.3.5 Flash Interface

Figure 4 illustrates how a boot ROM is connected to the expansion bus. The flash (ROM) used in the block diagram is the Intel StrataFlash® memory device TE28F256J3D — 32-Mbyte, 16-bit, flash in the 56-TSOP package. The Intel StrataFlash memory TE28F256J3D is part of the 0.18-µm, 3.3-V Intel StrataFlash memory.

Figure 4. Flash Interface Example



3.4 UART Interface

The UART interface are a 16550-compliant UART with the exception of transmit and receive buffers. Transmit and receive buffers are 64 bytes-deep versus the 16 bytes required by the 16550 UART specification.

The interface can be configured to support speeds from 1,200 Baud to 921 Kbaud. The interface supports the following configurations:

- Five, six, seven, or eight data-bit transfers
- One or two stop bits
- Even, odd, or no parity

The request-to-send (RTS0_N) and clear-to-send (CTS0_N) modem control signals also are available with the interface for hardware flow control. The hardware supports a four-wire interface:

- Transmit Data
- Receive Data
- Request to Send

- Clear to Send

Note: The UART module does not support full modem functionality. However, this can be implemented, by using GPIO ports to generate DTR, DSR, RI, and DCD and making some changes to the driver.

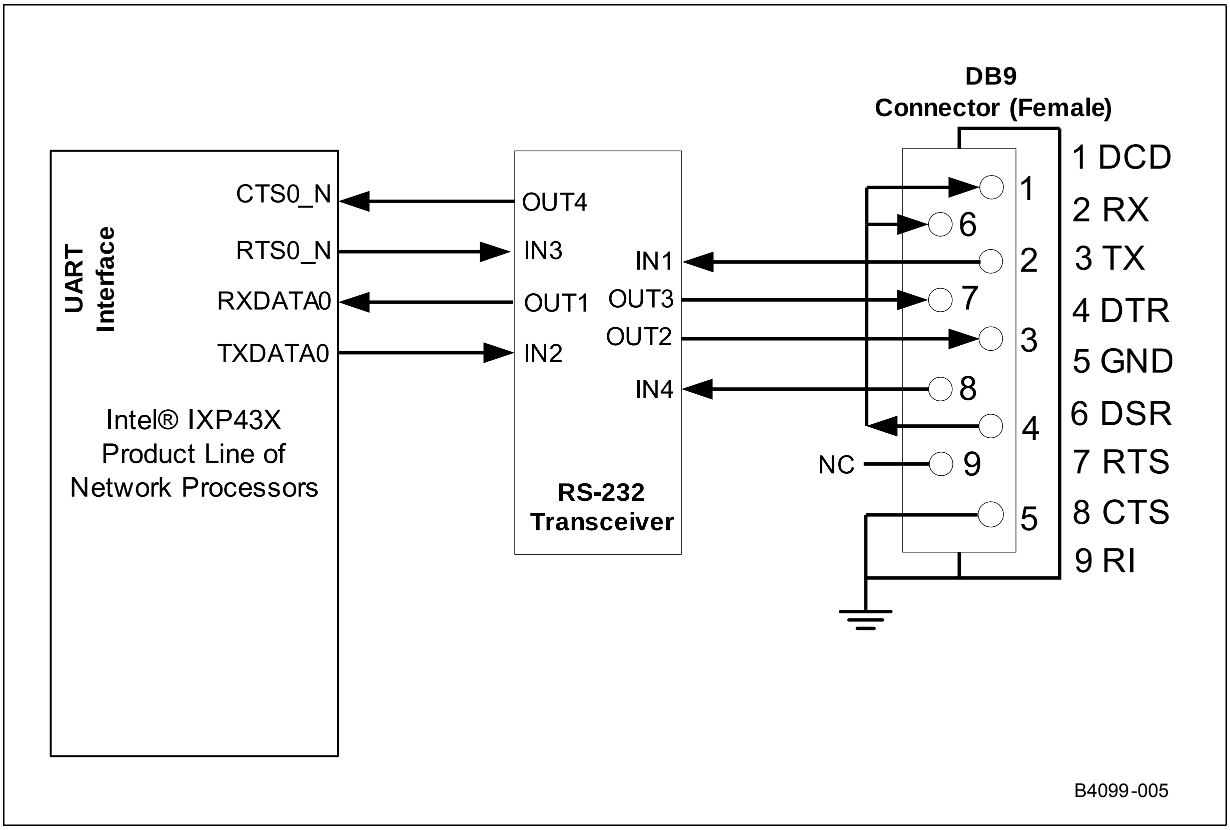
3.4.1 Signal Interface

Table 8. UART Signal Recommendations

Name	Type Field	Pull Up/ Down	Recommendations
RXDATA0	I	Yes	Serial data input Port 0. When signal is not being used in the system, this pin should be pulled high with a 10-KΩ resistor.
TXDATA0	O	No	Serial data output Port 0.
CTS0_N	I	Yes	Clear-To-Send Port 0. \When signal is not being used in the system, this pin should be pulled high with a 10-KΩ resistor.
RTS0_N	O	No	Request-To-Send Port 0.

The following figure contain a typical four signal interface between the UART and an RS-232 transceiver driver, required to interface with external devices. Unused inputs to the RS-232 driver can be connected to ground. This avoids signals floating to undetermined states which can cause over heating of the driver leading to permanent damage.

Figure 5. UART Interface Example



3.5 MII Interface

The IXP43X network processors support a maximum of two Ethernet MACs. Depending on the part number of the IXP43X network processors, various combinations can be used. Refer to the *Intel® IXP43X Product Line of Network Processors Datasheet* for a detailed list of features that can be enabled depending upon your requirements.

All MACs contained in the NPEs are compliant to the IEEE 802.3 specification and handle flow control for the IEEE 802.3Q VLAN specification.

The Management Data Interface (MDI) supports a maximum of 32 PHY addresses. MDI signals are required to be connected to every PHY chip. Each PHY port is assign a unique address in the external PHY chip from 0 to 31, totaling a maximum of 32 PHY addresses. The maximum number of MACs supported by the IXP43X network processors is two.

The MII interface supports clock rates of 25 MHz for 100-Mbps operation or 2.5 MHz for 10-Mbps operation.

3.5.1 Signal Interface MII

Table 9. MII NPE A Signal Recommendations

Name	Type Field	Pull Up / Down	Recommendations
ETHA_TXCLK	I	Yes	Transmit Clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHA_TXDATA[3:0]	O	No	Transmit Data.
ETHA_TXEN	O	No	Transmit Enable.
ETHA_RXCLK	I	Yes	Receive Clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHA_RXDATA[3:0]	I	Yes	Receive Data. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHA_RXDV	I	Yes	Receive Data Valid. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHA_COL	I	Yes	Collision Detect. If operating in a full duplex mode and there is no requirement to use the Collision Detect signal, then the pin must be pulled low with a 10-KΩ resistor.
ETHA_CRS	I	Yes	Carrier Sense. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:

1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals*.**

Table 10. MII NPE C Signal Recommendations (Sheet 1 of 2)

Name	Type Field	Pull Up / Down	Recommendations
ETHC_txclk	I	Yes	Externally supplied transmit clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps This MAC contains hardware hashing capabilities that are local to the interface. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHC_txdATA[3:0]	O	No	Transmit data bus to PHY, asserted synchronously with respect to ETHC_TXCLK. This MAC contains hardware hashing capabilities that are local to the interface.
ETHC_txen	O	Yes	Indicates that the PHY is being presented with nibbles on the MII interface. Asserted synchronously, with respect to ETHC_TXCLK, at the first nibble of the preamble, and remains asserted until all the nibbles of a frame are presented. This MAC contains hardware hashing capabilities that are local to the interface.

Table 10. MII NPE C Signal Recommendations (Sheet 2 of 2)

Name	Type Field	Pull Up / Down	Recommendations
ETHC_rxclk	I	Yes	Externally supplied receive clock: • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
ETHC_rxdATA[3:0]	I	Yes	Receive data bus from PHY, data sampled synchronously, with respect to ETHC_RXCLK. This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
ETHC_rxdv	I	Yes	Receive data valid is used to inform the MII interface about data that is being sent by the Ethernet PHY This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
ETHC_col	I	Yes	Asserted by the PHY when a collision is detected by the PHY. This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system When this interface is disabled through the NPE-C Ethernet soft fuse (refer to the Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual)* and is not being used a system design, this interface/signal is not required for any connection.
ETHC_crs	I	Yes	Asserted by the PHY when the transmit medium or receive medium are active. De-asserted when both the transmit and receive medium are idle. Remains asserted throughout the duration of collision condition. PHY asserts CRS asynchronously and de-asserts synchronously with respect to ETHC_RXCLK. This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in note 1 — only require pull-ups or pull-downs in the ***clock-input signals.***

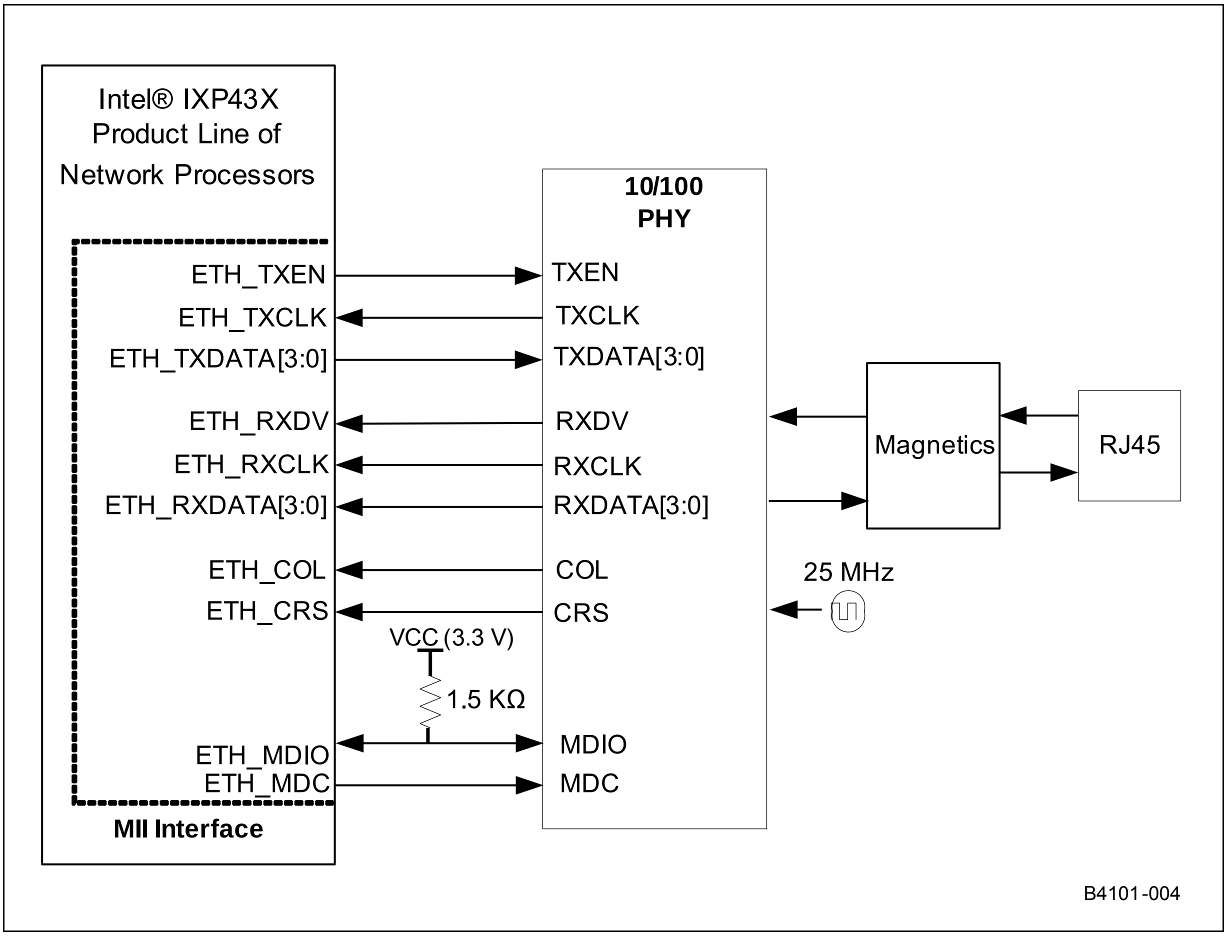
Table 11. MAC Management Signal Recommendations - NPE A and NPE C

Name	Type Field	Pull Up / Down	Recommendations
ETH_mdio	IO	Yes	NPE A and NPE C Management data input output. Provides the write data to both PHY devices connected to each MII interface. **An external pull-up resistor of 1.5K ohm is required on ETHC_MDIO to properly quantify the external PHYs used in the system.** For specific implementation, see the IEEE 802.3 specification. Should be pulled high through a 10-KΩ resistor when not being utilized in the system
ETH_mdc	O	No	NPE A and NPE C Management data clock. Management data interface clock is used to clock the MDIO signal as an output and sample the MDIO as an input. The ETHC_MDC is an input on power up and can be configured to be an output through Intel APIs documented in the *Intel® IXP400 Software Programmer's Guide*

3.5.2 Device Connection, MII

Figure 6 is a typical example of an Ethernet PHY device interfacing to one of the MACs via the MII hardware protocol.

Figure 6. MII Interface Example



3.6 GPIO Interface

The IXP43X network processors provide 16 general-purpose input/output pins to generate and capture application-specific input and output signals. Each individual pin can be programmed as an input or output.

When programmed as an input, GPIO 0 to GPIO 12 can be configured to be an interrupt source. Interrupt sources can be configured to detect either active high, active low, rising edge, falling edge, or transitional. In addition, GPIO14 and GPIO15 can be programmed to provide a user-programmable clock out.

During reset, all pins are configured as inputs and remain in this state until configured otherwise, with the exception of GPIO15, which by default provides a clock output. The driver strength of GPIO pins is sufficient to drive external LEDs with a proper limiting resistor.

3.6.1 Signal Interface

Table 12. GPIO Signal Recommendations

Name	Type Field	Pull Up/ Down	Recommendations
GPIO[13:0]	IO	Yes	General Purpose Input/Output. If used as an input interrupt (only GPIO [12:0]), should be pull-up or pull-down, depending on the level of activation. For example: Active high, use a 10-KΩ pull-down resistor. Active low, use a 10-KΩ pull-up resistor. Should be pulled high through a 10-KΩ resistor when *not* used. ***Note:*** Alternate function for GPIO[1] - External USB 48 MHz Bypass Clock
GPIO[14]	IO	Yes	General Purpose Input/Output. Same recommendations as GPIO[13:0]. An additional feature includes Clock generation, max clock out 33.33 MHz., set as input by default.
GPIO[15]	IO	Yes	General Purpose Input/Output. Same recommendations as GPIO[13:0]. An additional feature includes Clock generation, max clock out 33.33 MHz., set as output by default.

3.6.2 Design Notes

The drive strength for GPIO[15:14] is limited to 8 mA, while GPIO [13:0] can output up to 16 mA. When used for driving high current devices such as LEDs or relays, make sure to place current-limiting resistor; else there could be permanent damage to the driver of the IXP43X network processors.

It is recommended that a 10-KΩ pull-up resistor be used when a GPIO port is configured as an input and not being used.

3.7 USB Interface

There are two USBV2.0 Host Controllers in the IXP43X network processors. It supports Low-Speed, 1.5 Mbps, Full-Speed, 12 Mbps, High-Speed, 480 Mbps rate and interface is EHCI compliant.

Supported features are:

- Host function
- Low-speed interface
- Full-speed interface
- High-speed interface
- EHCI register interface
- UTMI+ Level 2 Compliant

The following is a partial list of features that are not supported:

- Device function
- OTG function

3.7.1 Signal Interface

Table 13. USB Host Signal Recommendations

Name	Type Field	Pull Up/ Down	Description
USB_P0_POS	I/O	Yes	Positive signal of the differential USB receiver/driver for the USB host interface. Use an 20Ω series termination resistor at the source. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P0_NEG	I/O	Yes	Negative signal of the differential USB receiver/driver for the USB host interface. Use an 20Ω series termination resistor at the source. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P0_PWREN	O	No	Enables the external VBUS power source.
USB_P0_OC	I	No	External VBUS power is in over current condition When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P1_POS	I/O	Yes	Positive signal of the differential USB receiver/driver for the USB host interface. Use an 20Ω series termination resistor at the source. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P1_NEG	I/O	Yes	Negative signal of the differential USB receiver/driver for the USB host interface. Use an 20Ω series termination resistor at the source. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P1_PWREN	O	No	Enable the external VBUS power source.
USB_P1_OC	I	No	External VBUS power is in over current condition When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*

A typical implementation of a USB interface Host down-stream is shown in Figure 9. The Host controller cannot be used as a Device controller.

Note: Depending on the data rate required, Low-speed, Full-speed or High-speed, the 1.5K resistor shown near the device interface must be connected on the D+ or D-.

Speed configuration at the Device can be set as stated in note 1 and 2 below. For more details, refer to the *Universal Serial Bus Specification*, Revision 2.0.

Note:

1. If a 1.5-KΩ, pull-up resistor is connected to USB_P_POS line, the USB port is identified as Full-speed and High-speed mode.

2. If a 1.5-KΩ, pull-up resistor is connected to USB_P_NEG line, the USB port is identified as Low-speed mode.

To maintain signal integrity and minimize end-users termination mismatch, the IXP43X network processors require external series termination resistors. The value of the terminating resistors is based on the operational speed and length of the transmission line.

Refer to following termination guidelines for High-speed:

1. High-speed USB designs require parallel termination at both the transmitter and receiver. For host controller designs that use external termination resistors, place the termination resistors as close as possible to the host controller signal pins. Recommend less than 200 mils if possible. Follow the manufacturer's recommendation for the termination value needed to obtain the required 45 ohm to ground parallel HS termination.
2. For downstream ports, a 15 kΩ pull down resistor on the connector side of the termination is required for device connection detection purposes. Note that this pull down might be integrated into the host controller silicon. Follow the manufacturer's recommendation for the specific part used.
3. A common mode (CM) choke should be used to terminate the high speed USB bus if they should pass EMI testing. Place the CM choke as close as possible to the connector as shown in Figure 8 on page 36. Common mode chokes can provide required noise attenuation. Design can include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing.

Note: Common mode chokes degrade signal quality, thus they should only be used if EMI is a known problem.

Figure 7. Common Mode Choke

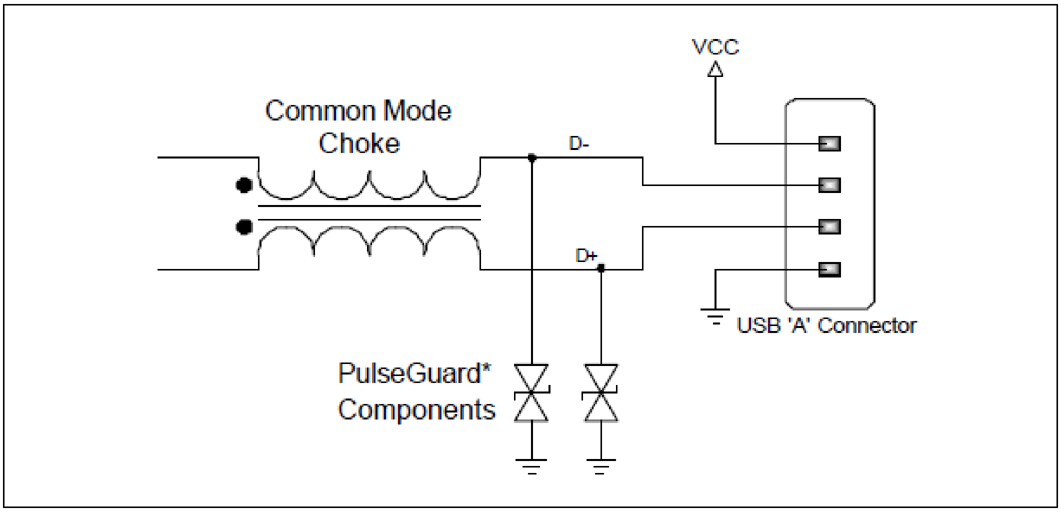


Figure 8. USB RCOMP and ICOMP Pin Requirement

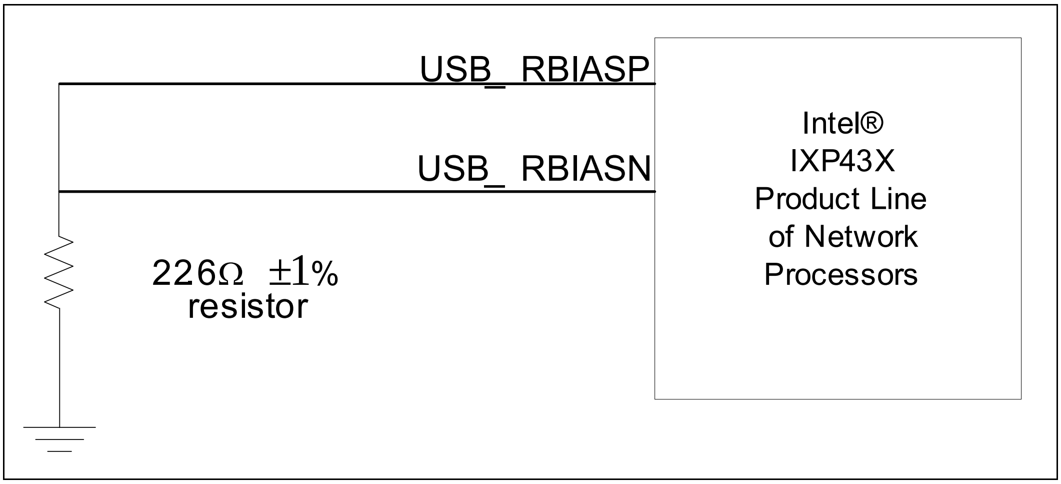
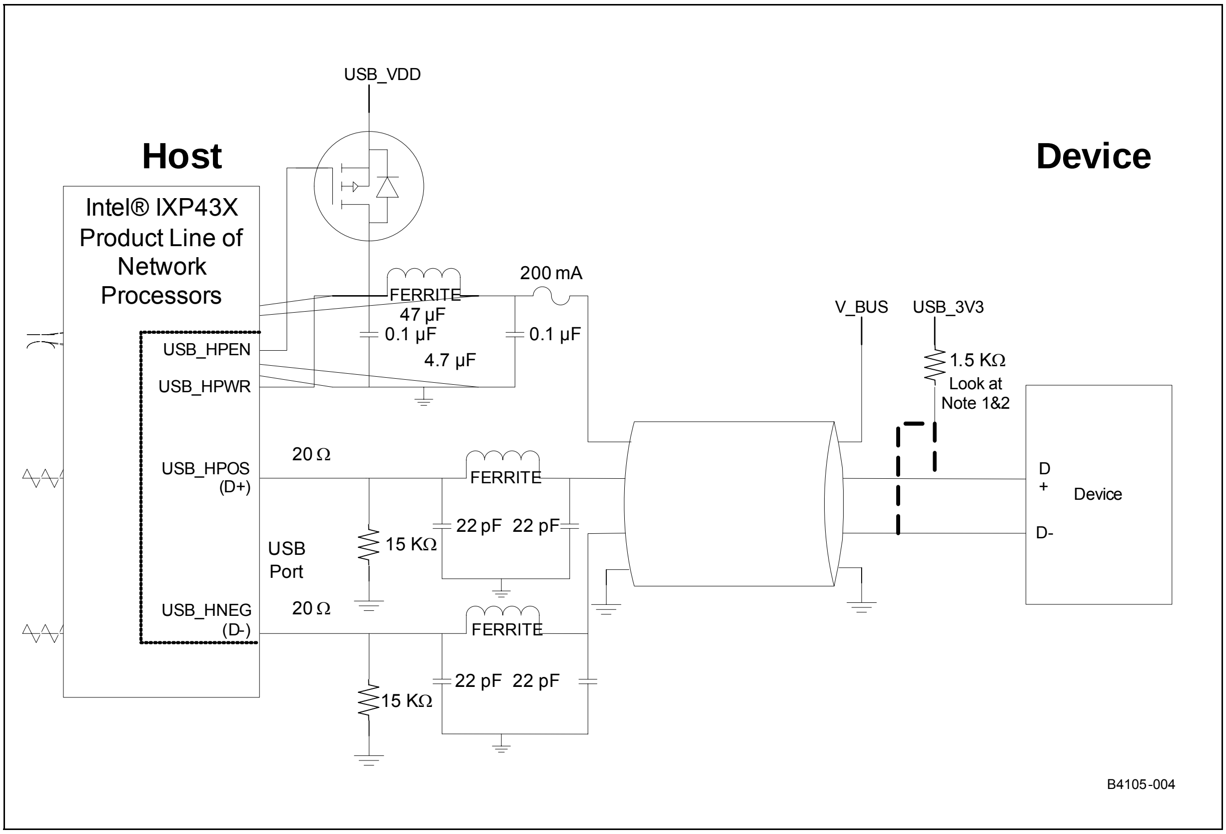


Figure 9. USB Host Down Stream Interface Example



3.8 UTOPIA Level 2 Interface

The IXP43X network processors support the industry-standard UTOPIA Level 2 bus interface. A dedicated Network Processor Engine (NPE) handles segmentation and reassembly of ATM cells, CRC checking/generation, and transfer of data to/from memory. This allows parallel processing of data traffic on the UTOPIA interface, off-loading processor overhead required by the Intel XScale® Processor.

The UTOPIA module is configured as a master and can support single-PHY (SPHY) or multi-PHY (MPHY).

The IXP43X network processors are in compliance with the ATM Forum, *UTOPIA Level 2 Specification*, Revision 1.0. For optimal design results, the guidelines of the specification should be followed.

3.8.1 Signal Interface

Table 14. UTOPIA Level 2/MII_A

Name	Type Field	Pull Up/ Down	Description
UTP_OP_CLK / ETHA_TXCLK	I	Yes	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 Transmit clock input. Also known as UTP_TX_CLK. This signal is used to synchronize all UTOPIA Level 2 transmit output to the rising edge of the UTP_OP_CLK. MII Mode of Operation: Externally supplied transmit clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_OP_FCO	TRI	Yes	UTOPIA Level 2 flow control output signal. Also known as the TXENB_N signal. Used to inform the selected PHY about data transmission. Placing the PHY's address on the UTP_OP_ADDR and bringing UTP_OP_FCO to logic 1 during the current clock, followed by the UTP_OP_FCO going to a logic 0, on the next clock cycle, selects the PHY that is active in MPHY mode. In SPHY configurations, UTP_OP_FCO is used to inform the PHY that the processor is ready to send data. This signal is tied to Vcc with an external 10-KΩ resistor.
UTP_OP_SOC	TRI	Yes	Start of Cell. Also known as TX_SOC. Active high signal is asserted when UTP_OP_DATA contains first valid byte of a transmitted cell. This signal is tied to Vss with an external 10-KΩ resistor.
UTP_OP_DATA[3:0] / ETHA_TXDATA[3:0]	TRI	No	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 output data. Also known as UTP_TX_DATA. Used to send data from the processor to an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Transmit data bus to PHY, asserted synchronously with respect to ETHA_TXCLK. This MAC interface does not contain hardware hashing capabilities that are local to the interface. In this mode of operation the pins represented by this interface are ETHA_TXDATA[3:0].

†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.

Name	**Type Field**	**Pull Up / Down**	**Description**
UTP_OP_DATA[4] / ETHA_TXEN	TRI	No	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 output data. Also known as UTP_TX_DATA. Used to send data from the processor to an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Indicates that the PHY is being presented with nibbles on the MII interface. Asserted synchronously, with respect to ETHA_TXCLK, at the first nibble of the preamble, and remains asserted until all the nibbles of a frame are presented. This MAC does not contain hardware hashing capabilities that are local to the interface.
UTP_OP_DATA[7:5]	TRI	No	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 output data. Also known as UTP_TX_DATA. Used to send data from the processor to an ATM UTOPIA Level 2-compliant PHY.
UTP_OP_ADDR[4:0]	I/O	Yes	Transmit PHY address bus. Used by the processor when operating in MPHY mode to poll and select a single PHY at any given time. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
UTP_OP_FCI	I	Yes	UTOPIA Level 2 Output data flow control input: Also known as the TXFULL/CLAV signal. Used to inform the processor, the ability of each polled PHY to receive a complete cell. For cell-level flow control in an MPHY environment, TxClav is an active high tri-stateable signal from the MPHY to ATM layer. The UTP_OP_FCI is connected to multiple MPHY devices. It sees the logic high generated by the PHY, one clock after the given PHY address is asserted and a full cell can be received by the PHY. The UTP_OP_FCI sees a logic low generated by the PHY one clock cycle, after the PHY address is asserted, and a full cell cannot be received by the PHY. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
UTP_IP_CLK / ETHA_RXCLK	I	Yes	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 Receive clock input. Also known as UTP_RX_CLK. This signal is used to synchronize all UTOPIA Level 2-received inputs to the rising edge of the UTP_IP_CLK. MII Mode of Operation: Externally supplied receive clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps This MAC interface does not contain hardware hashing capabilities that are local to the interface. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.			

Name	Type Field	Pull Up / Down	Description
UTP_IP_FCI	I	Yes	UTOPIA Level 2 Input Data flow control input signal. Also known as RXEMPTY/CLAV. Used to inform the processor of the ability of each polled PHY to send a complete cell. For cell-level flow control in an MPHY environment, RxClav is an active high tri-stateable signal from the MPHY to ATM layer. The UTP_IP_FCI, which is connected to multiple MPHY devices, sees logic high generated by the PHY, one clock after the given PHY address is asserted, when a full cell can be received by the PHY. The UTP_IP_FCI sees a logic low generated by the PHY, one clock cycle after the PHY address is asserted if a full cell cannot be received by the PHY. In a SPHY mode, this signal is used to indicate to the processor that the PHY has an octet or cell available for transferring to the processor. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse (refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual)* and is not being used in a system design, the interface/signal is not required for any connection.
UTP_IP_SOC	I	Yes	Start of Cell. RX_SOC Active-high signal that is asserted when UTP_IP_DATA contains the first valid byte of a transmitted cell. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
UTP_IP_DATA[3:0] / ETHA_RXDATA[3:0]	I	Yes	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Receives data bus from the PHY; asserted synchronously with respect to ETHA_RXCLK. When the interface/signal is enabled and is not being used in a system design, it should be pulled high with a 10KΩ resistor. When the interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. (Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual).*
UTP_IP_DATA[4] / ETHA_RXDV	I	Yes	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by to the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Receive data valid used to inform the MII interface about data that is being sent by the Ethernet PHY. This MAC does not contain hardware hashing capabilities that are local to the interface. When the interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse (and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*

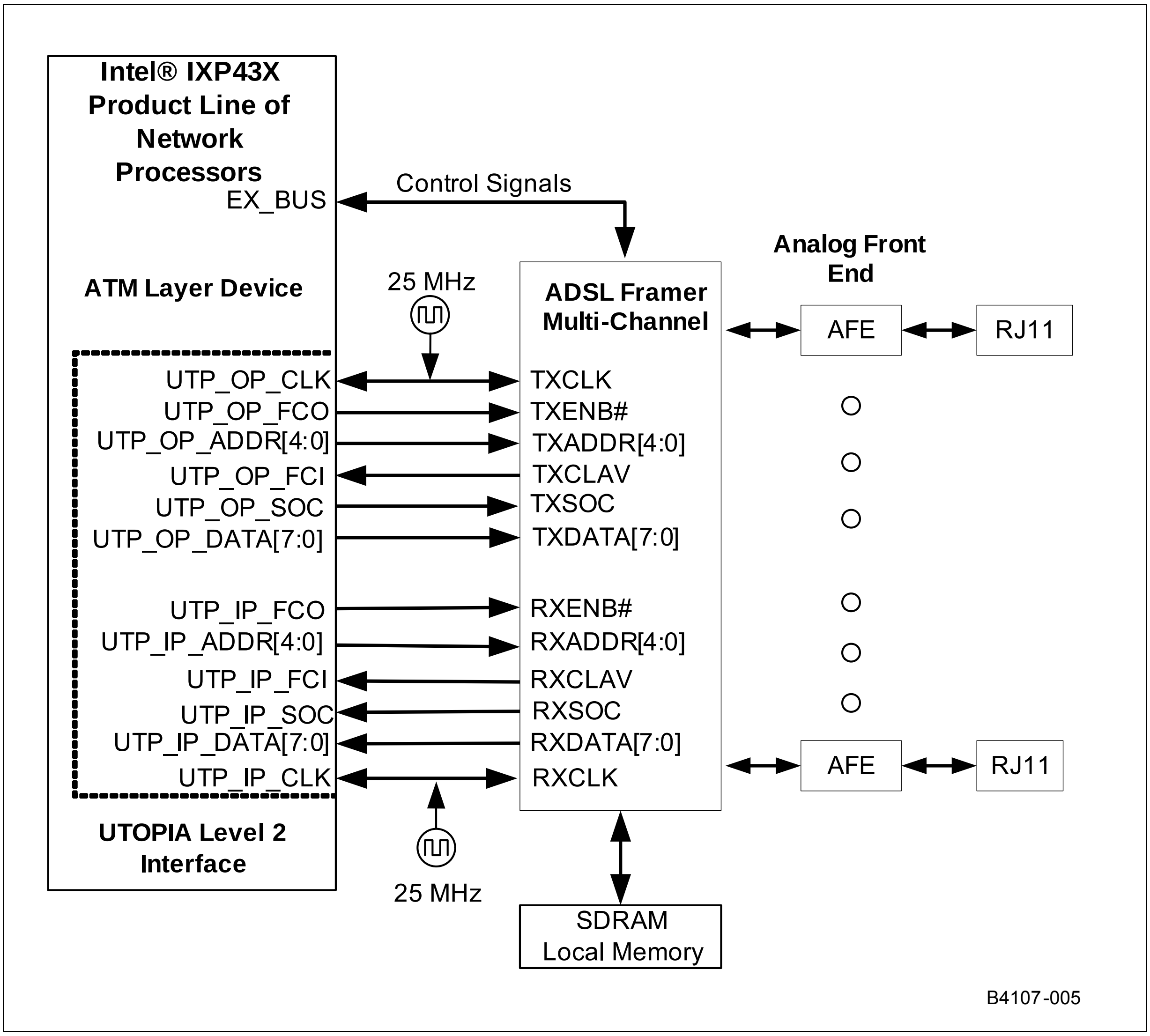
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.

Name	Type Field	Pull Up / Down	Description
UTP_IP_DATA[5] / ETHA_COL	I	Yes	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. • When an NPE A is configured in UTOPIA Level 2 mode of operation and the signal is not used, it should be pulled high through a 10-KΩ resistor. MII Mode of Operation: Asserted by the PHY when a collision is detected by the PHY. • When an NPE A is configured in MII mode of operation and the signal is not used, it should be pulled low through a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/ or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
UTP_IP_DATA[6] / ETHA_CRS	I	Yes	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Asserted by the PHY when transmit medium or receive medium is active. De-asserted when both the transmit and receive medium are idle. Remains asserted throughout the duration of collision condition. PHY asserts CRS asynchronously and de-asserts synchronously with respect to ETHA_RXCLK. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
UTP_IP_DATA[7]	I	Yes	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Not Used. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
UTP_IP_ADDR[4:0]	I/O	No	Receive PHY address bus. Used by the processor while operating in an MPHY mode to poll and select a single PHY at any given point of time.
UTP_IP_FCO	TRI	Yes	UTOPIA Level 2 Input Data Flow Control Output signal: Also known as the RX_ENB_N. In a SPHY configuration, UTP_IP_FCO is used to inform the PHY that the processor is ready to accept data. In MPHY configurations, UTP_IP_FCO is used to select those PHY drives that signals UTP_RX_DATA and UTP_RX_SOC. The PHY is selected by placing the PHY's address on the UTP_IP_ADDR and bringing UTP_OP_FCO to logic 1 during the current clock, followed by the UTP_OP_FCO going to a logic 0 on the next clock cycle. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.			

3.8.2 Device Connection

The following example shown in Figure 10 shows a typical interface to an ADSL Framer via the UTOPIA bus. Notice that depending on the framer used some control signals might be required which can be derived from the Expansion bus or the GPIO signals.

Figure 10. UTOPIA Interface Example



3.9 HSS Interface

NPE A has an integrated High-Speed Serial (HSS) module, whose primary function is to provide connectivity between the internal NPE A and the external HSS interface. There is one HSS port that can directly interface to SLIC/CODEC devices for voice applications, or serial DSL framers. The HSS ports are software configurable to support various serial protocols, such as T1/ E1/J1, and MVIP. For a list of supported protocols, see the *Intel® IXP400 Software Programmer's Guide.*

3.9.1 Signal Interface

Table 15. High-Speed, Serial Interface 0

Name	Type Field	Pull Up Down	Recommendations
HSS_TXFRAME0	I/O	Yes	Transmit frame. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_TXDATA0	OD	Yes	Transmit data out. Open Drain Output. When this interface/signal is enabled and is used or not used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor to Vcc33.
HSS_TXCLK0	I/O	Yes	Transmit clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXFRAME0	I/O	Yes	Receive frame. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXDATA0	I	Yes	Receive data input. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXCLK0	I/O	Yes	Receive clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

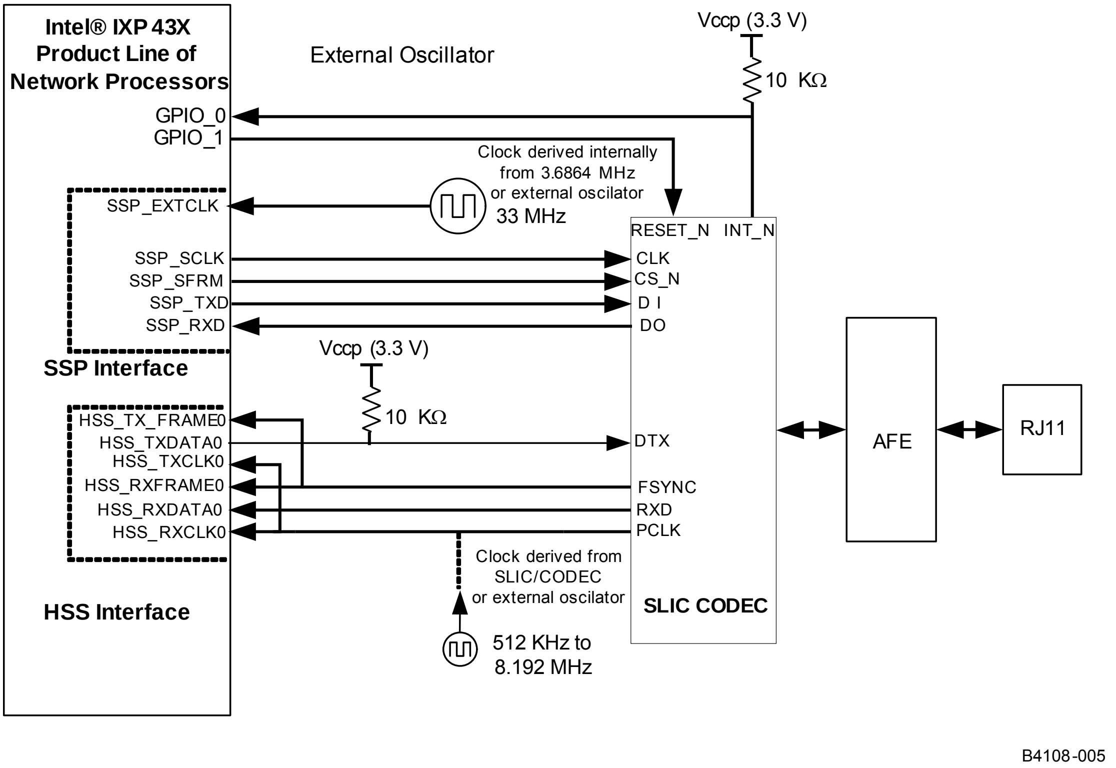
Notes:

1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features Enabled by a specific part number and required to be Soft Fuse-disabled, as stated in Note 1 alone require pull-ups or pull-downs in the ***clock-input signals.***

3.9.2 Device Connection

Figure 11 shows a typical interface between the IXP43X network processors and a SLIC CODEC, through the SSP and HSS ports, and a couple of GPIO signals.

Figure 11. HSS Interface Example



3.10 SSP Interface

The IXP43X network processors have a Synchronous Serial Peripheral Interface (SSP) module. Its primary function is to provide connectivity between the Intel XScale® Processor and an external SSP interface.

The SSP module supports Texas Instruments synchronous serial protocol (SSP)*, Motorola serial peripheral interface (SPI)* and National Microwire*.

The clock rate can be selected from an internal, 3.6864-MHz source or external source fed at input pin SSP_EXTCLK. The clock can then be divided down anywhere from 7.2 KHz to 1.84 MHz by setting bits 15:08 in SSP Control Register 0 (SSCR0). For instructions on the SSP configuration register, refer to the Serial Clock Register (SCR) subsection in the Memory Controller chapter of the *Intel® IXP43X Product Line of Network Processors Datasheet*.

3.10.1 Signal Interface

Table 16. Synchronous Serial Peripheral Port Interface

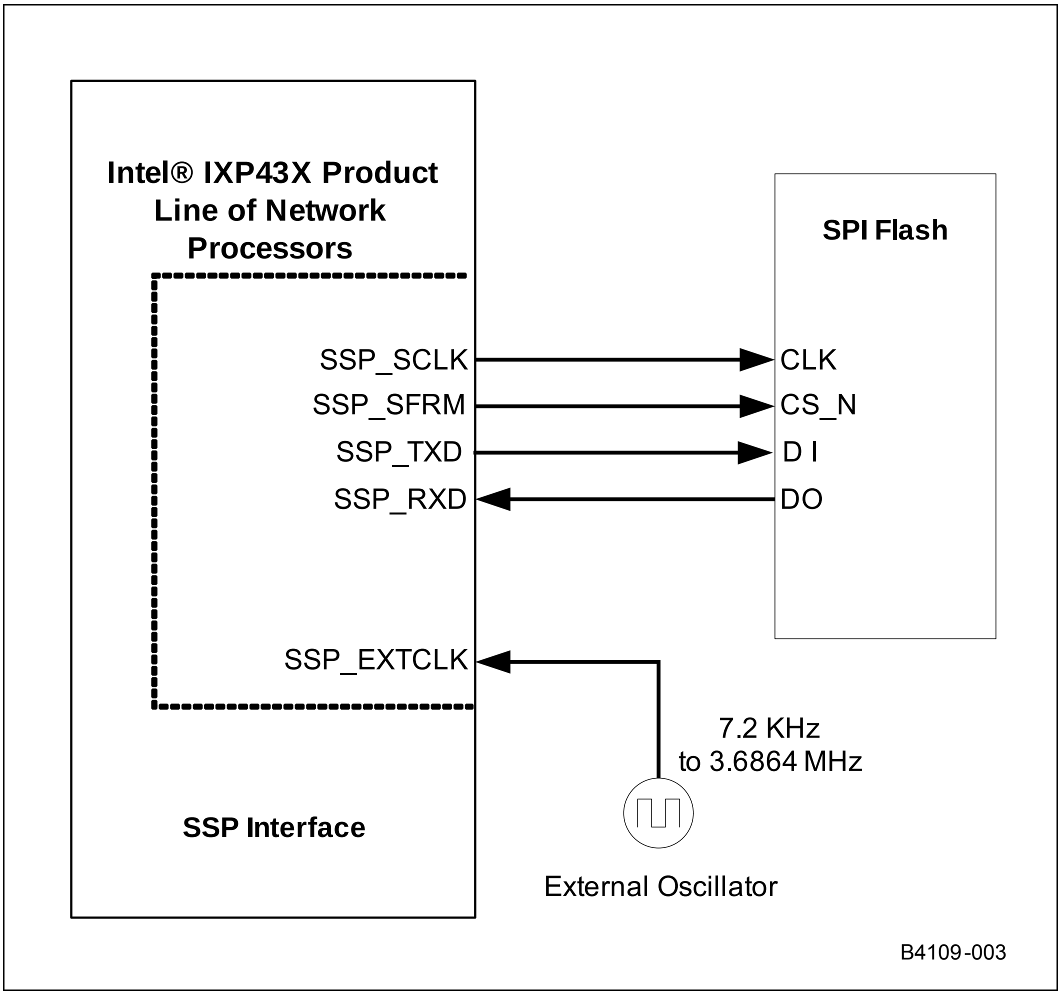
Name	Type Field	Pull Up/ Down	Recommendations
SSP_SCLK	O	No	Serial bit clock.
SSP_SFRM	O	No	Serial frame indicator.
SSP_TXD	O	No	Transmit data (serial data out).
SSP_RXD	I	Yes	Receive data (serial data in). Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
SSP_EXTCLK	I	Yes	External clock input. Should be pulled high through a 10-KΩ resistor when *not* being utilized in the system.

3.10.2 Device Connection

There are a number of devices available that can interface to SSP or SPI ports, these can range from RTC (Real-Time Clock), LCD (Liquid Crystal Displays), Digital Thermal Sensor to Flash memory devices.

One of the most common usage for SSP or SPI port, is serial flash code storage. Serial flash devices can be used to store board revision, serial numbers, or assembly information. Figure 12 provides an example of a Serial Flash device interface to the SSP port in the IXP43X network processors. For an additional example of SPI interface, refer to Figure 11, where a SLIC is connected to the SSP and HSS ports.

Figure 12. Serial Flash and SSP Port (SPI) Interface Example



3.11 PCI Interface

The PCI Controller of the IXP43X network processors is an industry-standard, 32-bit interface, high-performance bus that operates at 33 MHz(*PCI Local Bus Specification*, Rev. 2.2).

The PCI interface is capable of operating as a host or an option. This PCI implementation supports 3.3 V I/O only.

As indicated in Figure 13, a PCI transparent bridge is required to support Compact PCI.

General PCI routing guidelines can be found in Section 6.2, “Topology” on page 67. For detailed information, see the *PCI Local Bus Specification*, Rev. 2.2.

3.11.1 Signal Interface

Table 17. PCI Controller (Sheet 1 of 2)

Name	Type Field	Pull Up/ Down	Recommendations
PCI_AD[31:0]	I/O	Yes	PCI Address/Data bus. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_CBE_N[3:0]	I/O	Yes	PCI Command/Byte Enables. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_PAR	I/O	Yes	PCI Parity. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_FRAME_N	I/O	Yes	PCI Cycle Frame. When this interface/signal is enabled and is being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_TRDY_N	I/O	Yes	PCI Target Ready. When this interface/signal is enabled and is being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_IRDY_N	I/O	Yes	Initiator Ready. When this interface/signal is enabled and is being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_STOP_N	I/O	Yes	Stop. When this interface/signal is enabled and is being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_PERR_N	I/O	Yes	Parity Error. When this interface/signal is enabled and is being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_SERR_N	I/O	Yes	System Error. When this interface/signal is enabled and is being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_DEVSEL_N	I/O	Yes	Device Select: When this interface/signal is enabled and is being used or not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_IDSEL	I	Yes	Initialization Device Select. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_REQ_N[3:1]	I	Yes	Arbitration Request. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_REQ_N[0]	I/O	Yes	Arbitration Request: When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_GNT_N[3:1]	O	No	Arbitration Grant.
PCI_GNT_N[0]	I/O	Yes	Arbitration Grant. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

Notes:

1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals.***

Table 17. PCI Controller (Sheet 2 of 2)

Name	Type Field	Pull Up/ Down	Recommendations
PCI_INTA_N	O/D	Yes	Interrupt A. When this interface/signal is enabled and is used or not used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
PCI_CLKIN	I	Yes	Clock input. When this interface/signal is enabled and is not being used in a system design, the interface/ signal should be pulled high with a 10-KΩ resistor.

Notes:
1. Features disabled/enabled by Soft Fuse must be done during the boot-up sequence. *A feature cannot be enabled after being disabled without asserting a system reset.*
2. Features disabled by a specific part number, do not require pull-ups or pull-downs. Therefore, all pins can be left unconnected.
3. Features enabled by a specific part number — and required to be Soft Fuse-disabled, as stated in Note 1 — only require pull-ups or pull-downs in the ***clock-input signals.***

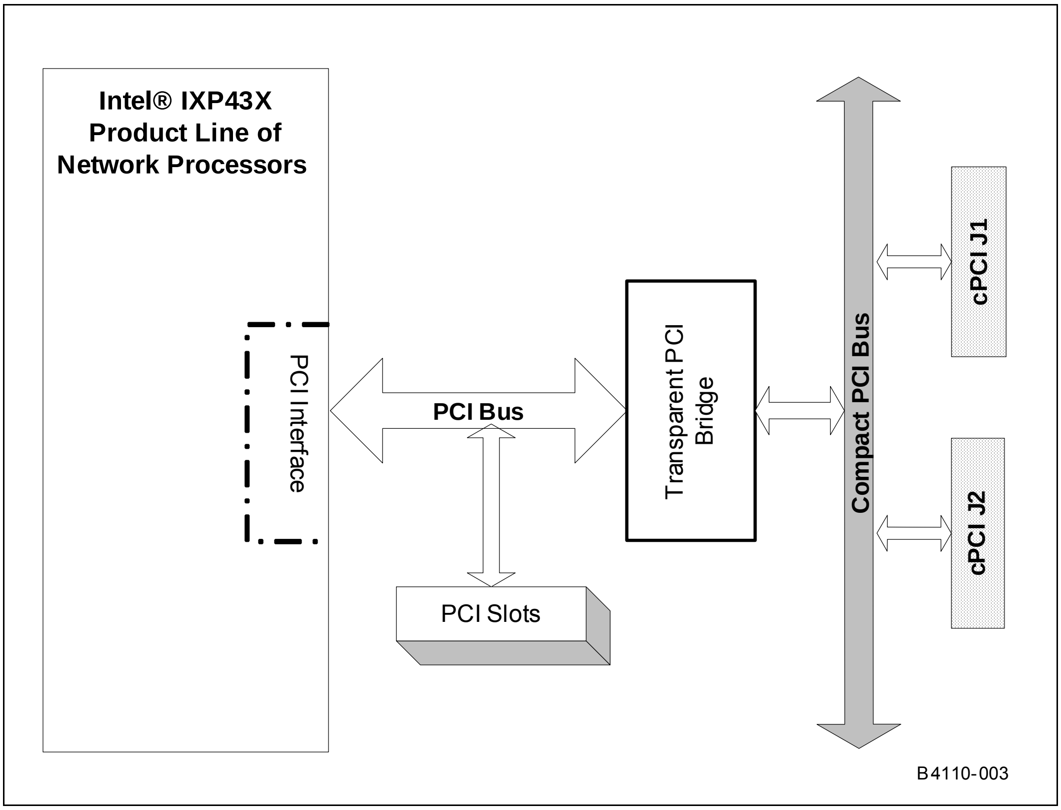
3.11.2 PCI Interface Block Diagram

While using the IXP43X network processors in Master mode, the PCI module can interface to up to four PCI cards (devices) at 33 MHz. The limitation is due to load requirements to maintain signal integrity.

The PCI-to-PCI bridge must be used to address the PCI requirement not to exceed one load per PCI connector unless it is through a PCI-to-PCI bridge.

The IDSEL signals on the PCI slots can be connected to one of the PCI_AD lines, preferable to the higher order address signals. Reset support can be accomplished by using one of the GPIO pins to generate a reset or through an external decoder of the Expansion bus.

Figure 13. PCI Interface



3.11.3 PCI Option Interface

The IXP43X network processors can be used in a design as a host or as an option device. This section describes how the IXP43X network processors can be connected as an option device to obtain proper functionality. There are slight differences in the hardware interface when designing for option mode. All routing and board recommendations described in this document apply, however the design must use the device pin connections listed in Table 18.

Table 18. PCI Host/Option Interface Pin Description (Sheet 1 of 3)

Name	Type Field	Device-Pin Connection	Option Type Field	Description
PCI_AD[31:0]	I/O	All address/data signals must be connected between the two devices.	I/O	PCI Address/Data bus
PCI_CBE_N[3:0]	I/O	Connect signals to same pins between the two devices.	I/O	PCI Command/Byte Enables
PCI_PAR	I/O	Connect signal to same pin between the two devices.	I/O	PCI Parity
PCI_FRAME_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	PCI Cycle Frame
PCI_TRDY_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	PCI Target Ready

Table 18. PCI Host/Option Interface Pin Description (Sheet 2 of 3)

Name	Type Field	Device-Pin Connection	Option Type Field	Description
PCI_IRDY_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	Initiator Ready
PCI_STOP_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	Stop
PCI_PERR_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	Parity Error
PCI_SERR_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	System Error
PCI_DEVSEL_N	I/O	Connect signal to same pin between the two devices. Connect a 10-KΩ pull-up resistor.	I/O	Device Select
PCI_IDSEL	I	Connect one of the higher order PCI address signals to the Device. Connect a 10K pull-up resistor to the Host.	I	Initialization Device Select
PCI_REQ_N[3:1]	I	From the Option device, connect output signal PCI_REQ_N[0] to one of the PCI_REQ_N[3:0] inputs to the Host. Note: the PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where **n** must be the same number in the square bracket.	I	Arbitration Request On the Option device, these signals are not used, they should be pulled high with a 10-KΩ resistor. ***Note:*** The PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where **n** must be the same number in the square bracket.
PCI_REQ_N[0]	I	From the Option device, connect output PCI_REQ_N[0] to one of the PCI_REQ_N[3:0] inputs to the Host. Note: the PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where **n** must be the same number in the square bracket.	O	Arbitration Request On the Option device, this signal is an output and must be connected to one of the PCI_REQ_N[3:0] inputs to the Host. ***Note:*** The PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where **n** must be the same number in the square bracket.
PCI_GNT_N[3:1]	O	Connect one of the Host outputs PCI_GNT_N[3:0] to PCI_GNT_N[0] input to the Option. Note: the PCI_GNT_N[n] must correspond to the PCI_GNT_N[n], where **n** must be the same number in the square bracket.	O	Arbitration Grant On the Option device, these signals are not used, they should be pulled high with a 10-KΩ resistor.
PCI_GNT_N[0]	O	Connect one of the Host outputs PCI_GNT_N[3:0] to PCI_GNT_N[0] input to the Option. Note: the PCI_GNT_N[n] must correspond to the PCI_GNT_N[n], where **n** must be the same number in the square bracket.	I	Arbitration Grant On the Option device, this signal is an input and must be connected to one of the PCI_GNT_N[3:0] outputs of the Host. ***Note:*** The PCI_REQ_N[n] must correspond to the PCI_GNT_N[n], where **n** must be the same number in the square bracket.

Table 18. PCI Host/Option Interface Pin Description (Sheet 3 of 3)

Name	Type Field	Device-Pin Connection	Option Type Field	Description
PCI_INTA_N	O/D	Connect PCI_INTA_N output from the Option to one of the GPIO input signals of the Host. The GPIO signal at the Host must be configure as an input interrupt level sensitive.	O/D	Interrupt A This interrupt is generated from the Option to one of the GPIO inputs to the Host. On the Host this signal is not used, it should be pulled high with a 10-KΩ resistor.
PCI_CLKIN	I	Clock must be connected to both devices. Trace lengths must be matched. Use point to point clock distribution.	I	Clock input

3.11.4 Design Notes

- The IXP43X network processors do not support the 5 V PCI signal interface by itself. Only the 3.3 V signal interface is supported without signal level conversion; however, it is possible to interface to 5 V logic while using a voltage level converter.
- The *PCI Local Bus Specification*, Rev. 2.2 requires that the bus is always **parked**, as some device is always driving the AD lines. You must use pull-ups on these signals. The specification states that the following control lines should be pulled up:
  - FRAME_N
  - STOP_N
  - INTA_N
  - TRDY_N
  - SERR_N
  - INTB_N
  - IRDY_N
  - PERR_N
  - INTC_N
  - DEVSEL_N
  - LOCK_N
  - INTD_N
- The GPIO pins of the IXP43X network processors can be used by PCI devices on PCI slots to request an interrupt from the processors' PCI controller.
- PCI_INTA_N is used to request interrupts to external PCI Masters. This signal is an open drain and requires a pull-up resistor.

3.12 JTAG Interface

JTAG is the popular name for IEEE standards 1149.1-1990 and 1149.1a-1993, *IEEE Standard Test Access Port and Boundary-Scan Architecture*, which provides support for:

- Board-level boundary-scan connectivity testing
- Connection to software debugging tools through the JTAG interface
- In-system programming of programmable memory and logic devices on the PCB

The interface is controlled through five dedicated test access port (TAP) pins: TDI, TMS, TCK, nTRST, and TDO, as described in the IEEE 1149.1 standard. The boundary-scan test-logic elements include the TAP pins, TAP controller, instruction register, boundary-scan register, bypass register, device identification register, and data-specific registers. These are described in the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

The IXP43X network processors can be controlled during debug through a JTAG interface to the processor, the debug tools such as the Macraigor Systems Raven*, EPI Majic*, Wind River Systems* visionPROBE*/ visionICE* or various other JTAG tools plug into the JTAG interface through a connector.

3.12.1 Signal Interface

Table 19. Synchronous Serial Peripheral Port Interface

Name	Type Field	Pull Up / Down	Recommendations
JTG_TMS	I	Yes	Test mode select. When the JTAG interface is not being used, the signal must be pulled high using a 10-kΩ resistor.
JTG_TDI	I	Yes	Test Input data. When the JTAG interface is not being used, the signal must be pulled high using a 10-kΩ resistor.
JTG_TDO	O	O	Test Output data.
JTG_TRST_N	I	Yes	Test Reset. When the JTAG interface is not being used, the signal must be pulled low using a 10-kΩ resistor.
JTG_TCK	I	Yes	Test Clock. When the JTAG interface is not being used, the signal must be pulled high using a 10-kΩ resistor.

3.13 Input System Clock

The IXP43X network processors require a 33.33-MHz reference clock to generate all internal clocks required including core clock and the various buses running internally within the system.

3.13.1 Clock Signals

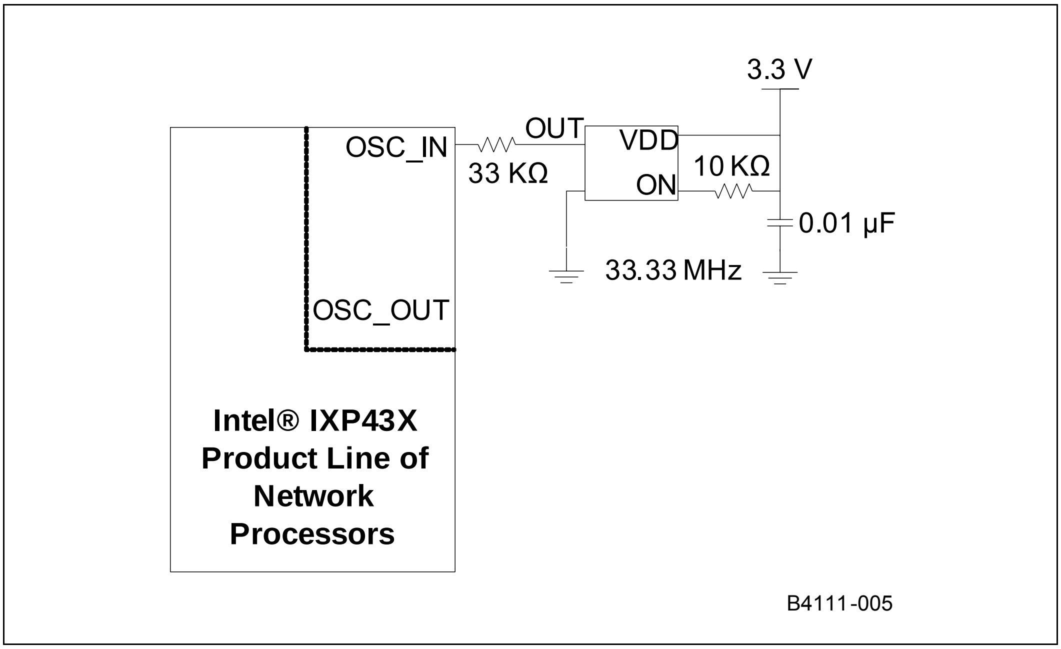
Table 20. Clock Signals

Name	Type Field	Description
OSC_IN	I	Source must be a clock input of 33.33-MHz. Use a series termination resistor, 10 Ω to 33 Ω at the source.
OSC_OUT	O	No connect

3.13.2 Clock Oscillator

While using an external clock oscillator to supply the 33.33-MHz reference system clock, connect the clock oscillator output to the OSC_IN pin through a series termination of 33 Ω as shown in Figure 14. The series termination helps to smooth the rise and fall edges of the clock and eliminate ringing. Leave the OSC_OUT pin unconnected.

Figure 14. Clock Oscillator Interface Example



3.13.3 Recommendations for Crystal Selection

The parameters that should be considered while selecting the crystal to be used are:

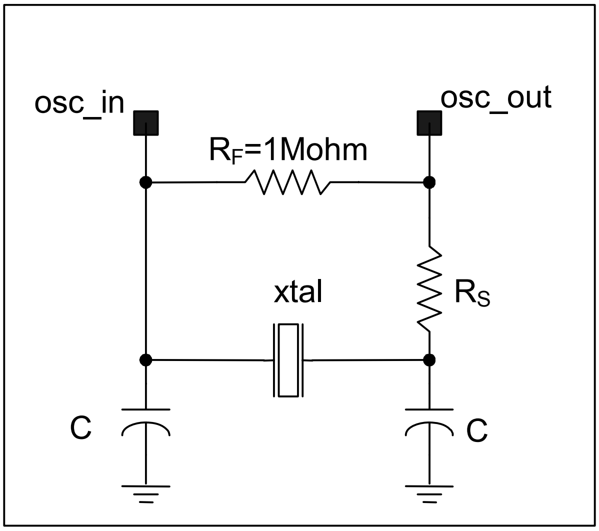
Frequency	33.33 MHz
Operation Mode	Fundamental
Load Capacitance	18 pF (This is the capacitance value of the discrete component) *Note1
Frequency Tolerance	+/- 30 ppm
Frequency stability over temperature	+/- 50 ppm
Effective Series Resistance (ESR)	20 ohm *Note2
Drive level	> 100 uW

Note: 1) The capacitance value here does not include stray capacitance. The design has been simulated to work with load capacitance up to 36pF.

2) This does not include the stray resistance. The design has been simulated to work up to 40 ohm series resistance.

The Rf and Rs may not needed. Please refer to the crystal vendor datasheet for recommendation.

Figure 15. Recommended circuit design on PCB for crystal oscillator



3.14 Power

The IXP43X network processors have separate power supply domains for the processor core, DDRII/I SDRAM memory, and input/output peripherals to enable low power system design.

Table 21. Power Supply

Name	Nominal voltage †	Description
VCC	1.3V	1.3-V power supply input pins are used for the internal logic.
VCC33	3.3V	3.3-V power supply input pins are used for the peripheral (I/O) logic.
VCCDDR	1.8V or 2.5V	1.8-V or 2.5-V power supply input pins are used for the DDRII/I memory interface.
VSS	GND	Ground power supply input pins are used for the 3.3-V, 2.5-V, 1.8-V, and the 1.3-V power supplies.
USB_v5REF	5.0V	5-V power supply input pins are used for reference voltage. **Note:** 3.3-V power supply input can be used but causes damage to the USB controller if signal pin is shorted to 5V VBUS.
VCCP_OSC	3.3V	3.3-V power supply input pins are used for peripheral (I/O) logic of the analog oscillator circuitry. Require special power filtering circuitry. See the *Intel® IXP43X Product Line of Network Processors Datasheet*
VCCF	1.3V	1.3-V power supply input pin. Dedicated for Fuse.
VSSAUBG	GND	Specialized ground for USB Band Gap.
VCCAUPLL	1.3V	1.3-V power supply input pins are used for USB PLL. Requires special power filtering circuitry.See the *Intel® IXP43X Product Line of Network Processors Datasheet*
VCCAUBG	3.3V	3.3-V power supply input pins are used for USB Band Gap Requires special power filtering circuitry. See the *Intel® IXP43X Product Line of Network Processors Datasheet*

Name	Nominal voltage †	Description
VCCPUSB	3.3V	3.3-V power supply input pins are used for USB IO.
VCCUSBCORE	1.3V	1.3-V power supply input pins are used for USB IO core.
VCCA	1.3V	1.3-V power supply input pins are used for internal logic of the analog phase lock-loop circuitry. Requires special power filtering circuitry. See the *Intel® IXP43X Product Line of Network Processors Datasheet*

3.14.1 Decoupling Capacitance Recommendations

It is common practice to place decoupling capacitors between the supply voltages and ground. Placement can be near the input supply pins and ground, with one 100-nF capacitor per pin. Additional decoupling capacitors can be place all over the board every 0.5" to 1.0". This ensures good return path for currents and reduce power surges and high-frequency noise.

It is also recommended that 4.7-µF to 10-µF capacitors be placed every 2" to 3".

3.14.2 VCC Decoupling

Connect one 100-nF capacitor per each VCC pin. Placement should be as close as possible to the pin. It is also recommended to place a 4.7-µF capacitor near the device.

Use traces as thick as possible to eliminate voltage drops in the connection.

3.14.3 VCC33 Decoupling

Connect one 100-nF capacitor per each Vcc33 pin. Placement should be as close as possible to the pin. It is also recommended to place a 4.7-µF capacitor near the device.

Use traces as thick as possible to eliminate voltage drops in the connection.

3.14.4 VCCDDR Decoupling

Connect one 100-nF capacitor per each VCCDDR pin. Placement should be as close as possible to the pin. It is also recommended to place a 4.7-µF capacitor near the device.

Use traces as thick as possible to eliminate voltage drops in the connection.

3.14.5 Power Sequence

Power sequence is crucial for proper functioning of the IXP43X network processors. For a complete description of power sequencing, see the *Intel® IXP43X Product Line of Network Processors Datasheet*.

3.14.6 Reset Timing

Proper reset timing is also a crucial requirement for proper functioning of the IXP43X network processors. There are two reset signal PWRON_RESET_N and RESET_IN_N which required assertion sequence.

For a complete description of their functionality, see the *Intel® IXP43X Product Line of Network Processors Datasheet* and its section titled **Reset Timings**. PWRON_RESET_N is used as a Power Good and RESET_IN_N is used for resetting internal registers.

The IXP43X network processors can be configured at reset de-assertion via external, pull-down resistors on the address expansion bus signals EX_ADDR[23:21]. For a complete description, see Section 6, “Boot/Reset Strapping Configuration” on page 22.

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4.0 General PCB Guide

4.1 PCB Overview

Beginning with components selection, this chapter presents general PCB guidelines. In cases where it is too difficult to adhere to a guideline, engineering judgment must be used. The methods are listed as simple DOs and DO NOT's.

This chapter does not discuss the functional aspects of any bus, or layout guides for any interfaced devices.

4.2 General Recommendations

It is recommended that boards based on the IXP43X network processors employ a PCB stackup yielding a target impedance of 50 Ω ± 10% with 5 mil nominal trace width. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces.

When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

4.3 Component Selection

- Do not use components faster than necessary

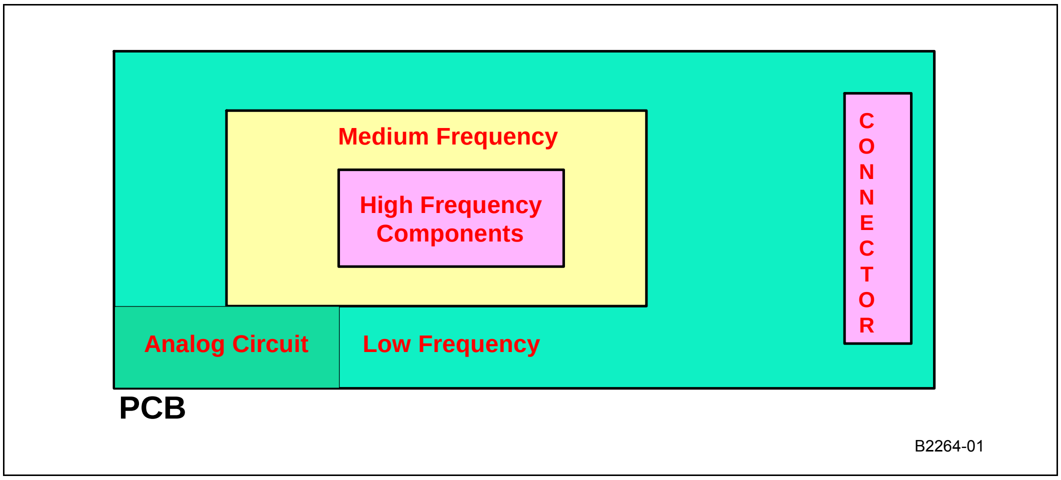
  Clock rise (fall) time should be as slow as possible, as the spectral content of the waveform decreases
- Use components with output drive strength (slew-rate) controllable if available
- Use SMT components (not through-hole components) as through-hole (leaded) components have more stub inductance due to the protruding leads.
- Avoid sockets when possible
- Minimize number of connectors

4.4 Component Placement

As shown in Figure 16 on page 57, when placing components, put:

- High-frequency components in the middle
- Medium-frequency around the high-frequency components
- Low-frequency components around the edge of the printed circuit board

Figure 16. Component Placement on a PCB



- Place noisy parts (clock, processor, video, and so on.) at least 1.5 – 3 inches away from the edge of the printed circuit board
- Do not place noisy components close to internal/external cables
    - Any loose cables picks up noise and acts as an antenna to radiate that noise
    - Be aware of the peak in-rush surge current into the device pins. This surge current can inject high-frequency switching noise into power planes of the printed circuit board
- Place high-current components near the power sources
- Do not share the same physical components (such as buffers and inverters) between high-speed and low-speed signals. Use separate parts.
- Place clock drivers and receivers such that clock trace length is minimized
- Place clock generation circuits near a ground stitch location. Place a localized ground plane around the clock circuits and connect the localized plane to system ground plane
- Install clock circuits directly on the printed circuit board, not on sockets
- Clock crystals should lie *flat* against the board to provide better coupling of electromagnetic fields to the board

4.5 Stack-Up Selection

Stack-up selection directly affects the trace geometry which, in turn, affects the characteristic impedance requirement for the printed-circuit board. Additionally, the **clean**, noise-free-planes design and placement is significantly important as components run at higher speeds requiring more power.

Considerations include:

- Low-speed, printed-circuit-board construction — for example two-layer boards:
    - Advantages:
        - Inexpensive
        - Manufactured by virtually all printed-circuit-board vendors
    - Disadvantages:

    - Poor routing density
    - Uncontrolled signal trace impedance
    - Lack of power/ground planes, resulting in unacceptable crosstalk
    - Relatively high-impedance power distribution circuitry, resulting in noise on the power and ground rails
- High-speed circuits require multi-layer printed circuit boards:
  - Advantages:
    - Controlled-impedance traces
    - Low-impedance power distribution
  - Disadvantages:
    - Higher cost
    - More weight
    - Manufactured by fewer vendors
- Symmetry is essential to keep the board stack-up symmetric about the center
  This minimizes warping
- For best impedance control, have:
  - No more than two signal layers between every power/ground plane pair
  - No more than one embedded micro-strip layer under the top/bottom layers
- For best noise control, route adjacent layers orthogonally. Avoid layer-to-layer parallelism
- Fabrication house must agree on design rules, including:
  - Trace width, trace separation
  - Drill/via sizes
- The distance between the signal layer and ground (or power) should be minimized to reduce the loop area enclosed by the return current
  - Use 0.7:1 ratio as a minimum.
    For example: 5-mil traces, 7-mil prepreg thickness to adjacent power/ground.

Figure 17 and Figure 18 provides an example for a six-layer and eight-layer board. For stripline (signals between planes), the stackup should be such that the signal line is closer to one of the planes by a factor of five or more. Then the trace impedance is controlled predominantly by the distance to the nearest plane.

Figure 17. 8-Layer Stackup

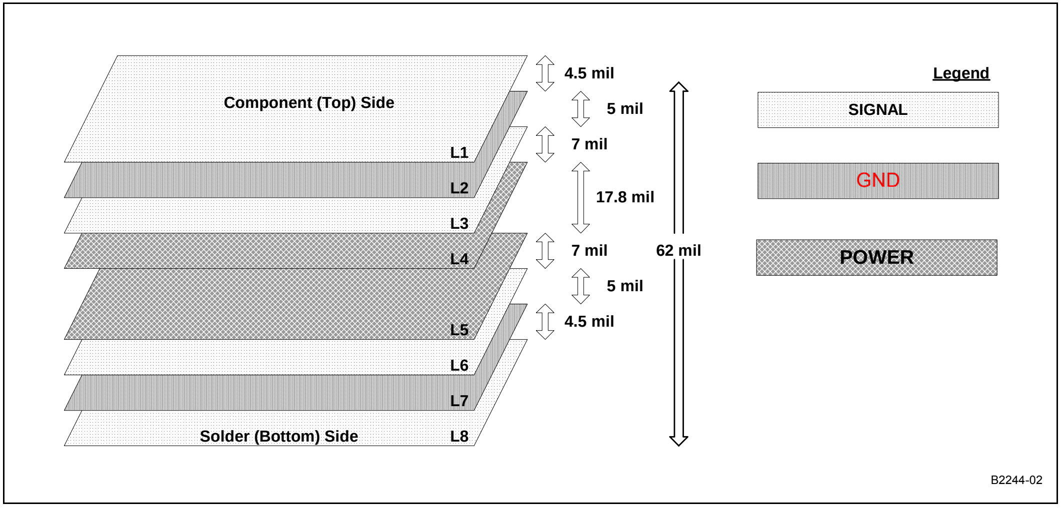
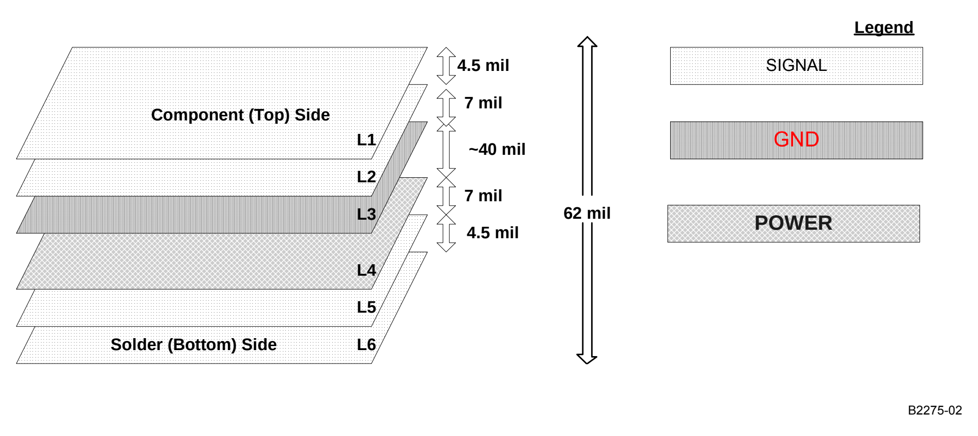


Figure 18. 6-Layer Stackup



- Fast and slow transmission line networks must be considered
- PCB-board velocities
- Board FR4 ~ 4.3
- Target impedance of 50 Ω ± 10%
- Trace width: 5 mils
- Signal Layers (1/2 oz. Copper)
- Power Layer (1 oz. Copper)
- Ground (GND) Layer (1 oz. Copper)

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5.0 General Layout and Routing Guide

5.1 Overview

This chapter provides routing and layout guides for hardware and systems based on the IXP43X network processors.

The high-speed clocking required when designing with the processors requires special attention to signal integrity. In fact, it is highly recommended that the board design be simulated to determine optimum layout for signal integrity. The information in this chapter provides guidelines to aid designers with board layout. In cases where it is too difficult to follow a design rule, engineering judgment must be used.

5.2 General Layout Guidelines

The layout guidelines recommended in this section are based on experience and knowledge gained from previous designs. Layer stacking varies, depending on design complexity, however following standard rules helps minimize potential problems dealing with signal integrity.

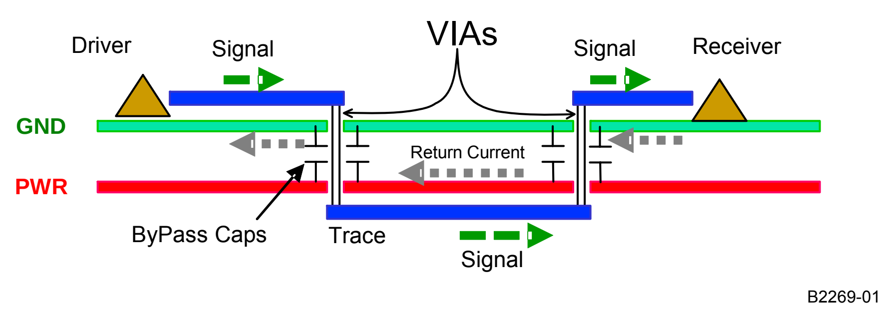
The following recommendations help to route a functional board:

- Provide enough routing layers to comply with minimum and maximum timing requirements of the IXP43X network processors and other components.
- Connectors, and mounting holes must be placed in a ways that will not interfere with basic design guidelines in this document.
- Provide uniform impedance throughout the board, specially for high speed areas such us clocking, DDRII/I-SDRAM, PCI, device bus, and so forth.
- Place analog, high-voltage, power supply, low-speed, and high-speed devices in various sections of the board.
- Decoupling capacitors must be placed next to power pins.
- Series termination resistors must be placed close to the source.
- Analog and digital sections of the board must be physically isolated from each other. No common ground, power planes, and signal traces are allowed to cross-isolation zones. Use appropriately sized PCB traces for larger enough to handle peak current. Keep away from high-speed digital signals.
- Keep stubs as short as possible (preferably, the electrical length of the stub less than half of the length of the rise time of signal).
- All critical signals should be routed before all other non-critical signals.
- Do not route signals close to the edge of the board, power or ground planes. Route signal at least 50 to 100 mils away from the edge of the plane.
- Try to match buses to the same trace length and keep them in groups adjacent to each other, away from other signals.
- Route processor address, data and control signals using a **daisy-chain** topology.
- Minimize number of vias and corners on all high speed signals.
- Do not route under crystals or clock oscillators, clock synthesizers, or magnetic devices (ferrites, toroids).
- Maintain trace spacing consistent between differential pairs and match trace length.
- Keep differential signals away from long and parallel, high-speed paths, such as clock signals and data strobe signals.

- Do not place high-frequency oscillators and switching network devices close to sensitive analog circuits.
- Arrange the board so that return currents for high-speed traces must never jump between planes. Restrict traces to remain on either side of whichever ground plane they start out nearest. This allows the use of naturally grouped horizontal and vertical routing layers.

If signals change between layers, the reference voltage changes, as shown in Figure 19. This creates discontinuity in the path of the signal.

Figure 19. Signal Changing Reference Planes



The design in Figure 19, routes a signal on the top layer, close to the GND plane, and provides a very good return current path. The signal then is routed to the bottom layer, close to the PWR plane, such that the return current flows to the ground plane through bypass caps. Thus the path for the return currents is less inductive than in the previous case where the signal is routed on the top layer.

5.2.1 General Component Spacing

- Do not place components within 125 mils to the edge of the printed circuit board. For exact dimensions consult your manufacturing vendor.
- Keep a minimum spacing between via and the solder pad edges $\geq$ 25mil.
- Position devices that interface with each other close to one another to minimize trace lengths.

Figure 20. Good Design Practice for VIA Hole Placement

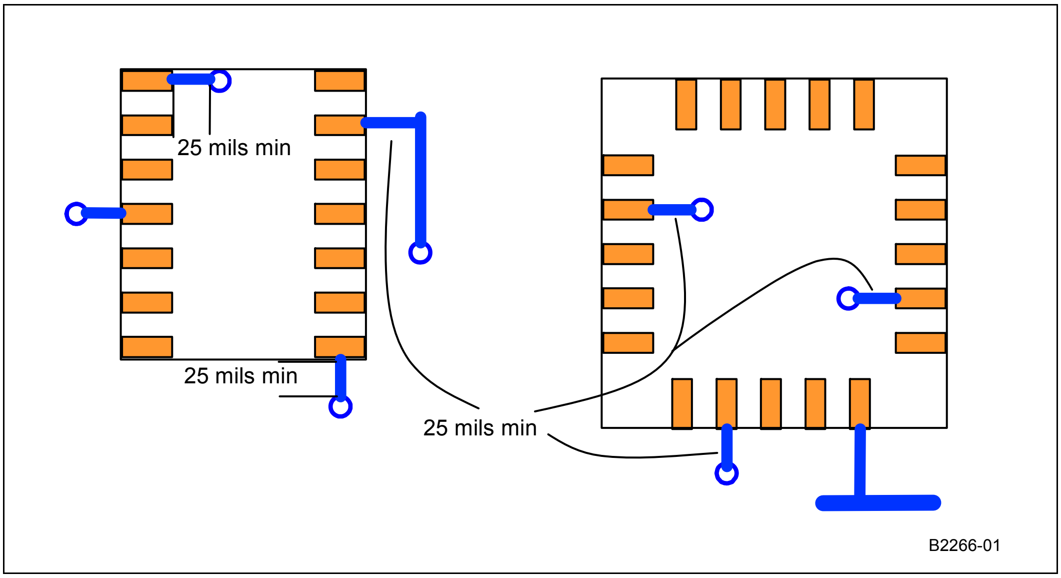


Figure 20 and Figure 21 show good and poor design practices for via placement on surface-mount boards.

Figure 22 shows minimum pad-to-pad clearance for surface-mount passive components and PGA or BGA components.

Figure 21. Poor Design Practice for VIA Placement

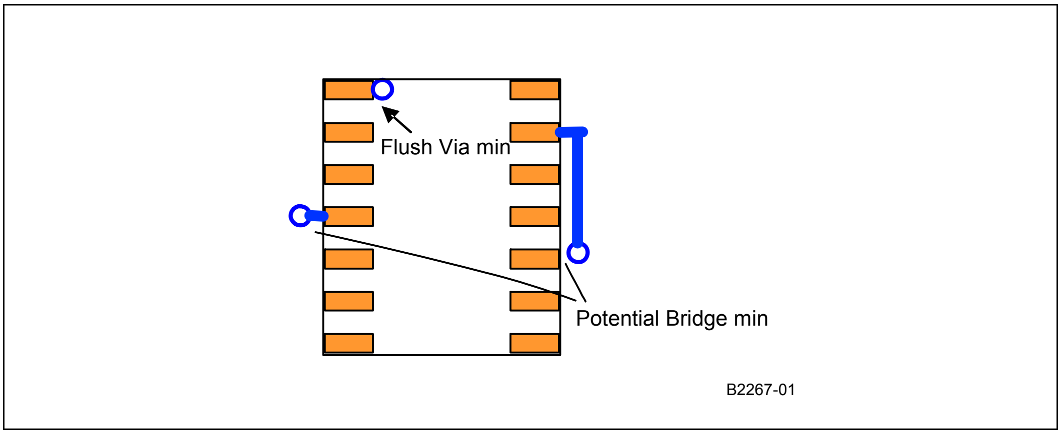
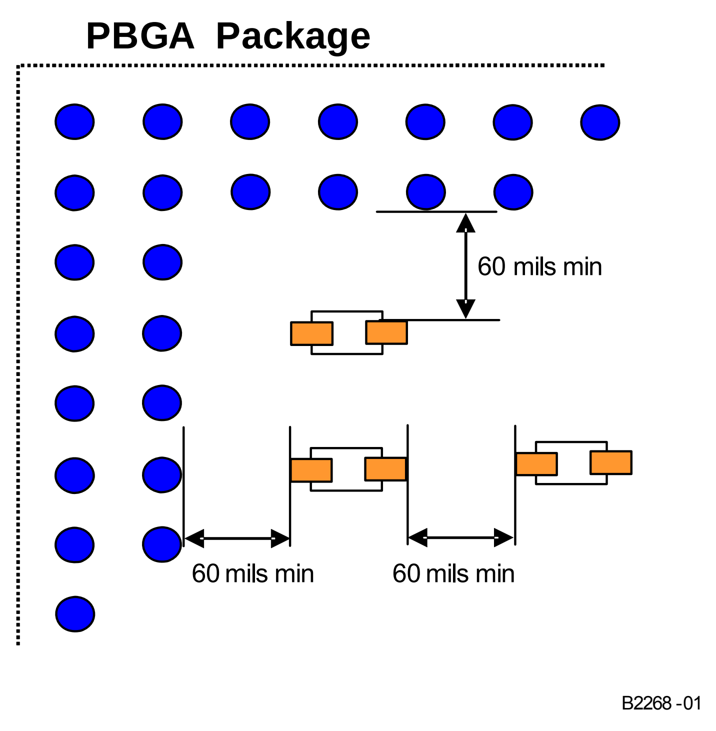


Figure 22. Pad-to-Pad Clearance of Passive Components to a PGA or BGA



5.2.2 Clock Signal Considerations

- Provide good return current paths for clock traces.
- Keep clock traces away from the edge of the board and any other high-speed devices or traces.
- Keep clock traces away from analog signals, including voltage reference signals.
- Clock signals should not cross over a split plane.
- Route clock signals in a single, internal layers and eliminate routing in multiple layers as much as possible.
- Do not route traces or vias under crystals or clock oscillators devices unless there is a plane between the trace and the component.
- Do not route parallel signal traces directly above or below clock traces unless there is a ground or at least a power plane separation between those layers.
- Route clock traces with a minimum number of vias.
- Space clock traces away from other signals three times the trace width on each side.
- Use guard traces when routing on top or bottom layers whenever possible. Guard traces must be connected to ground.
- Do not daisy-chain, instead use point-to-point clock distribution. Place a series termination resistor as close as possible to the source.
- Keep traces short to minimize reflections and signal degradation.
- Maintain control impedance for all clock traces, microstrip or stripline.

  - — Be aware of propagation delays between a microstrip and stripline.
  - — Calculate capacitive loading of all components and properly compensate with a series or parallel terminations.
- Measure and match trace lengths for devices that interface with each other and have their clock derived from the same source.

  If traces must be long, treat them as transmission lines. Terminate clock traces to match trace impedance.
- If there is a power plane, instead of a ground plane, make sure that the power plane has adequate decoupling to ground, especially near clock drivers and receivers.

5.2.3 MII Signal Considerations

MII signals run at 25 MHz and the required routing guide lines are as follows:

- Minimize the number of vias to two per trace
- Keep traces as short as possible and straight, away from other signals
- Control impedance to maintain at 50 Ω
- the length of Rx or Tx in each group must match
- Avoid sharp corners, using 45° corners instead

5.2.4 USB V2.0 Considerations

The following are recommendations for routing differential pair signal required to by the USB interface:

- Traces can be routed in tightly couple structure with 5mil trace width and 10mil air gap, or maintain air gap equal 2X trace width. It is recommended to route manually.
- Match trace length for each differential pair.
- Avoid sharp corners, use 45° corners instead.
- Always use a perfect symmetry within a differential pair.
- Minimize the number vias.
- Avoid routing other signals close by or in parallel to the differential pair, maintaining no less than 50 mil to any other signal.
- Maintain control impedance for each differential pair to 90 Ω +/- 15 Ω.
- Use high value ferrite beads (100 MHz/60 Ω – 100 MHz/240 Ω).

5.2.5 Crosstalk

Crosstalk is caused by capacitance and inductance coupling between signals. It is composed of both backward and forward crosstalk components.

Backward crosstalk creates an induced signal on the network that propagates in the opposite direction of the aggressor signal. Forward crosstalk creates a signal that propagates in the same direction as the aggressor signal.

Circuit board analysis software should be used to analyze your board layout for crosstalk problems.

- To effectively route signals on the PCB, signals are grouped (address, data, and so on.).
  - — The space between groups can be 3 w (where w is the width of the traces).

  - Space within a group can be just 1 w.
  - Space between clock signals or clock to any other signal should be 3 w. The coupled noise between adjacent traces decreases by the square of the distance between the adjacent traces.

5.2.6 EMI Design Considerations

It is strongly recommended that good electromagnetic interference (EMI) design practices must be followed while designing with the IXP43X network processors.

- Information on spread-spectrum clocking is available in the Intel® IXP4XX Product Line of Network Processors *and IXC1100 Control Plane Processor: Spread-Spectrum Clocking to Reduce EMI Application Note.*
- Place high-current devices as closely as possible to the power sources.
- Proper termination of signals can reduce reflections, which can emit a high-frequency component that contribute to more EMI than the original signal itself.
- Ferrite beads can be used to add high frequency loss to a circuit without introducing power loss at DC and low frequencies. They are effective when used to absorb high-frequency oscillations from switching transients or parasitic resonances within a circuit.
- Keep rise and fall times as slow as possible. Signals with fast rise and fall times contain many high-frequency harmonics which can radiate significantly.
- A solid ground is essential at the I/O connector to chassis and ground plane.
- Keep the power plane shorter than the ground plane by at least 5x the spacing between the power and ground planes.
- Stitch together all ground planes around the edge to the board every 100 to 200 mil. This helps reduce EMI radiating out of the board from inner layers.

5.2.7 Trace Impedance

All signal layers require controlled impedance of 50 Ω ±10 % microstrip or stripline (unless otherwise specified) where appropriate. Selecting the appropriate board stack-up to minimize impedance variations is very important.

When calculating flight times, it is important to consider the minimum and maximum trace impedance based on the switching neighboring traces.

5.2.8 Power and Ground Plane

Power and ground planes should have sufficient decoupling capacitors to ensure sustainable current needed for high-speed switching devices. See Section 3.14.1, “Decoupling Capacitance Recommendations” on page 54.

- It is highly recommended to use sufficient internal power and ground planes.
- The Intel® IXP43X Product Line requires a number of power supplies. It is appropriate to use power islands in the power plane under the processor, as it will be too expensive to have a power plane for each power source.
- Power islands must be large enough to include the required power supply decoupling capacitance, and the necessary connection to the voltage source and destination.
- Islands can be separated by a minimum of 20-mil air gap.
- Use at least one via per power or ground pin, wherever possible use more vias, depending on current drawn.

- Use at least one decoupling capacitor per power pin and place it as close as possible to the pin.
- Minimize the number of traces routed across the air gaps between power islands.
  - — Each crossing introduces signal degradation due to the impedance discontinuity.
  - — For traces that must cross air gaps, route them on the side of the board next to a ground plane to reduce or eliminate signal degradation caused by crossing the gap.
  - — When this is not possible, then route the trace to cross the gap at a right angle (90°).

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6.0 PCI Interface Design Considerations

The IXP43X network processors have a single, 32-bit PCI device module that runs at 33 MHz. This chapter describes some basic guidelines to help design hardware that interfaces with PCI devices.

The PCI module is compatible with the *PCI Local Bus Specification*, Rev. 2.2. For a complete functional description and physical requirements, see the *PCI Local Bus Specification*, Rev. 2.2.

6.1 Electrical Interface

The electrical definition is restricted to 3.3 V signaling environment. The device is *not* 5 V tolerant. All devices interfacing with the PCI module must operate at 3.3 V.

6.2 Topology

Interfacing devices must be connected in a daisy-chain topology. When more than one device is in the bus, connecting stubs must be kept as short as possible.

There is a limitation to the number of devices connected to the internal arbiter. If more than four devices are required to be connected, an external arbiter is required.

The system time budget must be satisfied for 33 MHz cycles. The following equation and timing parameters must be met while routing a board that interfaces with a single PCI device or up to four devices as shown in Figure 23.

$T_{CYC} \geq T_{VAL} + T_{PROP} + T_{SKEW} + T_{SU}$

where:

T_{VAL} = Valid Output Delay
T_{PROP} = Bus Propagation Delay (maximum time for complete flight)
T_{SKEW} = Total Clock Skew
T_{SU} = Input Setup Time

@33 MHz	T_{CYC} = 30 nSec	T_{VAL} = 11 nSec	T_{PROP} = 10 nSec	T_{SKEW} = 2 nSec	T_{SU} = 7 nSec

When defining the maximum length of segments A and B as shown in Figure 23, the calculation must:

- Include an additional trace length segment from the PCI connector to the input device within the expansion PCI card
- Assume the segment to be 1.5 inch
- Use trace propagation delay of 150 to 190 ps/in as specified by the PCI standard

Figure 23. PCI Address/Data Topology

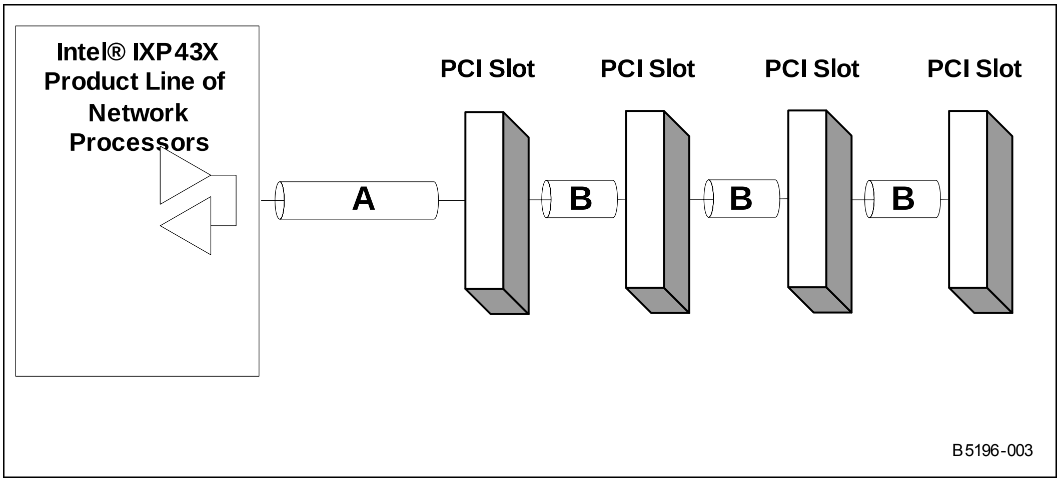

Table 22. PCI Address/Data Routing Guidelines

Parameter	Routing Guidelines
Signal Group	PCI Address/Data
Topology	Daisy Chain
Reference Plane	Ground
Characteristic Trace Impedance	55 Ω ±10%
Nominal Trace Width	5 mils
Nominal Trace Separation	10 mils
Spacing to Other Groups	20 mils
Limit the number of VIAS to 10 per Signal	10

6.3 Clock Distribution

To meet timing and avoid clock overloading, it is recommended to use point-to-point clock distribution as shown in Figure 24.

Clock skew between interfacing devices is very critical and must be met. The maximum skew must be measured between any two components. If designing a motherboard, the skew must be measured to the expansion card device and not to the PCI connector. Ensure that clock skew between all devices does not exceed the values in Section 6.2.

Figure 24. PCI Clock Topology

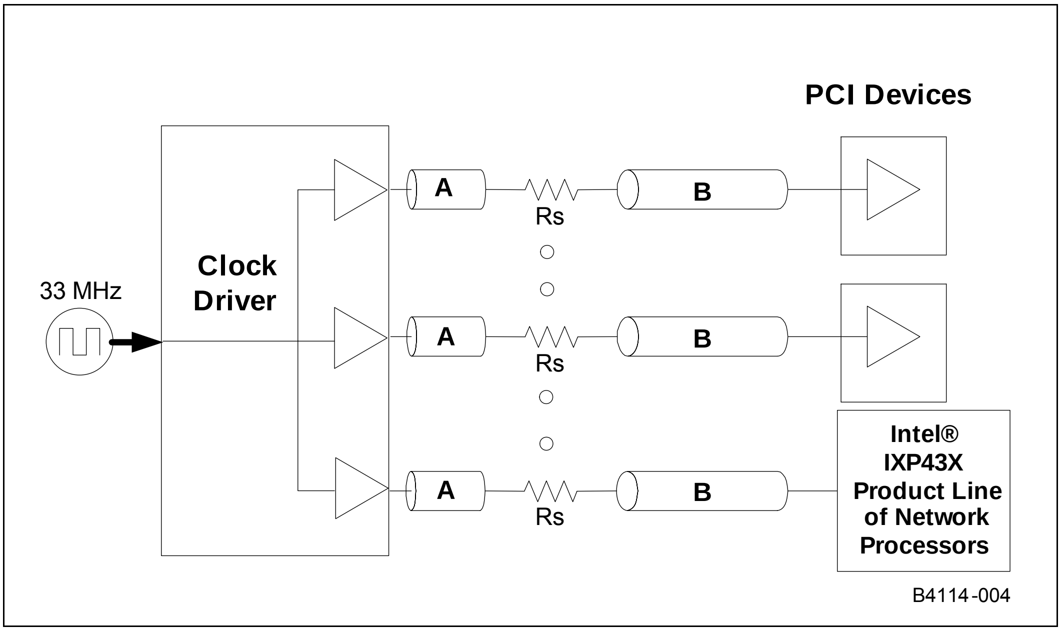

Table 23. PCI Clock Routing Guidelines

Parameter	Routing Guidelines
Signal Group	PCI Clock
Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 Ω ±10%
Nominal Trace Width	5 mils
Nominal Trace Separation	10 mils
Spacing to Other Groups	20 mils
Trace length A	Maximum 300 mils
Trace length B	There is no limit as long as the trace length is maintained for each clock and that maximum clock skew is not violated.
Resistor Rs	22 Ω ±10%
Maximum VIAS	6

6.3.1 Trace Length Limits

Maximum trace lengths can be calculated for specific speeds at which the bus is intended to run. The limitations of the maximum trace length can be calculated with the equations shown in Section 6.2. Solve for T_{PROP} and use it to calculate the maximum trace length. This is a straight-forward calculation, but very critical to meet timing. It is recommended to keep the trace lengths as short as possible and not to exceed T_{PROP}.

Note: For acceptable signal integrity at up to 33 MHz, it is very important to design the PCB board with controller impedance in the range of 55 Ω ±10%.

6.3.2 Routing Guidelines

It is recommended to route signals with respect to an adjacent ground plane. If routing signals over power planes, ensure that the signals are referenced to a single power plane voltage level and not multiple levels. For example, you can route signals over a 3.3 V plane or a 5 V plane, but do not route the same signal over both planes. If signals are routed over split planes, you must connect the splitting planes with 0.01 µF, high-speed capacitors near the signal crossing the split. The capacitors should not be placed more than 0.25 inches from the point at which the signals cross the split.

This manual does not repeat all the guidelines that are already stated in the *PCI Local Bus Specification*, Rev. 2.2. Refer to the specification when designing a motherboard or an expansion card.

6.3.3 Signal Loading

Shared PCI signals must be limited to one load on each of the PCI slots. Any violation of expansion board or add-on device trace length or loading limits compromises system-signal integrity.

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7.0 DDRII / DDRI SDRAM

7.1 Introduction

This document is intended to be used as a guide for routing DDRII/DDRI SDRAM based on the Intel® IXP435 Multi-Service Residential Gateway Reference Platform. It contains routing guidelines and simulation results for using x16 Thin Small Outline Package (TSOP) memory devices soldered onto the processor module.

The memory controller only corrects single bit ECC errors on read cycles. The ECC is stored into the DDRII/DDRI SDRAM array along with the data and is checked when the data is read. If the code is incorrect, the MCU corrects the data before reaching the initiator of the read. ECC error scrubbing is done with software. User-defined fault correction software is responsible for scrubbing the memory array and handling double-bit errors.

To limit double-bit errors from occurring, periodically read the entire usable memory array to allow the hardware unit within the memory controller to correct any single-bit. This also prevents the ECC errors that would have occurred prior to these errors becoming double-bit ECC errors. Implementing this method is system-dependent.

Note: It is important to note that when sub-word writes (byte writes or half-word writes within a word-aligned boundary) are done to a 32-bit memory with ECC enabled, the memory controller performs read-modify writes. There is a performance impact with read-modify writes that must be considered when writing software.

With read-modify writes, the memory controller reads the 32-bit word that encompasses the byte that is to be written when a byte write is requested. The memory controller modifies the specified byte, calculates a new ECC, and writes the entire 32-bit word back into the memory location it was read from.

The value written back into the memory location contains the 32-bit word with the modified byte and the new ECC value.

The MCU supports two physical banks of DDRII/DDRI SDRAM. The MCU has support for unbuffered DDRI 266 and DDRII 400 in the form of discrete chips only.

The MCU supports a memory subsystem ranging from 32 MB to 1 GB for 32-bit memory systems for DDRI SDRAM, from 64 MB to 512 MB for 32-bit memory systems for DDRII SDRAM, and supports 16 MB for 16-bit memory systems for DDRI SDRAM (non-ECC), and 32 MB for 16-bit memory systems for DDRII SDRAM (non-ECC). An ECC or non-ECC system can be implemented using x8, or x16 devices. Table 25, Table 26, Table 27 and Table 28 illustrate the supported DDRII/DDRI SDRAM configurations

The two DDRII/DDRI SDRAM chip enables (DDR_CS_N[1:0]) support a DDRII/DDRI SDRAM memory subsystem consisting of two banks. The base address for the two contiguous banks are programmed in the DDRII/DDRI SDRAM Base Register (SDBR) and is aligned to a 16 MB boundary. The size of each DDRII/DDRI SDRAM bank is programmed with the DDRII/DDRI SDRAM boundary registers (SBR0 and SBR1).

The DDRII/DDRI SDRAM devices comprise four internal leaves. The MCU controls the leaf selects within DDRII/DDRI SDRAM by toggling DDR_BA[0] and DDR_BA[1].

Table 24. DDRII/I Signal Groups

Group	Signal Name	Description
Clocks	D_CK[2:0] / DDR_CK[2:0]	DDRII/I SDRAM Differential Clocks
	D_CK_N[2:0] / DDR_CK_N[2:0]	DDRII/I SDRAM Inverted Differential Clocks
Data	D_CB[7:0] / DDR_CB[7:0]	ECC Data
	D_DQ[31:0] / DDR_DQ[31:0]	Data Bus
	D_DQS[4:0] / DDR_DQS[4:0]	Data Strobes
	D_DQS_N[4:0]	Complementary Data Strobes
	D_DM[4:0] / DDR_DM[4:0]	Data Mask
Control	D_CKE[1:0] / DDR_CKE[1:0]	Clock Enable - one per bank
	D_CS_N[1:0] / DDR_CS_N[1:0]	Chip Select - one per bank
Command	D_MA[13:0] / DDR_MA[13:0]	Address Bus
	D_BA[1:0] / DDR_BA[1:0]	Bank Select
	D_RAS_N / DDR_RAS_N	Row Address Select
	D_CAS_N / DDR_CAS_N	Column Address Select
	D_WE_N / DDR_WE_N	Write Enable

Figure 25. Processor-DDRII/I SDRAM Interface

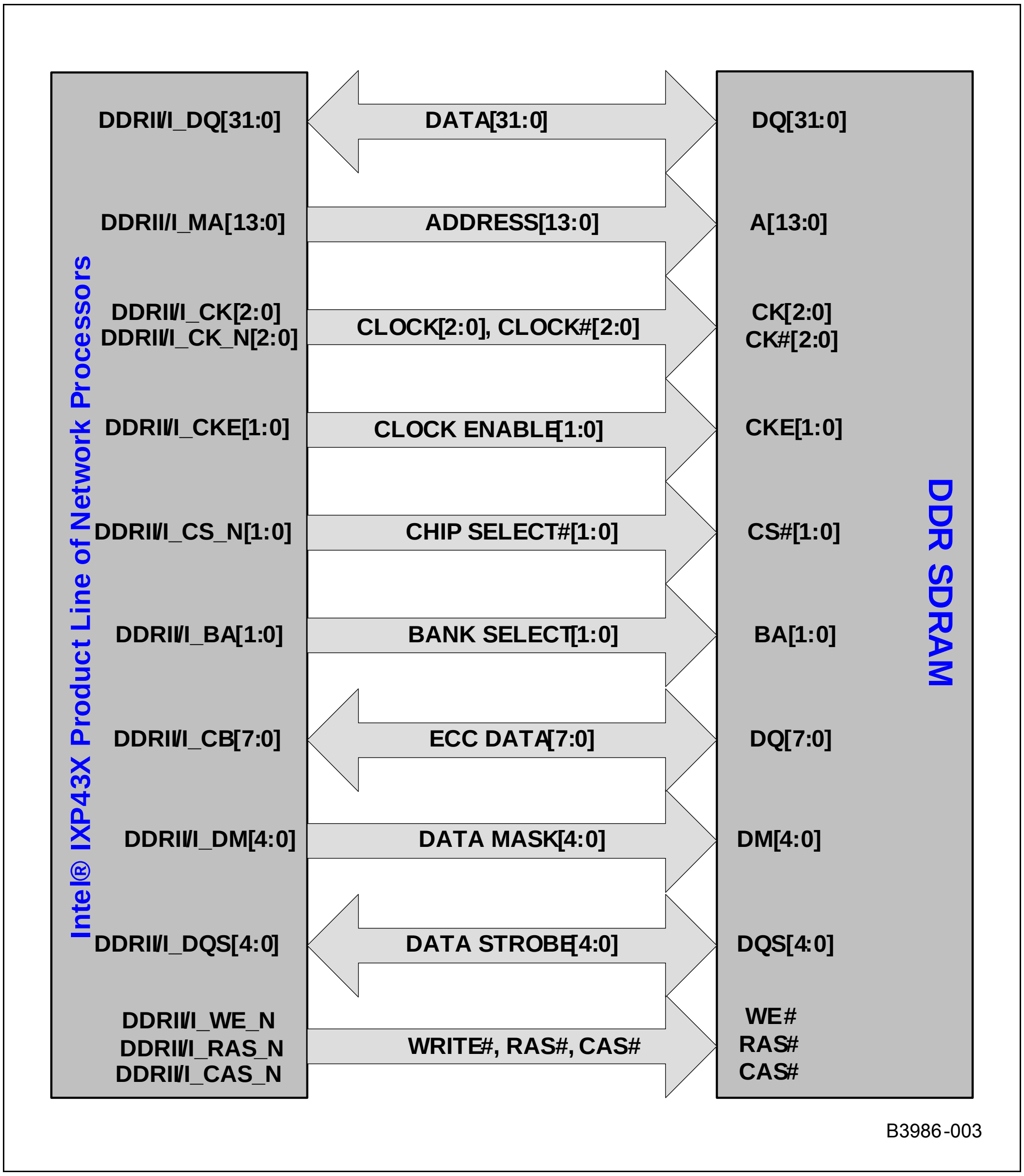


Table 25. Supported DDRI 32-bit SDRAM Configurations

DDR SDRAM Technology	DDR SDRAM Arrangement	# Banks	Address Size		Leaf Select		Total Memory Size[a]	Page Size[b]
			Row	Column	DDR_BA[1]	DDR_BA[0]		
128 Mbit[c]	16 M x 8	1	12	10	**ADDR[26]**	**ADDR[25]**	64 M	4KB
		2					128 M	4KB
	8 M x 16	1	12	9	**ADDR[25]**	**ADDR[24]**	32 M	2KB
		2					64 M	2KB
256 Mbit	32 M x 8	1	13	10	**ADDR[27]**	**ADDR[26]**	128 M	4KB
		2					256 M	4KB
	16 M x 16	1	13	9	**ADDR[26]**	**ADDR[25]**	64 M	2KB
		2					128 M	2KB
512 Mbit	64 M x 8	1	13	11	**ADDR[28]**	**ADDR[27]**	256 M	8KB
		2					512 M	8KB
	32 M x 16	1	13	10	**ADDR[27]**	**ADDR[26]**	128 M	4KB
		2					256 M	4KB
1 Gbit[c]	128 M x 8	1	14	11	**ADDR[29]**	**ADDR[28]**	512 M	8KB
		2					1 G	8KB
	64 M x 16	1	14	10	**ADDR[28]**	**ADDR[27]**	256 M	4KB
		2					512 M	4KB

a. Table indicates 32-bit wide memory subsystem sizes.
b. Table indicates 32-bit wide memory page sizes.
c. Supported with DDR SDRAM only

Table 26. Supported DDRII 32-bit SDRAM Configurations

DDR SDRAM Technology	DDR SDRAM Arrangement	# of Banks	Address Size		Leaf Select		Total Memory Size	Page Size
			Row	Column	DDR_BA[1]	DDR_BA[0]		
256 Mbit	32M x 8	1	13	10	ADDR[27]	ADDR[26]	128MB	4KB
		2					256MB	4KB
	16M x16	1	13	9	ADDR[26]	ADDR[25]	64MB	2KB
		2					128MB	2KB
512 Mbit	64M x 8	1	14	10	ADDR[28]	ADDR[27]	256MB	4KB
		2					512MB	4KB
	32M x16	1	13	10	ADDR[27]	ADDR[26]	128MB	4KB
		2					256MB	4KB

Table 27. Supported DDRI 16-bit SDRAM Configurations

DDR SDRAM Technology	DDR SDRAM Arrangement	# of Banks	Address Size		Leaf Select		Total Memory Size	Page Size
			Row	Column	DDR_BA[1]	DDR_BA[0]		
128 Mbit	8M x16	1	12	9	ADDR[23]	ADDR[22]	16MB	1KB

Table 28. Supported DDRII 16-bit SDRAM Configurations

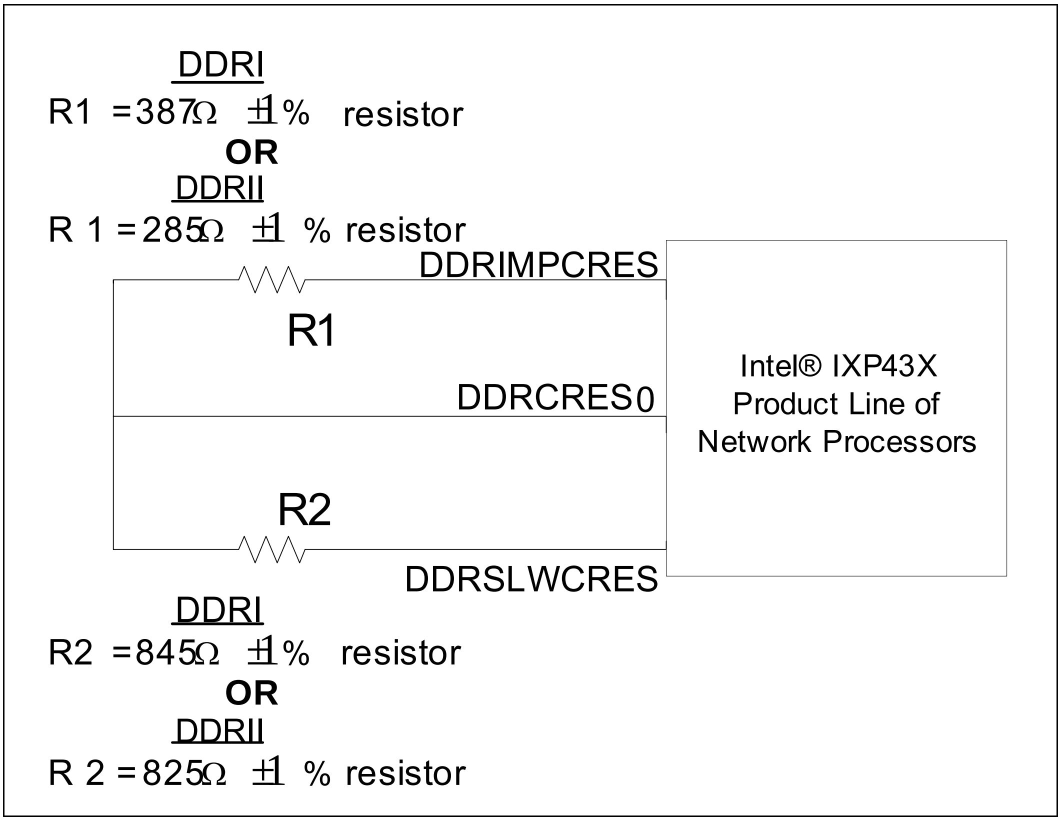
DDR SDRAM Technology	DDR SDRAM Arrangement	# of Banks	Address Size		Leaf Select		Total Memory Size	Page Size
			Row	Column	DDR_BA[1]	DDR_BA[0]		
256 Mbit	16M x16	1	13	9	ADDR[24]	ADDR[23]	32MB	1KB

The DDR_RCOMP signal must be terminated through resistors specified in Figure 26. This allows the DDRII/I controller to make temperature and process adjustments.

7.2 DDRII/DDRI RCOMP and Slew Resistances Pin Requirements

Figure 26 shows the requirements for the DDRII/DDRI RCOMP pin.

Figure 26. DDRII/DDRI RCOMP Pin External Resistor Requirements

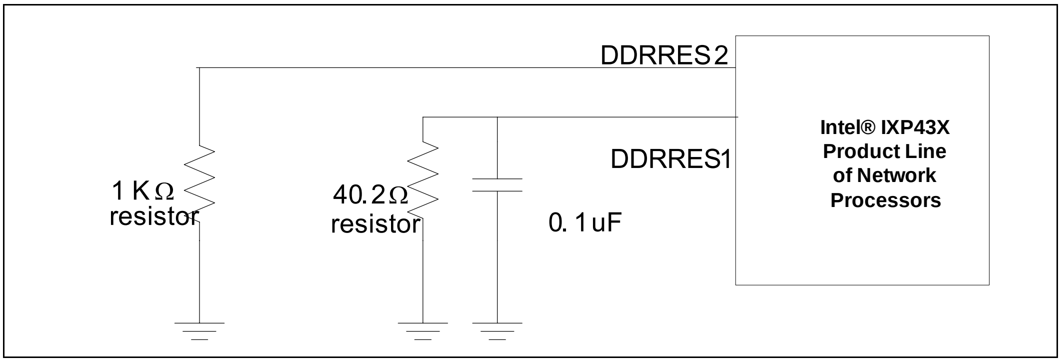


For example, when DDRI SDRAM is used, DDRIMPCRES is connected with 387Ω and DDRSLWCRES is connected with 845Ω resistor to DDRCRES0.

7.3 DDRII OCD Pin Requirements

Figure 27 shows the requirement for the DDRRES1 and DDRRES2 pins.

Figure 27. DDRII OCD Pin Requirements



Note: Since the OCD calibration function is not enabled, DDRRES2 must be pulled to ground with a 1-KΩ resistor.

7.3.1 Signal-Timing Analysis

Figure 28. DDR Clock Timing Waveform

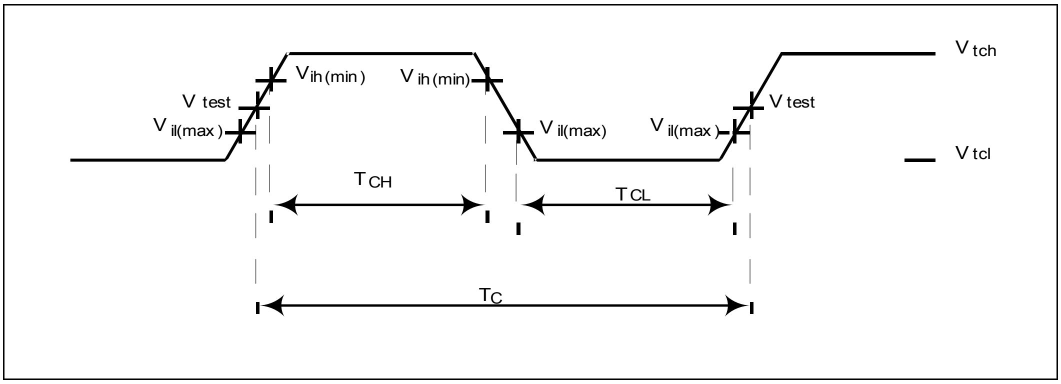


Table 29. DDR Clock Timings

Symbol	Parameter	DDR-II 400		DDR-I 266		Units	Notes
		Min	Max	Min	Max		
T_F	DDR SDRAM clock Frequency		200		133	MHz	
T_C	DDR SDRAM clock Cycle Time	5		7.5		ns	1
T_{CH}	DDR SDRAM clock High Time	2.15		3.37		ns	1
T_{CL}	DDR SDRAM clock Low Time	2.15		3.37		ns	1
T_{CS}	DDR SDRAM clock Period Stability		350		350	ps	
T_{skew}	DDR SDRAM clock skew for any differential clock pair (D_CK[2:0] - D_CK_N[2:0])		100		100	ps	

Notes:
1. See Figure 28, “DDR Clock Timing Waveform” on page 76
2. Vtest is nominally (0.5 * Vtch - Vtcl)

Figure 29. DDR SDRAM Write Timings

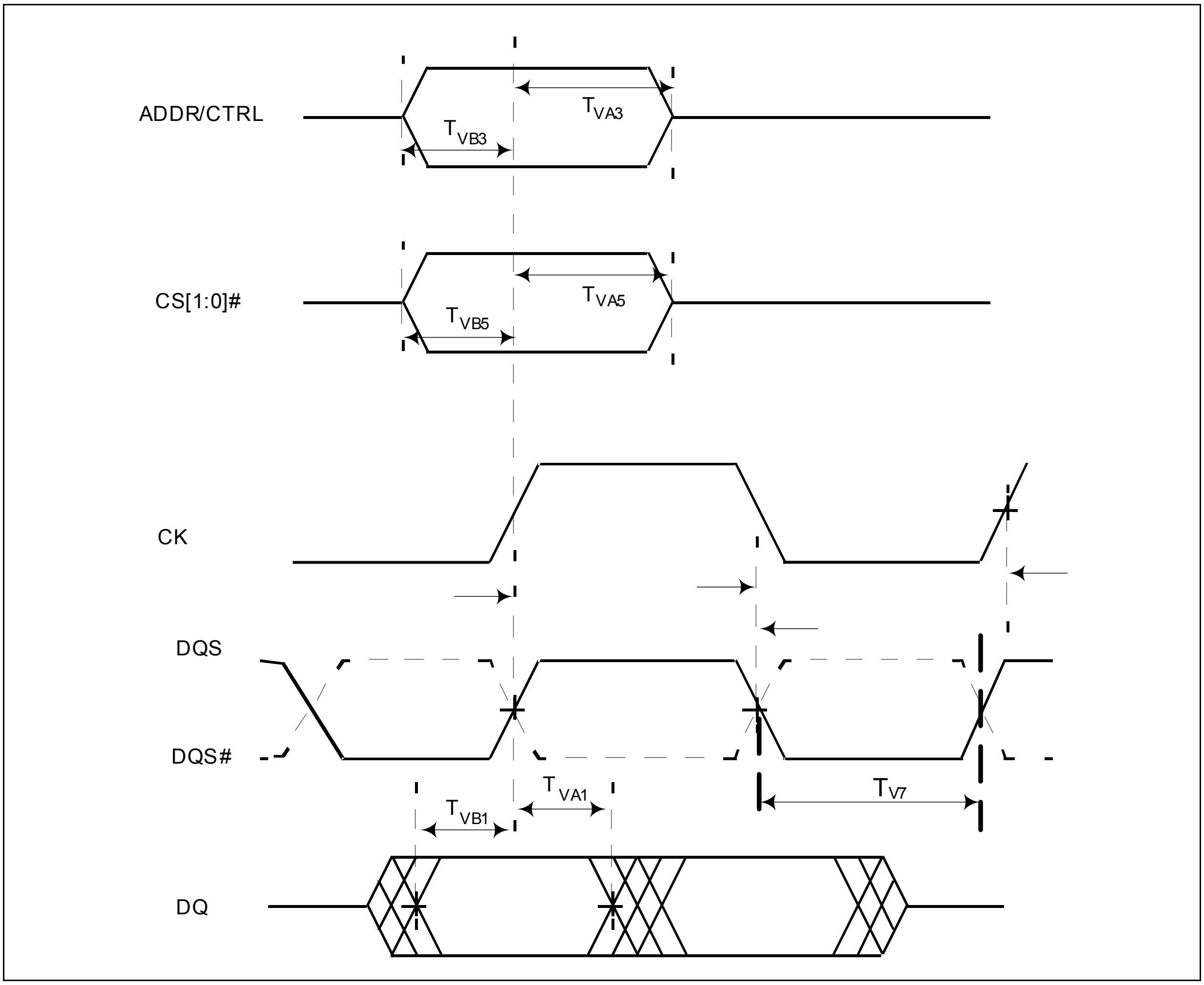


Figure 30. DDR SDRAM Read Timings

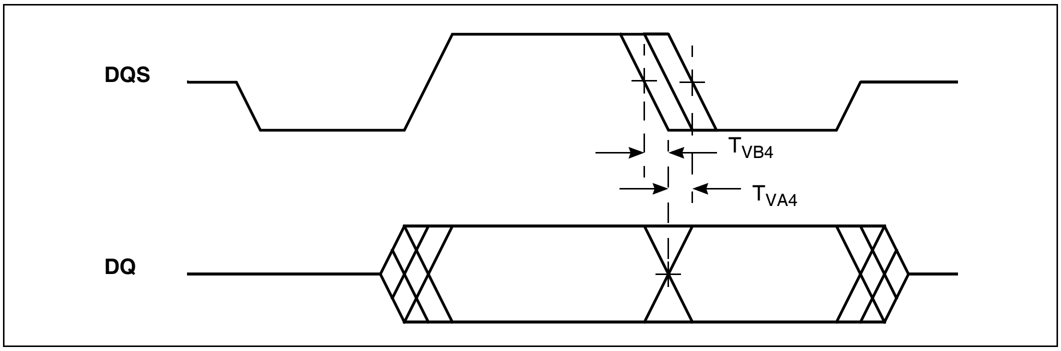


Figure 31. DDR - Write Preamble/Postamble Duration

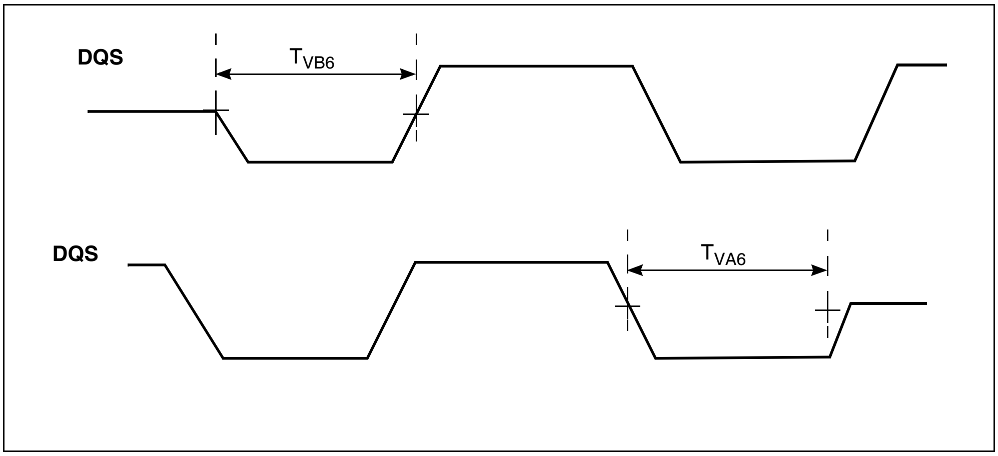


Table 30. DDRII-400 MHz Interface -- Signal Timings

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
T_{VB1}	DQ, CB and DM write output valid time before DQS.	521			ps	1
T_{VA1}	DQ, CB and DM write output valid time after DQS.	521			ps	1
T_{VB3}	Address and Command write output valid before CK rising edge.	1771			ps	1, 4
T_{VA3}	Address and Command write output valid after CK rising edge.	1771			ps	1, 4
T_{VB4}	DQ, CB and DM read input valid time before DQS rising or falling edges.	323			ps	2
T_{VA4}	DQ, CB and DM read input valid time after DQS rising or falling edges.	323			ps	2
T_{VB5}	CS_N[1:0] control valid before CK rising edge.	1771			ps	4
T_{VA5}	CS_N[1:0] control valid after CK rising edge.	1771			ps	4
T_{VB6}	DQS write preamble duration.		3750		ps	3
T_{VA6}	DQS write postamble duration.		2500		ps	3
T_{V7}	DQ, CB, and DM pulse width (tDIPW)		1750		ps	1

Notes:

1. See Figure 29, “DDR SDRAM Write Timings” on page 77
2. See Figure 30, “DDR SDRAM Read Timings” on page 77. The specified minimum requirements for the “Data to strobe read setup” and “Data from strobe read hold” are determined with the DQS delay programmed for 90 degree phase shift.
3. See Figure 31, “DDR - Write Preamble/Postamble Duration” on page 78
4. Address/Command pin group; RAS_N, CAS_N, WE_N, MA[13:0], BA[1:0]
5. Designed to JEDEC specification; it is recommended that IBIS models should be used to verify signal integrity on individual designs

Table 31. DDR II/I SDRAM Interface -- Signal Timings

Symbol	Parameter	Minimum	Nom.	Maximum	Units	Notes
T_{VB1}	DQ, CB and DM write output valid time before DQS.	1146			ps	1
T_{VA1}	DQ, CB and DM write output valid time after DQS.	1146			ps	1
T_{VB3}	Address and Command write output valid before CK rising edge.	3021			ps	1, 4
T_{VA3}	Address and Command write output valid after CK rising edge.	3021			ps	1, 4
T_{VB4}	DQ, CB and DM read input valid time before DQS rising or falling edges.	948			ps	2
T_{VA4}	DQ, CB and DM read input valid time after DQS rising or falling edges.	948			ps	2
T_{VB5}	CS_N[1:0] control valid before CK rising edge.	3021			ps	4
T_{VA5}	CS_N[1:0] control valid after CK rising edge.	3021			ps	4
T_{VB6}	DQS write preamble duration.		5625		ps	3
T_{VA6}	DQS write postamble duration.		3750		ps	3
T_{V7}	DQ, CB, and DM pulse width (tDIPW)		1750		ps	1

Notes:

1. See Figure 29, “DDR SDRAM Write Timings” on page 77
2. See Figure 30, “DDR SDRAM Read Timings” on page 77. The specified minimum requirements for “Data to strobe read setup” and “Data from strobe read hold” are determined with the DQS delay programmed for 90 degree phase shift.
3. See Figure 31, “DDR - Write Preamble/Postamble Duration” on page 78
4. Address/Command pin group; RAS_N, CAS_N, WE_N, MA[13:0], BA[1:0]
5. Designed to JEDEC specification; it is recommended that IBIS models should be used to verify signal integrity on individual designs

7.3.1.0.1 Printed Circuit Board Layer Stackup

The layer stackup used for the Intel® IXP435 Multi-Service Residential Gateway Reference Platform is a 6-layer, printed circuit board with four signal layers and two plane layers.

Details on the voltage reference layout are available in the CAD database or Gerber files database for the Intel® IXP435 Multi-Service Residential Gateway Reference Platform.

7.3.2 Timing Relationships

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width, spacing geometries, and typical routed lengths for each signal group. These parameters are recommended to achieve optimal signal integrity and timing.

All signal groups are length matched to the DDR clocks. The clocks on the processor module are length matched to within ±10 mils of each other. Once this overall clock length for any given DDR differential clock is determined, the command and control signals can be routed to within the timing specified. A simple summary of the timing results for each signal group is provided in Table 32 on page 80.

Control/Command Group to Clock Summary:

- The maximum allowable difference from any command/control signal to the clock is ±0.6 ns.

  - — Table 31 on page 79

Data Group to Strobe Summary:

- The more restrictive data group to strobe timing occurs for read operations
  - — Table 32 on page 80
  - — Table 33 on page 80
- The maximum allowable difference from any data group signal to the strobe is ±0.25 ns.
  - — Figure 30 on page 77
  - — Table 32 on page 80

Strobe to Clock Summary:

- The maximum allowable difference from any data strobe signal to the clock is -0.475 ns to +0.875 ns
  - — Figure 32 on page 83
  - — Table 34 on page 83

These are absolute maximum ratings for length mismatch based in ideal printed board conditions (exact signal propagation delays, ideal signal integrity with no reflections or settling, zero rise/fall times, and so on.). To compensate for these non-ideal conditions, more restrictive length matching conditions should be used based on signal integrity analysis and simulation to provide a buffer zone and avoid possible variations in silicon or printed circuit board manufacture.

Table 32. Timing Relationships

Signal Group	Absolute Minimum Length	Absolute Maximum Length
Control to Clock	Clock – 600 ps	Clock + 600 ps
Command to Clock	Clock – 600 ps	Clock + 600 ps
Data to Strobe	Strobe – 250 ps	Strobe + 250 ps
Strobe to Clock	Clock – 475 ps	Clock + 875 ps

In addition to any trace length differentials which must be considered between signal groups, differences in the package length between signals should be considered when determining the total propagation delay of the signals. When using the IXP435 reference platform IBIS model for signal analysis, package characteristics are included in the simulation results.

Table 33. Signal Package Lengths (Sheet 1 of 3)

Group	Signal Name	Length (mil)	Signal Name	Length (mil)
Clock	D_CK_N0 / DDR_CK_N0	558.19	D_CK0 / DDR_CK0	507.46
	D_CK_N1 / DDR_CK_N1	385.12	D_CK1 / DDR_CK1	385.12
	D_CK_N2 / DDR_CK_N2	504.20	D_CK2 / DDR_CK2	548.01

Table 33. Signal Package Lengths (Sheet 2 of 3)

Group	Signal Name	Length (mil)	Signal Name	Length (mil)
Data	D_CB0 / DDR_CB0	402.94	D_CB4 / DDR_CB4	385.50
	D_CB1 / DDR_CB1	393.93	D_CB5 / DDR_CB5	419.24
	D_CB2 / DDR_CB2	377.69	D_CB6 / DDR_CB6	398.22
	D_CB3 / DDR_CB3	378.47	D_CB7 / DDR_CB7	435.03
	D_DQ0 / DDR_DQ0	447.57	D_DQ16 / DDR_DQ16	536.32
	D_DQ1 / DDR_DQ1	449.41	D_DQ17 / DDR_DQ17	569.24
	D_DQ2 / DDR_DQ2	394.02	D_DQ18 / DDR_DQ18	545.35
	D_DQ3 / DDR_DQ3	366.03	D_DQ19 / DDR_DQ19	633.70
	D_DQ4 / DDR_DQ4	449.58	D_DQ20 / DDR_DQ20	604.01
	D_DQ5 / DDR_DQ5	470.40	D_DQ21 / DDR_DQ21	608.22
	D_DQ6 / DDR_DQ6	413.35	D_DQ22 / DDR_DQ22	479.46
	D_DQ7 / DDR_DQ7	384.02	D_DQ23 / DDR_DQ23	555.12
	D_DQ8 / DDR_DQ8	368.37	D_DQ24 / DDR_DQ24	472.85
	D_DQ9 / DDR_DQ9	399.54	D_DQ25 / DDR_DQ25	475.30
	D_DQ10/ DDR_DQ10	374.55	D_DQ26 / DDR_DQ26	421.35
	D_DQ11 / DDR_DQ11	398.20	D_DQ27 / DDR_DQ27	419.04
	D_DQ12 / DDR_DQ12	396.30	D_DQ28 / DDR_DQ28	480.43
	D_DQ13 / DDR_DQ13	408.81	D_DQ29 / DDR_DQ29	489.89
	D_DQ14 / DDR_DQ14	371.03	D_DQ30 / DDR_DQ30	430.18
	D_DQ15 / DDR_DQ15	388.23	D_DQ31 / DDR_DQ31	431.50
	D_DQS0 / DDR_DQS0	468.21	D_DQS2 / DDR_DQS2	517.45
	D_DQS1 / DDR_DQS1	371.60	D_DQS3 / DDR_DQS3	463.84
	D_DM0 / DDR_DM0	410.19	D_DQS4 / DDR_DQS4	653.53
	D_DM1 / DDR_DM1	482.30	D_DM3 / DDR_DM3	536.80
	D_DM2 / DDR_DM2	553.44	D_DM4 / DDR_DM4	428.52
Control	D_CKE0 / DDR_CKE0	385.61	D_CKE1 / DDR_CKE1	384.34
	D_CS_N0 / DDR_CS_N0	385.35	D_CS_N1 / DDR_CS_N1	421.27

Table 33. Signal Package Lengths (Sheet 3 of 3)

Group	Signal Name	Length (mil)	Signal Name	Length (mil)
Command	D_MA0 / DDR_MA0	515.78	D_MA7 / DDR_MA7	438.95
	D_MA1 / DDR_MA1	357.69	D_MA8 / DDR_MA8	394.65
	D_MA2 / DDR_MA2	509.12	D_MA9 / DDR_MA9	429.78
	D_MA3 / DDR_MA3	462.16	D_MA10 / DDR_MA10	378.96
	D_MA4 / DDR_MA4	444.71	D_MA11 / DDR_MA11	418.37
	D_MA5 / DDR_MA5	576.87	D_MA12 / DDR_MA12	392.79
	D_MA6 / DDR_MA6	513.40	D_MA13 / DDR_MA13	433.55
	D_BA0 / DDR_BA0	530.35	D_BA1 / DDR_BA1	535.27
	D_RAS_N / DDR_RAS_N	506.35	D_CAS_N / DDR_CAS_N	477.26
	D_WE_N / DDR_WE_N	513.09		

7.3.3 Routing Guidelines

7.3.3.1 Clock Group

The clock signal group includes the differential clock pairs D_CK[2:0] / DDR_CK[2:0] and D_CK_N[2:0] / DDR_CK_N[2:0].

Here are some tips on how to route the differential clock pairs:

- Ensure that DDR clocks are routed on a single internal layers, except for pin escapes
- A ground plane must be adjacent to the layer where the signals are routed
- Minimize the number of vias used, but ensure that the same number of vias are used in the positive and negative trace
- It is recommended that pin escape vias be located directly adjacent to the ball pads on all clocks
- Traces must be routed for differential mode impedance of 120 Ω
- Surface layer routing should be minimized (top or bottom layers)
- It is recommended to perform pre- and post-layout simulation

A series resistance value in the 25- to 50-Ω range should be used as it adds minimal propagation delay to the signal without adversely varying from the CLK plus DQ propagation delay average. The appropriate value for termination resistance should be verified through simulation for the specific topology.

Table 34 provides routing guidelines for signals within this group.

Figure 32. DDRII Clock Simulation Results: CK Signals

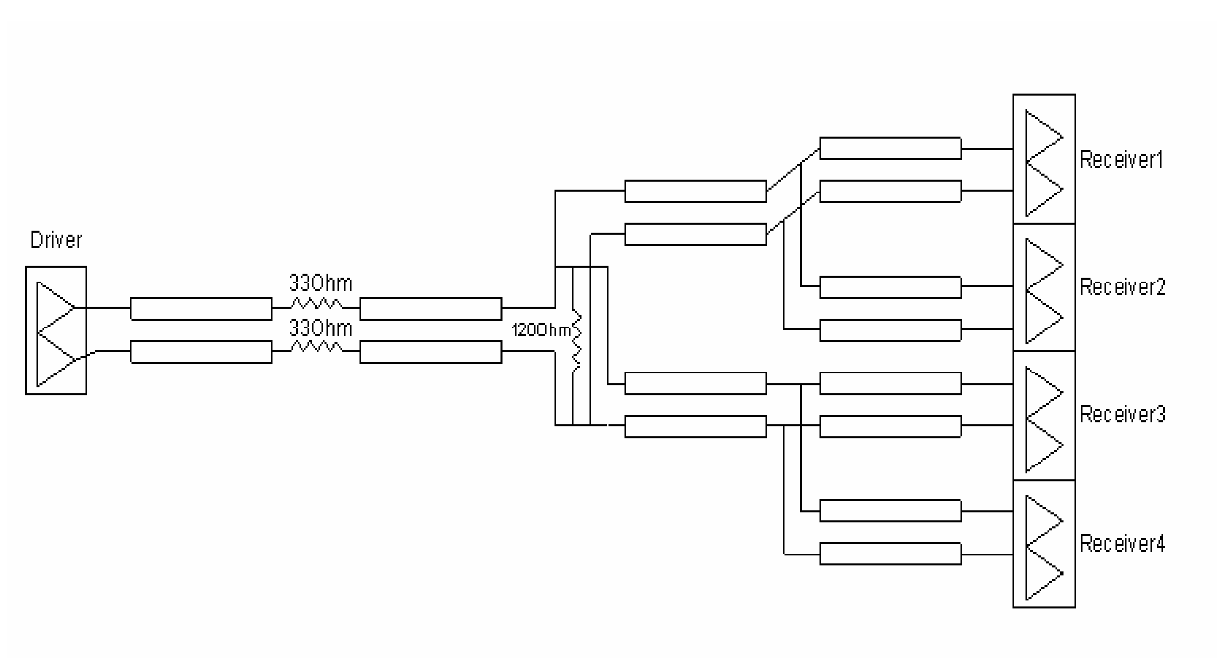


Table 34. Clock Signal Group Routing Guidelines

Parameter	Definition
Signal Group Members	D_CK[2:0] and D_CK_N[2:0]
Topology	Differential Pair Point to Point (1 Driver, 4 Receivers)
Single Ended Trace Impedance (Z_0)	50 Ω
Series Resistor	33 Ω
Nominal Trace Width[1]	Internal (Strip Line) 3.5 mils, External (Micro Strip) 5 mils
Nominal Pair Spacing (edge to edge) [2]	Internal (Strip Line) 10.5 mils, External (Micro Strip) 10 mils
Minimum Pair to Pair Spacing	Any layer 20mils
Minimum Spacing to Other DDR Signals	20.0 mils
Minimum Spacing to non-DDR Signals	25.0 mils
Maximum Via Count	5 per trace
Total Trace Length	500 mils to 1000 mils
DDR_CK to DDR_CK_N Length Matching	Match total length to +/- 10 mils between clocks

Notes:
1. Nominal trace width is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zo.
2. Nominal pair to pair spacing is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zdiff.

7.3.3.2 Data and Control Groups

The data and control signal group includes D_CB[7:0]/DDR_CB[7:0], D_DQ[31:0] / DDR_DQ[31:0], D_DQS[4:0]/DDR_DQS[4:0], D_DM[4:0]/DDR_DM[4:0]., D_CS[1:0]/ DDR_CS[1:0] and D_CKE[1:0]/DDR_CKE[1:0]. The groups should be routed on internal layers, except for pin escapes. It is recommended that pin escape vias be located directly adjacent to the ball pads on all signals. Surface layer routing should be minimized. The following table provides routing guidelines for signals within these groups.

Figure 33. DDRII Data and Control Simulation Results: DQ and DQS signals

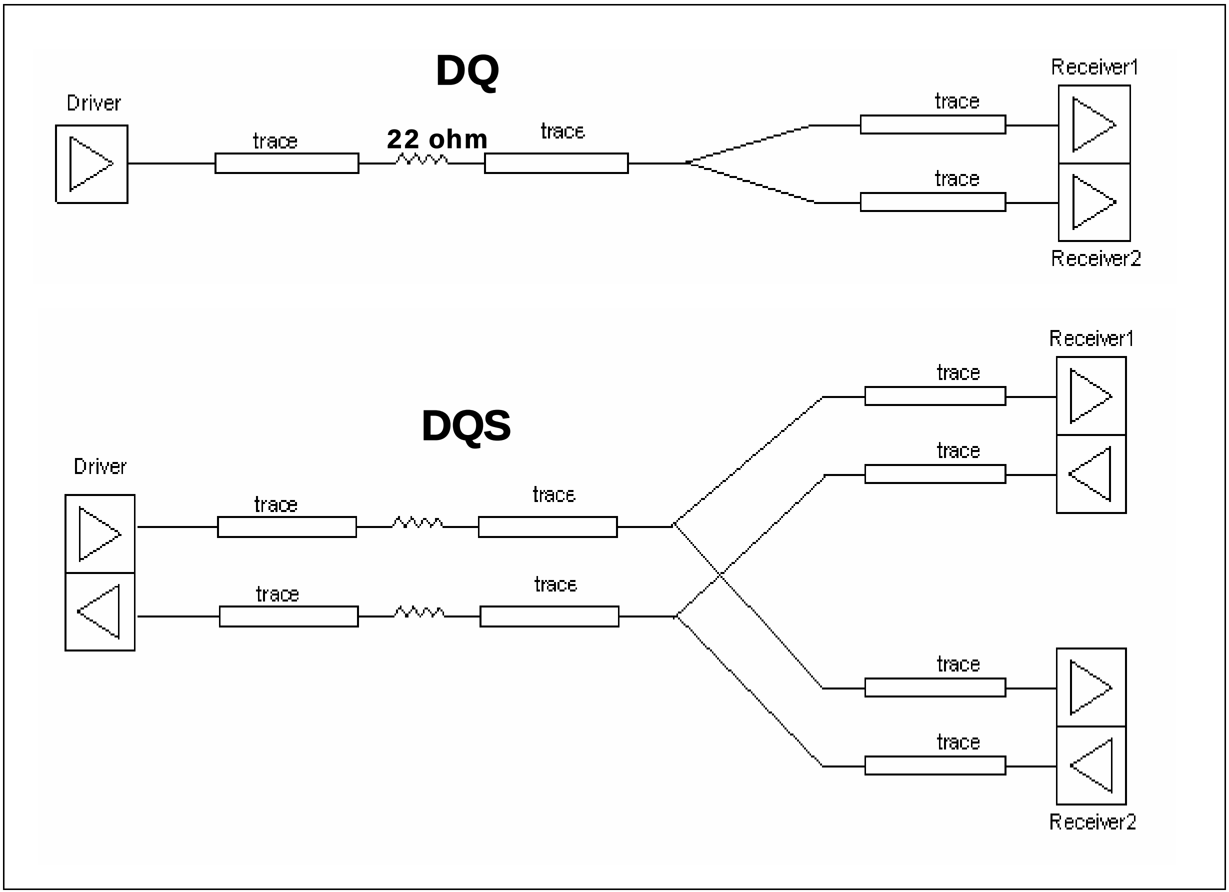


Table 35. DDRII Data and Control Signal Group Routing Guidelines

Parameter	Definition
Signal Group Members	D_CB[7:0]/DDR_CB[7:0], D_DQ[31:0] / DDR_DQ[31:0], D_DQS[4:0]/DDR_DQS[4:0], D_DM[4:0]/DDR_DM[4:0]., D_CS[1:0]/DDR_CS[1:0] and D_CKE[1:0]/DDR_CKE[1:0]
Topology	Differential Pair Point to Point (1 Driver, 2 Receivers)
Single Ended Trace Impedance (Z_o)	50 Ω
Series Resistor	22 Ω
Nominal Trace Width[1]	Internal (Strip Line) 3.5 mils, External (Micro Strip) 5 mils
Nominal Pair Spacing (edge to edge) [2]	Internal (Strip Line) 10.5 mils, External (Micro Strip) 10 mils
Minimum Pair to Pair Spacing	Any layer 20mils

Notes:

1. Nominal trace width is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zo.
2. Nominal pair to pair spacing is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zdiff.

Table 35. DDRII Data and Control Signal Group Routing Guidelines

Parameter	Definition
Minimum Spacing to Other DDR Signals	20.0 mils
Minimum Spacing to non-DDR Signals	25.0 mils
Maximum Via Count	5 per trace
Total Trace Length	1000 mils to 2000 mils

Notes:
1. Nominal trace width is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zo.
2. Nominal pair to pair spacing is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zdiff.

7.3.3.3 Command Groups

The command signal groups include all signals D_MA[13:0]/DDR_MA[13:0], D_BA[1:0]/DDR_BA[1:0], D_RAS/DDR_RAS, D_CAS/DDR_CAS and D_WE/DDR_WE. The groups should be routed on internal layers, except for pin escapes. It is recommended that pin escape vias be located directly adjacent to the ball pads on all signals. Surface layer routing should be minimized. The following table provides routing guidelines for signals within these groups.

Figure 34. DDRII Command Simulation Results: ADDRESS signals

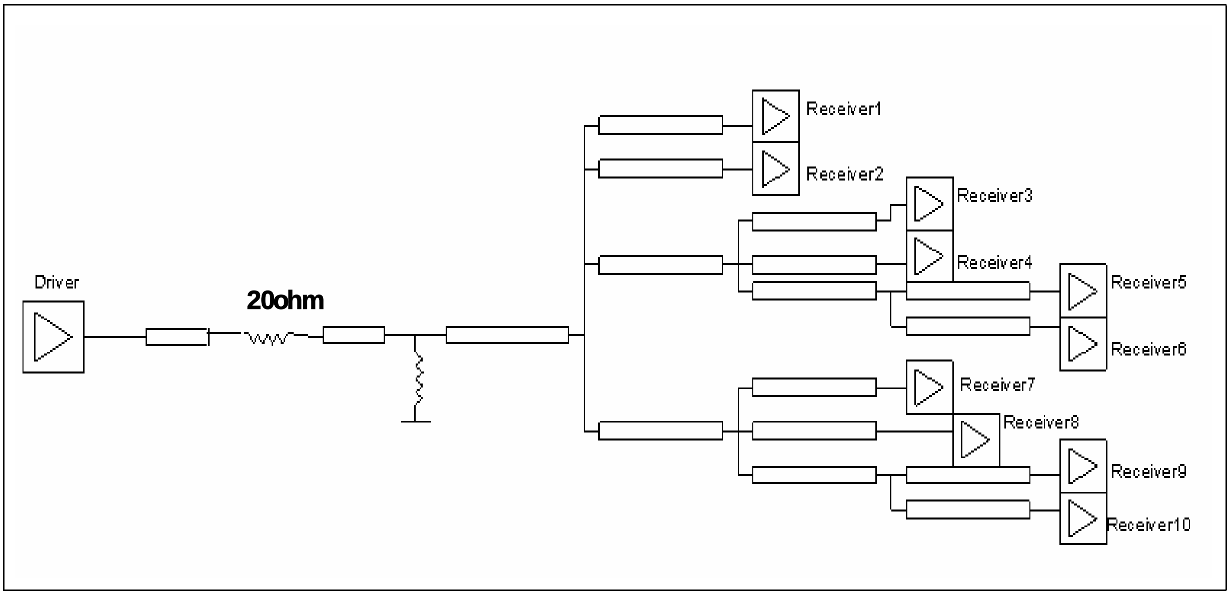


Table 36. DDRII Command Signal Group Routing Guidelines

Parameter	Definition
Signal Group Members	D_MA[13:0]/DDR_MA[13:0], D_BA[1:0]/DDR_BA[1:0], D_RAS/DDR_RAS, D_CAS/DDR_CAS and D_WE/DDR_WE.
Topology	Point to Point (1 Driver, 10Receivers)
Single Ended Trace Impedance (Z_0)	50 Ω

Notes:
1. Nominal trace width is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zo.
2. Nominal pair to pair spacing is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zdiff.

Table 36. DDRII Command Signal Group Routing Guidelines

Parameter	Definition
Series Resistor	20 Ω
Nominal Trace Width[1]	Internal (Strip Line) 3.5 mils, External (Micro Strip) 5 mils
Nominal Pair Spacing (edge to edge) [2]	Internal (Strip Line) 10.5 mils, External (Micro Strip) 10 mils
Minimum Pair to Pair Spacing	Any layer 20mils
Minimum Spacing to Other DDR Signals	20.0 mils
Minimum Spacing to non-DDR Signals	25.0 mils
Maximum Via Count	5 per trace
Total Trace Length	1500 mils to 2500 mils

Notes:

1. Nominal trace width is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zo.
2. Nominal pair to pair spacing is determined by board physical characteristics and stack-up. This value should be verified with the PWB manufacturer to achieve the desired Zdiff.

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