DSP Research

DSP376

User Manual

Revision History

Date	Comments	Engineer	Version
17/7/02	First rev, based on 361	GP	1.0.0
14/10/02	Remove SDBC, comport 2,5 and update memory mapping	Y.C	1.0.1
30/01/03	Firmware version 1.8	J.V	1.1
05/03/03	Firmware version 1.9 Update of the pinout for serial port header Table of content updated no other change	J.V.	1.4

Table of Contents

Contacting DSP Research

You can contact DSP Research for additional information by sending email to **information@dspr.com**

Notational Conventions

DSP376

Throughout this document the term DSP376 (or simply 376) will usually be used to refer to all processor variants. It should be clear from the context when a distinction is being drawn between the types of module.

C60

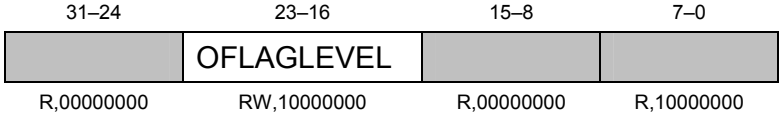
The term C60 will be used throughout this document in place of TMS320C6211, 6711 or 6713.

200 MB/sec Digital Bus

SDB or Digital Bus will be used throughout this document to refer to a 16-bit data bus carried by either a 200 MB/sec Digital Bus connector or a 400 MB/sec Digital Bus connector. The 400 MB/sec Digital Bus connector can carry two such 200 MB/sec Digital Bus buses.

Register Descriptions

The format of registers is described using diagrams of the following form:



The digits at the top of the diagram indicate bit positions within the register and the central section names bits or bit fields. The bottom row describes what may be done to the field and its value after reset. Shaded fields are reserved and should only ever be written with zeroes.

R	Readable by the CPU
W	Writeable by the CPU
RW	Readable and writeable by the CPU

Binary digits indicate the value of the field after reset.

Outline Description

The DSP376 is a C6211/6711/6713-based size 1 TIM offering the following features:

- TMS320C6211 integer processor running at 150MHz
- TMS320C6711 floating point processor running at 150MHz
- TMS320C6713 floating point processor running at 225MHz
- Four 20MB/s communication ports (comm.-ports)
- 256MBytes of SDRAM (100MHz)
- 2MByte Flash ROM for boot code and FPGA programming
- Global expansion connector
- High bandwidth data I/O via 200 MB/sec Digital Buses and
- 400 MB/sec Digital Buses

Architecture Description

The DSP376 TIM consists of a Texas Instruments TMS320C6211/6711/6713 running at up to 225MHz. Modules are populated with 256MBytes of synchronous DRAM (SDRAM).

A Field Programmable Gate Array (FPGA) is used to manage global bus accesses and implement four communication ports and 200/400 MB/sec Digital Buses. This is a Xilinx Spartan – IIE device.

TMS320C6211/6711

The processor will run with zero wait states from internal SRAM. The internal memory is 64k bytes in size and can be partitioned between normal SRAM and/or L2 cache.

An on-board crystal oscillator provides the clock used for the C60, which then multiplies this by 4 internally.

TMS320C6713

The processor will run with zero wait states from internal SRAM. The internal memory is 256k bytes in size and can be partitioned between normal SRAM and/or L2 cache.

An on-board crystal oscillator provides the clock used for the C60, which then multiplies this by a programmable amount internally to provide the required core and EMIF clocks.

Boot Mode

The DSP376 is configured to use the following boot sequence each time it is taken out of reset:

1. The processor copies a bootstrap program from the first part of the flash memory into internal program RAM starting at address 0.
2. Execution starts at address 0.

The standard bootstrap supplied with the DSP376 then performs the following operations:

1. All relevant C60 internal registers are set to default values.
2. The FPGA is configured from data held in flash memory and sets up the communication ports, the global bus and the 200/400 MB/sec Digital Buses. This step must have been completed before data can be sent to the comm-ports from external sources such as the host or other TIMs.
3. A C4x-style boot loader is executed. This will continually examine the four communication ports until data appears on one of them. The bootstrap will then load a program in boot format from that port; the loader will not read data arriving on other ports. See “Application Development” for details of the boot loader format.
4. Finally, control is passed to the loaded program.

The delay between the release of the board reset and the FPGA configuration is around 0.5s for a DSP376 (150MHz clock).

A typical time to wait after releasing the board reset should be in excess of this delay, but no damage will result if any of the I/Os are used before they are fully configured. In fact, the comm. Ports will just produce a not ready signal when data is attempted to be transferred during this time, and then continue normally after the FPGA is configured.

EMIF Control Registers

The C60 has a single external memory interface (EMIF) which is 32 bits wide.

The C60 contains several registers that control the external memory interface (EMIF). A full description of these registers can be found in the *C60 Peripherals Reference Guide*.

The standard bootstrap will initialize these registers to use the following resources:

Memory space (EMIF)	Resource	Address range
CE0	Spartan	0x80000000 - 0x8FFFFFFF
CE1	Flash	0x90000000 - 0x901FFFFF
CE2	SDRAM bank 0	0xA0000000 - 0xA7FFFFFF
CE3	SDRAM bank 1	0xB0000000 - 0xB7FFFFFF

SDRAM

Memory spaces CE2 & 3 are used to access 256MB of SDRAM over the EMIF.

The speed of the SDRAM is dependant on the processor variant. Using the C6x11, the SDRAM will operate at 100MHz.

Using the C6713, the SDRAM operates at a programmable rate up to the maximum allowed on the EMIF (TI data sheet = TBD).

The EMIF CE2 & 3 memory space control registers should be programmed with the value 0x00000030.

FLASH

A 2MByte Flash ROM device is connected to the C60 EMIF CE1 memory space.

The ROM holds boot code for the C60, configuration data for the FPGA, and optional user-defined code.

A software protection algorithm is in place to prevent programs accidentally altering the ROM's contents. Please contact DSP Research for further information about re-programming this device.

The CE1 memory space control register should be programmed with the value 0x105FFF23.

Version control

Revision numbers for both the boot code and FPGA firmware are stored in the Flash ROM during programming as zero-terminated ASCII strings.

The distribution disk contains a program, **`read_version_376.out`**, in the directory **`Reprogramming\version_control`**. You can load and run this program from code composer to display both the FPGA and boot code version numbers.

Reprogramming the firmware and boot code

The **`Reprogramming\flash`** directory of the distribution disk contains a utility that will run under code composer and program the flash ROM. The utility is called **`pflash`*`x_y_z`*`.out`**, where ***`x_y_z`*** is the FPGA version number.

You load the utility with the code composer "Load Program" option from the "File" menu. Once the program has loaded, you should select "Run" from the "Debug" menu. The reprogramming process takes a minute or so and should display "Flash programming complete" when it has finished. After the program has run you should select "Run Free". To confirm that the programming has been successful you should use the DSP Research Server to reset the board and execute one of the supplied test programs, or execute the confidence test using SMTBoardInfo.

A detailed description of the reprogramming process is available as an Application Note, which will also help you to develop your own core in the FPGA.

Interrupts

See general firmware description.

Communication ports

The DSP376 provides 4 comm-ports. They are Comm-port 0, 1, 3 and 4.

Comm-port 2 and 5 are interconnected on the module to allow a bypass to the next module.

See general firmware description.

200 MB/sec Digital Bus

The DSP376 provides two 200 MB/sec Digital Buses. These 16-bit data parallel links for synchronous transmission can achieve high-speed data transfer across 40-way flat ribbon cables with ground-interlaced 3.3v signals and Samtec QSH/QTH based cable designs.

The 200 MB/sec Digital Bus connector carries one 16 bits 200 MB/sec Digital Bus (SDB0).

The 400 MB/sec Digital Bus connector carries one 16 bits 200 MB/sec Digital Bus (SDB1). The second 16 200 MB/sec Digital Bus is not implemented.

See general firmware description.

200 MB/sec Digital Bus Clock selection

In this firmware the 200 MB/sec Digital Bus clock is not selectable and is fixed at 100MHz.

Changing the bit SDBCLK will have no effect.

Global bus

The DSP335 provides one global bus interface.

See general firmware description.

LED Setting

The DSP376 has 5 LEDs.

LED D6 always displays the state of the FPGA DONE pin. This LED is off when the FPGA is configured (DONE=1) and on when it is not configured (DONE=0).

This LED should go on when the board is first powered up and go off when the FPGA has been successfully programmed (this is the standard operation of the boot code resident in the flash memory device). If the LED does not light at power-on, check that you have the mounting pillars and screws fitted properly. If it stays on, the DSP is not booting correctly, or is set to boot in a non-standard way.

Four of the remaining LEDs can be controlled with the LED register. Writing 1 will illuminate the LED; writing 0 will turn it off.

LED Register

31–4	3	2	1	0
	LED D5	LED D4	LED D3	LED D2
	RW,0	RW,0	RW,0	RW,0

CONFIG & NMI

See general firmware description.

Timer

See general firmware description.

IIOF interrupt

The firmware can generate pulses on the external interrupt lines of the TIM.

See general firmware description.

Code Composer

This module is fully compatible with the Code Composer Studio debug and development environment. This extends to both the software and JTAG debugging hardware.

Application Development

You can develop code for DSP376 modules in several ways. The simplest is to use the DSP Research WSW6000 Server Loader and its associated libraries (shortly to be discontinued).

The Server Loader is an application that runs on a host PC under either Windows 98, 2000 or NT and allows you to run COFF-format applications. Modified forms of the TI RTS library support standard C I/O.

The Server Loader will read an **`.out`** file and convert it into C4x-style boot code, which is then transmitted down a comm-port to the DSP376.

The boot code is in the following format:

6-word header	Word[1] 1	0 Reserved
	Words 2, 3, 4	0, 0, 0
	Word 5	Start address
	Word 6	0
Load Block	Word 1	4*N: Length of load block (in bytes)[2]
	Word 2	Destination address (external memory only)
	Next N words	N data words
0 or more Load Blocks		
Terminator	Word 1	0[3]

[1] A word is 32 bits

[2] The length of each data block will be rounded up to a multiple of 4 bytes if necessary.

[3] Effectively a zero-length Load Block

Operating Conditions

Safety

The module presents no hazard to the user.

EMC

The module is designed to operate within an enclosed host system that provides adequate EMC shielding. Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system.

The module is protected from damage by fast voltage transients introduced along output cables from outside the host system.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.

General Requirements

The module must be fixed to a TIM40-compliant carrier board.

The DSP376 TIM is in a range of modules that must be supplied with a 3.3v power source. In addition to the 5v supply specified in the TIM specification, these new generation modules require an additional 3.3v supply to be presented on the two diagonally opposite TIM mounting holes. The lack of this 3.3v power supply should not damage the module, although it will obviously be inoperable; prolonged operation under these circumstances is not recommended.

This module is not directly compatible with earlier generations of TIM motherboards, although the 3.3v supply can be provided from a separate source. It is, however, compatible with the latest generation of DSP Research TIM carrier boards such as the PCI310Q and VME328, which present the 3.3v via conductive mounting pillars.

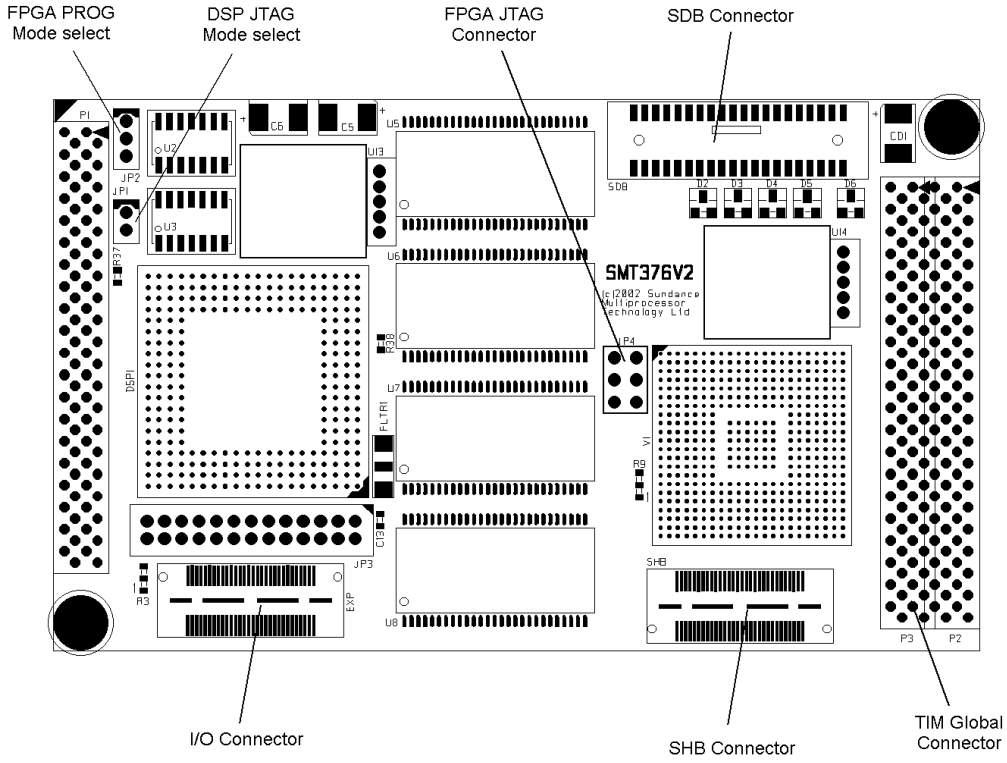
Use of the TIM on cPCI300Q motherboards may require a firmware upgrade. If LED D6 on the DSP376 remains illuminated once the TIM is plugged in and powered up, the cPCI300Q needs the upgrade. The latest firmware is supplied with all new boards shipped. Please contact DSP Research directly if you have an older board and need the upgrade.

The external ambient temperature must remain between 0˚C and 40˚C, and the relative humidity must not exceed 95% (non-condensing).

Power Consumption

The power consumption of this TIM is dependent on the operating conditions in terms of core activity and I/O activity. The maximum power consumption is 3W.

Connector Positions



Virtex Memory Map

See general firmware description with i = 14

The memory mapping is as follows:

```
#define CP0                         (volatile unsigned int *)0x80000000
#define CP1                         (volatile unsigned int *)0x80008000
#define CP3                         (volatile unsigned int *)0x80018000
#define CP4                         (volatile unsigned int *)0x80020000
#define CP0_STAT                    (volatile unsigned int *)0x80004000
#define CP1_STAT                    (volatile unsigned int *)0x8000C000
#define CP3_STAT                    (volatile unsigned int *)0x8001C000
#define CP4_STAT                    (volatile unsigned int *)0x80024000
#define GBSTAT                      (volatile unsigned int *)0x80034000
#define SDBSTAT                     (volatile unsigned int *)0x80038000
#define STAT                        (volatile unsigned int *)0x8003C000
#define SDBA                        (volatile unsigned int *)0x80040000
#define SDBB                        (volatile unsigned int *)0x80050000
#define SDBA_STAT                   (volatile unsigned int *)0x80048000
#define SDBB_STAT                   (volatile unsigned int *)0x80058000
#define SDBA_INPUTFLAG              (volatile unsigned int *)0x80044000
#define SDBB_ INPUTFLAG             (volatile unsigned int *)0x80054000
#define SDBA_OUTPUTFLAG             (volatile unsigned int *)0x8004C000
#define SDBB_OUTPUTFLAG             (volatile unsigned int *)0x8005C000
#define GLOBAL_BUS                  (volatile unsigned int *)0x800A0000
#define GLOBAL_BUS_CTRL             (volatile unsigned int *)0x80080000
#define GLOBAL_BUS_START            (volatile unsigned int *)0x80088000
#define GLOBAL_BUS_LENGTH           (volatile unsigned int *)0x80090000
#define TCLK                        (volatile unsigned int *)0x800C0000
#define TIMCONFIG                   (volatile unsigned int *)0x800C8000
#define LED                         (volatile unsigned int *)0x800D0000
#define IIOF                        (volatile unsigned int *)0x800D8000
#define INTCTRL4                    (volatile unsigned int *)0x800E0000
#define SDBINTCTRL4                 (volatile unsigned int *)0x800E4000
#define INTCTRL5                    (volatile unsigned int *)0x800E8000
#define SDBINTCTRL5                 (volatile unsigned int *)0x800EC000
#define INTCTRL6                    (volatile unsigned int *)0x800F0000
#define SDBINTCTRL6                 (volatile unsigned int *)0x800F4000
#define INTCTRL7                    (volatile unsigned int *)0x800F8000
```

```
#define SDBINTCTRL7                (volatile unsigned int *)0x800FC000
```

Connector Pin-outs

SDB0 Pin-Out

Pin	Signal	Signal	Pin
1	CLK	GND	2
3	D0	GND	4
5	D1	GND	6
7	D2	GND	8
9	D3	GND	10
11	D4	GND	12
13	D5	GND	14
15	D6	GND	16
17	D7	GND	18
19	D8	GND	20
21	D9	GND	22
23	D10	GND	24
25	D11	GND	26
27	D12	GND	28
29	D13	GND	30
31	D14	GND	32
33	D15	GND	34
35	UD0	DIR	36
37	WEN	REQ	38
39	UD1	ACK	40

FPGA JTAG

The following shows the pin-outs for JP4 (FPGA) JTAG connector:

Signal	Pin	Pin	Signal
V33	1	2	TCK
GND	3	4	TMS
TDO	5	6	TDI

400 MB/sec Digital Bus pin-out

Pin	Signal	Signal	Pin
1	SDB1_CLK	SDB1_D0	2
3	SDB1_D1	SDB1_D2	4
5	SDB1_D3	SDB1_D4	6
7	SDB1_D5	SDB1_D6	8
9	SDB1_D7	SDB1_D8	10
11	SDB1_D9	SDB1_D10	12
13	SDB1_D11	SDB1_D12	14
15	SDB1_D13	SDB1_D14	16
17	SDB1_D15	SDB1_U0	18
19	SDB1_U1	-	20
21	-	SDB1_WEN1	22
23	SDB1_REQ1	SDB1_ACK1	24
25	-	-	26
27	-	-	28
29	-	-	30
31	-	-	32
33	-	-	34
35	-	-	36
37	SDB2_CLK	SDB2_D0	38
39	SDB2_D1	SDB2_D2	40
41	SDB2_D3	SDB2_D4	42
43	SDB2_D5	SDB2_D6	44
45	SDB2_D7	SDB2_D8	46
47	SDB2_D9	SDB2_D10	48
49	SDB2_D11	SDB2_D12	50
51	SDB2_D13	SDB2_D14	52
53	SDB2_D15	SDB2_U0	54
55	SDB2_U1	-	56
57	-	SDB2_WEN	58
59	SDB2_REQ	SDB2_ACK	60

Not implemented

This standard is implemented using SAMTEC QSTRIP 0.50mm Hi-speed connectors.

To improve electrical performances, a ground plane is embedded in each QSTRIP connector.

For long distances micro-coax ribbon cable is used to connect 2 QSTRIP connectors.

Serial Ports & Other C60 I/O (EXP connector)

The C60 contains various I/O ports. These signals are connected to a QSH type connector. The pin-out of this connector is shown here:

Pin number	Signal	Signal	Pin number
1	HPI CS	HPI HDS1	2
3	HPI RDY	HPI HDS2	4
5	HPI CNTRL0	HPI CNTRL1	6
7	HPI HWIL	HPI RW	8
9	HPI AS	GND	10
11	3.3V	GND	12
13	HPI D0	HPI D8	14
15	HPI D1	HPI D9	16
17	HPI D2	HPI D10	18
19	HPI D3	HPI D11	20
21	HPI D4	HPI D12	22
23	HPI D5	HPI D13	24
25	HPI D6	HPI D14	26
27	HPI D7	HPI D15	28
29	HPI INT	GND	30
31	3.3V	DSP GPIO2	32
33	3.3V	GND	34
35	FPGA TTL0	FPGA TTL2	36
37	FPGA TTL1	FPGA TTL3	38
39	N/C	N/C	40
41	N/C	N/C	42
43	N/C	N/C	44
45	N/C	N/C	46
47	MCBSP CLKS1	MCBSP CLKS0	48
49	MCBSP CLKR1	MCBSP CLKR0	50
51	MCBSP CLKX1	MCBSP CLKX0	52
53	MCBSP DR1	MCBSP DR0	54
55	MCBSP DX1	MCBSP DX0	56
57	MCBSP FSR1	MCBSP FSR0	58
59	MCBSP FSX1	MCBSP FSX0	60

Serial Ports & Other C60 I/O (JP3 connector)

Pin number	Signal	Signal	Pin number
1	MCBSP CLKS1	MCBSP CLKR1	2
3	MCBSP CLKX1	MCBSP DR1	4
5	MCBSP DX1	MCBSP FSR1	6
7	MCBSP FSX1	GND	8
9	MCBSP CLKS0	MCBSP CLKR0	10
11	MCBSP CLKX0	MCBSP DR0	12
13	MCBSP DX0	MCBSP FSR0	14
15	MCBSP CLKS0	3.3V	16
17	FPGA TTL0	FPGA TTL1	18
19	FPGA TTL2	FPGA TTL3	20
21	DSP GPIO0	DSP GPIO1	22
23	DSP GPIO2	DSP GPIO3	24
25	GND	GND	26

FPGA PROG Pin Control (JP2 connector)

Jumper Position		
1-2	2-3	Out
PROG asserted continuously	PROG asserted for the duration of RESET. Can also be controlled by the DSP.	PROG under control of DSP

DSP JTAG Control (JP1 connector)

In	JTAG enabled to DSP
Out	JTAG enabled to DSP only after the DSP reads the flash

Data Sheets (Hyperlinks)

1. TMS320C6201/C6701 Peripherals Reference Guide (literature number SPRU190)
   http://www-s.ti.com/sc/psheets/spru190d/spru190d.pdf
   Describes common peripherals available on the TMS320C6201/C6701 digital signal processors. This book includes information on the internal data and program memories, the external memory interface (EMIF), the host port, multichannel-buffered serial ports, direct memory access (DMA), clocking and phase-locked loop (PLL), and the power-down modes.

2. Application Note: Flash Programming

3. TIM-40 MODULE SPECIFICATION Including TMS320C44 Addendum
   tim_spec_v1.01.pdf

4. 200 MB/sec Digital Bus Technical Specification
   Digital_Bus_Technical_Specification.pdf

5. 400 MB/sec Digital Bus Technical Specification
   High_Speed_Bus_Technical_Specification_v1_0.pdf

6. TMS320C4x User's Guide (literature number SPRU063)
   http://www-s.ti.com/sc/psheets/spru063c/spru063c.pdf
   Describes the C4x 32-bit floating-point processor, developed for digital signal processing as well as parallel processing applications. Covered are its architecture, internal register structure, instruction set, pipeline, specifications, and operation of its six DMA channels and six communication ports. Software and hardware applications are included.

7. Application Note: Creating New Firmware

8. Xilinx Spartan-IIE data sheet:
   http://www.xilinx.com/partinfo/ds077.htm

9. Texas Instruments TMS320C6211B data sheet:
   http://www-s.ti.com/sc/ds/tms320c6211b.pdf

10. Texas Instruments TMS320C6711 data sheet:
    http://www-s.ti.com/sc/ds/tms320c6711b.pdf

11. Texas Instruments TMS320C6713 data sheet:
    http://www-s.ti.com/sc/ds/tms320c6713.pdf

Index