

3.2. A/D Conversion

3.2.1. A/D Data Registers

The PCL-711B uses the data registers located at I/O ports BASE+4 and BASE+5 to store the converted A/D data. The low byte data is stored at BASE+4, and the high byte data is stored at BASE+5.

BASE+4 A/D Low Byte Data (Read)

D7	D6	D5	D4	D3	D2	D1	D0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

BASE+5 A/D High Byte Data (Read)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DRDY	AD11	AD10	AD9	AD8

Where:

AD0 through AD11: Represent the PCL-711B's A/D data bits. AD0 is the Least Significant Bit (LSB), and AD11 is the Most Significant Bit (MSB).

DRDY: Data ready bit. When A/D conversion is in progress, this bit remains as 1. It becomes 0 when the A/D conversion is completed. It will become to 1 after reading the low byte A/D data from BASE+4.

3.2.2. Gain Control Register

BASE+9 is used to set the PCL-711B's amplification gain for A/D conversion. The PCL-711B provides five different gains: x1, x2, x4, x8, and x16.

The following tables outline BASE+9's register format and corresponding gain settings:

BASE+9 Gain Control Register (Write)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	G2	G1	G0

G2	G1	G0	GAIN
0	0	0	x1
0	0	1	x2
0	1	0	x4
0	1	1	x8
1	0	0	x16

3.2.3. Multiplexer Scan Register

The PCL-711B can multiplex up to 8 channels of analog input. Users have to set this register, located at BASE+10, to select to the desired channel , which is going to be measured, before performing any A/D conversion. The register format is as below:

BASE+10 Multiplexer Scan Control (Write)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	C2	C1	C0

C2	C1	C0	CH.
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

3.2.4. Mode and Interrupt Control Register

The PCL-711B's A/D conversion can be triggered in one of the following three ways:

- **By software**

Writing any data to BASE+12 will generate a trigger pulse to the PCL-711B's on-board A/D converter.

- **By the on-board clock (pacer)**

The PCL-711B is equipped with a Intel 8253, a programmable interval timer/ counter, to generate precise clock output (pacer). The pacer clock rate of the PCL-711B is between 0.5MHz and 35 minutes per pulse. (See section 3.7 for details on programming the Intel 8253 timer/counter.)

- **By external pulse**

The PCL-711B allows users to use external signal, from D/I 0 (Pin 1 of the connector CN4), as the A/D trigger pulse. The A/D conversion will be triggered at the rising edge of the external signal.

Also, the PCL-711B provides two ways to transfer the converted A/D data to certain variables:

- **By software control (foreground)**

The software control data transfer utilizes advantage of the foreground polling concept. After the A/D converter has been triggered, the application program should keep checking the DRDY bit of I/O port BASE+5 until the DRDY bit is detected as 0. Then the program should read data from BASE+4 and BASE+5 to get the whole converted data.

- **By interrupt (background)**

The PCL-711B also provides background data transfer support, if it is programmed to be in the interrupt data transfer mode. If the PCL-711B is in interrupt data transfer mode, it will generate an interrupt to your PC after each A/D conversion is completed. The corresponding ISR (interrupt service routine) should handle everything to transfer the converted data to memory variables in your program.

I/O port BASE+11 is used to set the PCL-711B's operation mode and the IRQ level. The register format is as following:

BASE+11 Mode and Interrupt Control Register (Write)

D7	D6	D5	D4	D3	D2	D1	D0
-	I3	I1	I0	-	S2	S1	S0

Where:

S0 to S2: mode selection

S2	S1	S0	Operation Mode
0	0	0	S/W trigger with S/W data transfer
0	0	1	
0	1	0	External trigger * with S/W data transfer
0	1	1	External trigger * with INT data transfer
1	0	0	Pacer trigger with S/W data transfer
1	0	1	Reserved
1	1	0	Pacer trigger with INT data transfer
1	1	1	Reserved

Note: External trigger signal go through DI0 of CN4

I0 to I2: IRQ level selection

I2	I1	I0	Interrupt Level
0	0	0	IRQ2
0	0	1	N/A
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

3.2.5. Interrupt Status Register

If the PCL-711B is in interrupt data transfer mode, a hardware status flag will be set after each A/D conversion. Users have to clear the status flag, by writing any data to BASE+8, to let the PCL-711B accept next interrupt.

BASE+8 Clear Interrupt Status (Write)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	-

3.2.6. Software Trigger Register

Writing any data to BASE+12 will generate a trigger pulse to the PCL-711B's A/D converter.

BASE+12 Software A/D Trigger (Write)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	-

3.3. D/A Conversion

The PCL-711B provides one D/A output channel. The low byte and the high byte D/A data are set via BASE+4 and BASE+5 respectively.

Since the PCL-711B uses so-called double-buffer D/A output technology to avoid output glitch, the low byte data should be written first and the high byte data second, that is write BASE+4 first and BASE+5 second. The D/A output will not change until BASE+5 is updated.

BASE+4 D/A Low Byte Data (Write)

D7	D6	D5	D4	D3	D2	D1	D0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

BASE+5 D/A High Byte Data (Write)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	DA11	DA10	DA9	DA8

where:

DA0 through DA11: the D/A output data. DA0 represents the D/A' LSB data, while DA11 represents the D/A' MSB data.

3.4. Digital Input and Output

3.4.1. Digital Input Registers

The PCL-711B provides 16 bits of digital input. The registers are located at BASE+6 and BASE+7.

BASE+6 D/I Low Byte Data (Read)

D7	D6	D5	D4	D3	D2	D1	D0
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

BASE+7 D/I High Byte Data (Read)

D7	D6	D5	D4	D3	D2	D1	D0
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

3.4.2. Digital Output Registers

The PCL-711B provides 16 bits of digital output. The registers are located at BASE+13 and BASE+14.

BASE+13 D/O Low Byte Data (Write)

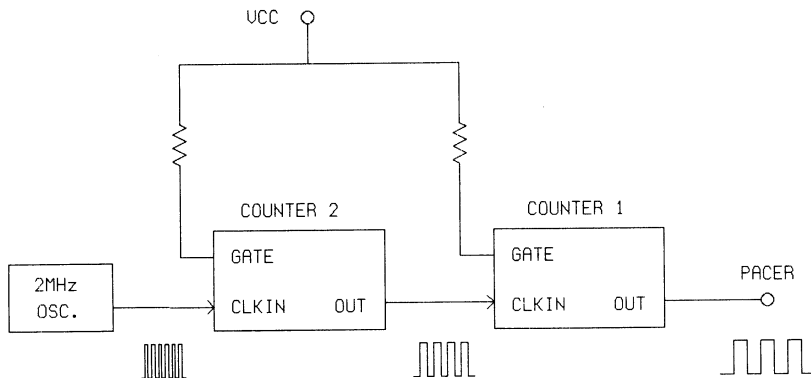
D7	D6	D5	D4	D3	D2	D1	D0
DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

BASE+14 D/O High Byte Data (Write)

D7	D6	D5	D4	D3	D2	D1	D0
DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8

3.5. Pacer Programming

The PCL-711B uses an Intel 8253, a 16-bit programmable counter/timer, to generate pacer clock. Each Intel 8253 provides three independent counter/timer channels, Counter 0, Counter 1 and Counter 2. The PCL-711B cascades Counter 1 and Counter 2 as a 32-bit frequency divider to support wide range of pacer clock rate, as shown below:



Intel 8253 has six operation modes, from Mode 0 through Mode 5. To generate pacer clock, both Counter 1 and Counter 2 should be programmed as Mode 2 (rate generator mode).

Four I/O ports, from BASE+0 through BASE+3, are used to program the on-board Intel 8253:

BASE+0:	Counter 0	(Read/Write)
BASE+1:	Counter 1	(Read/Write)
BASE+2:	Counter 2	(Read/Write)
BASE+3:	Counter Control	(Write only)

Please refer to the following steps to set desired pacer clock rate:

- Step 1: Write '74H' to BASE+3 to make Counter 1 work at Mode 2.
- Step 2: Write an appropriate data (16-bit data, ranging from 2 to 65535) to BASE+1 to set Counter 1's divisor constant C1. Since C1 is a 16-bit data, you have to first write the low byte of C1 to BASE+1, then write the high byte of C1 to BASE+1.
- Step 3: Write 'B4H' to BASE+3 to make Counter 2 work at Mode 2.
- Step 4: Write an appropriate data (16-bit data, ranging from 2 to 65535) to BASE+1 to set Counter 1's divisor constant C2. Since C2 is a 16-bit data, you have to first write the low byte of C2 to BASE+2, then write the high byte of C2 to BASE+2.

The pacer rate is determined by the following formula:

$$\text{Pacer rate} = (2 \text{ MHz}) / (C1 * C2)$$

In the following example (written in BASIC), C1 is set as 40 and C2 is set as 10, thus the pacer rate will be 5 KHz ($5\text{KHz} = 2\text{MHz} / (40 * 10)$).

```

.
.
.
500 OUT (BASE+3,&H74)      ' Set Counter 1 as Mode 2
510 OUT (BASE+1,40)        ' write low byte of C1
520 OUT (BASE+1,0)         ' write high byte of C1
530 OUT (BASE+3,&HB4)      ' Set Counter 2 as Mode 2
540 OUT (BASE+2,10)        ' write low byte of C2
550 OUT (BASE+2,0)         ' write high byte of C2
.
.
.

```

NOTE 1: Counter 0 is reserved to future developement.

NOTE 2: For more detailed information about Intel 8253's register formats, please refer to Appendix B.

APPENDIX A. CALIBRATION

In data acquisition and control application, it is important to constantly calibrate your measurement device to maintain its accuracy. A calibration program, CAL711B.EXE is provided in the PCL-711B software disk to assist your calibration work.

Minimum equipment required to perform a satisfactory calibration is a 4 1/2 digit digital multimeter. In addition, a voltage calibrator or a stable noise free d.c. voltage source that can be used in conjunction with the digital multimeter is required. A card extender, such as the PC-LabCard model PCL-757 is an inexpensive device that you will find greatly improves access to the board during calibration and will probably be useful with other boards.

Calibration is easily performed using the CAL711B.EXE program. This program will lead you through the calibration and set up procedure with variety of prompts and graphic displays directing you to correct settings and adjustment the variable resistors. The explanatory material in this section is brief and is intended for use in conjunction with the calibration program.

A.1. VR Assignments

The PCL-711B has five on-board VRs, which allow you to make accurate calibration adjustments for the card's A/D and D/A functions. Each VR's location is indicated in Figure A-1. The function of each VR is listed below:

VR1	D/A full scale adjustment
VR2	D/A offset adjustment
VR3	A/D offset adjustment
VR4	A/D full scale adjustment
VR5	Programmable amplifier offset adjustment

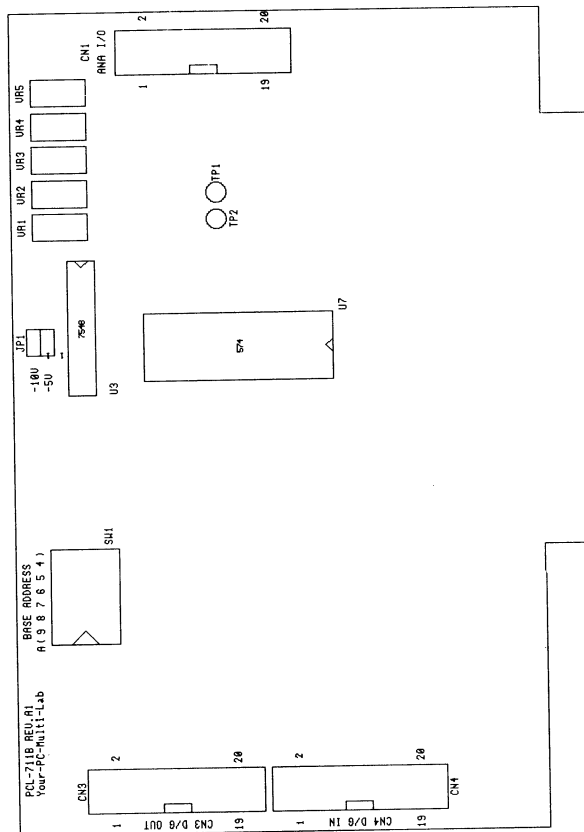


Figure A-1 VR location

A.2. D/A Calibration

The user should first choose the D/A output range to be calibrated by setting the J1 (5V or 10V). The zero offset and full scale of D/A channel can be tuned through two VRs: VR1 is for the full scale adjustment of D/A and VR2 is for the zero offset adjustment of D/A. The user should use a precision voltmeter to measure the D/A output.

Calibration steps:

1. Full scale adjustment. The D/A digital data is sent to 4095. Adjust VR1 until the reading of your voltmeter equals to VREF(reference voltage of D/A output) with opposite sign.
2. Offset adjustment. The D/A digital data is sent to 0. Adjust VR2 until the reading of your voltmeter is 0 volts.

A.3. A/D Calibration

Because the PCL-711B supports versatile A/D input ranges, accurately calibrated result for certain A/D range may still cause a small offset for the other ranges. It is suggested that you make a calibration again when you are going to use different A/D input range.

Calibration steps:

1. Short the A/D input of Channel 0 to AGND. Then, adjust the VR3 until the reading of the A/D conversion flickers between 2047 and 2048.
2. Apply a voltage with the full scale value corresponding to the specific A/D input range to A/D Channel 0. Then, adjust the VR4 until the reading of A/D conversion flickers between 4094 and 4095.

APPENDIX B. INTEL 8253 REFERENCE

B.1. Operation Modes

B.1.1. Mode 0 Stop on Terminal Count

In Mode 0, the counter/timer's output will initially be set low. The output will remain low, and the counter will start to count after the count has been loaded into the selected count register. When the terminal count has been reached, the output will be set high, and remain high until the selected counter is reloaded with this mode or a new count has been loaded. The counter will continue to decrement after the terminal count has been reached. Rewriting data to a counter register during counting generates the following results:

1. Writing to the first byte stops the current count.
2. Writing to the second byte starts a new count.

B.1.2. Mode 1 Programmable One-Shot

When in this mode, the output will be set low on the count that follows the gate input's rising edge. The output goes high on the terminal count. If a new count value is loaded while the output is set low, then it will not affect the duration of the one-shot pulse until after the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse. The one-shot is retriggerable. This allows the output to remain low for the full count after any rising edge from the gate input.

B.1.3. Mode 2 Rate Generator

When in Mode 2, the counter/timer's output will be set at low for one period of the input clock. The period from one output pulse to the next is equal to the number of input counts in the counter register. If the counter register is reloaded between output pulses, the present period will not be affected.

B.1.4. Mode 3 Square Wave Generator

This mode is similar to Mode 2, with the exception that the output remains high until one half of the count value has been completed (for even values), and then low for the other half of the count. This is accomplished by decreasing the counter by two on the falling edge of each clock pulse. When the counter reaches the terminal count, the output's state will be changed. The counter will be reloaded with the full count, repeating the entire process.

If the count value is odd, and the output high, then the first clock pulse (after the count is loaded) decrements the count by one. Subsequent clock pulses will decrement the count by two. After a timeout period, the output is set low, and the full count value is then reloaded. The clock pulse (following the reload) decrements the counter by three. Subsequent clock pulses decrement the count by two until a timeout occurs, then the whole process is repeated. In this way, if the count value is odd, the output will be set high for $(N + 1)/2$ counts, and low for $(N - 1)/2$ counts.

B.1.5. Mode 4 Software Triggered Strobe

Mode 4 sets the counter/timer's output high. When the count value is loaded, the counter begins counting. The output will be set low for one input clock period when the terminal count is reached, after which it will be set high again.

If the count register is reloaded during counting, the new count will be loaded on the next clock pulse. Also, the count will be inhibited while the gate input is low.

B.1.6. Mode 5 Hardware Triggered Strobe

When in Mode 5, the counter will start counting after the trigger input's rising edge, and will then be set low for one clock period when the terminal count is reached. The counter is retriggerable in this mode.

B.2. Counter Control Register Format**BASE+3 Counter Control Register (Write)**

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

Key:**SC1 & SC0 Select Counter**

SC1	SC0	COUNTER
0	0	0
0	1	1
0	0	2
1	1	illegal

RW1 & RW0 Select Read/Write Operation

RW1	RW0	OPERATION
0	0	Counter latch
0	0	Read/Write LSB
0	1	Read/Write MSB
1	1	Read/Write LSB first, then MSB

M2, M1, & M0 Select Operation Mode

M2	M1	M0	MODE
0	0	0	0 = Interrupt on terminal count
0	0	1	1 = Programmable one shot
X	1	0	2 = Rate generator
X	1	1	3 = Square wave rate generator
1	0	0	4 = Software triggered strobe
1	0	1	5 = Hardware triggered strobe

BCD Select Binary or BCD Counting

BCD	PURPOSE
0	16-bit binary counter
1	Binary coded decimal (BCD) counter with four decades

The BCD is defaulted to count in binary mode. The count can be set to any value from 0 up to 65535. If you set this bit to BCD (logic 1), then the count may be set to any value from 0 up to 9999.