Service Manual

ESS 66x8 SOLUTION

CONTENTS :

1. INFORMATIONS
Vibratto-II DVD Processor (ESS 66x8)

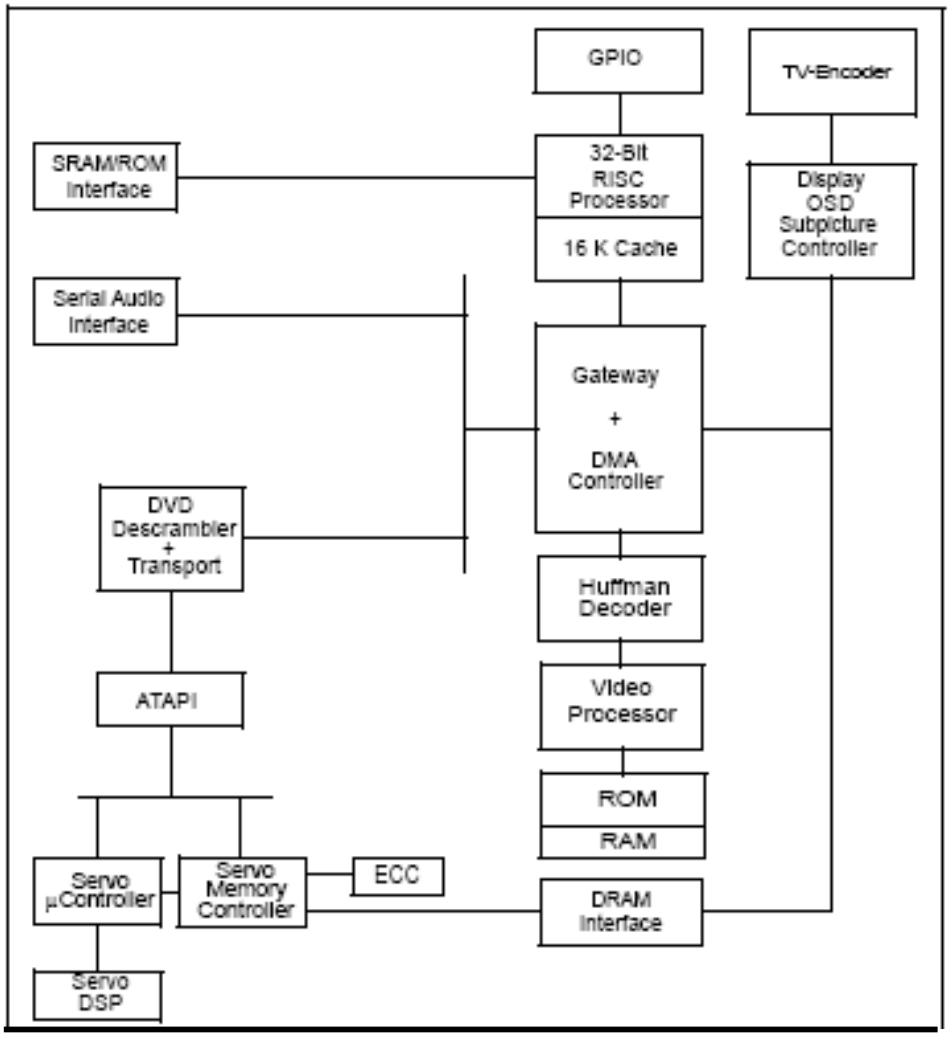
Vibratto-II DVD Processor

FEATURES:

- Single-chip DVD processoe incorporating all front-end and back-end functions
- Unified memory architecture
- Proven focusing, sledding, tracking, and CLV/CAV spindke servo control
- Proven ESS, EFM,?EFM+ demodulation, and EDC circuit
- Built-in ADCs and DACs for servo control signals
- Direct interface to ES6603 servo AFE chip
- Integrated NTSC/PAL encode with pixel-adaptive de-interlacer and five 10-bit 54MHz video DACs
- DVD-video, DVD-VR, VCD1.1 and 2.0, and SVCD
- DivX and MPEG-4 Advanced Simple profile at full screen(D1)
- Full DVD-audio support including MLP and LPCM decode, CPPM decryption, and watermark detection
- Media playback with CD-ROM, CD-R/RW, DVD-R/RW, and DVD+R/RW
- Up to 7.1 channel audio outputs
- Direct interface of 16 bit DRAM up to 128Mb capacity
- Direct interface for up to 4 banks of 8-bit EPROM or FLASH EPROM for up to 4MB per bank
- Macrovision 7.1 for NTSC/PAL (480p/576p) progressie scan video
- Simultaneous composite,S-video and YUV output
- CCIR656/601 yuv 4:2:2 output
- OSD controller supports 256 colors in 8 degrees of transparency
- Subpicture Unit(SPU) decoder supports karaoke iyric,subtitles,and EIA-608 compliant Line 21 Captioning.
- SmartBrght™ for clear and bright movie presentation.
- SmartColor™ for vivid flesh-tone image display.
- SmartLogo™ for custom JPEG wallpaper.
- JPEG digital photo CD support (Kodak Picture CD™ and Fujifilm FujiColor CD™.
- ESS Music Slideshor™.
- Bass management.
- Dolby Digital(AC-3),Dolby ProLogic™,and ProLogicll.
- DTS™surround(ES6698D only).
- S/PDIF digital audio input and output.
- MPEG AAC and Multichannel.
- SRS TruSurround
- Professional karaoke with full scoring scheme.

Functional Description:

The internal block digram for ESS 6698



Pinout Diagram

ES6698 PIN DEXCRIPTION

Names	Pin Numbers	I/P	Definitions
VD33	1.10.19.35.44.53.62.79.96.126.185.	P	I/O power supply.
VID_XI	2	I	Crystal input.
VID_XO	3	O	Crystal output.
VID_XO	3	O	Crystal output.
CLK	4	I	System clock.
DMA[11:0]	5:8 11:17 20	O	DRAM address bus.
VX33	9.18.34.43.52.61.78.95.119.127.186.208	G	Ground for I/O power supply.
DCAS#	21	O	DRAM column address strobe (active-low).
DCS[1:0]#	22.23	O	DRAM chip select (active-low).
DRAS[2:0]#	24.25.28	O	DRAM row address strobe (active-low).
VSS	26.70.86.137.197	G	Ground for core power supply.
VDD	27.71.87.138.198	P	Core power supply.
DSCK_EN	29	O	DRAM clock enable output .
DOE#		O	DRAM output enable(active-low).
DWE#	30	O	DRAM write enable(active-low).
DB[15:0]	31:33,36:42,45:50	I/O	DRAM data bus.
DSCK	51	O	Output clock to DRAM.
DQM	54	O	Data input/output mask.
LA[21:0]	55:60,63:69,72:77 80:82	O	RISC port address bus .
LCS[3:0]#	83:85 88	O	RISC port chip select (active-low).
LWRLL#	89	O	RISC port low-byte write enable(active-low).
LOE#	90	O	RISC port output enable (active-low).
LD[7:0]	91:94,97:100	I/O	RISC port data bus; (5V tolerant input).
RSD	101	I	Audio receive serial data; (5V tolerant input).
RBCK	102	I	Audio receive bit clock; (5V tolerant input).
RWS	103	I	Audio receive frame sync; (5V tolerant input).
VD33_PL	104	P	Power for PLL blocks.
VS33_PL	105	G	Ground for PLL blocks.
VREF	106	I	Internal voltage reference to video DAC.
YUV1		O	YUV pixel 1 output data .
COMP	107	I	Compensation input .
YUV3		O	YUV pixel 3 output data .
RSET	108	I	DAC current adjustment resistor input .
YUV4		O	YUV pixel 4 output data.
FDAC	109	O	Video DAC output. Refer to description and matrix for UDAC pin 115.

<table>
<tr><td>YUV7</td><td></td><td>O</td><td>YUV pixel 7 output data .</td></tr>
<tr><td>VDAC</td><td rowspan="2">110</td><td>O</td><td>Video DAC output . Refer to description and matrix for UDAC pin 115.</td></tr>
<tr><td>YUV6</td><td>O</td><td>YUV pixel 6 output data.</td></tr>
<tr><td>Names</td><td>Pin Numbers</td><td>I/P</td><td>Definitions</td></tr>
<tr><td>VD33_DA</td><td>111</td><td>P</td><td>Power for I/O power supply for VDAC.</td></tr>
<tr><td>VS33-DA</td><td>112</td><td>G</td><td>Ground for I/O power supply for VDAC.</td></tr>
<tr><td>YDAC</td><td rowspan="2">113</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 115.</td></tr>
<tr><td>YUV5</td><td>O</td><td>YUV pixel 5 output data.</td></tr>
<tr><td>CDAC</td><td rowspan="2">114</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 115.</td></tr>
<tr><td>YUV2</td><td>O</td><td>YUV pixel 2 output data .</td></tr>
<tr><td>UDAC</td><td></td><td>O</td><td>Video DAC output.
<table>
<tr><th>Pin</th><th>109</th><th>110</th><th>113</th><th>114</th><th>115</th></tr>
<tr><th>Value</th><th>FDAC</th><th>VDAC</th><th>YDAC</th><th>CDAC</th><th>UDAC</th></tr>
<tr><td>0</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>N/A</td></tr>
<tr><td>1</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>CVBS2</td></tr>
<tr><td>2</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>C</td><td>N/A</td></tr>
<tr><td>3</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>CVBS2</td></tr>
<tr><td>4</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>5</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>6</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>7</td><td>N/A</td><td>SYNC</td><td>G</td><td>B</td><td>R</td></tr>
<tr><td>8</td><td>CVBS/Chroma</td><td>Chroma</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>9</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>B</td><td>R</td></tr>
<tr><td>10</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>R</td><td>B</td></tr>
<tr><td>11</td><td>N/A</td><td>SYNC</td><td>G</td><td>R</td><td>B</td></tr>
<tr><td>12</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pr</td><td>Pb</td></tr>
<tr><td>13</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pr</td><td>Pb</td></tr>
<tr><td>14</td><td>Chroma</td><td>Y</td><td>G</td><td>R</td><td>B</td></tr>
</table>
F: VCBS/chroma signal for simultaneous mode.
Y: Luma component for YUV and Y/C processing.</td></tr>
</table>

			C: Chrominance signal for Y/C processing. U: Chrominance component signal for YUV mode. V: Chrominance component signal for YUV mode.
TWS	116	O	Audio transmit frame sync output.

<table>
<tr><th>Names</th><th>Pin Numbers</th><th>I/P</th><th>Definitions</th></tr>
<tr><td>SEL_PLL2</td><td></td><td>I</td><td>System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings. Strapped to VCC or ground via 4.7-KΩ resistor; read only during reset.
<table>
<tr><th>SEL_PLL 2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type(MHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>CLK*4.5</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>CLK*5.0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>CLK*4.0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>CLK*4.25</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>CLK*4.75</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>CLK*5.5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>CLK*6.0</td></tr>
</table></td></tr>
<tr><td>TSD0</td><td rowspan="2">117</td><td>O</td><td>Audio transmit serial data port 0.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Refer to the description and matrix for SEL_Pll2 pin 116.</td></tr>
<tr><td>TSD1</td><td rowspan="2">118</td><td>O</td><td>Audio transmit serial data port 1.</td></tr>
<tr><td>SEL_PLL1</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 116.</td></tr>
<tr><td>TSD[2:3]</td><td>120.121</td><td>O</td><td>Audio transmit serial data ports 2 and 3.</td></tr>
<tr><td>MCLK</td><td>122</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>123</td><td>O</td><td>Audio transmit bit clock.</td></tr>
<tr><td>SPD_DOBM</td><td rowspan="2">124</td><td>O</td><td>S/PDIF output .</td></tr>
<tr><td>SEL_PLL3</td><td>I</td><td>Clock source select. Strapped to VCC or ground via 4.7K Ω read only during reset .
<table>
<tr><th>SEL_PLL3</th><th>Clock Source</th></tr>
<tr><td>0</td><td>Crystal oscillator</td></tr>
<tr><td>1</td><td>CLK input</td></tr>
</table></td></tr>
<tr><td>SPDIF_IN</td><td>125</td><td>I</td><td>S/PDIF input; (5V tolerant input).</td></tr>
<tr><td>WBLCLK</td><td>128</td><td>O</td><td>DVD-RAM wobble detector circuit clock source to preamp.</td></tr>
<tr><td>WBL</td><td>129</td><td>O</td><td>DVD-RAM wobble output.</td></tr>
<tr><td>LG</td><td>130</td><td>O</td><td>DVD-RAM land/groove flag.</td></tr>
<tr><td>IP2</td><td>131</td><td>I</td><td>DVD-RAM header position index 2.</td></tr>
<tr><td>IP1</td><td>132</td><td>I</td><td>DVD-RAM header position index 1.</td></tr>
<tr><td>FLAG[3:0]</td><td>133:136</td><td>O</td><td>To monitor servo status .</td></tr>
<tr><td>TEXI</td><td>139</td><td>I</td><td>High-speed tracking error input .</td></tr>
<tr><td>TESTAD</td><td>140</td><td>I</td><td>Test AD input .</td></tr>
<tr><td>SBAD</td><td>141</td><td>I</td><td>Sub-beam addition input signal .</td></tr>
<tr><td>FEI</td><td>142</td><td>I</td><td>Focus input error signal.</td></tr>
<tr><td>AVSS_AD</td><td>143</td><td>G</td><td>Analog ground for ADC block .</td></tr>
</table>

CEI	144	I	Center error input signal .
TEI	145	I	Tracking error input signal .
RFRP	146	I	RF ripple/envelope input signal.
AVDD3_AD	147	P	Analog power supply for ADC block.
VREF21	148	O	2.1V reference voltage.
VREF09	149	O	0.9Vreference voltage.
VREF15	150	O	1.5V reference voltage.
Names	Pin Numbers	I/P	Definitions
IREF	151	I	Servo data PLL interface reference current generator connect a resistor between this pin and ground to set reference current .
AVDD3_DS	152	P	Analog power supply for data slicer .block.
IPIN	153	I	Inverting input of data slicer .
RFIN	154	I	Analog RF signal input after passing through equalizer(minus)
RFIP	155	I	Analog RF signal input after passing through equalizer(plus).
DSSLV	156	O	Data slicer level output.
AVSS_DS	157	G	Analog ground for data slicer block.
AVSS_PL	158	G	Analog ground for data PLL block.
PDOFTR1	159	O	Servo data PLL phase detector filter pin number 1.
FDO	160	O	Servo data PLL output node of frequency detector charge pump.
FTROPI	161	I	Servo data PLL input node of loop filter OP circuit .
AVDD3_OL	162	P	Analog power supply for data PLL block .
PLLFTR1	163	I	Servo data PLL loop filter pin number1.
PLLFTR2	164	I	Servo data PLL loop filter pin number2.
VREF0	165	O	Servo data PLL reference voltage output.
AWRC	166	I/O	Auto wide range control VCO signal from/to AWRC DAC.
AVSS_DA	167	G	Analog ground for DAC part.
RFRPCTR	168	I/O	Central level of RFRP.
TRAY	169	O	Output voltage level for tray buffer IC.
AVDD3_DA	170	P	Analog power supply for DAC part .
SPINDLE	171	O	Output voltage level for spindle buffer IC.
FOCUS	172	O	Output voltage level for focus buffer IC.
SLEGP	173	O	Output voltage level for Sledge buffer IC(plus).
SLEGN	174	O	Output voltage level for Sledge buffer IC(minus).
TRACK	175	O	Output voltage level for tracking buffer IC.
TESTDA	176	O	Test DA output .
FGIN	177	I	Spindle hall sensor input .
PHOI	178	I	Sledge photo interrupt signal input.
SCSJ	179	O	Chip selection signal to RF chip (serial data enable).
SDATA	180	I/O	Data signal from/to RF chip.
SCLK	181	O	Serial clock source to RF chip.
DFCT	182	I	Defect flag input signal.

LDC	183	O	Laser diode on/off control output.
SPDON	184	O	Spindle power driver on/off control output.
GPIO[9:4]	187:192	I/O	General-purpose input/output used for servo control; (5V tolerant input.)
EAUX[3:0]	193:196	I/O	Extended auxiliary ports;(5V tolerant input).
I^2CDATA	199	I/O	I^2C data I/O;(5V tolerant input).
AUX0		I/O	Auxiliary port (open collector);(5V tolerant input).
I^2C_CLK	200	I/O	I^2C clock I/O;(5V tolerant input).
AUX1		I/O	Auxiliary port (open collector);(5V tolerant input).
IOW#	201	O	I/O Write strobe(LCS1)(active-low).
HSYNC#		I/O	Horizontal sync (active low);(5V tolerant input).
AUX2		I/O	Auxiliary port ;(5V tolerant input).
Names	Pin Numbers	I/P	Definitions
IOR#	202	O	I/O Read strobe (LCS1)(active –low).
VSYNC#		I/O	Vertical sync (active-low);(5V tolerant input).
AUX3		I/O	Auxiliary port;(5V tolerant input).
C2PO	203	I	Error correction flag from CD;(5V tolerant input).
AUX4		I/O	Auxiliary port;(5V tolerant input).
AUX[5:6]	204:205	I/O	Auxiliary ports ;(5V tolerant input).
IR	206	I	Infrared remote control input;(5V tolerant input).
AUX7		I/O	Auxiliary port;(5V tolerant input).
RESET#	207	I	Reset input (active –low);(5V tolerant input).
Audio Port Interface	101	I	Audio receive serial data input[RSD];(5V tolerant input).
	102	I	Audio receive bit clock input [RBCK]:(5V tolerant input).
	103	I	Audio receive frame sync input[RWS];(5V tolerant input).
	116	O	Audio transmit frame sync output[TWS].
	117.118.120.121	O	Audio transmit serial data outputs [TSD[3:0]].
	122	I/O	Audio DAC master clock[MCLK].
	123	O	Audio transmit bit clock output[TBCK].
	124	O	Sony/Philips Digital Interface audio output [SPD_DOBM].
	125	I	Sony/Philips Digital Interface audio Input [SPDIF_IN];(5V tolerant input).
Auxiliary Port Interface	193:196	I/O	Extended auxiliary ports [EAUX[3:0]];(5V tolerant input).
	199.200	I/O	Open collectors [AUX[1:0]],(5V tolerant input).
	201:206	I/O	Primary auxiliary port I/Os [AUX[7:2]];(5V tolerant input).
Clock Inetface and Reset	2	I	27-MHz crystal clock input [VID_XI].
	3	O	27-MHz crystal clock output[VID_XO].
	4	I	System clock [CLK].
	29	O	DRAM clock enable output [DSCK_EN].
	51	O	Output clock [DSCK] to video memory (DRAM).
	116:118	I	Clock frequency select PLL outputs [SEL_PLL[2:0]].
	207	I	Reset input (active-low)[RESET#];(5V tolerant input).
Display Interface	106:110.113:115	O	Pixel data outputs [YUV[7:0]].
	201	I/O	Horizontal sync[HSYNC#];(%V tolerant input).

	202	I/O	Vertical sync [VSYNC#];(5V tolerant input).
EPROM/Flash ROM and RISC Port Intetface	55:60.63:69.72:77.80:82	O	RISC port address bus [LA[21:0]]to EPROM or Flash memory.
	83:85	O	RISC port chip select outputs [LCS[2:0]#]to EPROM or Flash memory.
	89	O	RISC port low-byte write enable output[LWRLL#]to EPROM or Flash memory.
	90	O	RISC port output enable[LOE#]to EPROM and Flash memory.
	91:94.97:100	I/O	RISC port data bus [LD[7:0]]to EPROM or Flash memory (5V tolerant input).
Filter and Reference voltang Interface	106	I	Video DAC reference voltage input[VREF].
	107	I	Compensation input[COMP].
Front Panel Display Interface	206	I	Infrared remote control input [IR];(5V tolerant input).
Names	Pin Numbers	I/P	Definitions
General-Purpose	187:192	I/O	General –purpose I/O[GPIO[9:4]];(5V tolerant input).
I^2C Bus Interface	199	I/O	I^2C data I/O[12C_DATA];(5V tolerant input).
	200	I/O	I^2C clock I/O[12C_CLK];(5V tolerant input).
Power and Ground	1.10.19.35.44.53.62.79.96.126.185	P	I/O power supply [VD33].
	9.18.34.43.52.61.78.95.119.127.186.208	G	I/O ground [VS33].
	26.70.86.137.197	G	Ground for core power [VSS].
	27.71.87.138.198	P	Core power supply [VDD].
	104	P	Power supply for PLL block .[VD33_PL].
	105	G	Ground for PLL block [VS33_PL].
	111	P	Power supply for video DAC[VD33_DA].
	112	G	Ground for video DAC[VS33_DA].
	143	G	Analog ground for ADC[AVSS_AD].
	147	P	Analog power supply for ADC[AVDD3_AD].
	152	P	Analog power supply for data slicer [AVDD3_DS].
	157	G	Analog ground for data slicer[AVSS_DS].
	158	G	Analog ground for data PLL [AVSS_PL].
	162	P	Analog power supply for data PLL[AVDD3_PL].
	167	G	Analog ground for DAC[AVSS_DA].
	170	P	Analog power supply for DAC[AVDD3_DA].
Serial Port Interface	203	I	C2PO error correction flag from CD[C2PO];(5V tolerant input).

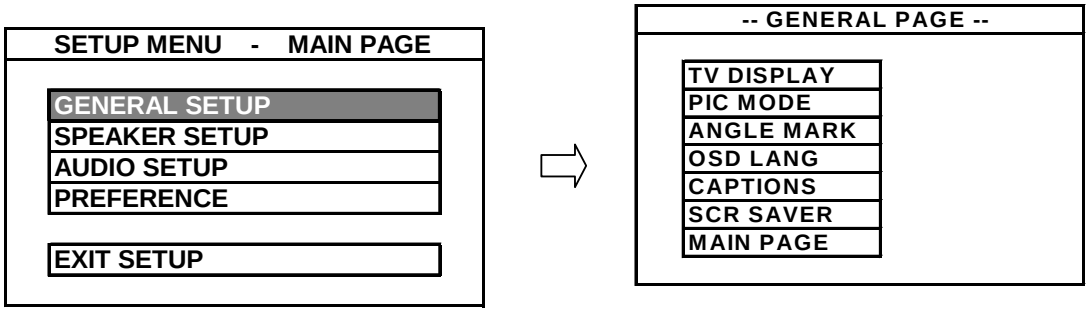
Servo Data Slicer Interface	153	I	Inverting input of data slicer [IPIN].
	154	I	Analog RF signal input after passing through equalizer(minus) [RFIN].
	155	I	Analog RF signal input after passing through equalizer(plus) [RFIP].
	156	O	Data slicer level output[DSSLV].

2.OPERATING INSTRUCTIONS

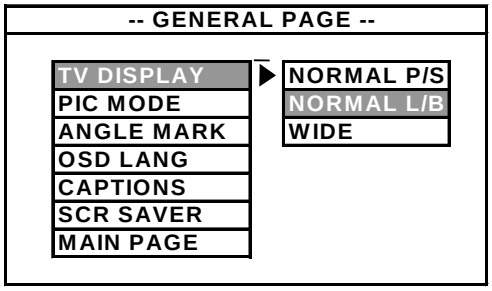
1. GENERAL SETUP

Pressing the SETUP button on remote control during STOP or PLAY mode to SETUP MENU.

sing  Cursor to select GENERAL SETUP. Press ENTER to enter GENERAL SETUP page.



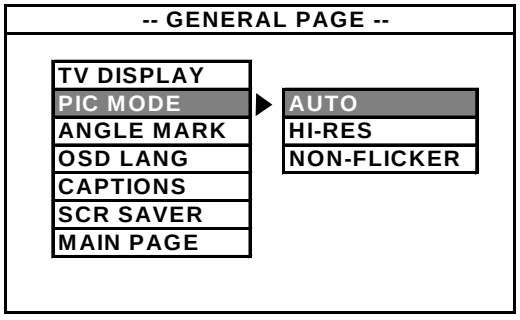
a.TV DISPLAY

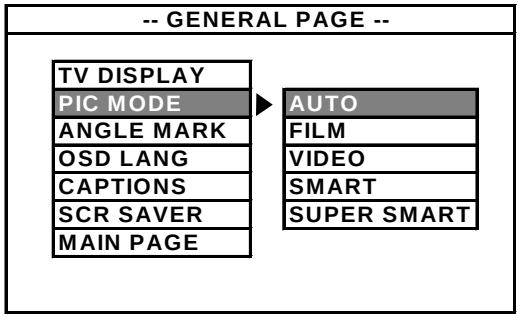


Using cursor to move to desired setting and press ENTER to confirm.
NORMAL/PS – 4 x 3 Pan Scan
Full screen of picture on TV. Normally, left and right edges cannot be shown.
NORMAL/LB – 4 x 3 Letter Box
Orginal ratio of aspect.
WIDE – 16 : 9 Widescreen

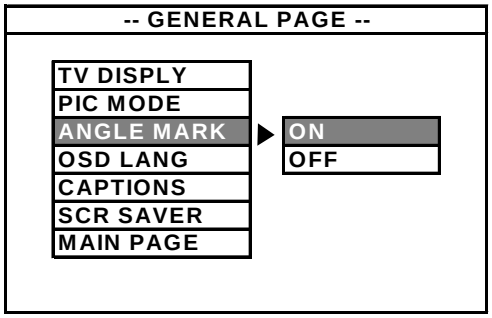
b. PIC MODE (PICTURE MODE)

(FOR PROGRESSIVE-SCAN MODEL)





c.ANGLE MARK

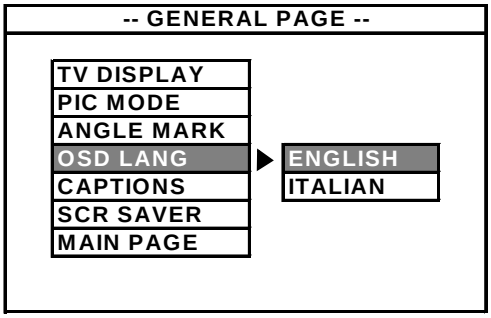


This feature is functioned only for the disc, which has ANGLE function:

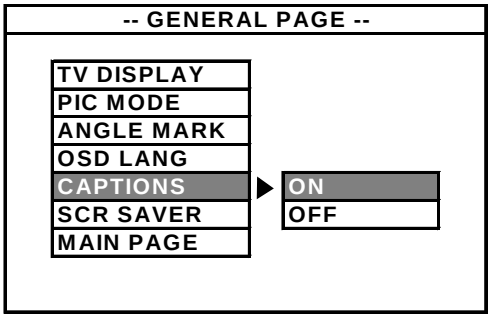
When the ANGLE MARK is set ON, the screen displays the mark.

When the ANGLE MARK is set OFF, the mark is not displayed.

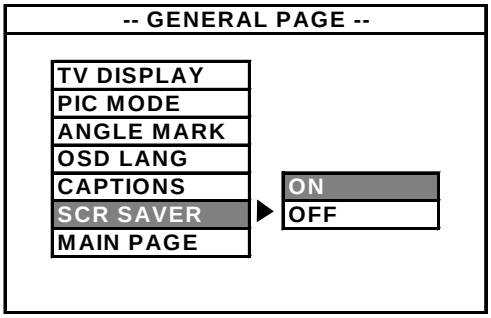
d. OSD LANG (ON SCREEN DISPLAY LANGUAGE)



e. CAPTIONS

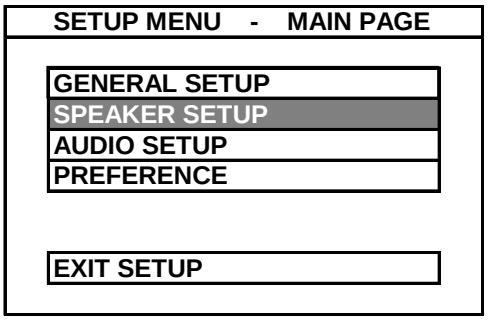


f. SCR SAVER

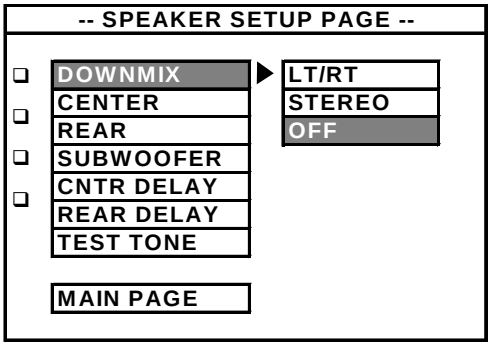


When the unit is stopped, no operation, no function button is pressed in 1 minute,screen saver appears for the purpose to protect the TV screen if SCR SAVER is set ON.

2.SPEAKER SETUP



a. DOWNMIX

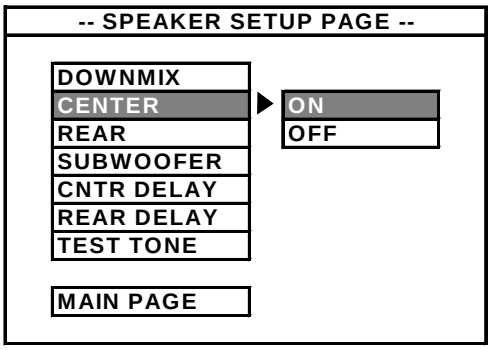


LT/RT : Left and Right output mode

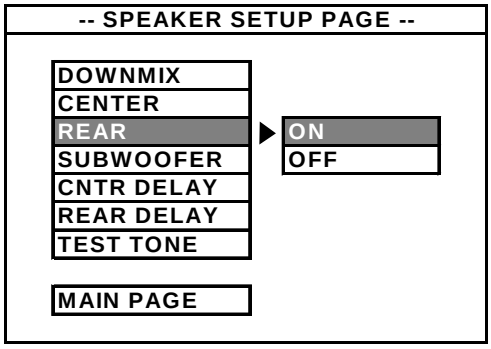
STEREO : Stereo output mode

OFF : Turn off the Downmix mode. **5.1 channels can be preformed only if Downmix is set OFF** and the rest of other setup can be activated.

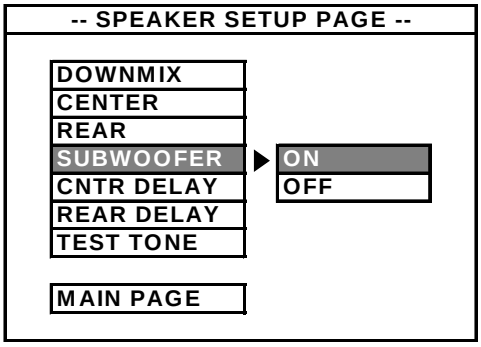
b. CENTER



c. REAR

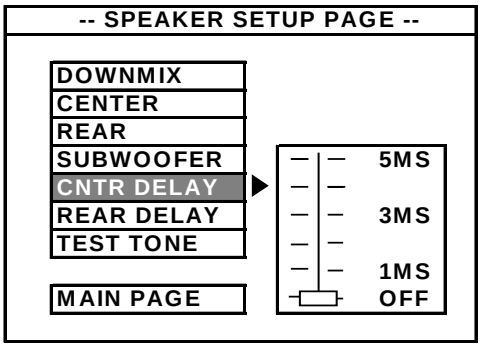


d. SUBWOOFER



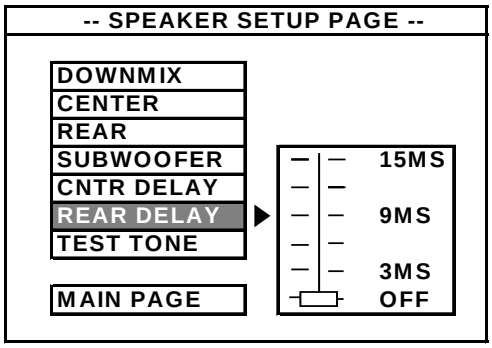
e. CNTR DELAY

Adjust the audio delay from center channel from 0 to 5MS.

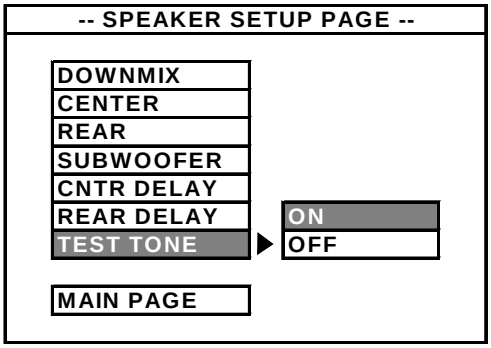


f. REAR DELAY

Adjust the audio delay from center channel rom 0 to 15MS.

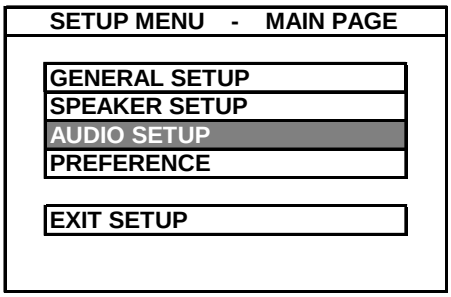


g. TEST TONE

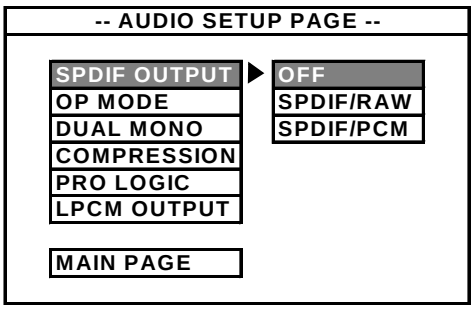


ON : open the 5.1 channel test function.
OFF : turn off the 5.1 channel test function.

3.AUDIO SETUP



a. SPDIF OUTPUT

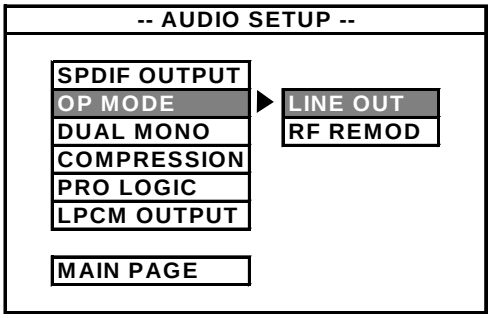


OFF: Audio signal is out from AUDIO OUT (RCA) jacks.

SPDIF/RAW: The player is connected to a Dolby Digital amplifier through DIGITAL OUT Coaxial or Optical jack.

SPDIF/PCM: The player is connected to a 2-channel digital mode or stereo amplifier through Coaxial or Optical jack.

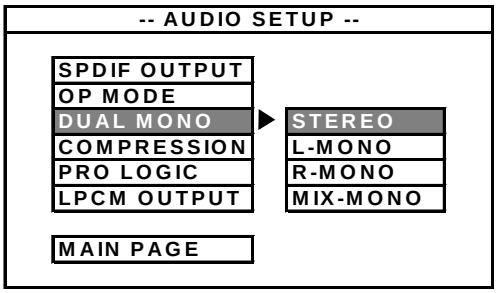
b. OP MODE



LINE OUT : Line out mode with digital dialog normalization, compress input linear signal.

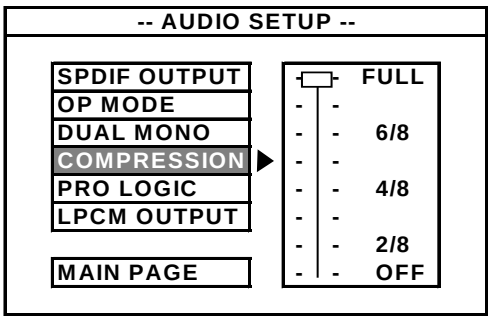
RF REMOD : RF remodulation mode with heavy compression and digital dialog normalization.

c. DUAL MONO



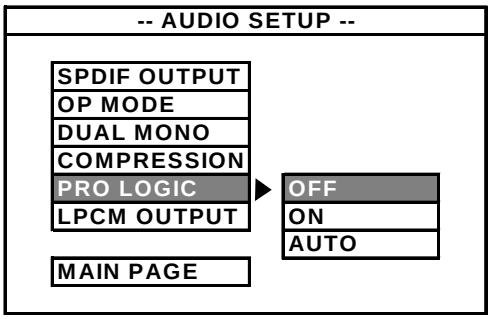
Output mode of the L/R signals. Mix-mono can be functioned only if the DVD is playing in 5.1 channel.

d. COMPRESSION



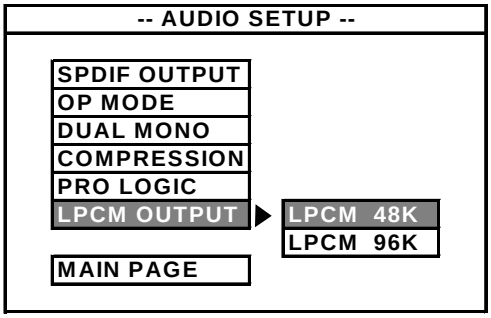
To adjust linear compression rate to obtain the different compression results of the signals only if the OP MODE is set to LINE OUT.

e. PRO LOGIC(optional)



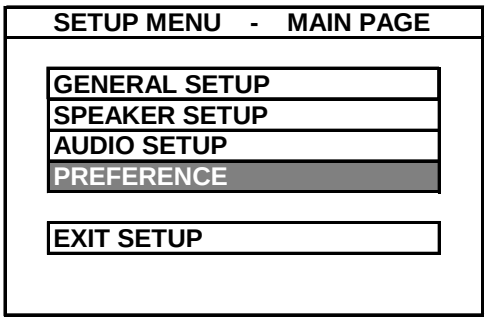
To select Dolby Prologic Surround mode.

f. LPCM OUTPUT

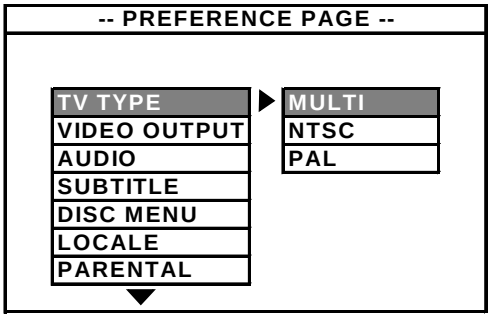


To select LPCM output at 48K or 96K.

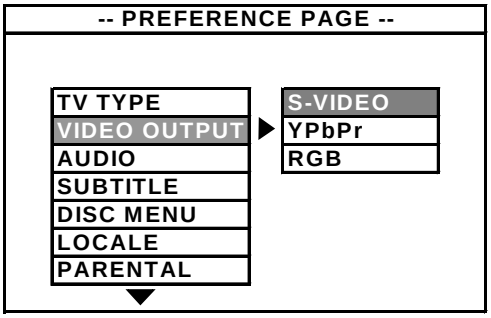
4. PREFERENCE



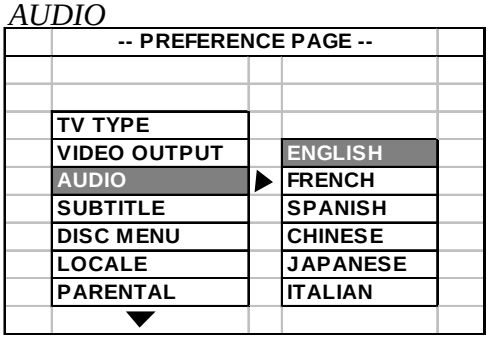
a. TV TYPE



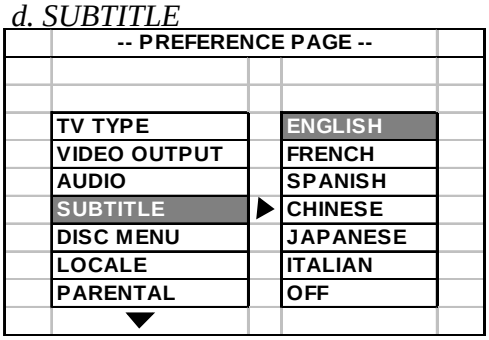
b. VIDEO OUTPUT



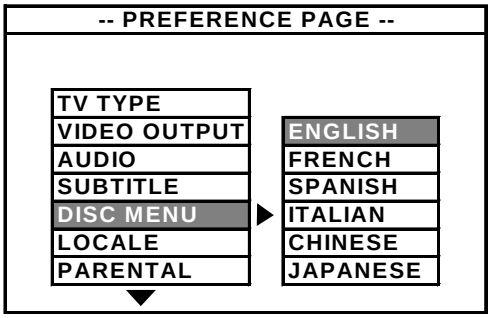
c. AUDIO



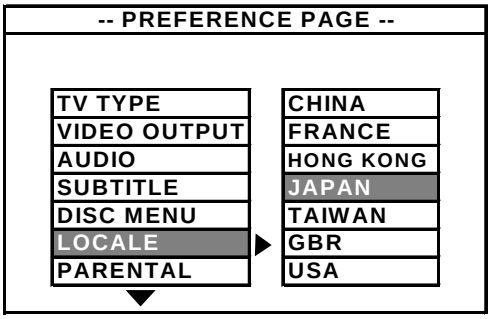
d. SUBTITLE



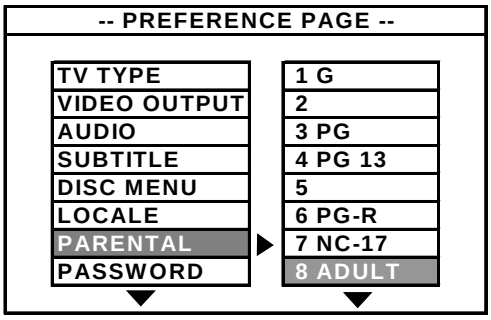
e. DISC MEUN



f. LOCALE

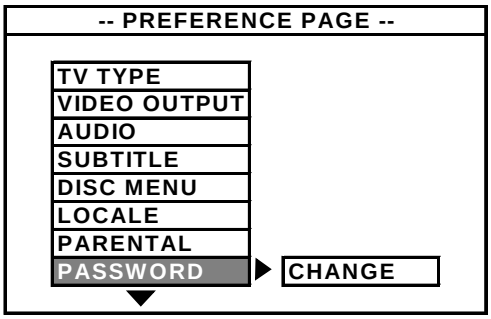


g. PARENTAL



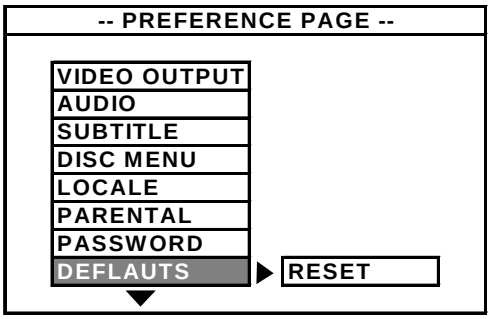
To select an age control grade according to the grade of the disc and your desired. The disc cannot be played for the rate higher than the grade set.
Go to the PASSWORD VERIFY PAGE to input password after selection of Parental grade.

h. PASSWORD



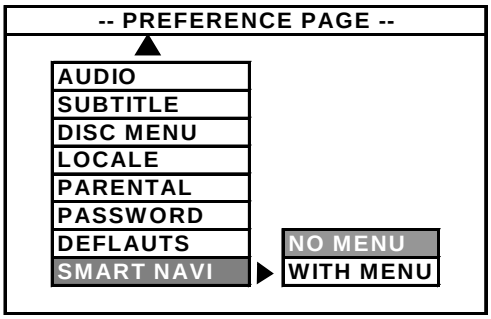
The default setting of password is 3308

i. DEFLAUTS



To reset the settings to factory setting

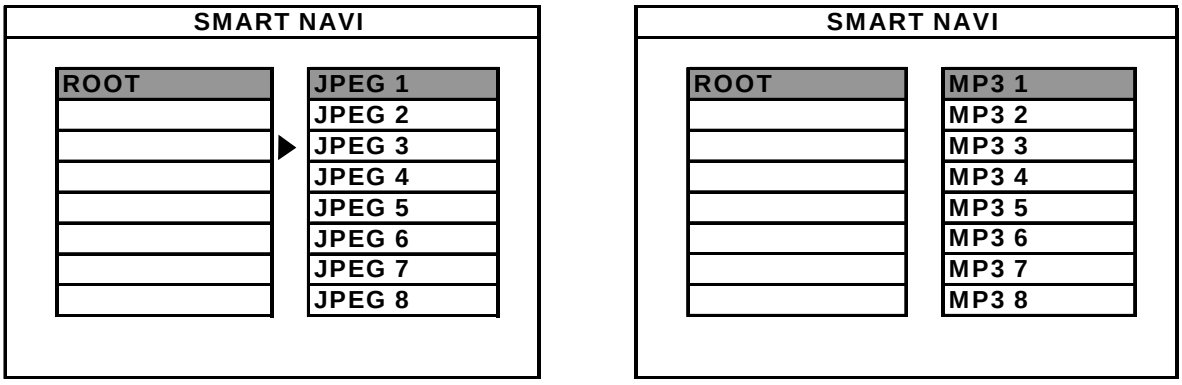
j. SMART NAVI



To select the display with MENU for playing MP3 and PHOTO CD (JPEG).

5. JPEG, MP3 & MPEG4 Format

(Playback of MP3, WMA, CD-R and CD-RW may depend on recording condition)



Press ⇦⇧⇨⇩ to select the „ROOT“ on the left columns & the „FILE“ on the right side, press ENTER“/“PLAY“ to view the JPEG PHOTOS or to play MP3 files. Then press “STOP” to go back to the menu of SMART NAVI”.

FUNCTION KEYS

Zoom Press the “ZOOM” Button, then the screen will show “ZOOM ON”, and press ▶▶ ◀◀ Icons to “zoom in” or “zoom out”.

Rotate Press ⇦⇧⇨⇩ to rotate the picture

Next/ Previous Press ▶▶| |◀◀ to the next or previous pictures/songs.

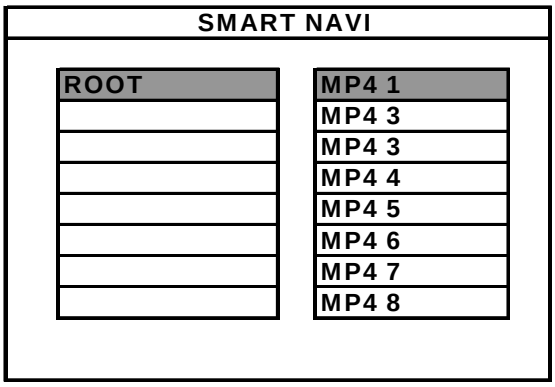
Forward/ Backward Press the ▶▶ ◀◀ icons to playing fast forward ans fast backward.

Menu Press “Menu” to preview the photos.

Mute Press “MUTE” button to turn the audio off. Press it again to resume.

Pause Press ▶II to pause playin & press again to resume.

MPEG4 FORMAT



FUNCTION KEYS

Forward/ Backward Press the ▶▶ ◀◀ icons to playing fast forward and fast backward. Continuously pressing and back to normal.

Next/ Previous Press ▶▶| |◀◀ to the next or previous chapter or files.

Mute Press “MUTE” button to turn the audio off. Press it again to resume.

Pause Press ▶II to pause playing & press again to resume.

Slow Press “SLOW” and playback of slow motion. Please “Play” to resume it.

Step Keeping press “STEP” repeatedly button to playing frames by frames.

GoTo Search the chapter and time you want. Functions please refer to “Function Buttons” on instruction book.

Subtitle In order to use the function of Subtitle (For the MPEG4 file with subtitle function):
Insert disc and choose the file in “?” icon, then press ‘ANGLE’ button in remote control, the screen will shown subtitle is being selected. Then get back to the appropriate .avi file and press ‘ENTER’ to playback, then the subtitle function is activate.

3.PRODUCT SPECIFICATIONS

A. Playback System

DVD Video
Video CD (1.1, 2.0, 3.0)
SVCD
CD and CDDA
CD-R/RW
PICTURE CD

B. Television Signal System

NTSC/PAL

C. Video Performance

Video Out	$1V_{PP}$ into 75ohm
S-Video Out	Y: $1V_{PP}$ into 75ohm C: $0.286V_{PP}$ into 75ohm
D/A Converter	27MHz/10 bit

D. Audio Performance

Frequency Response	DVD: fs48//96KHz, 4Hz-22/44KHz Video CD: fs 44.1KHz, 4Hz-20KHz Audio CD: fs44.1KHZ, 4Hz-20KHz
Output Level	Analog: $2V_{RMS}$(1KHZ) Digital: $1.15V_{PP}$
D/A Converter	96KHz/24bit
S/N Ratio	With LPF 95dB Without LPF 90dB

E. Connections

Coxial digital out	X1
Digital out	X1
Audio Analog out (5.1ch)	X1
S-Video out	X1

F. Power Supply

Power Source	AC 90-250V 50/60Hz
Power Consumption	<25 Watt

4.TROUBLESHOOTING

Symptom	Check and Action
No Power	1.Check the power cord has been properly connected to the wall outlet 2.Check the main power has been switched on
Do not play	1. No disc, load a disc 2. Disc has been loaded upside down. Place the disc with the label side up 3. Disc's region code is not matching to the unit 4. Disc is not correct type to be played 5. Disc is damaged or dirty, clean the disc or try another disc 6. Moisture may be condensed inside the unit. Remove the disc and leave the unit power on for one or two hours
No Picture	1. Check the TV set has been power on, and setting at the correct AV mode 2. Check the system connection is secure 3. Check if the connection cables are damaged 4. Clean the disc
Picture noise / distorted	1. Disc is dirty or damaged. Clean the disc or try another disc 2. Reset the color system of the DVD unit or the TV set 3. Try to direct the DVD unit to the TV set instead of via the components like VCR.
Picture not full screen	1. Select the screen format. Enter SETUP MENU → (TV DISPLAY) 2. Select the screen format from DVD disc menu
Cannot SKIP or SEARCH	1. Some disc are programmed that do not allow users to SKIP or SEARCH forward at some sections, especially at the beginning WARNING section 2. Single Chapter disc cannot apply SKIP function
No sound or Sound output not complete	1. Check the TV and amplifier has been power on and correctly setting 2. Check the TV and amplifier system connections are secure 3. Press AUDIO button select other audio tracks output of disc 4. Check if the MUTE function of the DVD, TV or amplifier has be activated 5. There will be no sound output during REVERSE PLAY / PAUSE / STEP / SLOW / SEARCH

5.MAINTENANCE INSTRUCTIONS

INDEX:

a. No power
   Please see Fiugure 1

b. No VFD display
   Please see Fiugure 2

c. No Video output
   Please see Fiugure 3

d. Cannot read disc
   Please see Fiugure 4

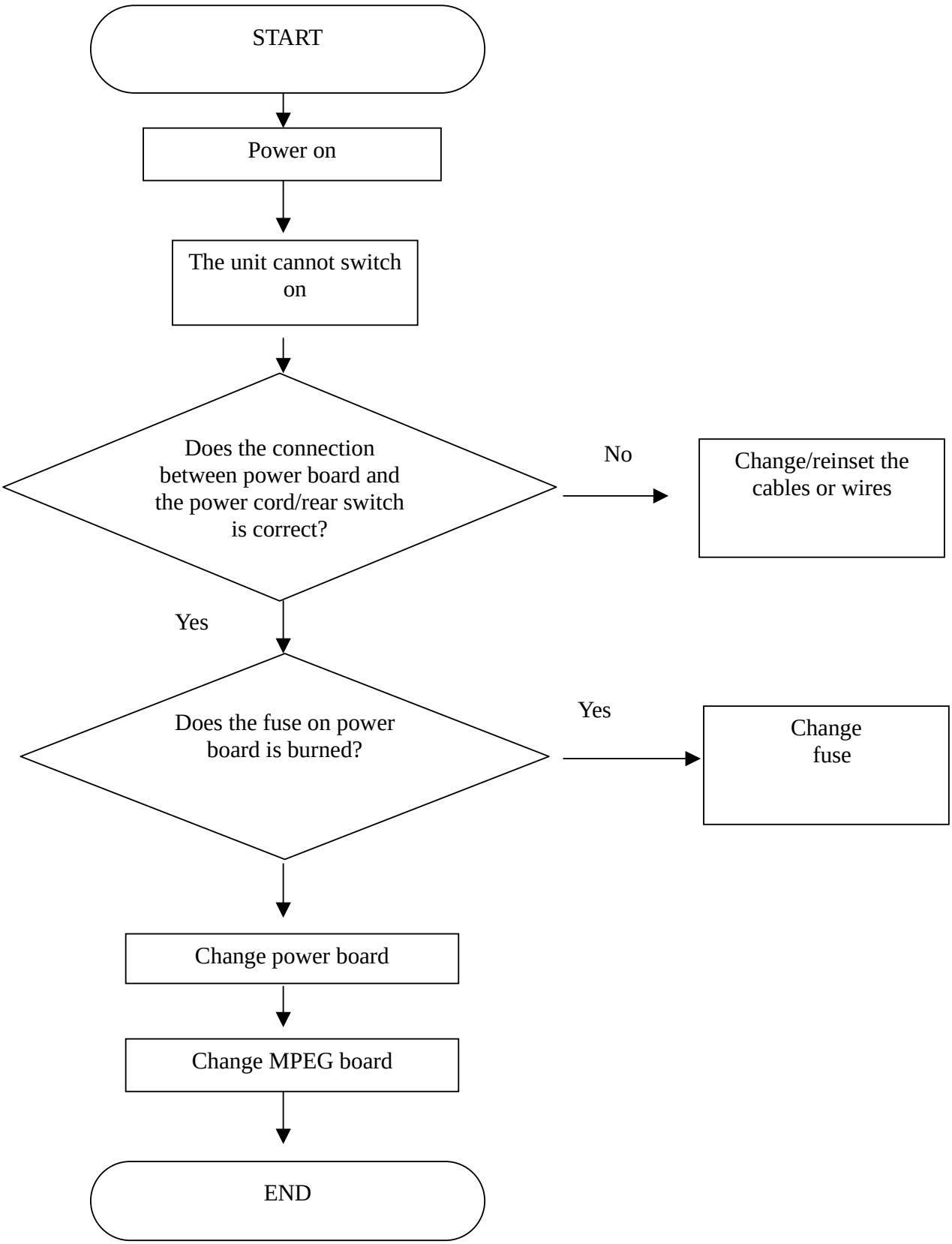
e. No ear phone output
   Please see Fiugure 5

f. Remote control no function
   Please see Fiugure 6

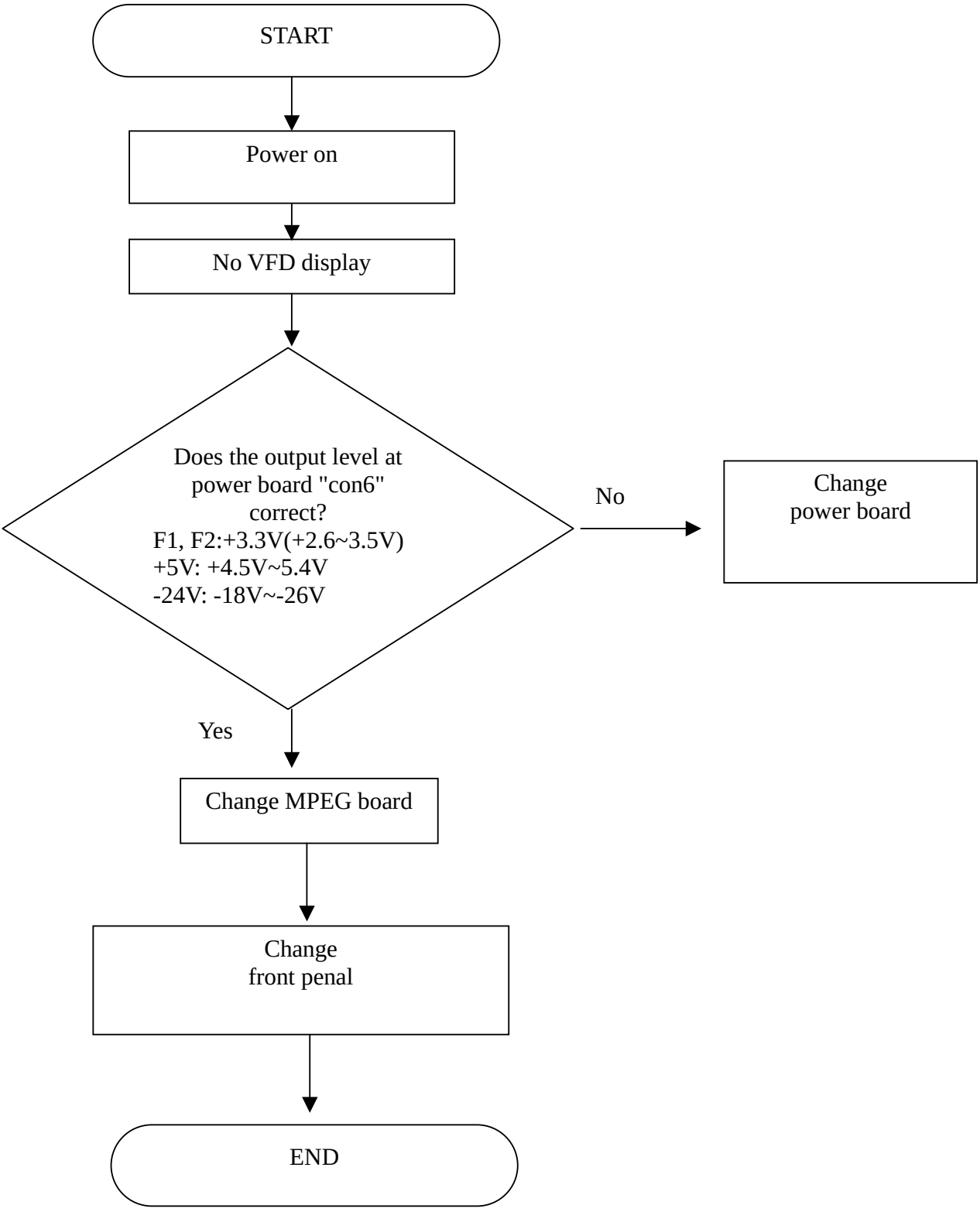
g. No 5.1ch output
   Please see Fiugure 7

h. Disc door cannot open
   Please see Fiugure 8

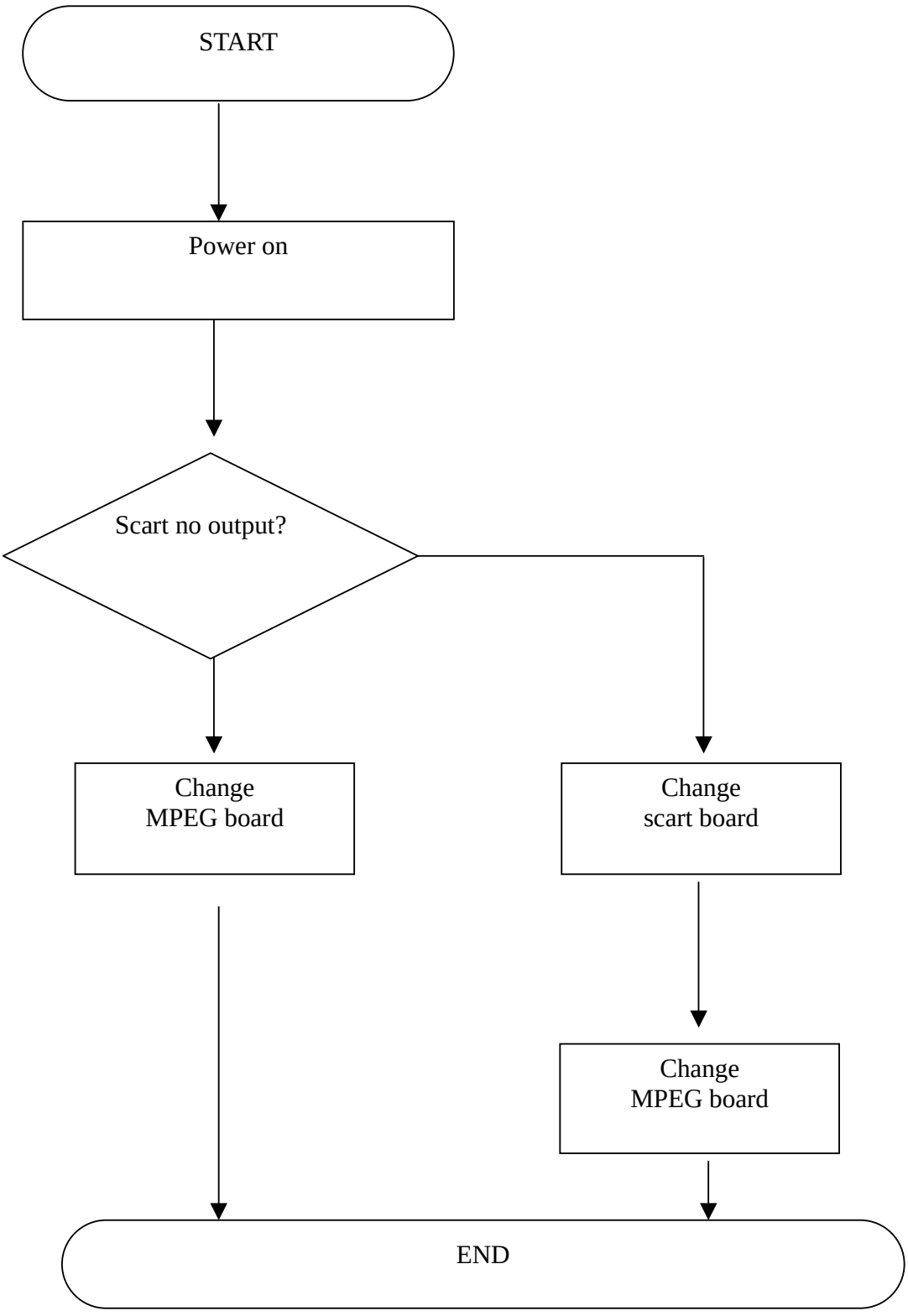
(i) Figure 1


START
Power on
The unit cannot switch on
Does the connection between power board and the power cord/rear switch is correct?
No
Change/reinset the cables or wires
Yes
Does the fuse on power board is burned?
Yes
Change fuse
Change power board
Change MPEG board
END

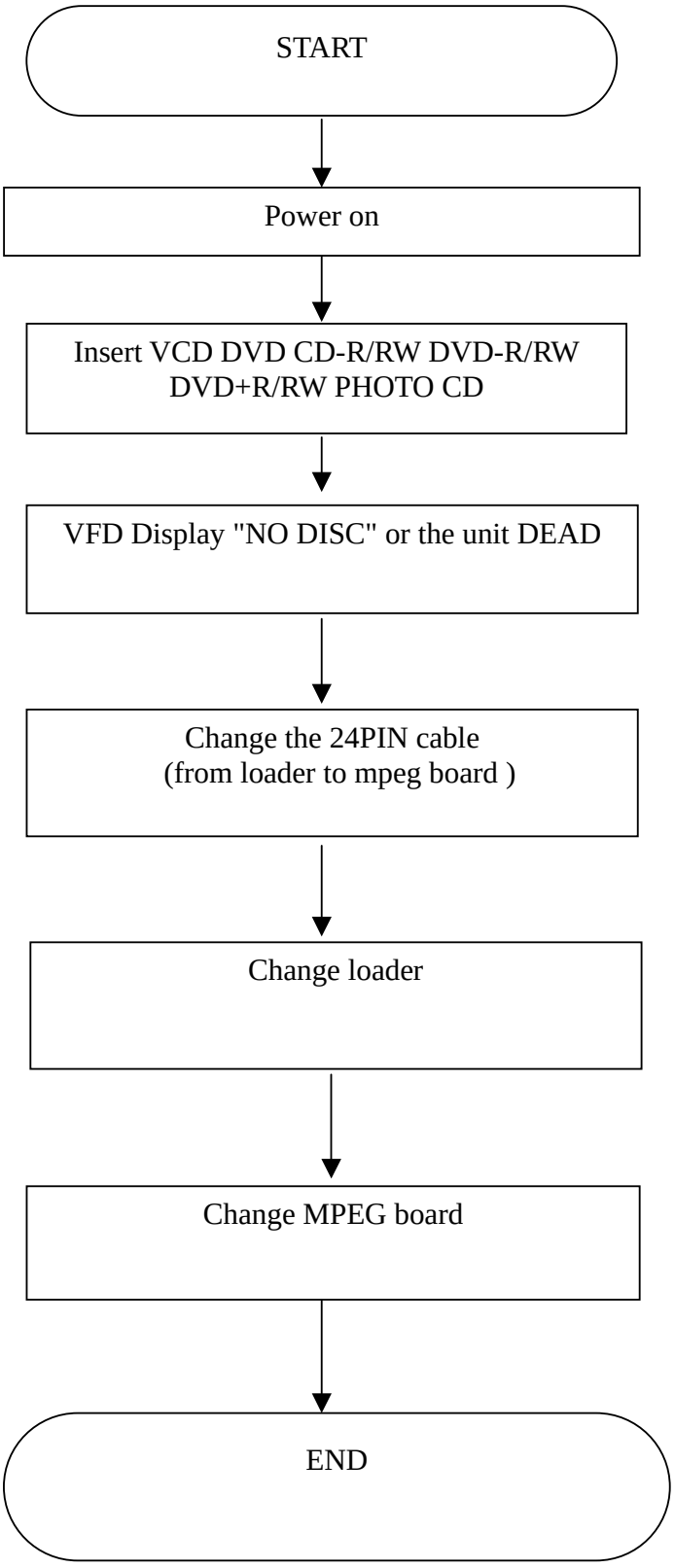
(ii) Figure 2


START
Power on
No VFD display
Does the output level at power board "con6" correct?
F1, F2:+3.3V(+2.6~3.5V)
+5V: +4.5V~5.4V
-24V: -18V~-26V
No
Change power board
Yes
Change MPEG board
Change front penal
END

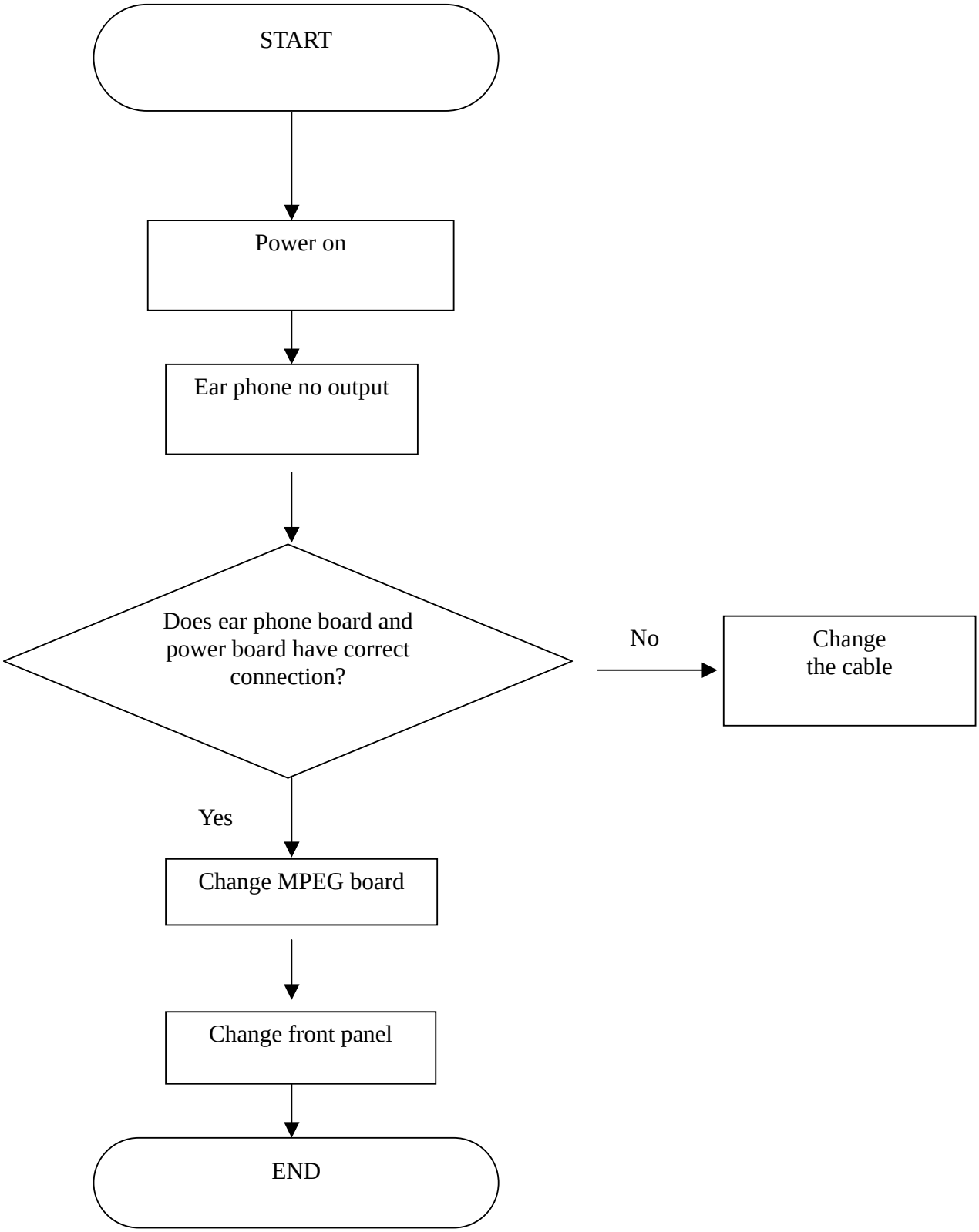
(iii)Figure 3


START
Power on
Scart no output?
Change
MPEG board
Change
scart board
Change
MPEG board
END

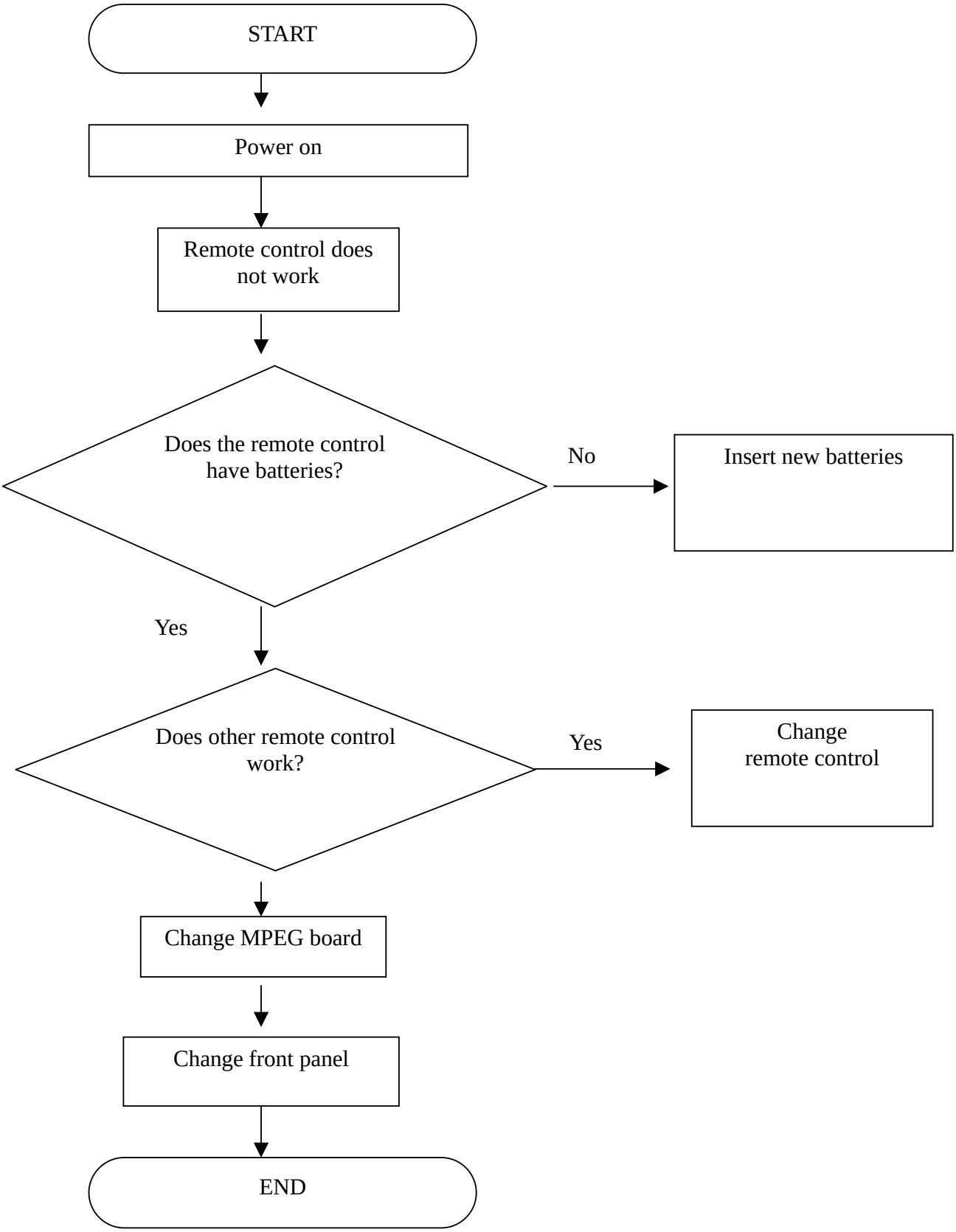
(iv)Figure 4


START
Power on
Insert VCD DVD CD-R/RW DVD-R/RW
DVD+R/RW PHOTO CD
VFD Display "NO DISC" or the unit DEAD
Change the 24PIN cable
(from loader to mpeg board)
Change loader
Change MPEG board
END

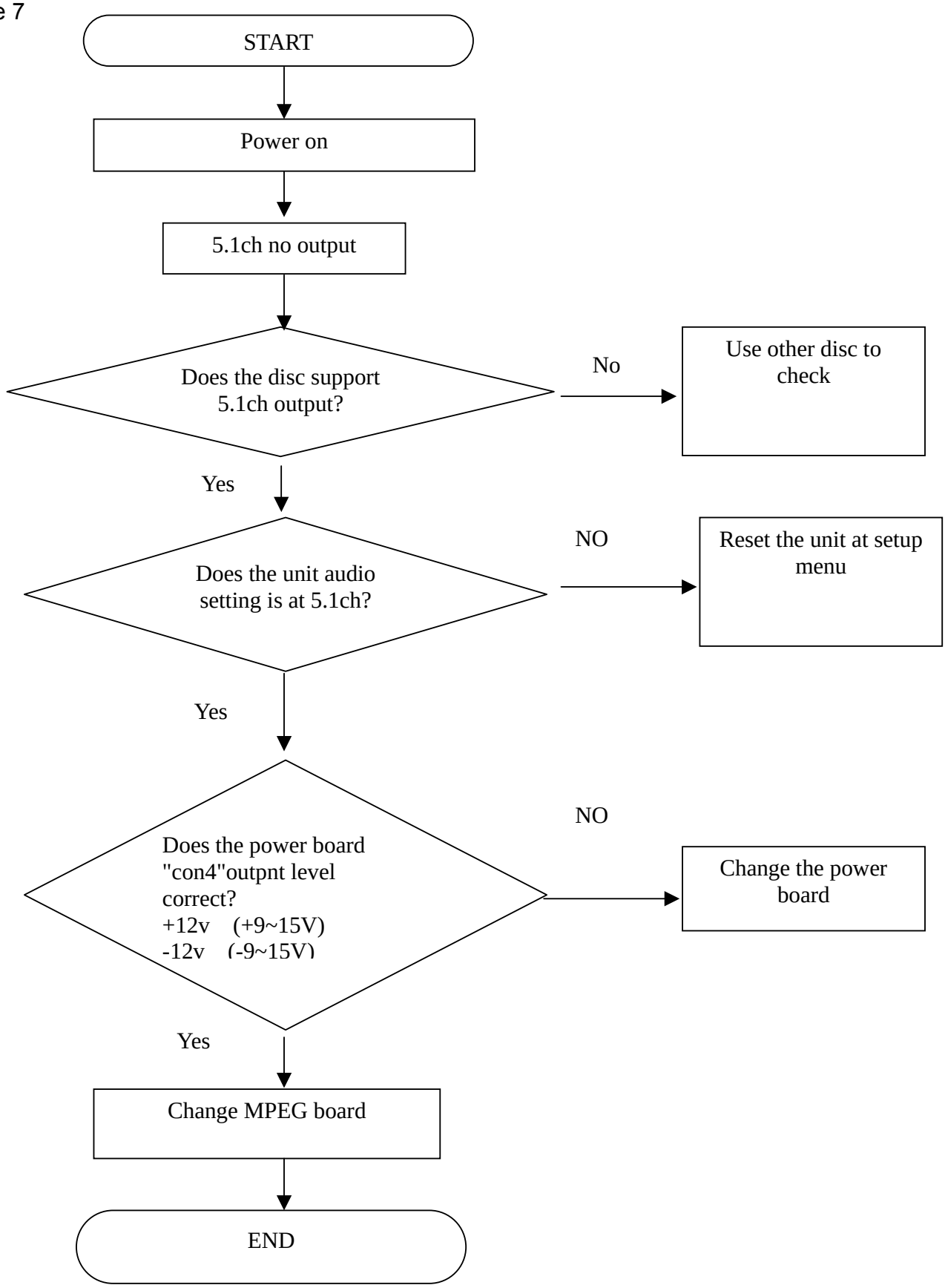
(v)Figure 5


START
Power on
Ear phone no output
Does ear phone board and power board have correct connection?
No
Change the cable
Yes
Change MPEG board
Change front panel
END

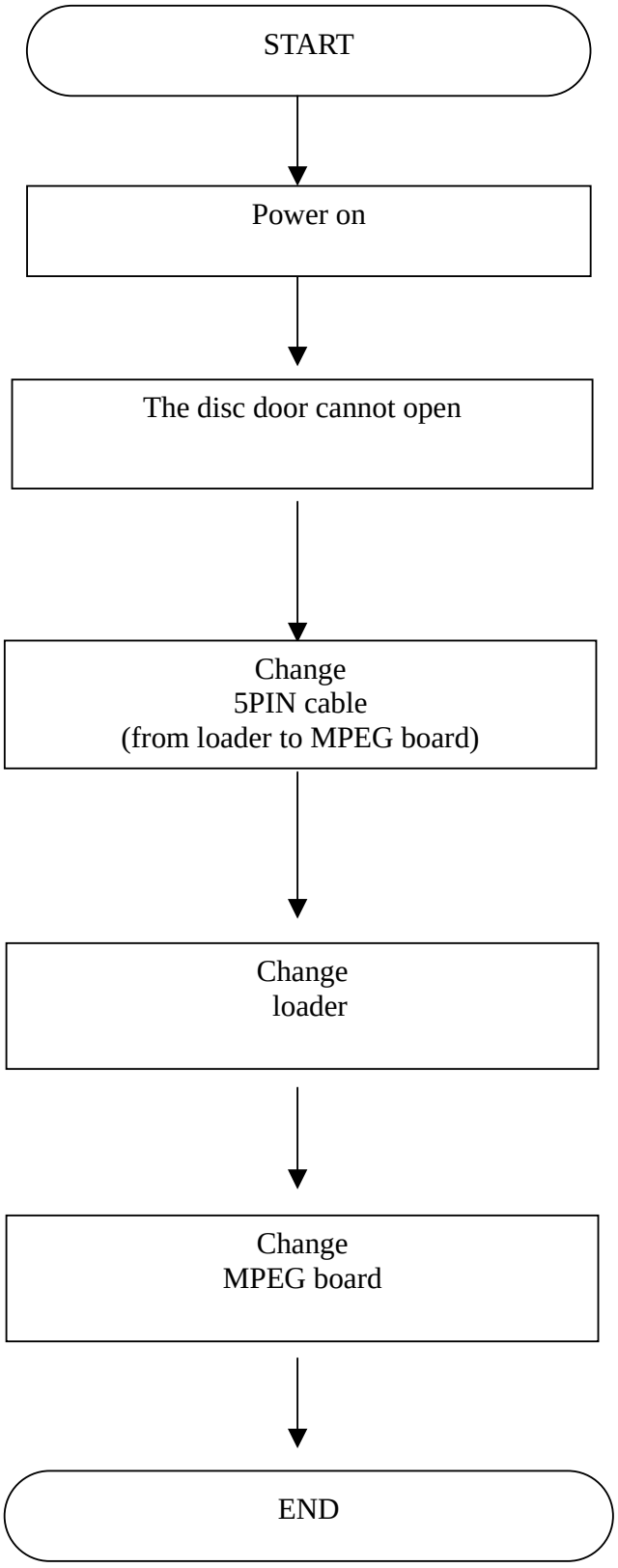
(vi) Figure 6


START
Power on
Remote control does not work
Does the remote control have batteries?
No
Insert new batteries
Yes
Does other remote control work?
Yes
Change remote control
Change MPEG board
Change front panel
END

(vii)Figure 7


START
Power on
5.1ch no output
Does the disc support 5.1ch output?
No
Use other disc to check
Yes
Does the unit audio setting is at 5.1ch?
NO
Reset the unit at setup menu
Yes
Does the power board "con4"outpnt level correct?
+12v (+9~15V)
-12v (-9~15V)
NO
Change the power board
Yes
Change MPEG board
END

(viii)Figure 8



6.ELECTRICAL PART LIST

A. MPEG board

Item	Name of Components	Specification	Qty	Location
1	PCB 板	ESS-66X8 PCB REV:1.3	1	
2	IC	8MFLASH 29F800BA--70PFTN	1	U2
3	IC	ES6688	1	U1
4	IC	ES6603	1	UU2
5	IC	SDRAM 4Mx16--6T,	1	U5
6	IC	24C02	1	U3
7	IC	74HC04	1	U13
8	IC	V6300	1	U8
9	IC	BA6287F	1	UU5
10	IC	BA5954FP	1	UU3
11	IC	WM8746 /DA1196	1	U9
12	IC	RC4558	3	U12，U14，U15
13	IC	TL3472	1	UU4
14	IC	AMS1117/LM1117	3	Q4,Q3,QQ4
15	Jack	TJC3-7(7pin x2.54mm)	1	J4
16	Jack	TJC3-3 (3pin x 2.54mm)	1	J1
17	Jack	FPC Jack(24Pin Pitch0.5mm）	1	JJ3
18	Jack	PH2.0 (5pin x 2.0mm)	2	JJ5, J2
19	Jack	PH2.0 (6pin x 2.0mm)	1	J12
20	Jack	PH2.0 (11pin x 2.0mm)	1	J6
21	Jack	TOTX179	1	J8
22	Jack	AV1-8.4-1S	1	J9

23	Jack	4PIN,AV4---8.4---13P	1	J13
24	Jack	6PIN,AV6---8.4---13P	1	J10
25	Crystal	27M-30ppm HC-49S	1	Y1
26	Transistor	PMBT3904，NPN type	1	Q9
27	Transistor	2SC3327	6	Q7,Q12,Q17,Q18,Q19,Q22
28	Transistor	8550	2	Q6,Q8
29	Transistor	8050	1	Q2
30	Transistor	2SB1132	2	QQ1,QQ2
31	Chip Bead	FB0805-0.2A-26@100MHz	9	LL1,LL2,LL4,LL5,LL6,FB1,FB2,FB4,LL3
32	Chip Bead	FB1206-0.2A-26@100MHz	6	L11,L12,L13,L14,L15,L16
33	chip Inductor	LG0805-0.2A-1.8uH±10%	5	L1,L2,L3,L4,L5
34	Chip diode	4.3V 1/2W	1	D14
35	Chip diode	1N6263	10	D1,D2,D3,D4,D5,D6,D7,D8,D9,D10
36	Chip diode	1N4148	7	D15,D16,D17,DD1,DD2,DD3,D13
37	chip Resistor	R0603-0Ω ±5%	18	RL3,R5,R14,R17,R19,R20,R40,R43 R61,R157,RR10,RR11,RR19,RR41 RR58,RR72,RR75,RR87
38	chip Resistor	R0805-1 Ω±5%	4	RR66,RR67,RR68,RR69
39	chip Resistor	R0805-3.3Ω±5%	1	RR83
40	chip Resistor	R0603-10Ω ±5%	8	R82,R98,R115,R127 R133,R145,RR45,RR46
41	chip Resistor	R0603-33Ω ±5%	23	R23,R24,R25,R26,R28,R29,R30,R31 R44,R48,R49,R50,R52,R58,R60,R63 R65,R66,R68,RR27,RR28,RR29,RR52
42	chip Resistor	R0603-47Ω±5%	1	R33
43	chip Resistor	R0603-68Ω±5%	1	R113
44	chip Resistor	R0603-75Ω±5%	5	R6,R11,R12,R15,R16
45	chip Resistor	R0603-91Ω±5%	1	R105
46	chip Resistor	R0603-100Ω±5%	2	RR35,RR36
47	chip Resistor	R0603-150Ω±5%	1	R76
48	chip Resistor	R0603-240Ω±1%	1	R80

49	chip Resistor	R0603-330Ω±1%	1	R75
50	chip Resistor	R0603-330Ω±5%	2	R102,R125
51	chip Resistor	R0603-360Ω±5%	1	R13
52	chip Resistor	R0603-412Ω±1%	2	R74,RR85
53	chip Resistor	R0603-470Ω±5%	1	R95
54	chip Resistor	R0603-681Ω±1%	2	R79,RR86
55	chip Resistor	R0603-1KΩ±5%	6	R21,R22,R89,R90,RR43,RR56
56	chip Resistor	R0603-1.2KΩ±5%	3	RR16,RR37,RR39
57	chip Resistor	R0603-1.5KΩ±5%	2	RR71,RR79
58	chip Resistor	R0603-2KΩ±5%	6	R88,R108,R131,R124,R140,R152
59	chip Resistor	R0603-2.2KΩ±5%	1	R85
60	chip Resistor	R0603-3.3KΩ±5%	11	R87,R107,R123,R130,R139,R151 RR3,RR4,RR5,RR6,RR55
61	chip Resistor	R0603-4.7KΩ±5%	7	R7,R8,R9,R10,R27,R73,RR76
62	chip Resistor	R0603-5.1KΩ±5%	3	RR18,RR24,RR50
63	chip Resistor	R0603-6.8KΩ±5%	6	R83,RR20,RR21,RR22,RR25,RR26
64	chip Resistor	R0603-10KΩ±5%	5	RR7,RR17,RR44,RR70,RR77
65	chip Resistor	R0603-11kΩ±5%	6	R86,R106,R122,R129,R138,R150
66	chip Resistor	R0603-12kΩ±1%	1	RR34
67	chip Resistor	R0603-12kΩ±5%	1	RR53
68	chip Resistor	R0603-18kΩ±5%	6	R94,R111,R126,R132,R141,R153
69	chip Resistor	R0603-20kΩ±5%	1	RR9
70	chip Resistor	R0603-22kΩ±5%	3	RR48,RR74,RR82
71	chip Resistor	R0603-33kΩ±5%	3	RR15,RR47,RR51
72	chip Resistor	R0603-47kΩ±5%	2	RR49,RR54
73	chip Resistor	R0603-68kΩ±5%	1	RR8
74	chip Resistor	R0603-100kΩ±5%	8	R42,R84,R100,R93, R117,R128,R136,R148
75	chip Resistor	R0603-1MΩ±5%	2	R96,RR73

76	chip Resistor	R0603-10MΩ±5%	1	R91
77	chip Resistor	0603 ,10Ωx4	3	RN1,RN2,RN3
78	chip Resistor	0603 ,33Ωx4	2	RN9,RN10
79	chip Resistor	0603 ,4.7kΩx4	1	RN4
80	chip capacitor	C0603-22P±5%	6	C37,C47,C56,C60,C67,C81
81	chip capacitor	C0603-27P±5%	2	C13,C14
82	chip capacitor	C0603-33P±5%	3	CC35,CC36,CC37
83	chip capacitor	C0603-47P±5%	1	CC25
84	chip capacitor	C0603-100P±5%	2	CC70,CC72
85	chip capacitor	C0603-120P±5%	1	CC57
86	chip capacitor	C0603-150P±5%	6	C40,C50,C57,C63,C69,C83
87	chip capacitor	C0603-160P±5%	1	CC65
88	chip capacitor	C0603-330P±20%	10	C1,C2,C3,C4,C5,C6,C9,C10,C11,C12
89	chip capacitor	C0603-470P±20%	3	CC41,CC43,CC86
90	chip capacitor	C0603-560P±20%	3	CC23,CC30,CC33
91	chip capacitor	C0603-820P±20%	1	CC48
92	chip capacitor	C0603-1000P±20%	12	C43,C52,C58,C64,C70,C90,CC1 CC2,CC3,CC4,CC64,CC71
93	chip capacitor	C0603-2200P±20%	4	CC51,CC52,CC53,CC56
94	chip capacitor	C0603-4700P±20%	3	CC6,CC11,CC73
95	chip capacitor	C0603-6800P±20%	1	CC17
96	chip capacitor	C0603-0.01U±20%	4	CC40,CC42,CC45,CC67
97	chip capacitor	C0603-0.015U±20%	3	CC28,CC31,CC32
98	chip capacitor	C0603-0.033U±20%	1	CC66
99	chip capacitor	C0603-0.047U±20%	2	CC21,CC54

100	chip capacitor	C0603-0.1U±20%	65	B9,B10,B11,B12,B15,B18,B23,B24,B25 B26,B27,B28,B29,B30,B31,B32,B33,B36 B37,B38,B39,B40,B41,B42,B44,B45,B46 B47,B48,B49,B50,C7,C8,C30,C42,C48 C72,C73,C74,C75,C84,C85,C86,CC5,CC13 CC14,CC15,CC22,CC24,CC26,CC27 CC34,CC38,CC39,CC44,CC47,CC49 CC50,CC60,CC62,CC75,CC77,CC80,CC81 ,CC94
101	chip capacitor	C0603-0.22U±20%	1	CC63
102	chip capacitor	C0603-1U±20%	6	CC10,CC12,CC20,CC83 CC88,CC92
103	Electrolytic capacitor	CD-11,4.7U/25V±20%	1	CC8
104	Electrolytic capacitor	CD-11,10U/25V±20% size:Φ4x5	18	B1,B60,C16,C17,C18,C20,C22,C26, C31 C35,C45,C55,C59,C65,C79,C87,C88,C89
105	Electrolytic capacitor	CD-11,10U/25V±20%	10	B13,B19,B34,B43,B51,B61,C71,C76,C77,C 78
106	Electrolytic capacitor	CD-11,100U/16V ±20%	12	B2,B3,B4,B20,B22,CC68,CC69 CC78,CC85,CC87,CC89,CC91
107	Electrolytic capacitor	CD-11,220U/16V±20%	5	B5,B7,C38,CC93,B14
108	Electrolytic capacitor	CD-11,470U/25V±20%	2	C36,CC84

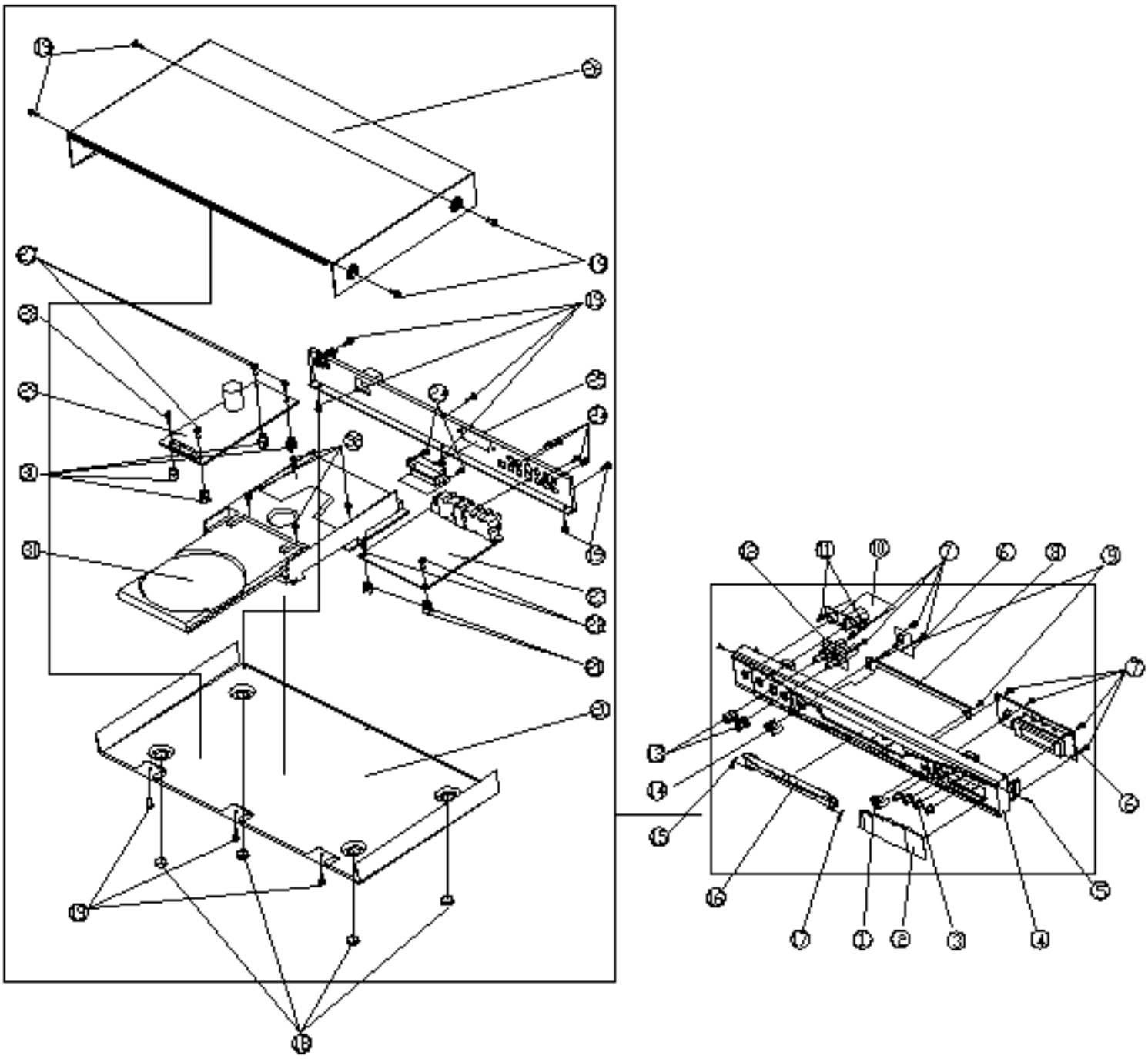
B. Power board

Item	Name of Components	Specification	Qty	Location
1	Carbon Film Resistor	RT14-1/4W-10-±5%	4	R7,R8,R16,R17
2	Carbon Film Resistor	RT14-1/4W-270-±5%	2	R15,R10
3	Carbon Film Resistor	RT14-1/4W-1K-±5%	4	R9,R14,R18,R21
4	Carbon Film Resistor	RT14-1/4W-2K2-±5%	1	R13
5	Carbon Film Resistor	RT14-1/4W-4K7-±5%	1	R19
6	Carbon Film Resistor	RT14-1/4W-100K-±5%	2	R5,R6
7	Carbon Film Resistor	RT14-1/4W-470K-±5%	4	R1,R2,R3,R4
8	Carbon Film Resistor	RT13-1/2W-22-±5%	3	L5,L3,L4
9	Metal Film Resistor	RJ14-1/4W-1K-±1%	2	R11,R12
10	Electrolytic capacitor	CD11-470u-16V--20%+80%	1	EC7
11	Electrolytic capacitor	CD11-47u-25V--20%+80%	1	EC9
12	Electrolytic capacitor	CD11-220u-25V--20%+80%	1	EC5
13	Electrolytic capacitor	CD11-22u-50V--20%+80%	3	EC2,EC11,EC13
14	Electrolytic capacitor	CD293-47u-400V--20%+80%	1	EC1 (6.5mm)
15	Electrolytic capacitor(high frequency)	CD288-1000u/16V--20%+80%	1	EC6
16	Electrolytic capacitor(high frequency)	CD288-100u/16V--20%+80%	1	EC12
17	Electrolytic capacitor(high frequency)	CD288-100u/25V--20%+80%	1	EC8
18	Electrolytic capacitor(high frequency)	CD288-470u/25V--20%+80%	1	EC4
19	Electrolytic capacitor(high frequency)	CD288-100u/50V--20%+80%	1	EC10
20	Ceramic capacitor	CC1-50V-0.1u--20%+80%	1	C19
21	Ceramic capacitor	CC1-50V-470P--20%+80%	2	C7,C9
22	Ceramic capacitor	CC1-50V-10n--±20%	1	C5
23	Polyester capacitor	CC1-100V-220n--20%+80%	1	C6
24	High Voltage Ceramic Capacitors	CC81-1KVDC-10nF-±20%	1	C4
25	High Voltage Ceramic Capacitors	CC81-1KVDC-0.1nF-±20%	1	C3

26	Safety Regulation capacitor	CT7-400VAC-1n-±20%	3	C16,C17,C18
27	Capacitor	CBB230-275VAC-100n-M	1	C1
28	ferrite core Inductor	22uH-±10%-9X12mm-5mm	2	L1,L2
29	Bead	LB-3.5*9mm-5A-90	1	L6
30	Diode	1N4007	4	D1,D2,D3,D4
31	Diode	SR360	1	D7
32	Diode	HER102	1	D11
33	Diode	HER103	3	D5,D9,D10
34	Diode	HER107	1	D6
35	Diode	HER153	1	D8
36	Zener Diode	3.9V-5mA-1/2W-(DO-35)	1	ZD1
37	IC	305T817	1	U2
38	IC	KA5L0380R	1	U1
39	IC	TL431	1	U3
40	Fuse	RTH-30-630mA-250VAC	1	(F1)
41	Fuse Jack	FC-21	2	F1
42	Jack	VH-3(7.92mm,2pins）	2	CON1,CON2
43	Jack	TJC3-5A(2.54mm,5pins）	1	CON6
44	Jack	TJC3-7(2.54mm,7pins）	1	CON4
45	Transformer	BCK28C929A	1	T1
46	Filter	LT16U137 68mH	1	LF1
47	grounding pin		2	
48	Heatsink	16x10x26mm	1	U1
49	Screw	PM3X8	1	U1
50	Jumper	φ0.6--9mm	3	R31,J3,J8
51	Jumper	φ0.6--4mm	1	J5

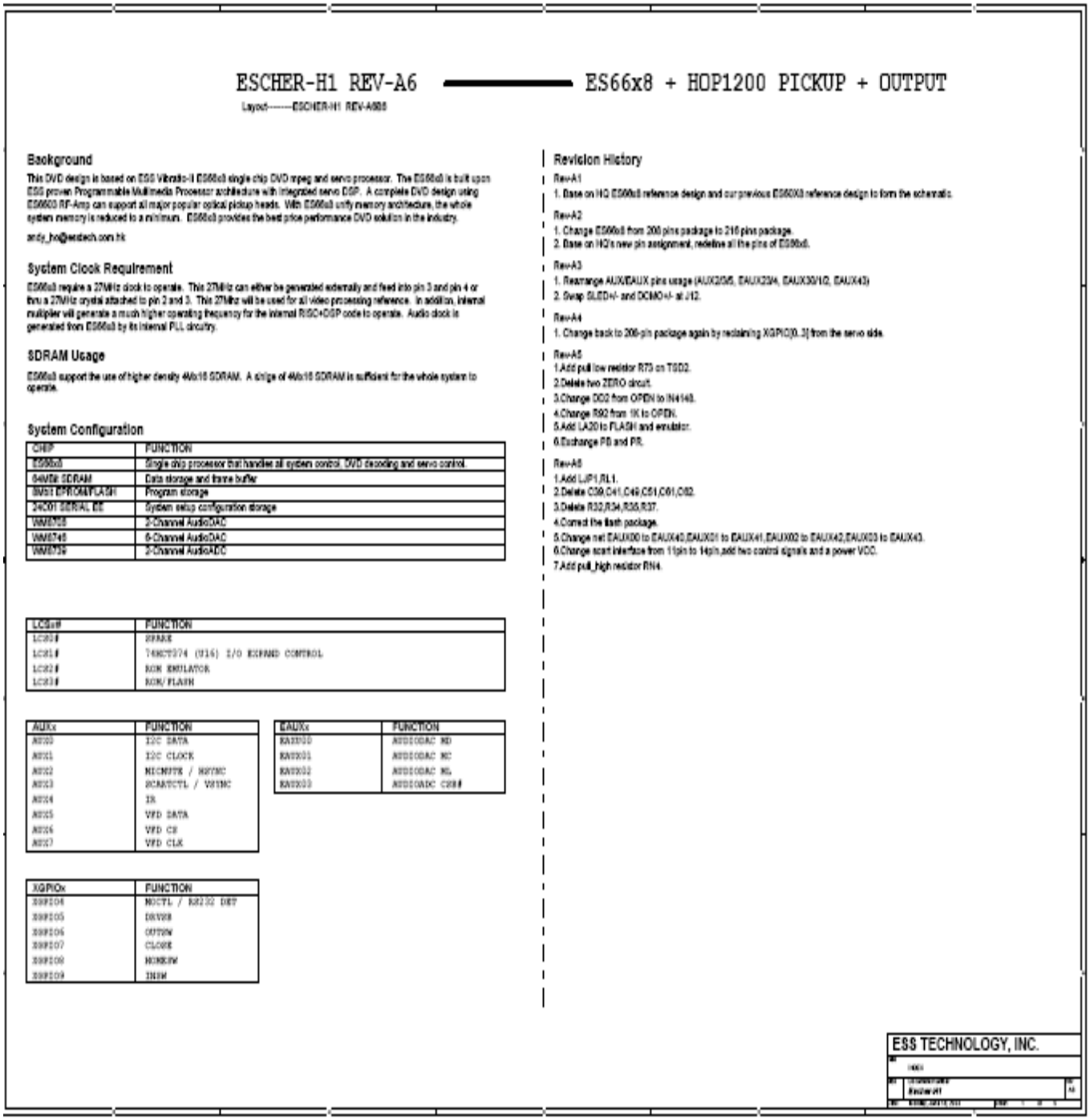
52	Jumper	φ 0.6--6.5mm	1	J7
53	Jumper	φ 0.6--15mm	2	J1,J2
54	PCB board	153mmX57mm	1	DVD-POWER-03 VER2.0

7.DISASSEMBLY AND REASSEMBLY



8.CIRCUIT DIAGRAMS

A. Index



ESCHER-H1 REV-A6 ——— ES66x8 + HOP1200 PICKUP + OUTPUT

Layout------ESCHER-H1 REV-A606

Background

This DVD design is based on ESS Vibrato-II ES66x8 single chip DVD mpeg and servo processor. The ES66x8 is built upon ESS proven Programmable Multimedia Processor architecture with integrated servo DSP. A complete DVD design using ES6603 RF-Amp can support all major popular optical pickup heads. With ES66x8 unify memory architecture, the whole system memory is reduced to a minimum. ES66x8 provides the best price performance DVD solution in the industry.

andy_ho@esstech.com.hk

System Clock Requirement

ES66x8 require a 27MHz clock to operate. This 27MHz can either be generated externally and feed into pin 3 and pin 4 or thru a 27MHz crystal attached to pin 2 and 3. This 27Mhz will be used for all video processing reference. In addition, internal multiplier will generate a much higher operating frequency for the internal RISC+DSP code to operate. Audio clock is generated from ES66x8 by its internal PLL circuitry.

SDRAM Usage

ES66x8 support the use of higher density 4Mx16 SDRAM. A single of 4Mx16 SDRAM is sufficient for the whole system to operate.

System Configuration

CHIP	FUNCTION
ES66x8	Single chip processor that handles all system control, DVD decoding and servo control
64MBit SDRAM	Data storage and frame buffer
8Mbit EPROM/FLASH	Program storage
24C01 SERIAL EE	System setup configuration storage
VAM6708	2-Channel AudioDAC
VAM6746	6-Channel AudioDAC
VAM6736	2-Channel AudioADC

LCSx#	FUNCTION
LCS0#	SPARE
LCS1#	74HCT374 (V16) I/O EXPAND CONTROL
LCS2#	ROM EMULATOR
LCS3#	ROM/FLASH

AUXx	FUNCTION
AUX0	I2C DATA
AUX1	I2C CLOCK
AUX2	MECHSTB / MSYNC
AUX3	SCANCTL / VSYNC
AUX4	IR
AUX5	VFD DATA
AUX6	VFD CE
AUX7	VFD CLK

EAUXx	FUNCTION
EAUX00	AUDIODAC MD
EAUX01	AUDIODAC MC
EAUX02	AUDIODAC ML
EAUX03	AUDIOADC CSB#

XGPIOx	FUNCTION
XGPIO4	MUCTL / RS232 DET
XGPIO5	DRVSB
XGPIO6	OPTSW
XGPIO7	CLOSE
XGPIO8	HOMESW
XGPIO9	INSW

Revision History

Rev-A1
1. Base on HQ ES66x8 reference design and our previous ES6603 reference design to form the schematic.

Rev-A2
1. Change ES66x8 from 208 pins package to 216 pins package.
2. Base on HQ's new pin assignment, redefine all the pins of ES66x8.

Rev-A3
1. Rearrange AUX/EAUX pins usage (AUX2/3/5, EAUX2/4, EAUX30/40, EAUX43)
2. Swap SLED+/- and DCMO+/- at J12.

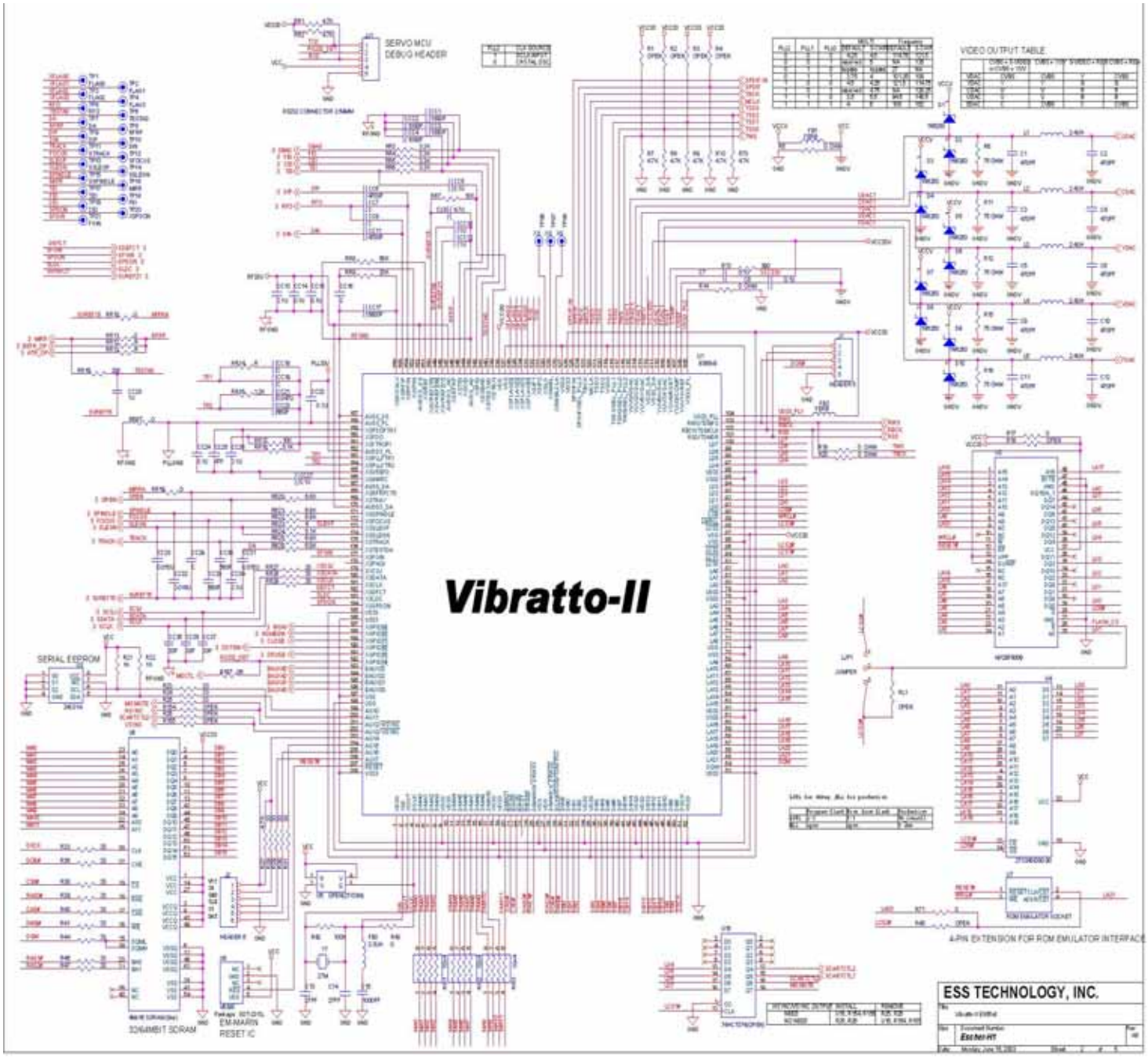
Rev-A4
1. Change back to 208-pin package again by reclaiming XGPIO[0..3] from the servo side.

Rev-A5
1.Add pull low resistor R70 on TSD2.
2.Delete two ZERO circuit.
3.Change DD2 from OPEN to IN4148.
4.Change R92 from 1K to OPEN.
5.Add LA20 to FLASH and emulator.
6.Exchange PB and PR.

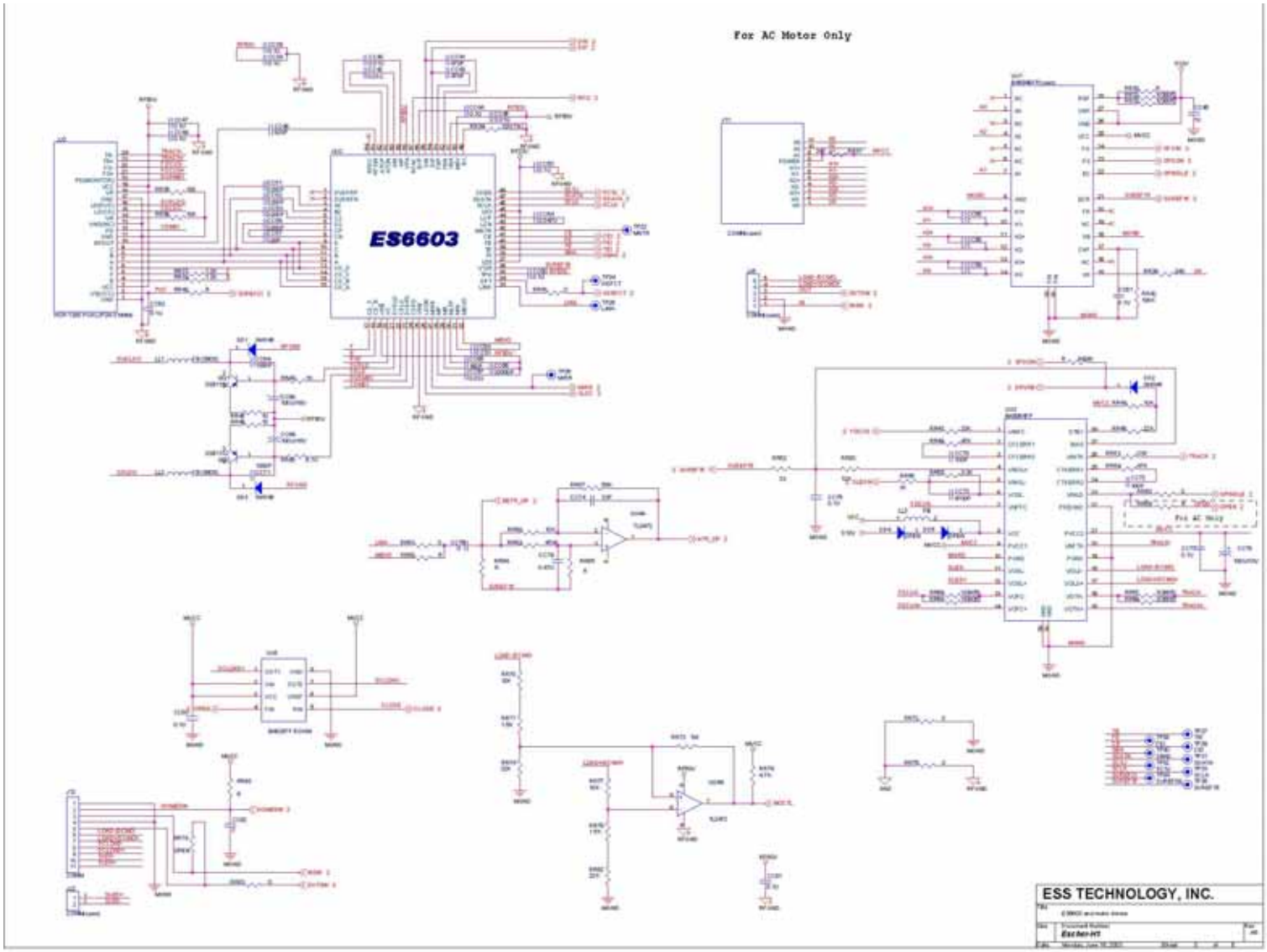
Rev-A6
1.Add LJP1,RL1.
2.Delete C39,C41,C49,C51,C61,C62.
3.Delete R32,R34,R35,R37.
4.Correct the flash package.
5.Change net EAUX00 to EAUX40,EAUX01 to EAUX41,EAUX02 to EAUX42,EAUX03 to EAUX43.
6.Change scart interface from 11pin to 14pin,add two control signals and a power VCC.
7.Add pull_high resistor RN4.

ESS TECHNOLOGY, INC.

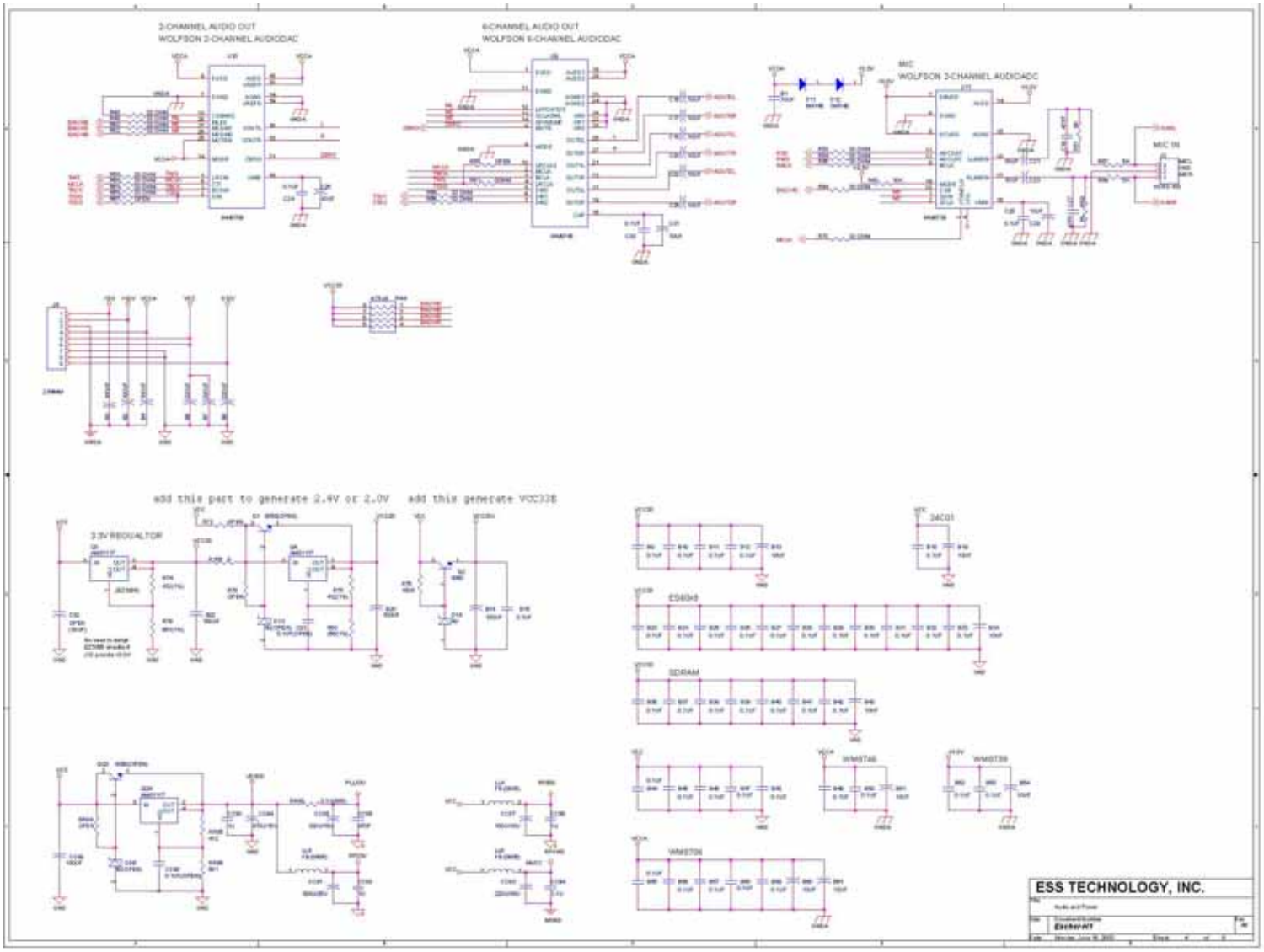
B. Vibratto-II ES66x8



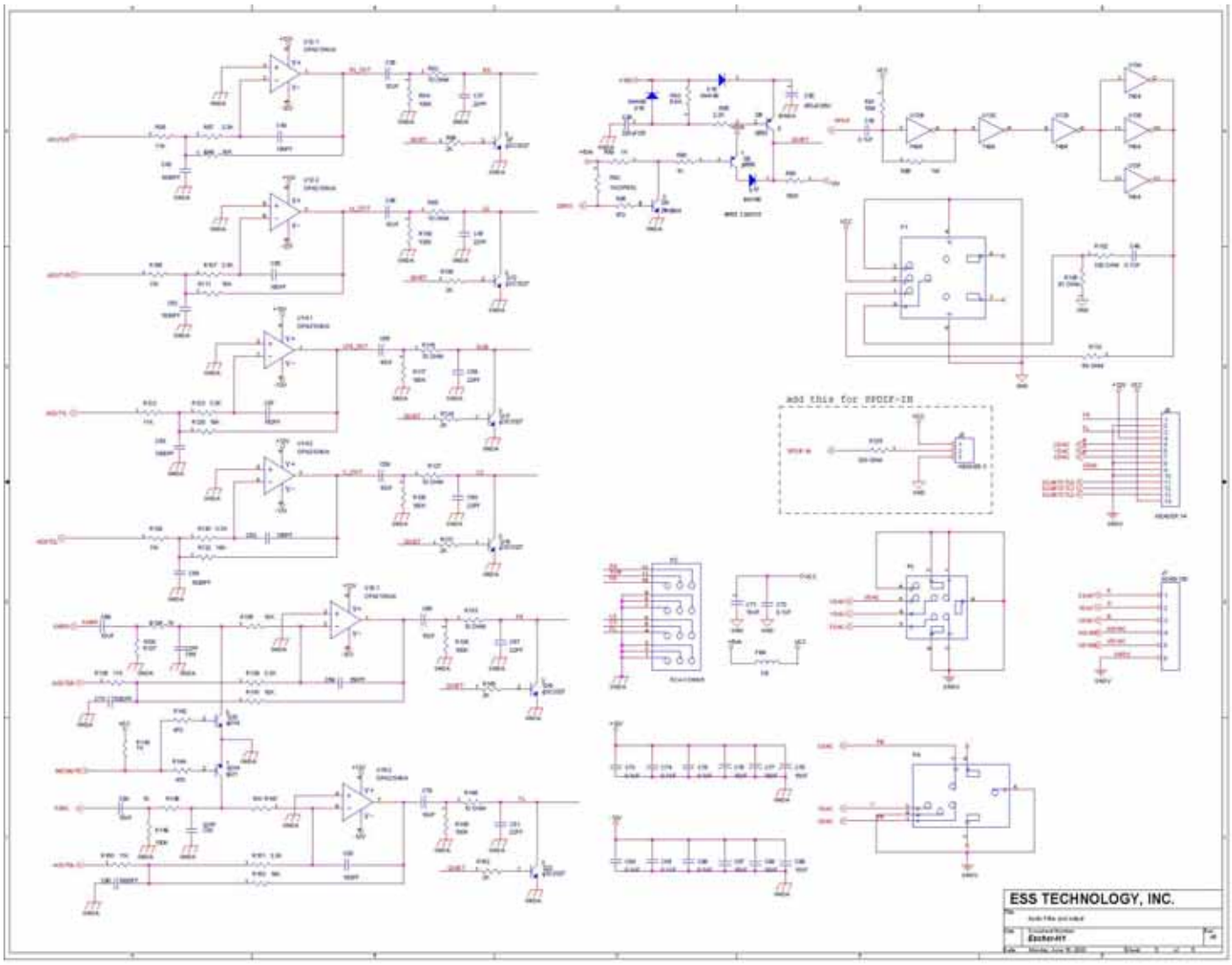
C. Motor Drives



D. Audio and Power



E. Audio Filter and output



8.WIRING DIAGRAM