LOGIC Emulation Source

User Guide

DN8000K10PCIEe

LOGIC EMULATION SOURCE

DN8000K10PCIEe User Manual
Version 0.0

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1

About This Manual

Welcome to DN8000K10PCIE Logic Emulation Board

Congratulations on your purchase of the DN8000K10PCIE LOGIC Emulation Board. If you are unfamiliar with Dini Group products, you should read Chapter 2, Quick Start Guide to familiarize yourself with the user interfaces the DN8000K10PCIE provides.

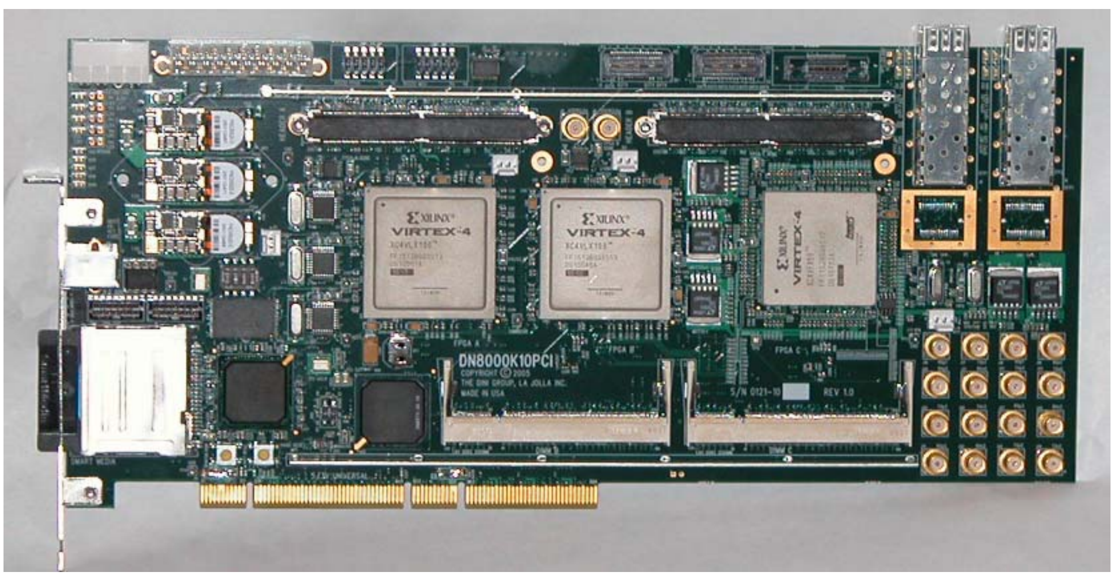


Figure 1 DN8000K10PCIE

1 Manual Contents

This manual contains the following chapters:

About This Manual

List of available documentation and resources available. Reader's Guide to this manual

Quick Start Guide

Step-by-step instructions for powering on the DN8000K10PCIE, loading and communicating with a simple provided FPGA design and using the board controls.

Board Hardware

Detailed description and operating instructions of each individual circuit on the DN8000K10PCIE

Controller Software

A summary of the functionality of the provided software. Implementation details for the remote USB board control functions and instructions for developing your own USB host software.

Reference Design

Detailed description of the provided DN8000K10PCIE reference design. Implementation details of the reference design interaction with DN8000K10PCIE hardware features.

FPGA Design Guide

Information needed to use the DN8000K10PCIE with third-party software, including Xilinx ISE, Synplicity Synplify, Certify, and Identify. Some commonly asked questions and problems specific to the DN8000K10PCIE

Ordering Information

Contains a list of the available options and available optional equipment. Some suggested parts and equipment available from third party vendors.

2 Additional Resources

For additional information, go to http://www.dinigroup.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
UserDN8000K10PCIE User Guide	This is the main source of technical information. The manual should contain most of the answers to your questions
Dini Group Web Site	The web page will contain the latest manual, application notes, FAQ, articles, and any device errata and manual addenda. Please visit and bookmark: http://www.dinigroup.com
Virtex 4 User Guide	Xilinx publication UG070 http://www.xilinx.com/bvdocs/userguides/ug070.pdf Most of your questions regarding usage and capabilities of the Virtex 4 devices will be answered here, including readback, boundary scan, configuration, and debugging
E-Mail	You may direct questions and feedback to the Dini Group using this e-mail address: support@dinigroup.com
Phone Support	Call us at **858.454.3419** during the hours of 8:00am to 5:00pm Pacific Time.
FAQ	The download section of the web page contains a document called **DN8000K10PCIE Frequently Asked Questions (FAQ)**. This document is periodically updated with information that may not be in the User's Manual.

Figure 2 Support Resources

3 Conventions

This document uses the following conventions. An example illustrates each convention.

3.1 Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: -100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** ***`design_name`***

Convention	Meaning or Use	Example
Garamond bold	Commands that you select from a menu	**File →Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	ngdbuild *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Braces [ ]	An optional entry or parameter. However, in bus specifications, such as bus[7:0], they are required.	ngdbuild [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**lowpwr ={on|off}**
Vertical bar |	Separates items in a list of choices	**lowpwr ={on|off}**
Vertical ellipsis - - -	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' - -
Horizontal ellipsis . . .	Repetitive material that has been omitted	**allow block** *block_name* *loc1 loc2 ... locn;*
Prefix "0x" or suffix "h"	Indicates hexadecimal notation	Read from address 0x00110373, returned 4552494h
Letter "#" or "_n"	Signal is active low	INT# is active low fpga_inta_n is active low

3.2 Content

3.2.1 File names

Paths to documents included on the User CD are prefixed with "D:\". This refers to your CD drive's root directory.

3.2.2 Physical orientation and Origin

By convention, the board is oriented as show on page 3, with the "top" of the board being the edge near Headers A and B, and the edge with the optical module connectors. The "right" edge is near the SMA connectors, the "left" side is the side with the PCI bezel. "topside" refers to the side of the PWB with FPGAs soldered to it, "backside" is the side with the daughtercard connectors. The reference origin of the board is the center of the lower PCI bezel mounting hole.

3.2.3 Part Pin Names

Pin names are given in the form <*X*><*Y*>.<*Z*>; The <*X*> is one of: U for ICs, R for resistors, C for capacitors, P or J for connectors, FB or L for inductors, TP for test points, MH for mounting structures, FD for fiducials, BT for sockets, DS for diodes, F for fuses, HS for mechanicals, PSU for power supply modules, Q for discreet semiconductors, RN for resistor networks, X for oscillators, Y for crystals. <*Y*> is a number uniquely identifying each part from other parts of the same X class on the same PWB. <*Z*> is the pin or terminal number or name, as defined in the datasheet of the part. Datasheets for all standard and optional parts used on the DN8000K10PCIE are included in the Document library on the provided User CD.

3.2.4 Schematic Clippings

Partial schematic drawings are included in this document to aid quick understanding of the features of the DN8000K10PCIE. These clippings have been modified for clarity and brevity, and may be missing signals, parts, net names and connections. Unmodified Schematics are included in the User CD document library as *Appendix Schematics*. Please refer to this document. Use the PDF search feature to search for nets and parts.

3.2.5 Terminology

Abbreviations and pronouns are used for some commonly used phrases.

MGT and **RocketIO** are used interchangeably. MGT is multi-gigabit transceiver. RocketIO is the Xilinx trademark on their multi gigabit transceiver hardware.

MCU is the Cypress FX2 Microcontroller, U39

Chapter

2

Quick Start Guide

The Dini Group DN8000K10PCIE is the user-friendliest board available with multiple Virtex 4 FPGAs. However, due to the number of features and flexibility of the board, it will take some time to become familiar with all the control and monitoring interfaces equipped on the DN8000K10PCIE. Please follow this quick start guide to become familiar with the board before starting your ASIC emulation project.

1 Provided Materials

Examine the contents of your DN8000K10PCIE kit. It should contain:

- DN8000K10PCIE board
- Two Smart Media cards
- USB SmartMedia card reader
- RS232 IDC header cable to female DB9
- USB cable
- CD ROM containing:
  - Virtex 4 Reference Design
  - User manual PDF
  - Board Schematic PDF
  - USB program (usbcontroller.exe)
  - Source code for USB program, and DN8000K10PCIE firmware

2 ESD Warning

The DN8000K10PCIE is sensitive to static electricity, so treat the PCB accordingly. The target markets for this product are engineers that are familiar with FPGAs and circuit boards. However, if needed, the following web page has an excellent tutorial on the "Fundamentals of ESD" for those of you who are new to ESD sensitive products:

http://www.esda.org/basics/part1.cfm

There are two large grounded metal rails on the DN8000K10PCIE.

The DN8000K10PCIE has been factory tested and pre-programmed to ensure correct operation. You do not need to alter any jumpers or program anything to see the board work. A reference design is included on the provided CD and SmartMedia card.

The 200-pin connectors are not 5V tolerant. According to the Virtex 4 datasheets, the maximum applied voltage to these signals is VCCO + 0.5V (3.0V while powered on). These connections are not buffered, and the Virtex 4 part is sensitive to ESD. Take care when handling the board to avoid touching the daughtercard connectors.

3 Power-On Instructions

The image below represents your DN8000K10PCIE. You will need to know the location of the following parts referenced in this chapter.

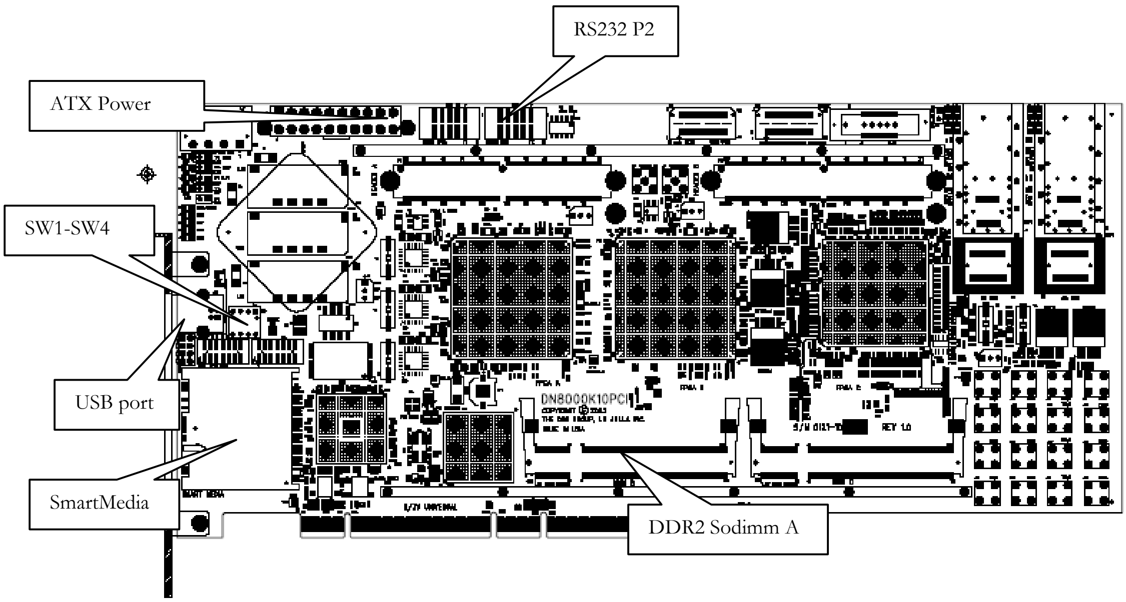


Figure 3 DN8000K10PCIE configuration controls

To begin working with the DN8000K10PCIE, follow the steps below :

3.1 Verify Switch Settings

The DN8000K10PCIE uses a DIP switch to program the FPGA configuration circuitry. The function of these DIP switches is Listed in Table 2. Verify that the switch settings on your board match the default settings.

Table 2 – Switch Description

Switch	Default Position	Signal Name	On setting	Off setting
S1-1	Off	Reserved		
S1-2	Off	Reserved		
S1-3	Off	Bootmode	Firmware update	Normal operation (default)

Switch	Default Position	Signal Name	On setting	Off setting
S1-4	Off	Reserved		

3.2 Memory and heatsinks

There should be an active heatsink installed on each FPGA on the DN8000K10PCIE and a fan over the power supply units. Virtex 4 FPGAs are capable of dissipating 15W or more, so you should always run them with heatsinks installed.

The DN8000K10PCIE comes packaged without memory installed. If you want the Dini Group reference design to test your memory modules, you can install them now in the 1.8V DDR2 DIMM sockets.

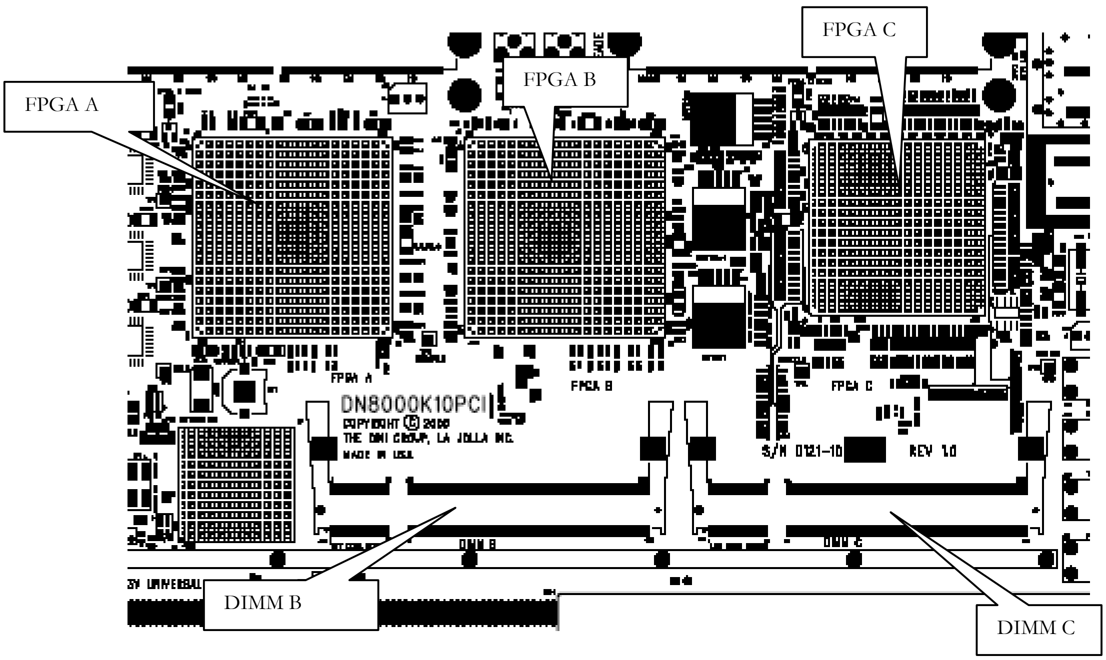


Figure 4 FPGA Names

The socket DIMMB is connected to FPGA B. The socket can accept any capacity DDR2 Sodimm module. Note that DDR1 modules will not work in these slots since they are supplied with 1.8V power and DDR1 requires 2.5V power (and a completely different pin-out).

3.3 Prepare configration files

The DN8000K10PCIE reads FPGA configuration data from a SmartMedia card. To program the FPGAs on the DN8000K10PCIE, FPGA design files (with a .bit file extension) put on the root directoty of the SmartMedia card file using the provided usb card reader.

The DN8000K10PCIE ships with a 32 MB SmartMedia card preloaded with the Dini Group reference design.

1. Insert the provided SmartMedia card labeled "Reference Design" into your usb card reader. Make sure the card contains the files:

   FPGA_A.bit

   FPGA_B.bit

   FPGA_C.bit

   main.txt

   The files FPG_A-C.bit are files created by the Xilinx program bitgen, part of the ISE 7.1 tools. The file main.txt contains instructions for the DN8000K10PCIE configuration circuitry, including which FPGAs to configure, and to which frequency the global clock networks should be automatically adjusted.

2. Insert the SmartMedia card labeled "Reference Design" into the DN8000K10PCIE's SmartMedia slot, contacts down.

3.4 Connect cables

The configuration circuitry can accept user input to control FPGA configuration or provide feedback during the configuration process. The configuration circuitry IO can also be used to transfer data to and from the user design.

1. Use the provided ribbon cable to connect the MCU RS232 port (P2) to a computer serial port to view feedback from the configuration circuitry during FPGA configuration. Run a serial terminal program on your PC (On Windows you can use HyperTerminal Start->Programs->Accessories->Communications->HyperTeminal) and make sure the computer serial port is configured with the following options:

   - Bits per second: 19200
   - Data bits: 8
   - Parity: None
   - Stop Bits: 1
   - Flow control: None
   - Terminal Emulation: VT100

2. Use the provided USB cable to connect the DN8000K10PCIE to a Windows computer (Windows XP is recommended).

3. Plug an ATX power supply into J1, or plug the DN8000K10PCI into a PCI slot. **Do not plug an external power supply into J1 if the DN8000K10PCI is in a PCI slot.** Turn on the ATX power supply.

When the DN8000K10PCIE powers on, it automatically loads Xilinx FPGA design files (ending with a .bit extension), found on the SmartMedia card in the SmartMedia slot into the FPGAs.

3.5 View configuration feedback over RS232

As the DN8000K10PCIE powers on, your RS232 terminal (connected to P2) will display useful information about the Configuration process.

3.5.1 Watch the configuration status output

No USB cable detected, rebooting from FLASH...please wait	
Setting ACLK… N 01 M: 000001000 DONE Setting BCLK... N: 01 M: 000001000 DONE Setting DCLK... N: 01 M: 000001000 DONE Setting R1CLK... N: 01 M: 000001000 DONE Setting R2CLK... N: 01 M: 000001000 DONE	The global clocks (ACLK, BCLK, DCLK) are frequency-configurable. The M binary sequence represents the multiplication applied to the installed crystal. The N represents the division applied. See Appendix X, Clocks and Schematics, U6, U14, U20, U31 and the ICS8442AY datasheet. The MCU is setting the clocks to their default values ACLK 200Mhz, BCLK 108.8Mhz, DCLK 128Mhz, R1CLK (not available on DN8000K10PCIE), R2CLK (**DEFAULT**)
=-=- DN8000K10PCIe MCU FLASH BOOT -=-= -- FPGAS STUFFED -- A B	The MCU detects which FPGAs are present
-- SMART MEDIA INFO -- MAKER ID: EC DEVICE ID: 75 SIZE: 32 MB	The MCU detects if a SmartMedia card is present
-- FILES FOUND ON SMART MEDIA CARD FPGA_B.BIT FPGA_A.BIT MAIN~1.TXT MAIN.TXT -- CONFIGURATION FILES -- FPGA A: FPGA_A.BIT FPGA B: FPGA_B.BIT	The MCU tries to access the SmartMedia card. If the MCU is not successful in reading the files on the SmartMedia card, be sure you have not formatted the card in Windows. Windows uses a non-standard format for media cards and will make the card unreadable. You can download a format utility from dinigroup.com to repair your incorrectly-formatted SM card.
--OPTIONS-- Message level set to default: 2 Sanity check is set to default: ON N: 00 M: 000001010 DONE Setting BCLK... N: 01 M: 000001100 DONE Setting DCLK... N: 01 M: 000001000 DONE Setting R1CLK... N: 01 M: 000001000 DONE Setting R2CLK... N: 01 M: 000001000 DONE	The MCU reads the contents of the file MAIN.TXT and executes each instruction line. Here the MCU is setting the clocks according to instructions in MAIN.TXT
****************************CONFIGURING FPGA: A**************************** -- Performing Sanity Check on Bit File -- -- BIT FILE ATTRIBUTES -- FILE NAME: FPGA_A.BIT FILE SIZE: 003A943B bytes PART: 4vlx100ff151317:09:38 DATA: 2005/07/25 TIME: 17:09:38 Sanity check passed	The MCU is configuring FPGA A according to instructions in MAIN.TXT The sanity check option reads the design (".bit") file headers and verifies that the design is compiled for the same type of FPGA that the MCU detects on your DN8000K10PCIE. If the design and FPGA do not match, the MCU will reject the file and flash the Error LED. You may need to disable to sanity check option (See Chapter X, section X) if you want to encrypt or compress your configuration

Sanity check passed ....DONE WITH CONFIGURATION OF FPGA: A	files.
****************************CONFIGURING FPGA B**************************** -- Performing Sanity Check on Bit File -- -- BIT FILE ATTRIBUTES -- FILE NAME: FPGA_B.BIT FILE SIZE: 003A943B bytes PART: 4vlx100ff151317:05:01 DATA: 2005/07/19 TIME: 17:05:01 Sanity check passed ....DONE WITH CONFIGURATION OF FPGA: B	The MCU is configuring FPGA B according to instructions in MAIN.TXT The MCU is setting the temperature threshold to cause a board reset.
-- TEMPERATURE SENSORS -- A YES B YES FPGA Temperature Alarm Threshold: 80 degrees C DN8000K10PCIe MAIN MENU (Jul 27 2005 10:38:05) 1.) Configure FPGAs using "MAIN TXT" 2.) Interactive configuration menu 3.) Check configuration status 4.) Change MAIN configuration file 5.) List files on Smart Media 6.) Display Smart Media text file 7.) Change RS232 PPC Port 8.) Set FPGA Address 9.) Write to FPGA at current address a.) Read from FPGA at current addres g.) Display FPGA Temperatures h.) Set FPGA Temperature Alarm Threshold ENTER SELECTION:	Here is the MCU main menu Options 8,9, and A are only available when the DN8000K10PCIE reference design is loaded. For more information on how the MCU communicates with the reference design, see Chapeter X, The Reference Design.

Figure 5 RS232 Output

You should see the DN8000K10PCIE MCU main menu. If the reference design is loaded in the Virtex 4 FPGAs, then you should see the above on your terminal. Try pressing 3 to see see if the configration circuit was successful in programming the FPGAs.

```
ENTER SELECTION: 3

******************** CONFIGURATION STATUS *******************

FPGA B NOT configured
```

The easiest way to verify your FPGAs are configured is to look at DS18, DS14, DS16 located above each FPGA. When the green LEDs are lit, the FPGA under it is successfully configured.

3.5.2 Interactive configuration

If you want to put multiple designs on a single Smart Media card, you can use the interactive configuration menu to select which .bit file to use on each FPGAs. Select menu option 2.

```
ENTER SELECTION: 2
-=-= INTERACTIVE CONFIGURATION MENU =-=-


1) Select bit files to configure FPGA(s)
2) Set verbose level (current level = /)
3) Enable sanity check for bit files
M) Main Menu


Enter Selection:
```

Figure 6 Interactive Config Menu

3.5.3 Read temperature sensors

The DN8000K10PCIE is equipped with temperature sensors to measure and monitor the temperature on the die of the Virtex 4 FPGAs. According to the Virtex 4 datasheet, the maximum recommended operating temperature of the die is 85C degrees. If the microcontroller measures a temperature above 80 degrees, it will reset the DN8000K10PCIE.

If you think your DN8000K10PCIE is resetting due to temperature overload, you can use the temperature monitor menu to measure the current junction temperature of each FPGA.

```
ENTER SELECTION: g


-- FPGA TEMPERATURES (Degrees Celsius [+/- 4]) --
B 29
-- Set FPGA Temeraturе Alarm Threshold  --
(degrees C, decimal values, range [1-127])
Old Threshold: 80
New Threshold: 85
Threshold Updated: 85 Degrees C
```

Figure 7 Temperature Threshold Menu

The Virtex 4 FPGA can operate as hot as 120C degrees before damaging the part, although timing specifications are not guaranteed. The MCU allows you to change the reset threshold, although we recommend improving your heat dissipation to maintain a low junction temperature.

3.5.4 Multiplex Serial port

The DN8000K10PCIE has one serial port (P1) for user use. This single port is multiplexed so that any FPGA can access it through its RX and TX signals. You can use the RS232 MCU interface to change the FPGA to which P1 is connected.

```
ENTER SELECTION: 7


PORT 1: D
 PORT 2: A
 PORT 3: A
 PORT 4: A


Enter Port to change (1-4, q to quit): 1
Enter FPGA to set port to (A-I): B
Do you want to change more RS232 Ports (y or n)?: n
```

Figure 8 RS232 Port Menu

The DN8000K10PCIE only has one serial port (Port 1). Changing ports 2-4 will have no effect.

3.6 Check LED status lights

The DN8000K10PCIE has many status LEDs to help the user confirm the status of the configuration process.

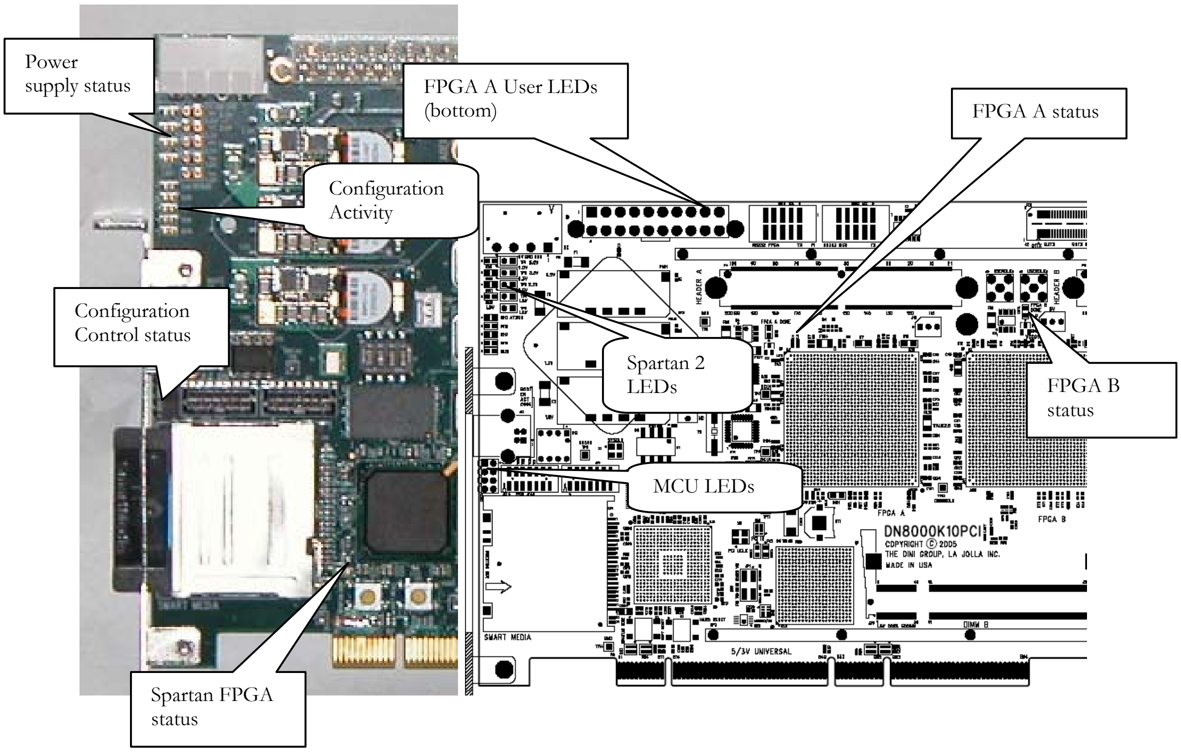


Figure 9 Configuration Status LEDs

1. Check the power voltage indication LEDs to confirm that all voltage rails of the DN8000K10PCIE are present. From the top, the LEDs indicate the presence of 5V, 3.3V, 2.5V, and "ATX POWER OK" Green lit LED's on the voltage present LEDs indicate the rails are greater than 1.7V. A green lit "ATX power OK" indicates that the voltage monitors inside the ATX power supply are within acceptable operating ranges (5V is 4.5 – 5.5V, 3.3V is 3.0-3.6V). If this LED is not lit green, the DN8000K10PCIE might not function properly.

2. Check the Configuration status LEDs. These LEDs are visible from outside the case when the DN8000K10PCIE is installed in an ATX case. Under error conditions, all four red LEDs will blink.

3. Check the Spartan FPGA status LED, DS24. This LED indicates that the Spartan II FPGA has been configured. If this LED is not lit soon after power on, then there may be a problem with the firmware on the DN8000K10PCIE. This LED off or blinking may indicate a problem with one of the board's power supplies.

4. Check the FPGA A status LED, DS18 to the upper left of FPGA A. This green LED is lit when FPGA A is configured and operational. This light should be on if you loaded the reference design from the SmartMedia card.

5. Check the FPGA B status LED, DS14 directly above FPGA B. This light should be lit green if your DN8000K10PCIE was installed with the FPGA B option, and the reference design is loaded.

6. Check the FPGA C status LED, DS16 to the upper left of FPGA C. This green LED will light if you have the FPGA C option and the FPGA is configured.

7. Check the FPGA A User LEDs on the bottom side of the DN8000K10PCIE. If you have successfully loaded the Dini Group's DN8000K10PCIE reference design, these should flash all 8 green LEDs.

8. Check the FPGA C User LEDs on the bottom side of the DN8000K10PCIE. If you have ordered the "FX" FPGA C option, and the reference design is loaded, these will flash all 16 LEDs.

9. If you suspect one or more FPGAs did not configure properly, check the configuration circuitry's status lights. These are four right-angle mounted LEDs viewable out the side of the PC case. If there has been an error, the four LEDs will blink. If there has been no error, the two lower LEDs will be ON and the upper two OFF. If there was an error, the easiest way to determine the cause of the error is to connect a terminal to the RS232 port (P2) and try to configure again. Configuration feedback will be presented over this port.

You should also notice the Fans mounted above the 3 Virtex 4 FPGAs and the Fan mounted above the power supplies spinning.

Assembly Number	**Signal**	**Comment**
DS9	5.0V_PRESENT	The 5.0V power rail is present (above ~1.7V)
DS10	3.3V_PRESENT	The 3.3V power rail is present (abobe ~1.7V)
DS11	2.5V_PRESENT	The 2.5V power rail is present (above ~1.7V)
DS12	1.8V_PRESENT	The 1.8V power rail is present (above ~1.7V)
DS13	ATX_POK	The ATX power supply is generating 5.0V and 3.3V

		within 5% at the source
DS15	SPARTAN_LED3	
DS17	SPARTAN_LED2	This LED will flicker when there is Main Bus activity (See section X.X.X)
DS19	SPARTAN_LED1	This LED will flicker when there is USB activity (Bulk Transfer)
DS20	SPARTAN_LED0	This LED will flicker when there is SmartMedia card activity.
DS21.1 (top)	MCU_LED0	MCU_LED[1:0] Codes:
DS21.2	MCU_LED1	01 FPGA A is configuring 10 FPGA B is configuring 11 FPGA C is configuring
DS21.3	MCU_LED2	The last FPGA configuration was successful
DS21.4 (bottom)	MCU_LED3	Blinking: There was a configuration error. Use the RS232 port to read the error. Off: Configuring. On: The last configuration command was successful
DS24	SPARTAN_DONE	The Spartan 2 configuration FPGA is configured. This light will turn off if the board is in power reset

DS18	FPGA_A_DONE	The Virtex 4 FPGA A is configured
DS14	FPGA_B_DONE	The Virtex 4 FPGA B is configured
DS16	FPGA_C_DONE	The Virtex 4 FPGA C is configured
DS8	SFP2_LOS	SFP module 2 Loss-of-signal
DS4	SFP2_FAULT	SFP module 2 transmitter fault
DS5	XFP2_INT	XFP module 2 error
DS1	XFP2_FAULT	XFP module 2 transmitter fault
DS6	SFP1_LOS	SFP module 1 Loss-of-signal
DS2	SFP1_FAULT	SFP module 1 transmitter fault
DS7	XFP1_INT	XFP module 1 error
DS3	XFP1_LOS	XFP module 1 Loss-of-signal
DS48, DS47, DS46, DS45, DS44, DS43, DS42, DS41,		User LEDs from FPGA C
DS40,DS39, DS38, DS37, DS36, DS35, DS34, DS33,		User LEDs from FPGA A
DS32, DS31, DS30, DS29, DS28, DS27, DS26, DS25		User LEDs from FPGA A

Figure 10 DN8000K10PCIE LEDs

4 Using the Reference Design with the Provided Software

To communicate with the reference design on the DN8000k10PCIE, you should use the USB interface.

The USB interface allows configuration of the FPGAs and bulk data transfer to and from the User design. The RS232 interface allows low-speed data transfers to and from the User design, and control and monitoring of the configuration process.

This section will get you started and show you how to operate the provided software. For detailed information about the reference design and implementation details, see Chapter X, The Reference Design.

4.1 Operating the USB controller program

Use the provided USB monitoring software to verify that the design is loaded into the FPGAs.

1. Insert the CDROM that came with your DN8000K10PCIE into the CDROM drive of your computer.

2. Connect the USB cable to your DN8000K10PCIE and a Windows XP PC. (Before or after the DN8000K10PCIE has powered on)

3. When you connect the USB cable to your PC for the first time, Windows detects the DN8000K10PCIE and asks for a driver. The board should identify itself as a "DiNi Prod FLASH BOOT". When the new device detected window appears, select the option "install from a list" -> select "search for the best driver in these locations". Select "include the location in the search" and browse to the product CD in "Source Code\AETEST_USB\driver\win_wdm\" ->select "finish"

4. After Windows installs the driver, you will be able to see the following device in the USB section of Windows device mananger: "DiniGroup DN8000K10PCIE FLASH boot".

5. Run the USB controller application found on the product CD in "Source Code\USBController\USBController.exe".

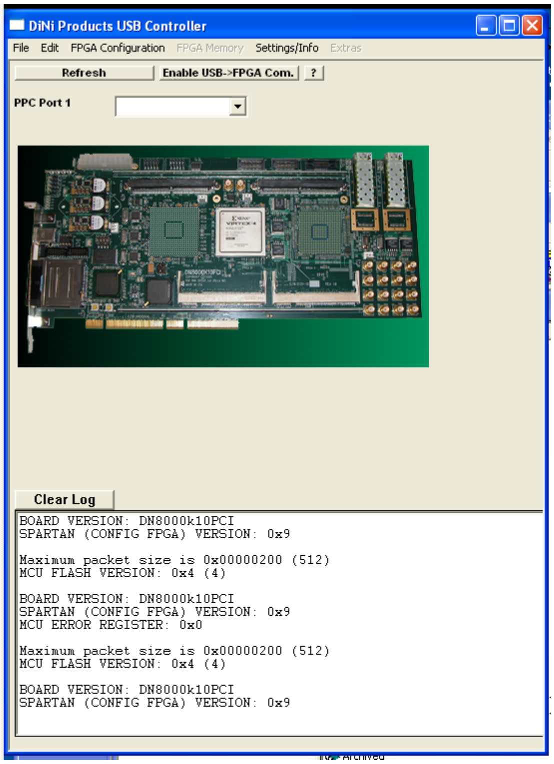


Figure 11 USB Controller Window

6. This window will appear showing the current state of the DN8000K10PCIE. Next to each FPGA a green light will appear if that FPGA is configured successfully. The above window shows the USB Controller connected to a DN8000K10PCIE with a single FPGA in the B position.If you have the reference design loaded and a DDR2 SODIMM installed, you can use the USB Controller to run tests of the SODIMM. From the FPGA Memory menu, select Test DDR.

7. Clear the FPGAs of their configurations. Right-click on an FPGA and select from the popup menu, "Clear FPGA". The green light above the FPGA on the GUI and on the board should stop shinning green.

8. Configure an FPGA using the USB Controller program. Right-click on an FPGA and select Configure FPGA via USB from the popup menu. The program will open a dialog box for you to select the configuration file to use for configuration. Browse to the provided user's CD
"USERCD:\\BitFiles\8000K10PCI\MainTest\LX100\fpga_a.bit"
If you are configuring an LX200 or FX60 devices you should select a bit file from the LX200 or FX60 directories instead. If you are configuring FPGA B or FPGA C, you should select fpga_b.bit or fpga_c.bit instead.

```
Done
FPGA B cleared successfully.
```

```
FPGA A cleared successfully.
Doing a sanity check...Sanity Check passed. Configuring FPGA
B via USB...please wait.
File
D:\\dn_BitFiles\DN8000K10PCIE\MainTest\LX100\fpga_b.bit
transferred.
Configured FPGA B via USB
```

Figure 12 USB Controller Log Output

9. The message box below the DN8000K10PCIE graphic should display some information about the configuration process

The USB Controller program also allows you to easily configure and transfer data to and from the user design on the emulation board. More information is provided in Chapter X, "The USB program"

4.2 Communicating to the User Design over the Serial Port

You may want to communicate with your design over the user serial port (P1). Only one FPGA can use P1 at a time. Before you can communicate to your design, change the RS232 multiplexing settings as described in Section 3.6.4. You can also change the RS232 multiplexing settings using the USB Controller software.

Connect a second RS232 cable to P1, the FPGA RS232. It is located right next to the configuration RS232 port, P2. If you have the reference design loaded, the FPGA RS232 port runs at 19200 bps, 8 bit, no parity. By default, the FPGA RS232 port is connected to FPGA A. One the computer's terminal, the reference design is programmed to digitally loopback the input to the output. If on the terminal you can read your own output, then the reference design was able to capture the RS232 signal and generate an RS232 signal that your computer could capture.

If you are familiar with previous Dini Group products, the reference design test outputs could be read from this serial port. On the DN8000K10PCIE, you must use the AETEST application to read the results of self-test.

4.3 Using AETEST to run hardware tests

AETest is the program that you can use to verify the hardware on the DN8000K10PCIE, as well as to demonstrate the reference design function. The following instructions assume you have a PC running the Windows XP operating system. The user CD includes a Windows version of the AETest program. If you plan to use the DN8000K10PCIE in stand-alone mode, connect the DN8000K10PCIE to your WindowsXP computer and use aetest_usb in D:\aetest_usb\aeusb_wdm.exe. If the computer asks for a driver, click "Have Disk" and browse to D:\AETest_sb\driver\win_wdm\dndevusb.inf

4.3.1 AETest on Linux or Solaris

To use the AETest application on Linux or Solaris, you must compile the source code included on the User CD. Instructions for compiling AETest are found in chapter 3.

4.3.2 Use AETest

The Aetest application should display it's main menu.

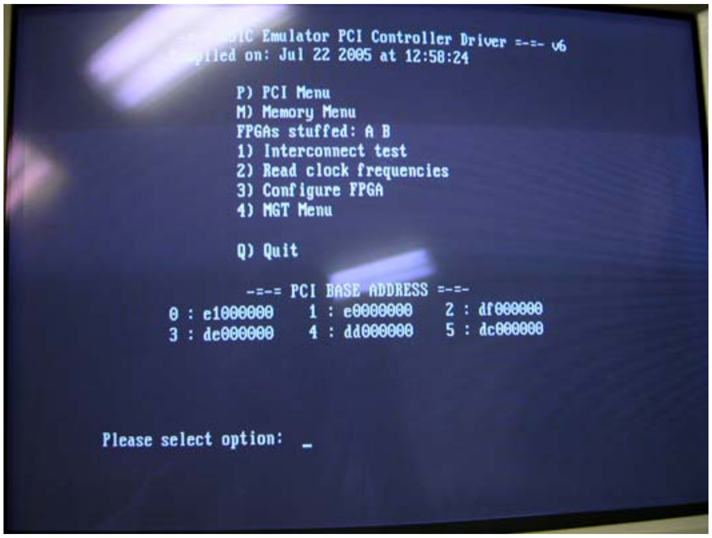


Figure 13 AETEST Main Menu

Run one of the tests. Choose option 1. Remember, the FPGA you test has to be loaded with the reference design, or the test will fail.

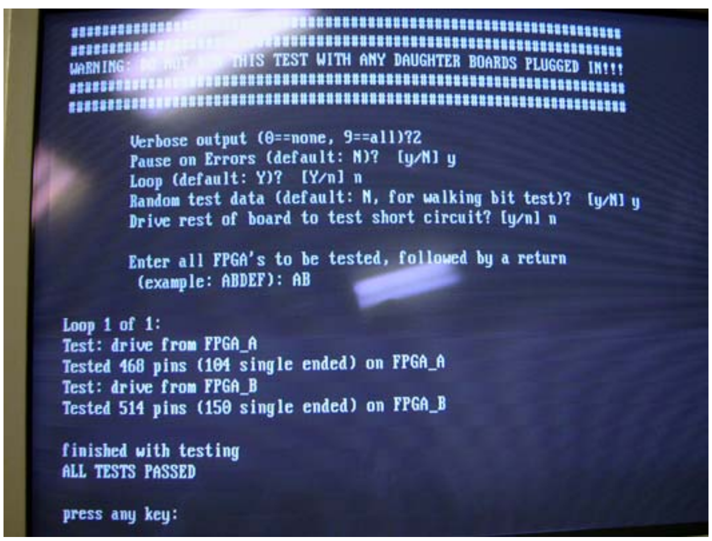


Figure 14 AETest Interconnect Menu

For more information on the AETEST program, see Chapter 3.

4.4 Moving On

Congratulations! You have just programmed the DN8000K10PCIE and learned all of the features that you must know to start your emulation project. If you are new to Xilinx FPGA, you might want move to chapter 4, introduction to ISE and Virtex 4 and start adding your Verilog code to the reference design. You will want to use Appendix X, FPGA pins to place the IOs in your design. All of the source code for the reference design in Verilog, including embedded PowerPC code and utility is included on the provided CD.

Chapter

3

Controller Software

1 USB Controller

USBController application is used to communicate with the DN8000K10PCIE.

All USBController source code is included on the CD-ROM shipped with the DN8000K10PCIE. The USBController can be installed on Windows 98/ME/2000/XP. There is a command line version called AETEST_USB that can be installed on Linux and Solaris.

The USBController Application contains the following functionality:
- Verify Configuration Status
- Configure FPGA(s) over USB
- Configure FPGAs via Smartmedia card
- Clear FPGA(s)
- Reset FPGA(s)
- Set Global clocks frequency
- Set RocketIO CLK Frequency
- Update MCU FLASH firmware

The following function interface with the Dini Group reference design.
- Read/Write to FPGA(s) – see Appendix A for address maps
- Test DDRs/FLASH/Reigsters/FPGA Interconnect

1.1 Menu Options

1.1.1 File Menu

The File Menu has the following 2 options:

a. Open – opens a file with the selected text editor (notepad by default). To change the text editor see Settings/Info Menu section

b. Exit – Closes the USBController application

1.1.2 Edit Menu

The Edit Menu performs the basic edit commands on the command log in the bottom half of the USBController window.

1.1.3 FPGA Configuration Menu

The FPGA Configuration Menu has the following options:

(1) Configure via USB (individually) – After selecting this option a window will pop and ask which FPGA you want to configure and then what bitfile you want to configure the selected FPGA with. The status of the FPGA configuration will detailed in the log window and the DN8000K10PCIE will be updated after the bitfile has been transferred.

(2) Configure via USB using file – This option allows the user to configure more than one FPGA over USB at a time. To use this option you must create a setup file that contains information on which FPGA(s) should be configured and what bitfiles should be used for each FPGA. The file should be in the following format, the first character of each line represents which FPGA you want configured (a-f or A-F), this letter should be followed by a colon and then the path to the bitfile to use for this FPGA. The path to the bitfile is realative to the directory where this setup file is, or you can use the full path. Below is an example of an accepted setup file:

A: fpga_a.bit

B: fpga_b.bit

C: fpga_c.bit

(3) Configure via SmartMedia Card – This option allows the user to use a SmartMedia card to configure the FPGAs. Please section Creating Configuration File "main.txt" for information on what files should be on the SmartMedia card to use this option.

(4) Clear All FPGAs – This option will deconfigure all FPGAs.

(5) Reset – This options sends an active low reset (active for approx. 20ns) to all FPGAs on the signal called RESET_FPGASn which is connected to the following I/O pins:

FPGA A: AK19

FPGA B: K21

FPGA C: AG18

1.1.4 Settings/Info Menu

The Settings/Info Menu has the following options

(1) Set FPGA RocketIO CLK Frequency – When the DN8000K10PCIE is first powered up the RocketIO CLK inputs to the FPGAs are inactive. The RocketIO CLK Inputs are connected to the following FPGA Differential CLK inputs on all FPGAs: F21/G21 and AT21/AU21. This menu option allows the user to specify what frequency the RocketIO CLKs should be set at for each FPGA. The supported frequency range is 31.25MHz – 700MHz. After selecting this option, a pop-up window will ask which FPGA's RocketIO Frequency you want to set (or you can choose to set all to the same frequency), and then what frequency you want. Check the log window to verify what frequency the CLKs were actually set at.

(2) Set Global clock frequencies

The clocks on the DN8000K10PCIE are automatically adjusted to the user's desired frequency by reading the setup file on the SmartMedia card. If you wish to change the frequency after power-on, or do not want to use a SmartMedia card, you can set the frequency in the USB program.

ACLK) ACLK is generated from a 25MHz crystal. Available frequencies are:

31.25	34.375	37.5	40.625	43.75	46.875	50	53.125	56.25	
59.375	62.5	65.625	68.75	71.875	75	78.125	81.25	84.375	87.5
93.75	100	106.25	112.5	118.75	125	131.25	137.5	143.75	150
156.25	162.5	168.75	175	187.5	200	212.5	225	237.5	250
262.5	275	287.5	300	312.5	325	337.5	350	375	400
425	450	475	500	525	550	575	600	625	650
675	700								

BCLK) BCLK is generated from a 14.318 Mhz crystal. Supported frequencies are:

32.22	34.01	35.80	37.58	39.37	41.16	42.95	44.74	46.53	48.32
50.11	51.90	53.69	55.48	57.27	59.06	60.85	62.64	64.43	66.22
68.01	69.80	71.59	73.38	75.17	76.96	78.75	80.54	82.33	84.12
85.91	89.49	93.07	96.65	100.2	103.8	107.4	111.0	114.5	118.1
121.7	125.3	128.9	132.4	136.0	139.6	143.2	146.8	150.3	153.9
157.5	161.1	164.7	168.2	171.8	179.0	186.1	193.3	200.5	207.6
214.8	221.9	229.1	236.2	243.4	250.6	257.7	264.9	272.0	279.2
286.4	293.5	300.7	307.8	315.0	322.2	329.3	336.5	343.6	358.0
372.3	386.6	400.9	415.2	429.5	443.9	458.2	472.5	486.8	501.1
515.4	529.8	544.1	558.4	572.7	587.0	601.4	615.7	630.0	644.3
658.6	672.9	687.3							

DCLK) DCLK is generated from a 16.0 Fundamental crystal. Supported frequencies:

32	34	36	38	40	42	44	46	48	50
52	54	56	58	60	62	64	66	68	70
72	74	76	78	80	82	84	86	88	92
96	100	104	108	112	116	120	124	128	132
136	140	144	148	152	156	160	164	168	172
176	184	192	200	208	216	224	232	240	248
256	264	272	280	288	296	304	312	320	328
336	336	344	352	368	384	400	416	432	448
464	480	496	512	528	544	560	576	592	608
624	640	656	672	688					

(3) Change Text Editor – This options allows the user to select a text editor to use (the default editor is notepad).

(4) FPGA Stuffing Information – This option will display the type of FPGAs that are stuffed on the DN8000K10PCIE.

(5) MCU Firmware Version – This option will display the MCU Firmware version in the log window.

(6) BOARD/SPARTAN Version – This option will display the Board Version along with the Spartan (Config Fpga) Version.

2 Updating the Firmware

Dini Group may release firmware bug fixes or added features to the DN8000K10PCIE. If a firmware update is released you will need to

There are two firmware files that Dini Group may release, the first is a Micro controller (MCU) software update that is stored in a flash memory. This update can be accomplished easily from within the USBController application.

The second update that may be required is a Spartan FGPA core update. The configuration data for the Spartan FPGA is contained in a Xilinx configuration PROM. This update can be accomplished with the Xilinx JTAG programming program, iMpact.

2.1 Updating the MCU (flash) firmware

To protect against accidental erasure, the MCU firmware cannot be updated unless the board is put in firmware update mode during power-on. Find Switch block 1 on the DN8000K10PCIE.

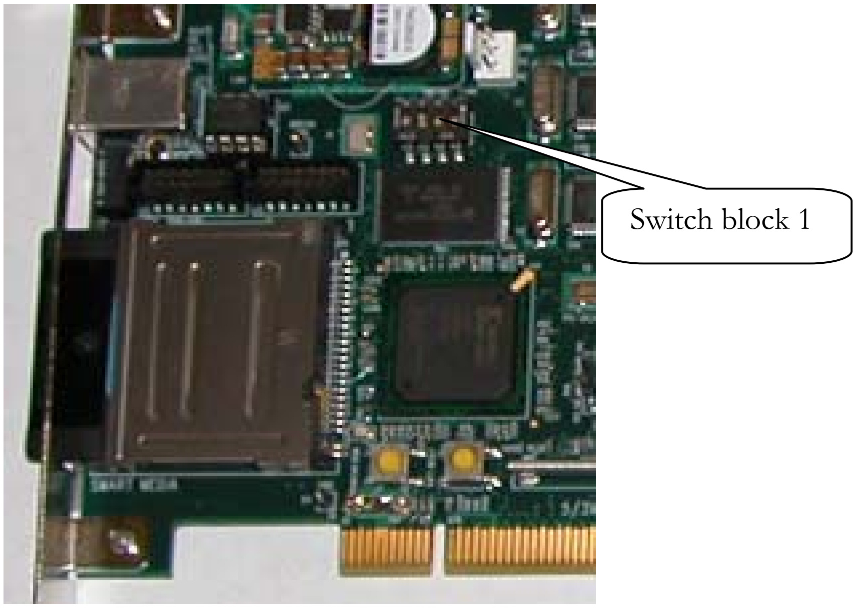


Figure 15 Switchblock 1

Move switch S1 #3 to the ON position. Power on the DN8000K10PCIE.

Open the USB Contoller program. If the DN8000K10PCIE powered on in firmware update mode, there will be an "Update Flash" button near the top of the USB Controller window. Click on this button.

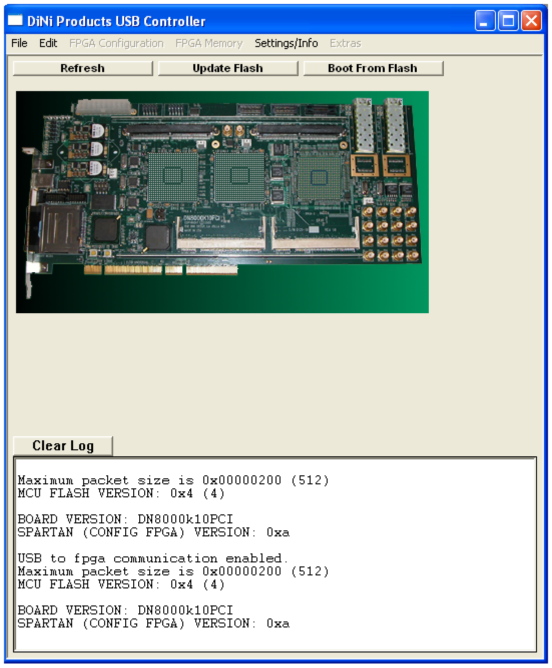


Figure 16 USB Controller Firmware Update Mode

When the Open… dialog box appears, navigate to the Firmware image file supplied by Dini Group. The file name should be "flash_flp.hex". Press OK.

The USB Controller should freeze for about 10 seconds while the firmware update is taking place. When the download is complete, the Log window should print, "Update Complete"

Move Switchblock 1 # 3 to the OFF position to put the DN8000K10PCIE back into normal operation mode. Power cycle the board.

2.2 Updating the Spartan (EEPROM) firmware

Connect a Xilinx Parallel IV configuration cable to the parallel port of your computer. The Parallel IV cable requires external power to operate, so you may need to connect the keyboard connector power adapter. When the Parallel IV cable has power, the status LED on Parallel IV turns amber.

Use a 2mm IDC cable to connect the Parallel IV cable to the DN8000K10PCIE connector J14.

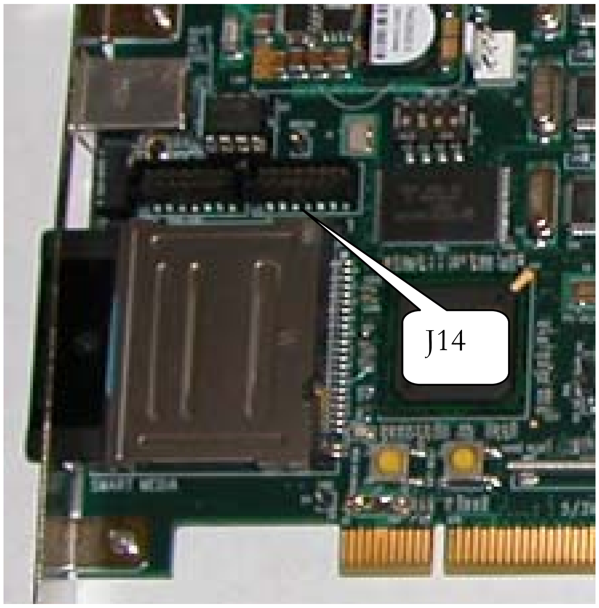


Figure 17 Firmware Update Header

Power on the DN8000K10PCIE. When the Parallel IV cable is connected to a header, the status light turns green.

Open the Xilinx program Impact, usually found at Start->programs->Xilinx ISE 7.1->Accessories->impact

Impact may ask you to open an impact project. Hit cancel.

Choose the menu option File->Initialize Chain

Impact should detect 2 devices in the JTAG chain. Xc18v02 and Xc2s200. For each item in the chain Impact will direct you to select a programming file for each. For the xc18v02 device, select the Spartan Firmware update file provided by Dini Group. This file should be named prom.mcs. Hit Open. Impact will then ask for a programming file to program the xc2s200. Press Bypass.

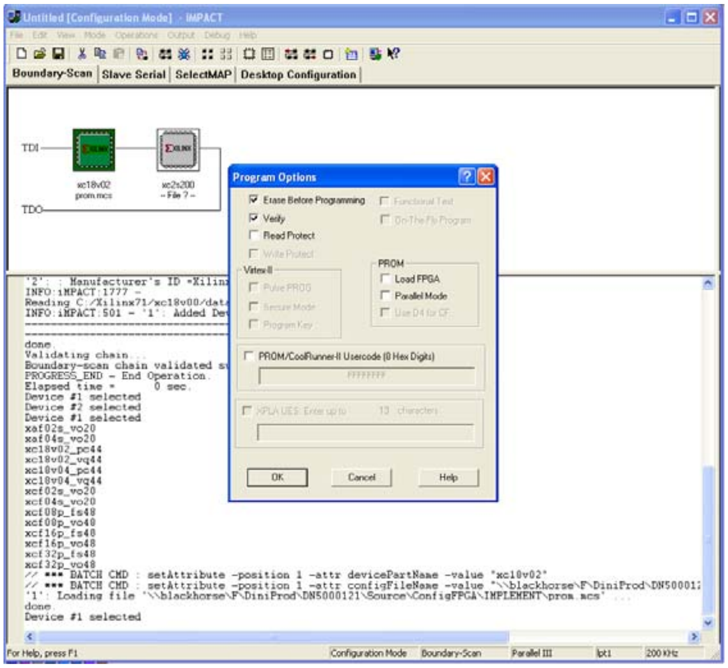


Figure 18 Impact Window

To program the prom. Right-click on the prom and select Program… from the popup menu. In the options dialog that follows, the options "Erase before programming" should be selected, and "Verify" should be deselected. Press OK. The programming process takes about 35 seconds over the parallel port.

Power cycle the DN8000K10PCIE. The new firmware is now loaded. You can close impact and disconnect the Parallel IV cable.

Chapter 5

Hardware

3 Overview

The DN8000K10PCIE was designed to maximize the number of useful gates in your emulation project running at speed by providing the densest interconnect possible. To achieve this goal, the DN8000K10PCIE is equipped with the highest-capacity FPGAs available today, the Xilinx Virtex 4 LX200. The FPGAs on the DN8000K10PCIE are in the largest, 1513-ball package to give the user extremely high IO count, for high bandwidth and low-latency interconnect between FPGAs. Three hundred eighty nine differential links between FPGAs A and B allow for as much as 189 Gb/s communication between the two FPGAs.

In order to support enough bandwidth to deliver real time data to your design at speed, the DN8000K10PCIE is equipped with an optional Xilinx Virtex 4 FX100 with RocketIO Multi-Gigabit Tranceivers. Serial connections over Fibre, Coax ribbon cable, and Coax SMA cables allow for a total aggregate 150 Gb/s off-board communication.

To allow you to connect the FPGA to the resources that will be on your end product, the DN8000K10PCIE also has highspeed expansion capabilities.

Below is a block diagram of the DN8000K10PCIE

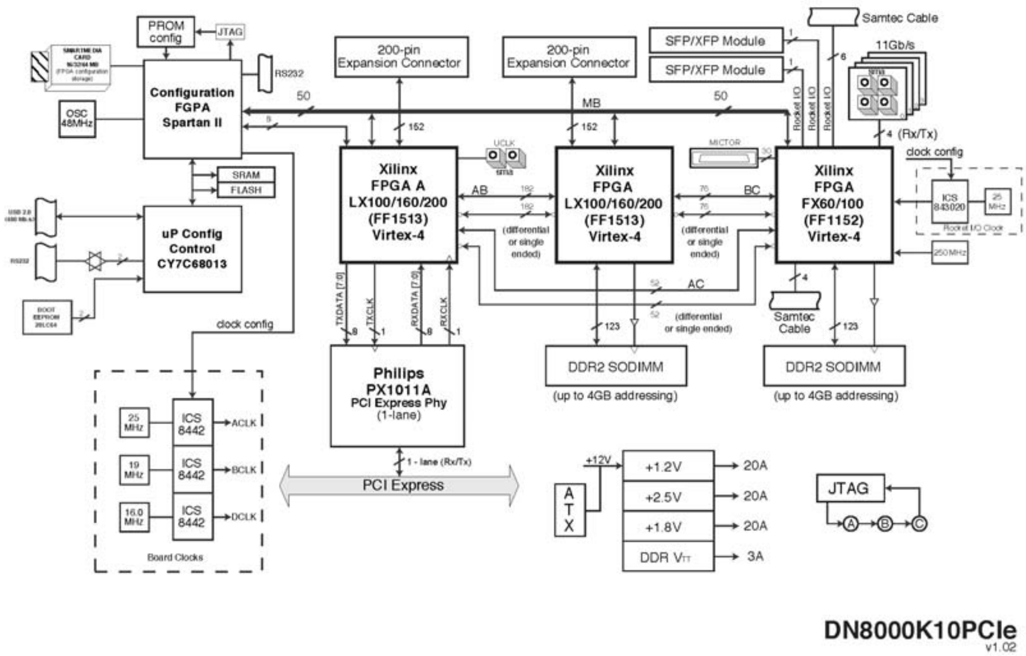


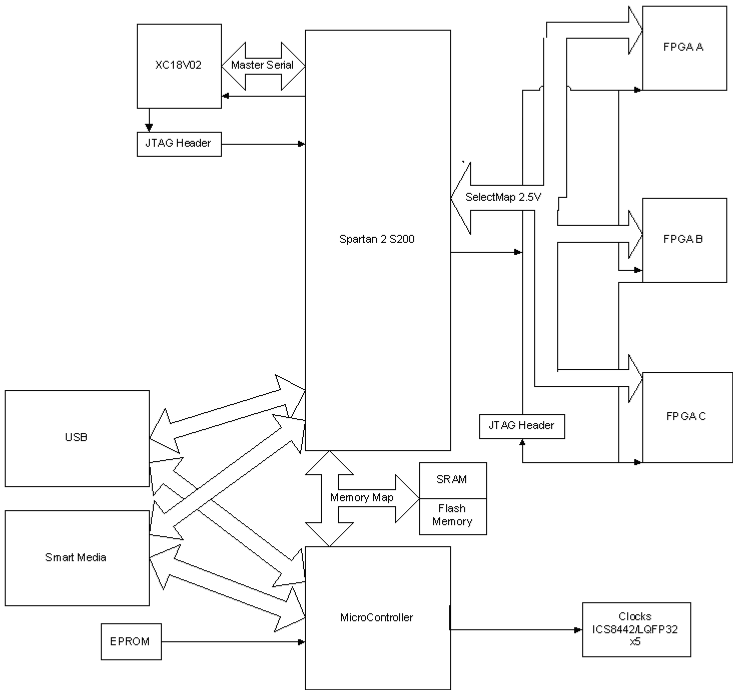
Figure 19 DN8000K10PCIE Block Diagram

The following sections describe in detail each circuit on the DN8000K10PCIE. Note that Schematics appearing in this section are illustrative and may have had details omitted or have been modified for clarity and brevity. If you need to probe, modify or design around the DN8000K10PCIE you will need to examine the complete schematics. See *Appendix Schematics*. An assembly drawing has also been provided to help you find probe points on the DN8000K10PCIE. See *Appendix Assembly*.

4 Configuration Circuit

4.1 Overview

The goal of the configuration circuit on the DN8000K10PCIE is to allow the user to configure his FPGAs using any host interface. The configuration system on the DN8000K10PCIE allows configuration over PCI, USB, JTAG, or automatic configuration from a SmartMedia card.



The circuit is designed to provide an easy configuration solution that will work out-of-the-box for most users. For special configuration requirements, the configuration circuitry is programmable. The verilog code for the configureation FPGA and the C code for the microcontroller are both provided on the reference CD. The C code for the USB Windows GUI controller program are also included on the User CD.

4.2 The Spartan 2 FPGA

The configuration circuitry of the DN8000K10PCIE is built around a Xilinx Spartan II Fpga. The SelectMap interface of the user FPGAs is connected directly to the general purpose IOs of the Spartan 2, allowing the maximum flexibility of configuration. The Spartan 2 also shares connectivity with the three user FPGAs over a 40-bit Main bus, allowing fast transfers from a computer to the user design over USB. The Spartan 2 FPGA also provides IO expansion for the Cypress Microcontroller. The Spartan II FPGA comes preloaded with a core that provides a way to program the Virtex 4 FPGAs over PCI, USB and SmartMedia.

The Spartan FPGA is connected to the Cypress microcontroller's address and data busses, and the control registers within the Spartan II FPGA that control FPGA configuration are memory-mapped into the MCU's address space.

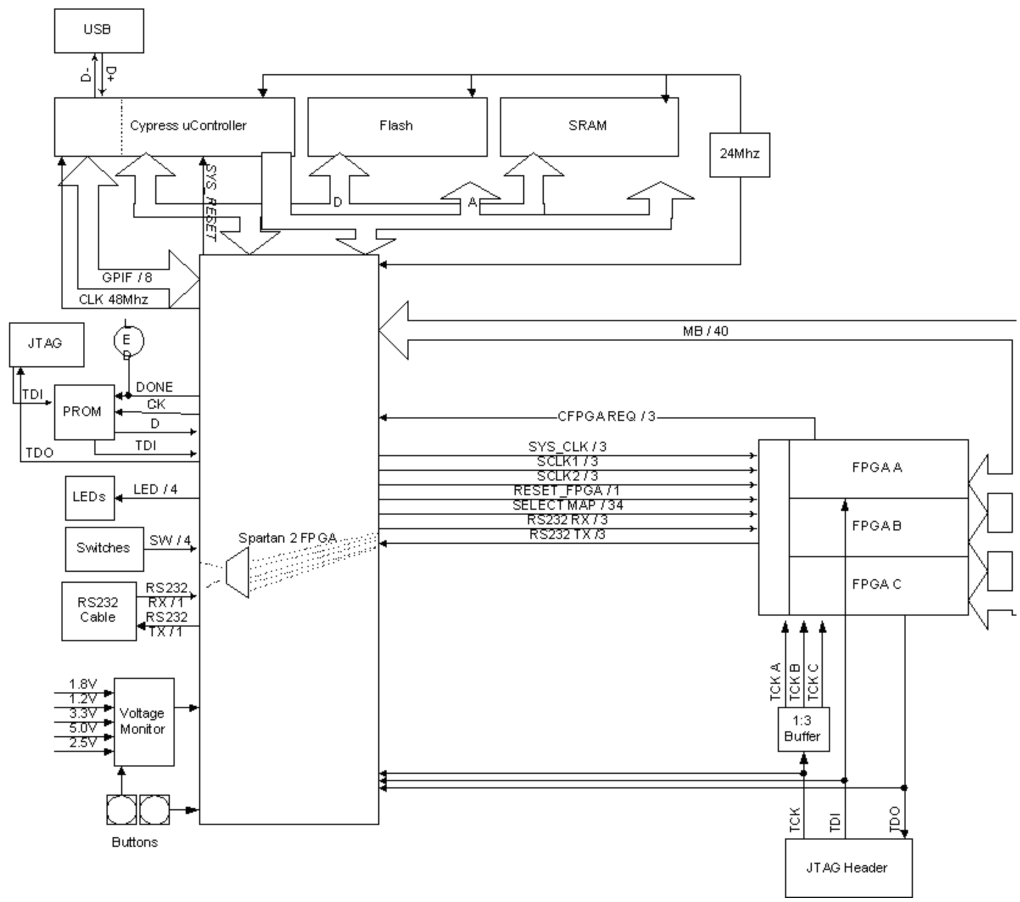


Figure 20 Spartan II IO Connections

4.2.1 Spartan Configuration

The Spartan 2 FPGA is configured from a Xilinx serial prom. The Spartan's configuration mode is hard-wired into Master Serial mode. After power up, the Spartan automatically clocks an external PROM, U41, which programs the FPGA over the serial configuration data pin DIN.

A green LED, DS24, lights when the DONE pin is high. This signal is driven by the Spartan 2 FPGA when it is configured and running.

Both the Spartan and the serial prom are connected in a JTAG chain attached to J14. This header is used when performing firmware updates to update the PROM.

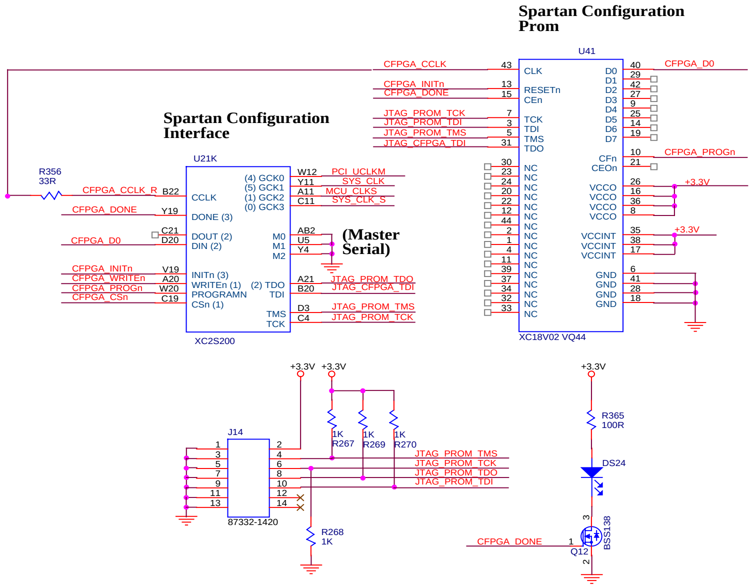


Figure 21 Spartan II Configuration

As soon as the Spartan II FPGA is configured, it resets the Cypress microcontroller. Pull-downs on the PROG pin of FPGAs A B and C ensure that the FPGAs cannot be active unless the Spartan II is successfully configured.

4.2.2 Smart Media

The Smart Media card interface is connected to the IOs of the Spartan 2 FPGA.

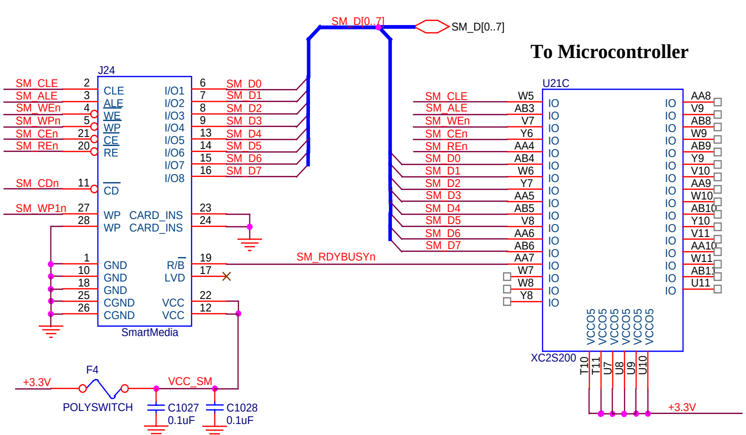


Figure 22 Smart Media interface

The Smart Media data bus, D[0-7], also connects to the microcontroller. Currently the MCU connection is not used. The Microcontroller is able to read from the Smart Media interface by accessing the Spartan's memory-mapped data over the MCU memory interface for the purposes of reading instructions from SmartMedia cards.

For instructions on creating a Smart Media card for configuring the DN8000K10PCIE, see the section *Configuration Options: Smart Media.*

4.2.3 MCU communication

The MCU communicates to the Spartan 2 FPGA over it's external memory interface, pins D0:7 and A0:15. The Spartan 2 is assigned the address range 0xDF00 to 0xDFFF in the Microcontrollers memory space.

The 480Mbs data rate of USB 2.0 is too fast for the microcontroller to control, so the MCU's hardware passes USB bulk transfer data to the MCU GPIF interface. These signals, SM[0-7] and GPIF_CTL, GPIF_RDY, connect to the Spartan FPGA. The SM[0-7] signals also connect to the SmartMedia card socket, although the MCU does not communicate with the SmartMedia interface directly. The MCU_IFCLK signal provides a clock for this interface. The signal is driven from the Spartan 2 FPGA.

4.2.4 RS232

The DN8000K10PCIE has two RS232 headers. One (P2) is used by the microcontoller unit to provide configuration feedback and control. The other (P1) is connected to the Spartan 2 FPGA. The Spartan 2 FPGA has one RX and one TX signal connected to each Virtex 4 FPGA. The Spartan FPGA will multiplex the RX and TX signals to the Virtex FPGAs to the RS232 header P1. The Spartan 2 internally multiplexes the signals on the user RS232 header P1, to one of these three sets of signals. To change the Virtex 4 FPGA that has access to the RS232 headers, you can use the provided USB application program, or you can change the setting on a terminal connected to the Microcontroller unit's RS232 port (P2).

Since RS232 uses a 12V signal levels, the RS232 signals from the SpartanII are first buffered through a voltage translation buffer shown below.

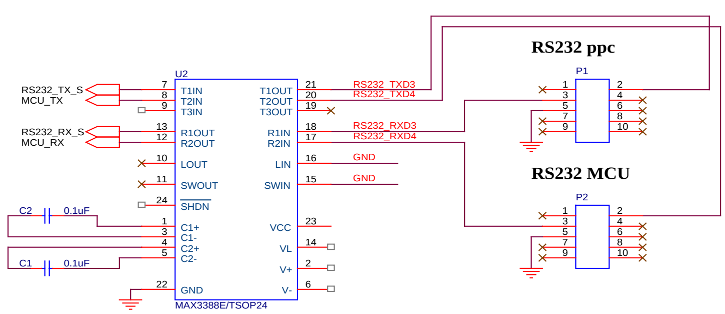


Figure 23 RS232 buffer

On the back side of the DN8000K10PCIE, there are two duplicate RS232 ports (P7 and P8) that can be used if an installed daughter card is covering the headers on the front. These duplicate headers are not installed by default, but can be installed on request. They are compatible with a surface mount, 5x2 0.1" header.

4.2.5 IIC

There is a single IIC bus on the DN8000K10PCIE connecting all IIC enabled chips on the board. On this bus are three MAX1617A temperature sensing chips (U3, U4, U24), two DDR2 SODIMM sockets, and a serial eprom. The temperature sensors on the IIC bus are polled about once per second by the MCU to read the temperature of each FPGA.

4.3 Configuration Options

The DN8000K10PCIE allows FPGA configuration from any of four methods.

When a Virtex 4 FPGA is configured, the DONE pin on the FPGA is pulled high. The DN8000K10PCIE has a green LED attached to the DONE signal of each to indicate the state of the DONE pin on the three Virtex 4 FPGAs and on the SpartanII configuration FPGA.

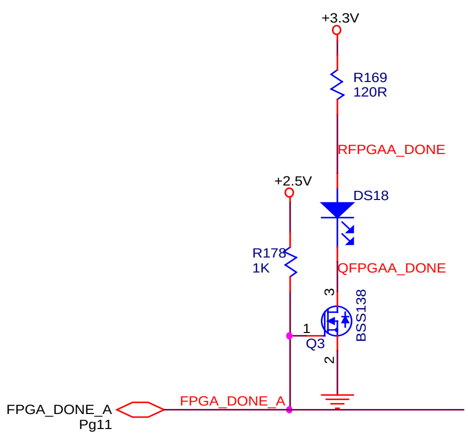


Figure 24 DONE LEDs

4.3.1 Jtag

Jtag is the only configuration method on the DN8000K10PCIE that does not use the Virtex 4 SelectMap configuration interface. When programming the user FPGAs over a JTAG cable plugged into J13, the DN8000K10PCIE configuration circuitry is not used.

A JTAG connection is required to use some Xilinx configuration tools like ChipScope, and readback from Impact. Also, this header can be used with Synplicity's Identify. Configuration over JTAG is slower than SelectMap. You can still use the SmartMedia or USB interfaces to control clock settings if you plan to configure through JTAG.

To configure using JTAG, we recommend using Xilinx Parallel cable IV, or Xilinx platform USB cable. The Xilinx program. You should set the configuration speed of your JTAG cable to 4Mhz or below.

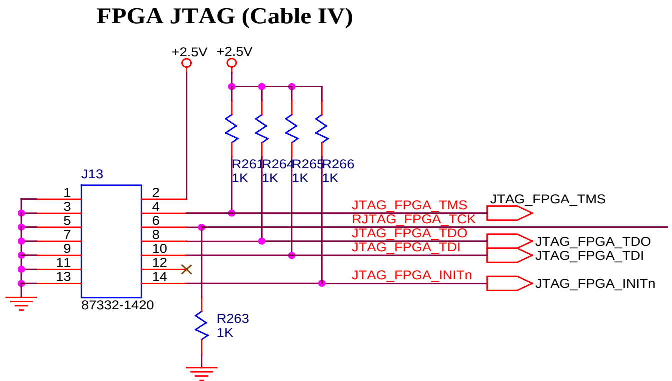


Figure 25 FPGA JTAG Header

The JTAG signals TMS is bussed to all three Virtex 4 FPGAs. TDO connects to FPGA A, the TDO of FPGA is connected to TDI of FPGA B, the TDO of FPGA B connects to the TDI of FPGA C and TDO of FPGA C is connected to the TDI of J13. TCK is buffered and passed to each FPGA in a point-to-point fassion.

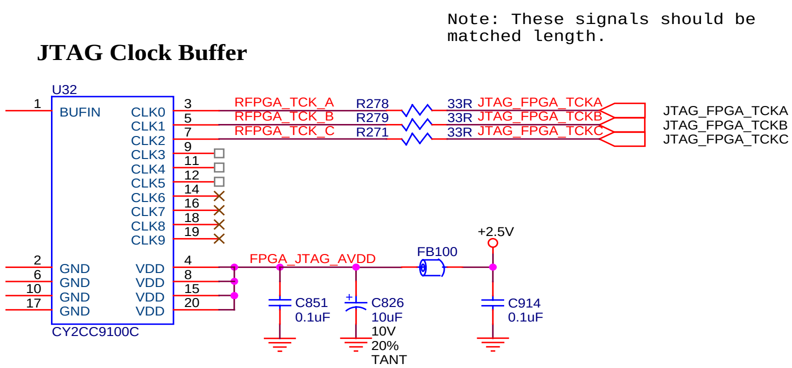


Figure 26 TCK buffer

The INITn signal is not used.

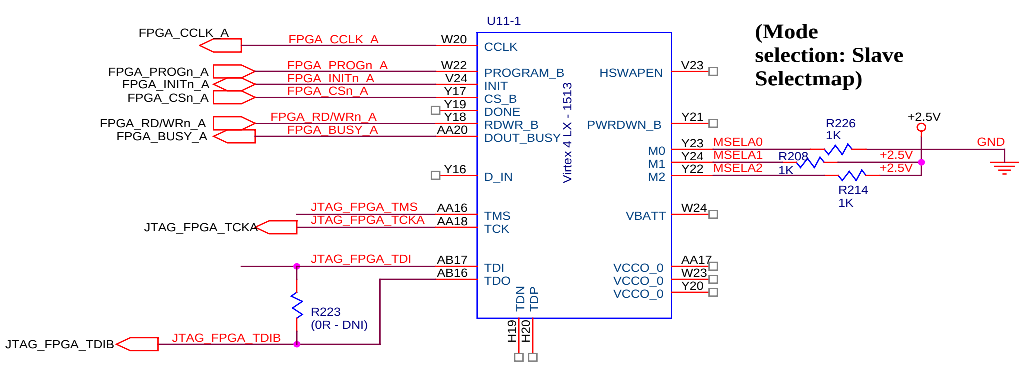


Figure 27 FPGA A Configuration Bank

If you ordered your DN8000K10PCIE with one or more FPGAs not installed (Option FPGA A NONE, FPGA B NONE, or FPGA C NONE) then a bypass resistor is installed connecting the TDI pin to the TDO pin of the uninstalled FPGA. This is so the JTAG chain will remain intact when FPGAs are missing.

4.3.2 SmartMedia

When the DN8000K10PCIE powers on, the microcontroller reads the contents of any SmartMedia card that is in the SmartMedia slot. The microcontroller by default opens a file on the root directoy named "Main.txt" if it exists. This file contains instructions for the configuration circuitry to configure the Virtex 4 FPGAs.

To create a SmartMedia card to control the DN8000K10PCIE configuration, insert the SmartMedia card into a card reader (provided) and connect it to a PC. Create a file on the root directory of the card and call it "Main.txt"

In main.txt, write a series of configuration commands, separated each by a new line. A valid command is one of the following:

```
// <comment>
FPGA A:<filename>
FPGA B:<filename>
FPGA C:<filename>
CLOCK FREQUENCY: <clockname> N <number> M <number>
SANITY CHECK: <yn>
VERBOSE LEVEL: <level>
RS232: <portnumer> <fpganame>
CONFIG REG 0x<SHORTADDR> 0x<BYTE>
MAIN BUS 0x<WORDADDR> 0x<WORDDATA>
```

<comment> can be any string of characters except for newline.
<filename> can be the name of a file on the root directory of the SmartMedia Card.
<number> can be any one or two digit positive integer in decimal
<clockname> can be [A,B,D,2] A is ACLK, B is BCLK, D is DCLK and 2 is the RocketIO clock synthesizer.
<yn> can be the letter y or the letter n
<level> can be 0,1,2 or 3
<portnumber> can be 1,2,3, or 4. The DN8000K10PCIe only has 1 user RS232 port (1) so 2-4 will cause no operation.
<fpganame> can be [A,B,C,D,E,F,G,H,I]. The DN8000K10PCIE only has 3 fpgas (A,B,C), so D-I will cause the RS232 port to not function.
<SHORTADDR> is a 2-digit hex number (16 bits)

<BYTE> is a 1-digit hex number (8 bits)
<WORDADDR> 4-digit (32 bit) hex number representing a main bus address
<WORDDATA> 4-digit (32 bit) hex number containing data for a main bus transaction

The following table describes the function of each of the available main.txt commands.

Instruction	Function
// <comment>	The MCU performs no operation and moves to the next command.
VERBOSE LEVEL: <level>	This command will set the amount of output the MCU will produce over the RS232 port during configuration. When level is set to 0, the MCU will produce only error output. Before this command is executed, the level is set to the default value 3.
FPGA A:<filename>	The Virtex 4 FPGA "A" will be configured with the file named by <filename>
FPGA B:<filename>	The Virtex 4 FPGA "B" will be configured with the file named by <filename>
FPGA C:<filename>	The Virtex 4 FPGA "C" will be configured with the file named by <filename>
SANITY CHECK: <yn>	If <yn> is set to y, then the MCU will examine the headers in the .bit files on the SmartMedia card before using them to configure each FPGA. If the target FPGA annotated in the .bit file header is not the same type as the FPGA the MCU detects on the board, it will reject the file and flash the error LED. Before this command is executed, <yn> is set to the default value y. If you want to encrypt of compress your bit files, you will need to set <yn> to n. Encrypting bit files is not supported or recommended by Dini Group. Previous revisions of Xilinx parts have been vulnerable to permanent damage caused by bugs in the encryption circuitry.
MAIN BUS 0x<WORDADDR> 0x<WORDDATA>	Writes data in <WORDDATA> to the address on the main bus interface at <WORDADDR>. This command only makes sense in the context of the Dini Group reference design, unless your design implements a compatible controller on the main bus pins. See *Appendix Pins Other*. The Specification for this interface is in the *Referece Design* Chapter.
CONFIG REG 0x<SHORTADDR> 0x<BYTE>	Writes to an address in the MCU XDATA memory space.
RS232: <port> <fpga>	The RS232 port (P1) will be controlled by the FPGA <fpga> if <port> is 1
CLOCK FREQUENCY: <clockname> N <number> M <number>	The MCU will adjust the clock synthesizer producing clock <clockname> to multiply it's reference frequency by <M> and divide it by <N> Note that the clock synthesizers have a limited bandwidth, and for clocks A B and D, the reference frequency * M must fall in the range 250Mhz-700Mhz. For clock 2 (RocketIO), reference * M must fall between 540 and 680Mhz. See datasheets for parts ICS8442AY and ICS843020-01 The reference frequencies are ACLK 25Mhz BCLK 14.18Mhz DCLK 16Mhz 2CLK 25Mhz

Figure 28 Main.txt Commands

An example main.txt file:

```
VERBOSE LEVEL:0
// This will prevent the MCU output over RS232 to speed up configuration
FPGA A:a.bit
//this will load the configuration a.bit into FPGA A
CLOCK FREQUENCY: A N 4 M 10
// This will cause Aclk frequency to be
// 25*10=250 / 4 = 62.5Mhz
MAIN BUS: 0x0000 0x0001
//Writes to a register in FPGA A.
```

Even if you are not planning to configure your Virtex 4 FPGAs using a SmartMedia card, you may want to leave a SmartMedia card in the socket to automatically program your global and rocketIO clock. (Clocks may also be programmed using the provided USB application, or over the MCU RS232 terminal.)

4.3.3 USB

The USB interface on the DN8000K10PCIE is provided by the Cypress microcontroller unit. The Cypress microcontroller is programmed to interrupt when it receives a USB vendor request.

When the MCU receives over USB a Bulk Transfer type request, it does not interrupt. The raw data contained in the bulk transfer is driven out on the GPIF pins of the MCU (the SM[0-7] signals) to the Spartan 2. The data is clocked out using the MCU_IFCLK clock signal to the Spartan 2. As long as the signal GPIF_CTL is held high by the MCU, the Spartan 2 clocks MCU_IFCLK to receive the USB data.

When data is written to the Spartan 2 from a bulk transfer over the MCU's GPIF interface, the Spartan 2 either writes that data onto the SelectMap interface of the Vitex4 FPGAs, or onto the Main bus using the Main Bus interface described in the *Reference Design* chapter.

The control register FPGA_SELECT within the Spartan 2 determine to which interface this data is routed to.

4.4 FPGA configuration Process

For information regarding the JTAG interface and configuration, See Xilinx publication UG071, Virtex 4 configuration guide.

When configuring over USB or SmartMedia, the FPGAs are configured over the Virtex 4 SelectMap bus.

All SelectMap signals are connected directly to the Spartan2 FPGA. The SelectMap signals are:

D[0-7] SelectMap data signals.

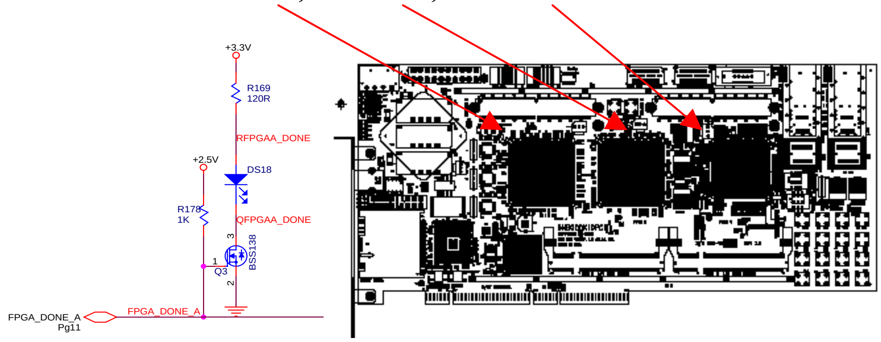
PROGRAM_B	Active low asynchronous reset to the configuration logic. This will cause the FPGA to become unconfigured. The documentation refers to this signal as PROGn
DONE	After the FPGA is configured, it is driven high by the FPGA.
INIT	Low indicates that the FPGA configuration memory is cleared. After configuration, this could indicate and error.
RDWR_B	Active low write enable. The Documentation refers to this signal as RDWR
BUSY	When busy is high, the SelectMap configuration stream must stop until BUSY goes low.
CS_B	SelectMap chip select. The documentation refers to this signal as CSn
CCLK	Signals D[0:7], DONE, RDWR_B and CS_B are clocked on CCLK

Each Virtex 4 FPGA has a complete set of SelectMap signals connected point-to-point to the Spartan 2, except for FPGA B and C, who share signals D[0-7]. All signals are 2.5V CMOS signals except for D[0-7] of FPGA A (Signals SELECTMAP_3V_D[0-7]), which are 3.3V CMOS.

All commands required to configure a Virtex 4 FPGA are created and embedded in the .bit files created by the Xilinx Bitgen program. The DN8000K10PCIE does not interact with the SelectMap interface other than to reset the FPGA using the PROGn-INTn-PROGn resetr sequence described in UG071, and to copy a bit stream file unaltered to the FPGA over the data pins D[7-0]. Select map commands can be issued to the Virtex 4 FPGA from the host using the same interface used to configure and FPGA.

After a Virtex 4 FPGA is configured, it asserts the signal DONE. On the DN8000K10PCIE, these signals have an LED attached to each DONE signal placed near the upper corner of each FPGA.

FPGA A's LED is DS18, B is DS14, C is DS16



If your Virtex 4 FPGA design is failing to produce the intended (or any) results, you should check the DONE light above the FPGA to make sure it is configured correctly. The design files created by Xilinx bitgen software contain a CRC check, so if the Virtex 4 FPGA detects a CRC failure, there was a trasmission error during configuration and the DONE light will not glow. The DN8000K10PCIE microcontroller also checks the design files you send to make sure they are compiled for the FPGAs that are installed on your board. If they are not, then the microcontroller unit halts the configuration process. As a result, when the DONE light goes on, you will know that the configuration process was successful.

4.5 MCU

The operation of the Spartan II is monitored and controlled by a Cypress CY7C68013 microcontroller. The microcontroller also has a USB 2.0 interface that can be used to monitor the board, control configuration, or transfer data to and from the user FPGA design. Basic operation can be controlled over an RS232 link from a computer terminal.

4.5.1 RS232

The primary method of user interaction with the DN8000K10PCIE configuration circuitry is the MCU's RS232 port (P2). The Cypress CY7C68013 has two RS232 pins that are buffered through a 12V voltage translation buffer for use with a standard computer serial port.

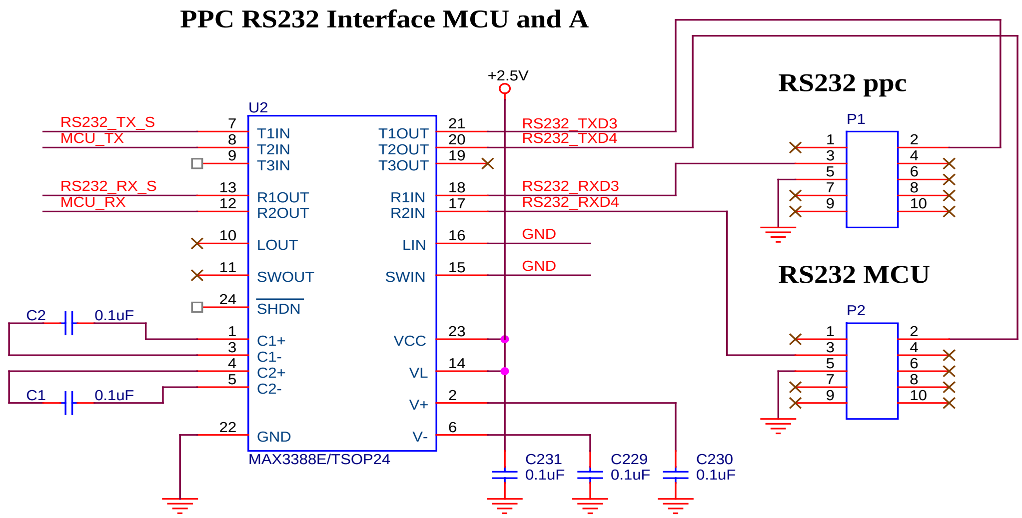


Figure 29 RS232 Buffer and Headers

The RS232 port will be able to communicate with a standard PC serial port set to 19200 baud, 8 data bits, no parity, no handshaking. When you connect a computer terminal to the port and power on the DN8000K10PCIE, the firmware loaded on the microcontroller unit will display a menu on the terminal. This menu will allow you to control the basic configuration options of the DN8000K10PCIE including configuration, clock frequencies, and the Virtex 4 FPGA RS232 ports.

4.5.2 Clocks

The Cypress CY7C68013 is also responsible for configuring the global clocks and RocketIO clock of the DN8000K10PCIE. The Cypress CY7C68013 MCU reads the file "main.txt" from the SmartMedia card in the socket (J24), and follows the users clock configuration commands.

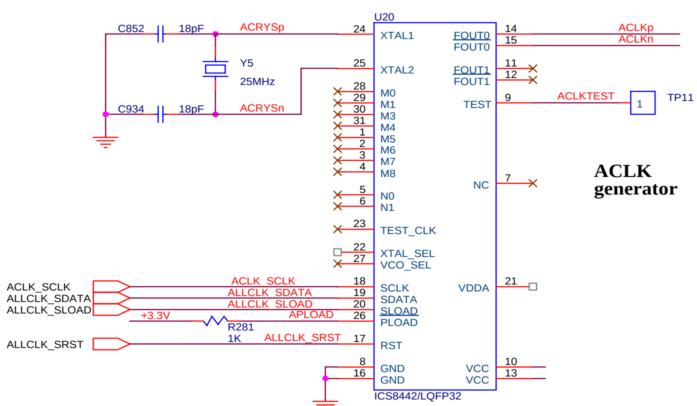


Figure 30 8442 Clock synthesizer

The 3 ICS8442 clock synthesizers on the DN8000K10PCIE used for generating the global clocks, ACLK, BCLK and DCLK, share a serial configuration bus connected to the MCU to program them. The ICS8442 frequency synthesizers are capable of multiplying and dividing the reference frequencies provided by their reference crystals. The MCU loads the user's desired multiplication "M" value, and division, "N" value into the settings registers in the ICS8442 chip.

4.5.3 LEDs

The MCU is connected to 4 red LEDs that are visible from outside the PC case when the DN8000K10PCIE is plugged into a PCI slot. The LEDs flash a status code during and after configuration.

All four flashing LEDs means there has been an error configuring at least one FPGA.

4.5.4 Memory space

The XDATA memory space of the MCU is partitioned into four sections.

0x0000 - 0x1FFF	internal data/program memory
0x2000 - 0xCFFF	external SRAM
0xDFF0 - 0xDFFF	memory mapped registers (no external memory accesses)
0xE000 - 0xFFFF	reserved by MCU, RD/WR strobes not active in this region

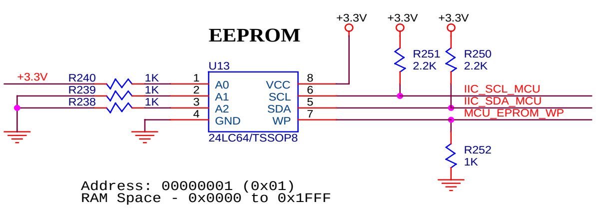
The internal data memory region is mapped to an internal SRAM in the Cypress MCU. When the microcontroller code calls memory access from this region, the external Address and Data busses are not used. After power on reset, the MCU reads from the IIC Eprom connected to the MCU_EPROM signals and fills this internal memory before allowing the PC to run. The code in this section of memory contains core functions of the Dini Group firmware, like setting up the interrupt registers, communicating with USB, and allowing firmware updates.

The external SRAM is used for heap data.

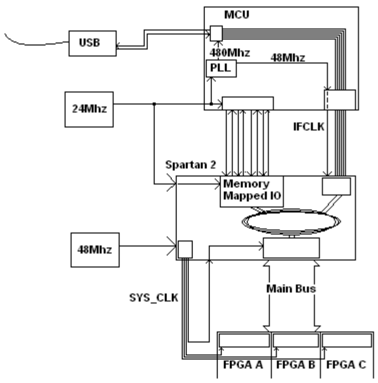
The memory mapped register region (The DF region) contains registers in the Spartan 2 FPGA that control FPGA configuration.

The program memory space of the MCU is directly mapped to the external Flash memory.

When the Cypress MCU is reset (which happens after the Spartan 2 is configured), it loads its boot code into its 8kB of internal memory from a serial EEProm (U13). The code in the EPROM instructs the MCU to execute code located on the FLASH memory (U19). The code in the EEPROM and FLASH is located on the user CD.

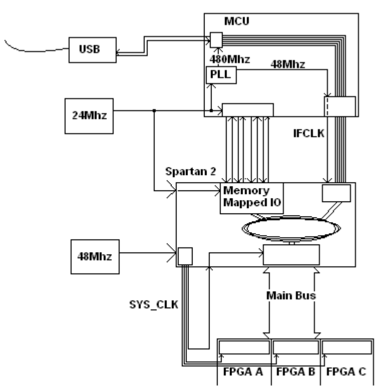


Communication over the MCU memory bus to the Spartan 2 is synchronized to the 24Mhz MCU_CLK (X3). For information regarding the timing of transactions on this bus, see the Cypress CY7C68013 user manual.



The Configuration FPGA is connected to the MCU_DATA[7:0] signals, the MCU_ADDR[15:0] signals and the MEM_OE signal, allowing it to decode address accesses of the MCU. The Configuration FPGA is programmed to respond to accesses in the XDATA address space in the address range of 0xDF00 to 0xDFFF

Communication over the MCU memory bus to the Config FPGA is synchronized to the 24Mhz MCU_CLK (X3). For information regarding the timing of transactions on this bus, see the Cypress CY7C68013 user manual.



The following registers implemented in the Configuration FPGA are accessible as part of the MCU's XDATA address space.

Register Name	**XDATA Address**	**Description**
DATA	DF00	Used when reading from SM but not configuring
COMMAND	DF01	Commands for the SM

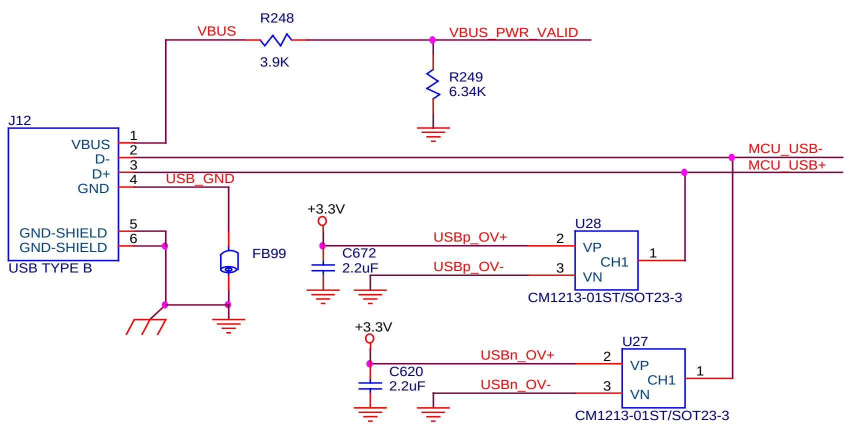
ROW_LADDR	DF02	Holds lower 8-bits of SM address
ROW_HADDR	DF03	Holds upper 8-bits of SM address
ROW_XADDR	DF04	Holds extra bits of SM address
NUM_BYTES_0	DF05	Holds lower 8-bits of the number of bytes to read
NUM_BYTES_1	DF06	Holds upper bits of number of bytes to read in
BITS_1	DF07	BIT7: mcu_fpga_config_rd BIT6:
BITS_2	DF08	BIT4: FPGA_DONE BIT3 CPLD_idle BIT2:
SM_SIGNALS	DF09	
MCU_XADDR	DF0A	Address register for upper FLASH/SRAM bits
MCU_CNTL	DF0B	Address register for upper FLASH/SRAM bits
FPGA_SELECT	DF0C	FPGA_select[5:0] = bits 5:0
PPC_RS232_ABSELECT	DF0D	
PPC_RS232_CDSELECT	DF0E	
FPGA_CNTRL	DF0F	bits[1:0] = 01 (write address), 10 (data write), 11
FPGA_BE	DF10	select byte in addr, read, and data bytes
FPGA_RD_DATA	DF11	
FPGA_WR_DATA	DF12	
FPGA_ADDR	DF13	
FPGA_ERROR	DF14	
GPIF_DATA	DF20	
GPIF_ERROR	DF21	
HOLD_DONES	DF22	
STATES	DF23	[7:4] = GPIF_STATE, [3:0] = FPGA_STATE
FPGA_FREQ_H	DF24	
FPGA_FREQ_SEL	DF25	
FPGA_FREQ_L	DF26	
MCU_STUFFING1	DF27	
MCU_STUFFING2	DF28	
SERIAL_CLK_CTRL_0	DF29	
SERIAL_CLK_CTRL_1	DF30	
MB80_1_CTRL0	DF36	
MB80_1_CTRL1	DF37	
MB80_2_CTRL0	DF38	
FPGA_COMMUNICATION	DF39	
MB80_2_CTRL1	DF40	
MB64_1_CTRL	DF41	
MB64_2_CTRL	DF42	
MB64_3_CTRL	DF43	
CPLD_CS_N_CTRL	DF44	
CPLD_DATA	DF45	
CPLD_ADDR	DF46	
GCLK_MSEL_CTRL	DF47	

FPGA_PH0_DVAL	DF48	
FPGA_PH1_DVAL	DF49	
FPGA_PH2_DVAL	DF50	
CF_REG_OFFSET	DFE	
NEW_CONFIG_VERSION	DFFD	
NEW_BOARD_VERSION	DFFE	
OLD_BOARD_VERSION	DFFF	

These registers can be written to from the USB interface. See *USB Software: Programmers Guide.*

4.5.5 USB

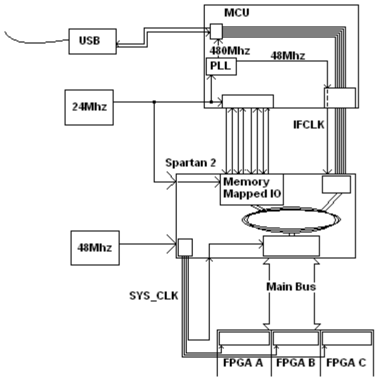
The Cypress CY7C68013 has a built-in USB 2.0 interface. The USB type B connector on the DN8000K10PCIE (J12) is connected directly to the USB pins on the Cypress MCU.



USB Transient Protection

The USB protocol is completed by the Cypress CPU.

The Cypress receives a 24Mhz clock from an oscillator (X3). The Cypress internally multiplies this clock to 480Mhz for USB 2.0 and 48Mhz for GPIF operation. The core runs at 24Mhz along with the external memory interface. Communication over this external memory interface is clocked using the MCU_IFCLK signal driven from the MCU at 48Mhz. (The Spartan communicates over main bus with the Virtex 4 FPGAs using a separate 48Mhz oscillator (X1) and distributes this clock to each FPGA including itself)



4.5.6 Smart media

The SmartMedia card socket pins are bussed among the Cypress MCU GPIF pins, the Spartan 2 FPGA IOs, and the SmartMedia card socket. After reset, the MCU uses this connection to look for and read the contents of the file main.txt on the SmartMedia card. The main.txt file contains instructions for configuring the user design into the three Virtex 4 FPGAs.

After reading the configuration instructions, the MCU reads the headers of the user's FPGA design (".bit") files and verifies that they target the correct type of FPGA that are installed on your DN8000K10PCIE. This will prevent damage to the FPGA from an incorrect or corrupt .bit file. This behavior can be turned off.

If this check is passed, MCU uses its memory mapped interface with the SpartanII to instruct the SpartanII to read the SmartMedia card and configure the Virtex 4 FPGAs over SelectMap bus.

5 Clocking

The clocking circuitry on the DN8000K10PCIE is designed for high-speed operation. The flexible clock design should meet the most difficult clocking needs, allowing 8 totally asynchronous, controllable clock sources for each FPGA.

All clocks operating above 100Mhz are fully differential, LVDS signaled, low skew, low jitter clocks.

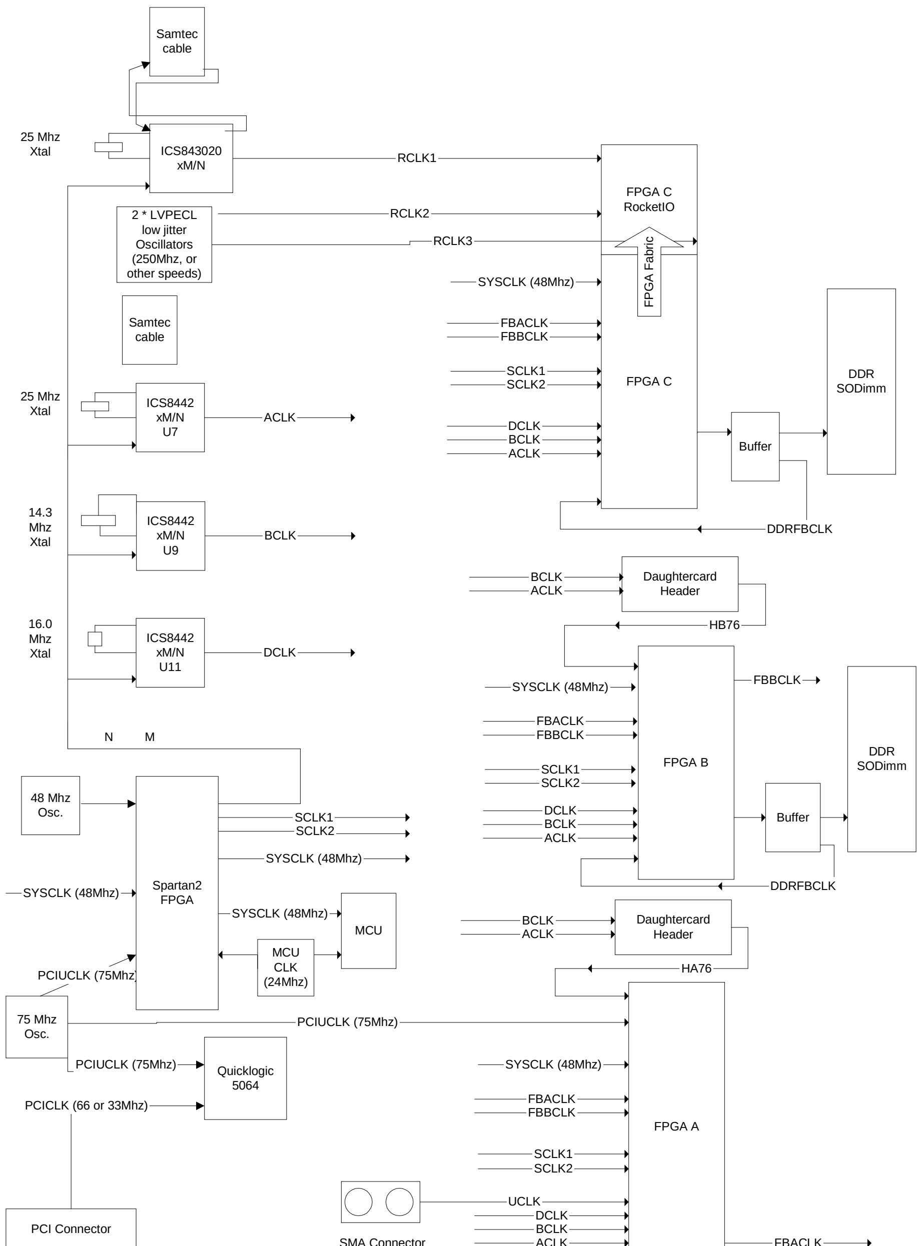


Figure 31 DN8000K10 clocking

From the above diagram, the global clocks are listed here.

RCLK1 – An ICS frequency synthesizer, either an ICS8442, ICS84321 (100-250Mhz), or ICS84020 (667Mhz). This clock is configured from the MCU using the USB controller or the SmartMedia card. This clock is supplied to MGT_CLK pins on FPGA C and can be used as an MGT reference clock for any MGT tile on the left column. The Synthesizer can also be configured to use an external clock input from the QSE-DP Samtec RocketIO connector J3.

RCLK2/3 – An Epson 250Mhz oscillator. This clock can be used to supply an MGT reference clock to FPGA C in either the right of left columns.

ACLK, BCLK, DCLK. These global clocks are supplied by ICS8442 frequency synthesizers. They are configured from the MCU to output a user-specified frequency from 31 to 700Mhz. They are each distribuited to FPGAs A B and C.

SCLK1/2 – These single-ended clocks run at low-speed and are controllable from the USB interface, allowing for software that controls single-stepping designs. Both clocks are delivered to FPGAs A B and C. The clock is sourced directly from the Spartan 2 configuration FPGA.

Sysclk – this 48Mhz, single-ended clock is driven from the configuration FPGA at a fixed frequency. It is delivered to FPGAs A, B, C and the configuration FPGA. This clock is used by the Dini Group reference design to clock the Main Bus interface.

MCU clk- this reference clock is used by the MCU to generate frequencies required for the USB protocol. It is not available to the user.

UCLK – This differential clock input is delivered to FPGA A.

FBACLK – This differential clock is driven from FPGA A and delieverd to FPGA A, B and C. This clock can be used for controlled-clocks, odd clock division and multiplication, or forwarding a clock from on FPGA to another.

FBBCLK – This differential clock is driven from FPGA B and recived at FPGA A, B and C.

HACLK – This differential clock is driven from the daughtercard header A to FPGA A.

HBCLK – This differential clock is driven from the daughtercard header B to FPGA B.

DDRACLK, DDRBCLK – This differential clock is driven by the FPGA to its associated DDR2 Sodimm header. A copy of the clock is externally buffered and the clock is recived on the FPGA synchronized with its arrival at the SODIMM on the signal DDR_FBCLK.

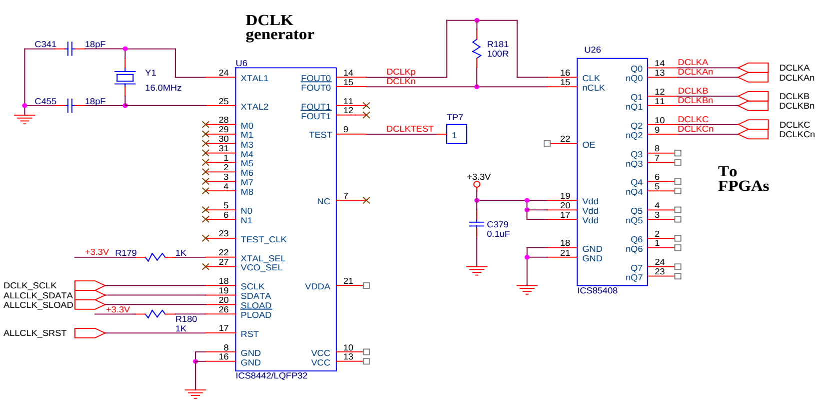
5.1 Global Clocks

The three main global clocks are driven by ICS8442 clock synthesizers, each capable of producing frequencies of 700Mhz (or greater). The clock synthesizers can be programmed from a SmartMedia card, from the GUI application (See Chapter X, the USB Application) or left at their default values (ACLK 100Mhz, BCLK 57.2Mhz, DCLK 64Mhz).

Each ICS8442 has an interal multiplication PLL that can operate between 250 and 700 Mhz. With 1, 2, 4, or 8x division on the output, the possible output frequencies are 31.25 – 700Mhz. VCO_SEL can be used to disable the PLL, so ACLK BCLK and DCLK can operate at their fundamental 25Mhz, 14.3Mhz and 16Mhz respectively.

The Serial configuration bus is connected to the Cypress MCU GPIF pins and controlled through software.

The crystal inputs are parallel resonant, fundamental mode.

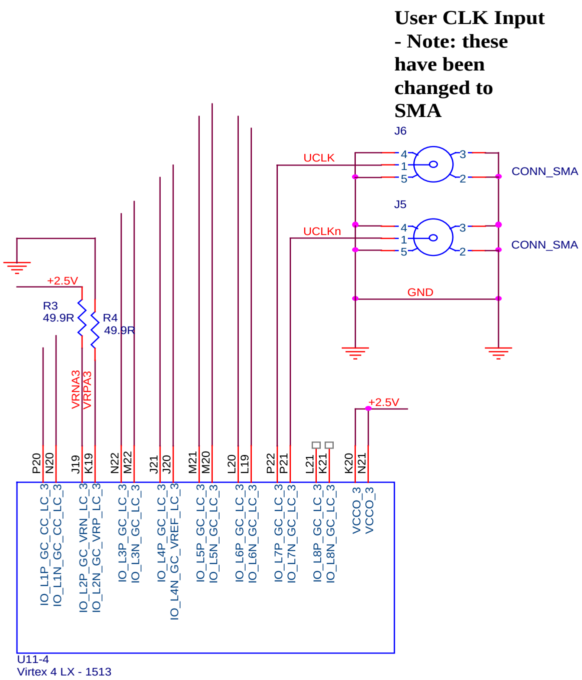


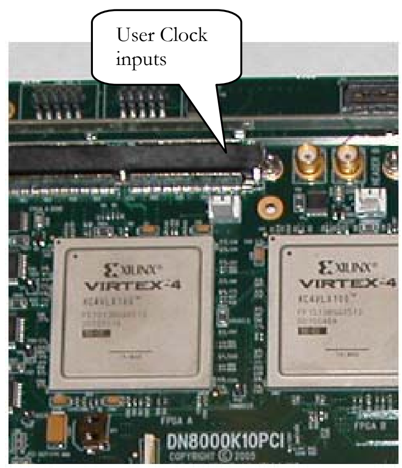
The 8442 outputs are connected to a 1:8 LVDS buffer, and distributed to the FPGAs. Aclk and Bclk are also distributed to the expansion headers as well.

For the input pad sites used for accessing the global clocks in the FPGA fabric, see Appendix X, FPGA pins.

5.2 User Clock

The DN8000K10PCIE has an SMA pair reserved specifically for inputing a clock. The SMA pair is connected to a differential clock input on FPGA A (LVDS_DCI is a preferred input standard, but LVCMOS_25 will work also).





To use this clock in a synchronous design, send a copy of the clock out through the FBA (Feedback A) clock output pairs A, B and C.

For a chart of clock input pad sites on FPGA A, See Appendix X, FPGA pins.

5.3 Feedback Clocks

User FPGA A and B each are capable of sourcing a clock that is distributed to all FPGAs (including back to itself). These "feedback clocks" allow the user to control a clock from inside the user design for single-stepping, multiplication/division, or distributing a clock to which only one FPGA has access (like a header clock, or the user clock input).

FPGA A has 6 feedback outputs, one differential pair to each Virtex 4 FPGA.

FBACLKAp/FBACLKAn, FBACLKBp/FBACLKBn, FBACLKCp/FBACLKCn

FPGA B has 6 feedback outputs, one differential pair to each Virtex 4 FPGA.

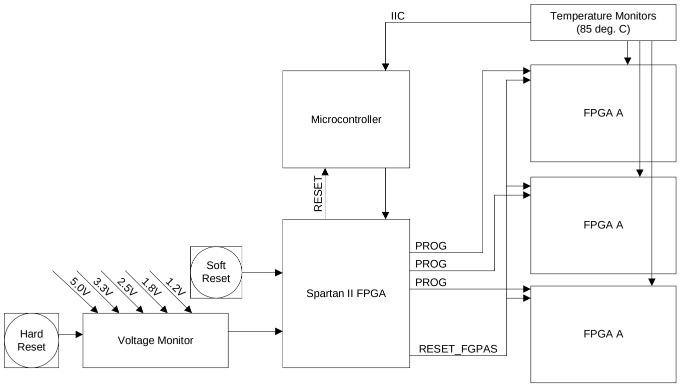
FBBCLKAp/FBBCLKAn, FBBCLKBp/FBBCLKBn, FBBCLKCp/FBBCLKCn

For the pad site locations of the inputs and outputs, see Appendix X, FPGA pins.

Clocks can also be exchanged from one FPGA to another on the source-Synchronous clock inputs. See Chapter X, Section X, FPGA interconnect.

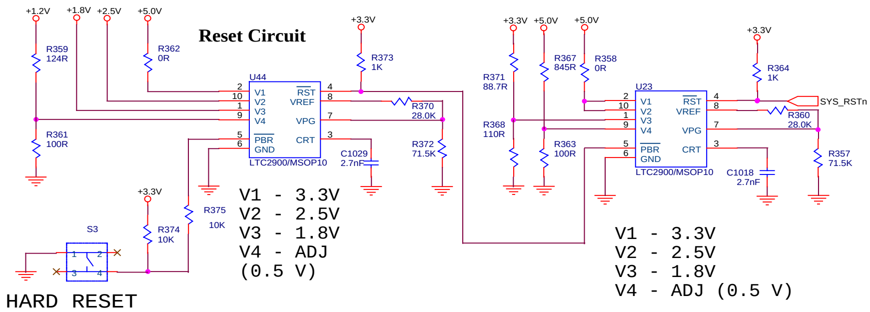
6 Reset Topology

The DN8000K10PCIE is protected from undervoltage and over temperature by a reset circuit. When the board powers on, a voltage monitor waits until all voltages are above their minimum voltage levels, then deasserts reset. The Spartan 2 distributes the reset signal to all FPGAs and the Microcontroller unit, so until the Spartan 2 is configured, reset remains asserted.



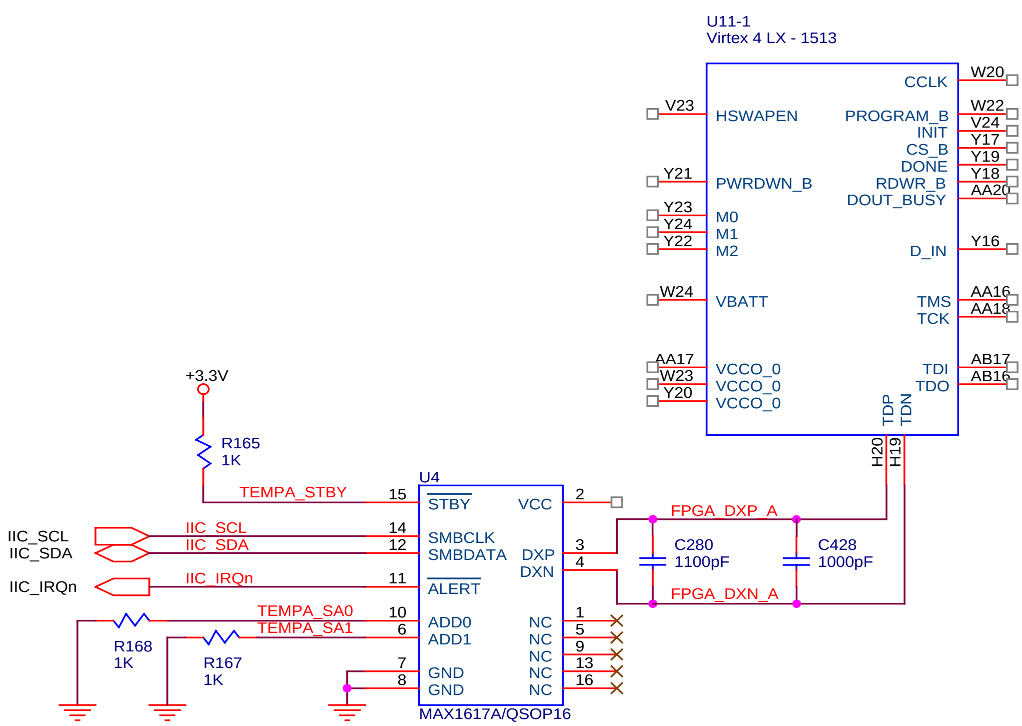
The user may also assert reset by pressing S3, "Hard reset" This will trigger the reset signal "SYS_RSTn" which is monitored by the Spartan FPGA. When SYS_RST is asserted, the Spartan FPGA resets the Virtex 4 FPGAs, causing them to lose their configuration data and deactivate. The Spartan also causes a reset on the Microcontroller unit, which will cause the microcontroller to reload configuration instructions from the Smart Media card. USB contact will be lost with the USB host, and the DN8000K10PCIE will have to re-enumerate.

There is a second button, S2 called "Soft Reset". When this button is pressed, the signal "RESET_FPGAs" is asserted. This signal is sent to the Virtex 4 FPGAs on a user IO pin, and could be used by the user design as a reset signal. This signal is also asserted to all FPGAs after any FPGA becomes configured. RESET_FPGAs is an asynchronous signal.



The above circuit shows how two LTC2900 voltage monitors are daisy chained together to monitor 5 different voltages.

Each FPGA is also connected to a temperature monitor. The Virtex 4 FPGA can easily overheat if a heatsink and fan are not used. The recommended operating temperature for the Virtex 4 is 85 degrees C. The absolute maximum temperature for operation is 125 degrees C. If at any time the junction temperature of the Virtex 4 exceeds 85 degrees, the Microcontroller will reset the FPGAs, causing them to lose their configuration data. An overheating FPGA could be the result of a misconfiguration, a clock that is set incorrectly, or an inadequate heatsink unit. The heatsink and fan assembly that comes with the DN8000K10PCIE is appropriate for dissipating the amount of heat energy available through a PCI slot without the auxiliary power connector (25W total for the card). If you are operating the DN8000K10PCIE at very high speeds in stand alone mode and you are causing heat overload resets, you may need to install a larger heatsink, or increase the system airflow.



This circuit shows the MAX1617 temperature monitor. The IIC bus is connected to the Cypress microcontroller.

7 Power

The DN8000K10PCIE gets is power from the 12V and 3.3V rails of the PCI Express card edge connector. It can also be operated in stand-alone mode with a 20-pin ATX power supply connector.

The PCI slot is capable of sourcing 25W.

The main rails of the DN8000K10PCIE are:

- 1.2V – This is the main power supply rail used for the internal digital logic of Virtex 4 FPGAs.

- 1.8V – This is used for IO signaling and interal logic of DDR2 SDRAM memory. It is also used to supply some Gigabit optical modules, and is used as a low-power current source to supply RocketIO isolated power rails.

- 2.5V – This is used to power FPGA interconnect with low-power LVDS. It is also used as the analog power supply on the Virtex 4 FPGAs.

- 3.3V – This voltage supplies the LVDS clock distribution trees. It is also used to power the LVTTL interfaces of the Cypress microcontroller.

- 12V – This voltage is used to supply power to the 1.2, 2.5, 5.0 and 1.8V switching power supplies. It also powers the FPGA cooling fans. If the PCI slot isn't providing enough power, then a Hard Drive 4-pin power cable can be connected to the board (from the same ATX power supply) to reduce the voltage droop on 12V. Please note that the board is capable of exceeding the 25W limit of the PCI connector (depending on the desity of the FPGAs utilized, and the operating frequency).

- 5V – This voltage supplies some RocketIO power.

The DN8000K10PCIE also has these secondary rails:

- 0.9V – This voltage is used to terminate the SSTL18 signaling of the DDR2 memory module. Current is drawn from 3.3V

- RocketIO 1.2V top, 1.2V right, 1.2V bottom – These linear regulated rails are very low noise supplies for the RocketIO CML inputs and outputs, and RocketIO logic. They are isolated from each other to improve the isolation of multiple RocketIO channels operating simultaneously.

- RocketIO 1.5V – This linearly regulated voltage rail supplies the internal digital logic of the RocketIOs.

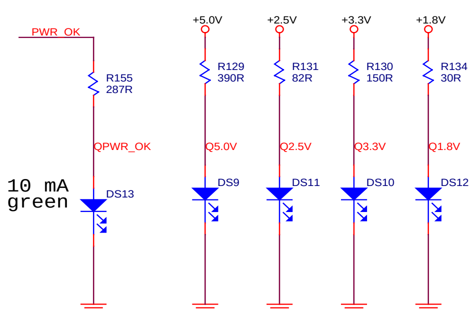
- RocketIO 2.5V – this linearly regulated voltage rail supplies the internal analog circuits of the RocketIO.

- -12V – This rail is passed directly from the PCI edge connector and ATX power connector to the Micropax expansion header. See Chapter X, Section X, Expasion Headers. Note that the fuse between -12V and the expansion headers is not installed on the board.

- XFP VEE5 – Power for this rail is not supplied by the DN8000K10PCIE, but is required for the operation of ECL optical modules. To power this rail, you will need to connect an external power connector to the board from a low-noise voltage supply.

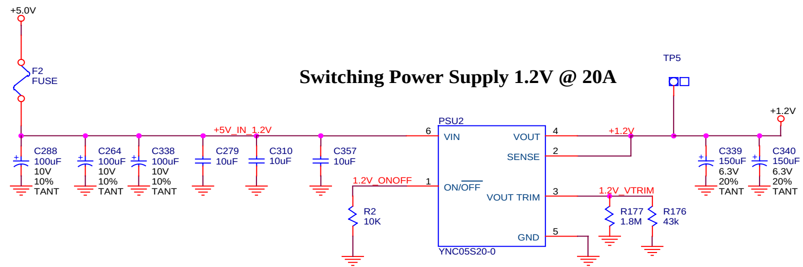
There are test points for measuring the voltage levels of each rail near the top left of the DN8000K10PCIE. Each rail is monitored by a voltage monitor circuit, and will cause a reset if any of the primary supplies drop 5% or more below their setpoints.

There are also LEDs next to each testpoint to indicate the presence of each voltage rail. These LEDs do not indicate that a rail is within 5% of its setpoint, only that the rail is present and above ~1.6V. A power OK led shows the status of the ATX power supply's PWR_OK signal. If this LED is lit, then +5.0V and +3.3V (and +12V –12V) are within 5% of their setpoints.



7.1 Switching power supplies

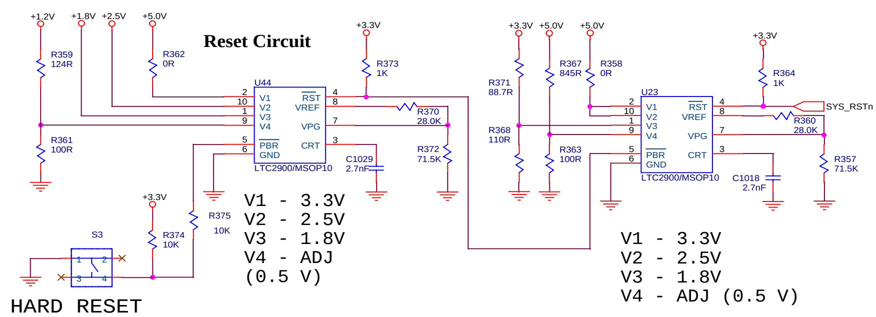
The main power rails for the Virtex 4 FPGAs are produced on board with three 20A switching power supplies, one for each of 1.8V, 2.5V, and 1.2V.



The DN8000K10PCIE is shipped with a fun mounted above the power supplies to help keep them cool. If you need to remove this fan, the DN8000K10PCIE will function properly without it, but be careful not to touch the power supplies with your fingers because they will burn!

Each power supply is protected with a 15A fuse on the inputs. If you need to operate the DN8000K10PCIE with more than 15A of current for a power supply, you can change this fuse, but you need to find a heatsink solution for keeping the Virtex 4 FPGAs cool. The heatsink and fan provided are appropriate for a power consumption of about 10-15W per FPGA.

Each of the primary power rails (5.0, 3.3, 2.5, 1.8, 1.2) is monitored for undervoltage. If the voltage monitor circuit detects a low voltage, it will hold the board in reset until the supply is back within 5% of its setpoint. See section X, Reset Circuit for information on reset.



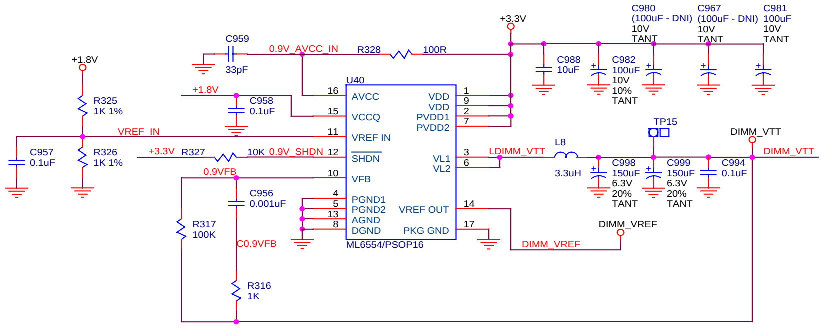
7.2 Secondary Power Supplies

The secondary power supplies are derived from a primary supply.

7.2.1 DDR2 Termination Power

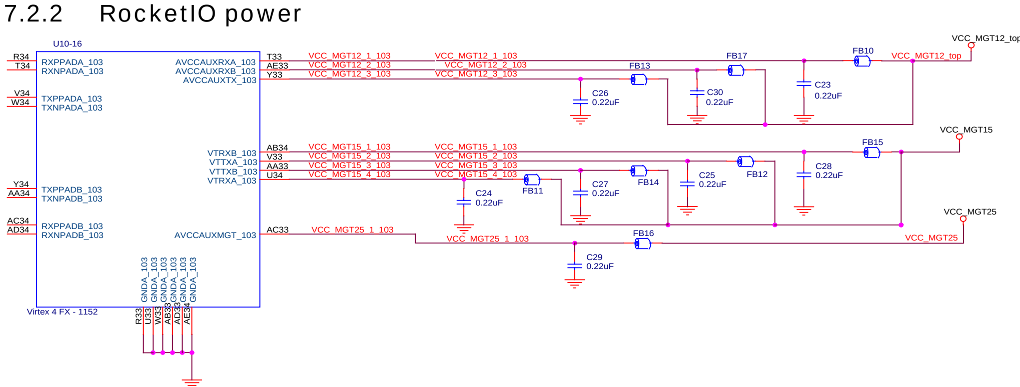
DDR2 memory modules use the SSTL18 signaling standard. Properly terminating SSTL18 requires a termination power supply of 0.9V. Since as much as 1.6 Amps of termination current are needed, a switching power supply is required.

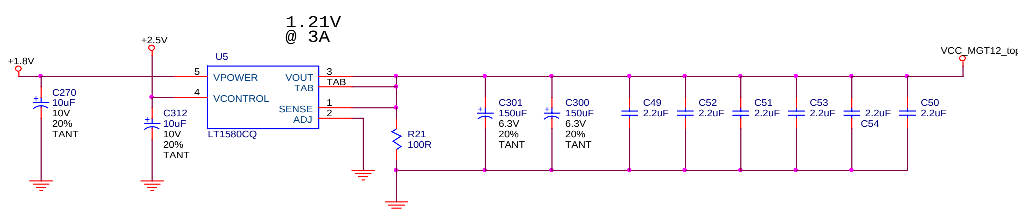
DDR Switching Power Supply VTT - 0.9V @ 3A



The ML6554 produces up to 3A of the required 0.9V termination power rail along with a stable 0.9V reference voltage supply.

7.2.2 RocketIO power

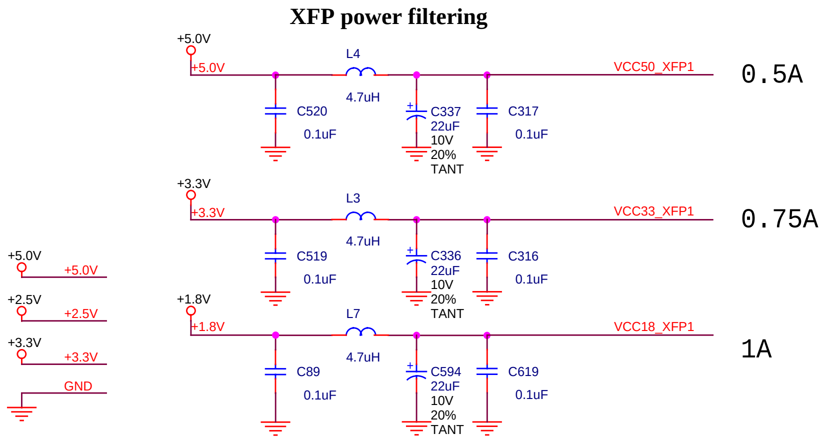




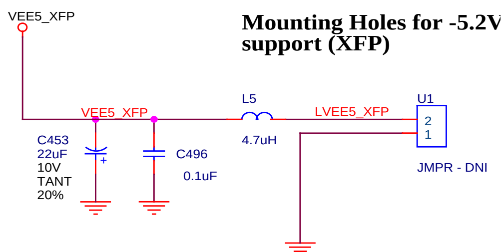
Five linear rails

7.2.3 Optical Module Power

Optional optical modules have a variety of power supply requirements, most of which are met by the DN8000K10PCIE.

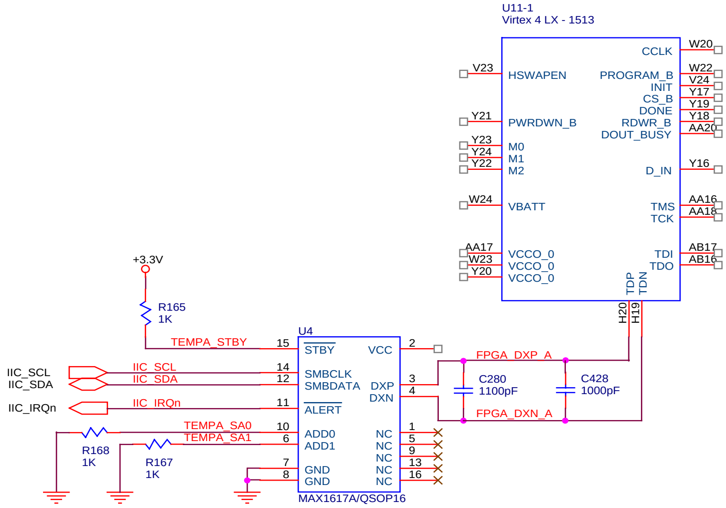


Since the DN8000K10PCIE has no negative voltage supply, it cannot generate the –5.2V required to supply ECL-based optical tranciever modules. An auxiliary power connector is supplied to connect to an external voltage supply if ECL signaling is required.

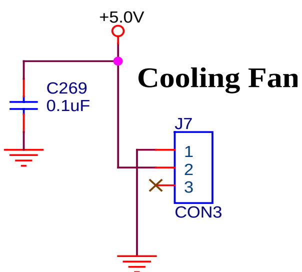


7.3 Heat dissipation

Virtex 4 FPGAs are capable of drawing incredible amounts of current from their 1.2V and 2.5V power supplies. According to Xilinx online power estimator tool, a fully utilized FPGA running at 300Mhz can draw more than 30W of power. With this much power used in each FPGA, the DN8000K10PCIE can dissipate 75 or more Watts of heat. For all but the most trivial designs, a heatsink must be used with the Virtex 4 FPGA. The DN8000K10PCIE comes with a forced air heatsink rated at 2 degrees per Watt. Since the maximum operating junction temperature of a Virtex 4 FPGA is 85 degrees, assuming an ambient temperature of 50 degrees (the inside of your computer case) the most amount of energy dissipated by the FPGA using the standard fan is 85 – 30 / 2 = 27.5W. This should be sufficient for most applications. If you intend to operate the Virtex 4 FPGA at very high speeds, or are getting overheating issues with your design, you will need to install a larger heatsink.



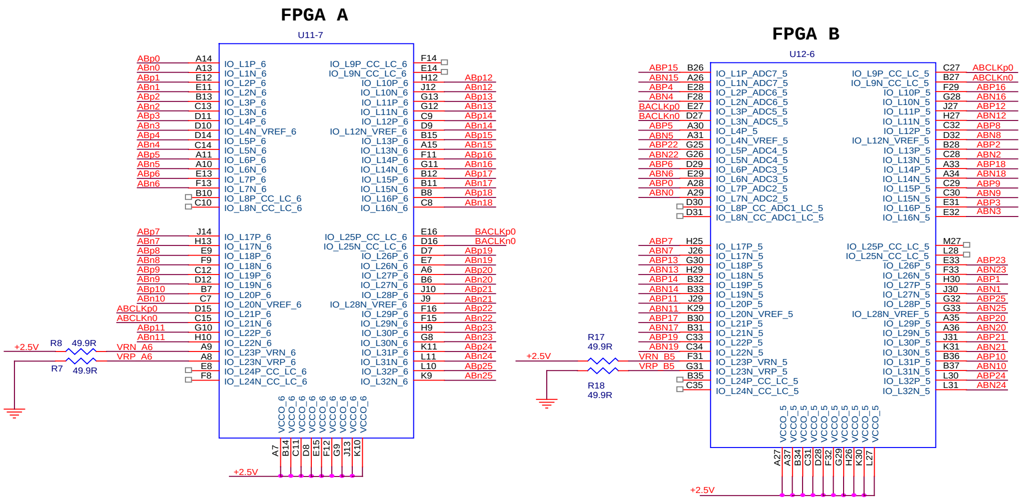
Above: The FPGA temperature monitor circuit. The MAX1617's IIC bus is connected to the Cypress MCU.



Above: Colling fan power connector.

8 FPGA interconnect

The DN8000K10PCIE was designed to maximize the amount of interconnect between the two primary Virtex 4 FPGAs A and B. This interconnect was routed as tightly coupled differential LVDS to provide the best immunity to power supply and crosstalk noise so that your interconnect can operate at the full switching speed of the output buffers. Following Xilinx recommendations, the interconnect on the DN8000K10PCIE was designed to operate at 1Gb/s for every LVDS pair. (Note 1Gb/s operation requires the fasted speed-grade part, LX200 –12) In order to achieve such breakneck speeds, you will need to operate the busses of signals using a source-synchronous clocking scheme. The interconnect signals on the DN8000K10PCIE have been optimized to operate in "lanes" There are 7 lanes between FPGAs A and B, three between B and C and two between FPGAs A and C. Each lane has a differential LVDS source-synchronous clock in each direction. For a complete pinout of the Virtex 4 FPGA interconnect, along with a breakdown of lane assignments, see Appendix X, FPGA pins.



Clocking incoming data at high speeds required the used of the each input's delay buffer to align each bit. The incoming clock needs to be adjusted and used to clock the inputs within its lane. This process can be automated by the use of the new Virtex 4 feature IDELAYCTL.

For detailed description of the required user design to achieve 1Gbs operation, see Xilinx Application note XAPP704, "High Speed SDR LVDS Tranceiver".'

Synchronus clocking and single-ended signaling are still possible on the DN8000K10PCIE, you are not required to use highspeed serial design techniques. Single ended interconnect is recommended for signaling below 133Mhz. Because of the DN8000K10PCIE's excellent low-skew clocking network, global synchronous clocking should work fine for your interconnect at speeds lower than 300Mhz. The source synchronous clock signals can also be used as single ended or differential interconnect, or to forward clocks from one FPGA to another.

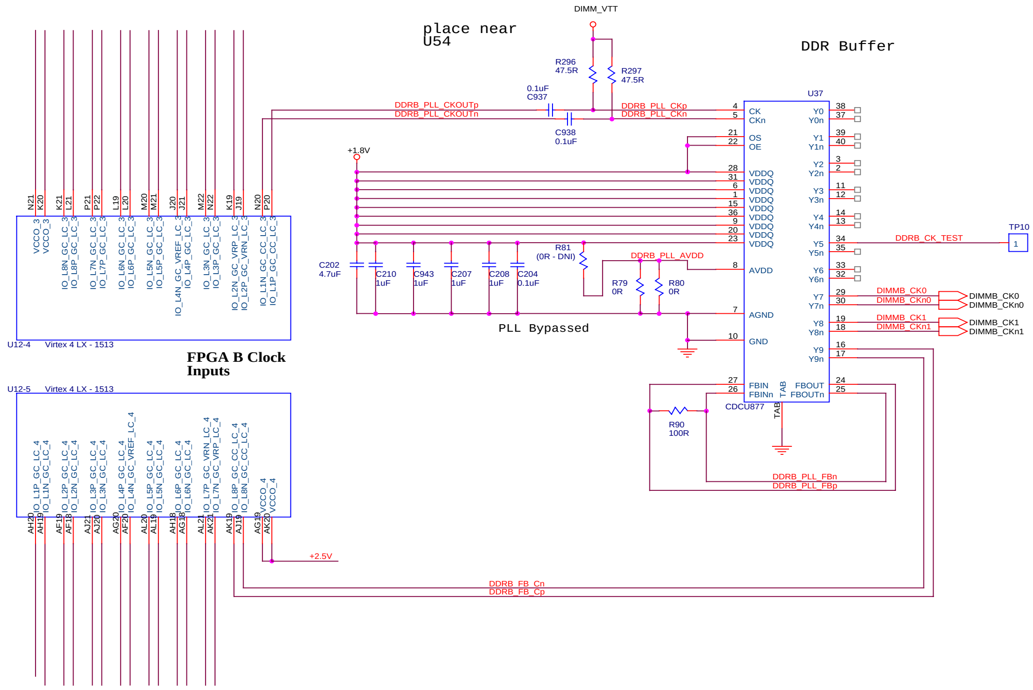
The total interconnect counts between FPGAs

- A-B 378
- B – C 154
- A – C 164

9 Memory interface

There are two standard 200-pin DDR2 SODIMM module sockets on the DN8000K10PCIE. These sockets are supplied with 1.8V power and keyed for use with DDR2 SDRAMs. One socket is connected to FPGA B and the other is connected to FPGA C.

9.1 Clocking

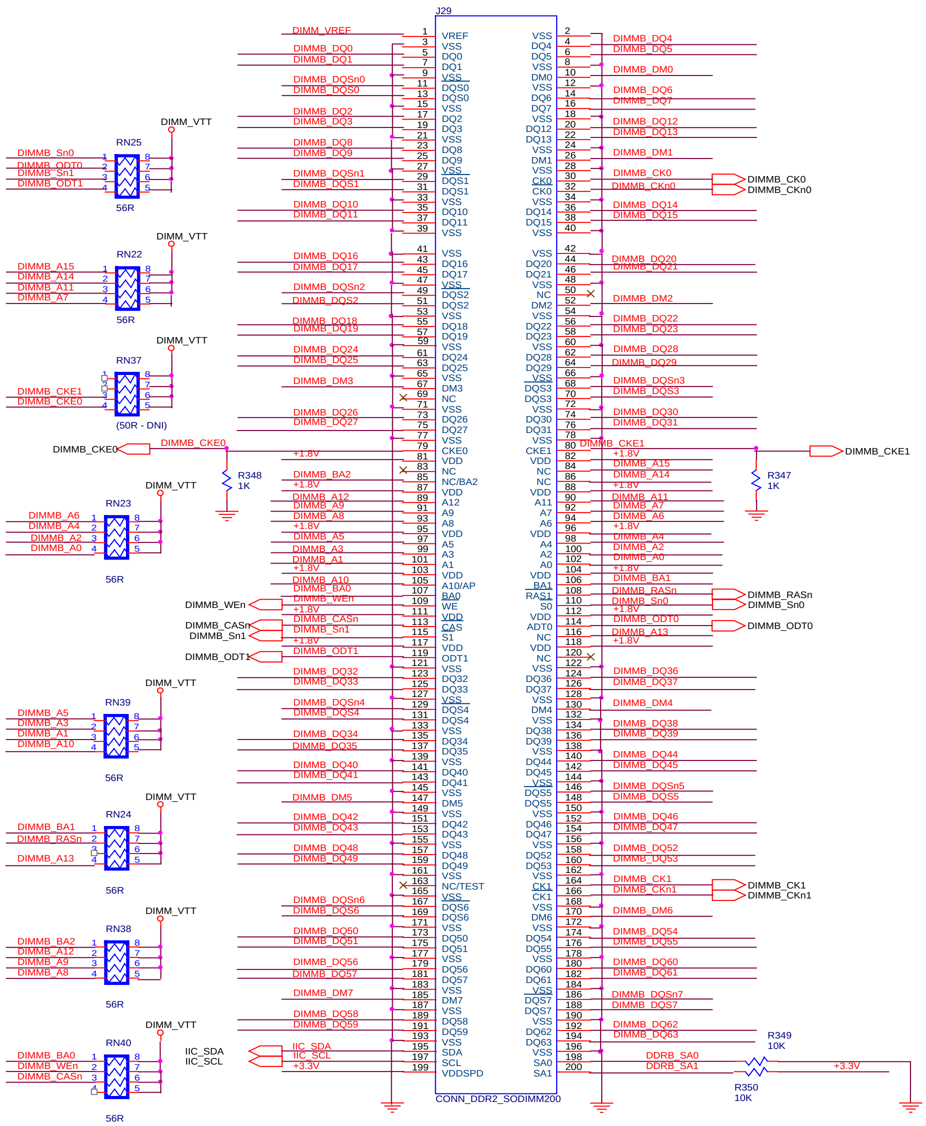


SODIMM interfaces:

See Appendix X, FPGA pins

9.2 Serial presence detect.

The EEPROM on the SODIMM is accessable by PCI, USB, or configuration UART.



10 Headers

There are two daughtercard headers on the DN8000K10PCIE; one attached to FPGA A (Header A), and one attached to FPGA B (Header B). Header A contains 135 user IOs designed to operate as 134 differential pairs. Header B has 154 user IOs that can be used as 77 differential pairs.

The signals RESET_FPGAs is driven by the Spartan Configuration FPGA. This signal is the same as the RESET_FPGAs driven to FPGAs A B and C.

PDETECTA and PDETECTB are signle-ended signal with an external pull up resistor. The daughtercard can ground these signals to indicate the daughtercard's presence.

The HAp/nCC and HBp/nCC signals are connected to global clock input pins on the FPGAs. These can be used as differential clock inputs from the daughtercard headers to the FPGAs. They can also be used as outputs.

The ACLK and BCLK signals are copies of the DN8000K10PCIE global differential clocks ACLK and BCLK. The signals are synchronized at the daughtercard connector with the ACLK and BCLK signals at the pins of the FPGA.

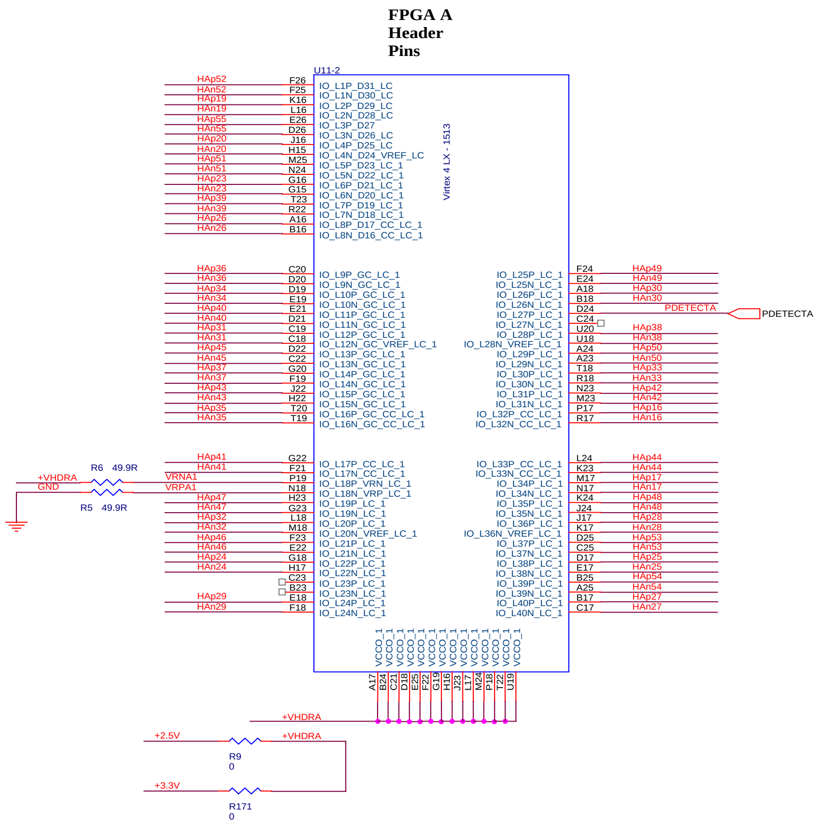
Header B has more signals than Header A. A daughtercard designed to work with header A will work with header A.

10.1 3000K10 Compatibility

The DN8000K10PCIE headers use pinout similar to that on the DN3000K10. A compatibility chart with the DN3000K10SD and Mictor daughtercards is given in the *Appendix Pins*. The +1.5V power supplies, MBCLKA-F are not present.

10.2 FPGA Connection

On the DN8000K10PCIE, all header signals are connected to "LC" pins on the Virtex 4 FPGA. See the Virtex 4 User's Guide for detail about these signals. The main result of this is that the headers on the DN8000K10PCIE may not be used with the Virtex 4's current-mode LVDS drivers. Virtex 4 LVDS receivers may still be used. Outputs compatible with LVDS can still be achieved using the proper selectIO driver settings and termination.



On both Header A and Header B, there is a bank that is dedicated entirely to the Headers. For details about Virtex 4 IO banks, see the Virtex 4 user guide. This bank can be used for standards requiring a threshold volrage reference, such as SSTL. You can also use this bank for source-synchronous clocking.

10.3 IO Power

The IOs connected to the headers on the Virtex 4 FPGAs are powered with a +2.5V power rail.

10.4 Physical

Micropax part number FCI 91294-003

The standard Dini Group mounting hole location for all 200-pin Micropax connections is (430 mils)

10.5 Daughtercard Power

Power is supplied to the daughtercard though dedicated power supply pins. The maximum allowed current for each of the daughtercard supplies is

5.0V – 1A
3.3V – 1A
2.5V – 1A

12V – 250mA
-12V – 250mA

The 12V and –12V supplies are by default disconnected by removing the series jumper resistors R413, R412, R411, R414. This help prevent accidental damage due to careless probing. The 12V and –12V supplies may be able to source as much as 0.5A of current if the current can be supplied by the host PC.

10.6 The Mictor

There is a Mictor connected designed to be used with an aginlent logic analyzer. Riscwatch power PC debugger can also be used over this connection.

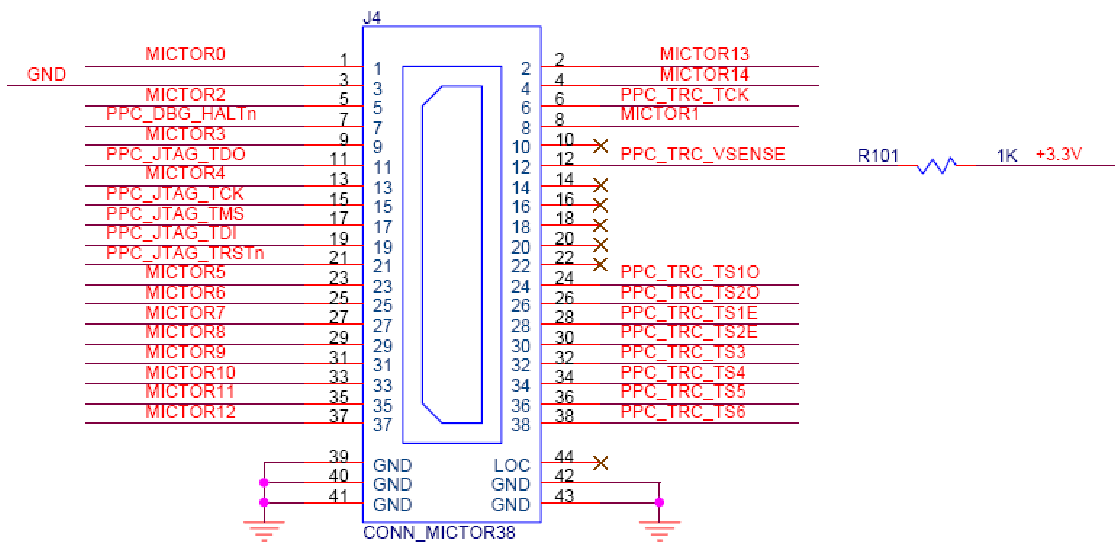


Figure 32 Mictor Header

11 LEDs

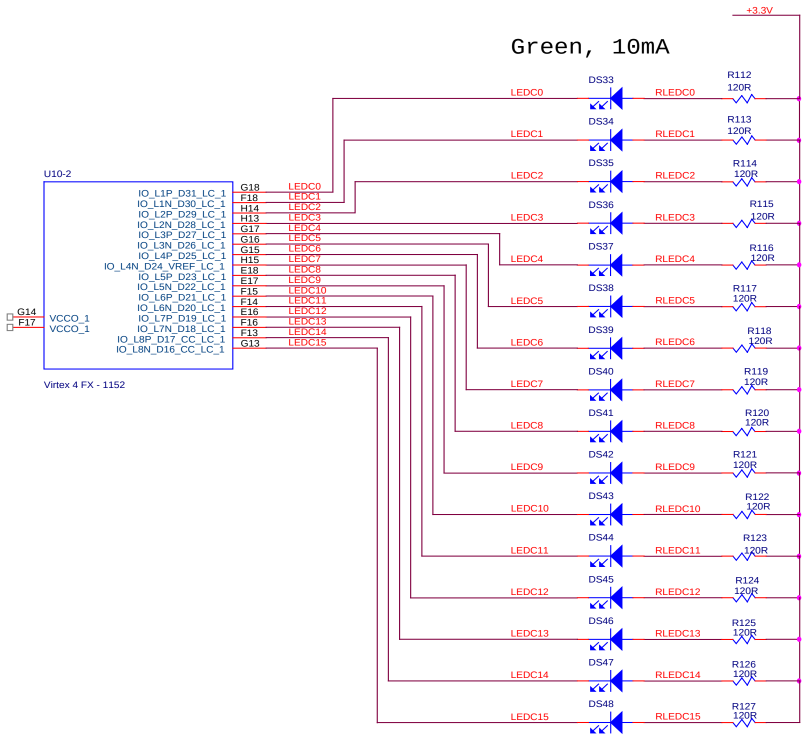


Figure 33 FPGA C LEDs

FPGA A is connected to 8 green LEDs. FPGA C is connected to 16 LEDs. These LEDs can be used for the user design. The brightness of these LEDs can be controlled by changing the output standard on the LED signals from 2, 4, 12, 16 or 24mA.

12 RocketIO

12.1 RocketIO Clock Resources

Since it is impossible to determine during manufacturing the clocking requirements of every possible end application, the DN8000K10PCIE comes with a flexible clock network capable of a wide range of serial frequencies, while maintaining the tight jitter requirements of the 10 Gigabit serial trancievers.

The RocketIO clock tree is driven by a synthesizer and two oscillators, and dedicated multiplexers inside the Virtex 4 FPGA allow the user to switch between these clock sources.

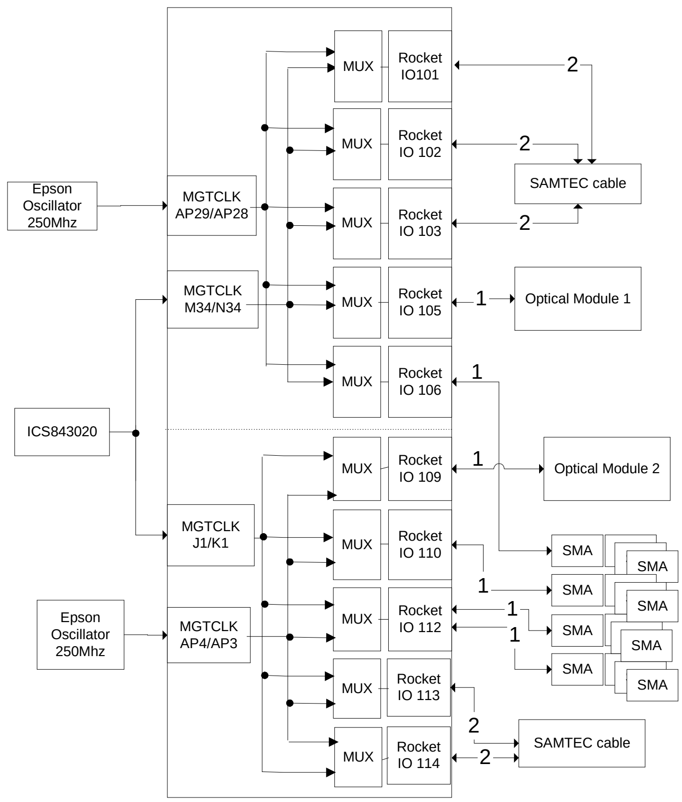


Figure 34 Internal MGT clocking

The RocketIOs on the Virtex 4 FPGA is divided into two columns, X0 and X1. The clock network of each column is separate and clocks may not be shared between the two columns. Each column has two clock distribution trees and two clock inputs. Each tree can be driven by a clock input, by a clock from a global clock input
(not recommended) or by a recovered clock. Finally, each tile has a multiplexer than can select from one of the two clock trees to clock that entire tile.

The diagram above shows the two RocketIO columns and the connectivity of each.

Once a clock is routed to an MGT tile, that clock can be multiplied and divided by the MGT tile.

Most users will want to use the frequency synthesizer for generating RocketIO reference clocks. The ICS843020-01 synthesizer is very low jitter and should suitable for operation up to 6Gbs RocketIO operation. The frequency of the synthesizer can be adjusted through the main.txt file on the SmartMedia card, or through the USB GUI program.

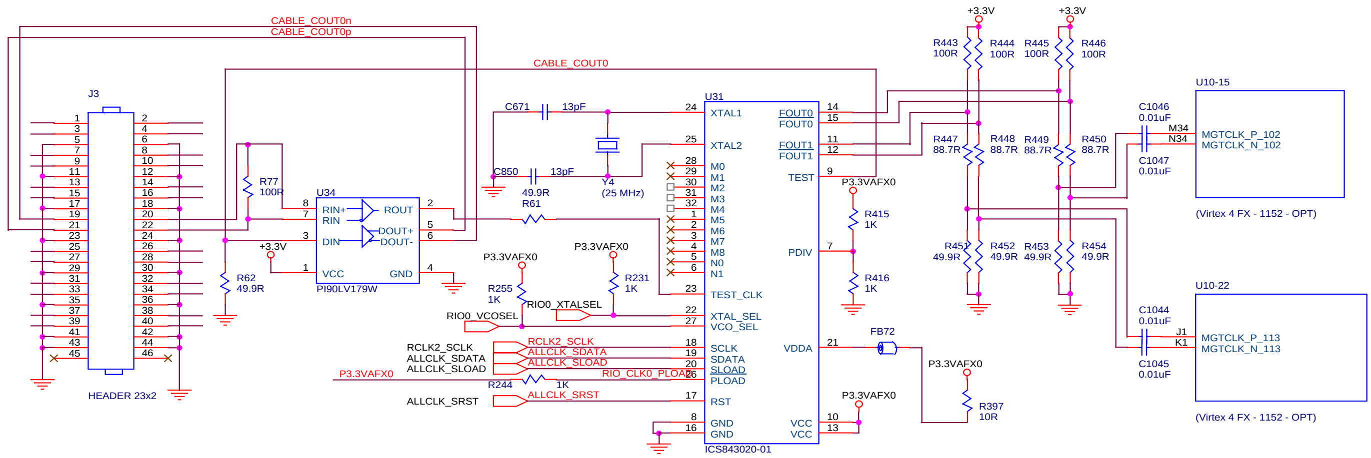


Figure 35 MGT 8442 Connections

The LVPECL outputs of the ICS843020 are scaled down to meet the input requirements of the MGTCLK inputs.

An output from the ICS843020-01 is also converted to LVDS and driven to J3 pins 19 and 21, the Samtec QSE-DP connector. This can be used to forward a RocketIO clock off board along with rocketIO signals to support standards that require an exact reference clock, like PCI Express. J3 may also drive pins 20 and 22. The ICS843020-01 can receive this clock and use it to generate a frequency for the MGTCLK inputs.

For 10Gb serial transmission rates, you should use one of the low-jitter fundamental frequency SAW oscillators. These oscillators operate at 250Mhz and so cover the gaps in the frequency synthesis options given by the ICS843020-01.

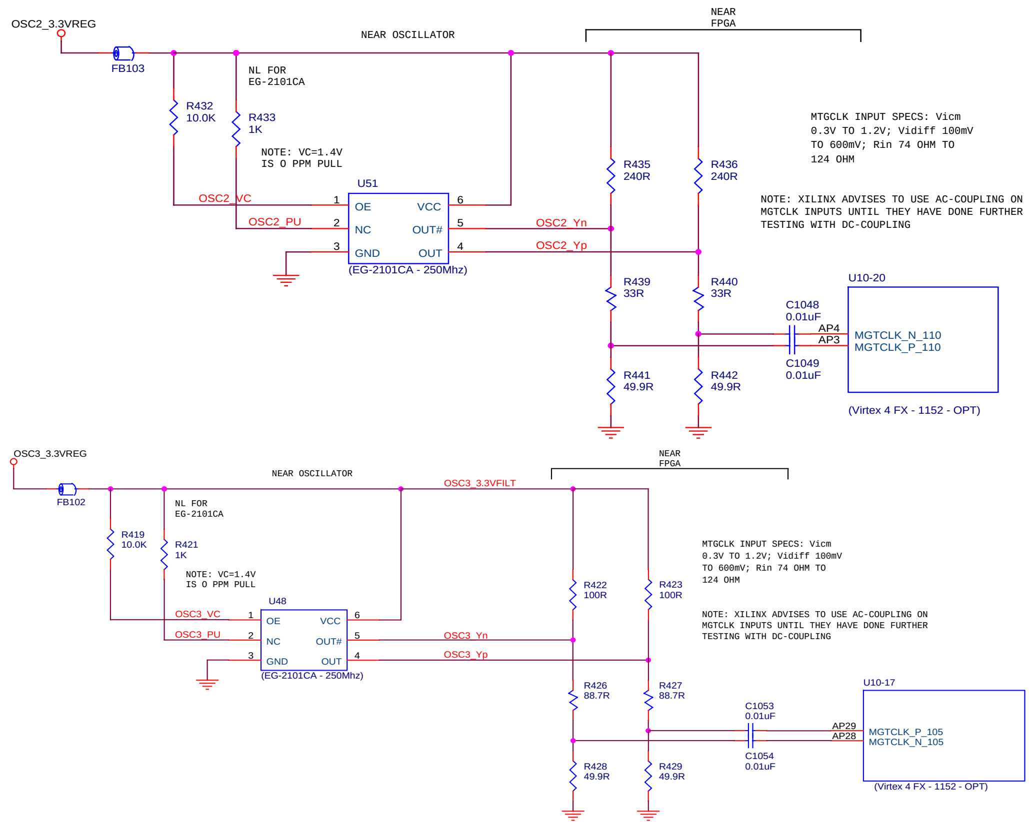


Figure 36 MGT PECL Oscillators

There are two Epson2101CA SAW oscillators, U51 and U48. Each one drives a MGTCLK on to one side of the

The ICS843020-01 Frequency Synthesizer is a very low phase noise. With the default 25Mhz oscillator, the frequency synthesizer is capable of producing frequencies in the ranges 71.875-84.375, 143.75-168.75, 287.5-337.5, and 575-675 Mhz.

12.2 MGT Power network

The RocketIO strict power supply constraints require the use of heavy power supply filtering. The RocketIO's three power rails are each generated by a linear voltage regulator.

12.2.1 FX CES2 rework

If your DN8000K10PCIE came with the option "FPGA C – FX60CES2", then a late-breaking Virtex 4 erratum required the following rework. This rework is not shown in Appendix X, Schematic

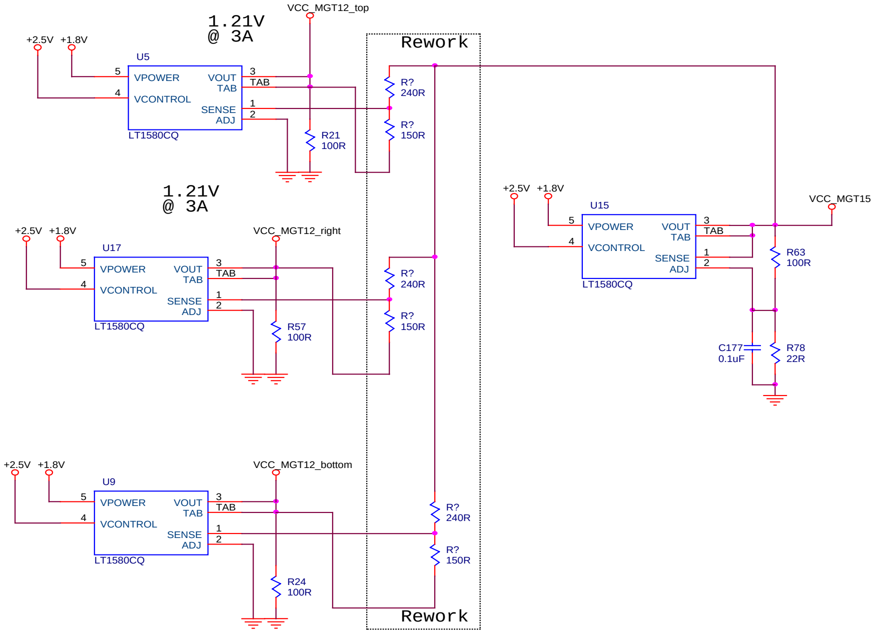


Figure 37 MGT 1.1V rework

This rework drops the 1.2V RocketIO supply from 1.25V to 1.14V.

12.3 The connections

The following sections list the individual RocketIO connections. For a complete pinout of the RocketIO connections, See Appendix X, Pins.

12.4 Samtec Multi Gigabit ribbon cable

For board-to-board high-density connections, two Samtec ribbon cable connectors (J2 and J3) are connected to RocketIO. The pinouts on the cable allow two DN8000K10PCIE boards to be connected to each other for a total of 10 bi-directional channels operating at 5Gbs per channel, per direction.

The Samtec part number (J2, J3) QSE-014-01-F-D-DP-A

An appropriate crossover cable for cabling two DN8000K10PCIEs together is the Samtec EQDP-014-09.00-TBR-TBL-4

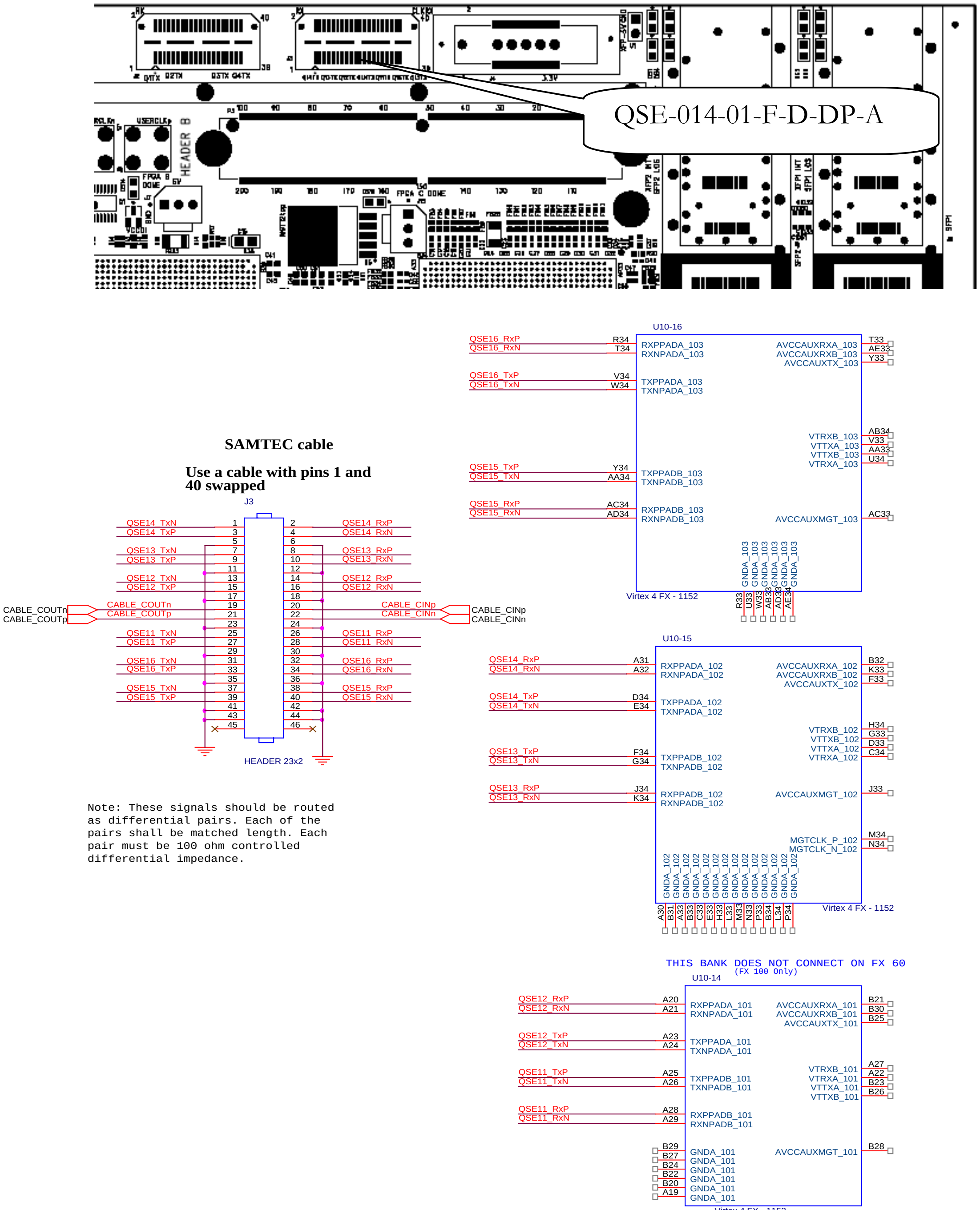
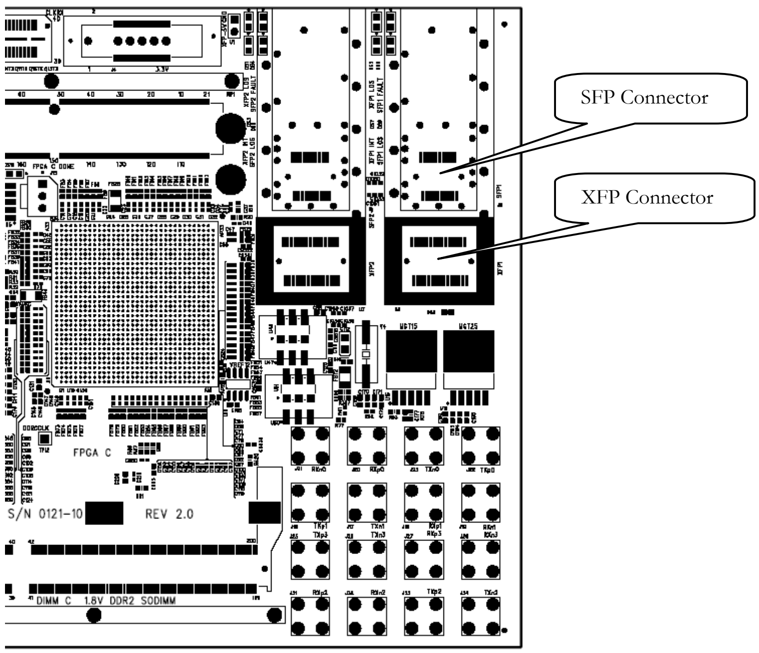


Figure 38 QSE Connector

Each connector also has a clock input that can be routed to the MGT CLK of FPGA C to allow standards that require transmitting at an exact frequency, such as PCI Express.

12.5 Optical Modules

The DN8000K10PCIE comes with two optical module connectors. If you need to interface to a specific standard, the easiest way is to buy an SFP or XFP module that supports that standard.



12.5.1 SFP

SFP modules support 1-4.5Gbs serial trasmission rate.

Two red LEDs show the status of the channel. The LOS LED indicates that the far end transmitter is not operating, the cables are not secured or matched to the transmitter wavelength. The INT LED indicates. The FAULT LED indicates a transmission laser failure, or an unsecured module.

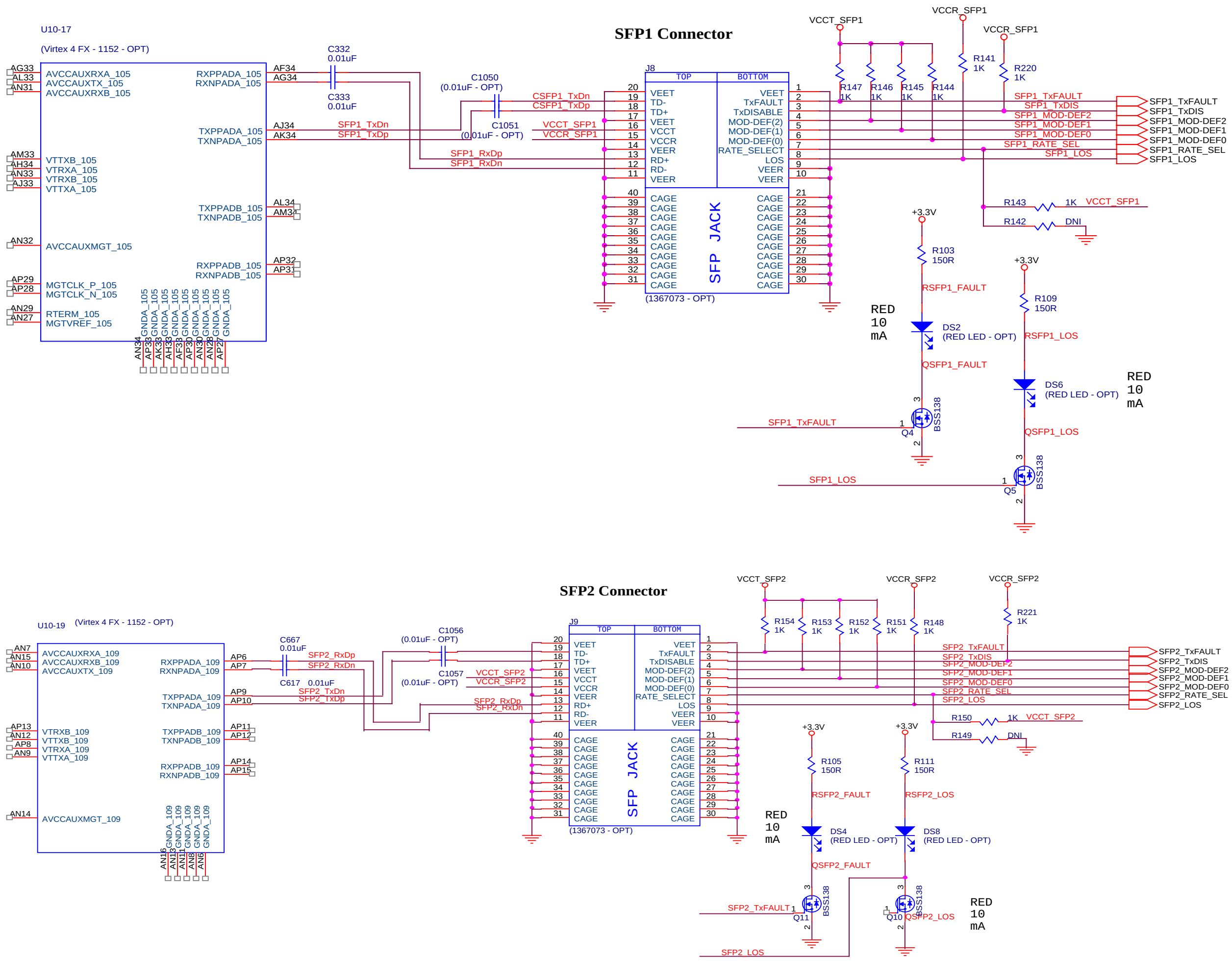
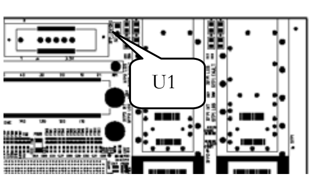


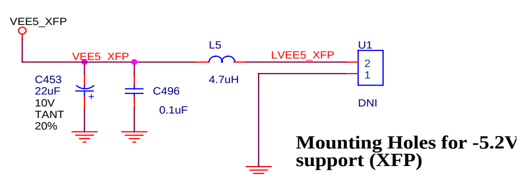
Figure 39 SFP modules

12.5.2 XFP

XFP modules are the fastest optical modules that do not require a

The XFP specification allows for an optional –5.2V power supply to be provided by the host board for ECL transmitter modules. The DN8000K10PCIE provides no –5.2V power, so a mounting point (U1) is provided for the use of a bench supply if ECL signaling is required.





Some XFP modules may require a reference clock to retime the transmitted signal (The REFCLK signal in the XFP specification). The REFCLK signal is connected to a RocketIO output on FPGA C. The REFCLK signal should be 1/64 of the data rate driven onto the XFP's TX pins. To drive this signal, See Xilinx Application note XAPP656. To meet the input requirements of the XFP module, you must increase the differential swing voltage of the MGT transmitter outputs. Set TXDAT_TAP_DAC to 800mV.

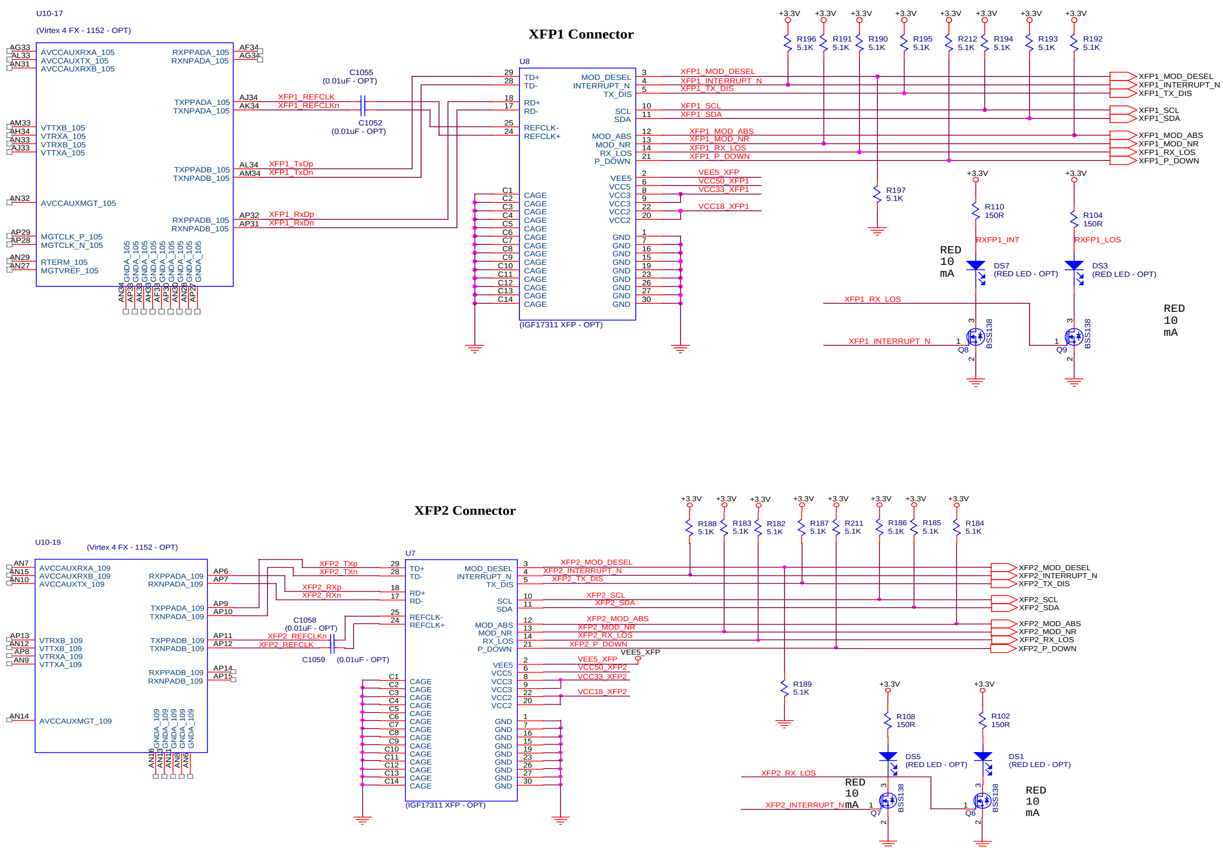


Figure 40 XFP Modules

12.6 The SMAs

The easiest way to connect two RocketIO channels is through the use of SMA cables. The SMA connections on the DN8000K10PCIE were designed to operate at the full 11Gb potential of the Virtex 4 RocketIO trancievers.

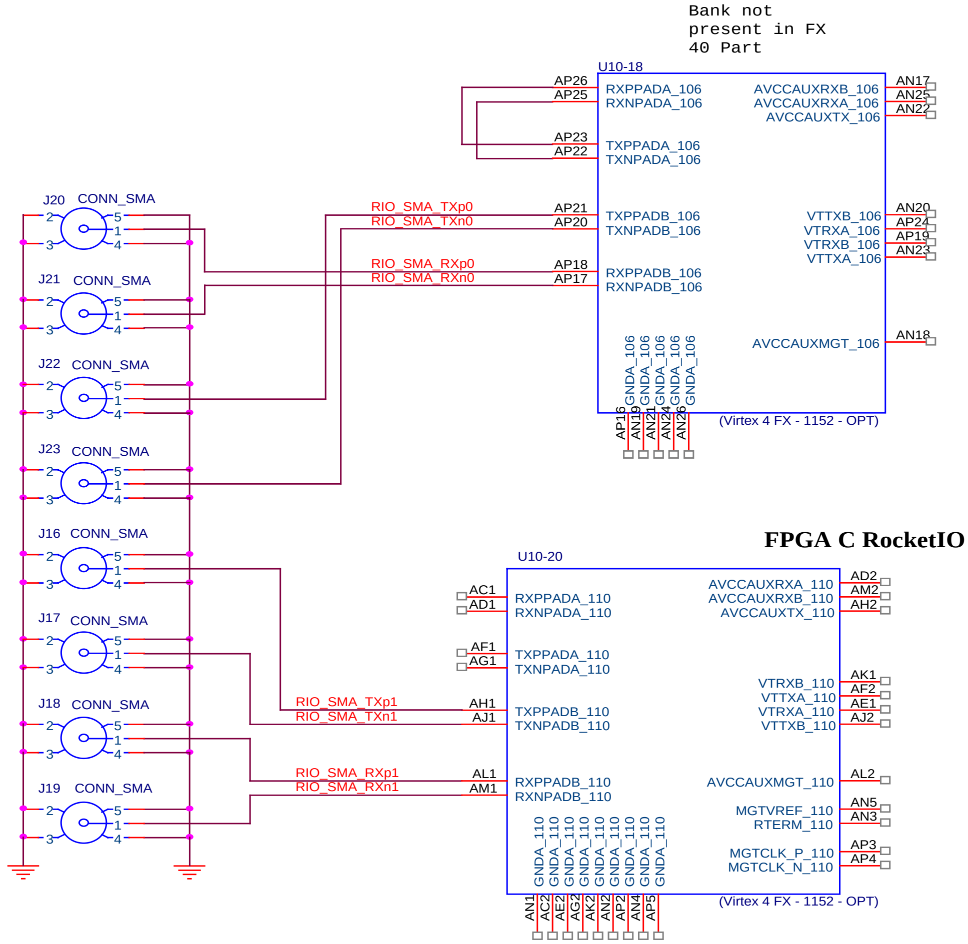
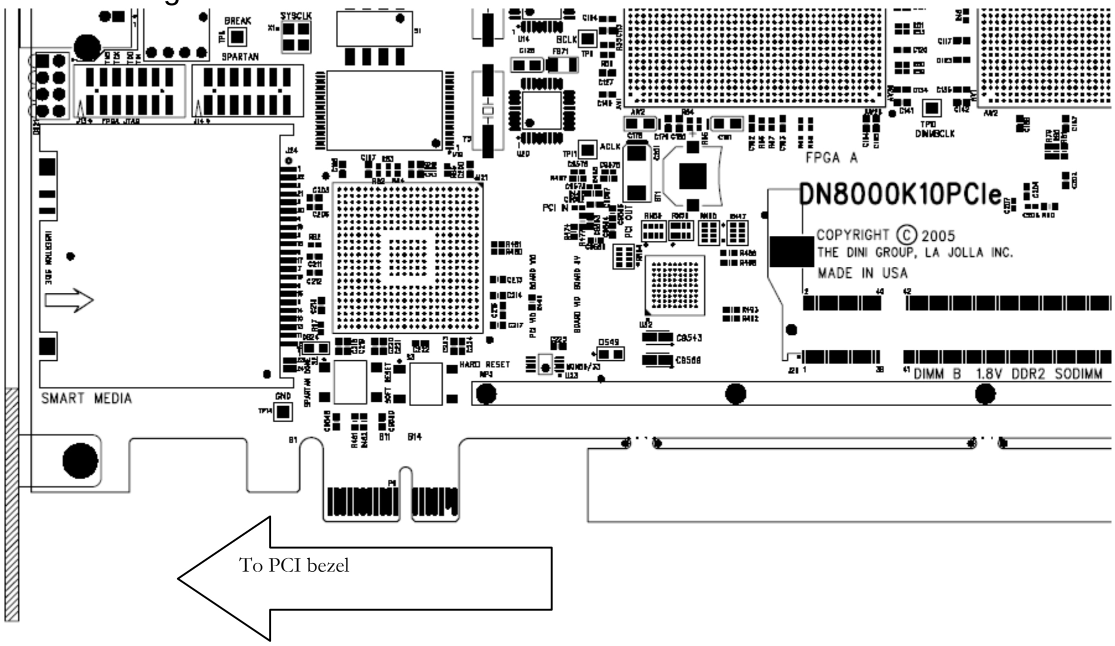


Figure 41 SMA Connections

The loopback pair AP26 and AP25 can be used to test your Virtex 4 fabric design. You may want to get the loopback pair working before attempting to transmit high data rates over a cable system.

13 PCI Express interface

13.1 PCI edge connector



13.2 The Phillips PX1011A

The Phillips PX1011A is a 1x PCI Express PHY chip, providing an 8-bit, 250Mhz interface to FPGA A. Since this chip does nothing more than serializing and 8B/10B encoding, the PCI express protocol will have to be implemented in the logic of FPGA A.

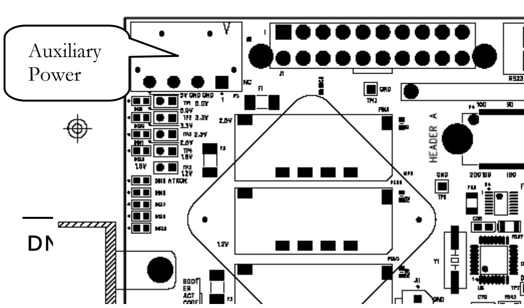
13.3 Virtex 4 FPGA Communication

13.4 PCI clocking

The PX1011A recovers a 100Mhz clock from the PCIexpress edge connector. This clock is used to capture the 2.5Gbs PCI express signal. The parallel interface of the PX1011A is synchronous to the RXCLK signal that

13.5 PCI Power

In some applications, the DN8000K10PCIE can draw its power from the PCI Express slot. The PCI express specification guarentees that the motherboard provide 25W of 12V power for the DN8000K10PCIE to use (Most motherboards provide well in excess of this amount, supplying the power for PCI cards directly from the ATX power supply). In high power applications exceeding 25W, you may need to connect the Auxiliary power connector (P3).

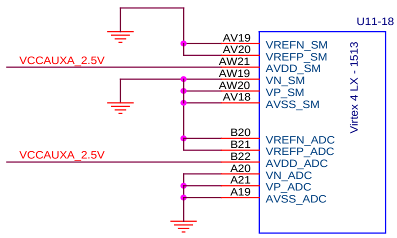


The Aux. Power connector is a standard IDE hard drive power connector and should be supplied by the ATX power supply that is in your computer case. Aux power connector 12V is shorted to the PCI slot 12V. **The power suppy driving the PCI slot and IDE power cable must be the same unit.**

14 FPGA System monitor/ADC

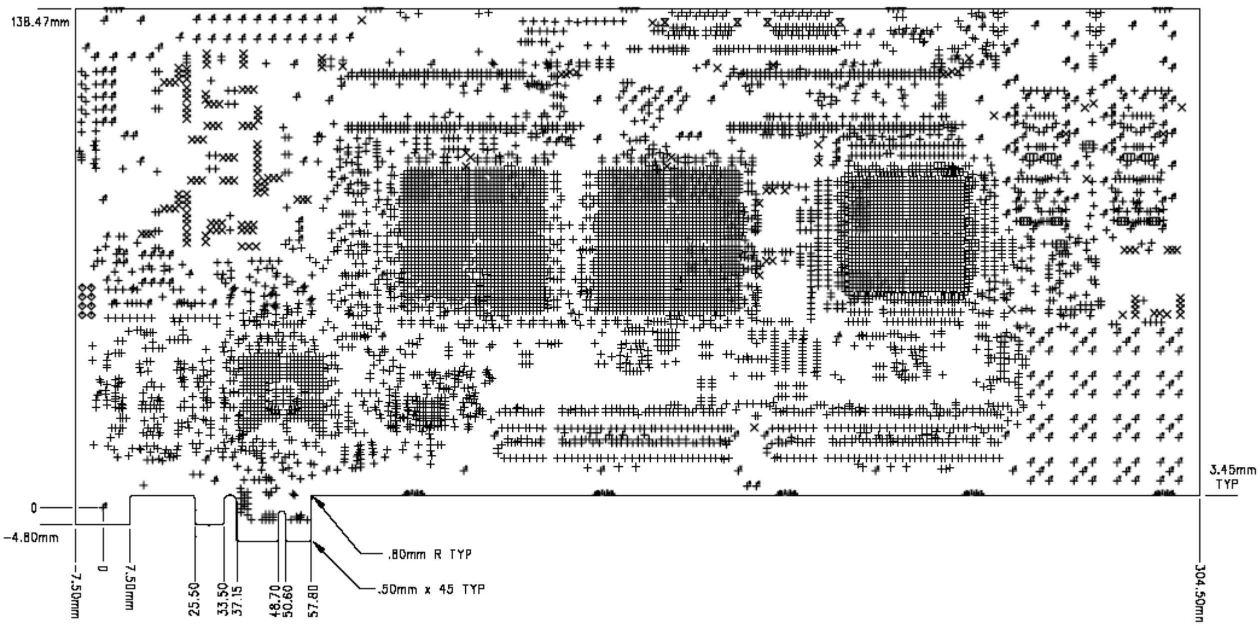
The System Monitor and ADC functions of the Virtex 4 FPGA are no longer supported by Xilinx. The most important responsibility of the System Monitor, temperature sensing, has been moved to the configuration circuitry. The DN8000K10PCIE will automatically monitor and prevent thermal overload in the three Virtex 4 FPGAs. No user action is required.

FPGA A LX 200 Reserved pins



15 Mechanical

The dimensions of the PWB are 312mm long by 135mm tall, plus a 8.25mm PCI edge connector. This is taller than the PCI specification allows, although the DN8000K10PCIE fits easily inside most ATX computer cases.



The topside clearance with the factory installed active heatsinks is 23mm. This leaves just enough room for airflow if the adjacent PCI slot is left unoccupied, or the DN8000K10PCIE is the last PCI card in the row. The default heatsinks can be removed if you do not require high-power operation, allowing the DN8000K10PCIE to meet the PCI height restriction. The back-side clearance is 3.5mm. This exceeds the PCI specification by 1.5mm.

If it is required that the DN8000K10PCIE use only one PCI slot, the fan can be removed from the active heatsink assembly, as long as sufficient airflow is provided. Most PC cases do not provide sufficient airflow for high-power applications.

Chapter
4

Introduction to Virtex 4 and ISE

16 Virtex 4

The Virtex 4 FPGA solution is the most technically sophisticated silicon and software product development in the history of the programmable logic industry. The goal was to revolutionize system architecture "from the ground up." To achieve that objective, the best circuit engineers and system architects from IBM, Mindspeed, and Xilinx co developed the world's most advanced FPGA silicon product. Leading teams from top embedded systems companies worked together with Xilinx software teams to develop the systems software and IP solutions that enabled new system architecture paradigm.

The result is the first FPGA solution capable of implementing high performance system-on-a-chip designs previously the exclusive domain of custom ASICs, yet with the flexibility and low development cost of programmable logic. The Virtex 4 family marks the first paradigm change from programmable logic to programmable systems, with profound implications for leading-edge system architectures in networking applications, deeply embedded systems, and digital signal processing systems. It allows custom user-defined system architectures to be synthesized, next-generation connectivity standards to be seamlessly bridged, and complex hardware and software systems to be co-developed rapidly with in-system debug at system speeds. Together, these capabilities usher in the next programmable logic revolution.

16.1 Summary of Virtex 4 Features

The Virtex 4 has an impressive collection of both programmable logic and hard IP that has historically been the domain of the ASICs.

- High-performance FPGA solution including:
    - Up to Sixteen RocketIO™ embedded multi-gigabit transceiver blocks (based on Mindspeed's SkyRail™ technology)
    - Two IBM® PowerPC™ RISC processor blocks

- Based on Virtex 4 FPGA technology
    - Flexible logic resources, up to 200,448 Logic Cells
    - SRAM-based in-system configuration
    - SelectRAM™ memory hierarchy
    - Up to 556 Dedicated 18-bit x 18-bit multiplier blocks
    - High-performance clock management circuitry
    - SelectIO™-Ultra technology
    - Digitally Controlled Impedance (DCI) I/O

16.2 PowerPC™ 405 Core

- Embedded 300+ MHz Harvard architecture core
- Low power consumption: 0.9 mW/MHz
- Five-stage data path pipeline
- Hardware multiply/divide unit
- Thirty-two 32-bit general purpose registers
- 16 KB two-way set-associative instruction cache
- 16 KB two-way set-associative data cache
- Memory Management Unit (MMU)
    - 64-entry unified Translation Look-aside Buffers (TLB)
    - Variable page sizes (1 KB to 16 MB)
- Dedicated on-chip memory (OCM) interface
- Supports IBM CoreConnect™ bus architecture
- Debug and trace support
- Timer facilities

16.3 RocketIO 10.3 Gbps Transceivers

- Full-duplex serial transceiver (SERDES) capable of baud rates from 622 Mb/s to 10.3 Gb/s (please reference the Xilinx publication DS302 for speed grade limitations) Initial availability is 3.125Gb/s.
- Monolithic clock synthesis and clock recovery (CDR)
- Fibre Channel, 10 Gigabit Ethernet, PCI Express, 10 Gb Attachment Unit Interface (XAUI), and Infiniband-compliant transceivers

- 8-, 16-, 32- or 64-bit selectable parallel internal FPGA interface
- 8B /10B and 64B/68B encoder and decoder
- 50/75 on-chip selectable transmit and receive terminations
- Programmable comma detection
- Channel bonding support (two to sixteen channels)
- Rate matching via insertion/deletion characters
- Four levels of selectable pre-emphasis
- Five levels of output differential voltage
- Per-channel internal loopback modes
- 2.5V transceiver supply voltage

16.4 Virtex 4 FPGA Fabric

Description of the Virtex 4 Family fabric follows:

- SelectRAM memory hierarchy
  - Up to 9 Mb of True Dual-Port RAM in 18 Kb block SelectRAM resources
  - Up to 1.7 Mb of distributed SelectRAM resources
  - High-performance interfaces to external memory
- Arithmetic functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible logic resources
  - Up to 111,232 internal registers/latches with Clock Enable
  - Up to 111,232 look-up tables (LUTs) or cascadable variable (1 to 16 bits) shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and Sum-of-Products support
  - Internal 3-state busing
- High-performance clock management circuitry
  - Up to eight Digital Clock Manager (DCM) modules
    - Precise clock de-skew
    - Flexible frequency synthesis

        - High-resolution phase shifting
    - 16 global clock multiplexer buffers in all parts
- Active Interconnect technology
    - Fourth-generation segmented routing structure
    - Fast, predictable routing delay, independent of fanout
    - Deep sub-micron noise immunity benefits
- Select I/O-Ultra technology
    - Up to 960 user I/Os
    - 57 supported IO standards including eight differential standards
    - Programmable LVTTL and LVCMOS sink/source current (2 mA to 48 mA) per I/O
    - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
    - PCI support(1)
    - Differential signaling
        - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
        - Bus LVDS I/O
        - HyperTransport™ (LDT) I/O with current driver buffers
        - Built-in DDR input and output registers
    - Proprietary high-performance SelectLink technology for communications between Xilinx devices
        - High-bandwidth data path
        - Double Data Rate (DDR) link
        - Web-based HDL generation methodology
- SRAM-based in-system configuration
    - Fast SelectMAP™ configuration
    - Triple Data Encryption Standard (DES) security option (bitstream encryption)
    - IEEE1532 support
    - Partial reconfiguration
    - Unlimited reprogrammability
    - Readback capability

- Supported by Xilinx Foundation™ and Alliance™ series development systems
    - Integrated VHDL and Verilog design flows
    - ChipScope™ Pro Integrated Logic Analyzer
- 0.13-µm, nine-layer copper process with 90 nm high-speed transistors
- 1.5V (VCCINT) core power supply, dedicated 2.5V VCCAUX auxiliary and VCCO power supplies
- IEEE 1149.1 compatible boundary-scan logic support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) packages in standard 1.00 mm pitch
- Each device 100% factory tested

17 Foundation ISE 7.1i

ISE Foundation is the industry's most complete programmable logic design environment. ISE Foundation includes the industry's most advanced timing driven implementation tools available for programmable logic design, along with design entry, synthesis and verification capabilities. With its ultra-fast runtimes, ProActive Timing Closure technologies, and seamless integration with the industry's most advanced verification products, ISE Foundation offers a great design environment for anyone looking for a complete programmable logic design solution.

17.1 Foundation Features

17.1.1 Design Entry

ISE greatly improves your "Time-to-Market", productivity, and design quality with robust design entry features. ISE provides support for today's most popular methods for design capture including HDL and schematic entry, integration of IP cores as well as robust support for reuse of your own IP. ISE even includes technology called IP Builder, which allows you to capture your own IP and reuse it in other designs.

ISE's Architecture Wizards allow easy access to device features like the Digital Clock Manager and Multi-Gigabit I/O technology. ISE also includes a tool called PACE (Pinout Area Constraint Editor), which includes a front-end pin assignment editor, a design hierarchy browser, and an area constraint editor. By using PACE, designers are able to observe and describe information regarding the connectivity and resource requirements of a design, resource layout of a target FPGA, and the mapping of the design onto the FPGA via location/area.

This rich mixture of design entry capabilities provides the easiest to use design environment available today for your logic design.

17.1.2 Synthesis

Synthesis is one of the most essential steps in your design methodology. It takes your conceptual Hardware Description Language (HDL) design definition and generates the logical or physical representation for the targeted silicon device. A state of the art synthesis engine is required to produce highly optimized results with a fast compile and turnaround time. To meet this requirement, the synthesis engine needs to be tightly integrated with the physical implementation tool and have the ability to proactively meet the design timing requirements by driving the placement in the physical device. In addition, cross probing between the physical design report and the HDL design code will further enhance the turnaround time.

Xilinx ISE provides the seamless integration with the leading synthesis engines from Mentor Graphics, Synopsys, and Synplicity. You can use the synthesis engine of your choice. In addition, ISE includes Xilinx proprietary synthesis technology, XST. You have options to use multiple synthesis engines to obtain the best-optimized result of your programmable logic design.

17.1.3 Implementation and Configuration

Programmable logic design implementation assigns the logic created during design entry and synthesis into specific physical resources of the target device.

The term "place and route" has historically been used to describe the implementation process for FPGA devices and "fitting" has been used for CPLDs. Implementation is followed by device configuration, where a bitstream is generated from the physical place and route information and downloaded into the target programmable logic device.

To ensure designers get their product to market quickly, Xilinx ISE software provides several key technologies required for design implementation:

- Ultra-fast runtimes enable multiple "turns" per day
- ProActive™ Timing Closure drives high-performance results
- Timing-driven place and route combined with "push-button" ease
- Incremental Design
- Macro Builder

17.1.4 Board Level Integration

Xilinx understands the critical issues such as complex board layout, signal integrity, high-speed bus interface, high-performance I/O bandwidth, and electromagnetic interference for system level designers.

To ease the system level designers' challenge, ISE provides support to all Xilinx leading FPGA technologies:

- System IO
- XCITE

- Digital clock management for system timing
- EMI control management for electromagnetic interference

To really help you ensure your programmable logic design works in context of your entire system, Xilinx provides complete pin configurations, packaging information, tips on signal integration, and various simulation models for your board level verification including:

- IBIS models
- HSPICE models
- STAMP models

18 Virtex 4 Developer's Kit

V2PDK is the Virtex 4 Developer's Kit, and is included to provide an existing framework of hardware and software code to explore the capabilities of the Virtex 4, as well as a basis to build new systems.

A wide variety of software and hardware tools are used to build a Virtex 4™ design. V2PDK The design flow is a tool chain methodology that exists to simplify the entire design process by providing integration between the tools and automating tasks. The main focus of the design flow is integrating the programs with each other to accomplish the system design.

The system design process can be loosely divided into the following tasks:

- Builds the software application
- Simulates the hardware description
- Simulates the hardware with the software application
- Simulates the hardware into the FPGA using the software application in on-chip memory
- Runs timing simulation
- Configures the bitstream for the FPGA

19 Helpful HInts

Make sure that the clock your design uses is running.
> Check the pinout in your constraint file. Check the .PAR report file to
> make sure that 100% of your IOBs used have LOC constraints. Use the .PAD
> report to make sure your constraints were applied correctly.
> Double-check that the connections match between your FPGA pins and the
> daughtercard pins.
> Make sure that none of the other FPGAs are driving those MB pins. Check for
> logic in your source code, and make sure that the "Unused IOBs" option in
> the ISE settings is set to "Float." If it is set to "Pulldown," then those
> FPGAs are driving any pin that is not assigned in the source code.
> If the connections are on J3 and/or J4 on the daughtercard, make sure the OE
> pins on the daughtercard buffers are active.

Chapter

5

Introduction to the Reference Design

This chapter introduces the DN8000K10PCIE Reference Design, including information on what the reference design does, how to build it from the source files, and how to modify it for another application.

1 Exploring the Reference Design

1.1 What is the Reference Design?

The reference design is a fully functional Virtex 4 FPGA design capable of demonstrating most of the features available on the DN8000K10PCIE. Features exercised in the reference design include:

- Access to the DDR2 SDRAM Modules At 200Mhz
- UART Communication
- FPGA Interconnect
- Interaction with the Configuration FPGA and MCU
- Use of Embedded PowerPC Processors (eventually)
- Memory Mapped Access Between PPC And User Design (eventually)
- Access to external LEDs
- Communication via Rocket I/O Transceivers
- Instantiation of Daughter Card Test Headers
- USB memory map to DDR2 memory.
- Pin-multiplexed FPGA interconnect using LVDS at 650Mbs per signal pair

All source code for the reference design is included on the CD and may be used freely in customer development. Precompiled bit files for the most common stuffing options are also included and can be used to verify board functionality before beginning development. A build utility, described in the section Compiling The Reference Design, can be used to generate new bit files, or to generate bit files for less common configurations of the DN8000K10PCIE.

The reference design was created using

Here are the default main.txt file lines.

```
 verbose level: 2
sanity check: y
 clock frequency: A N 4 M 16 // 100 MHz – not used for PCI/MB test,
header test uses this clk
 clock frequency: B N 2 M 28 // 200 MHz
 clock frequency: D N 2 M 25 //  200 MHz
 clock frequency: 1 N 2 M 25 // 312 MHz
 clock frequency: 2 N 2 M 25 // 312 MHz
```

2 Reference Design Memory Map

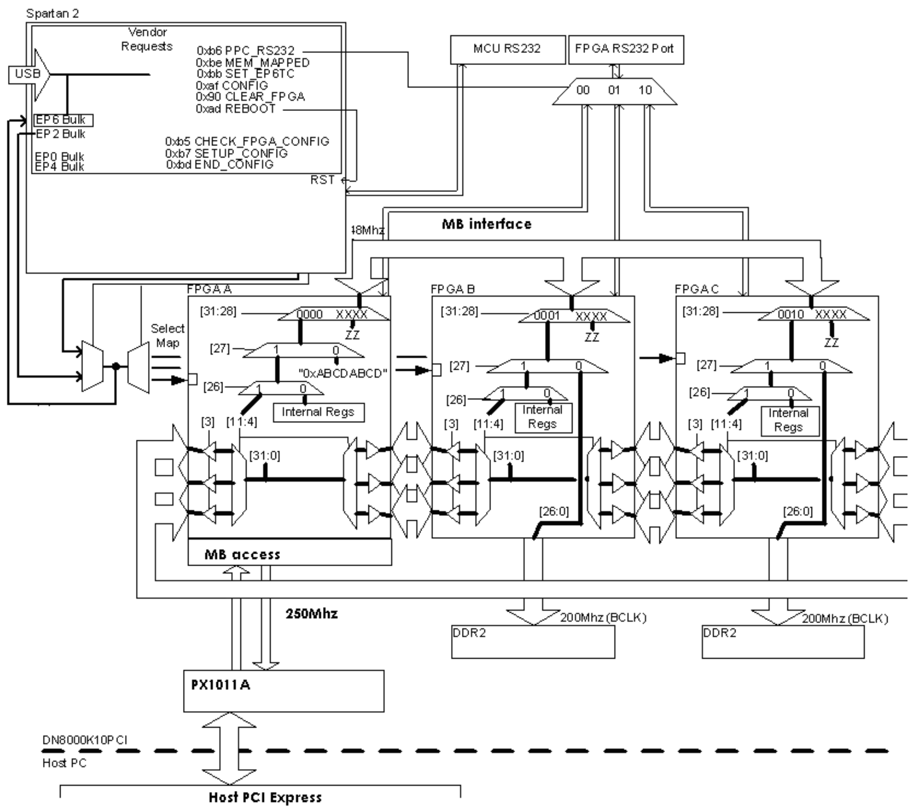
The Dini Group reference design memory maps the main features of the DN8000K10PCIE to the host interfaces: PCI, USB, and RS232.

The Main Bus interface is used to access the reference design memory map. Addresses are 32-bits. Each address contains a 32-bit word.

FPGA A	0x08000002	IDCODE	0x05000121
FPGA A	0x08000004	INTERCONTYPE	0x34561111
FPGA A	0x08000006	RWREG	Scratch Register for testing
FPGA A	0x08000010	LED_OE	Controls LED output enables
FPGA A	0x08000011	LED_OUT	Controls LED outputs
FPGA A	0x08100001	CLK_COUNTER	Contains contents of ACLK counter
FPGA A	0x08100002	CLK_COUNTER	Contains contents of BCLK counter
FPGA A	0x08100003	CLK_COUNTER	Contains contents of DCLK counter
FPGA A	0x08100004	CLK_COUNTER	Contains contents of SYSCLK counte
FPGA A	0x0C000000	ABP0 OUT	W; the output state of FPGA IOs connected to the ABP0 interconenct bus
FPGA A	0x0C000004	ABP0 OE	W; The ouput enable of each FPGA

			IO on the ABP0 interconnect bus.
FPGA A	0x0C000008	ABP0 IN	The input state of each FPGA IO…
			…on the ABP0 interconnect bus
FPGA A	0x0C00000C	ABP0 Name	"ABP0" (ascii)
FPGA A	0x0C000010	ABP1 OUT	W; ABP1 IO output values
FPGA A	0x0C000014	ABP1 OE	W; Output enable of ABP1 bus
FPGA A	0x0C000018	ABP1 IN	R; ABP1 input values
FPGA A	0x0C00001C	ABP1 Name	"ABP1" (acsii)
FPGA A	0x0C000XX0	BUS XX OUT	XX can be 0-21 hex. Output status of IOs on bus XX.
FPGA A	0x0C000XX4	BUS XX OE	XX can be 0-21 hex. OE status of IOs
FPGA A	0x0C000XX8	BUS XX IN	XX can be 0-21 hex. The input values
FPGA A	0x0C000XXC	BUS XX Name	The name of the bus XX (schematic)
FPGA B	0x10000000 -	DDR2 B space…	Mapped to DDR2 SODIMM…
FPGA B	0x17FFFFFF	…	…interface
FPGA B	0x18000002	IDCODE	0x05000121
FPGA B	0x18000004	INTERCONTYPE	0x34561111
FPGA B	0x18000006	RWREG	Scratch Register for testing
FPGA B	0x18000010	LED_OE	Controls LED output enables
FPGA B	0x18000011	LED_OUT	Controls LED outputs
FPGA B	0x18100001	CLK_COUNTER	Contains contents of ACLK counter
FPGA B	0x18100002	CLK_COUNTER	Contains contents of BCLK counter
FPGA B	0x18100003	CLK_COUNTER	Contains contents of DCLK counter
FPGA B	0x18100004	CLK_COUNTER	Contains contents of SYSCLK counte
FPGA B	0x18000001	DDR2HIADDR	upper address bits for DDR2 interface
FPGA B	0x18000003	HIADDRSIZE	number of bits in DDR2HIADDR
FPGA B	0x18000005	DDR2SIZEHIADDR	The size of the DDR2 module.
FPGA B	0x18000007	DDR2TAPCNT0	Current IDELAY values of DDR2…
FPGA B	0x18000008	DDR2TAPCNT1	…interface
FPGA B	0x1C000XX0	BUS XX OUT	XX can be 0-21 hex. Output status of IOs on bus XX.
FPGA B	0x1C000XX4	BUS XX OE	XX can be 0-21 hex. OE status of IOs
FPGA B	0x1C000XX8	BUS XX IN	XX can be 0-21 hex. The input values
FPGA B	0x1C000XXC	BUS XX Name	The name of the bus XX (schematic)
FPGA C	0x20000000-	DDR2 C space…	Mapped to DDR2 SODIMM…
FPGA C	0x27FFFFFF	…	… interface
FPGA C	0x28000002	IDCODE	0x05000121
FPGA C	0x28000004	INTERCONTYPE	0x34561111
FPGA C	0x28000006	RWREG	Scratch Register for testing

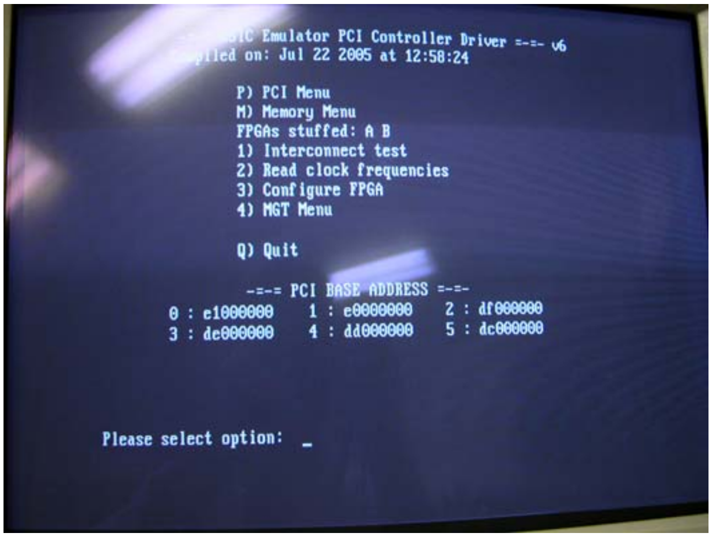
FPGA C	0x28000010	LED_OE	Controls LED output enables
FPGA C	0x28000011	LED_OUT	Controls LED outputs
FPGA C	0x28100001	CLK_COUNTER	Contains contents of ACLK counter
FPGA C	0x28100002	CLK_COUNTER	Contains contents of BCLK counter
FPGA C	0x28100003	CLK_COUNTER	Contains contents of DCLK counter
FPGA C	0x28100004	CLK_COUNTER	Contains contents of SYSCLK counte
FPGA C	0x28000001	DDR2HIADDR	upper address bits for DDR2 interface
FPGA C	0x28000003	HIADDRSIZE	number of bits in DDR2HIADDR
FPGA C	0x28000005	DDR2SIZEHIADDR	The size of the DDR2 module.
FPGA C	0x28000007	DDR2TAPCNT0	Current IDELAY values of DDR2…
FPGA C	0x28000008	DDR2TAPCNT1	…interface



2.1 Using the Reference Design

2.1.1 Built-In RocketIO test

From the AETest main menu, select option 4, MGT Menu. The MGT test sends a repeating test pattern out all of the RocketIO transmit pairs, and compares the input of each RocketIO channel to that pattern. To run the test, you must loop back each RocketIO pair.



You can easily loopback the SMA channels by connecting the RX and TX connectors of each MGT pair together with an SMA cable. The SFP modules can be tested with an LR loopback attenuator.

Option 5 of the MGT menu allows you to invert the polarity of one of the SFP channels. For the test to pass, this must be done, since SFP2 is received with inverted polarity.

The MGT tiles are connected as follows

	MGT A	MGT B
COL0, TILE0	QSE 1	QSE 1
COL0, TILE1	QSE 1	QSE 1
COL0, TILE2	SFP 1 (XFP REFCLK1)	XFP 1
COL0, TILE3	LOOPBACK	SMA J22
COL1, TILE0	QSE 0	QSE 0
COL1, TILE1	SMA J31	SMA J25
COL1, TILE2	NC	SMA J17
COL1, TILE3	XFP 2	SFP 2

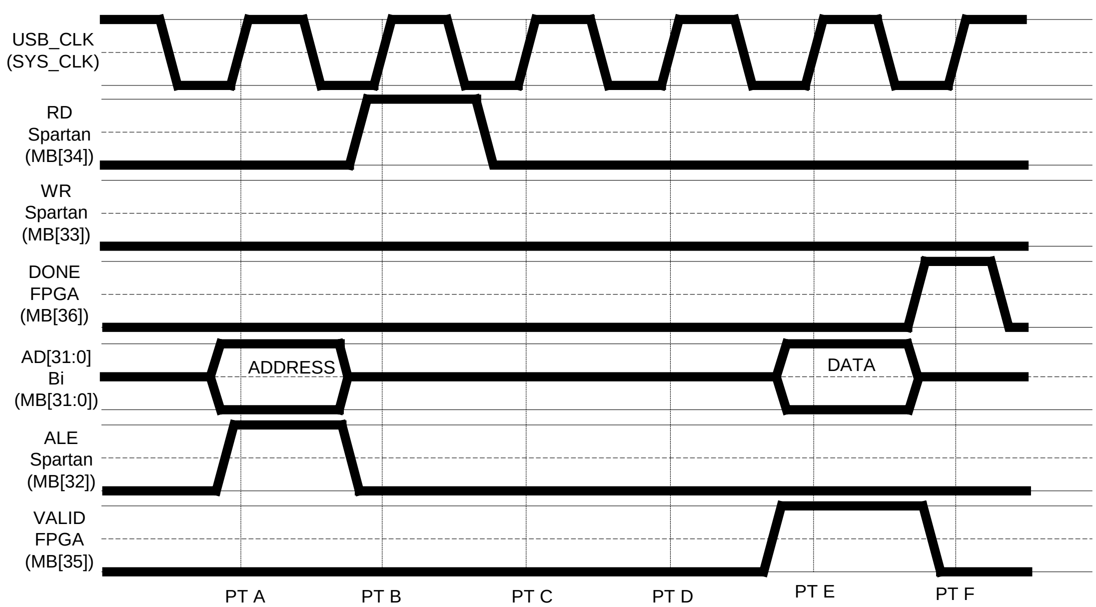
REFCLK2 – 250MHz EPSON

REFCLK1 – ICS 84020 Synthesizer

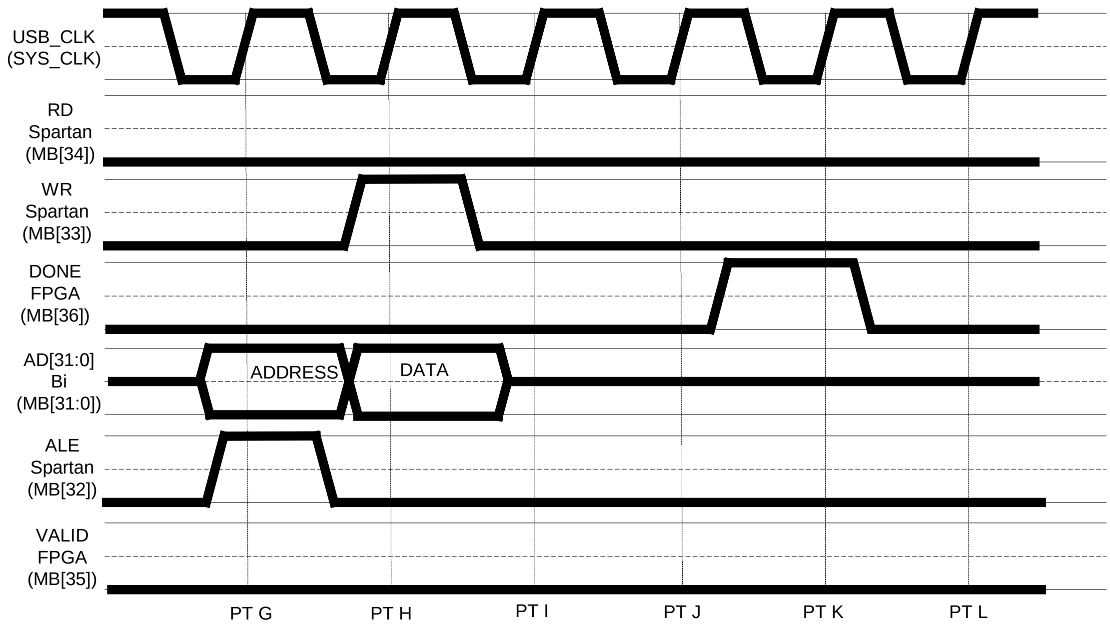
```
******************
FPGA_A: MAIN MENU
******************

a) Run Full Test Suite
b) Test Registers
c) Test SRAM
d) Test DDR
e) Test Interconnect
f) Write Memory Location
g) Read Memory Location
h) Display Memory in 8 DWORDS per Line Format
i) Fill Memory with specified DWORD pattern
j) Toggle Mem Owner: INTERNAL (User)
k) Interconnect Test Menu

q) Quit
```

3 Memory Mapped Data flow

All memory mapped transactions in the reference design occur over the MB bus. This 40-signal bus connects to all Virtex 4 FPGAs and to the Spartan II configuration FPGA. All access to the MB bus is initiated by the Spartan II FPGA when the reference design is in use.



Here is a write



3.1 Compiling the Reference Design

This section deals with the source code to the Reference Design, which can be found on the CD-ROM. All file references are with respect to the root directory of the Reference Design source code (/source/FPGA). Files that are specific to the DN8000K10PCIE design are found in the DN8000K10PCIE subdirectory, whereas general application code is found in the common subdirectory.

3.1.1 The Xilinx Embedded Development Kit (EDK)

The Reference Design uses the Xilinx EDK to instantiate an embedded PowerPC Processor. The EDK project can be found at 'DN8000K10PCIE/PPC/system.xmp' and can be opened and modified with the Xilinx Embedded Development Kit software.

3.1.2 Synplicity Synplify

The Dini Group uses Synplicity's Synplify software to for design synthesis. The Synplicity projects for each of the 3 FPGAs on the DN8000K10PCIE can be found at 'DN8000K10PCIE/synthesis/*.prj'. These projects have been compiled using Synplify Pro version 7.3.

3.1.3 Xilinx ISE

3.1.4 The Build Utility: Make.bat

The Build Utility is found at 'DN8000K10PCIE/build/make.bat'. This batch file is used to set system parameters to the desired configuration (i.e. V4FX60 vs. V4FX100, etc.), and to invoke all of the above tools from the command line. Instructions for invoking the batch file can be found by viewing the batch file with a text editor. Additional information about using the batch file to build the reference design is found below. Taking the reference design through all of the various tools for several FPGA's can be very tedious and time consuming- this batch file can do it all in one command!

The command line utility "Make.bat" is an MS-DOS batch file compatible with Windows 2000 and later operating systems. Make.bat should be run from the command line, with command line parameters. It should not be double clicked from the windows environment. A command prompt shortcut is provided in the same directory as Make.bat, and can be double clicked to open a command prompt window with the proper working directory.

4 Getting More Information

4.1 Printed Documentation

The printed documentation, as mentioned previously, takes the form of a Virtex 4 datasheet and a DN8000K10PCIE User Guide.

4.2 Electronic Documentation

Multiple documents and datasheets have been included on the CD.

4.3 Online Documentation

There is a public access site that can be found on the Dini Group web site at http://www.dinigroup.com/.

Chapter

9

Ordering Information

Part Number

DN8000K10PCIE

5 FPGA Options

5.1 FPGA A:

Select an FPGA part to be supplied in the A position. This FPGA is connected to the PCI bus, an expansion header, and can source global clocks. The –12 speed grade is required for full speed operation (1Gbs/pair) of the interconnect between fpgas.

NONE

LX100 –10 –11 –12

LX160 –10 –11 –12

LX200 –10 –11

5.2 FPGA B:

Select an FPGA part to be supplied in the B position. This FPGA is connected to an expansion header, a memory module socket, and can source global clocks. The –12 speed grade is required for full speed operation (1Gbs/pair) of the interconnect between FPGAs.

NONE

LX100 –10 –11 –12

LX160 –10 –11 -12

LX200 –10 –11

5.3 FPGA C:

Select an FPGA part to be supplied in the C position. This fpga is connected to a momory module socket. This FPGA is required to provide Multi-Gigabit serial communication. In order to achieve 10 Gbs selectIO operation, the –12 speed grade is required.

NONE

FX40 –10 –11 -11x –12 (This option makes the 200-pin SODIMM memory socket, one SMA channel and one QSE cable channel unusable)

FX60 –10 – 11 -11x –12 (This option makes one channel of SMA and one channel of 5Gb QSE cable unusable)

FX100 –10 –11 -11x –12

6 Multi-Gigabit Serial Options

6.1 Serial Clock Crstals

If you need to interface to a specific Multi-gigabit serial IO protocol, you may want to specify a compatible crystal. For information on the impact of the selected crystal option, see Appendix X, Clock configuration.

Chose one of the following frequencies (in Mhz):

9.8304
12.890
14.318
16.000
21.477
24.576
25.000

The default option is 25.000 Mhz.

6.2 Module Sockets

XFP and SFP Modules provide 1.0 – 10.5 Gb optical serial communications to FPGA C. DN8000K10PCIE has two optical ports, each can be installed with either an SFP or XFP connector. XFP modules operate only in the 9.5-10.5 Gb/s range. Available SFP modules operate between 1-4.25 Gb/s. For 10Gb operation, a –12 speed grade FX part may be required. These parts may not yet be available before.

If you have the FPGA C option, you may select one of the following options.

OPTICAL – SFP, SFP (default)

OPTICAL – XFP, XFP

OPTICAL – SFP, XFP

7 Other Options

7.1 3.3 V Headers

The DN8000K10PCIE can be configured to accept 3.3V input and output on a *subset of expansion header pins*. These IOs are not voltage selectable by the software. You must specify on your order that you would like this option. For a list of header pins that can be used in 3.3V interfaces, see Appendix A, FPGA pins.

Select any of the following options. The default option is all 2.5V header IO.

3.3V Header A

3.3V Header B

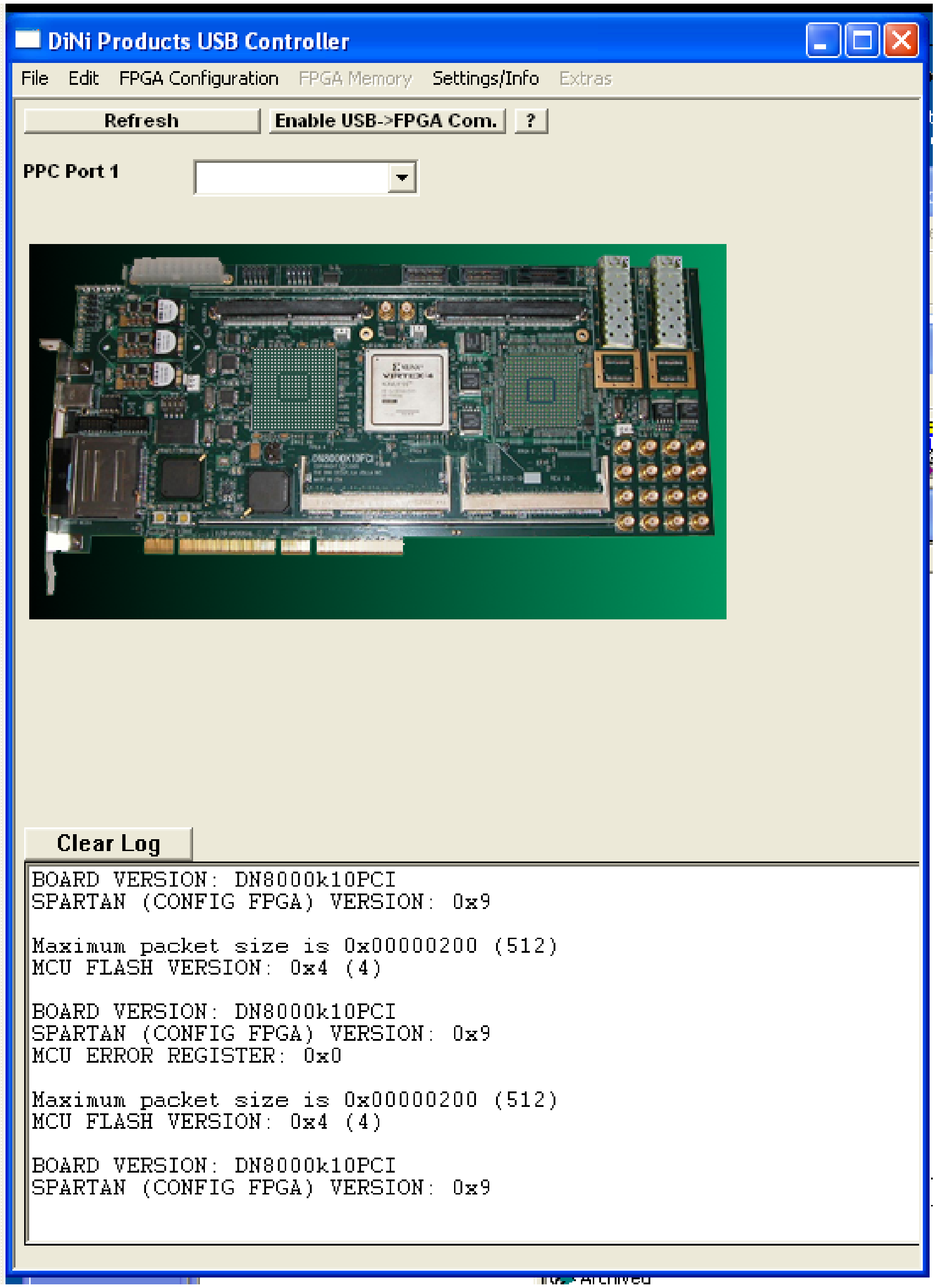
7.2 12V Power

Daughtercard supply voltages +12V and –12V are, by default, disabled by jumpers R411 (Header A +12V), R412 (Header B +12V), R414 (Header A –12V), R413 (Header B –12V). This default setting reduces the chance of damage to the Virtex 4 FPGA IO buffers due to user error or careless use of probes. Specify this option to have the jumpers factory installed.

8 Optional Equipment

The Dinigroup supplies standard daughtercards and memory modules that you can use with the DN8000K10PCIE.

- SE card – 80 signals on .1" pitch headers.
- Mictor Card – 5 Mictor38 headers for use with logic analyzers.
- SRAM module for use in the 200-pin SODIMM sockets of the DN8000K10PCIE. QDRII, 300Mhz 64x2Mb
- SRAM module for use in the 200-pin SODIMM socket. 64x2Mb Standard SDR SRAM. Pipelined or Flowthrough, NoBL available
- RLDRAM module for use in the 200-pin SODIMM socket. 64x16Mb, 300Mhz DDRII
- Flash module for use in the 200-pin SODIMM header.
- Mictor module for use in the 200-pin SODIMM header. (2 Mictor 38 connectors for use with logic analyzer)



The Dini Group can optionally provide the following accessories

- DN3k10SD Daughter card (Provides tenth inch pitch test points)

- DNMictor Daughter card (Provides 5 Mictor connectors compatible with logic analyzers)

- Memory modules for use in the DN8000K10PCIE DDR2 SODIMM sockets A and B. (Available Q4 '05)

  - QDRII SRAM 64x1Mb, 300Mhz
  - Flash memory 32x4Mb, 2x4Mb serial flash
  - Reduced Latency DRAM (RLDRAM) 64x8Mb, 300Mhz
  - Standard SRAM, 64x2M (Select ZBT, Pipelined, Flowthrogh)
  - Test connection module (with two Mictor38)

You may also want to obtain from a third party vendor

- 200-pin DDR2 SODIMM(s)

- SFP modules (for Gigabit Ethernet, infiniband, …)

  IBM part 13N1796 from insight.com $180

- XFP modules

  Intel part TXN181070850X18 from insight.com $692

  XFP heatsink/clip – Tyco part 1542992-2

  -5.2V bench supply for powering ECL-based XFP modules (if required)

- Xilinx Parallel IV cable

- LVPECL oscillators for RocketIO MGT clocking. (The DN8000K10PCIE is supplied with a 250Mhz oscillator)

  Epson Part EG-2102CA PECL

Synplicity Identify, or Xilinx Chipscope for embedded logic analyzer functionality.