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Designer & User Guide

for

ANSI/VITA 23-1998

VME64 Extensions for Physics and Other Applications (VME64xP)

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by the
VMEbus Standards Organization

U. S. Department of Energy
Office of Science
Division of High Energy Physics

Foreword

This document serves as a guide for design and implementation of VMEbus components and systems as described in VITA 23-1998, “VME64 Extensions for Physics and Other Applications (VME64xP)” issued by the VITA Standards Organization (VSO). It will be useful also to users and designers of other VMEbus instrumentation. The information contained herein is to be updated as necessary.

This document was developed by the NIM Committee (supported by the U. S. Department of Energy), consisting of representatives of the U.S. National Laboratories and other major laboratories. Representatives of the VME Standards Organizations (VSO), ESONE Committee of European Laboratories, as well as of individual European, Canadian and Japanese Laboratories have also contributed to the development.

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1 Introduction

1.1. General

This document serves as a guide for design and implementation of VMEbus[1] components and systems as described in VITA 23-1998, “VME64 Extensions for Physics and Other Applications (VME64xP)” issued by the VITA Standards Organization (VSO). It will be useful also to users and designers of other VMEbus instrumentation.

1.2. Compatibility Issues

VME64xP Modules are compatible with all members of the VMEbus family. This is the core of the ‘backwards compatibility’ VSO mandates in VMEbus systems such that new devices may take advantage of new features or protocols but are still required to comply with all previous versions of the standard. There are issues of compatibility with secondary (P2/J2 and/or P0/J0) buses for VMEbus devices. VME64xP Modules have the same compatibility problems when connecting to the user defined pins. The system integrator must be aware of these issues and properly configure the system. The availability of keying can help insure that the Modules are not installed in incorrect slots.

This chapter first briefly summarizes the various addressing and data transfer protocols that have been developed as VMEbus standards. This Chapter then addresses specific items regarding addressing, Control/Status Register (CSR) assignments and Configuration ROM (CR) assignments for VME64xP Modules. For a complete description of CR/CSR space the user is referred to VME64, Chapter 2 and VME64x, Chapter 9.

Modules that implement the VME64x standard and/or the VME64xP standard will not be able to utilize some VME64x features in older VMEbus systems. Most of the difficulty occurs due to the older systems using the 3-row connector and not providing the extra signals available on the ‘z’ and ‘d’ rows of J1, the ‘z’ and ‘d’ rows of J2, and the J0 connector. The following bullets highlight the differences and indicate which features are still available to the new Modules in older systems.

- The +V and –V (nominally 48 V) supplies defined in the VME64x standard will not be present in older subracks. This will disable any Modules that depend upon that supply for DC-DC converter power.
- The +3.3 V supply defined in the VME64x standard will not be present in older subracks. Modules dependent upon +3.3 V power can, however, derive it from the VMEbus +5 V supply by use of an internal regulator or DC-DC converter.
- The lack of Geographic Address pins in older subracks will require that a bus Master or Monarch load the CR/CSR Base Address Register.
- Live Insertion capability is not supported in older subracks.
- Test and Maintenance Bus features are not supported in older subracks.
- The lack of the RTRY* line disables the use of the 2eVME and 2eSST protocol for Slave Termination.
- The lack of the J0 connector makes the user defined voltages Vw, Vx, Vy and Vz unavailable.

1. The lack of the J0 connector reduces the amount of +5 V current that can be supplied to the Module since the six additional +5 V pins on J0 are not available.

[1] Term used herein for VME family of buses (VME, VME64, VME64x, *etc*.)

1.3. Chapter Content Summary

- **Chapter 1 (Introduction)** This Chapter.
- **Chapter 2 (Reference Standards and Resources)** List of reference documents.
- **Chapter 3 (Module Logical Implementation)** This comprehensive Chapter is must reading for both designers and users of VMEbus Modules. It discusses addressing modes and bus cycles, CR/CSR Registers, Base Address registers and data transfers. It is closely related to Chapter 3 of VITA 23.
- **Chapter 4 (VME64xP Modules)** This Chapter provides useful information for designers and users of **VME64xP** Modules. It deals with details of Module construction, powering, protection and cooling of the Modules. It is closely related to Chapter 4 of VITA 23.
- **Chapter 5 (VME64xP Transition Modules)** This Chapter deals with construction details of **VME64xP** Transition Modules. It is closely related to Chapter 4 of VITA 23.
- **Chapter 6 (Mezzanine Cards and Carriers)** This Chapter provides detailed information regarding mezzanine cards that attach to Module circuit boards through connector pairs. Characteristics and use of PMC and IP Modules are discussed briefly as are power, temperature and cooling considerations. It is closely related to Chapter 5 of VITA 23.
- **Chapter 7 (VME64xP Subracks)** This Chapter includes recommendations and observations regarding construction of **VME64xP** subracks. It discusses power buses and connections, including the power supply attachment bulkhead, as well as remote sense connections, and subrack cooling. It is closely related to VITA 23, Chapter 6 and Appendices A and B.
- **Chapter 8 (Subrack Power)** This Chapter provides information regarding voltages on the backplane and recommended configurations for providing power for ECL logic. It is closely related to Chapter 7 of VITA 23.
- **Chapter 9 (Rack System Configuration)** This Chapter will be of interest to the system integrator who has responsibility for assembling the subracks and racks into a safe and well coordinated operating system. Guidelines are provided regarding cooling and protection.
- **Chapter 10 (DC-DC Converters: Usage Guidelines)** The use of on-board DC-DC converters has been strongly encouraged. This Chapter provides useful guidelines for their selection and implementation.
- **Chapter 11 (Analog Module Design Considerations)** This Chapter discusses analog circuit design, achievable performance levels, noise considerations, power provision, use of DC-DC converters, shielding and isolation, and other matters that need attention in design and implementation of analog circuits, particularly high resolution circuits.
- **Chapter 12 (EMC/ESC Considerations)** This Chapter is concerned with (1) the design, construction and connection of Modules and subracks for electromagnetic compatibility (EMC) to limit electromagnetic radiation and electromagnetic interference (EMI), and with (2) electrostatic discharge (ESD) from boards prior to their mating with the backplane in order to protect the boards and the integrity of data on the bus.
- **Chapter 13 (Useful Documents)** This Chapter includes a list of VITA, IEEE, IEC and other documents which may be useful to system implementers. A short description is included for each document.

- **Chapter 14 (I/O Connections - Physical)** This Chapter is concerned with interconnection methods for digital signals. It discusses ECL, NIM, LVDS, PECL, RS-422A and RS-485 signals, as well as the associated cables and connectors.

- **Chapter 15 (Components)** This Chapter is a compilation of available components including connectors, connector hardware and driver, receiver, and interface ICs used with VMEbus equipment.

1.4. Definitions, Ground, Earth, etc.

The following terms relate to ground, zero volts and other terms that may be used in confusing ways. The following are the definitions as used in this document.

- Ground (GND): A wire, conductor or plane which provides the path for current to return to the power supply from the circuit. A GND is not Earth as sufficient current through GND can cause it to develop voltage differences from other returns in the power supply system. Typically return current from digital circuitry flows through GND. Ideally GND is connected to Earth in only one place in a system.

- Earth Ground (Earth): A point used as a base reference for multiple subsystems and, if used, is typically provided through a long conductive rod driven into the soil to provide sub-milliohm resistance. A point of minimum potential in the circuit that does not appreciably vary with changes in current through the point. See also VME64x, Section 8.2.5 for resistances in Earth and GND as related to safety.

- Reference Voltage: This is a voltage used in analog circuitry as a reference to which other signals are compared. The reference circuit ideally has no current flow. Since no current flows, this point is very stable under all conditions and the same voltage at all points.

- Shield: The conductive case that surrounds electronics and serves to inhibit the radiation or reception of EMI. It is typically connected to Earth.

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2 Reference Standards and Resources

The information below should help a user when building and/or using VME64, VME64x and VME64xP compatible subracks, modules and transition modules. VITA documents may be ordered from the VMEbus International Trade Association office. The information can be found at: http://www.vita.com/publist.html

2.1 Reference Specifications

The following documents are referenced herein. (All IEC documents have the new numbering system that adds 60000 to previous numbers.)

- VITA 1-1994: VME64 Specification
- VITA 1.1-1997 VME64 Extensions (VME64x)
- VITA 1.2-199x: High Availability VMEbus Draft Specification
- VITA 1.3-1997: VME64x 9U x 400 mm Format (VME64x9U)
- VITA 1.4-199x: VME64x Live Insertion Draft Specification (VME64xLI)
- VITA 2-199x: ETL Specification, Draft 0.5, 22 August 1997
- IEEE 1014: Versatile Backplane Bus 1987 (original VME standard)
- IEEE 1101.1: IEEE Standard for Mechanical Core Specifications for Microcomputers using IEC 60603-2 Connectors, 26 September 1991
- IEEE 1101.10: IEEE Standard for additional Mechanical Specifications for Microcomputers using the IEEE 1101.1 Equipment Practice, 1996
- IEEE 1101.11: IEEE Proposed Standard for Mechanical Rear Plug-in Unit Specifications for Microcomputers using the IEEE 1101.1 and IEEE 1101.10 Equipment Practice,x 30 June 1998
- IEC 60821: International Electrotechnical Commission equivalent of IEEE 1014

2.2 Other Standards

- IEC 61076-4: Connectors with Assessed Quality, for use in DC Low Frequency Analog and in High Speed Data Applications - Part 4: Sectional Specification - Printed Circuit Connectors
- IEC 60603-2: Connectors for Frequencies below 3 MHz for use with Printed Circuit Boards - Part 2: Detailed Specification for Two-Part Connectors with Assessed Quality, for Printed Circuit Boards, for Basic Grid of 2.54 mm (0.1 in) with Common Mounting Features
- IEC 60297-1: Dimensions of Mechanical Structures of the 482.6 mm (19 in) Series - Part 1: Panels and Racks
- EIA 310-E: Cabinets, Rack Panels, and Associated Equipment

2.3 IEEE Mechanical References

The following references should help the designer find the proper references in the IEEE mechanical documents that are applicable to VMEbus standards.

2.3.1 IEEE 1101.1

Item	Reference
General PCB sizes and tolerances	Clauses 6/7/8/9
Front mounted PCB assembly Test/Inspection dimensions - DT2	Table 5
General Backplane sizes and tolerances	Clause 10
Backplane bow, static and dynamic	Clause 11
General non-EMC Subrack sizes and tolerances	Clause 11 (8)
Subrack assembly Test/Inspection dimension - Dc	Table 7
Non-EMC Front Panels	Figures 13/14
Front Panel/PCB/Connector/Backplane relationship	Figure 15
Board to Board relationship	Figure 16

2.3.2 IEEE 1101.10

Item	Reference
EMC Subrack interface dimensions	Clause 5
EMC PCB Front Panel and Filler Panel interface dimensions	Clause 5
EMC Front Panel and PCB relationship	Figure 5
Keying and Alignment Pin	Clause 6
Programming Key	Figure 10
Programming of Keys	Figure 11
Alignment Pin Test dimensions	Figure 12
Protective Solder Side Cover (for PCB mounting holes see IEEE 1101.1)	Clause 7
Subrack Injector/Extractor detail	Clause 8
Subrack Injector/Extractor Test dimension	Figure 15
Injector/Extractor detail	Figure 15
Front Panel assembly with Injector/Extractor Test dimension G	Table 6
ESD protection	Clause 9
5 row 160-pin Connector mounting detail	Clause 10

2.3.3 IEEE 1101.11

Item	Reference
Inline mounting of rear PCB assemblies	Clause 5
Rear mounted PCB sizes	Clause 6
Rear mounted PCB assembly Test/Inspection dimensions - DT2	Table 2
Connector Orientation and Labeling	Clause 7
Rear mounted PCB assembly Subrack Test/Inspection dimensions for RDc/RDx	Table 2
Maximum Backplane thickness	Clause 9
Connector Labeling	Clause 10
Connector performance	Clause 12
Connector alignment	Clause 13
Front/Rear PCB Panel assembly Safety GND	Clause 15
J0, 2 mm metric Connector mounting	Appendix A

2.4 Reference Materials

The following are a list of useful books for the board and system designer. In addition to electronic topics this list includes mechanics and cooling. Today's engineer also needs to understand simulation languages and software. This list is the favorite of the editors and the designers they contacted.

2.4.1 Connectors

- *Electronic Connector Handbook : Theory and Applications (Electronic Packaging and Interconnection Series)* Robert S. Mroczkowski, McGraw Hill Text, (October 1997)
- *Electronic Packaging and Interconnection Handbook (Electronic Packaging and Interconnection Series)*, Charles A. Harper (Editor), McGraw Hill Text, 2nd edition (November 1996)

2.4.2 Cooling

- *Cooling Techniques for Electronic Equipment* Dave S. Steinberg, John Wiley & Sons, 2nd edition (October 1991)
- *Compact Heat Exchangers* W. M. Kays, A. L. London, Krieger Publishing Company, 3rd edition (September 1997)
- *Handbook of Heat Transfer*, Warren M. Rohsenow (Editor), James P. Hartnett (Editor), Young I. Cho (Editor), McGraw Hill Text, 3rd edition (June 1998)

2.4.3 Grounding and Shielding

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- *Noise Reduction Techniques in Electronic Systems*, H. W. Ott, John Wiley & Sons, 2nd edition (March 1988)
- *Grounding and Shielding Techniques*, Ralph Morrison, John Wiley & Sons, 4th edition (February 1998)
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- *Introduction to Electromagnetic Compatibility*, Clayton R. Paul, John Wiley & Sons, (1992)
- *Electronic System Design: Interference and Noise-Control Techniques*, John R. Barnes, Prentice-Hall, (1987)

2.4.4 Mechanical

- *Vibration Analysis for Electronic Equipment*, Dave S. Steinberg, John Wiley & Sons, 2nd edition (November 1988)
- *Mark's Standard Handbook for Mechanical Engineers*, Eugene A. Avalone (Editor), Theodore Baumeister III (Editor), McGraw Hill, 10th edition (July 1996)

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- *Microelectronics Packaging Handbook: Technology Drivers (Part 1)*, Rao R. Tummala (Editor), Eugene J. Rytmaszewski (Editor), Alan G. Klopfenstein, Chapman & Hall, 2nd edition (August 1997)
- *Microelectronics Packaging Handbook: Semiconductor Packaging (Part 2)*, Rao R. Tummala (Editor), Eugene J. Rymaszewski (Editor), Alan G. Klopfenstein, Chapman & Hall, 2nd edition (January 1997)

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- *Hybrid Microelectronics Handbook (Electronic Packaging and Interconnection)*, Jerry E. Sergent, Charles A. Harper (Editor), McGraw Hill Text, 2nd edition (September 1995)
- *Printed Circuit Board Materials Handbook (McGraw-Hill Electronic Packaging and Interconnection Series),* Martin W. Jawitz (Editor), McGraw Hill Text, 2nd edition (June 1997)
- *Printed Circuits Handbook*, Clyde F., Jr. Coombs (Editor), McGraw Hill Text, 4th edition (January 1996)

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- *Switched Mode Power Supplies: Design and Construction (Electronic & Electrical Engineering Research Studies. Electrical Energy Series, 2)*, H. W. Whittington, B. W. Flynn, D. E. MacPherson, Research Studies Press, 2nd Edition (April 1997)

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- *Microelectronic Circuits (Oxford Series in Electrical Engineering)*, Adel S. Sedra, Kenneth C. Smith, Oxford University Press, 4th edition (June 1997)
- *MECL System Design Handbook*, Bill Blood, Motorola Handbook
- *The Art of Electronics*, Paul Horowitz, Winfield Hill (Contributor), Cambridge University Press, 2nd edition (August 1989)
- *High-Speed Digital Design : A Handbook of Black Magic*, Howard W., Ph.D. Johnson, Martin, Ph.D. Graham, Prentice Hall, (January 1993)
- *The VMEbus Handbook*, Wade Peterson, VITA

2.4.8 Hardware Simulation Languages

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- *The Verilog Hardware Description Language*, Philip R. Moorby, Donald E. Thomas, Kluwer Academic Publishers, 4th edition (May 1998)
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- *Troubleshooting Analog Circuits*, Robert A. Pease, Butterworth-Heinemann (December 1993)

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3 Module Logical Implementation

3.1 Introduction

This Chapter provides additional information to the designer of VME64xP Modules. Address widths, data widths and information on CR/CSR space is covered herein. Compatibility issues are discussed in Section 1.2.

3.2 Module Addressing ... A Review Of Current Standards and Practices

The following subsections describe the various protocols for addressing and data transfer that is available to the system designer in the VMEbus family of standards. Two-edged (2eVME) protocols are detailed in VME64x (VITA 1.1) and are not covered in this overview. The 2eSST protocols are in VITA 1.5.

3.2.1 Address Widths and AM Codes

As VMEbus has matured, the number of bits of address available to both Masters and Slaves has increased. VME defined A16, A24 and A32 modes of addressing. Rule 2.61 of the IEEE 1014 requires that Masters which support A24 addressing also support A16 addressing. Rule 2.62 extends Rule 2.61 such that A32 Masters also support A24 and A16. There is no similar rule for Slaves; thus, an A32-only Slave plugged into a subrack controlled by an A16 Master will result in a system that doesn't work and yet still complies with the standard.

The VME64 standard has extended the addressing scheme by the addition of the A40 and A64 address modes. The A40 mode is designed to allow extended addressing to 3U devices that contact only the J1 connector, and the A64 is a general extension. Rules 2.74 and 2.75 of the VME64 standard reiterate Rules 2.61 and 2.62 of IEEE 1014, in that all Masters must support the A16 mode, and A32 Masters must also support A24. VME64 extends this with Rule 2.73, which requires that A40 Masters support A24 and A16 in addition to A40. VME64, Rule 2.72 also requires A64 Masters to support A32, A24 and A16. A32 and A64 Masters may also support A40 for full compatibility, but are not required to do so. In VME64, the Slaves are still allowed to support only a single addressing mode; therefore, the choice of Master is still determined by the address modes that are supported by all Slaves within the subrack.

Observation 3.2.1-a (Slave addressing mode support):

VMEbus Slaves are allowed to support only a single addressing mode; therefore, the choice of Master is determined by the address modes that are supported by all Slaves within the subrack. Table 3.2-1 in VITA 23 lists preferred VME64xP AM codes.

3.2.2 Data Transfer Widths

VME supports the design of eight-bit (D08(O) and D08(EO)), sixteen-bit (D16) and thirty-two bit (D32) wide devices. To allow older Masters to read newer Slaves, the VME standard includes Rules which require wide data path Slaves to support the narrower data path access modes. Rule 2.63 of IEEE 1014 requires that D32 devices also support D08(EO) and D16 transfer capabilities. Similarly, Rule 2.64 of the VME standard requires that D16 devices support the D08(EO) transfer mode. The D08(O) (eight bit, odd byte only) transfer mode is designed for support of 8-bit devices that cannot provide adjacent locations in response to a double-byte read cycle, and is not a required mode for wider devices.

In keeping with this same backwards compatibility scheme for data transfers, the VME64 standard recommends that devices which support the sixty-four bit wide MBLT transfer modes should also support

D32, D16 and D08(EO) capability (see Recommendation 2.5 in VME64 standard). No increases in data width past 64 bits are provided in either the VME64x standard or the VME64xP standards.

A 32-bit data mode (MD32) is specified for 3U VMEbus Modules. This mode is not used for 6U or 9U VMEbus Modules and therefore is not recommended in this document.

3.2.3 CR/CSR and The Base Address Register

VME64 specifies a standard method to access a Module's CR and CSR space. Each Module is assigned a unique block of 512 kB of CR/CSR space accessed in A24 address mode using a standard AM code, 2F. Module CR/CSR space may have the same numeric addresses as those in another "space" within the Module, but no conflict exists because CR/CSR space is accessed with a unique AM code. All other AM codes reference a space that is different from CR/CSR space.

VME made no mention of the Base Address Register (BAR). The BAR was introduced in the VME64 standard to select one of the 31 available 512 kB CR/CSR regions (region 00 is reserved). Section 2.3.12 of the VME64 standard introduces the BAR. Prior to the VME64x standard, there were little or no Rules or Recommendations regarding CR/CSR space and data space accessing. Designers of a Module conforming to VME and requiring access to both CR/CSR space and data space would usually design the Module to be accessed at a bank of consecutive addresses by the use of switches, jumpers or a programmable component. Address Modifier (AM) codes to which the Module responds would be selected in a similar manner. For example, if the Module had A32 addressing, the positions of an eight-bit address switch and its allowed AM codes would be compared to Address lines A(31:24) and Address Modifier code AM(5:0), respectively, during an address cycle to decide whether the Module is addressed. The bank of addresses selected with the eight-bit switch would typically be divided, with perhaps lower addresses used to access data registers and higher addresses used to access CR and/or CSR registers.

3.3 VME64xP Module Addressing Modes and Data Transfers

The following subsections apply to the design of VME64xP Modules that can be used in VME and VME64 subracks as well as in VME64x subracks.

3.3.1 Addressing Modes and Address Cycle Address Information Latching

The VME64x standard has not introduced any new address widths, but has added two new AM codes, 20 and 21. The defined XAM codes for AM code 20 and 21 are for block transfers.

Recommendation 3.3.1-a (VME64xP Slave data space implementation):

In order to simplify VME64xP 6U and 9U Slave Modules, data space should have only one data space defined. Table 3.2-1 in VITA 23 lists the recommended AM codes.

Permission 3.3.1-b (A24 modes):

For compatibility with Masters which do not generate AM code 2F, a VME64xP Module which has no A24 data space may allow A24 access to CR/CSR via A24 AM codes in addition to 2F.

3.3.2 Data Transfer Widths

Observation 3.3.2-a (support of D16 and D08(EO) transfers):

Rule 2.77 of the VME64 specification requires that D32 Slaves shall implement the D16 and D08(EO) transfer modes. Recommendation 2.4 of the VME64 specification suggests that D32 Masters should also contain D16 and D08(EO) capabilities. This document does not require D(16) or D08(EO) except where necessary for compatibility.

3.3.3 VME64x and CR/CSR Space Access

The Geographical Address pins, GA(4:0)* are used in the VME64x standard to access VMEbus CR/CSR space, including the Base Address Register, and to access user CSR and user CR space. The BAR is a single byte, located at the highest address within the 512 kB CR/CSR block assigned to the Module. Under normal operations the BAR is not directly accessed by software, but instead is automatically loaded from the Geographic Address pins by logic within the Slave Module. Bits 3 through 7 of the eight-bit BAR value correspond to bits 19 through 23 of an A24 address, and define the base address for the CR/CSR space of the Module. Chapter 9 of the VME64x standard gives more details.

For VME64x CSR/CR access, the Geographical Address of a Module is shifted left 19 bits to form a base address from which the Module's CR/CSR space consumes a fixed 512 kB block. The CR/CSR section of Modules in adjacent subrack slots have contiguous 512 kB address blocks. Modules designed to use GA pins, when plugged into older systems that do not have the Geographic Address pins, need to derive the equivalent of the five bits of geographical address from switches, jumpers or a programmable component. Programmable components may be loaded from a serial line on the VMEbus backplane or by removing them and using a suitable programmer. The serial protocols for such an operation are currently not specified by VMEbus, however, work is in progress on such a definition in the HA-VME task group within the VSO.

Observation 3.3.3-a (Geographic Address pins):

VMEbus subracks with the standard 3-row DIN connectors or VME64 subracks with the 5-row DIN connectors do not support Geographic Addressing. Section 7.1 of the VME64 standard introduces the new 5-row connector; however, the GA pins were not added to this connector until the VME64x standard.

3.4 VME64xP Module Implementation Of CR/CSR Registers

The following subsections detail specifications for the contents of Configuration ROM and Control/Status Registers in VME64xP Modules. VME64xP Modules designer should use VME64x, Chapter 10 as a guide to implementing CR/CSR Space. Tables 3.4.1-1, 3.4.2-1 and 3.4.3-1 have information contained in Chapter 10 of VME64x and the VME64xP specific registers. They are provided here as a convenience to the user. For convenience, the VME64 and VME64x registers are included in the tables. The user should always refer to the source document to confirm the information.

3.4.1 VME64xP Modules and Configuration ROM and Control/Status Registers

The VME64 Standard document describes the basic method by which Configuration ROM and Control/Status Registers are allocated in VMEbus address space. VME64xP Modules may implement additional read/write protocols that require additional CSR's in order to operate. The CR/CSR specifications in the VME64x standard indicate that all user CR/CSR locations are found by providing pointers from fixed locations in CR/CSR space. These pointers provide addresses of the beginning and end of both user CR and CSR locations that are defined in the hardware of the device. These pointers allow user CR and CSR's to be located anywhere within the Module's free CR/CSR space. An additional set of pointers defines a Configuration RAM (CRAM) space. The use of the CRAM space is defined in Chapter 10 of VME64x.

Table 3.4.1-1
CR/CSR Address Space Chart

Address ↓	Definition
0x00003 • • • 0x0005B	VME64 Defined CR
0x0005F • • • 0x0007F	VME64 Reserved CR Program ID (0x07F only)
0x00083 • • • 0x0074F	VME64x Defined CR
0x00753 • • • 0x00FFF	VME64x Reserved CR (555 bytes)
≋	≋
BEG_USER_CR • • • END_USER_CR	User CR Space (optional) VME64xP CR
≋	≋
BEG_CRAM • • • END_CRAM	Configuration RAM (optional) CRAM
≋	≋
BEG_USER_CSR • • • END_USER_CSR	User CSR Space (optional) VME64xP CSR
≋	≋
0x7FC03 • • • 0x7FF5F	VME64x Reserved CSR (216 bytes)
0x7FF63 • • • 0x7FFF3	VME64x Defined CSR
0x7FFF7 • • • 0x7FFFF	VME64 Defined CSR

3.4.2 VME64xP Modules, Additional Configuration ROM Assignments

VME64xP introduces one new Configuration ROM assignment, a one-byte VME64xP CR Space Capabilities register (see VME64xP, Table 3.3.3-2). The VME64xP Capabilities register informs software of the protocols supported by the Module to allow for optimum readout speed.

Table 3.4.2-1
VMEbus (VME, VME64, VME64x, VME64xP) Module Configuration ROM (CR) Assignments
Part 1

CR Address [MSB .... LSB]	Content	Size	Relevant Standard
0x03	Checksum	1 byte	VME64
0x07, 0x0B, 0x0F	Length of ROM	3 bytes	VME64
0x13	Configuration ROM data access width	1 byte	VME64
0x17	CSR Data access width	1 byte	VME64
0x1B	CR/CSR Space Specification ID	1 byte	VME64
0x1F	0x43 (ASCII “C”)	1 byte	VME64
0x23	0x52 (ASCII “R”)	1 byte	VME64
0x27, 0x2B, 0x2F	Manufacturer’s ID (IEEE OUI)	3 bytes	VME64
0x33, 0x37, 0x3B, 0x3F	Board ID supplied by manufacturer	4 bytes	VME64
0x43, 0x47, 0x4B, 0x4F	Revision ID supplied by manufacturer	4 bytes	VME64
0x53, 0x57, 0x5B	Pointer to a null terminated ASCII printable string or 0x000000	3 bytes	VME64
0x5F to 0x7B	RESERVED	8 bytes	VME64
0x7F	Program ID code	1 byte	VME64
0x83, 0x87, 0x8B	Offset to BEG_USER_CR	3 bytes	VME64x
0x8F, 0x93, 0x97	Offset to END_ USER_CR	3 bytes	VME64x
0x9B, 0x9F, 0xA3	Offset to BEG_CRAM	3 bytes	VME64x
0xA7, 0xAB, 0xAF	Offset to END_CRAM	3 bytes	VME64x
0xB3, 0xB7, 0xBB	Offset to BEG_USER_CSR	3 bytes	VME64x
0xBF, 0xC3, 0xC7	Offset to END_ USER_CSR	3 bytes	VME64x
0xCB, 0xCF, 0xD3	Offset to BEG_SN	3 bytes	VME64x
0xD7, 0xDB, 0xDF	Offset to END_SN	3 bytes	VME64x
0xE3	Slave Characteristics Parameter, see Table 10-1	1 byte	VME64x
0xE7	User-defined Slave Characteristics	1 byte	VME64x
0xEB	Master Characteristics Parameter, see Table 10-2	1 byte	VME64x
0xEF	User-defined Master Characteristics	1 byte	VME64x
0xF3	Interrupt Handler Capabilities	1 byte	VME64x
0xF7	Interrupter Capabilities	1 byte	VME64x
0xFB	Reserved, Read as zero	1 byte	VME64x
0xFF	CRAM_ACCESS_WIDTH, see Table 10-10	1 byte	VME64x

Table 3.4.2-1
VME Standard and VME64xP Module Configuration ROM (CR) Assignments
Part 2

CR Address [MSB .... LSB]	Content	Size	Relevant Standard
0x103	Function 0 Data Access Width DAWPR, see Table 10-3	1 byte	VME64x
0x107	Function 1 Data Access Width	1 byte	VME64x
0x10B	Function 2 Data Access Width	1 byte	VME64x
0x10F	Function 3 Data Access Width	1 byte	VME64x
0x113	Function 4 Data Access Width	1 byte	VME64x
0x117	Function 5 Data Access Width	1 byte	VME64x
0x11B	Function 6 Data Access Width	1 byte	VME64x
0x11F	Function 7 Data Access Width	1 byte	VME64x
0x123 … 0x13F	Function 0 AM Code Mask AMCAP, see Table 10-5	8 bytes	VME64x
0x143 … 0x15F	Function 1 AM Code Mask	8 bytes	VME64x
0x163 … 0x17F	Function 2 AM Code Mask	8 bytes	VME64x
0x183 … 0x19F	Function 3 AM Code Mask	8 bytes	VME64x
0x1A3 … 0x1BF	Function 4 AM Code Mask	8 bytes	VME64x
0x1C3 … 0x1DF	Function 5 AM Code Mask	8 bytes	VME64x
0x1E3 … 0x1FF	Function 6 AM Code Mask	8 bytes	VME64x
0x203 … 0x21F	Function 7 AM Code Mask	8 bytes	VME64x
0x223 … 0x29F	Function 0 XAM Code Mask XAMCAP, see Table 10-5	32 bytes	VME64x
0x2A3 … 0x31F	Function 1 XAM Code Mask	32 bytes	VME64x
0x323 … 0x39F	Function 2 XAM Code Mask	32 bytes	VME64x
0x3A3 … 0x41F	Function 3 XAM Code Mask	32 bytes	VME64x
0x423 … 0x49F	Function 4 XAM Code Mask	32 bytes	VME64x
0x4A3 … 0x51F	Function 5 XAM Code Mask	32 bytes	VME64x
0x523 … 0x59F	Function 6 XAM Code Mask	32 bytes	VME64x
0x5A3 … 0x61F	Function 7 XAM Code Mask	32 bytes	VME64x
0x623 … 0x62F	Function 0 Address Decoder Mask ADEM, see Table 10-4	4 bytes	VME64x
0x633 … 0x63F	Function 1 ADEM	4 bytes	VME64x
0x643 … 0x64F	Function 2 ADEM	4 bytes	VME64x
0x653 … 0x65F	Function 3 ADEM	4 bytes	VME64x
0x663 … 0x66F	Function 4 ADEM	4 bytes	VME64x
0x673 … 0x67F	Function 5 ADEM	4 bytes	VME64x
0x683 … 0x68F	Function 6 ADEM	4 bytes	VME64x
0x693 … 0x69F	Function 7 ADEM	4 bytes	VME64x
0x6A3	Reserved, read as zero	1 byte	VME64x
0x6A7	Reserved, read as zero	1 byte	VME64x
0x6AB	Reserved, read as zero	1 byte	VME64x
0x6AF	Master Data Access Width DAWPR, see Table 10-3	1 byte	VME64x
0x6B3 … 0x6CF	Master AM Capability AMCAP, see Table 10-5	8 bytes	VME64x
0x6D3 … 0x74F	Master XAM Capability XAMCAP, see Table 10-5	32 bytes	VME64x
0x753 … 0xFFF	RESERVED	552 bytes	VME64x
C(BEG_USER_CR) = Y	VME64xP Capabilities CR Register	1 byte	VME64xP
0x(Y + 4) … 0x(Y + 3C)	VME64xP Reserved	15 Bytes	VME64xP

3.4.3 VME64xP Module Control/Status Register Additions

VME64xP Modules can implement a few additional Control/Status registers that provide for increased functionality. These registers assist the designer in creating diagnostic features and assist the software designer by allowing dynamic address reconfiguration.

Table 3.4.3-1
VMEbus Control/Status Register (CSR) Assignments

CSR Address [MSB ………… LSB]	Content	Size	Relevant Standard
0x7FFFF	CR/CSR (BAR) Base Address Register	1 byte	VME64
0x7FFFB	Bit Set Register see Table 10-6	1 byte	VME64
0x7FFF7	Bit Clear Register see Table 10-7	1 byte	VME64
0x7FFF3	CRAM_OWNER Register	1 byte	VME64x
0x7FFEF	User-Defined Bit Set Register	1 byte	VME64x
0x7FFEB	User-Defined Bit Clear Register	1 byte	VME64x
0x7FFE3 … 0x7FFE7	RESERVED	2 bytes	VME64x
0x7FFD3 … 0x7FFDF	Function 7 ADER see Table 10-8	4 bytes	VME64x
0x7FFC3 … 0x7FFCF	Function 6 ADER	4 bytes	VME64x
0x7FFB3 … 0x7FFBF	Function 5 ADER	4 bytes	VME64x
0x7FFA3 … 0x7FFAF	Function 4 ADER	4 bytes	VME64x
0x7FF93 … 0x7FF9F	Function 3 ADER	4 bytes	VME64x
0x7FF83 … 0x7FF8F	Function 2 ADER	4 bytes	VME64x
0x7FF73 … 0x7FF7F	Function 1 ADER	4 bytes	VME64x
0x7FF63 … 0x7FF6F	Function 0 ADER	4 bytes	VME64x
0x7FC00 … 0x7FF5F	RESERVED	216 bytes	VME64x
0xX … 0x(X + 3C)[2]	VME64xP Reserved	16 bytes	VME64xP
0x(X + 40)	CBLT/MCST Register 1	1 byte	VME64xP
0x(X + 44)	CBLT/MCST Register 2	1 byte	VME64xP

Note 1: See Observations 3.3.2-l and 3.3.2-m in VITA 23 for byte ordering.
Note 2: X = C(BEG_USER_CSR)

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4 VME64xP Modules

4.1 Introduction

A VME64xP Module is a VMEbus Module that conforms also to the rules of this document. A VME64xP Module is inserted into the front of a subrack and mates with the subrack backplane through the VME64x circuit board connectors. It includes one or more VME64xP module circuit boards (with mezzanine cards, if any) and a front panel with its attachments. This document is concerned with two basic Module sizes, the 6U x 160 mm as in VME64x and the 9U x 400 mm as in VME64x9U.

4.2 VME64xP Module Construction

Observation 4.2-a (9U adapters for 3U or 6U circuit boards and Modules):

A 3U or 6U circuit board or Module, described in Annex C of VITA 1.3, can be used as part of a 9U x 400 mm Module. The assembly constitutes a 9U x 400 mm Module. The 9U x 400 mm adapter plate, in addition to supporting the smaller board or Module, serves to prevent the shunting of airflow into adjacent subrack slots. The adapter also has injector/ejector/locking handles and the hardware for keying.

Observation 4.2-b (flush-mounted Modules on adapters):

Where the 3U or 6U Module is flush with the 9U front panel, the keying mechanism and the other front panel items of Section 4.2 of VITA 23, as well as any front panel connectors, are mounted on or flush with the 9U panel. The adapter can have keying for the 3U and 6U Modules along with the mechanics for latching/injection/ejection.

Observation 4.2-c (recess-mounted Modules on adapters):

Where the 3U or 6U Modules are not flush with the 9U front panel and do not have a full front panel, the keying mechanism will be on the 9U front panel of the adapter. The location of the other front panel items will depend on feasibility and on the wishes of the user.

Observation 4.2-d (special subracks for mixed Module sizes):

Smaller Modules, complete with their front panels, can be inserted into the subracks for 9U Modules so as to mate directly with the backplane in subracks that are constructed so as to permit such insertion. In this case 9U adapters may not be necessary though airflow blocking plates will be needed to prevent the cooling air from escaping or from shunting into adjacent slots.

4.3 VME64xP Module Circuit Board

Permission 4.3-a (6U board thickness):

Except as specified otherwise in IEEE 1101.10, the board thickness for 6U VME64xP circuit boards may be a maximum of 2.6 mm (0.101 in).

Recommendation 4.3-b (chamfers):

A chamfer of approximately 45° and measuring 1.5 ± 0.5 mm should be on the top and bottom of the rear (connector) end of the board to prevent “chiseling” of the card guide on insertion.

Observation 4.3-c (lead trimming):

It is important that leads are trimmed on the solder side of the board such that they conform to the clearance dimensions given in IEEE 1101.10. This is to prevent the

trimmed leads from shorting to components or abrading the EMI gaskets on the adjacent Module. The maximum lead protrusion from the component side is 3.1 mm (0.122 in). The back side shield is at 4.00 mm from the component side which clears the interboard separation plane by 0.07 mm. On the component side the maximum component height above the board surface cannot exceed 13.71 mm (0.540 in).

Observation 4.3-d (board stiffeners):

9U x 400 mm Modules may require board stiffeners to maintain the alignment of the rear connectors within the insertion tolerances and to keep the board from encroaching on the neighboring Module space. It is also advisable to make the Module circuit board for 9U x 400 mm Modules as thick as practical, preferably 2.4 ± 0.2 mm (0.093 ± 0.008 in). A stiffener bar, if required, could be located across the board vertically as close to the rear connectors (P1-P6) as practical. A second bar placed vertically near the center, is advisable. The bars are required to be within the Module maximum component height as specified in IEEE 1101.10. If the front of the printed circuit board is firmly attached to the front panel, the panel could act in lieu of a front stiffener.

Observation 4.3-e (pre-stress stiffeners):

Some boards may furnish enough resistance to straightening that a simple board stiffener cannot flatten the board. If a stiffener is designed to be pre-stressed, the tension or compression (depending on the direction of warp) of the stiffener will provide the necessary force to flatten the board.

Observation 4.3-f (PCB warpage spec):

The printed circuit board, prior to loading or installing stiffeners, is required to have a maximum deviation from flatness of 0.8 mm and a maximum bow or twist of 0.07 mm/cm. The flatness is measured by laying the unweighted board on a flat surface and measuring the deviations with an appropriate gauge. Twist is measured along the edge of the printed circuit board that contacts the card guide. Warp across the connector edge is removed by the use of stiffeners. See IEC 61076-4-101, Section 3.3 for connector mating tolerances (IEC 60602-2 connectors are similar). IEEE 1101.1 and 1101.10 specify that the module cannot extend beyond the inter-board separation plane. This warpage specification is consistent with the documents cited here.

Suggestion 4.3-g (construction to minimize warpage):

To minimize board warpage the printed circuit board material, the board manufacturing procedures and the soldering procedures require careful consideration. Manufacturers of circuit boards are advised to note the following:

- *Proper circuit board fabrication technique* – Multi-layer printed circuit boards need to be fabricated with alternate layers of weave orthogonal in order to minimize warpage.
- *Proper installation of connectors* - Connectors are not to be soldered onto a circuit board via mass termination techniques such as wave soldering or infrared heat application without protection against solder wicking into the contacts. The consequences of solder wicking is ultimately the destruction of the expensive subrack multi-layer backplane. Only facilities with special techniques and competent personnel can assure that no wicking takes place during mass soldering operations.
- *Hand soldering* - Soldering connectors onto the circuit boards by hand requires care to avoid warpage of the connector and board. The soldering process would be to hold the board flat and carefully tack the connector at about every 10th socket position, working around the connector, prior to proceeding with the actual soldering of the socket tail pieces onto the board. This soldering, too, requires care to avoid the wicking of solder into the connector.

- *Cooling after soldering* - Boards that have passed through a soldering process are warmed to the point where the board material (*e.g.*, FR-4) becomes plastic. It is important to constrain the board so it is flat during the cooling period. If it is not held flat the board can retain any irregularities induced while cooling.

Observation 4.3-h (press fit connectors):

If press-fit connectors are used soldering problems are eliminated. Most connectors available are available only with press-fit and are not to be soldered (See Chapter15).

The P0, P4, P5, and P6 connectors may be purchased with optional shields that provide extra ground connections. The shield consists of two parts; when installed on the Module or Transition Module connector, the top shield makes contact with the 'z' row of the backplane connector, and the bottom shield makes contact with the 'f' row of the backplane connector. Mechanical constraints on some shields may not allow the use of a bottom shield, which contacts the backplane 'z' row, on the Module connector. This is due to the intrusion of the bottom shield into the adjacent interboard separation plane (see IEEE 1101.10). The top shield connects to the Module by utilizing every odd-numbered pin position in the Module 'f' row, and the bottom shield connects to every even-numbered pin in the Module 'f' row. Use of the top shield without the bottom shield allows the Module designer to drill only every other hole in the 'f' row; however, this would prevent the user from adding the bottom shield at a later time.

Observation 4.3-i (other connector options):

Where special system requirements demand, connectors other than the 2 mm types specified in VME64x and VME64xP can be used for P4, P5 and P6. VME64x9U (VITA 1.3) discusses the options.

Suggestion 4.3-j (connector size and compatibility):

It is important to check pin lengths carefully; see especially VME64x Rule 4.4. It is also important that connectors from different manufacturers not be intermixed when configuring P5/J5 and P6/J6. Variations in end finishing can result in interference and cause misalignment.

4.4 VME64xP Module Front Panel

Observation 4.4-a (front panels, connector isolation):

VME64xP Module front-panels are part of the overall EMI/EMC 'shield' and thus are not to be connected to ground (GND). This requires also that any front-panel connectors be isolated from ground.

Observation 4.4-b (power OK):

The POWER (Red) LED indicates that the Module power is on. This indicator is the logical 'or' of all voltages on the Modules. Where protection or converter circuitry is present on the Module (*e.g.* fuses), the voltages are sensed at the output(s) of those circuits.

Suggestion 4.4-c (detailed power indicators):

An indicator on each voltage within the Module (on the load side of the fuse, if any) can help in trouble shooting. Due to panel space limitations these indicators may be interior to the Module.

Recommendation 4.4-d (Activity indicator off period):

The off period for the ACTIVITY LED should be a minimum of 100 milliseconds so that the human eye can recognize the blink. This LED is on when the Module has been initialized and is able to communicate on the bus.

Observation 4.4-e(processor running):

The RUN or HALT (red/green) LED indicates the condition of a Module's processor or state machine. The LED is green if the processor or state machine is running and red if stopped or a fault occurs. This indicator is used only on Modules that contain a processor or state machine.

Recommendation 4.4-f (front panel issues):

1) A front panel should always be used.
2) A mounting bracket with lock washer should be used near the middle of the front panel to secure the panel to the module circuit board.
3) Lock washers should be used to secure the injector/ejector handles to the module circuit board and front panel. Note that these may not be in the kit from the manufacturer. One can also use Loctite 222® or equivalent on all screws.
4) The separation between the top and bottom injector/ejector handles should be carefully checked against the dimensions given in IEEE 1101.1 to prevent possible handle failures.

4.5 VME64xP Module Shielding

Modules may require partial or complete shielding in order to obtain adequate low-level analog performance or to help maintain an EMC environment. IEEE 1101.10 provides guidance regarding designing for EMC and ESD environments. See also Chapter 12.

Observation 4.5-a (cooling and shields):

Care is necessary when using shields on a Module to avoid interference with adequate cooling of that and other Modules.

Suggestion 4.5-b (shield construction):

The component side shield needs to be insulated to prevent shorting. One way of accomplishing this is to use FR4 with a copper plane. Shorting may be avoided by having the copper as an interior layer or by using an insulating material or spacers.

4.6 VME64xP Connector Forces

Observation 4.6-a (insertion/extraction forces):

Table 4.6-1 gives approximate exertion and extraction forces for modules.

Table 4.6-1
Insertion/Extraction Forces

Board Height	Standard	Connector(s)	Total Pins	Insertion Force[2] max.	Extraction Force[2] min.
3U	VME/VME64	J1	96	90 N	20 N
6U	VME/VME64	J1/J2	192	180 N	40 N
6U	VME64x	J1/J0/J2	435	345 N[1]	89 N
9U	VME64x-9U	J1/J0/J2/J4/J3	746	575 N[1]	146 N
9U	VME64x-9U	J1/J0/J2/J4/J5/J6	905	730 N[1]	175 N

Note 1: Harting 160-pin connectors purchased before June 1998 will raise these numbers by about 25 N per J1, J2 and/or J3 connector that is installed.

Note 2: To convert N (Newton) to pound-force multiply by 0.225.

4.7 VME64xP Module Live Insertion

Observation 4.7-a (use of precharge):

The VPC pins are for pre-powering the ETL bus interface integrated circuits. This voltage and associated ground is located on longer pins at the ends of the P1 and P2 connectors. When the board is inserted these pins make first and the ETL transceiver is powered into a state where the VMEbus signals are at high impedance. This prevents glitches on the backplane and stops the inadvertent driving of a bus line(s).

Observation 4.7-b (power for VPC):

In many VMEbus backplanes the VPC pins are connected to the +5 V power. It is permissible to connect VPC to +3.3 V instead where lowering the power consumption of a system is important.

Observation 4.7-c (live insertion feature):

The VITA "live insertion" feature can be used on VME64xP modules. The intent of live insertion capability is to permit the insertion and extraction of Modules while the subrack backplane is powered without damage to the Modules or contamination of the data or upsetting of the system status. This optional feature involves voltage connections to the backplane connectors, connector pin lengths, and other features in the Modules. (See ANSI/VITA-3 (BLLI) and/or VITA 1.4-199x (VME64x Live Insertion System Requirements). See also Recommendation 4.9-a.

4.8 VME64xP Module Die and Module Temperatures

Excessive operating temperatures and excessive thermal differential between devices result in increased noise and chances for system failure. The following are to be considered when designing the bulk cooling system.

Observation 4.8-a (high-power issues):

Modules exceeding the power dissipation of Recommendation 4.3-l of VITA 23 could be used in a subrack provided that the current limits of the P1/J1, P2/J2 and/or P0/J0 connector contacts are not exceeded. However, great care needs to be taken in system cooling design to insure proper removal of heat. The user of such a system can not expect simple fan trays to provide adequate air flow. Heat exchangers and/or water cooling, plus the use of plenums to direct the air flow, will almost certainly be required.

Suggestion 4.8-b (power density):

Module designers should try for an even power distribution on the board and avoid "hot spots". A good rule of thumb for air cooled systems is not to exceed 1 W/in^2 (average).

Observation 4.8-c (hot spots):

If an IC package cannot maintain a maximum die temperature of 85 °C in the subrack air flow, it should be classed as high power, and protective measures are required. Heat sinks or heat spreaders attached to these ICs can possibly reduce the die temperature to 85 °C or lower.

4.9 VME64xP Module Circuitry Protection

Safety is an important consideration in systems, especially those with high current power supplies, since shorts or other failures in the Module can potentially cause fires. Some protection schemes have side effects on the design of boards that must be considered.

Recommendation 4.9-a (hazards of live insertion):

Modules that do not include the features for live insertion should not be inserted into subracks with power on nor should any Modules be inserted into subracks with power on if the subracks are not wired and powered for live insertion. Failure to observe this precaution can result in damage to the Module and in errors in the data or the status of the system. Keying as specified in Appendix C of VITA 23 can be used to mitigate this problem.

Observation 4.9-b (fusing of commercial Modules):

Fusing is controversial in industrial equipment; consequently, many commercial Modules will not have fusing at the board level.

Observation 4.9-c (high speed signals and fuses):

When designing with high-speed electronics the return current path lengths become very important as it affects signal quality. The general rule is that the return path be such that the propagation time along it is the same as that of the signal path. In this way the induced signal travels in phase with the signal and does not generate 'noise'. If fuses are used the return current paths must be carefully considered. See Section 4.9.3.

Observation 4.9-d (CMOS and fuses):

If CMOS circuits are used on a board that has fuses and a fuse opens, it is possible that a powered CMOS device will be driving an unpowered CMOS device. When this occurs, the powered CMOS device may be destroyed by excessive current flowing from its output through the input of the unpowered CMOS device. For boards with segmented power separately fused, a series resistor may be necessary when CMOS signals cross a segment boundary. TTL, ECL and *some* CMOS logic families do not have this problem.

4.9.1 Overvoltage Protection

Tests have been performed using PICO® fuses (Littlefuse Corp.) and ICTE-5® (International Rectifier Corp.) transient suppressors. These devices were chosen because of their fast acting properties.

Tests of these fuses and transient suppressors have shown that to protect modules from overvoltage during a power supply failure one transient suppressor is required for every five amps of fuse rating. Thus for 10 amps at +5 volts using a single 15 amp fuse, three transient suppressors in parallel to digital common (circuit ground) at the downstream end of the fuse are required. If two 10 amp fuses in parallel are used, four transient suppressors in parallel are required, etc. Since the transient suppressor reacts in a few hundreds of picoseconds, the energy required to blow the fuse is less than the energy to destroy the transient suppressor.

Initial studies and tests indicate no problem with paralleling PICO fuses. Further tests on the effect of paralleling fuses during turn-on current surges are required.

Because other fuses may require more energy to blow than do PICO fuses, it is strongly recommended that only PICO or equivalent fuses, in conjunction with the ICTE-5 transient suppressors, be used.

4.9.2 Fusing Boards By Sectioning

ICTE-5 or equivalent transient suppressors can sustain enough power for a sufficient time (enough energy) to protect circuitry from overvoltages until the 5 amp PICO fuses open. Fusing boards by sectioning is recommended if this introduces no other problems.

Sectioning is dividing up the board circuitry into parts and fusing (and overvoltage protecting) each section individually. For example, if a board's +5V current draw is 14 amps the board's circuitry can be divided into three approximately equal current draw

‘sections’, each fused with a single 5 amp PICO fuse and each overvoltage protected with an ICTE-5 equivalent transient suppressor on the load side of the fuse.

A potential problem exists with fusing boards by sectioning, especially if the board contains some MOS circuitry. Destruction of certain types of MOS components can occur if they are unpowered but have powered inputs. This can occur, for example, when a fuse opens in the section with these MOS components but other fuses in other sections do not open. These types of MOS components should also not be driven directly from external inputs. See Section 4.8.4 for more details on partial power.

4.9.3 High Speed Signals and Sectioning Issues

Sectioning power or ground planes can have an effect on “high” speed signals. A signal that is over a plane induces a current in that plane which must arrive at the receiver in time with the driven signal. If these two currents arrive out of time, noise is generated and spurious signals may be generated by the receiver. Likewise, the driver has to receive the return current in time or signal distortion can occur.

Return current noise problems can be minimized by installing capacitors (typically 0.01 μF) across the cuts in the planes. Also, these capacitors are needed from each plane that has induced currents to the ground plane of the driver and receiver near these ICs. The spacing of the capacitors depends on the rise time of the signals. For a signal of rise time t_r the path difference between the driven signal and the induced signal should be less than L where $L = v_d/(4t_r)$ and v_d is the velocity of the signal on the board. For a 1 ns rise time signal a one inch grid will provide an acceptable solution.

4.9.4 Partial Power

The use of 3.3 V logic mixed with 5 V logic and the use of fuses has the potential for harming integrated circuits where the voltages interface. The following data is compiled from application notes written by Texas Instruments (TI).

The product feature one needs to look for when operating a mixed 3.3 and 5 volt board is “3.3 V logic with 5 V tolerance”. TI lists the following families and manufacturers as having this “tolerance”. The table also shows family equivalents between TI and other manufacturers.

Table 4.9.4-1
3.3-V logic with 5-V toleranc

TI	Fairchild	Hitachi	IDT	Motorola	Pericom	Phillips	Quality	Toshiba
ALVT					ALVT	ALVT		
LVT	LVT	LVT		LVT	LVT			
LVC	LCX	LVC	LVC	LCX	LCX	LVC	LCX	LCX
LV	LVQ LVX	LV		LVQ LVX		LV		LVQ LVX

“Partial power down and live insertion are becoming a major issue in today’s system designs. Many new standards have included this as part of their specification. The “plug-and-play” feature is beginning to dominate the PC market and the telecom industry has been using it for a long time. When a system is partially down, the unpowered device is expected to go into a high-impedance state so the device does not disturb or disrupt the data on the bus. When using standard CMOS devices, there is a path from either the input or the output (or both) to V_{CC}. This prevents partial power down for such applications as hot-card insertion without adding current-limiting components. This is not the case with ABT, LVT, LVC, GTL, and BTL, as these paths have been eliminated with the use of

either blocking diodes or current-blocking circuits. Figure 4.9.4-1 shows functionally-equivalent schematics of the input and output structures for these families. The data sheets contain more detailed information on the input and output behavior under these conditions.

In Figure 4.9.4-2 the driving device is powered with $V_{CC} = 5$ V while the receiving device is powered down ($V_{CC} = 0$). LV, ALVC, or ALB receivers can be powered up through diodes D2 and D3 when the driver is in a high state. ABT, LVT, LVC, GTL, and BTL devices do not have a comparable path and are thus immune to this problem, making them more desirable for power down applications. The electrical characteristics table in the TI data sheets have a specification called I_{OFF}. This specification shows the test condition and the maximum leakage a device can source or sink when V_{CC} is off. Refer to the individual data sheets for more details."

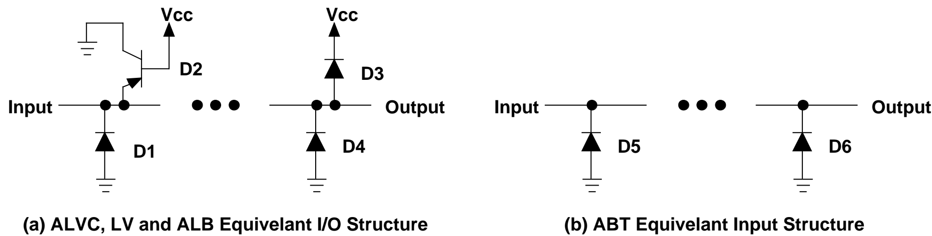

Figure 4.9.4-1
Simplified Input Structures for CMOS and ABT Devices

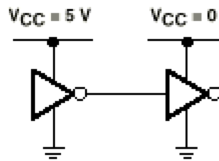

Figure 4.9.4-2
Example of Partial-System Power Down

(End of TI literature.)

4.10 What Voltages are on the bus? … The Designer's Dilemma

In producing Modules for a general market (as distinguished from a customer's special procurement for a particular implementation) the manufacturer is faced with the question as to what voltages and what bused power lines or planes will be available on the backplane. Though power is covered in Chapter 7 of VITA 23, the following summary is presented here for guidance of designers of Modules and Transition Modules:

+ 5 V: This has long been the principal voltage used on VMEbus Modules. The Module manufacturer can depend on the +5 V being bused on the backplane and connected to the backplane pins on J1 as required by the VME64 specifications and can depend on the +5 V power being provided to the backplane. (Note that an additional six, +5 V pins are on the J0 connector in all slots except slot 1 of VME64xP subracks.)

V1/V2 (nominal 48 V): The backplane is bused for this voltage and is connected to the J1 connector as required by the VME64 standard. The nominal 48 V supply is usually the logical choice for powering DC–DC converters within the Modules and is therefore very likely to be provided at the backplane. The 48 V is typically referenced with the positive terminal near ground.

Vw, Vx, Vy, Vz: As noted and detailed inVME64xP, Chapter 7, the recommended configuration for these user defined voltages is for high-power ECL implementation providing -5.2 V and -2.0 V. However, since they are User Defined, they are sometimes implemented with different voltages, for example ±15 V. Vw, Vx, Vy, and Vx are bused on J0 but only on VME64xP subracks, with the busing being to all slots except slot number 1. It is necessary to exercise extreme caution and not make any assumptions regarding these voltages and their availability. It is especially important to implement proper keying to avoid disaster.

+3.3 V: The use of +3.3 V power in new integrated circuits is increasing. The Module manufacturer needs to have the +3.3 V plane connected to the backplane connector J1 pins as required by the VME64 standard, but it is likely that many installations will not provide +3.3 V power to the backplane. Therefore, it may be advisable for the designer to consider providing any necessary +3.3 V power from on-board DC–DC converters. (See Chapter 10 herein.)

+12 V and –12 V: These voltages (as is the case with +5 V) are among the original VME voltages. Thus the manufacturer can usually depend on them being bused on the backplane and connected to the backplane pins on J1 as required by the VME64 specifications and can depend on the +12 V and –12 V power being provided to the backplane. The +12 V and –12 V supplies have been of low quality with high ripple. However, the quality of the supplies has improved in recent years and Observation 8.2-a points out that high quality ±12 V supplies can be utilized that will be useful for some analog circuitry.

+5 V Standby: These pins are bused on the backplane but typically not connected to any power supply.

VPC (voltage precharge): These pins are bused on VME64 Extensions compatible backplanes and typically connected to the +5 V power.

As pointed out herein, Module manufacturers are faced with the fact that some of the voltages required by circuitry within the Modules will not always be available on the backplane. On-board DC–DC converters considerably ease the problem in that respect and are also useful for high-resolution analog circuitry. The use of DC–DC converters will continue to increase as the variety of voltages required for solid state devices further proliferate. High quality, high efficiency converters are available from numerous sources. Chapter 10 herein provides useful information regarding their implementation.

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5 VME64xP Transition Modules

5.1 Introduction

A VME64xP Transition Module is a VMEbus Transition Module that conforms also to the rules in this document. A VME64xP Transition Module is inserted in the back of the subrack and mates with the rear of the backplane through the Transition Module connector(s). A VME64xP Transition Module includes a VME64xP Transition Board and a rear panel with its attachments. The rear of the Transition Module is defined here as the end that mates with the backplane. The Transition Module card cage is discussed in Section 6.4 of VITA 23.

5.2 VME64xP Transition Modules

Observation 5.2-a (Transition Module adapters):

The Transition Modules that are designed for 6U Module subracks will require adapters when used in 9U Module subracks.

Observation 5.2-b (board stiffeners):

Transition Modules of heights greater than 6U may require board stiffeners to align rear connectors within the insertion tolerances and to keep the board from encroaching on the neighboring Transition Module space. Stiffener bars may also be necessary with the bar located across the board vertically as close to the rear connectors as practical. The bar needs to be within the Module maximum component height as specified in IEEE 1101.11. If the front of the board is firmly attached to the front panel, the panel will act in lieu of a stiffener at the front of the board.

Observation 5.2-c (press fit connectors):

If press-fit connectors are used soldering problems are eliminated. Most connectors available are available only with press-fit and such connectors are not to be soldered (See Section 4.3 herein).

The RP0, RP4, RP5 and RP6 connectors can be purchased with optional shields that provide extra ground connections. The shield consists of a top shield and a bottom shield. When installed on the Module or Transition Module connector, the top shield makes contact with the 'z' row of the backplane connector, and the bottom shield makes contact with the 'f' row of the backplane connector. Mechanical constraints on some shields may not allow the use of a bottom shield, which contacts the backplane 'z' row, on the Module connector. This is due to the intrusion of the bottom shield into the adjacent interboard separation plane (see IEEE 1101.10). The top shield connects to the Module by utilizing every odd-numbered pin position in the Module 'f' row, and the bottom shield connects to every even-numbered pin in the Module 'f' row. Use of only the top shield allows the Module designer to drill only every other hole in the 'f' row, however, this would prevent the user from adding the bottom shield at a later time.

5.3 VME64xP Transition Module Front Panel

Recommendation 5.3-a (front panel issues):

1) A front panel should always be used.
2) A mounting bracket with lock washer should be used near the middle of the front panel to secure the panel to the module circuit board.
3) Lock washers should be used to secure the injector/ejector handles to the module circuit board and front panel. Note that these may not be in the kit from the manufacturer. One can also use Loctite 222® or equivalent on all screws.

4) The separation between the top and bottom injector/ejector handles should be carefully checked against the dimensions given in IEEE 1101.1 to prevent possible handle failures.

Observation 5.3-b (reverse):

Front panels used on Transition Modules have a left-right reversal to the ones used on the VME64xP Modules. See IEEE 1101.11.

Observation 5.3-c (front panels, connector isolation)

Transition Module front-panels are part of the overall EMI/EMC 'shield' and thus are not connected to power supply returns. This requires that any front-panel connectors be isolated from ground.

Recommendation 5.3-d (EMC/EMI front panels & analog circuitry)

Transition Modules and subracks containing high-resolution analog circuitry should use EMC front-panels and EMC-protected filler-panels as in IEEE 1101.11.

Suggestion 5.3-e (detailed power indicators):

An indicator on each voltage within the Module (on the load side of the fuse, if any) can help in trouble shooting. Due to panel space limitations these indicators may be interior to the Module.

5.4 VME64xP Transition Module Designers Dilemma

See Section 4.10 – "What Voltages are on the Bus?"

5.5 VME64xP Transition Module Shielding

As in Section 4.5.

5.6 VME64xP Transition Module Die and Module Temperatures

As in Section 4.8.

5.7 VME64xP Transition Module Circuitry Protection

See Section 4.9. Most issues apply to Transition Modules with active components.

6 Mezzanine Cards and Carriers

6.1 Introduction

A Mezzanine Card is a slim circuit board that is mounted in a Module parallel to the Module circuit board and is attached to the Module circuit board through one or more connectors. The "mezzanine concept" is to use general-purpose base boards that carry application specific mezzanine boards. This gives users an easy way to customize their systems with off-the-shelf or in-house designed components.

Base boards, or carrier, or mother boards, provide common infrastructure features (*e.g.*, backplane-bus interfacing, compute resources, networking capabilities, etc.) for the mezzanines connected to them. Mezzanines are also known as daughter boards or piggy-backs. Both carriers and mezzanines follow a "mezzanine-bus" specification that defines the mechanics and the electrical and logical layers.

Carriers exist as "intelligent" (with an onboard processor) or "dumb" (Slave-only capability) boards. One finds stand-alone or bus-based (*e.g.*, VMEbus, etc.) carriers. The mezzanines perform application specific functions, such as analog-to-digital conversion (ADC), digital input/output, graphics, communications, etc. Carriers and mezzanines exist in different sizes (form factors). Examples are 3U or 6U sized VMEbus carriers, and single- or double-width mezzanines, with or without front panel option. Typically, carriers can accommodate one to four mezzanines.

With the growing popularity of mezzanines, one could observe a proliferation of products and specifications. For instance, the VMEbus International Trade Association's VMEbus Product Directory lists vendors of company-specific mezzanine solutions. Mezzanine specifications were submitted for standardization to VSO (VITA Standards Organization) and the IEEE:

- VITA 4-1995 - IP-Modules
- VITA 12-199x - M-Modules
- VITA 14-199x - CXC / ModPack
- (IEEE) P1386 - Draft Standard for a Common Mezzanine Card Family: CMC
- (IEEE) P1386.1 - Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC

6.2 PMC and IP-Modules

Looking at possible application areas in physics, one finds a whole spectrum, ranging from simple industrial I/O to very-high bandwidth applications. It appears that, at least for the time being, no single mezzanine standard covers all system needs.

Observation 6.2-a (bandwidth issues):

An application-area overlap between IP-Module and PMC exists. Factors, like the existing environment (*e.g.*, predominantly industrial I/O or predominantly high bandwidth) will determine whether to choose one or the other (or both) mezzanine families in the specific case.

Observation 6.2-b (data transfer rates):

Peak data transfer rates for IP-Modules are 64 MB/s for the 32 MHz clock version and 32-bit wide implementation. PMC Modules are the preferred mezzanine card for high bandwidth applications, with their peak data transfer rate of 264 MB/s (64 bit

implementation). IP-Modules, with their smaller size and simpler protocol, are intended to cover application areas with lower bandwidth requirements.

Observation 6.2-c (flexibility):

Mezzanines provide a convenient base for in-house developments. Carrier boards provide infrastructure features, like networking capability, backplane bus interface, compute resources, graphics, *etc.* If designers base in-house developments on mezzanines, they can take advantage of these existing features, without having to (re)design them.

Observation 6.2-d (PMC Module carriers):

PMC Modules can be used on carriers based on buses other than VMEbus. Such carriers that provide I/O through the backplane will comply with the respective standards that define I/O mapping schemes.

Observation 6.2-e (IP-Module carriers):

IP-Modules can be used on carriers based on buses other than VMEbus. Such carriers that provide I/O through the backplane will comply with the respective standards that define I/O mapping schemes such as PICMG X, IP I/O Pin Assignment on CompactPCI (cPCI).

6.3 Power Dissipation

The PCI Local Bus Specification discusses power requirements, sequencing, consumption, decoupling, and routing. The PMC and IP specifications discuss mezzanine-specific power dissipation and should be consulted for details.

Observation 6.3-a (mezzanine card power dissipation):

Rule 4.3-l of VITA 23 concerns the total power dissipation within a Module, including that on mezzanine cards.

Observation IL.3-b (PCI power dissipation):

The PMC specification allows a maximum of 25 watts per card. The PMC specification suggests that cards over 10 watts have a controller that limits the power to less than 10 watts until the system sends a full power command. More details are in Chapter 4 of the PMC specification. See Section 5.1 of VITA 23.

6.4 Die And Module Temperatures

PCI and IP specifications do not state maximum temperatures. Good design practice requires that die temperatures are kept as low as practical to give maximum life to the semiconductors. The following are based on generally accepted engineering practice for air cooled computer equipment.

Recommendation 6.4-a (temperatures):

Mezzanine card and die temperatures should conform to the specifications, as appropriate, in Section 4.5 of VITA 23. See also Recommendation 4.3-l of VITA 23.

6.5 Cooling

PMC and IP specifications discuss cooling and can be consulted for details.

Recommendation 6.5-a (cooling):

The cooling for Mezzanine Cards should conform to the specifications, as appropriate, in Section 6.7 of VITA 23 and Chapter 9 herein. See also Section 4.8 herein.

Observation 6.5-b (cooling):

The mezzanine card becomes an integral part of the VMEbus Module when mounted and can affect the cooling of both the VMEbus Module and the mezzanine card. The cooling system needs to accommodate this mother/daughter board construction. Cooling information is contained in Section 6.7 of VITA 23 and Chapter 9 herein.

6.6 Circuitry Protection - Fusing and Overvoltage Protection

Observation 6.6-a (fuses and transient suppressers):

Section 4.6 of VITA 23 contains suggestions on protection of VMEbus Modules. Similar protection is recommended for Mezzanine Cards.

6.7 Compliance

The PMC specification states that each PMC vendor shall document in the product's literature to which electromagnetic compatibility, shock and vibration, environmental, and MTBF standards the product was designed and tested to (if tests were performed).

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7 VME64xP Subracks

7.1 Introduction

A VME64xP subrack is a VMEbus subrack that conforms also to the rules in this document. VME64xP subracks come in two basic sizes, one for use with 9U x 400 mm Modules, and the other for use with 6U x 160 mm Modules. Both subracks are typically 1U taller than the Modules that fit into them to allow space for the power supply connections to the backplane at the top of the subrack. This chapter describes both types of subracks in terms of general mechanics, the Module card cage, an optional Transition Module card cage, the backplane and the power supply connections.

Backplanes for VME64xP subracks that accommodate 9U x 400 mm Modules can be either full-height monolithic backplanes (hereafter referred to as J1/0/2/4/5/6 backplanes) or backplanes which cover only the J1, J0 and J2 areas (hereinafter referred to as J1/0/2 backplanes).

The mechanical and electrical specifications herein are such as to maximize backward compatibility with existent VMEbus standards.

VME64xP subracks are constructed in such a manner that, with the use of proper front and rear front panels and filler plates, the entire outside surface of the subrack forms a continuous shield that confines the electromagnetic noise. More information on Electromagnetic Compatibility (EMC) issues is available in Chapter 12 herein. Typical VME64xP subracks are described in Appendices A and B of VITA 23.

Connector designations and locations are shown in Figure 15.1-1 herein.

A VME64xP subrack is an assembly that, at a minimum, consists of:

- A Module card cage which holds the VMEbus Modules, providing mechanical support and alignment of the Modules with the backplane;
- A backplane which provides power distribution and inter-Module communication paths;
- A power connection assembly that interfaces external power supplies to the backplane.

Optionally, a VME64xP subrack may also include:

- A Transition Module card cage which provides mechanical support and alignment of Transition Modules which interface to the rear side of the backplane;
- A cooling apparatus which provides necessary air and/or water flow to remove excess heat generated by the Modules within the Module and/or Transition Module card cage.

7.2 VME64xP Subrack General Mechanical Specifications

VME64xP subracks consist of basic mechanical mounting structures that allow for modular construction. A user can usually purchase a VME64xP subrack without a backplane and Transition Module card cage from one manufacturer and the backplane from another, and at a later date decide to add a Transition Module card cage. (A typical VME64xP subrack accommodates 21 single-width VMEbus Modules).

In some applications there is a need to restrict the amount of EMI and RFI being radiated from the front of a subrack without the aid of a special cover. The EMC subracks, when used in conjunction with Modules and their front panels (Plug-in Units), are intended to provide this capability. Electrostatic discharge (ESD) provision requirements for Modules and for subracks are specified in IEEE 1101.10. Similar provision requirements for Transition Modules are specified in IEEE 1101.11. See also Chapter 12 herein.

7.3 VME64xP Subrack Module Card Cage

The Module card cage houses VMEbus Modules, providing mechanical support and alignment of the Modules to the backplane.

Recommendation 7.3-a (Modules sizes accommodated in subracks for 9U Modules):

Subracks for 9U Modules should accommodate 9U, 6U and 3U Modules in accordance with Appendix C of the VME64x9U. For an alternative construction see Observation 7.3-c herein.

Recommendation 7.3-b (Modules sizes accommodated in subracks for 6U Modules):

The subracks should accommodate 6U and 3U Modules in a manner similar to that shown in Appendix C of the VME64x9U. For an alternative construction see Observation 7.3-c herein.

Observation 7.3-c (alternative Module card cage construction):

The subrack for 9U x 400 mm Modules can incorporate mechanics to provide for the insertion of recessed 6U and 3U x 160 mm Modules. By using recessed card guides, modules with front panels and keying hardware attached such can mate directly with the backplane without the using extenders. Subracks constructed this way will need airflow blocking plates to ensure that cooling air does not escape from the slots that accommodate the 160 mm deep Modules.

A similar alternative applies to subracks for 6U x 160 mm Modules regarding the accommodation of 3U x 160 mm Modules though extenders or recessed rails are not needed. However, air flow directing plates are necessary. Note that such alternative Module card cages may require the use of special front panels on the 3U Modules. See Section 7.2.

Observation 7.3-d (guide rails for Modules):

The Module card cage top and bottom card guide rails conform to the guides specified in IEEE 1101.11. The rails and their supports meet load specifications per IEC 60297-3 and 60297-4.

Observation 7.3-e (air blockage):

When designing card cages it is important that attention be given to the flow of air through the card cage area. No obstructions are to be placed in the air path other than those necessary for the mechanical integrity of the card cage. The air flow to each card position should be as uniform as possible.

7.4 VME64xP Subrack Transition Module Card Cage

Subracks support the use of an optional Transition Module card cage. This card cage allows for the insertion of Transition Modules that interface to the rear side of the backplane. A VME64xP subrack can be constructed with or without a Transition Module card cage.

Observation 7.4-a (connector mating):

Note that mating with RJ4 is possible only for J1/0/2/4/5/6 monolithic backplanes since with split backplanes there will be no RJ4 connectors.

7.5 Subrack Power Connections

Power connections from external power supplies to the subrack are made through a Power Supply connection Assembly that consists of:

- A Power Supply Attachment Bulkhead (PSAB), and
- A Bulkhead to Backplane Power Connection Assembly (B-BPCA)

The Power Supply Attachment Bulkhead (PSAB) is located at the rear upper 1U of the subrack. It provides the connection points to which the power supply outputs are connected for routing to the backplane through the busses and cables that constitute the Bulkhead to Backplane Power Connection Assembly (B-BPCA). The B-BPCA has to be adequate to carry the currents required but with limited obstruction of the airflow in the Transition Module card cage (See Rule 6.7-c and Rule 6.7-d of VITA 23). In addition, the Bulkhead requires sufficient mechanical strength to withstand the torque exerted during cable attachment and removal.

General power connection items are included in this section. Connections from the backplane to the subrack power supply attachment bulkhead are covered in Section 7.6. Connections from the power supplies to the subrack power supply attachment bulkhead are covered in Section 7.7. Remote sense is discussed in Section 6.6 of VITA 23 and in Section 7.8 herein.

The assembly, including voltage and return bus bars, cables and their connections for power supply cable lugs, should be supported to prevent shorts to each other or to other parts of the subracks and be sufficiently rigid to withstand the torque associated with connecting and disconnecting the cables.

Subracks require a cover that serves to protect the bus bar, cable connections, including the conductive parts of the power supply cable lugs, against shorts due to objects dropped from above. The cover needs to be removable so as to permit easy installation and removal of the power supply cables.

7.6 Subrack Power Supply Attachment Bulkhead (PSAB)

The area in the rear of the subrack that is used for connections to the backplane power feeds is referred to as the Power Supply Attachment Bulkhead (PSAB). Typically power cables and sense cable(s) attach on the PSAB. The PSAB may also contain connector(s) which are used to monitor the subrack power.

Observation 7.6-a (bus bars and cables to backplane):

Bus bars and cables connecting to the backplane are user specified.

Recommendation 7.6-b (cable connections for minimal subrack depth):

Cable connections to the subrack should be such that minimal depth at the rear of the subrack is required for the connections.

Observation 7.6-c (stud current density):

If the power supply connection lugs are designed for a current density of less than 6000 A/in^2 they generally meet safety codes. The allowed current density needs to be checked against local codes before designing power connections.

Observation 7.6-d (V1 and V2 power connections):

The V1 and V2 pins are assigned to nominal 48 V power. In some instances the nominal 48 V may differ such that V1 is used for one value of the nominal 48 V and V2 for another. If that is not the case and it is desired to utilize the combined current capacity of V1 and V2 for a single nominal 48 V, +V1 and +V2 can be tied together. In that case –

V1 and –V2 would be commoned. In most systems the positive V1 and V2 pins are near ground.

Observation 7.6-e (Vw, Vx, Vy and Vz implementations):

Sections 7.2-e and 7.2-g of VITA 23 have recommendations regarding use of Vw, Vx, Vy and Vz.

Recommendation 7.6-f (Vw, Vx, Vy and Vz power connections):

At the power supply connection bulkhead, power supply connections to Vw, Vx and their two RET_WX connections should be grouped together. Similarly, Vy, Vz and their two RET_YZ connections should be grouped together. All eight connections should also be adjacent to facilitate additional groupings. By grouping these connections the user can easily tie power connections together with copper bars. As a result, common supply(ies) of higher current may be formed from combinations of Vw, Vx, Vy and Vz. The copper bars connect the voltage connections should be made above the power supply connection bulkhead voltage connections so if a protective cover was used it would not interfere.

For example, suppose a user needed 180 A of –5.2 V and 60 A of –2.0 V. A copper bar capable of carrying 180 amps could connect Vw, Vx and Vy forming the desired "extra" –5.2 V on the backplane for that particular application. The –2 V would connect to Vz and carry 60 A. Similarly, for a subrack for 6U Modules, such an implementation would permit 60 A of –5.2 V and 20 A of –2 V. The positive side of the –5 v and –2 V supplies would both connect to the RET_WX and RET_YZ connections and also to COM.

7.7 Power Connections to Subrack

Observation 7.7-a (cables to subrack):

Cables from external power supplies connect to the rear of the subrack, typically to the Power Supply Attachment Bulkhead (PSAB). In many cases they enter vertically from above and attach without bends though the manner of entering can vary depending on the particular installation.

Observation 7.7-b (power connection techniques):

Power connections do not rely on screws or bolts as the current-carrying paths. Only the connection surface of the cable lug and its corresponding contact pad determines the current capacity. Where bolts are used to provide compression connection via lug surfaces, conductive joint compound can be used to avoid oxidation and a conical compression washer (*e.g.,* Belleville washer) utilized. Materials utilized for conducting electrical currents need to be suitable for such usage. Any power bus connections made by means of plugs and sockets utilize connectors classified as gas-tight and are employed within their rated current capacities.

Table 7.7-1
Power Cable Sizing Chart

Current in Amps	AWG Wire Gauge (Metric Gauge)	R/1000 ft in ohms (R/km)	Voltage Drop in mV/inch (mV/cm)	Length for 100 mV Drop in inches (meters)
300	4/0 (120)	0.0537 (0.0164)	1.343 (0.5285)	74.5 (1.892)
300	3/0 (100)	0.0678 (0.0207)	1.695 (0.6673)	59.0 (1.499)
300	2/0 (90)	0.0852 (0.0260)	2.130 (0.8386)	46.9 (1.191)
100	2/0 (90)	0.0852 (0.0260)	0.710 (0.2795)	140.8 (3.576)
100	1/0 (80)	0.1080 (0.0329)	0.900 (0.3543)	111.1 (2.822)
100	#2 (70)	0.1690 (0.0515)	1.408 (0.5545)	71.0 (1.803)
60	1/0 (80)	0.1080 (0.0329)	0.540 (0.2126)	185.2 (4.704)
60	#2 (70)	0.1690 (0.0515)	0.845 (0.3327)	118.3 (3.005)
60	#4 (50)	0.2485 (0.0757)	1.243 (0.4892)	80.5 (2.045)
30	#4 (50)	0.2485 (0.0757)	0.621 (0.2446)	161.0 (4.089)
30	#6 (40)	0.4190 (0.1277)	1.048 (0.4124)	95.5 (2.426)
30	#8 (35)	0.6610 (0.2015)	1.653 (0.6506)	60.5 (1.537)
10	#10 (25)	1.1800 (0.3597)	0.983 (0.3871)	101.7 (2.583)
10	#12 (20)	1.8700 (0.5700)	1.558 (0.6135)	64.2 (1.631)
10	#14 (16)	2.8700 (0.8748)	2.392 (0.9416)	41.8 (1.062)
10	#16 (14)	4.5400 (1.3838)	3.783 (1.4895)	26.4 (0.671)

Observation 7.7-c (power wiring guide):

Table 7.7-1 is a guide for system engineers sizing cables for power supplies. Many low voltage power supplies have 500 mV or less for remote sensing. The cables that connect these supplies to the subracks have to not only be rated for their current carrying capacity but also for the voltage drop. Table 7.7-1 shows the minimum wire size for each current and also the wire size based on the connection length that will result in a 100 mV drop on that wire at the specified current.

If the system designer sizes the power cables so that a known drop results (*e.g.* 100 mV) at the rated output of the power supply, then that voltage drop can be sensed by external circuitry for current monitoring. The power connection cable and the connections from the subrack power connection to backplane connector pins act as a shunt (>100 mV) but do not get additionally deducted from the remote sense voltage drop budget.

7.8 Recommended Remote Sense and Monitoring

Recommendation 7.8-a (remote monitoring):

Wherever possible, a remote monitoring connection should be provided on a panel-mounted connector for routing to external monitoring systems. The remote monitoring can either utilize contacts in the connectors used for remote sense (see Rules 6.6-a and Rule 6.6-b of VITA 23) or can use separate connectors. However, the remote monitoring connections should be resistively isolated from the remote sense connections. The monitor connections should utilize an independent path such that current drawn by the remote monitoring system or faults in it (*e.g.* shorts) do not adversely affect operation of the remote sense.

Observation 7.8-b (VMEbus power status signals):

If signals are available from external power monitoring hardware they can be transmitted to the subrack via the remote monitor connector. These utility bus signals are specified in VME64 and include SYSFAIL*, ACFAIL* and SYSRESET*.

7.9 Busbar Sizing

Observation 7.9-a (bus bar current density):

General practice for bus bar design limits the current density to less than 1000 amperes per cmil. The user is urged to check local codes.

7.10 VME64xP Subrack Cooling

Observation 7.10-a (fans):

For high power systems muffin fans are generally not adequate. Because of the air flow required, the air handling system requires blowers that can deliver the necessary volume against the high back pressure. Squirrel cage blowers are usually the choice. They tend to emit less acoustical noise than other high-pressure blowers.

Recommendation 7.10-b (blower assemblies):

When a blower assembly is specified it should extend from the front of the subrack to the rear of the Module area or the rear of the Transition Module area, as specified by the user. A blower assembly in a 21 slot subrack for 6U Modules should typically provide sufficient air flow to cool 1 kW of electronics evenly distributed within the subrack at an ambient temperature of 30 °C. A blower assembly in a 21 slot subrack for 9U Modules should typically provide sufficient air flow to cool 2.5 kW of electronics evenly distributed within the subrack at an ambient temperature of 30 °C. A plenum can be useful in achieving this even distribution. In some implementations the Transition Modules are lightly loaded and the user can specify an air flow distribution that differs from the above.

Recommendation 7.10-c (cooling objective):

Subrack cooling should be such that the temperatures for the Modules and Transition Modules conform to the requirements of Section 4.5 of VME64xP. System cooling issues are discussed in Chapter 9 herein.

8 Subrack Power

8.1 General

This Chapter provides information regarding voltages on the backplane and recommended configurations for providing power for ECL and analog circuitry. Thus it is closely related to Chapter 7 of VITA 23.

The primary source of power for a VITA 23 system is the Subrack Power Supply that provides power to the subrack backplane. Additionally, on-board DC–DC converters (as discussed in Chapter 10 herein) are increasingly used:

- to supplemental power;
- to provide power at voltages not available from the backplane, and
- for use with high resolution analog circuitry or for other circuitry requiring isolation.

For maximum analog resolution, special care needs to be employed in the layout and design of the printed circuit board power distribution.

The reader is referred to Appendix D of VITA 23 for typical power supply specifications that can be used as a guide for purchase orders.

8.2 Voltages on VME64xP Backplane

In accordance with the VME64 specification, the subrack backplane has provision for providing power to the subrack slots at the +5 V, +5 V STDBY, +12 V and –12 V connector pins. See also Section 4.9 herein.

The VME64 Extensions standard defines pins at the backplane for +3.3 V and "48 V" (V1, V2) power. The "48" volt supply is intended primarily for the powering of on-board DC-DC converters.

In addition to power at the voltages designated in VME64 and VME64x, power at the various voltages, designated Vw, Vy, Vx and Vz can is bused to the J0 connectors on VME64xP Type A-7U and Type A-10U subrack backplanes (see VME64xP, Appendices A and B). Typically, these voltages could include –5.2 V and –2.0 V primarily for ECL circuits and +15 V and –15 V primarily for analog circuitry.

Observation 8.2-a (superior 12 volt output):

If 12 V supplies are provided that have superior output specifications and low noise, they can be suitable for some analog applications and thus eliminate the need for providing separate analog supplies.

Suggestion 8.2-b ("48 V" for DC-DC converters):

If Modules that use "48 V" for DC–DC converters have wide-input-range converters, they will minimize the potential for failure due to the different "48 V" supply seen in various countries.

Observation 8.2-c (powering of DC-DC converters):

Though voltages other than 48 V can be used to power DC-DC converters, it is advantageous to use the 48 V because of the improved efficiency and the isolation from other circuitry. The isolation provided by the 48 V can minimize the noise from the DC-DC converters that is coupled into other voltage rails which power potentially sensitive circuits.

Observation 8.2-d ("48 V" and OSHA):

In the United States, the nominal value of 48 V is derived from common usage in the telecommunications industry. In addition, power supplies in excess of 50 volts are subject to OSHA regulation 1910.303(c)(2)(i), Guarding of live parts, a partial quote of which is: "...live parts of electric equipment operating at 50 volts or more shall be guarded against accidental contact by approved cabinets or other forms of approved enclosure, or by any of the following means:..." , after which a discussion of various methods follows. For the precise wording of the regulation, the reader is referred to Occupational Safety and Health Standards for General Industry, 29CFR Part 1910, available from Commerce Clearing House Inc., 4025 West Peterson Avenue, Chicago, IL 60646.

Observation 8.2-e ("hazardous" voltage level):

Underwriters Laboratories in the United States, and other standards in Europe, define any system which has a potential difference of 60 volts or more to be 'hazardous'. The combination of 48 V and any voltage higher than 12 volts of opposite polarity in the VIPA subrack will normally provide a potential difference greater than 60 volts, which can require special certification or lockout procedures.

Observation 8.2-f ("48 V" supply safety requirements):

The actual voltage of the nominal 48 V supply, when added to the maximum other voltage of the opposite polarity, needs to be limited so as to comply with the safety requirements of the country involved.

Observation 8.2-g (setting "48 V" supplies for UL compliance):

To accommodate the Underwriters Laboratory (UL) rule for hazardous equipment, systems using +15 V, consider setting the negative side of the 48 V supplies to no more than -45 volts. Another option is to offset the positive side of the 48 V volt supply by +3 volts thereby maintaining the 60 volt UL maximum.

Observation 8.2-h ("48 V" elsewhere):

The use of 48 V is common but not universal. To conform to a specific nation's safety rules a technique similar to that in Observation 8.2-g may be needed.

8.3 Recommended Configuration of Vw, Vx, Vy and Vz for ECL Circuitry

Although many combinations of Vw, Vx, Vy and Vz are possible, the strongly recommended configuration is advisable in order to provide interoperability between Modules and systems. This implementation of Vw, Vx, Vy and Vz provides power for Modules which incorporate ECL logic. Typically 1/3 to 1/2 the -5.2 V current is required for –2.0 V terminations: thus three of the Vw, Vx, Vy and Vz voltages are -5.2 V and one –2.0 V.

9 Rack System Configuration

9.1 Introduction

This Chapter is intended to assist the VMEbus system designer in assembling subracks and racks of VMEbus Modules into a system. It includes guidelines for bringing 3-phase AC power into a rack as well as rack cooling and protection guidelines.

9.2 Rack Powering - 3 Phase AC Input Power

High powered systems, *e.g.* those drawing more than 30 amperes single phase should design the AC power distribution around 3-phase AC. With a modest amount of care, imbalances in the legs can be avoided. High power DC supplies can operate more efficiently on higher input voltages. The wire gauges are smaller for the same AC power delivered. 10 kW of AC power can be delivered with modest sized connectors. If more than 10 kW is needed the size of the connections nearly triples under UL ratings. 10 kW lets one design a rack with three 2.5 kW subracks and have 2.5 kW waste heat from the power supplies, *e.g.* about 75% efficient.

Recommendation 9.2-a (three-phase rack power):

When connecting loads to 3-phase, 208Y, 120 VAC, system implementers should attempt to balance the loads between the three phases, and minimize the harmonic currents due to non-linear loads.

9.3 Rack Cooling

In single self contained subracks or test stands air cooling is usually adequate. However, a combination air/water cooling is more effective for racks with multiple subracks. A large centrifugal blower and inter-subrack heat exchangers offer more cooling and higher reliability than arrays of small fans. Calculations regarding cooling are not necessarily accurate since all the parameters are not always known accurately. Any system needs to be prototyped and tested before committing the design to production.

9.3.1 Air Cooling

Observation 9.3.1-a (air flow):

An air flow of 108 liters per second (230 ft^3/min) in a subrack for 9U Modules operating at a power level of 2 kW is usually suitable.

Observation 9.3.1-b (temperature rise):

The temperature rise of the air flowing through a 9U subrack dissipating 2 kW will be about 8^oC (15^oF) for an air flow of 108 L/s (230 ft^3/min).

Observation 9.3.1-c (air velocity):

For proper cooling the linear velocity of the air stream is also important to achieve sufficient heat transfer. A higher velocity will create more turbulence and hence increase the heat transfer. Calculating the volume flow only does not necessarily insure proper cooling of all components. An air velocity of 2.5 m/s (500 ft/min) is generally a good number for initial design.

Observation 9.3.1-d (noise):

Noise can be generated by air passing over edges at high velocities. An air system with velocities over 5 m/s (1000 ft/min) can generate such noise. Since 80% to 90% of the maximum heat exchange is typically achieved at velocities below 5 m/s one can limit this source of noise.

9.3.2 Air/Water Cooling

Observation 9.3.2-a (water flow):

In a closed, re-circulating system with air/water heat exchangers, a subrack for 9U Modules dissipating 2 kW can be satisfactorily cooled by the combination of a water flow of about 7.6 L/m (2 Gal/min) with an airflow of 108 L/s (230 CFM). These parameters will result in a temperature rise of 15 °C for the air and of 4 °C for the water.

Observation 9.3.2-b (temperature rise of cooling water):

Water flowing through a typical air/water heat exchanger at a flow of 3.8 L/m (1 Gal/min) will rise in temperature about one degree Celsius per 250 watts of absorbed heat energy.

9.4 Rack Protection

This section describes a typical rack protection system, discussing the list of properties that are measured, what faults may be sensed, and the typical reaction to each type of fault. The system described in this section is not all encompassing, but does provide a reasonable level of protection for most rack-based electronics.

A rack protection system monitors the operation of the cooling water and cooling air systems, equipment temperatures, power supply voltages and currents, and watches for smoke. The system provides local interlocks to shutdown equipment if hazardous situations such as power supply over temperature, smoke, water leaks, or blower failures occur. The system also provides for monitoring via computer. A Rack Monitor Interface is employed to interface the rack environment sensors (smoke, drip, water flow, blower) into the control system and to provide local power supply interlocks. The rack protection system does not consist of a single chassis or a single interlock path.

Rack monitor, integral sensors, fuses, hazard detectors and an AC distribution chassis working together form the Rack Protection System. Each subsection is mounted within the rack at the point where the hazard is monitored. The various sensors are interfaced together via wires that all tie together at the Rack Monitor, as shown in Figure 9.4.1.

The system designer can, if desired, implement the rack protection in such a way that detection of a fault condition first alerts appropriate personnel and then instigates automatic shutdown only if the fault persists or increases in severity. This "two-step" approach allows for manual intervention before automated response, which can reduce false shutdowns, but also creates the possibility of greater damage in a true fault condition. This document suggests a "one-step" response while allowing the designer the freedom to choose otherwise for their particular application. "Two-step" approaches are sometimes adequate for over-temperature or water flow sensors. The "two-step" approach is not appropriate for critical sensors such as smoke, humidity or water leak sensors.

9.4.1 General Features

Figure 9.4-1 shows the basic components of a rack protection system. The "intelligence" in the system is typically both local and in the central monitor computer. In addition, the monitor should have some hard trip points built in if the computer(s) are down. The monitor computer should maintain a "long" term data

base on all sensor readings. Trend analysis can help spot potential trouble points before actual failure occurs. This is especially true for power supply monitoring. In many cases slight "wandering" of the supply out of the trend line can flag imminent failure. For example an output filter capacitor beginning to fail will result in more output ripple. Since the voltage is sampled the measurements will be taken at different points on the increased ripple. As a result an increased spread in voltages will be detected.

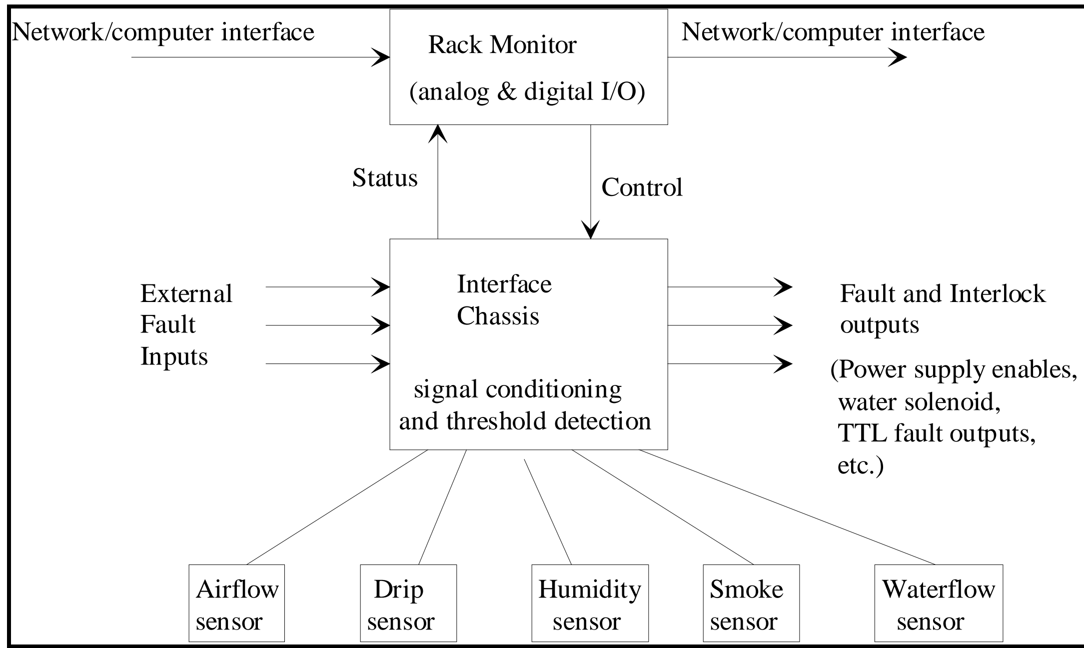

Figure 9.4-1
Typical Rack Protection System

Recommendation 9.4.1-a (local control):

The monitor should be designed so it can be controlled locally. This is important for testing and debugging. Also, the main computer may not be on-line or available.

Recommendation 9.4.1-b (fail safe):

The monitor should be designed to be fail safe independently of the computers. Failure of fans for more than a few seconds, smoke detected, etc. should cause the system to be powered down without waiting for computer shut down commands.

9.4.2 Cooling

The wide variety of possible rack configurations renders simple measurements of airflow unreliable as general indicators of proper heat removal. A carefully designed system can have strategically placed airflow sensors which provide useful information about heat transfer, but the average system has air flows too turbulent for airflow monitoring to be effective. To that end, this document recommends the use of over-temperature monitors, combined with direct fan operation sensors, to provide rack protection. Airflow monitoring, if desired, is an excellent addition in those systems where proper engineering analysis has determined the correct points at which airflow can be reliably used to measure heat transfer. A more direct approach to temperature measurement is to place temperature sensors on the boards in the subracks themselves.

Recommendation 9.4.2-a (temperature measurements in open-loop air-cooled systems):

Temperature measurements in open loop air-cooled systems should be made at the air exhaust point. An additional sensor at the air intake can provide ancillary information regarding the temperature rise through the rack, which gives an indication of the performance of the cooling system. As air flows are usually uneven, a set of sensors at exhaust and inlet, averaged together, often provides more accurate temperature measurements.

Recommendation 9.4.2-b (temperature measurements in closed-loop air-cooled systems):

Temperature measurements in closed loop air-cooled systems should be made at the hottest point within the rack. An additional sensor at the coolest point can provide ancillary information regarding the temperature rise through the rack, which gives an indication of the performance of the cooling system. As air flows are usually uneven, a set of sensors averaged together often provides more accurate temperature measurements.

Recommendation 9.4.2-c (temperature measurements in water-cooled systems):

Temperature measurements in water-cooled systems should include water inlet and outlet temperature measurements in addition to the appropriate air temperature measurements. The temperature rise of the cooling water supply is the critical measurement and should always be made.

Observation 9.4.2-d (water flow control):

The temperature difference of the inlet and outlet water in a heat exchanger can be used to throttle the water flow and thereby optimize the size of the chilled water source. Typically the flow control valve is used to restrict the water flow until a temperature difference of no more than 5 °C is achieved.

Suggestion 9.4.2-e (water flow detection sensors):

Water flow detection sensors can be located in the exit pipe of the rack cooling water. The sensor should be of the vane or turbine type with an output proportional to the flow rate. This sensor should not be used in lieu of the heat exchanger water temperature sensors discussed above.

Recommendation 9.4.2-f (water flow detection action):

When the water flow sensor detects that water flow has fallen below preset limits (as determined by the system designer) the sensor should initiate action to disconnect power from the rack.

Observation 9.4.2-g (temperature sensor type):

Many different types of sensors can be used to monitor temperatures within a rack. Some common types include the AD592BN and AD22100AT by Analog Devices and LM35CZ by National.

Recommendation 9.4.2-h (over temperature action):

Any monitor within a rack that senses temperatures above 50 °C (122 °F) should initiate action to disconnect power from the rack and alert appropriate personnel.

Recommendation 9.4.2-i (fan speed sensor):

A fan speed sensor should be mounted on every fan in the system that gives an indication that fans are operating at rated speed. Any fan that operates at less than 80% of rated speed should initiate action to alert appropriate personnel.

Recommendation 9.4.2-j (rack air velocity sensor):

An air velocity sensor, if implemented, should be located in an unobstructed plenum above the uppermost subrack in the rack and should be monitored. This sensor can either directly measure the velocity as an analog quantity or as a simple 'yes/no' sail type. An air velocity sensor should alert appropriate personnel upon detecting air flow less than 1.3 m/s (250 ft/min).

9.4.3 Smoke Detectors

Recommendation 9.4.3-a (smoke detection sensor):

Smoke detection sensors should be located at the top of the rack and should be monitored. Two types of smoke detector are commonly used, ionization and particulate detection. Ionization detectors are normally used, except in those areas subject to ionizing radiation.

Observation 9.4.3-b (ionization sensors):

Ionization sensors have a small radioactive source (typically Americium) which ionizes the gas in the smoke and causes current to flow between electrodes.

Observation 9.4.3-c (particulate sensors):

Particulate sensors use an LED and a sensor to detect decreases in the transmitted light. Smoke particles in the air will attenuate the light at the sensor.

Recommendation 9.4.3-d (air velocity and smoke sensors):

The sensor should be mounted so that high velocity air does not impinge on the unit. High velocity air can invalidate the sensitivity of the detector. Baffles can be used but they should not restrict the air infiltration to the sensor such that it has a long lag time, e.g. more than an additional 15 seconds.

Recommendation 9.4.3-e (smoke detection action):

When smoke is detected in a rack the sensor should initiate action to disconnect power from the rack.

Recommendation 9.4.3-f (fire system alert):

It is recommended that the rack smote detection system be connected to the fire department enunciator panel so they are automatically alerted.

9.4.4 Leak Detectors

Recommendation 9.4.4-a (water leak detection sensors):

Leak detection sensors should be located at the bottom of a rack containing air/water heat exchangers and should be monitored. For detection of leaks from the cooling water loop there should be provision for as many detectors as the application requires. Sensors should be placed in proximity to possible leak points or in a position to catch leaking water as it falls from water carrying components. The sensors should be of the conductivity type. Sensors using flat parallel screen mesh plane construction mounted under heat exchangers and planar interdigitated conductor types for surface mounting in the lower parts of the rack are recommended.

Recommendation 9.4.4-b (water leak detection action

When a water leak is detected in a rack the sensor should initiate action to disconnect power from the rack and discontinue water flow.

9.4.5 Humidity Sensors

Recommendation 9.4.5-a (humidity sensor):

A relative humidity sensor that alerts appropriate personnel if condensation conditions exist should be located at the top of the rack.

Observation 9.4.5-b (humidity alert):

The warning point for humidity sensors is dependent on the environment in which the electronics is operated. The warning point should be 5 °C above dew point since this type of sensor in difficult to manufacture to high accuracy.

9.4.6 Interlocks

Recommendation 9.4.6-a (external interlock connections):

All rack protection systems should provide a minimum of two external interlock connections (input and output) which allow daisy-chaining of racks and/or interlocking by remote devices, such as high voltage power supplies, gas monitors or building fire protection systems. All rack protection systems should provide a minimum of one isolated relay output which activates an alarm upon the first occurrence of any alarm condition or power failure and continues to indicate the alarm condition until power is restored and all alarm conditions are cleared. The typical implementation of this is a relay that is energized by the combination of power on and no alarms present. Upon power off or any alarm, the relay de-energizes and stays in that state until power is on and all alarms are cleared. This "fail-safe" mode of operation ensures that the alarm system still functions even if the cables become disconnected.

Recommendation 9.4.6-b (jumper or switch response programming):

For each quantity measured which provides a warning and/or alarm status, the capability should be made available to selectively disable any individual warning or alarm in any combination at the time of installation. When disabled, the status for that sensor should default to the normal no-fault condition. This feature should be used to disable the response to any status that is not implemented or not appropriate for the particular application. An example would be the disabling of the water flow and leak detection status in a rack system that does not use water for cooling. A set of jumper blocks or internal programming switches is suitable for this purpose.

Recommendation 9.4.6-c (disconnected warning components):

The system should respond with the highest enabled warning and/or alarm if any sensor is disconnected.

9.4.7 Alarms

Recommendation 9.4.7-a (audible and visual alarms):

All alarm conditions should have an audible alarm indication and a unique visual indicator for each type of sensor within the system. In addition, some form of reporting to a remote computer system should be provided.

9.5 Electrical Safety

Electrical safety issues are dependent on the country in which the equipment is being operated. The system designer should always become familiar with the local codes. The following items are general issues and apply to many different environments.

9.5.1 AC Power

Recommendation 9.5.1-a (rack AC power input):

AC power to equipment should be supplied through a circuit breaker incorporating an under-voltage and over-voltage trip. Other alarm conditions should also trip the breaker. This breaker should be controlled by the rack protection system and should disconnect the AC power from all loads in the protected rack except the rack protection system.

Recommendation 9.5.1-b (rack protection system power):

The rack protection system should receive power from a source independent of the rack circuit breaker. This insures that any alarm status is maintained after the rack has been shut down.

The following is considered good practice in many installations. It is recommended that the user check local codes and safety rules before implementing safety circuits.

Recommendation 9.5.1-c (power supply input power):

Power supply inputs should be protected by a circuit breaker. For systems connected to multi-phase power (*e.g.* 208/220 VAC), all phases of the line should be protected with ganged breakers such that all connected phases are opened upon fault detection. Neutral and earth ground connections should not be broken.

9.5.2 DC Power

The following rules denote equipment that is required in racks for protection of the power supplies and personnel operating that equipment (see also Chapter 8 herein and Appendix D of VITA 23). The individual installation needs to be carefully checked for compliance with the local codes and safety rules for other protection devices that might be required. The following Rules might be used in specifying a safety system for power supplies.

Rule 9.5.2-a (output protection):

Output of each supply shall be short-circuit protected. Fold-back current limiting shall not be employed. A continuous short circuit shall not damage the supply.

Rule 9.5.2-b (output limiting):

The outputs shall be protected by limiting circuits so that under no power supply failure, turn on conditions or turn off conditions will the output voltage exceed the lesser of 15% or 1.0 V above the nominal output voltage except for the “48 V” supply.

Rule 9.5.2-c (“48 V” protection):

The over voltage protection for the “48 V” supply shall operate such that the maximum safe voltage is not exceeded.

Rule 9.5.2-d (thermal protection):

Thermal protection circuits shall be provided and shall disable the supply when the temperature exceeds a safe operating value.

Rule 9.5.2-e (recovery from protection trip):

Operation of the protection circuits shall not damage the supply.

9.6 Protection and Cooling of Test Stands

Typical test stands consist of the devices under test, an oversized power supply, and insufficient and poorly mounted air cooling. As such, the usual test stand presents numerous hazards to designers and hardware alike. Proper test systems will use the guidelines presented here for equipment in permanent installations.

Recommendation 9.6-a (test stand rack protection systems):

Test stands should have rack protection and cooling similar in scope to final installation racks. Test stand rack protection systems should not, however, prohibit the designer from creating stressful environments to fully test the operational envelope of the design.

10. DC to DC Converters: Usage Guidelines

10.1 Introduction

The use of a distributed power architecture can provide distinct advantages to the system designer. The VME64 Extensions backplane includes a bus for supplying a nominal 48 volts from a bulk power supply to the Module slots. DC-DC converters can be used on the individual VMEbus Modules to provide locally generated voltages, derived as needed from this “48” volt supply. The DC-DC converters can be used to provide voltages that are unavailable from the standard VMEbus power supplies; or to provide isolated power supplies for sensitive analog circuitry. However, the use of DC-DC converters requires careful attention to fundamental engineering practices. Noise and heat are the two most significant problems to be solved. Improper application can result in high output noise, poor load regulation, excessive temperature rises, and power bus instability. The requirements of the application have to be well understood before selecting and implementing a converter.

The variety of commercial converters is broad enough that a close match can be found for nearly any application. Inadequate engineering at the beginning of the design process will result in poor converter selection requiring eventual engineering compromises such as added input and output filtering, after-the-fact thermal management or reduced performance specifications. Some guidelines for implementing DC-DC converters are provided in this Chapter.

The most important guideline is to "follow the manufacturers recommendations". Vendors provide excellent application information.

10.1.1 Single Converter for Different Voltages

Many DC–DC converters are available with multiple output voltages. Some converters can provide all the necessary voltages in a single package, minimizing layout, noise and thermal management problems.

10.1.2 Multiple Converters for Same Voltages

Use of multiple sources for the same voltage introduces internal loop currents from the inevitable mismatches between various drivers of the same voltage. These loop currents flow from one source to the other through the very small resistance of the power supply connection traces, and can dissipate surprisingly large amounts of power.

Recommendation 10.1.2-a (recovery from protection trip):

Unless absolutely required by the application, multiple sources should not be used for the same voltage. Specifically, the situation should be avoided where a DC–DC converter is used in parallel with a voltage taken directly from the backplane. If forced into this situation (*e.g.*, to increase available current), then multiple, independent power planes should be implemented.

Recommendation 10.1.2-b (DC–DC converters slaved to each other):

If DC–DC converters are connected in parallel (*e.g.*, to increase available current while distributing thermal loads), DC–DC converters that are specifically designed to be slaved to each other should be used.

10.1.3 Pertinent Converter Specifications

Precision, low noise, high efficiency DC–DC converters are expensive and are not to be specified unless required by the application. An over-specified converter can easily cost 10 times that of an adequate commercial unit. On the other hand, an inadequate unit would fail to perform as required and could degrade the performance of the design and perhaps even degrade the performance of other modules in the subrack (by conducted and radiated noise or by excess heating). The following list of specifications and comments is intended to prompt the designer to consider the issues involved in the initial selection process.

- Case Material: Choose models with six sided continuous metal case shielding for minimum radiated emissions and maximum thermal efficiency.
- Cooling: Be aware of the converter's cooling requirements. Some models require heat sinks and/or specified airflow if they are to provide maximum output.
- Efficiency: Choose high efficiency models for power levels above ≈ 5 watts. The extra cost will be offset by the decreased attention required to thermal management.
- Input Reflected Ripple: Choose models with low input reflected ripple to minimize conducted and radiated noise along the "48 V" subrack bus. Better models incorporate input filters. Some venders offer separate external filters that can reduce input line reflected ripple current to below the strictest of standards.
- Input Voltage Range: If the "48 V" power supply is used (as opposed to +5 V or ±12 V), then note that the VME64 Extensions allows a voltage range of 38 V to 75 V. Thus, a converter is chosen which utilizes this input range. (Safety rules in the USA require that the maximum differential voltage in a system be no greater than 60 V.)
- Inrush Current Limiting: It is desirable to limit the inrush currents in high current applications. Many converters have internal limiting.
- Output Ripple and Noise: Be more concerned with the peak to peak value than with the RMS value unless output filtering is planned. Choose models with noise levels commensurate with requirements. For example, an analog circuit that digitizes a 0 to 10 V signal with 12 bits of accuracy resolves to 2.44 mV per LSB. Since analog circuits have very low power supply rejection ratios at the frequencies used by DC–DC converters, it is important to use a low noise converter or to add output filtering. Digital circuits are far more tolerant. Choose models for digital circuits with peak to peak noise and ripple of less than 10% of the noise margin of the logic family. Many venders offer external filters to reduce noise to very low levels.
- Output Voltage Tolerance (Accuracy): Choose models with ±1% or better.
- Regulation: Choose models with 0.05% or better for both line and load.
- Short Circuit Protection: Choose models with output short circuit protection and current limiting.

10.2 Input Circuits

10.2.1 Overcurrent Protection

The purpose of input fusing is to provide protection of the PC board and connectors in the event of a catastrophic failure of the converter resulting in excessive current draw and overheating.

Recommendation 10.2.1-a (fast-blow type fuse):

Inputs to DC/DC converters should be fused with a fast-blow type fuse rated to carry at least the maximum continuous input current.

Observation 10.2.1-b (rated load for fusing):

Fusing at 150% of rated load is usually necessary to prevent fuse action due to normal inrush currents at the time power is applied. Fusing in excess of 200% is excessive and can result in inadequate protection to the circuitry. For reasons of safety, slow-blow fuses are not to be used. Their use could result in the device being deemed unacceptable by UL or other agencies. In any event, the I^2T rating of the fuse needs to be selected to support the inrush current of the selected DC–DC converter.

10.2.2 Transient Voltage Protection

The purpose of transient protection is to protect the DC–DC converter in the event of an overvoltage condition on the bulk power distribution line. Some converters are already provided with inherent transient protection and some are not. Consult the manufacturer’s data sheet for individual device specifications.

Recommendation 10.2.2-a (zener transient suppresser):

An avalanche zener type transient suppresser should be used across the inputs of DC–DC converters unless already built into the device. The suppresser clamps the input to a safe level in the event of a power line transient. The suppresser should be between the converter and the fuse such that a sustained overvoltage condition will open the fuse.

The voltage rating of the suppresser needs to be above the maximum rating of the bulk power supply and below the maximum input voltage of the converter as specified in the manufacturer's data.

10.2.3 Reducing Conducted Emissions and Susceptibility in Input Circuits

The system needs to be designed to avoid interfering with nearby electronics by <u>conducting</u> noise generated inside the converter back into the bulk power supply. Conducted interference will affect nearby circuitry. A decision needs to be made as to how much interference the application will be allowed to produce. Any circuit which emits noise by conduction is probably also <u>susceptible</u> to noise which arrives by conduction. Vendor's data sheets usually provide information on emissions and immunity; often plotting emissions vs. frequency (see Figure 12.2-1).

Input filters can be used to reduce the emission and susceptibility of conducted noise by a converter. Input filtering to the DC–DC converter is useful not only to provide cleaner inputs to the converter itself but, more importantly, to limit the amount of noise fed back to other boards in the system through the backplane. Many converters are internally provided with input filters to reduce reflected ripple current. If a converter cannot be obtained with sufficient input filtering, then external filter components could be added. Each manufacturer provides guidelines suitable for its products. Some manufacturers supply EMI filter Modules that can be added to reduce input noise to well below MIL Spec standards.

Recommendation 10.2.3-a (adding filter):

VME64xP boards that use DC–DC converter modules should be filtered on the input side of the converter in order to reduce conducted noise. The filter should be built into the converter or added externally.

Observation 10.2.3-b (filtering by ceramic capacitors):

Input filters can be as simple as ceramic capacitors across the inputs and/or to the input return. Refer to manufacturer's recommendations.

Observation 10.2.3-c (Balun filter to suppress common mode noise):

An input Balun filter is sometimes required at the input of DC–DC converters to suppress common mode noise generated by the converter and conducted back into the power line. The Balun filter presents a high inductance to the common mode noise but virtually none to the differential mode current.

10.3 Output Circuits

10.3.1 Overcurrent Protection

Output short circuit protection is necessary to protect the DC–DC converter and the rest of the printed circuit board from physical damage in the event of a sustained over-current condition on the output of the DC–DC converter. Some converters are already provided with inherent short circuit protection and some are not. Consult the manufacturer’s data sheet for individual device specifications. Output fusing is not recommended because it affects regulation of the converter and reduces noise margins.

Recommendation 10.3.1-a (internal current limiting and output short circuit protection):

Devices with internal current limiting and output short circuit protection should be used rather than output fusing since output fusing results in undesirable voltage drops. Converters with excess output current capacity should not be used. The converter should be sized appropriately for the load.

10.3.2 Reducing Differential and Common Mode Noise in Output Circuits

It is important to minimize both differential and common mode noise on the output of the converter in order to avoid interference to circuitry being powered by the converter. Output filtering is sometimes necessary to reduce harmonic noise coming from the DC–DC converter which can severely degrade analog and possibly digital circuit performance.

The effect of noise on digital circuits is decreased noise margins and possibly false switching. The effect on analog circuits is decreased resolution and the addition of offsets to the signals.

Analog components typically have a power supply noise rejection ratio which is inversely proportional to the frequency of the noise. An operational amplifier that has 100 dB of power supply rejection ratio at DC could degrade to 20 dB at 100 kHz (and to 0 dB at 1 MHz!). Manufacturer's recommendations need to be closely followed with respect to reducing output noise.

Differential noise (*e.g.* on the power or signal lead with respect to the return lead) can be readily filtered and controlled. However, common mode noise (noise common to the power and return leads with respect to earth ground) is more difficult to control. For example, an analog circuit could have a sensitive transducer providing input from a remote location. If the analog circuit itself is bouncing around on a common noise platform with respect to the earth ground, then precision and sensitivity could be difficult to obtain.

The amount of noise that a circuit will tolerate depends on the noise margins of the digital circuits and the required resolution of the analog circuits. Most of the common mode noise in a subrack is due to capacitive coupling in the power supplies and backplane.

Observation 10.3.2-a (applications literature):

Vendors provide applications literature that extensively discusses the control of output noise.

Observation 10.3.2-b (external filters):

Converter manufacturers frequently offer external filters for customers who require very low noise. These filters are typically better than one can design in-house.

Observation 10.3.2-c (ESR of ceramic capacitors):

Differential mode output noise filtering can often be obtained by the simple addition of an external capacitor across the output. Only high quality, low equivalent series resistance (ESR) ceramic capacitors, with low impedance at the frequency of interest, are suitable for this application. At the switching frequency of most DC–DC converters, most electrolytic and tantalum capacitors are outside of their useful range. Filter capacitors are most effective when connected as near the output pin and the common pin as practical. Different capacitor types become self-resonant at different frequencies due to lead inductance. These resonant frequencies are to be avoided when filtering DC-DC converters.

Observation 10.3.2-d (2nd order LC filter for noise filtering):

Additional differential mode output noise filtering can be obtained by the addition of a 2nd order LC filter in the output. Such a filter is more predictable than the simple capacitor discussed in Observation 10.3.2-c and will work better at high frequencies. However, the inductor needs to be able to carry full load ampere-turns without core saturation. Care needs be taken to ensure that the resonant frequency of the filter is outside of the converter's control loop bandwidth. Use the minimum inductance necessary in order to have negligible effect on the load regulation due to effective series resistance (ESR).

Observation 10.3.2-e (obtain noise attenuation by use of capacitors):

Adequate common mode noise attenuation can be often obtained by merely connecting capacitors from the output leads to the case. This requires that the case be correctly connected to the power input return and the lead length of the capacitors kept as short as possible.

Observation 10.3.2-f (use of Balun type filter):

A Balun type filter can also be used for common mode noise, and the leakage inductance of the Balun used with differential mode capacitors as a low impedance pi filter to attenuate differential mode noise. By properly phasing the inductors in the Balun, the net differential mode core flux will always be zero in the Balun but the common mode flux will be additive presenting a high impedance to common mode currents.

10.3.3 Common Reference Points (Grounding)

Proper arrangement of the supply and return leads to the loads will minimize unwanted interactions between circuits. Incorrect management of the power supply and return paths is a common problem associated with using DC–DC converters. It has little to do with grounding, but grounding is the term most often (mis)used to describe the arrangement of the return path of the output of a power supply. Grounding, properly defined, is the connection of a local reference point within a circuit to an external reference point, which can withstand large currents without significant change in potential, which is common to all subsystems within a

larger system. (Tying the power supply return of a backplane to a copper stake driven four feet into the earth is grounding; connecting an input of an op-amp to a local power return plane is not.)

Recommendation 10.3.3-a (signal return currents):

Designers need to be aware that signal return currents will, whenever possible, flow along the same path (but, of course, upon their own layer) as the signal supply current. Return current planes should fully underlie the respective supply signals to insure that return currents have a direct and simple path back to the power supply thereby minimizing noise. If the return current cannot follow the path of the supply current, a loop of increased inductance will be formed which will increase noise and decrease noise margins.

Recommendation 10.3.3-b (control of loop area):

Loop areas should be kept small and attention paid to where the currents will flow. A common error is to provide physically disparate paths for the flow of current from supply to load, and from load to supply. Noise picked up by the system from external interference, the noise floor of the circuit itself and the noise injected by the system into adjacent systems are all directly proportional to the area enclosed by the complete loop. See also Sections 11.4.3 and 12.3.4.

Recommendation 10.3.3-c (placing of loads):

Planes should be used for power distribution. They provide low inductance paths for high-speed digital signals. Heavy loads should be placed nearest the converter and lighter loads placed farther away.

Recommendation 10.3.3-d (analog and digital returns):

The supply and return planes for analog and digital circuits should be kept separated except to connect the returns together at a single point as close to the DC–DC converter common as possible. Failure to do this will result in degraded performance by allowing DC voltage levels and noise from one circuit to interact with another circuit.

Recommendation 10.3.3-e (providing analog reference):

Analog circuits should be provided with a single analog reference with all analog signals returning to the reference via separate PC board tracks. This arrangement is often called a star ground system. If individual returns are impractical due to layout density, an analog return plane should be used which is separate from the digital return plane.

Observation 10.3.3-f (reduction in coupling by series of inductance):

Further reduction in coupling between analog currents and digital currents can in some cases be achieved by placing a small series inductance between the analog return and the digital return such that digital noise sees a lower impedance to the backplane than to the adjacent analog return plane.

10.3.4 Design Considerations for Power and Return Planes

Good design practice dictates that power planes and return planes completely underlie all components which connect to that power source with no internal blockages to the flow of current that would result in internal current loops. Components in the plane(s) need to be laid out to provide unrestricted current flow to those devices that consume the greatest amount of instantaneous current. The objective is to minimize the trace resistance and inductance from the power source to the load.

Solid planes are preferable to screen planes. Return signals always follow the path of least impedance back to their source. The path of least impedance at high frequencies is the path of minimum loop area. Thus the return signal prefers to stay as close as possible to its outgoing signal.

10.3.5 Bypassing and Decoupling

Capacitors are placed across integrated circuits for both decoupling and bypassing purposes. (Many of the items here are identical to those for analog module design, Section 11.3.4.)

High speed digital circuits draw current impulses from the power supply leads when they switch. The coupling of this noise into the power supply plane has to be minimized or it will affect the operation of other circuits. Decoupling capacitors can supply the current for these impulses locally at the IC. Thus the impulse currents do not flow through the inductance of the power supply planes and do not contribute to the noise.

The noise on the power supply leads needs to be bypassed around the analog ICs to avoid degrading the operation of the circuits. Bypassing capacitors provide this function.

Recommendation 10.3.5-a (minimize noise by providing decoupling capacitors):

Designers should provide decoupling capacitors at each load (integrated circuit) to minimize noise spikes generated across the inductance of the power leads by rapidly changing currents in high-speed analog and digital circuits. Care should be taken to choose proper components for decoupling.

Observation 10.3.5-b (monolithic ceramic capacitors):

Monolithic ceramic capacitors have very low series inductance. They are ideal for high frequency decoupling. Disc ceramic capacitors, although less expensive, are sometimes quite inductive.

To ensure that an analog circuit is adequately decoupled and bypassed at both high and low frequencies, a solid aluminum electrolytic capacitor is used in parallel with a monolithic ceramic one. The combination will have high capacitance and will remain capacitive at VHF frequencies. (See also Section 11.3.4 herein.)

Recommendation 10.3.5-c (placement of decoupling capacitors):

Decoupling capacitors should be as close to the power/ground pins as practicable with absolutely minimal lead length. Even the shortest of lead length or PCB trace will provide inductance that lowers the effective frequency of the capacitor - perhaps negating the capacitance completely.

Observation 10.3.5-d (placement of bypassing capacitors):

The correct placement of bypassing capacitors across analog circuits is not always immediately apparent. The objective is to provide the shortest return path for noise currents to return to their sources. (See also Section 11.3.4 herein.)

10.4 Radiated Emissions and Susceptibility

The designer needs to suppress radiated emissions and also reduce the susceptibility to radiated emissions. Radiated emissions can be propagated as magnetic coupling, electric field coupling or electromagnetic radiation. Emissions can have differential-mode or common-mode origins. Differential-mode emissions result from current flowing around loops formed by signal and return conductors within circuits. Common-mode emissions result from voltage drops in circuits that cause some parts of the circuits to be at common-mode potentials above "ground", for example, voltage drops in the digital logic ground system.

Electro-magnetic radiation is generally not a factor. Magnetic and electric field coupling, however, require attention.

Most converters are designed with careful attention to magnetic design to minimize loop area; and utilize shielded packaging to block electric field coupling. Low cost, low power converters of less than 5 watts

frequently have plastic cases and thus need to be carefully evaluated for electric field emissions. Higher power converters are designed with metal cases both for thermal performance and shielding. Metal cases are either five sided or six sided. Five sided cases require a power return plane beneath the converter to complete the shield. All converters require connection of the shield to the input power return or as designated by the manufacturer. Manufacturer's data needs to be examined to ascertain effectiveness of their shielding.

10.4.1 Applicable Emission and Susceptibility Standards

The same organizations that provide standards for conducted emissions and susceptibility, also provide standards for radiated emissions and susceptibility (see Section 12.2.2). Each vendor provides technical specifications regarding their products. As in the case of conducted emissions, the MIL-STD provides the most comprehensive standards and test procedures; and can be used also to design interference free non-military equipment.

Considering the narrow spacing between Modules and the dense circuitry in a VMEbus subrack, the acceptable noise level needs to be specified as very low. Any interference with the operation with other Modules in the subrack is unacceptable.

10.4.2 The Effects of Radiated Noise

The effects of radiated differential and common mode noise are identical to those from conduction, *i.e.*, false triggering, decreased noise margins, decreased analog resolution. Every effort needs to be made to suppress this interference.

10.4.3 Reducing Radiated Emissions and Susceptibility

Near-field magnetic emissions and susceptibility are not easily reduced with shielding. Stray magnetic fields can be minimized by using good circuit layout and design techniques, *i.e.* minimization of loop area and inductance. Shielding is effective for minimizing the effects of noise coupled by <u>electric</u> fields.

Recommendation 10.4.3-a (placement of circuits susceptible to radiated interference):

Circuits that are susceptible to radiated interference should be placed as far away as feasible from the backplane and the board guides.

Recommendation 10.4.3-b (minimizing radiated noise):

DC–DC converters used in VMEbus boards with analog circuitry should have fully enclosing metal cases (six sided). These cases should be connected as specified by the manufacturer to minimize radiated noise.

Observation 10.4.3-c (placement of Faraday shield for further reductions in radiated noise):

Further reductions in radiated noise can be achieved by designing a Faraday shield around the entire Module or around susceptible circuitry. In the ideal case, a full Faraday cage shield can be made from the board return plane, the side panel, the front panel, plus top and bottom ventilated shields, as is described in the NIM (DOE/ER-0457T) and the VXI standards.

10.5 Thermal Considerations

Observation 10.5-a (heat build up in the converter):

Modules with DC-DC converters need to be designed to facilitate the removal of heat generated by the converters. Thermal considerations can well be the most important in utilizing DC-DC converters. The wide range of application possibilities precludes a

simplistic set of guidelines. Each situation requires thermal analysis to some degree. A converter in still air with no other conductive cooling paths will have a thermal resistance as stated by the manufacturer. In situations where this will result in exceeding the allowable base plate temperature of the converter or will cause excessive localized temperatures on the PCB, additional measures to remove heat will be required. The simplest measure is to thermally attach the converter to the PCB to provide a conductive thermal path. Next, the contribution of airflow over the converter to the thermal resistance needs to be analyzed. If the situation is still not acceptable, the final measure is to provide additional heat sinking to the converter as determined by manufacturer's recommendations. The use of heat sinks can sometimes, but not always, increase the component height of the converter to the point where the use of a double width Module is required.

Observation 10.5-b (reference of thermal characteristics):

Manufacturer's data sheets and application notes are to be carefully considered with regard to thermal characteristics.

Recommendation 10.5-c (examining efficiency curves):

DC-DC power supply efficiency curves should be carefully examined and a converter selected that is as efficient as possible at the expected operating current. The more efficient the supply the less the losses in the converter and therefore the approach required for cooling is simpler. Also, output voltage regulation may be improved and the total power available when a short circuit develops will be minimized.

10.5.1 Cooling DC to DC Converters

The most important advice here is to follow the manufacturer's recommendations.

Observation 10.5.1-a (addition of cooling):

Practical application of high density DC–DC converters with outputs exceeding about 5 watts can require the addition of a heat sink or forced air flow.

Recommendation 10.5.1-b (air flow):

Air flow past the DC–DC converter should not be restricted.

Recommendation 10.5.1-c (placement of high heat generation devices):

High heat generating devices should be placed toward the top of the Module.

Observation 10.5.1-d (derating of air flow):

In a typical application the airflow across a DC–DC converter is reduced by as much as 60% to 80% from the nominal across the Module because of the back pressure and turbulence encountered near the converter.

Recommendation 10.5.1-e (orientation of heat sinks):

If heat sinks are used, they should be oriented such that the fins are parallel to the airflow (*i.e.* vertical).

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11. Analog Module Design Considerations

11.1 Introduction to the Implementation of Analog Circuitry in VMEbus

VMEbus has not been an ideal platform for sensitive analog implementations, but is nevertheless often used in such applications. This Chapter gives a number of guidelines and recommendations that together describe a suitable VMEbus environment.

Implementing accurate, low level analog circuitry in a VMEbus environment is difficult. The original VMEbus specification, IEEE 1014, is noisy. VME64x and VME64xP significantly lessen the noise by using 5-row rather than 3-row backplane connectors and, optionally, EMI gaskets and solder-side covers between Module and Transition Module slots. These 5-row connectors add a substantial amount of digital ground pins. The primary problem is common mode noise found at higher frequencies where the common mode rejection of analog amplifiers is typically inadequate. In addition to its direct influence, high frequency noise is often rectified by active and passive components resulting in signal offsets.

When common mode noise couples into unbalanced circuits, it becomes differential noise. Common mode noise effects can be reduced by; (a) proper circuit design, (b) the use of differential amplifiers, (c) DC-DC converters, (d) filtering and (e) careful printed circuit layout. However, the circuits need to be connected to a common reference and cannot be left floating. The analog power returns are eventually connected to a common power return that is bouncing with capacitively coupled noise finding its way back to its source.

Normal VMEbus backplanes do not provide a clean earth ground. The VME64xP backplane specification provides an AGRD pin that can be used for this purpose. Additionally the VME64xP backplane and subrack provide a large number of additional grounds and clean voltages that considerably ease the problems previously encountered in analog applications.

Noise can be generated by power supplies, backplanes, and circuitry on Modules. The best solution is to reduce the noise at its source, prevent or avoid it in the first place. Use low noise power supplies that reduce capacitive coupling, wiring harnesses that minimize loop areas, and lower the inductance of power return paths. Properly designed backplanes that comply with VMEbus specifications for stub lengths and bus loading can help reduce noise. Design circuits with careful attention to edge speeds, terminations and signal return paths.

Once everything has been done to reduce noise at the source, then the analog circuitry needs to be isolated from the noise sources and/or designed to tolerate them.

11.1.1 Relation to VXIbus

The VMEbus Extensions for Instrumentation (VXIbus) specification describes extensions to the VME specification that provide the features necessary for the implementation of modular instrumentation. VXIbus includes features similar to those specified in this document: ECL and analog power, screening and large Module format.

11.1.2 Achievable Performance Levels

There are two areas of concern when defining achievable performance levels. The first is resolution and the second is throughput. Throughput can be sacrificed to increase resolution and, conversely, resolution can be sacrificed to increase throughput. The noise level in the subrack and adjacent circuitry provides the baseline around which the tradeoffs are made. A noisy environment will limit the resolution and throughput unless the circuitry can be isolated from the noise or designed to tolerate it.

In the normal situation where the noise level of the installation is unknown or beyond the Module designer's control, such as for a commercial product offering, careful design of the circuitry can still provide good

performance. Careful attention to noise tolerance and isolation typically produces digitizer Modules capable of 12 bits of resolution at 10M samples per second throughput and up to 16 bits of resolution at perhaps 50K samples per second throughput (based on offerings in the VMEbus Product Directory). Resolutions of 18 bits are possible at very low throughputs. The noise level determines how much isolation, filtering and/or integrating will be required.

As a comparison, VXIbus digitizer Modules, where the subrack and Modules are designed specifically for instrumentation, are offered with 12 bits of resolution at 20M samples per second; and with 16 bits of resolution at up to 100K samples per second.

11.2 Reducing Common Mode Noise in the Subrack

11.2.1 Digital Power Supplies and Harnesses

The primary source of noise from power supplies is due to capacitive coupling of rectifiers and switching elements to the power supply frame which is grounded. This common mode noise is conducted over the output and return lines to the backplane and Modules. From there it finds its way back to its source by several paths including capacitive coupling to circuits and hence to ground or direct connection to ground via power supply reference connections. The common mode noise currents flow through the resistances and inductances of the circuits creating voltage drops which effectively raise the entire subrack above ground reference level. When common mode noise couples into unbalanced circuits (such as single-ended circuits), it becomes differential noise that adversely affects accuracy and resolution.

The primary source of noise from harnesses is due to the simple principle of loop area. When power and return lines are not kept adjacent (i.e. twisted pair), the resulting loop area increases the inductance of the lines. Common and differential mode noise currents flowing through these inductances magnetically couple to surrounding backplanes, power conductors and Module circuitry; and create voltages which electrically couple to same. The result is to add to the noise level of the subrack above ground.

Twisting power supply wires tightly couples the magnetic fields of the supply wire and its associated return, minimizing the amount of magnetic flux which is radiated to other conductors in the system. Twisting does not significantly affect the electric field coupling from one wire set to another since the E field coupling is controlled by capacitive effects. Control of electric fields is obtained through careful placement and shielding. The general approach to noise is to tightly couple signals and their returns to reduce magnetic coupling, and to provide shielding to reduce electric field coupling.

Recommendation 11.2.1-a (power supply output filtering):

Power supplies for VMEbus subracks should have common mode filters on their outputs. Consult the manufacturer for recommendations. The idea is to shunt the common mode noise currents back to the power supply case. The filters could be as simple as capacitors from the outputs to the case.

Recommendation 11.2.1-b (power supply harness wiring):

Power supply harnesses to subracks should be twisted pair conductors. The idea is to decrease the loop area (thus inductance) between the supply and return lines.

11.2.2 Backplanes

VMEbus backplanes contribute substantially to the noise level in the subrack. The mechanism is primarily capacitive coupling of the high frequencies inherent in the fast switching, high current digital bus lines to power supply, power supply return and signal lines.

Recommendation 11.2.2-a (Backplane construction):

Backplanes should be high quality with low-impedance, non-current-carrying planes electrically connected to the subrack frame on both outside layers. The next inner layer on each side should be a low-impedance return or an AC return (voltage) plane with all required signal planes and additional voltage and return planes sandwiched in between.

11.3 Providing Low-Noise Analog Power Supplies

11.3.1 Using the ±12 V Supplies

The ±12 V supplies are generally used to power communication circuits (e.g., RS-232 ICs) and thus are likely to carry conducted noise. Furthermore, 12 V does not always provide sufficient range for analog circuits processing 10 V signals. Nevertheless, the standard VMEbus ±12 V supplies can sometimes be used effectively if the application does not need DC isolation or require high resolution and if the integrated circuit power needs can be met.

Local filtering of differential and common mode noise will usually be required due to the distance from the source, distribution over the backplane, conduction from other Modules etc. Excellent EMI suppression filters are available which provide high insertion loss (i.e. 40 dB 1 MHz to 1 GHz) and require minimal circuit board space. In addition, effective decoupling and bypassing needs to be implemented.

Recommendation 11.3.1-a (grounding):

A common mode/differential mode EMI suppression filter should be used on the ±12 V supplies in the VMEbus Module if the ±12 V is used to power analog circuitry. The single point connection between the analog and digital ground planes should be at the "power supply ground" side of the filter as opposed to the "circuit ground" side. This single point is then attached to Earth. (See also Section 10.3.3 herein.)

11.3.2 Using DC to DC Converters

If DC isolation of the analog circuits are required, or voltages other than ±12 V are required, or current demands exceed 1.5 A from each supply, or if the ±12 V supplies are too noisy; then a DC–DC converter could be used to supply power to the analog circuitry. See also Recommendation 7.2-d in VITA 23. The converter is powered by the V1 or V2 lines (nominally 48 volts, as per VME64x) or by other bused power. Powering by the 48 volts is preferred.

DC–DC converters introduce new engineering challenges, the most offensive of which are noise, heat and a need for printed circuit board space. The most valuable source of information in using DC-DC converters is the vendors of these devices. Chapter 10 herein provides guidelines for usage of DC-DC converters.

11.3.3 Analog Power and Ground Planes

Analog circuits require power and reference (ground) conductors that are separate from those of the digital circuits. The ideal construction would be to have analog reference planes on top and bottom of the board to provide shielding and low inductance signal and power returns. The analog power planes would then be sandwiched between the grounds and the analog signals sandwiched between the power planes and reference planes. VMEbus is a noisy environment for analog circuits and such measures are necessary for high-resolution/high-throughput applications. The following suggestions are offered:

Recommendation 11.3.3-a (reference planes):

The reference conductor should be a plane which entirely underlies the analog circuits including ICs, power and signal conductors. This plane should be connected to the digital reference (VMEbus GND) at a single location. This connection should be made inherently through the EMI filter, if used, or as recommended by the manufacturer if a DC–DC converter is used.

Recommendation 11.3.3-b (voltage planes):

The separate voltage conductors should be made as wide as practicable (full planes if at all feasible) to reduce their inductance; and should overlay one another with the reference plane in the middle to reduce the loop area for signals which have less than obvious return paths . Anything that increases capacitance (such as wide traces over a ground plane) will reduce inductance. Reducing the inductance of the traces will reduce the AC voltage (noise) developed by changing currents flowing in the traces; and will reduce the susceptibility of the circuits to noise coupled from other sources.

Recommendation 11.3.3-c (analog signal routing):

Each analog signal should be analyzed and its conductor routed in close proximity to its signal return path whether it is a power conductor or a reference plane. Current takes the path of least *impedance*, which is not necessarily the path of least *resistance*. For frequencies greater than 3 kHz, least impedance means smallest loop area.

11.3.4 Bypassing and Decoupling

Capacitors are placed across integrated circuits for both decoupling and bypassing purposes. High frequency capacitors can also provide a return path for driver return currents that are induced in voltage or ground planes. (Many of the items here are identical to those for DC-DC converters in Section 10.3.5.)

High-speed circuits draw current impulses from the power supply leads when they switch. The coupling of this noise into the power supply plane has to be minimized or it will affect the operation of other circuits. Decoupling capacitors supply the current for these impulses locally at the integrated circuit. Thus the impulse currents do not flow through the inductance of the power supply planes and do not contribute to the noise.

Operational amplifier circuits could have power supply rejection ratios of 100 dB at DC, but could degrade to 20 dB at 100 kHz (and to 0 dB at 1 MHz). The differential noise on the power supply leads can be reduced at the inputs of the analog ICs through the use of bypass capacitors.

Observation 11.3.4-a (bypassing):

Even so-called ‘balanced’ circuits such as differential drivers or ECL logic will create current pulses that can be properly bypassed. Differential drivers which utilize saturated logic will have faster transition times on one side than the other, resulting in a current spike which is proportional to the difference in $\delta v/\delta t$ between the outputs. Similarly, differences in trace length and capacitive loading in current-switching logic will result in differential currents between complimentary outputs.

Recommendation 11.3.4-b (power decoupling capacitors):

Decoupling capacitors should be provided at each integrated circuit to minimize noise spikes generated across the inductance of the power leads by rapidly changing currents in high-speed analog circuits. Care should be taken to choose components for decoupling that are effective at the frequencies involved. Many capacitors are ineffective or inductive at frequencies above 50 MHz.

Observation 11.3.4-c (decoupling current-switching logic):

Current-switching logic requires a different approach than voltage-switching logic. In typical applications the current-switching circuitry has a nearly constant current and injects little noise into the system. Thus, the active circuits of current-switching logic require minimal decoupling, only enough to maintain a stable power supply. However, the current in the DC termination resistance used to convert current-switching signals into voltage signals (e.g., the termination resistance used in ECL) requires decoupling at the resistor which can filter the high-frequency switching transients.

Observation 11.3.4-d (SIP resistor networks):

Single-in-line resistor networks provide a convenient physical package for termination resistors. The construction of a SIP resistor, however, provides a nearly ideal breeding ground for noise. At high frequencies, the inductive connection of each resistor to the common point, plus the varying current requirements from the sum of all the currents in all the resistors, make these devices impractical at frequencies above 50-100 MHz. For best noise performance, an individual chip termination resistor with adjacent decoupling capacitor is required. Several resistors may share the same capacitor under certain circumstances.

Recommendation 11.3.4-e (termination capacitances)

Monolithic ceramic capacitors that have very low series inductance should be used as they are ideal for high frequency decoupling. Disc ceramic capacitors, although less expensive, are sometimes quite inductive. To ensure that an analog circuit is adequately decoupled (see Observation 11.3.4-f) and bypassed at both high and low frequencies, a solid aluminum electrolytic capacitor should be used in parallel with a monolithic ceramic one. The combination will have high capacitance and will remain capacitive at VHF frequencies.

Observation 11.3.4-f (decoupling capacitors):

Decoupling capacitors need to be as close to the power/ground pins as possible with absolutely minimal lead length. Even the shortest of lead length or PCB trace will provide inductance that lowers the effective frequency of the capacitor - perhaps negating the capacitance completely. A better technique is to use planes for the voltage supply and its return, and sink the leads of the decoupling capacitor directly into the planes, as close to the IC as possible. Surface mount, multi-layer ceramic capacitors placed on the solder side of the PC board, beneath the IC, are a nearly optimal combination of small size and low inductance connection.

Observation 11.3.4-g (bypass capacitor placement):

The correct placement of bypassing capacitors across analog circuits is not always immediately apparent. The placement of these capacitors should provide the shortest return path for noise currents to return to their sources.

11.4 Isolation from Noisy Digital Circuits

Sensitive analog circuits need to be located as far as possible from sources of noise. The most offensive sources of noise are the VMEbus backplane, unshielded DC-DC converters and high-speed digital circuits.

Recommendation 11.4-a (placement of sensitive components):

Circuits susceptible to radiated emissions should be located away from any sources of noise such as DC-DC converters, digital circuits, the backplanes and the board guides. The preferred position is near the front panel, in the middle of the board.

11.4.1 Separate Digital and Analog Connectors

It is not advisable to route analog signals through the P1 or P2 connectors because of high intensity noise in that area. The preferred routing is through the front panel or, in the case of 9U Modules, through the P3 or P5/P6 connector. EMI filters are available integrated into front panel type connectors that provide excellent protection against external noise entering analog circuitry. Attention is called to the 2 mm hard metric connectors offered by multiple manufacturers that contain internal and external shielding components.

Recommendation 3.4.1-a (routing of analog signals):

Analog signals should not be routed through or in the vicinity of connectors that carry high-speed digital signals.

Recommendation 11.4.1-b (use of EMI suppression filters):

Analog signals should be routed onto VMEbus boards through connectors with integral EMI suppression filters. (Such filters can be procured from Murata Erie, Coilcraft and others.)

11.4.2 Continuous Metal Shielding

Continuous metal shielding, properly grounded, can be extremely effective against electrostatically coupled noise; and can be fairly effective against "high frequency" magnetic and electromagnetically coupled noise. The standards (VME, VME64 and VME64x) do not provide guidance for full Module shielding, nor do they provide for a clean earth ground. Although VME64x does specify an EMC front panel and subrack which could optionally be used to build an integrated system that is electromagnetically compatible, it is not intended to address the problem of shielding sensitive analog circuits. The "VXIbus" standard however, does contain detailed shielding guidance. (See also Observation 12.3.4-a.)

Continuous metal shielding as is used in VXIbus Modules is difficult in VMEbus Modules unless one is willing to occupy more than a single Module width. When used in the high density VMEbus environment, full shielding could interfere with cooling and with surface mounting of components on the solder side of PC boards. It is practical however to use reference planes as partial shields as mentioned previously, or to shield the most susceptible circuitry individually. An example is the six-sided shields on DC-DC converters that are very effective.

The shield material required depends on the type of interference being shielded against. Noise which is coupled by mutual inductance (i.e. magnetic and/or RFI) requires magnetic materials such as silicon steel to absorb the magnetic fields. Noise that is coupled via electric fields requires high-conductivity materials such as copper to avoid voltage drops and prevent continuation of the field within the shield. Copper is relatively effective against electric field noise at the high frequencies present in VMEbus subracks; but not against low frequency magnetic fields. These low frequency noise sources could be addressed by good circuit design (minimizing loop area, and the use of balanced circuits and differential analog devices).

Recommendation 11.4.2-a (Grounding of shields):

Shielded components should be used where practical; for example, DC-DC converters which have six-sided metal shield cases. If shields are used, or shielded components are used, the shields should be connected to a reference. An unconnected shield merely couples noise into circuits through mutual parasitic capacitances. Follow the manufacturer's recommendations as to "grounding" these shields.

Observation 11.4.2-b (EMC subracks):

The EMC front panels and subracks of the VME64x specification are effective in reducing EMI and RFI being radiated into a room and to some extent, against

susceptibility to noise already present in the room (such as from power lines, fluorescent lights etc.).

11.4.3 Minimizing Loop Area

Stripline layout techniques are one of the most powerful tools available to the printed circuit designer. They provide the dual benefit of carefully controlled impedance and increased noise immunity. Most circuit boards are designed with the power and return planes on adjacent inner layers of the board as in Figure 11.4.3-1 to maximize the distributed capacitance between the two plane layers. Although a laudable practice, this places the signal traces on the outer layers of the board where they are susceptible to externally induced noise. The electric field of the outer layer conductors is also non-uniform as the relative permittivity of the printed circuit board is different from that of air. The permittivity difference, plus the geometric effects of 'wire over plane' construction, lead to increased trace-to-trace coupling of signals. In boards with more than four layers, the outer signal layers also have a different characteristic impedance than the inner circuit layers, resulting in impedance discontinuities where the signals change from an inner layer to an outer layer (or visa versa).

A better technique is to use stripline layout where the signal-carrying layer is sandwiched between the power and return planes as in Figure 11.4.3-2. In this geometry the field lines are much more uniform and trace-to-trace coupling is greatly reduced. Since the traces are well covered by planes that present a low impedance to external interference, electro-statically coupled noise is also reduced.

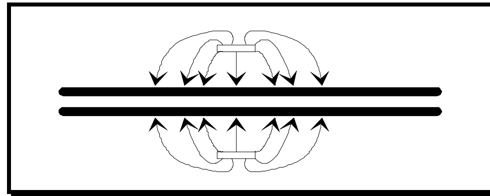

Figure 11.4.3-1
Example of field lines in standard microstrip construction

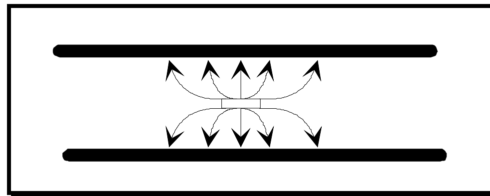

Figure 11.4.3-2
Example of field lines in stripline construction

Recommendation 11.4.3-a (use of stripline techniques):

Stripline printed circuit board techniques, where the conducting trace is on an inner layer between two planes as in Figure 11.4.3-2, should be used to control trace impedance and reduce noise emissions.

11.4.4 Differential and Isolation Amplifiers

When common mode noise couples into unbalanced circuits, it becomes differential noise. Differential amplifiers and balanced circuits are effective against the low frequency common mode noise (up to about 100 kHz). However, the common mode noise rejection of typical analog devices is insufficient to provide

rejection of the high frequencies (tens of MHz) present in VMEbus systems. Common mode noise entering a VMEbus subrack from an external signal source can be reduced with the use of filtered connectors as discussed elsewhere in this document.

Recommendation 11.4.4-a (external connection of analog signals):

Analog input signals should, whenever practical, be differential, and routed through balanced circuits to differential analog devices.

Recommendation 11.4.4-b (filtering of analog signals):

Analog signals should be filtered and buffered upon input to the board both to reduce external noise entering the VMEbus subrack, and to reduce noise feedback from the subrack to the signal source.

11.4.5 Shielded Twisted Pair Cable

If properly used, shielded twisted pair cable provides an excellent defense against magnetic and electric field noise coupling into sensitive circuits. The twisted pairs provide minimized loop area (reduced inductance) and balanced lines. Each pair needs to contain the signal and return from a single source even if the returns are all connected together at one end. The return current for the signal will follow the minimum inductance path back to its source - which is the same pair as its signal. Sharing return wires between two or more signals completely negates the twisted pair. If this is necessary, use the shielded flat cable described next.

Shielding on the cable provides defense against electric field coupling. The shield needs to be connected to reference on one end only. The proper end to connect is whichever end the signals are referenced (typically the driver end). Then, the shield and returns will be at nearly the same potential that reduces capacitive coupling of noise from distant sources. Connecting the shield at both ends of the cable will likely result in decreased noise immunity due to differential ground currents coupling into the signals.

Recommendation 11.4.5-a (use of shielded twisted pair cable):

If shielded twisted pair cable is used, each pair should contain the signal and return for a single source. The return should not be shared with another signal. The shield should be connected to a reference at the same end that the signals are referenced (typically the driver end).

11.4.6 Shielded Flat Ribbon Cable

Shielded flat ribbon cable is not as effective as shielded twisted pair. However, in single ended applications the balanced line benefit is lost when conductor assignments are at a premium and there are not enough returns for each signal. Flat cable can be used to share signal returns and still remain somewhat effective against noise. Each return will try to follow its signal back to the source. By arranging the returns as shown in Figure 11.4.6-1, each signal has an adjacent ground. Signal density is increased while maintaining minimal loop area and benefiting from microstrip effects. If even fewer conductors can be delegated as returns, they should be distributed so as to minimize loop area for each signal/return pair.

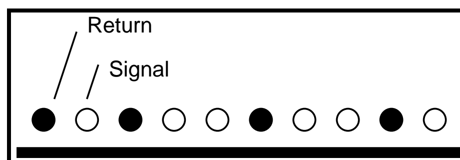

Figure 11.4.6-1
End view of ribbon cable with integral shield used for differential transmission

Recommendation 11.4.6-a (shielded flat ribbon cable):

Shielded flat ribbon cable should be used only as a last resort to increase signal density in single ended systems. The signals and returns should be arranged such as to minimize loop area. The cable shield should be connected to a reference at one end only, the end where the signals are referenced.

11.5 Mixed Analog and Digital Systems

The configuration of analog and digital ground is often a problem for the board designer. This dilemma typically occurs when implementing Analog to Digital Converters (ADC's). The problem is how to minimize the noise that is generated by the digital circuitry from finding its way into the analog section. An excellent article by Analog Devices addresses these issues.

The following is from Analog Dialog 26-2 (1992). This is a publication of Analog Devices Corporation.

"Inside an IC that has both analog and digital circuits, such as an ADC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 11.5-1 shows a simple model of an ADC. There is little the IC designer can do about the wire bond inductance and resistance associated with the pads to the package pins. The rapidly changing digital currents produce a voltage at point β that will

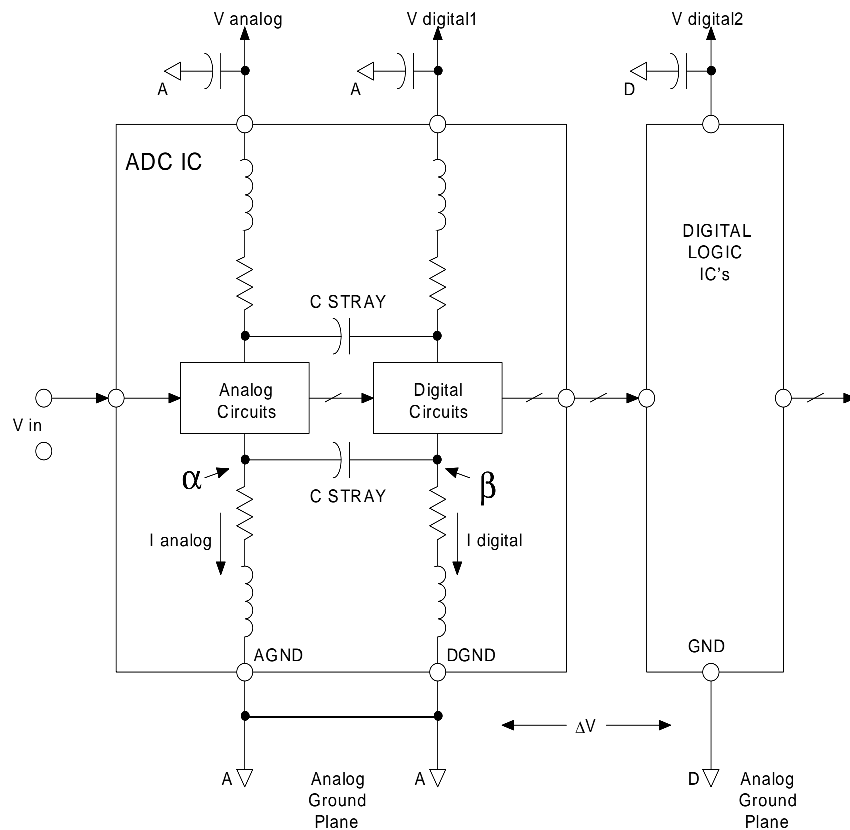

Figure 11.5-1
Typical ADC IC and Associated Circuitry

inevitably couple into point α of the analog circuits through the stray capacitance. It's the IC designers job to make the chip work in spite of this. However, you can see that in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the same low impedance ground plane with

minimal lead lengths. Any extra external impedance in the DGND connection will cause more digital noise into the analog circuit through the stray capacitance. Through an extremely simple model, this serves to illustrate the point.

By connecting the analog and digital grounds together one will incur some reduction in digital noise margin, but it is usually acceptable with TTL or CMOS logic if it's less than a few hundred millivolts or so. If the ADC has single-ended ECL outputs, a push-pull gate on each digital output, *i.e.*, one with both true and complementary outputs can help. Tie the grounds of this gate package to the analog ground plane and connect the logic signals differentially across the interface. Use a differential line receiver at the other end that is grounded to the digital ground plane. The noise between the analog and digital ground planes is now common-mode-most of it will be rejected at the output of the differential line receiver. The same technique can be used with TTL or CMOS, but there is usually enough noise margin not to require differential transmission techniques.

In general, it is unwise to connect the ADC outputs directly to a noisy data bus. The bus noise may couple back into the ADC analog input through the stray internal capacitance-which may range from 0.1 to 0.5 pF. It is much better to connect the ADC outputs directly to an intermediate buffer latch located close to the ADC. The buffer latch is grounded to the digital ground plane, so its output logic levels are now compatible with those of the rest of your system.

The same grounding philosophy applies to DAC's. The DAC's AGND and DGND pins should be tied together and connected to the analog ground plane. If the DAC has no input latches, the registers driving the DAC should be referenced and grounded to the analog ground plane to prevent digital noise from coupling into the analog output.

Mixed signal chips also have same grounding philosophy. One should never think of a complex mixed-signal chip, such as an analog DSP, as being only a digital chip. The same guidelines should be applied. Even though the effective sampling rate of the 16 bit sigma-delta ADC and DAC is only 8 ksps, the converter may operate at an oversampling frequency of 1 MHz. Such a device can require an external 13 MHz clock from which an internal 52 MHz processor clock is generated by a phase-locked loop. High speed design techniques for analog and digital circuitry will have to be applied for these devices."

The designer is encouraged to look at the rest of this article.

11.6 References

See Section 2.4.10 for references on analog design.

12 EMC/ESD Considerations

12.1 General Observations

In some applications there is a need to restrict the amount of Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) being radiated from a subrack without the aid of a special cover. The Electromagnetic Compatible (EMC) subracks described in IEEE 1101.10, when used in conjunction with VMEbus Modules and their front panels (Plug-in Units) described in IEEE 1101.10, are intended to provide this capability. In addition, the discharge of static electricity is addressed with ESD hardware.

Observation 12.1-a (electrostatic discharge):

Electrostatic discharge (ESD) provision requirements are specified in IEEE 1101.10 and IEEE 1101.11.

Recommendation 12.1-b (electromagnetic compatibility):

When specifying EMC compatible subracks and Modules, it is recommended that they be in accordance with IEEE 1101.10 for the front Module area and IEEE 1101.11 for the rear Transition Module area.

Observation 12.1-c (CE and FCC compliance):

Modules in compliance with EEC EMC directives EN50082-1 (1992) and EN50081-1 (1992) and so certified are marked “CE”. Modules may also be in compliance with the FCC requirements.

12.2 Emission Standards and Limits

There are several standards that can be consulted for emission standards information. The Federal Communications Commission (FCC) in the United States and Verband Deutscher Elektrotechniker (VDE) in Europe set standards for commercial products. The applicable regulations are Title 47 CFR Part 15 Subpart J; and VDE 0871A, 0871B and 0875N. The strictest radiation standards are specified in U. S. Department of Defense MIL-STD-461B. That standard establishes limits for conducted and radiated emissions well below any of the commercial standards referred to above. Many manufacturers provide converters that comply with MIL-STD-461B. This standard is usable as a guideline for designing interference-free equipment. The standard includes guidelines for making measurements (MIL-STD-462).

The VXIbus specification also provides simplified limits and test guidelines for conducted emissions and susceptibility applicable to instrumentation buses and VMEbus form factors. Thus it can serve as a guide.

Other regulatory agencies standards include the Canadian Standards Association (CSA), the British Standards Institution (BSI), the British Approvals Board for Telecommunications (BABT), the International Special Committee on Radio Interference (CISPR), or the International Electrotechnical Commission (IEC).

Figure 12.2-1 shows noise level standards issued by the FCC and VDE. The CE03 curve, which is the MIL-STD-461B conducted emissions, power and interconnecting leads, 15 kHz to 50 MHz limit, is not directly comparable to the FCC and VDE curves since the test procedures are quite different; but is included here for general information purposes.

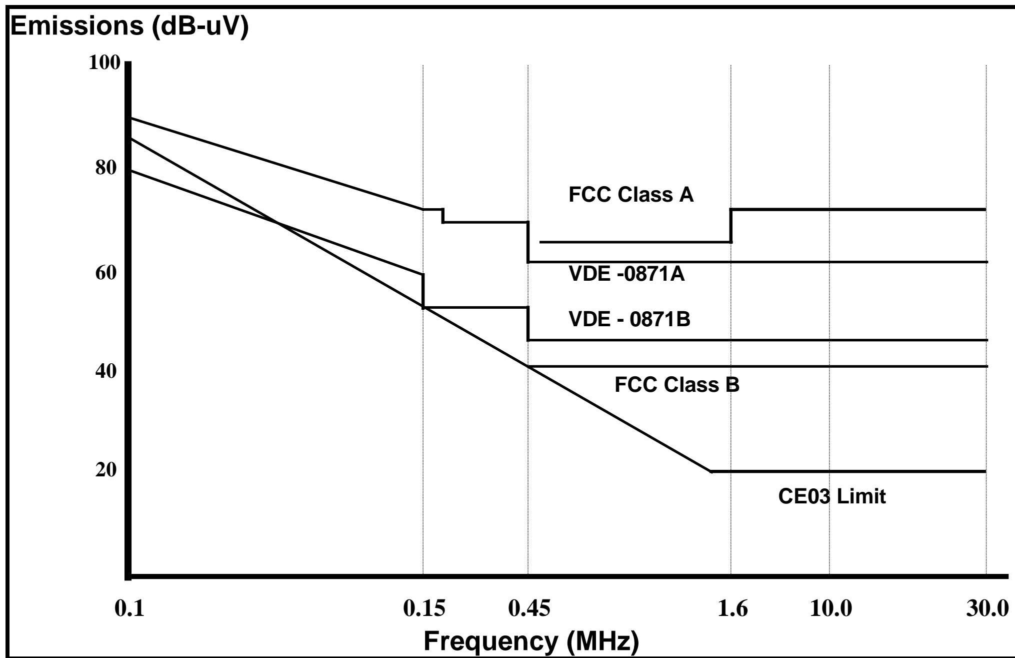

Figure 12.2-1
FCC, VDE and CE03 Emission Limits

12.3 Sources and Control of EMI

12.3.1 Minimizing Radiated Noise

Whenever current is flowing in a system, energy is radiated. To minimize this radiated energy the design needs to ensure that the path that the return current takes is as physically close to the path that the source current takes as possible. The purpose of this practice is to minimize the total volume and area enclosed by the path and its return. In board design this is usually accomplished by the use of voltage and return planes. An alternate technique is to make identically shaped and parallel traces in the planes of the board. The same minimization of the enclosed volume is a consideration that needs to be given to cables that carry single-ended signals between Modules in a system. Differential signals in cables inherently minimize the volume, hence, minimize the net radiated energy of the pair. This is discussed additionally in Sections 12.3.4, 11.4.3 and Recommendation 10.3.3-b.

12.3.2 Subrack design for EM Compliance

All active circuitry, including power and power return planes constitute a radiator that needs to be enclosed in a shield that is connected to ground for effective control of EMC. Wires which extend outside the shield, such as power supply feeders, need to be twisted with their return (not ground) to minimize radiation.

Common practice is to reference one output lug (e.g. the negative output if the supply is used for +5 V logic) of a floating power supply to the Earth Ground, although this is not required. If an output of a supply is referenced to Earth Ground, the system designer needs to ensure that this connection is made at one and only one point to avoid ground loops. An equivalent practice is to connect the subrack shield, the cable shield and the power supply box shield in series, and then run one and only one wire from the set to earth ground.

One or more sides of the EMC shield can be made up of VMEbus Modules and or Transition Modules with EMC front panels which, when properly inserted in the subrack, constitute effectively one solid conducting

sheet. In some critical cases the entire subrack could be contained inside a conducting box. If Transition Modules are not present then the backplane could be constructed so as to act as the shield in the rear.

Figure 12.3.2-1 shows the basic elements of a subrack with power supply, backplane and Modules. Earth Ground is the lowest impedance point in a system. Earth Ground is typically defined by using a conducting rod driven into the soil to a depth sufficient to maintain sub-milliohm resistance at all times.

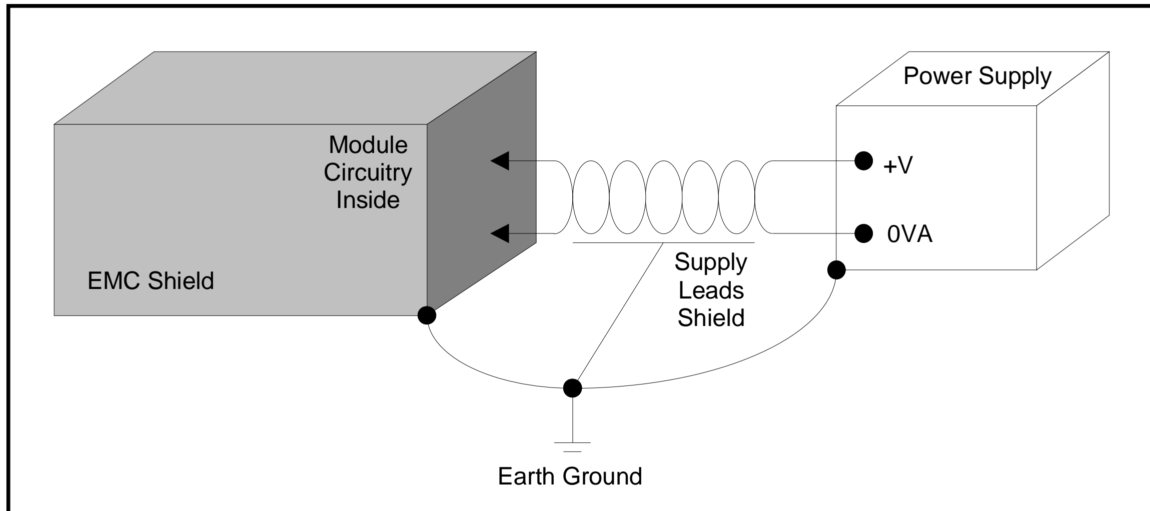

Figure 12.3.2-1
Subrack and Power Supply Connections

The following items are a guide for properly connecting a subrack and power supply to minimize the radiated energy from a system:

- EMC shield completely surrounds all circuitry, including backplane.
- EMC shield connected to Earth, NOT to GND.
- Module and Transition Module Front Panels connected to Earth, NOT to GND.
- Shield enclosure surrounding power supply connected to Earth, NOT 0VA point.
- PC Board "ground plane" connected to Voltage Return, NOT Earth. (The term "ground plane" is a misnomer.)
- Wires connecting power supply to backplane need to be twisted together to minimize loop area. For maximum compliance the twisted pair could be encased in a shield which is connected to Earth, NOT return, via a separate grounding wire so that all connections to Earth are made at one and only one point.
- All active circuitry, including power and power return planes, are considered a radiator which needs to be enclosed in a shield that is connected to ground for effective control of EMC. Wires which extend outside the shield, such as power supply feeders, need to be twisted with their return (not ground) to minimize radiation.
- Common practice is to reference the 0VA point of the power supply to the Earth, although this is not required. If the 0VA point is referenced to Earth, the system designer needs to ensure that this connection is made at one and only one point to avoid ground loops.
- The three shields are not be electrically connected when each has its own separate grounding wire, otherwise a ground loop is formed. An equivalent practice is to connect the subrack shield, the cable shield, and the power supply box shield in series; then run one and only one wire from the set to Earth.

12.3.3 Cable Connections and Grounding

The correct technique for interconnecting two Modules is to use cabling which minimizes the total loop area of the cable to reduce emissions, with balanced currents in the wire pairs. For better control of noise, the balanced pair needs to be enclosed in a shield that is connected to Earth, but not to either Module's return plane. The Earth Ground connections can be made by connecting the cable shield to the front panel of either Module, but not both, so loops are not created.

Figure 12.2.3-1 shows current flow for differential or single ended connections that have a matched return over twisted pair cables. Figure 12.2.3-2 shows a similar arrangement but with an overall cable shield and two possible shield connection points. When the shield is connected, it is connected at one end, not both. This latter method of connection will eliminate currents flowing in the shield because of ground potential shifts between equipment.

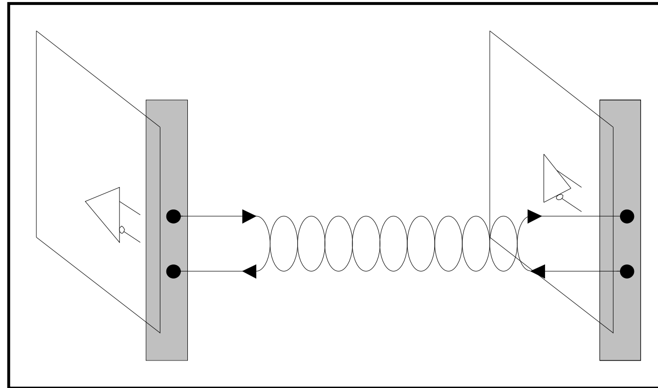

Figure 12.3.3-1
Typical current flow for differential or single-ended with matched return over twisted pair

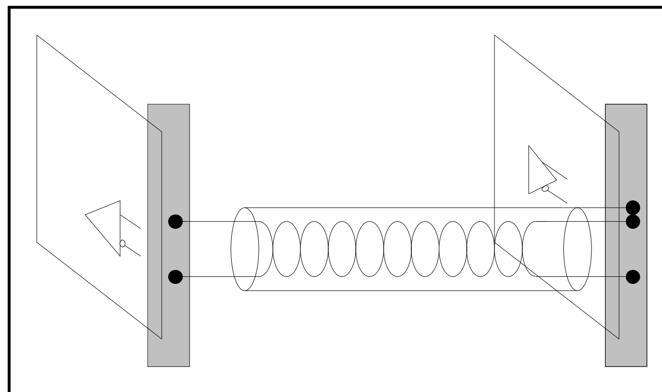

Figure 12.3.3-2
Similar to Fig. 12.3.3-1 except shield the cable has a shield.

12.3.4 Module Design to Minimize Radiated Noise

Everywhere current is flowing in a Module, the Module designer has to ensure that the path the current takes is as close as practical to the path taken by the return current. This will minimize the total volume and area enclosed by the path and its return. In board design this is usually accomplished by the use of voltage and return planes as shown in Figure 12.3.4-1. An alternative technique is to make identically shaped and parallel traces in two planes of the board. See also Section 11.4.3 and Recommendation 10.3.3-b)

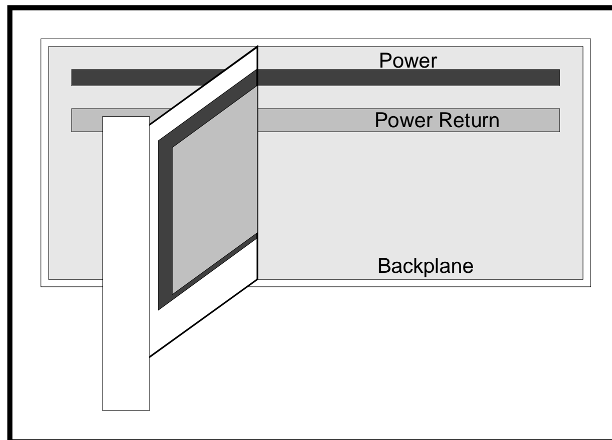

Figure 12.3.4-1
Example of correct layout Minimal loop area using power planes on Module

Figure 12.3.4-2 shows an incorrect method of laying out the Module printed circuit board. This layout results in a large loop area enclosed by the source and return currents and consequently radiating energy.

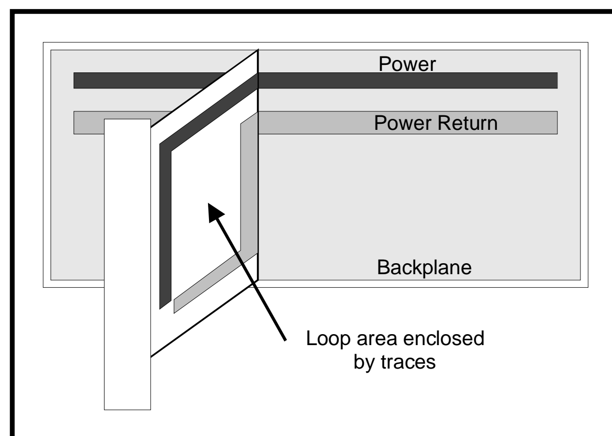

Figure 12.3.4-2
Example of incorrect layout showing loop area created within Module by power traces

Observation 12.3.4-a (shielding for low noise):

Modules for low noise applications, such as for high-resolution analog circuits, will require shielding, the degree of which will depend on the particular circuitry, its environment, and the degree of noise immunity required. Such shielding could include side panels, top and rear covers (though it is important that they not prevent adequate flow of cooling air), and suitable front and rear panels. The use of a double width Module will, in some cases, permit the installation of superior shielding panels. Shielding for low noise is discussed further in Chapter 11 herein dealing with continuous metal shielding for Modules for low-level analog applications.

12.4 ESD

Observation 12.4-a (grounding for static discharge):

VIPA circuit boards and subracks have provision for discharge of static electricity (ESD) from the boards prior to contact with the backplane as in IEEE 1101.10 and IEEE 1101.11. In VITA 23 see Rule 6.2-k regarding ESD clips on subrack card guides and Rule 4.2-s regarding ESD strips on Modules and Transition Modules.

Observation 12.4-b (ESD implementation):

ESD is implemented as follows:

- VIPA Module and Transition Module circuit boards use one or two ESD strips in one or both of the following locations: bottom edge or top edge on the component side of the board. The ESD strip(s) on the board break contact with the subrack ESD contact spring prior to the connector engagement. Position and size of the ESD strip(s) is specified in IEEE 1101.10 and IEEE 1101.11.
- The Module and Transition Module circuit board's ESD strips are in contact with the subrack ESD contact spring during most of the board's insertion into the subrack but are not connected from the subrack ESD contact spring when the board is fully inserted into the backplane. This feature reduces ground loop problems.
- Two one-megohm resistors in series are connected between each ESD strip implemented and the board's ground plane for the dissipation of any electrical charge build up.

Observation 12.4-c (discharging front panel):

Any electrical charge build-up on the front panel will be discharged into the system subrack through the ESD contacts between the front panel and the subrack.

Observation 12.4-d (alignment pin):

The alignment pin specified in IEEE 1101.10 connects the front panel to the frame of the subrack. The subrack frame is typically connected to Earth, not directly to the board's common.

Observation 12.4-e (signal return path):

Since the front panel is not directly connected to the board common, the designer cannot rely on the panel for the return currents in the shield of coax and other similar connections.

12.5 References

See Section 2.4.3 for references on Grounding and Shielding and related topics.

13 Useful Documents

13.1 Other Useful References

The following are either standards or standards "in the making". Some may be useful to system implementers since in many cases commercial equipment is available which conforms to these documents. The following list gives a short description of each document. For more details one should contact the appropriate issuing body.

13.1.1 VITA Standards

ANSI/VITA 3: BLLI

ANSI/VITA 3-1995, Board Level Live Insertion for VMEbus (recommended practices document)

ANSI/VITA 4: IP Modules

ANSI/VITA 4–1995 is a mezzanine module specification that defines a versatile module known as an "IP module". The IP module provides a convenient method of implementing a wide range of I/O, control, interface, slave processor, analog and digital functions

ANSI/VITA 4.1: IP I/O Mapping to VME64x

ANSI/VITA 4.1-1996.defines the mapping of the 50 user defined I/O pins from the IP I/O connectors to VME64x board's rear I/O connectors

VITA 5: RACEway Interlink

ANSI/VITA 5-1994 is a standard for a parallel-bused cross-bar switched interconnect on the P2 connector of the VMEbus. Slot-to-slot connectivity is implemented on active overlay boards in a Clos topology. Built around the characteristics of the i860, it delivers bandwidth from 160 MB/s to over a GB/s.

ANSI/VITA 6: SCSA

ANSI/VITA 6-1994 (Signal Computing System Architecture) and is an application-specific P2 proposal for voice processing and status. A minimum of 2000 voice channels can be carried and switched with this system.

ANSI/VITA 6.1: Extensions to SCSA

.ANSI/VITA 6-1994.defines the J2/P2 pinout and operating modes of additional SCbus controls - provides several nested levels of capacity with increasing redundancy features, each oriented towards specific segments of the computer telephony market.

VITA 7: QuickRing RT, Draft 0.9.2, 21 May 1995

QuickRing is proposed as a front panel interconnect or, with VME64 Extensions, as a P2 option. QuickRing defines a 16 line TDM data transfer sub-bus for exchange of real time telephonic voice, fax, data, and video streams. A second sub-bus is a serial, peer-to-peer communication link for interprocess control described in this white paper, with scaling from 200 MB/s to over a GB/s. National Semiconductor began sampling the controllers in September, 1993. Currently available devices operate at 50 Mhz.

ANSI/VITA 10: SKYchannel Packet Bus on P2

ANSI/VITA 10-1995 is a high performance 320 MB/s, 64 bit packet switched architecture being proposed as a P2 subsystem bus. It is implemented using active backplane boards, crossbars, and a serial link.

VITA 11: Autobahn

Autobahn proposes multiple serial differential connections (eight or more) running at 200 MB/s. each. This architecture can be implemented with crossbar connections or multidimensional connections that are envisioned for varying topologies and fault tolerance. Single-chip ECL spanceivers are being developed jointly by PEP Modular Computers and Motorola. In its initial implementation existing VMEbus protocols would be used to set up Autobahn data transfers that could take place concurrently with VMEbus activities. Current Autobahn chips have demonstrated data rates of 50 and 100 MB/s.

ANSI/VITA 12: M-Module Mezzanine

ANSI/VITA 12-1996.mezzanine module specification - allows the use of specialized modules to meet specific application requirements.

ANSI/VITA 13: VMEbus Pin Assignment for ISO/IEC 14575, IEEE 1355-1995 (H.I.C.)

ANSI/VITA 13-1995, Heterogeneous InterConnect (HIC) is being developed as a standard within the IEEE as P1355. HIC is a packet-switching technique implemented with point-to-point serial connections. HIC is defined as a low cost, low latency, scaleable, serial interconnect for parallel system construction. Proposed by INMOS in Europe (Transputer manufacturer), this technique also envisions using an active backplane. The purpose of the standardization effort within the VSO is to define a P2 pinout appropriate for the HIC protocol as defined by P1355.

VITA 16: Multi-Vendor Integration Protocols for the VMEbus, Draft 0.2, 28 August 1995

Multi Vendor Interface Protocol is a telephony standard. Natural Microsystems, Primary Rate, and Ariel have agreed to support the standardization of MVIP on the VMEbus in the VSO. MVIP is a currently existing industry specification (MVIP-90) which is being put into proper format for eventual submission to ANSI.

ANSI/VITA 17: FPDP

ANSI/VITA 17-1997 Front Panel Data Port (FPDP) is a 32-bit parallel synchronous data path that is bused across the front panels of VMEbus Modules using an 80-conductor ribbon cable. This de facto standard is now supported by analog input, analog output, digital signal processor, and interface products from at least six companies, including Ariel, CSPI, Interactive Circuits & Systems, Ixthos, Mercury Computer Systems and SKY Computer.

FPDP provides a point to point bus on which a single Master is permitted; therefore the bus is not subject to contention. However, multi-drop configurations are allowed so that multiple Modules may transmit or receive data from the bus. Systems using FPDP to carry more than 1000 channels of data can easily be constructed. Since the bus carries no address information, the maximum possible bandwidth is available for data transmission, which makes it ideal for use in data acquisition and processing systems. In addition, a signal is available to indicate the start of each data frame, which is essential for processing multi-channel data. The bus implements a handshake between the Master and the receiving Module(s) to implement flow-control; this allows for data buffers in the receiver(s) to be emptied or switched. The bus has been tested to its full rated bandwidth of 160 MB/s. This bandwidth exceeds that of the current VMEbus and VSBbus by a considerable margin, and allows data traffic to be off loaded from these buses.

In addition, data acquisition systems may have multiple FPDP paths, thus greatly increasing the aggregate bandwidth available. For example, one FPDP path might connect a number of data acquisition Modules to a DSP Module. Another FPDP path might connect other data acquisition Modules to a digital tape recorder interface, while a third FPDP path connects a DSP Module to some analog output Modules. The FPDP interface is simple, and may be designed into new products with only a few standard

integrated circuits. The software to control FPDP is simple. No special drivers or protocol stacks are required.

VITA 19: Summary and Introduction to the BusNet Standard

VITA 19-1997.overview of the current BusNet specifications and their draft or approval status -BusNet specifications consist of several independent documents - this document is informational only - it is not and never will be an approved document

ANSI/VITA 19.1: BusNet Media Access Control (MAC)

ANSI/VITA 19.1-1997.describes the lowest layer of the BusNet protocol - equivalent to the IEEE 802.2 Media Access Control layer which is the IEEE's lower subdivision of layer two of the ISO/OSI standard network model

ANSI/VITA 19.2: BusNet Link Layer Control (LLC)

ANSI/VITA 19.2-1997.describes the layer directly above the BusNet MAC layer - this layer is equivalent to the IEEE 802.2 Logical Link Control layer which is the IEEE's upper subdivision of layer two of the ISO/OSI standard network model

VITA 20: Conduction Cooled PCI Mezzanine Card (CCPMC)

VITA 20-199x.defines the mechanical and thermal interface for a conduction cooled PCI mezzanine card

VITA 22: ATM Cells Bus (ACB) on VME

VITA 22-199x.defines a low-cost structure for building ATM access systems using the Bus User Port device - ACB is being proposed as an optional inclusion for the VME backplane, included on the P0/J0 connector

ANSI/VITA 25: VISION

ANSI/VITA 25-1997,.VISION (Versatile I/O Software Interface for Open-bus Networks) is a software specification which standardizes the low-level aspects of bus I/O

ANSI/VITA 26: Myrinet-on-VME Protocol

ANSI/VITA 26-1998.defines the building block components of a Myrinet network

VITA 29: PC*MIP

VITA 30: 2mm Equipment Practice for Eurocard

VITA 30 is a good reference for placing Hard Metric connectors on Euroboards. All dimensions needed by the board mechanical designer are in this document.

VITA 31: NGIO on P0

VITA 31 addresses high speed serial connections on the P0 connector. This standard is being coordinated with cPCI and their use of P4 (physically the same connector).

VITA 32: Processor PMC (PPMC) Standard For Processor PCI Mezzanine Cards

VITA 32.incorporates a set of extensions to the IEEE P1386.1 standard which will bring the compliance of the PCI interface to the latest revision 2.1, and will allow the creation of a new class of PMC cards: Processor- or system controller-based PMC cards

13.1.2 Other Standards and Documents

(IEEE) P1596.3:

IEEE Proposed Standard for Low-Voltage Differential Signals for Scalable Coherent Interface, Draft 1.05, 28 February 1995.

VXI0:

VXIbus - VME Extensions for Instrumentation (VXIbus Consortium Inc.)

ISO/IEC 11458:

VICbus - VME Inter-Crate Bus Specification

IEC 516-1975:

A Modular Instrumentation System for Data Handling: CAMAC System

ANSI/IEEE Std. 583-1982:

Modular Instrumentation and Digital Instrumentation Interface System (CAMAC)

IEC 935 (1996-07):

Modular High-Speed Data Acquisition System - FASTBUS

IEEE Std 960-1993: (recognized as American National Standard - ANSI):

IEEE Standard FASTBUS Modular High-Speed Data Acquisition and Control System

U.S. Dept. of Energy DOE/ER-0457T (May 1990):

Standard NIM Instrumentation System

VMEbus Products Directory:

Available from VITA as are all other ANSI/VITA standards listed above.

14 I/O Connections - Physical

14.1 Introduction

Two different interconnection methods for digital signals are commonly used in physics instrumentation modules: NIM (Nuclear Instrument Module) - a current switching standard) and ECL (Emitter Coupled Logic). These signal standards are used in the vast majority of front panel control and status signals of NIM, CAMAC and FASTBUS Modules in physics laboratories and other facilities. In newer high-speed designs which do not have –5.2 V power, the use of the Low Voltage Differential Specification (LVDS) is becoming popular. VMEbus Modules that use the LVDS signals are not necessarily backward compatible with older equipment. Differential ECL or LVDS are the preferred methods for electrical digital signal interconnect. They require less physical front panel space than NIM signals and have greater common mode rejection. These interconnection methods as well as those for TTL (Transistor-Transistor Logic), RS-485 and other standards and techniques under development are discussed in this Chapter.

Signals are described in terms of levels and transitions. A signal line is always assumed to be in one of two levels, or in transition between these levels. Confusion can arise due to the various uses associated with different logic families. Within this document the conventions in Table 14.1-1 are observed.

Table 14.1-1
Definitions of standard signal levels

Signal Type	Meaning of the term Logic 1	Meaning of the term Logic 0	Use of the Asterisk *
ECL	A voltage more positive than -0.9 V with respect to GND	A voltage more negative than -1.7 V with respect to GND	A signal whose active level is ~ -1.7 V
NIM	A current of 16 mA ± 2 mA that develops a nominal voltage of -0.8 V across a 50 Ω resistor from the signal to GND	A current of 0 mA ± 1 mA that develops a nominal voltage of zero V across a 50 Ω resistor from the signal to GND	A signal whose active level ~ 0 V
TTL	A voltage more positive than +2.0 V with respect to GND at the receiver or +2.4 V min. at the driver	A voltage less than +0.8 V with respect to GND at the receiver or +0.4 V max. at the driver	A signal whose active level is ~ 0 V
LVDS	A voltage more positive than +1.4 V with respect to GND	A voltage more negative than +1.0 V with respect to GND	A signal whose active level is ~ +1.0 V
PECL	A voltage more positive than -0.9 V with respect to +5 V	A voltage more negative than -1.7 V with respect to +5 V	A signal whose active level is ~ +3.3 V

When discussing differential signals, the terms HIGH and LOW, and the asterisk, refer to the '+' side of the differential pair (the side that has the same polarity as the single-ended equivalent at the driver).

Recommendation 14.1-a (preferred signals):

Whenever possible, differential ECL or LVDS should be used. For single-ended signals NIM is an acceptable alternative.

Observation 14.1-b (ECL and LVDS common mode):

ECL and LVDS drivers and receivers have a limited common mode input voltage range and are not necessarily suitable for environments where the common mode voltage could exceed one volt. Common mode voltages of more than one volt can result in the improper operation of the receiver and/or driver. Voltages exceeding the common mode range by three or more volts could damage these devices.

Observation 14.1-c (PECL):

PECL (Positive voltage referenced ECL, typically +5 V) is not recommended for use on connectors since shorting the signal to ground will potentially result in the destruction of the driver. Good design practice mandates the use of external signals that are tolerant of grounding. The use of PECL inside the Module can be considered where circuit speed and single power rails dictate this solution.

Observation 14.1-d (LVDS incompatibility):

The use of LVDS will be incompatible with older equipment using differential ECL.

14.2 Differential Signals on Multipin Connectors

14.2.1 Cables for Differential Signals

Recommendation 14.2.1-a (impedance of multi-pair cabling):

Interconnections should be made with single or multiple pair cable of nominal 100 Ω impedance when driven differentially, unless specifically marked otherwise.

14.2.2 Connectors for Differential Signals

The following recommendations are for certain popular types of connectors common in research equipment. Other types are possible and are not precluded though not listed below. As new types become popular they will be added to this section.

Recommendation 14.2.2-a (IDC (insulation displacement connectors)):

Connectors for differential signals should be of the IDC (Insulation Displacement Connector) type or equivalent with a 2.54 mm x 2.54 mm (0.100 in x 0.100 in) grid.

Recommendation 14.2.2-b (IDC usage):

It is recommended that when IDC connectors are used the pin connector or header assembly be on the Module and the socket connector or receptacle assembly) be on the cable. The Module connector assembly should have square pins with a cross-section of 0.635 mm x 0.635 mm (0.025 in x 0.025 in) and length of 6.20 ± 0.50 mm (0.244 ± 0.020 in). For single twisted pair interconnections the cable connector assembly should have a thickness of not more than 2.54 mm (0.100 in).

Observation 14.2.2-c (Module connector assembly):

The term "Module connector assembly" as used herein refers also to connector assemblies mounted on circuit and auxiliary boards.

Observation 14.2.2-d (multi-pin, multi-socket, multi-contact):

The terms "multipin" and "multi-socket" refer to connectors that have two or more pins or sockets, respectively. The term "multi-contact" is a general term referring to either multipin or multi-socket connectors.

Recommendation 14.2.2-e (connector assembly keying):

The cable connector assembly should preferably be keyed as in MIL-C-83503 (1984) General Specifications for Connector, Electrical Flat Cable and Printed Wiring Boards, Non-environmental, or color coded and should have a locking mechanism. (The detailed recommendations and requirements herein are consistent with Specification MIL-C-83503 (1984).)

Observation 14.2.2-f (connector mounting):

If connectors can be mounted such that they do not protrude beyond the edges of the front panel there will be less chance of damage during handling of the equipment.

14.2.3 Multipin Connectors for Differential Signals

Recommendation 14.2.3-a (connector shrouds):

Two row connectors on Modules, circuit boards, or auxiliary boards (mounted connectors) should have an integral shroud on at least three sides (four-sided shrouds are preferred). The shrouds should have a key that is compatible with the mating connector.

Observation 14.2.3-b (marking on connector housings):

A special mark (for example, a triangle) on the connector housing indicates the position of pin number one. The pin opposite is designated pin number two. The numbering continues alternating, with all pins numbered sequentially. The keying mechanism is along the odd pin number side of the connector.

Recommendation 14.2.3-c (visibility of designation):

The "pin one" designator or key mechanism should be visible when the connector is in the installed position.

Observation 14.2.3-d (connector orientation):

Multi-pin connectors on VMEbus boards will generally have the “pin one” designator pointing down. Because of the left right reversal of the board, Transition Modules will generally have the indicator up.

Recommendation 14.2.3-e (fixed "pin one" indication):

If the mounted connector is recessed or mounted in such a manner that the "pin one" designation on the connector is not visible, the housing, mounting surface, or panel should be marked to clearly denote "pin one". The recommended marking is an equilateral triangle 2.5 mm, minimum, on a side, near "pin one" with a vertex pointing toward "pin one". When multi-pin connectors do not have a shroud or a key, the housing, mounting surface or panel should clearly indicate the position of "pin one".

Recommendation 14.2.3-f (cable "pin one" indication):

The mating multi-contact cable connector should identify socket contact number one. This contact should mate with pin one of the connector.

Recommendation 14.2.3-g (keying of cable connectors):

It is recommended that the mating multi-contact cable connectors be keyed.

14.2.4 Differential Signals on Multi-contact Connectors

Recommendation 14.2.4-a (signal polarity assignments):

For differential signals on multipin connectors, the positive going signals should be on the odd numbered pins and the negative going signals on the even numbered pins.

Permission 14.2.4-b (signal pairing):

Where the differential signal pairs utilize the contact pairs 1-2, 3-4, etc. without gaps or interspersions, the markings described above will suffice.

Recommendation 14.2.4-c (signal/ground layout):

For configurations of differential signals with interspersed ground lines or other lines, or of other configurations that are not the simple 1-2, 3-4 layout, the signal configuration of the connector should be identified.

14.2.5 Differential Signals on Two-Contact Connectors

Recommendation 14.2.5-a (signal/ground layout):

For a cable that contains only one differential pair and that mates to a mounted multipin connector, the cable connector housing should be marked to clearly indicate the contact that is to mate with the odd numbered row of the mounted multipin connector. The mounted connector should be marked as described in Observation 14.2.3-b.

Recommendation 14.2.5-b (fixed housing marking):

If the mounted connector is a two-pin connector containing a single differential signal pair, there should be a clear indication as to the location of the positive signal.

14.3 Differential Interconnections for ECL

This specification is based on design recommendations of the major ECL logic manufacturers for signals connecting different parts of a system. They advise differential line driving and receiving for high noise immunity and cancellation of ground potential differences. This specification is consistent with IEC 60912 and IEC 60935 and with ANSI/IEEE 960.

14.3.1 Signal Amplitudes and Levels

Recommendation 14.3.1-a (ECL signals):

Signals should be ECL 10K or 10KH compatible differential pairs with nominal –0.9 V level on one line and nominal –1.7 V level on the other line.

14.3.2 ECL Drivers, Receivers and Terminators

Observation 14.3.2-a (output driver types):

ECL 10K or equivalent output drivers which deliver a nominal differential voltage swing of 1.6 V peak-to-peak (0.8 V with changing polarity) into the 100 Ω load (cable) are suitable.

Recommendation 14.3.2-b (driver pull-down resistors):

The driver should have pull-down resistors of such value as to permit a current that provides a full voltage swing as indicated above, into the cable's impedance. (See Figure 14.3.2-1)

Recommendation 14.3.2-c (cable terminators):

The cable terminators should be on the receiver side and shall be 100 Ω, unless specifically marked otherwise.

Observation 14.3.2-d (matching impedances):

When driving signals whose rise and fall time are less than half the propagation time of the cable, it is important that the differential characteristic impedance of the cable and the termination resistance are matched. For lossy cables proper termination is less important though attention should be paid to signal quality.

Observation 14.3.2-e (termination resistance):

In some specific implementations the cables used have characteristic impedances that differ substantially from 100 ohms. In such instances, if the signals are such that a close termination match is necessary, the user should replace the termination resistors to match the cable impedance. Such a change needs to be clearly noted on the device.

Recommendation 14.3.2-f (termination design):

It is recommended that the cable terminators be made symmetrical with respect to ground by, for example, connecting a 51 Ω, ± 5% resistor from each input point to the receiver reference voltage V_{bb} as specified for ECL with 100 Ω cable. In order to limit common mode currents to V_{bb} a resistor of approximately 100 Ω should be inserted between V_{bb} and the junction of the two 51 Ω resistors.

Observation 14.3.2-g (termination circuit):

Figure 14.3.2-1 illustrates the circuit elements for ECL cable drivers.

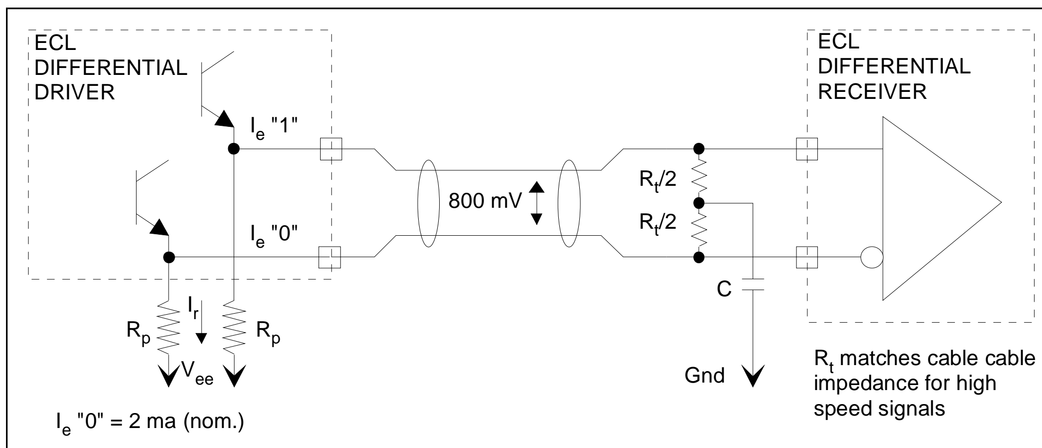

Figure 14.3.2-1
ECL Cable Driving Circuit

Note to Figure 14.3.2-1: The two resistors labeled $R_t/2$ and the capacitor to GND can be replaced with a single resistor R_t across the signal pair lines. See Chapter5 for grounding issues.

Observation 14.3.2-h (pull-down resistor calculation):

The value of the pull-down resistor R_p can be calculated by Equation 14.3.2-1. This ensures that at least 2 mA will flow from the emitter of the "0" state side to keep the emitter transistor biased on. It is sufficient to generate 800 mV across the cable terminator.

$$R_P = \frac{(V_{ee} - 1.7)R_t}{(0.8 + 0.002\,R_t)} \qquad \textbf{Equation 14.3.2-1}$$

where: R_p is the value of the pull-down resistor (in ohms)

V_{ee} is the value of the power supply voltage (typically –5.2 V or –4.5 V)

R_t is the value of the cable terminating resistor (in ohms)

Observation 14.3.2-i (general value for R_p):

When minimizing power is not necessary, R_p can be set at 240 Ω (V_{ee} = –5.2 V) or 200 Ω (V_{ee} –4.5 V). The value of R_p will accommodate cable impedances from 70 Ω to 140 ohms and limit the current flowing from the "1" state emitter to less than 30 mA. The power dissipation for both resistors is a constant 128 mW (for –5.2 V) or 104 mW (for -4.5 V). This single value resistor approach will cause power dissipated to be 35-40% higher than optimal for 100 Ω cables and up to 80% for 140 Ω cables. The single pull-down resistor scheme has the advantage that only the terminator needs to be adjusted to match the cable impedance.

Suggestion 14.3.2-j (receiver defined output state):

Design Modules to have the receiver output be in a defined state when the cable is not connected.

Observation 14.3.2-k (acheiving receiver output state):

The output state of the receiver can be set by offsetting one input with respect to the other by not less than 70 mV. Some receivers designed to achieve a defined state without an external bias.

14.3.3 Multi-pair Cables

The recommended multi-pair cables and usage for differential ECL are discussed in Section 14.2.

14.4 Front Panel Interconnections for NIM Logic

NIM signals originated in the NIM standard and are still popular. This digital signaling convention can be ideal for fast trigger generation and distribution as well as clock distribution. NIM logic is useful for long signal runs, when sub-nanosecond timing is important, where signal sources are widely separated and not conducive to cabling with ribbon style cables, and when a single-ended signal is preferred. In addition, for many temporary laboratory set-ups, NIM signals can be more quickly interconnected with readily available coaxial cable assemblies.

NIM offers many advantages over single-ended ECL data transmission. NIM's strengths lie in the use of coaxial cable and the fact that its drivers are current sources. The coaxial cable brings good immunity to crosstalk and reduced high frequency attenuation over long distances as compared to twisted pair. This helps maintain fast edge rates on signals and minimizes ringing.

14.4.1 Connectors and Cables for NIM Interconnects

Recommendation 14.4.1-a (cables):

50 Ω coaxial cables are recommended for NIM signal interconnects.

Recommendation 14.4.1-b (connectors):

Suitable connectors for NIM signal interconnects are listed in Chapter 1.

14.4.2 Polarity and Signaling Levels

Observation 14.4.2-a (single ended):

The current source driver, resistive termination strategy of NIM is an excellent solution for single ended signal distribution. The NIM driver in the logic "false" state is "off" (0 mA) except for leakage (±1 mA max.). The logic "false" voltage level is determined by ground at the termination resistor's location that is normally at the input to the receiver. The receiver then has control over both the "false" state level and the switching threshold. The driver's responsibility is to ensure a proper signal swing from the logic "false" to the logic "true" state. This method provides a considerably better noise margin then the single-ended ECL case where the receiver generates only a switching threshold and the driver can do whatever its local ground dictates!

Observation 14.4.2-b (negative logic):

When a logic "true" is to be generated, the NIM driver sinks 16 ± 2 mA, which develops a voltage across the termination resistor. In a nominal 50 Ω system the logic levels for NIM are: "false" = 0 ± 0.05 V and "true" = –0.8 ± 0.1 V. Note that this is inherently "negative" logic such that the leading edge of a timing pulse is "falling". This is the opposite of the ECL convention which is "positive" logic (important when conversion from NIM to ECL is to be made).

14.4.3 Double NIM

Observation 14.4.3-a (outputs and terminations):

A "Double NIM" output can sink 32 mA that is twice the normal 16 mA "true" NIM current. The double NIM output can be terminated with 50 Ω resistors in two places, such as both ends of a line. Double NIM outputs typically have two coaxial connectors connected in parallel on the front panel of a Module. If only a single coaxial line is to be driven, then the other connector needs to be terminated with 50 Ω.

14.4.4 Bused NIM

The busing of NIM signals is achieved with bridged inputs. A bridged input consists of two coaxial connectors that are mounted on the front panel and connected together. Another method is to use coaxial "T" connectors. Both methods have the accompanying risk of reflections on the cable and a loss of fidelity of the distributed signal. The reflection can be minimized by connecting each of the bridged input connectors to the receiver input instead of to each other and then to the receiver (see Figure 14.4.4-1).

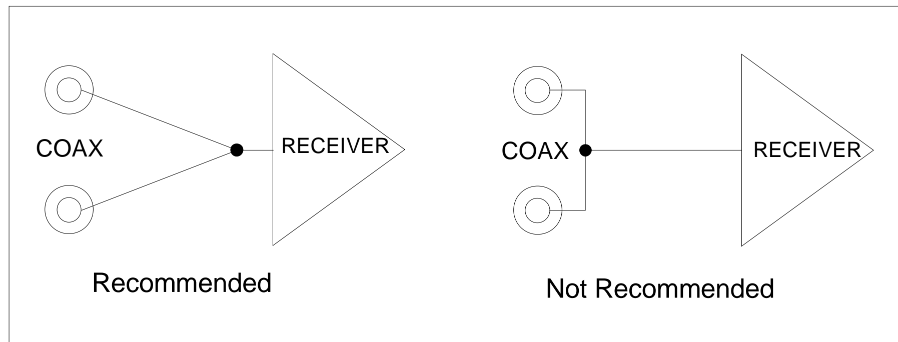

Figure 14.4.4-1
Methods of bridging NIM inputs

14.5 Front Panel Interconnections for TTL Logic

Recommendation 14.5-a (implementation):

TTL is not recommended for front-panel interconnects. It should be used on an "as needed" basis, such as connecting existing designs or the implementation of a "proprietary" bus between two sister Modules.

Observation 14.5-b (TTL properties):

- TTL has the following undesirable properties:
- Large voltage swing
- Hard to terminate properly unless using high-current drivers
- Large δV/δt which can radiate and cross-talk
- Lack of differential drivers and receivers

Recommendation 14.5-c (markings):

All TTL front-panel input and outputs should be identified.

14.6 Low Voltage Differential Logic Interconnections

This section is based on the (IEEE) P1596.3 draft standard Low-Voltage Differential Signals (LVDS) for Scaleable Coherent Interface (SCI). It is an electrical specification compatible with digital CMOS processes operating from 2 V to 5 V power supplies. Signals are uni-directional, point to point (one driver and one receiver) connections. LVDS input and output cells are available for custom ICs. The standard is appropriate for connections between boards within a chassis and short (<5 M) chassis to chassis interconnections. The interconnection techniques could include wire bonds, multi-chip modules, packages and pins, printed circuit boards, and cables with connectors. The standard does not specify particular cables or connectors. The use of this technology is expected to expand as low voltage designs develop. See Chapter 1 for typical components.

This standard specifies very high speed (500 Mbits per second), low voltage swing (400 mV maximum) differential signals. The differential signaling provides adequate noise margin in practical systems. Each receiver is assumed to have termination resistors. The ground potential difference is 950 mV maximum.

Advances in technologies (BiCMOS, FPGAs, etc.) makes it increasingly possible to avoid power-hungry ECL for high-speed applications and thus also avoid the need for negative voltage power supplies. In such case, a signaling standard with comparable performance and similar advantages as differential ECL, but compatible to BiCMOS technology becomes very attractive.

14.6.1 LVDS Main Characteristics

LVDS, like differential ECL, exhibit:

- near constant total drive current (decreasing noise on the supplies).
- excellent immunity to ground potential differences (between driver and receiver) and induced noise.
- low EMI (low, equal and opposite currents create small and canceling electromagnetic fields).

In addition to the electrical characteristics above, LVDS has other features that are useful in systems. The receiver output goes into the high state under any of the following conditions:

- The receiver is powered and the driver is not powered.
- The input wire pairs are shorted.
- The input wire pairs are disconnected.

Rule 14.6.1-a (LVDS signal specifications):

LVDS signals shall conform to (IEEE) P1596.3.

Recommendation 14.6.1-a (no bus with LVDS):

Because of signal distortion, LVDS connections should not be chained. Modules should have receiver - driver pairs (repeaters) to pass signals to other Modules.

Recommendation 14.6.1-b (signal polarity):

The output of LVDS receivers should be active low to detect the failure of cables or drivers.

14.6.2 LVDS Voltage Levels

Observation 14.6.2-a (driver signal specifications):

At the driver side (100 Ω load across opposite polarity outputs) the following specifications apply:

- (V_{oh}) min.: 1.4 V
- (V_{ol}) max.: 1.0 V
- (V_{od}) differential output swing: 250 mV min., 350 mV typical, 400 mV max.
- loop current high state: +3.5 mA typical.
- loop current low state: –3.5 mA typical

Observation 14.6.2-b (receiver signal specifications):

At the receiver side the following apply:

- common mode input range: 0 to 2.4 V (referred to receiver ground)
- differential input threshold “high”: +100 mV max.
- differential input threshold “low”: –100 mV max.
- input current: ± 1 µA typical, ± 10 µA max.

14.6.3 Differential Noise Margins

Observation 14.6.3-a (margins):

The “high” and “low” noise margins are 150 mV min., 250 mV typical.

14.6.4 Switching

Observation 14.6.4-a (rise/fall time):

Typical rise and fall times are 300 ps.

14.6.5 Drivers and Receivers

Observation 14.6.5-a (typical drivers/receivers):

Typical drivers and receivers are listed in Chapter 1.

14.6.6 Power Comparison

Observation 14.6.6-a (ECL and LVDS):

The power consumption between differential ECL and LVDS compare as follows:

- 10H124/10H125 driver/receiver pair: 120 mW per channel.
- DS90C031/DS90C032 driver/receiver pair: 20 mW per channel.

14.6.7 Multi-pair Cables

The recommended multi-pair cables and usage for LVDS are discussed in Section 14.2.

14.7 PECL

PECL is an ECL family of logic that uses +5 V and 0 V as the power connections to the integrated circuit rather than 0 volts and –5.2 V as in ECL. In fact, ECL circuits can be used as PECL circuits by simply connecting the positive power terminal to +5 V and the negative power terminal to 0 volts. The advantage of the +5 V power comes when mixing TTL and ECL on the same board. This means that only one power supply is necessary. However, the designer has to be careful when constructing the power distribution since noise from the TTL system can feed into the outputs of the PECL devices. PECL, as is also true for ECL, has no rejection for noise on the positive rail. The outputs of PECL are terminated in a similar fashion to ECL, but use +3 V instead of –2 V. In cases where +3 V power is available a separate supply for the terminators is saved. If a +3 V supply is not available one needs to be added or the outputs terminated with a Thevenin circuit. Some devices use +3 V (note: +3.3 V does not have the requisite 2 V drop from the positive rail).

The use of PECL exterior to the board is not recommended. A standard design requirement for external signals is to have them survive a short to ground. This is a common problem since cables attached to the PECL outputs can easily be shorted to ground.

14.8 RS-422A and RS-485 Interconnections

RS 422A is a point-to-point differential signaling specification originally developed for replacing RS-232-C. Differential signaling eliminates the ground-referenced nature of RS-232. This improves noise immunity. RS-485 is similar to RS-422A except that it is specified as a party line. Both specifications are length sensitive as Table 14.8-1 shows.

Table 14.8-1
Data Rate vs. Line Length
for RS-422A and RS-485

Line Length	Max. Data Rate
12 Meters	10 Mb/s
120 Meters	1 Mb/s
1200 Meters	100 kb/s

14.8.1 RS-422A and RS-485 Circuits

The following integrated circuits are examples of possible interfaces.

Drivers:

- AM26LS31: Specified at up to 20 Mb/s
- 75ALS192: This is a 30 Mb/s equivalent of the 26LS31

Receivers:

- AM26LS32: Specified at up to 20 Mb/s
- 75ALS197: This is a 30 Mb/s equivalent of the 26LS32

14.8.2 Multi-pair Cables

Recommended multi-pair cables and usage with RS-422A and RS-485 are discussed in Section 14.2

14.9 Coaxial Connectors

14.9.1 Coaxial Signal Connectors

Recommendation 14.9.1-a (coaxial signal connectors):

Coaxial signal connectors should be of the types listed below:

- Series SMB connectors in accordance with IEC Publication 60169-10, first edition (1983). Also MIL-C-39012 October 1993, slash sheets 39012\67-70 dated 17 October 1988. (1984).
- Type 50CM connectors in accordance with Subsection 4.2.5 of ANSI/IEEE 583, "Modular Instrumentation and Digital Interface System (CAMAC)." Commercial designations include LEMO and Kings K-Loc.
- 50 ohm BNC type in accordance with IEC Publication 60313, "Coaxial Cable Connectors used in Nuclear Instrumentation", also defined in ANSI Standard N544, "Signal Connectors for Nuclear Instruments."

Observation 14.9.1-b (other coaxial connectors):

Other coaxial connectors may be used where system configurations demand them. For example, SMC (screw fixing version of SMB) might be necessary where a more positive attachment was necessary. If other cable impedances are required, such as 75 ohm, then SMA might be appropriate.

14.9.2 Coaxial High-Voltage Connectors

Observation 14.9.2-a (voltage limitation applied to coaxial connectors):

Safety regulations require coaxial connectors for high voltage applications up to 5 kV be the "Safe High Voltage Connectors" (commonly referred to as Type SHV). These connectors are in accordance with ANSI Standard N42.4, "High Voltage Coaxial Connectors for Nuclear Instruments" and are also defined as Type B Connector in IEC Publication 60498 (1975), “High-voltage Coaxial Connectors used in Nuclear Instrumentation."

Observation 14.9.2-b (SHV high-voltage connectors):

The SHV high-voltage connectors are of the "safe" type in that the pin and socket contacts are securely recessed in the connector so as to minimize the possibility of electrical shock when the connectors are handled with rated voltage applied.

15 Components

This chapter provides information regarding typical components found in both Modules and subracks. The listing is not complete and inclusion herein does not imply endorsement. Other manufacturers that make compatible devices will be listed in future additions of this document as they are brought to the attention of the editors.

The user is cautioned to check with the manufacturer before ordering parts since catalog items change from time to time. Checking with manufacturers is advisable also because additional products are continually being introduced and improvements are made to existing products.

15.1 Backplane and Module Connectors

Figure 15.1-1 shows the connector positions and the nomenclature used herein to identify their placement.

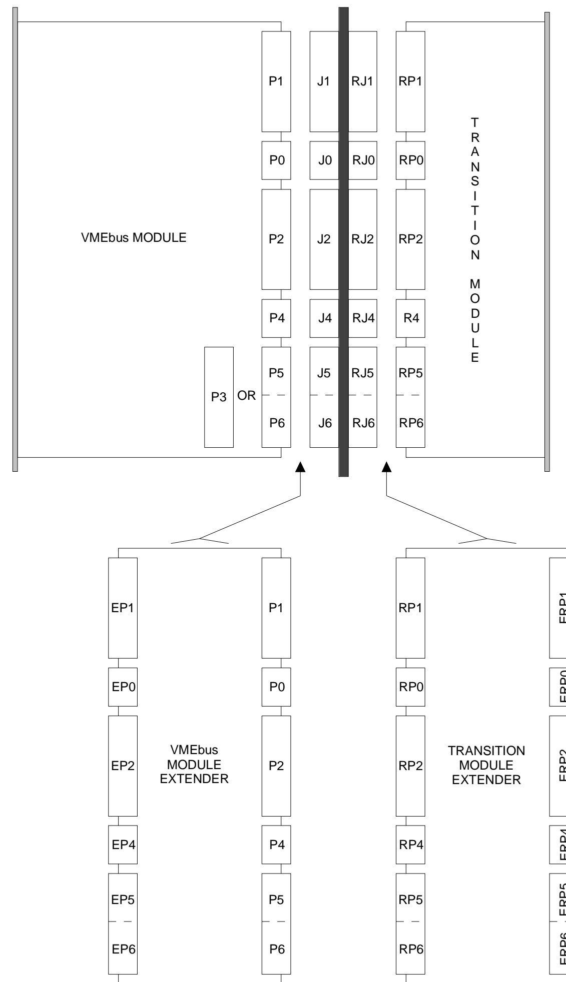

Figure 15.1-1
Connector Designations and Locations Diagram

15.1.1 VMEbus Board Connectors

VMEbus Modules use right-angle connectors on the printed circuit boards. Table 15.1.1-1 lists Module connectors and their placement. The 160 pin DIN connectors are available only in solder versions. The 2 mm hard metric connectors are available only in press fit. The keyed connector at P6 is preferred since it offers extra guidance for rear transition modules.

Table15.1.1-1
VMEbus Module Connectors

Connector Type	Placement
3-row, 96-pin DIN[1]	P1, P2, P3
5-row, 160-pin DIN	P1, P2, P3
5-row, 95-pin 2 mm[2]	P0, P4
5-row, 110-pin 2 mm	P5
5-row, keyed, 110-pin 2 mm	P6
5-row, 125-pin 2 mm	P6

Note: 1) DIN refers to connectors made to DIN 41912 or IEC 60603-2.

2) 2 mm refers to connectors made or IEC 61076-4-101, Level 2.

15.1.2 Subrack Backplane Connectors

VMEbus backplanes use straight connectors on the printed circuit board. All connectors have long tails for rear attachment of Transition Modules or cables. Table 15.1.2-1 lists backplane connectors and their placement.

Table 15.1.2-1
Backplane Connectors

Connector Type	Placement
3-row, 96-pin DIN	J1, J2, J3
5-row, 160-pin DIN	J1, J2, J3
5+2-row, 95-pin 2 mm HM	J0, J4
5+2-row, 110-pin 2 mm HM	J5
5+2-row, keyed, 110-pin 2 mm HM	J6
5+2-row, 125-pin 2 mm HM	J6

15.1.3 Transition Module Connectors

VMEbus Transition Modules use right-angle connectors on the printed circuit board. Table 15.1.3-1 lists Transition Module connectors and their placement.

Table 15.1.3-1
Transition Module Connectors

Connector Type	Placement
3-row, 96-pin DIN	RP1, RP2, RP3
5-row, 160-pin DIN	RP1, RP2, RP3
5-row, 95-pin 2 mm HM	RP0, RP4
5-row, 110-pin 2 mm HM	RP5
5-row, keyed, 110-pin 2 mm HM	RP6
5-row, 125-pin 2 mm HM	RP6

15.1.4 VMEbus Extender Connectors

VMEbus Extenders use right-angle connectors on the printed circuit board. Table 15.1.4-1 lists extender board connectors for VMEbus Modules and their placement. The extender connectors that attach to the backplane are the same as for VMEbus Modules in Table 15.1.1-1. The connectors that are outboard are listed in Table 15.1.4-1.

Table 15.1.4-1
VMEbus Module Extender Connectors

Connector Type	Placement
3-row, 96-pin DIN	EP1, EP2, EP3
5-row, 160-pin DIN	EP1, EP2, EP3
5-row, 95-pin 2 mm HM	EP0, EP4
5-row, 110-pin 2 mm HM	EP5
5-row, keyed, 110-pin 2 mm HM	EP6
5-row, 125-pin 2 mm HM	EP6

15.1.5 Transition Module Extender Connectors

Transition Module Extenders use right-angle connectors on the printed circuit board. Table 15.1.5-1 lists extender board connectors for Transition Modules and their placement. The extender connectors that attach to the backplane are the same as for Transition Modules in Table 15.1.3-1. The connectors that are outboard are listed in Table 15.1.5-1.

Table 15.1.5-1
Transition Module Extender Connectors

Connector Type	Placement
3-row, 96-pin DIN	ERP1, ERP2, ERP3
5-row, 160-pin DIN	ERP1, ERP2, ERP3
5-row, 95-pin 2 mm HM	ERP0, ERP4
5-row, 110-pin 2 mm HM	ERP5
5-row, keyed, 110-pin 2 mm HM	ERP6
5-row, 125-pin 2 mm HM	ERP6

15.1.6 Shields

The use of certain bottom shields can interfere with the adjacent Module insertion or withdrawal. The shield, in some styles, extends beyond the Module's solder side datum. The bottom shield is omitted in most designs since the majority of shielding is provided by the top shield. Table 15.1.6-1 lists connector shields and their placement.

Table 15.1.6-1
Shields

Connector Type	Placement
5-row, 95-pin 2 mm HM	S0, S4
5-row, 110-pin 2 mm HM	S5
5-row, keyed, 110-pin 2 mm HM	S6
5-row, 125-pin 2 mm HM	S6

15.1.7 Shrouds

VMEbus backplanes use shrouds to protect the pins extending from the rear and act as a guide for the Transition Module connector. In addition to the shroud, a spacer is necessary to adjust the insertion depth for the backplane thickness. Shrouds and spacers are typically paired and are obtained from the same manufacturer. Some vendors can adjust the insertion depth with an integral shroud-spacer. Table 15.1.7-1 lists shrouds and their placement.

Table 15.1.7-1
Shrouds

Connector Type	Placement
3-row, 96-pin DIN	SR1, SR2, SR3
5-row, 160-pin DIN	SR1, SR2, SR3
5-row, 95-pin 2 mm HM	SR0, SR4
5-row, 110-pin 2 mm HM	SR5
5-row, keyed, 110-pin 2 mm HM	SR6
5-row, 125-pin 2 mm HM	SR6

15.1.8 Current Ratings

Table 15.1.8-1
VMEbus Connector Current Ratings

Connector	30° C	60° C
96 and 160 pin DIN Style	1.5 A	1.25 A
Hard Metric Pins	1.4 A	1.2 A
Hard Metric Shield Pins	1.0 A	1.0 A

The shield pin current rating is less than the signal pin current rating because they only make contact on one edge. The signal pins have contact on two surfaces.

15.1.9 160 pin – IEC 61076-4-113 Manufacturers

Harting Electronic Inc.
2155 Stonington Avenue, Suite 212
Hoffman Estates, IL 60195
ph: 847-519-7700
fax: 847-519-9771
URL: www.harting.pader.net

AMP Incorporated
Harrisburg, PA
ph: 717-564-0100
fax: 717-986-7813
URL: www.amp.com

15.1.10 2 mm Connector and Related Hardware

Manufacturers of 2 mm Hard Metric connectors also make associated hardware which can be of use to the system designer. Most of the hardware described below can be used in conjunction with VMEbus Modules

and Transition Modules. Cavities are per DIN 41612 type M, power and coax interfaces are per DIN 41626.

Some general features of these connectors are as follows:

a) Cable connectors for single conductor and twisted pair, shielded or unshielded, are made to plug directly onto the male pins. Backplane shrouds that have latching mechanisms to retain these cable connectors are available.

b) Some connector housings have 4.8 mm diameter holes for high current contacts. These contacts are made with ratings of 10 to 40 amperes. Some have connections onto the printed circuit board, others connect directly to wires from 16 AWG to 8 AWG.

c) The 4.8 mm housings have coax cable contacts for board mount or direct cable attachment. RG174, 188 and 316 are typical cable types.

d) Fiber optic contacts for single or multimode cable are also compatible with the 4.8 mm cavities. Typically these accommodate 125 µm diameter fiber.

e) Housings can have a mixture of 2 mm grid pins and 4.8 mm diameter cavities.

f) Key plugs are available for the 125 pin version of the 2 mm connectors. The key removes 3 rows (15 pins) from the center of the connector leaving the user with 110 pins. This key is not necessary for VIPA hardware since the function is provided by the keying mechanism built into the subracks and the Module panels. The keyed connectors are used in the PCI specification and could be specified for J3 if inserting PCI Modules onto the backplane.

The range of available hardware in the 2 mm Hard Metric technology is very broad and beyond the scope of this document to describe. The user is advised to contact one of the vendors below for details on the family.

AMP Incorporated
Harrisburg, PA
ph: 717-564-0100
fax: 717-986-7813
URL: www.amp.com

FCI/Berg Electronics
825 Old Trail Road
Etters, PA 17319
ph: 800-237-2374
fax: 717-938-7620
URL: www.berg.com

ERNI Components Inc.
112701 N. Kingston Ave.
Chester, VA 23831
ph: 804-530-5012
fax: 804-530-5232
URL: www.erni.com

Harting Electronic Inc.
2155 Stonington Avenue, Suite 212
Hoffman Estates, IL 60195
ph: 847-519-7700
fax: 847-519-9771
URL: www.harting.pader.net

15.1.11 Tooling

Most connectors used in VMEbus are now press fit. Special tooling and an arbor press with a capacity of several tons is needed to install these connectors. The holes for the press fit pins require tighter tolerances than solder holes. The board designer is encouraged to consult the connector manufacturer's data sheets for hole specifications. The manufacturers listed in Section 15.1.10 can furnish data for the 2 mm hard metric types. Hole data and tooling for the 96 and 160 pin connectors used for J1/P1 and J2/P2 can be obtained from:

Harting Electronic Inc.
2155 Stonington Avenue, Suite 212
Hoffman Estates, IL 60195
ph: 847-519-7700
fax: 847-519-9771
URL: www.harting.pader.net

AMP Incorporated
Harrisburg, PA
ph: 717-564-0100
fax: 717-986-7813
URL: www.amp.com

All connectors listed in Tables 15.1.1-1 through 15.1.5-1 are press fit with the exception of the DIN connectors in Table 15.1.1-1 and 15.1.4-1.

15.2 Coaxial Connectors

This section provides information regarding typical coax connectors found in both Modules and subracks. The listing is not complete and inclusion herein does not imply endorsement. Other manufacturers that make compatible devices will be listed in future additions of this document as they are brought to the editors attention.

Examples of Series SMB connectors (See Section 14.9.1 herein) are as follows:

Right angle receptacle for printed circuit:

AMP 228435-1
Sealectro (ITT/Cannon) 51-053-000

Front Panel front mount:

AMP 228216-1
Sealectro (ITT/Cannon) 51-045-000

Front Panel rear mount:

AMP 228215-1
Sealectro (ITT/Cannon) 51-043-000

Examples of Type 50CM connectors (See Section 14.9.1 herein) are as follows:

Right angle receptacle for printed circuit:

LEMO EPL.00.250.NTN
WW Fischer DLP101-A004-10

Printed circuit board end launch receptacle:

LEMO EPN.00.250.NTN
WW Fischer DP101 A-004-10

Right angle dual receptacle for printed circuit - two connectors in one body:

LEMO EPY.00.250.NTN

Front Panel rear mount:

LEMO ERA.00.250.CTL

15.3 Components for Low Voltage Differential Logic Interconnections

This Section provides information regarding typical LVDS integrated circuits found in VMEbus Modules. The listing is not complete and inclusion herein does not imply endorsement. Other manufacturers that make compatible devices will be listed in future additions of this document as they are brought to the editors attention.

Typical components are listed below:

National Semiconductor

DS90C031:

4 channels driver
TTL inputs
21 mA max. supply current
5 V supply
2 ns typ. propagation delay
400 ps max. differential skew
600 ps max. channel to channel skew

DS90C032:

4 channel receiver
10 uA input current
tri-stable TTL outputs
17 mA max. supply current
5 V supply
3 ns typ. propagation delay
500 ps max. differential skew
This driver/receiver pair allows 150 Mb/s transmission rate

QR0001 QuickRing Data Controller operating at 350 Mb/s) with LVDS, like differential ECL, exhibits:

- near constant total drive current (decreasing noise on the supplies)
- excellent immunity to ground potential differences (between driver and receiver) and induced noise.
- low EMI (low, equal and opposite currents create small and canceling electromagnetic fields)

15.4 Standard VMEbus Interface Integrated Circuits

The following listings are not complete and inclusion herein does not imply endorsement. Other manufacturers that make compatible devices will be listed in future additions of this document as they are brought to the editors attention.

Several Cypress interfaces are listed below. The designer is encouraged to contact Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134 for additional information.
(ph: 408-943-2600, URL: www.cypress.com)

VIC068A - VMEbus Interface Controller:

32 bit VMEbus interface Master/Slave interface. Address and data path only 8 bits in this chip. For full 32 bit interface other chips are required such as VAC068A.

VAC068A - VMEbus Address Controller:

Auxiliary chip for the VIC068A that implements I/O DMA, local memory mapping, and several other useful features. Provides 24 bits of address and data to complete VIC068A as 32 bit interface.

VIC64 - VMEbus Interface Controller with D64 Functionality:

Complete VME64 Master/Slave interface with MBLT capability.

CY7C960/CY7C961 - Slave VMEbus Interface Controller:

The CY7C960 Slave VMEbus Interface Controller is an integrated VME64 interface. It is 64-pin device that can be programmed to perform all transaction defined in the VME64 specification. The CY7C961 is a 100-pin device based upon the CY7C960 and includes additionally Remote Master capability such that the CY7C961 can be instructed to move data as a VMEbus Master.

The CY7C960 has the circuitry required to control large DRAM arrays and local I/O circuitry without the intervention of a local CPU. The CY7C960 fetches its own configuration parameters during the power-on reset. After reset it responds appropriately to VMEbus activity and controls local circuitry.

CY7C964 - Byte Wide Address and Data Path:

Byte wide address and data path for use with VIC068A or VIC64. Three chips required for full 64 bit interface in combination with VIC64.

The CY7C964 integrates several functions into one small package. It contains counters, comparators, latches, and drivers useful for interfacing with address and data buses, particularly VMEbus interfaces. The on-chip drivers can drive the VMEbus directly.

The CY7C964 is a companion part to Cypress's VIC068A, VIC64, the CY7C960, and CY7C961. Three or four of these devices are needed per controller to drive the address and data buses. The controllers provide the control and timing signals to the CY7C964 as it acts as a bridge between the VMEbus and the Local bus.

Several Tundra (formerly Newbridge) interfaces are listed below. The designer is encouraged to contact the Tundra Semiconductor Corporation, 603 March Road, Kanata, ON K2K 2M5, Canada for additional information.
(ph: 613-592-1320, URL: www.newbridge.com/Tundra/)

SCV64

The SCV64 (TM) transfers data rates up to 60 Mb/s on the VMEbus. The SCV64 uses internal FIFOs to decouple the transfer of data between the VMEbus and local bus to compensate for mismatches in relative bus performance. The SCV64 has block transfer capability (both BLT and MBLT), an integral DMA controller, an asynchronous VMEbus interface and 40 MHz local bus operation.

The SCV64's local bus interface also allows connections to a variety of processor families, including the following: Intel's x86 and ix60, Motorola's 680x0, and Texas Instruments TMS320Cx0. For Slave-only designs, the SCV64 offers auto-boot logic for automatic base addressing. Tundra can provide Verilog model and Logic Modeling support for the SCV64.

Universe:

The Universe(TM) uses built-in FIFOs to decouple the transfer of data between the VMEbus and PCI Bus, to compensate for mismatches in relative bus performance. In addition, the Universe offers block transfer capability including BLT and MBLT, an integral DMA controller, and a high speed VMEbus port.

As with the SCV64, the Universe implements a full suite of VMEbus address and data transfer modes including D64. In addition, it provides full VMEbus system controller functionality with multi-level arbitration modes. All VMEbus features are fully programmable from the PCI and VMEbus sides. With its other VMEbus functions, the Universe provides full VMEbus interrupter and interrupt handler capability, automatic system controller logic, and a multilevel VMEbus requester. The Universe uses BGA packaging technology with a contact array pitch of 0.050 inches; the package size is less than one square inch.

Trooper II:

Trooper II(TM) is for use as a VMEbus interface on intelligent Slave Modules such as communications, disk, SCSI boards, tape controllers, and image processors. It provides 43 direct connects to the VMEbus, so that 5 buffer chips (such as the 74F760) are adequate to complete the interface to the VMEbus and local bus.

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12. EMC/ESD Considerations

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14. I/O Connections - Physical

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