SIS3805
VME Multiscaler

User Manual

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2 Introduction

The SIS3805 is the high end 32 channel SIS multiscaler with regard to the implemented channel depth of 48-bit. The unit was originally designed for the FNAL CDF experiment and two different firmware designs are available to meet the requirements of a wider community of high data rate users. An overflow will not occur before 16 days of counting at the maximum frequency of 200 MHz with this design.
Both SIS3805 firmware designs are non auto clearing, i.e. the contents of the scaler channel is preserved upon readout/bank switch. The first design is a two bank implementation along the lines of the SIS3801, the second design is based on the shadow register concept of the SIS3800 scaler with the extension, that the contents of the shadow register is transferred to the FIFO.
As on all SIS360x/38xx boards the available input and output options are NIM, ECL and TTL via LEMO (NIM/TTL) or flat cable (ECL/TTL) connectors. Input to output level adaptations (TTL in, NIM out e.g.) can be implemented on request. The SIS3805 is a single width 6 U VME card, due to an on board DC-DC converter no non standard VME voltages are required for operation.
Like in the 24-bit SIS3801 design two user bits are latched into the data stream of the SIS3805 upon the next time slice signal to provide means to monitor the status of external parameters, like the actual state of a chopper wheel or a beam shutter.
All cards of the SIS360x/38xx family are equipped with the 5 row VME64x VME connectors, a side cover and EMC front panel, as well as the VIPA LED set. For users with VME64xP subracks VIPA extractor handles can be installed. The base board is prepared for VIPA style addressing, the current first version of the SIS3801 firmware does not feature VIPA modes yet however.
As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm. A list of available firmware designs can be retrieved from http://www.struck.de/sis3638firm.htm

3 Technical Properties/Features

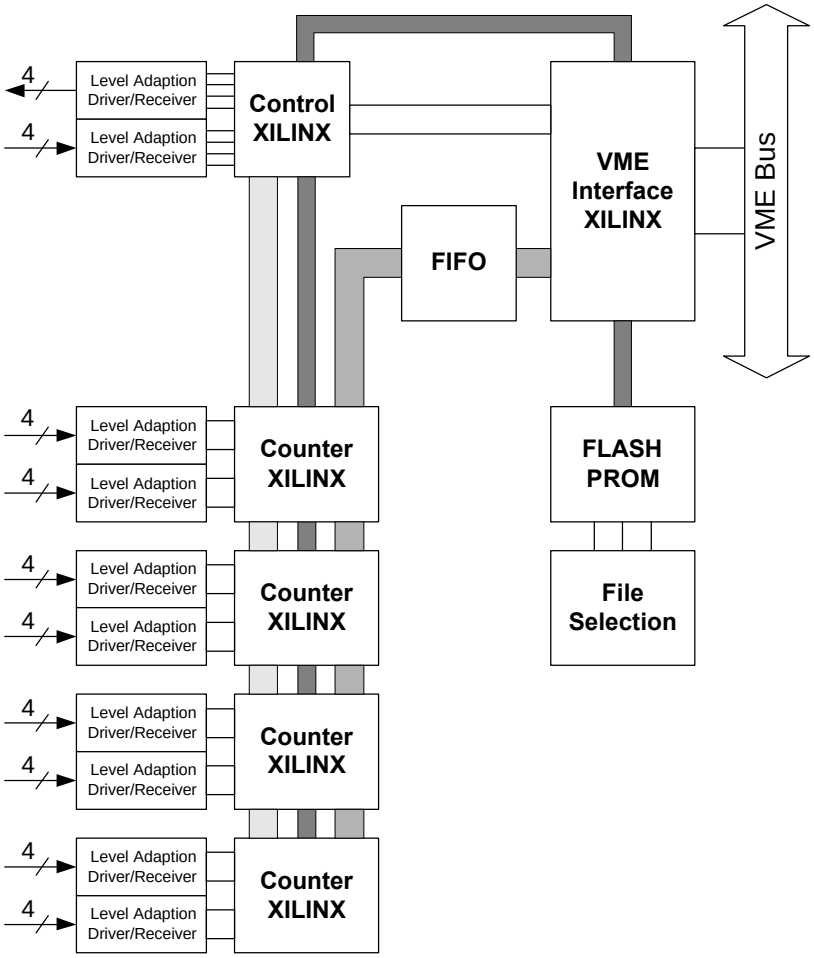
The SIS3805 is rather a firmware design in combination with given board stuffing options, than a name for the board (this is the reason, why the modules are named SIS360x/38xx on the front panel and the distinction of the units is made by the module identifier register). The firmware makes use of part of the possibilites of the SIS360x/38xx PCB, if the SIS3805 or other firmware designs of the family come close to what you need, but something is missing, a custom firmware design may be an option to consider.

Find below a list of key features of the SIS3801.

- 32 channels
- 200 MHz counting rate (ECL and NIM), 100 MHz for TTL
- 48-bit channel depth
- NIM/TTL/ECL versions
- flat cable (TTL/ECL) and LEMO (TTL/NIM) versions
- 64K FIFO (256 K available on request)
- A16/A24/A32 D16/D32/BLT32 (CBLT32 prepared)
- Base address settable via 5 rotary switches (A32-A12) and one jumper (A11)
- VME interrupt capability
- VIPA geographical addressing prepared
- VIPA LED set
- 14 µs minimum dwell time
- 2 external user bits
- Up to eight firmware files
- single supply (+5 V)

3.1 Board Layout

Xilinx FPGAs are the working horses of the SIS360x/38xx board series. The counter (prescaler, latch, ...) logic is implemented in one to four chips, each chip handles eight front end channels. The VME interface and the input and output control logic reside in two Xilinx chips also. The actual firmware is loaded into the FPGAs upon power up from a FLASHPROM under jumper control. The user can select among up to eight different boot files by the means of a 3-bit jumper array. The counter inputs, the control inputs and the outputs can be factory configured for ECL, NIM and TTL levels. The front panel is available as flat cable (ECL and TTL) or LEMO (NIM and TTL) version. The board layout is illustrated with the block diagram below:

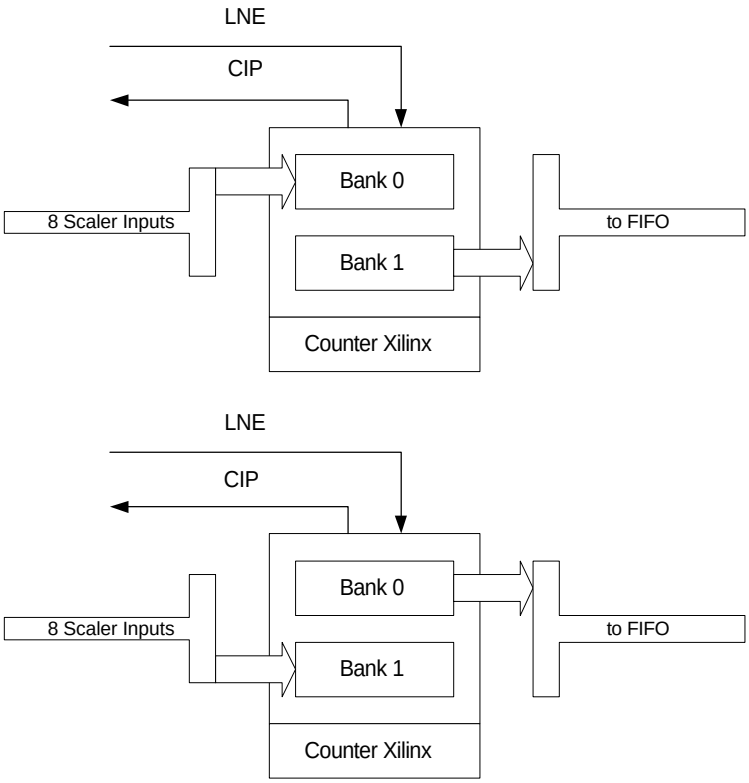


SIS3805 Block Diagram

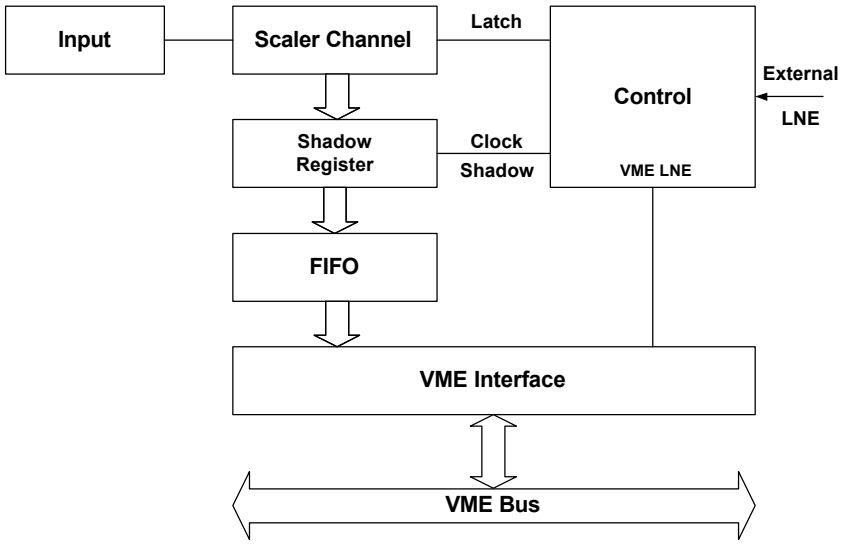
3.2 Counter Design and Modus Operandi

The counters are implemented in XILINX FPGAs. One of the counter FPGAs holds 8 48-bit deep counter channels. Two counter banks are implemented in the SIS3805 version 1 design, the actual multiscaling mechanism is implemented as bank switching between the two counter banks and copying the data of the inactive bank to the FIFO. Bank switching can be initiated via an external pulse or a VME command. A sketch of the bank mechanism can be found below.

In the second firmware design (SIS3805 version 2) multiscaling is implemented via a shadow register, which contents is passed to the FIFO. This version is basically of read on the fly type like the SIS3800, but the data are read through the FIFO instead of a direct read from the shadow register. A sketch of this mechanism can also be found below. Both SI3805 are non clearing multiscaler versions, i.e. the counts of the current time slice are added to the counts which have been acquired earlier. This implies, that the counts are scattered over the two banks in the SIS 3805 version 1 (bank switching) design.



SIS3805 version1 bank switching principle



SIS3805 version2 shadow principle

3.2.1 SIS3805 Version 1 (bank design)

The version 1 design behaves like a SIS3801 multi scaler with the exception, that the inactive bank is not cleared after its data are transferred to the FIFO. The result of the data obtained from the readout are accurate, but during the bank switching phase, which takes in the order of 5ns, a count may be acquired by the old bank, by the new bank or may be not seen at all. Depending on the application

3.2.2 SIS3805 Version 2 (shadow design)

The version 2 design acts like a standard scaler, which data are clocked to the shadow register and transferred to the FIFO afterwards. The main advantage is, that the counts are not scattered over the two banks. As the shadow register is a read on the fly, the status of the lowest 6 bits may be inaccurate, but no counts are lost, i.e. if the counter is disabled before readout or no counts are seen by the unit during the shadow process the result over the full counting period is accurate.

3.3 Minimum Dwell Time

In nuclear physics on refers to the time slice length (i.e. the period during which counts are acquired into the same bank) as dwell time. In many cases the dwell time will be constant, but the user is free to use varying time intervals, as long as the minimum time between two next event pulses is smaller than the minimum dwell time. An approach to measure the length of the time slices is the readout of a fixed frequency clock on one of the counter channels, the accuracy of the measurement is defined by the frequency stability of the clock and the interval length.

The minimum dwell time on the SIS3805 isdefined by the time which is needed to copy the data from the idle scaler bank (version 1) or the shadow register (version 2) to the FIFO. The time required to copy one 64-bit data word from the counter Xilinx chips to the FIFO is some 400 ns. The overhead is 600 ns, thus the minimum dwell time is some14 µs.

3.4 Readout Considerations

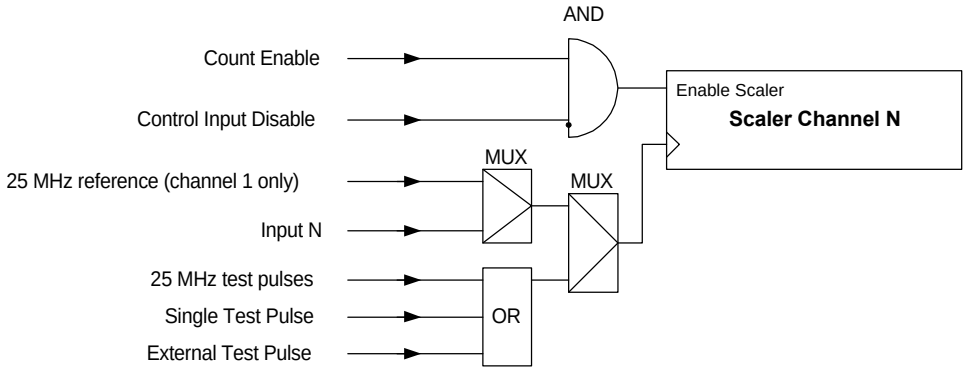
One of the major advantages of a FIFO based counter/multiscaler is the decoupling of the time slice/bank switching and the actual VME readout of the data. Depending on the application the FIFO may be used to buffer one or two reads only, before a DSP processes the data on the fly, in this case the FIFO is used to establish readout pipelining, in other cases the maximum possible FIFO size is of interest to store a complete set of data points for a pulsed or non continuous measurement. Continuous multiscaling can be established as long as the VME master can cope with the amount of data generated by the scaler, i.e. the FIFO is never allowed to run into the FIFO full condition. The 64K default FIFO size of the SIS3805 is considered to be a save value for most applications, for more demanding applications the FIFO size can be increased to 256K. One as to keep in mind, that four FIFO words are needed to hold one 48-bit scaler value, i.e. a 64K FIFO can hold 16K scaler words or 0.5K events (time slices) with all 32 channels enabled. The packing of the FIFO data into VME D32 words is handled without user intervention upon VME read cycles from the FIFO. In high data rate applications, the readout scheme will make use of the FIFO half full flag via a VME interrupt or polling in most cases, as a minimum known number of 32K longwords can be read out (being blocked into smaller chunks by VME) with a block transfer.

Example: Assume 32 channels are read out with a dwell time of 20 µs (i.e. at a rate of 50 KHz). The data rate is 32 channels x 8 bytes x 50 KHz corresponding to some 12 MB/s. The FIFO half full interrupt or flag will be asserted for the first time after 0.5 ms of data acquisition, the VME master has to digest 64Kbytes within less than 0.5 ms (including IRQ handling or polling) to prevent the FIFO from overflow.

Note: No new data can be acquired before a FIFO reset if the FIFO full condition has occurred (i.e. the FIFO full condition is considered an error condition, which should not occur in standard operation).

3.5 Count Enable Logic

A channel acquires input or test counts, if the count enable and the global count enable conditions are true. Via the test enable toggle bits in the control register the input of the counter is switched to test pulses or front panel signals.



4 Getting Started

The minimum setup to operate the SIS3805 requires the following steps:

- Check the proper firmware design is selected (should be design zero, i.e. all jumpers of jumper array J500 set.
- Select the VME base address for the desired addressing mode
- Select the VME SYSRESET behaviour via J520
- turn the VME crate power off
- install the scaler in the VME crate
- connect your signals to the counter
- turn crate power back on
- issue a key reset by writing to 0x60
- issue FIFO clear by writing to 0x20
- enable next logic by writing to 0x28
- issue first next clock pulse to start counting by soft- or hardware
- after one or more subsequent next clock pulses data can be read from the FIFO from the addresses 0x100 through 0x1FC.

A good way of checking first time communication with the SIS3805 consists of switching on the user LED by a write to the control register at offset address 0x0 with data word 0x1 (the LED can be switched back off by writing 0x100 to the control register)..

4.1 Factory Default Settings

4.1.1 Adressing

SIS3805 boards are shipped with the En_A32, the En_A24 and the En_A16 jumpers installed and the rotary switches set to:

Switch	SW_A32U	SW_A32L	SW_A24U	SW_A24L	SW_A16	J A_11	Bits 7-4	Bits 3-0
Setting	3	8	3	8	3	8	0	0

Jumper A_11 is open (bit 11 set).
Hence the unit will respond to the following base addresses:

Mode	Base address
A32	0x38383800
A24	0x383800
A16	0x3800

Firmware Design
Design 0 (SIS3805, Version 1) of the FLASHPROM is selected (all jumpers of jumper array J500 set).

4.1.2 System Reset Behaviour

J520 is set, i.e. the SIS3805 is reset upon VME reset.

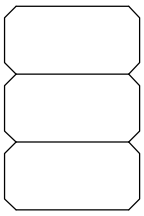
5 Firmware Selection

The FLASH PROM of a SIS360x/38xx board can contain several boot files. A list of available FLASHPROM versions can be found on our web site http://www.struck.de in the manuals page. If your FLASHPROM has more than one firmware design, you can select the desired firmware via the firmware selection jumper array J500 . You have to make sure, that the input/output configuration and FIFO configuration of your board are in compliance with the requirements of the selected firmware design (a base board without FIFO can not be operated as multi channel scaler e.g.). A total of 8 boot files from the FLASHPROM can be selected via the three bits of the jumper array. The array is located towards the rear of the card between the VME P1 and P2 connectors. The lowest bit sits towards the bottom of the card, a closed jumper represents a zero, an open jumper a one.

5.1 Examples

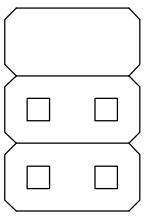
The figures below show jumper array 500 with the soldering side of the board facing the user and the VME connectors pointing to the right hand side.

Bootfile 0 selected



With all jumpers closed boot file 0 is selected

Bootfile 3 selected



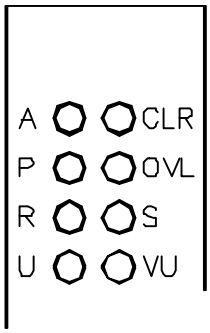
With the lowest two jumpers open bit 0 and bit 1 are set to 1 and hence boot file 3 is selected

Front Panel LEDs

The SIS3805 has 8 front panel LEDs to visualise part of the units status. Three LEDs according to the VME64xP standard (Power, Access and Ready) plus 5 additional LEDs (VME user LED, Clear, Copy in Progress, Scaler enable and VIPA user LED).

Designation	LED	Color	Function
A	Access	yellow	Signals VME access to the unit
P	Power	red	Flags presence of VME power
R	Ready	green	Signals configured logic
U	VME user LED	green	To be switched on/off under user program control
CLR	Clear	yellow	Signals bank clear
OVL (CIP)	Copy in Progress	red	Signals copy in progress
S	Scaler Enable	green	Signals one or more enabled channels
VU	VIPA user LED	green	for future use

The LED locations are shown in the portion of the front panel drawing below.



The VME Access, the Clear and the Scaler enable LED are monostable (i.e. the duration of the on phase is stretched for better visibility), the other LEDs reflect the current status.
An LED test cycle is performed upon power up (refer to the chapter 16.1).

6 VME addressing

6.1 Address Space

As bit 11 is the lowest settable bit on the 360x/38xx board, an address space of 2 Kbytes (Offset plus 0x000 to 0x7ff) is occupied by the module.

6.2 Base Address

6.2.1 VME

The VME addressing mode (A16/A24/A32) is selected via the jumpers EN_A16, EN_A24 and EN_A32.The mode is selected by closing the corresponding jumper, it is possible to enable two or all three addressing modes simultaneously.
The base address is set via the five rotary switches SW_A32U, SW_A32L, SW_A24U, SW_A24L and SW_A16 and the jumper J_A11. The table below lists the switches and jumpers and their corresponding address bits.

Switch/Jumper	Affected Bits
SW_A32U	31-28
SW_A32L	27-24
SW_A24U	23-20
SW_A24L	19-16
SW_A16	15-12
J_A11	11

In the table below you can see, which jumpers and switches are used for address decoding in the three different addressing modes (fields marked with an x are used).

	SW_A32U	SW_A32L	SW_A24U	SW_A24L	SW_A16	J_A11
A32	x	x	x	x	x	x
A24			x	x	x	x
A16					x	x

Note: J_A11 closed represents a 0, J_A11 open a one

6.2.2 VIPA/VME64x

As the VME64x and the VME64xP (VIPA) standard are not yet standards to refer to and to declare conformity with, addressing modes (like geographical addressing e.g.) according to these standards are prepared but not yet implemented in the current firmware revisions.

6.3 Address Map

The SIS360x/38xx boards are operated via VME registers, VME key addresses and the FIFO (where installed). The following table gives an overview on all SIS3801 addresses and their offset from the base address, a closer description of the registers and their function is given in the following subsections.

Offset	Key	Access	Type	Function
0x000		R/W	D16/D32	Control and Status register
0x004		R/W	D16/D32	Module Identification and IRQ control register
0x00C		W	D16/D32	Copy disable register
0x010		W	D16/D32	Write to FIFO (in FIFO test mode)
0x020	KA	W	D16/D32	clear FIFO, logic and counters
0x024	KA	W	D16/D32	VME next clock
0x028	KA	W	D16/D32	Enable next clock logic
0x02C	KA	W	D16/D32	Disable next clock logic
0x030	KA	W	D16/D32	Broadcast, clear FIFO, logic and counters
0x034	KA	W	D16/D32	Broadcast; VME next clock
0x038	KA	W	D16/D32	Broadcast; Enable next clock logic
0x03C	KA	W	D16/D32	Broadcast; Disable next clock logic
0x060	KA	W	D16/D32	reset register (global reset)
0x068	KA	W	D16/D32	Test pulse (generate a single pulse)
0x100-0x1FC		R/(W)	D16/D32/ BLT32	read FIFO

Note: D08 is not supported by the SIS38xx boards

The shorthand KA stands for key address. Write access with arbitrary data to a key address initiates the specified function

7 Register Description

7.1 Status Register (0x0)

The status register reflects the current settings of most of the SIS3805 parameters in read access, in write access it functions as the control register.

Bit	Function
31	Status VME IRQ source 3 (FIFO full)
30	Status VME IRQ source 2 (FIFO half full)
29	Status VME IRQ source 1 (FIFO almost empty)
28	Status VME IRQ source 0 (start of CIP)
27	VME IRQ
26	internal VME IRQ
25	0
24	0
23	Status VME IRQ Enable Bit Source 3
22	Status VME IRQ Enable Bit Source 2
21	Status VME IRQ Enable Bit Source 1
20	Status VME IRQ Enable Bit Source 0
19	software disable counting bit
18	Status external disable
17	Status enable external clear
16	Status enable external next
15	Status Enable next logic
14	0
13	0
12	FIFO flag full
11	FIFO flag almost full0
10	FIFO flag half full
9	FIFO flag almost empty
8	FIFO flag empty
7	Status broadcast mode handshake controller
6	Status broadcast mode
5	Status input test mode
4	Status 25 MHz test pulses
3	Status input mode bit 1
2	Status input mode bit 0
1	Status FIFO test mode
0	Status user LED

The reading of the status register after power up or key reset is 0x300 (see default settings of control register).

7.2 Control Register (0x0)

The control register is in charge of the control of most of the basic properties of the SIS3805 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which has a different location within the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

Bit	Function
31	disable IRQ source 3 (*)
30	disable IRQ source 2 (*)
29	disable IRQ source 1 (*)
28	disable IRQ source 0 (*)
27	clear software disable counting bit (*)
26	disable external disable (*)
25	disable external clear (*)
24	disable external next (*)
23	enable IRQ source 3
22	enable IRQ source 2
21	enable IRQ source 1
20	enable IRQ source 0
19	set software disable counting bit (*)
18	enable external disable (*)
17	enable external clear (*)
16	enable external next (*)
15	disable broadcast mode handshake controller (*)
14	disable broadcast mode (*)
13	disable input test mode (*)
12	disable 25 MHz test pulses (*)
11	clear input mode bit 1 (*)
10	clear input mode bit 0 (*)
9	disable FIFO test mode
8	switch off user LED (*)
7	enable handshake controller for broadcast mode
6	enable broadcast mode
5	enable input test mode
4	enable 25 MHz test pulses
3	set input mode bit 1
2	set input mode bit 0
1	enable FIFO test mode
0	switch on user LED

(*) denotes the default power up or key reset state

7.3 Module Identification and IRQ control register (0x4)

This register has two basic functions. The first is to give information on the active firmware design. This function is implemented via the read only upper 20 bits of the register. Bits 16-31 hold the four digits of the SIS module number (like 3805 or 3600 e.g.), bits 12-15 hold the version number. The version number allows a distinction between different implementations of the same module number, the SIS3801 for example has the 24-bit mode with user bits and the straight 32-bit mode as versions.

Bit	Read/Write access	Function	
31	read only	Module Identification Bit 15	Module Id Digit 3
30	read only	Module Identification Bit 14	
29	read only	Module Identification Bit 13	
28	read only	Module Identification Bit 12	
27	Read only	Module Identification Bit 11	Module Id Digit 2
26	read only	Module Identification Bit 10	
25	read only	Module Identification Bit 9	
24	read only	Module Identification Bit 8	
23	read only	Module Identification Bit 7	Module Id Digit 1
22	read only	Module Identification Bit 6	
21	read only	Module Identification Bit 5	
20	read only	Module Identification Bit 4	
19	read only	Module Identification Bit 3	Module Id Digit 0
18	read only	Module Identification Bit 2	
17	read only	Module Identification Bit 1	
16	read only	Module Identification Bit 0	
15	read only	Version Bit 3	
14	read only	Version Bit 2	
13	read only	Version Bit 1	
12	read only	Version Bit 0	
11	read/write	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	
10	read/write	VME IRQ Level Bit 2	
9	read/write	VME IRQ Level Bit 1	
8	read/write	VME IRQ Level Bit 0	
7	read/write	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	
6	read/write	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	
5	read/write	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	
4	read/write	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	
3	read/write	IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle	
2	read/write	IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle	
1	read/write	IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle	
0	read/write	IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle	

The second function of the register is interrupt control. The interrupter type of the SIS3805 is D08(O) . Via bits 0-7 of the module identifier and interrupt control register you can define the interrupt vector, which is placed on the VME bus during the interrupt acknowledge cycle. Bits 8 through 10 define the VME interrupt level, bit 11 is used to enable (bit set to 1) or disable (bit set to 0) interrupting.

Module identification and version example:

The register for a SIS3801 in straight 32-bit mode (version 1) reads 0x38011nnn, for a SIS3801 in 24-bit mode (version 2) it reads 0x38012nnn. (the status of the lower 3 nibbles is denoted with n in the example).

7.4 Copy disable register 0xC

The copy disable register can be used to exclude single channels or arbitrary groups of channels from the copy process. The value from the copy disable register is used from the following next pulse on, i.e. the user has the possibility to change the readout pattern in a dynamic fashion. In the current implementation the copy in progress time is not depending on the number of active channels, it was measured to be 14 µs .
If bit N of the register is set, channel N+1 is excluded from the copy process..
Example: If 0x5 is written to the copy disable register, the data of channel 1 and 3 are not copied into the FIFO.

7.5 FIFO (0x100-0x1FC)

The FIFO can be accessed from addresses 0x100 through 0x1FC to facilitate the readout with different types of CPUs. For masters with block transfer capability without address increment its most convenient to read all data from address 0x100. For masters with block transfer address auto increment it is straightforward to set up repeated block reads with a length of 256 Bytes (the maximum VME block transfer size) from address 0x100 (and the autoincrement uses the addresses 0x100 through 0x1FC for the transfer).
If FIFO test mode is enabled data can be written to the FIFOs addresses.

8 Broadcast Addressing

Broadcast addressing is an efficient way to issue the same command to a number of modules. It can be used in A24 and A32 mode on SIS360x/38xx boards. The higher address bits are used to define the broadcast class, the distinction of the modules is done via the A16 rotary switch and the A_11 jumper. If broadcast addressing is used, the A32_U, the A_32_L, the A24_U and the A24_L rotary switches must have the same setting in A32 mode, in A24 mode the A24_U and A24_L setting must be the same on all participating units. One of the participating units must be configured as broadcast handshake controller by setting bit 7 in the units control register. All of the participating units must have set bit 6 (enable broadcast) in the control register. The broadcast time jitter was measured to be less than 40 ns within a VME crate, i.e. you have the possibility issue commands under software control with a maximum uncertainty of 40 ns (like clear all counters), what sure is worse, than a hard wired front panel clear, but is much better than a VME single cycle loop over a number of units. The four broadcast commands are executed via the VME key addresses at offset 0x030 through 0x3C.

A32 Broadcast Example:
Let four SIS3805 participate by setting the A_32 jumper and setting the base address of the units to:

```
Unit 1: 0x32001000
Unit 2: 0x32001800
Unit 3: 0x32002000
Unit 4: 0x32002800
```

Switch on enable broadcast by setting bit 6 in the control register of the four units.
Enable broadcast handshake controller on unit 4 by setting bit 7 of its control register.
An A232 write to address 0x32000034 will issue one software next clock on units 1 through 4.

A24 Broadcast Example:

Let three SIS3805 participate by setting the A_24 jumper and setting the base address of the units to:

```
Unit 1: 0x541000
Unit 2: 0x542000
Unit 3: 0x543000
```

Switch on enable broadcast by setting bit 6 in the control register of the three units.
Enable broadcast handshake controller on unit 1 by setting bit 7 of its control register.
An A24 write to address 0x540030 will clear the counters, FIFOs and the logic on units 1 through 3.

9 VME Interrupts

Four VME interrupt sources are implemented in the SIS3805 firmware design:

- start of CIP
- FIFO half full
- FIFO almost full
- FIFO full (error condition)

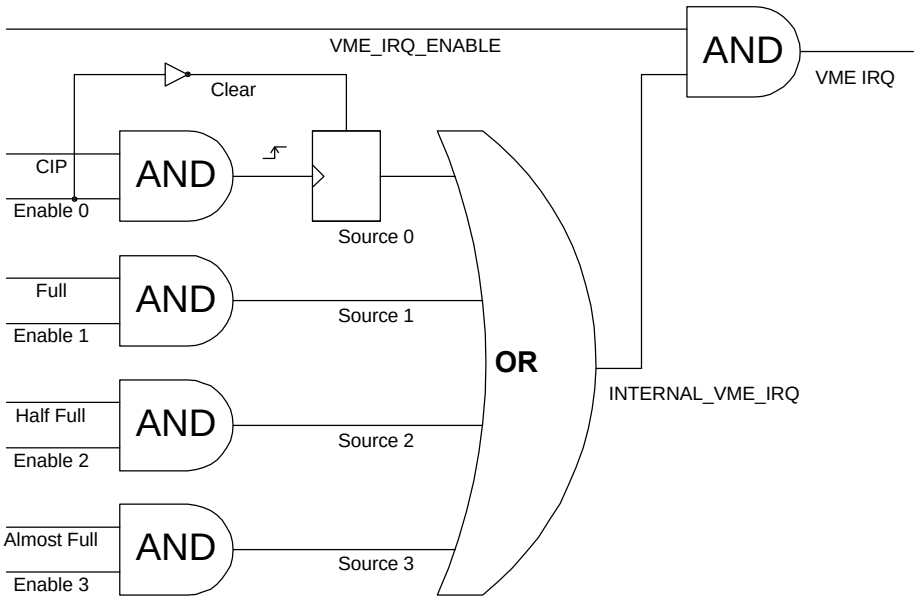
The interrupter is of type D8(O).

The interrupt logic is shown below. For VME interrupt generation the corresponding interrupt source has to be enabled by setting the respective bit in the VME control register (disabling is done with the sources J/K bit). Interrupt generation has to be enabled by setting bit 11 in the IRQ and version register. The internal VME interrupt flag can be used to check on an IRQ condition without actually making use of interrupts on the bus.

The VME interrupt level (1-7) is defined by bits 8 through 10, and the VME interrupt vector (0-255) by bits 0 through 7 of the VME IRQ and version register.

In general an interrupt condition is cleared by disabling the corresponding interrupt, clearing the interrupt condition (i.e. clear overflow) and enabling the IRQ again.

Note: In most cases your experiment may not require interrupt driven scaler readout, but the interrupt capability of the SIS3805 provides a way to overcome the problem of missing front panel inputs on most commercial VME CPUs.



10 Data Format

The data format of the actual counter values is described for D32 and 16 in this section.

Bit	Contents
U1	User Bit 1
U0	User Bit 0
B	Bank number (0/1 always 0 in version 2)
C4	Channel number Bit 4
C3	Channel number Bit 3
C2	Channel number Bit 2
C1	Channel number Bit 1
C0	Channel number Bit 0

10.1.1 D16

	high Byte								low Byte							
first read	0	0	B	C4	C3	C2	C1	C0	0	0	U1	U0	0	0	0	0
second read	Data Bits 47-40								Data Bits 39-24							
third read	Data Bits 31-24								Data Bits 23-16							
fourth read	Data Bits 15-8								Data Bits 7-0							

10.1.2 D32

first read																
0	0	B	C4	C3	C2	C1	C0	0	0	U1	U0	0	0	0	0	Data Bits 47-32
second read																
Data Bits 31-16																Data Bits 15-0

11 Input Configuration

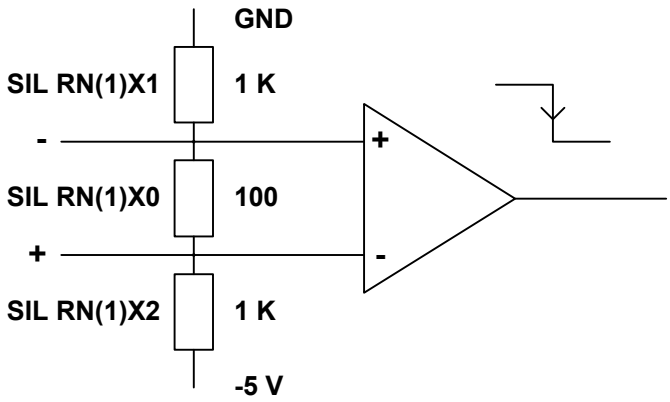
SIS36/38xx boards are available for NIM, TTL and ECL input levels and in LEMO and flat cable versions. The boards are factory configured for the specified input level and connector type, input termination is installed.

11.1 ECL

The 100 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

Network	Channels	1 K Networks
RN10	1-4	RN11/12
RN20	5-8	RN21/22
RN30	9-12	RN31/32
RN40	13-16	RN41/41
RN50	17-20	RN51/52
RN60	21-24	RN61/62
RN70	25-28	RN71/72
RN80	29-32	RN81/82
RN110	Control 1-4	RN111/RN112
RN120	Control 5-8	RN121/RN122

The schematics of the ECL input circuitry is shown below.

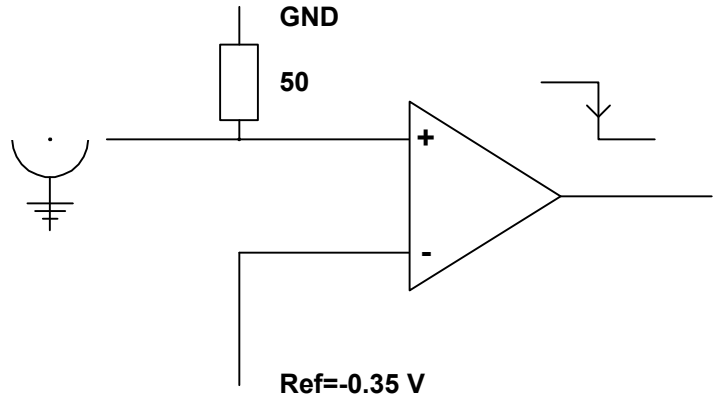


11.2 NIM

The 50 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

Network	Channels
U15 (Pins 10 to 6)	1-4
U15 (Pins 1 to 5)	5-8
U35 (Pins 10 to 6)	9-12
U35(Pins 1 to 5)	13-16
U55 (Pins 10 to 6)	17-20
U55 (Pins 1 to 5)	21-24
U75 (Pins 10 to 6)	25-28
U75 (Pins 1 to 5)	29-32
U115 (Pins 10 to 6)	Control 1-4
U115 (Pins 1 to 5)	Control 5-8

The schematics of the NIM input circuitry is shown below.

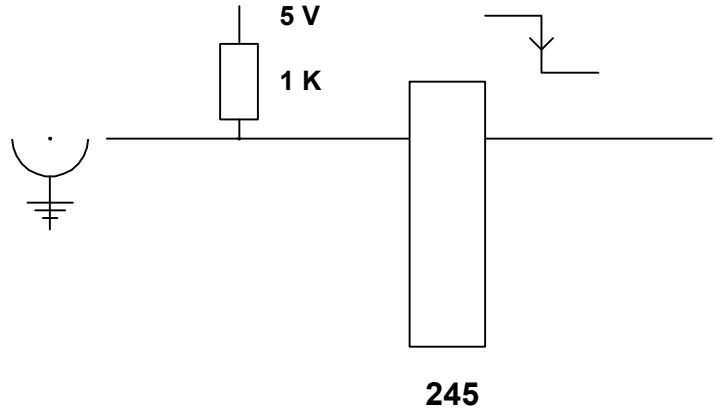


11.3 TTL

The TTL input level option is possible with LEMO and flat cable connectors.

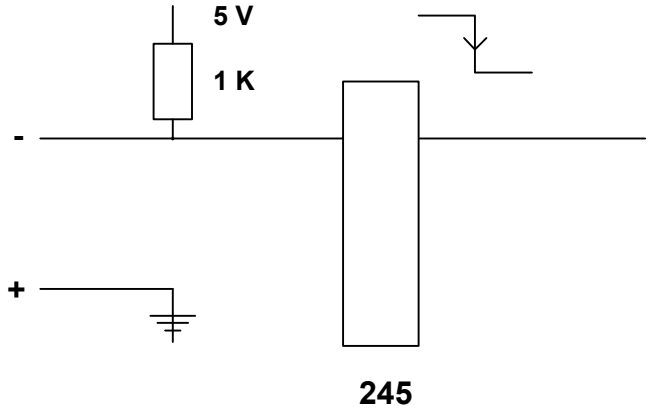
11.3.1 TTL/LEMO

The (low active) TTL/LEMO input circuitry is sketched below. A high active version can be implemented by replacing the 74F245 with a 74F640



11.3.2 TTL/Flat Cable

In the flat cable TTL version the positive (right hand side) of the connector is tied to ground.



12 Connector Specification

The four different types of front panel and VME connectors used on the SIS360x and SIS38xx boards are:

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
20 pin header	Control (flat cable versions)	DIN41651 20 Pin (AMP e.g.)
34 pin header	Inputs (flat cable versions)	DIN41651 34 Pin (AMP e.g.)
LEMO	Control and Input (LEMO versions)	LEMO ERN.00.250.CTL

13 Control Input Modes

The assignment of the control inputs can be defined via the input mode bits in the control register. Inputs

Control Input Modes

Mode 0 (bit1=0, bit0=0):	input 1 -> external next pulse input 2 -> external user bit 1 input 3 -> external user bit 2 input 4 -> FIFO reset and counter clear
Mode 1 (bit1=0, bit0=1):	input 1 -> external next pulse input 2 -> external user bit 1 input 3 -> disable counting input 4 -> FIFO reset and counter clear
Mode 2 (bit1=1, bit0=0):	input 1 -> external next pulse input 2 -> external user bit 1 input 3 -> external user bit 2 input 4 -> disable counting
Mode 3 (bit1=1, bit0=1):	input 4 -> external test

13.1 Outputs

Four ouput signals are defined on the SIS3805 board. They are copy in progress (CIP), FIFO empty, FIFO half full and FIFO full (ERROR). Their assignments to the control lines are listed in the table below.

Signal	Control Signal
CIP	5
FIFO empty	6
FIFO half full	7
FIFO full	8

14 Signal Specification

14.1 Control Signals

The width of the clear and external next pulse has to be greater or equal 10 ns, an external inhibit (disable counting) has to be present for the period you desire to disable counting. An internal delay of some 15 ns has to be taken into account for all external signals.

14.2 Inputs

The SIS3805 is specified for counting rates of 200 MHz for ECL and NIM signals and 100 MHz for the TTL case. Thus the minimum high and low level duration is 2.5 ns (5 ns respective). Signal deterioration over long cables has to be taken into account.

14.3 User Bits

The status of the user bits (Version 2) is latched with the leading edge of the external next pulse. A setup time of greater equal 10 ns and a hold time of 25 ns is required, i.e..the signal should have a length of greater 35 ns and has to be valid 10 ns before the leading edge of the next clock pulse arrives.

15 Operating conditions

15.1 Power Consumption/Voltage requirement

Although the SIS3805 is prepared for a number of VIPA features, it was decided to use an ob board DC/DC converter to generate the –5 V, which are needed for driver and receiver chips, to allow for the use of the module in all 6U VME environments. The power consumption is counting rate dependent, it varies from the idle value of +5 V 3,3 A to +5 V 4,5 A with all channels counting at 200 MHz(i.e. the power consumption is < 23 W).

15.2 Cooling

Forced air flow is required for the operation of the SIS3805 board.

15.3 Insertion/Removal

Please note, that the VME standard does not support live insertion (hot swap). Hence crate power has to be turned off for installation and removal of SIS3805 scalers.
The leading pins on the SIS3805 VME64x VME connectors and connected on board circuitry are designed for hot swap in conjunction with a VME64x backplane (a VME64x backplane can be recognised by the 5 row VME connectors, while the standard VME backplane has three row connectors only).

16 Test

The SIS380x scaler series provides the user with a number of test features, which allow for debugging of the unit as well as for overall system setups.

16.1 LED (selftest)

During power up self test and LCA configuration all LEDs except the Ready (R) LED are on. After the initialisation phase is completed, all LEDs except the Ready (R) LED and the Power (P) have to go off. Differing behaviour indicates either a problem with the download of the firmware boot file or one or more LCA and/or the download logic.

16.2 Internal pulser tests

16.2.1 Single Pulse

A single pulse into all channels can be generated with a write to the key address 0x68 if test mode is enabled via the control register. In conjunction with the count enable register more complex count patterns, like increment patterns e.g., can be generated before readout.

16.2.2 25 MHz Pulser

Simultaneous pulsing at 25 MHz into all channels can be used to test the complete readout chain and internal counter logic of the SIS3801. The feature is activated by enabling input test mode and 25 MHz test pulses via the corresponding bits in the control register.
The 25 MHz test pulser gives easy access to your VME CPUs readout timing. By making subsequent reads to the same counter and multiplying the difference in counts with 40 ns you can measure the single word access time.

16.3 Signal-Input Priority

If the user happens to enable more than one input option (enable test mode, enable reference pulser, scaler enable) at the same time, the priority is as show in the table below:

Priority	Feature
1	Test mode
2	Front Panel Inputs

Example: If test mode and front panel inputs are enabled at the same time, the channels will count test pulses (i.e. will count synchronous with the test pulser).

16.4 FIFO Test

FIFO tests via the VME bus are helpful to debug the FIFO on the SIS38xx in case of spurious data and to debug an overall VME system with driver problems on the CPU side or flaky VME termination e.g.. In FIFO test mode the user can write defined data into the units FIFO via the VME bus and to compare them wit the read back result.
FIFO test mode is enabled by setting bit one of the control register and disabled by setting bit 9 of the control register. With FIFO test mode enabled data can be written to the FIFO at the address offset +0x100 (through 0x1FC). Writing to the location with FIFO mode

17 Software Support

VME multiscaler boards are tested at SIS with an OR VP6 VME CPU (Pentium II based) under Windows 95 and a National Instruments CVI user interface. The actual VME C code makes use of the OR Windows 95 DLL, which has straightforward to read and understand routines like:

```
VMEA24StdWriteWord(a32address + KEY_RESET, 0x0);   /* Key Reset */
rdata = VMEA24StdReadWord(a32address + STAT_REG);
```

In most cases the user setup will be using different hardware, a full fleshed real time operating system like VxWorks, and a different user interface. We still believe, that it is helpful to have a look at the code which is used to test the units and to take it as an example for the implementation of the actual scaler readout application. A floppy with our test software is enclosed with SIS3805 shipments.
Depending on the user feedback and co-operation we expect, that we will have drivers or at least example routines for the commonly used VME CPU operating systems at hand in the mid term.

17.1 Contents of the included Floppy

The Floppy contains a readme.txt file with the most up to date information, the CVI project file and all home made files from the project. The important part of the code for the implementation of your own program is sitting in the CVI call back routines.

18 Appendix

18.1 Address Modifier Overview

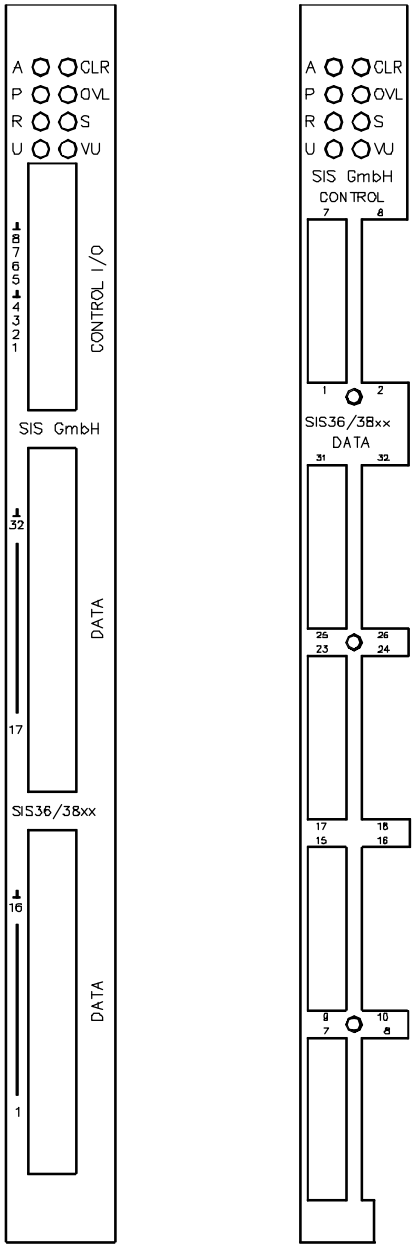
Find below the table of address modifiers, which can be used with the SIS360x/38xx (with the corresponding addressing mode enabled).

AM code	Mode
0x3F	A24 supervisory block transfer (BLT)
0x3D	A24 supervisory data access
0x3B	A24 non-privileged block transfer (BLT)
0x39	A24 non-privileged data access
0x2D	A16 supervisory access
0x29	A16 non-privileged access
0x0F	A32 supervisory block transfer (BLT)
0x0D	A32 supervisory data access
0x0B	A32 non-privileged block transfer (BLT)
0x09	A32 non privileged data access
	Future option: CBLT

18.2 Front Panel Layout

The front panel of the SIS3805 is equipped with 8 LEDs, 8 control in- and outputs and 32 counter inputs. On flat cable units (ECL and TTL) the control connector is a 20 pin header flat cable connector and the channel inputs are fed via two 34-pin headers. On LEMO (NIM and TTL) units the control in- and outputs are grouped to one 8 channel block and the counter inputs are grouped into 2 blocks of 16 channels. The units are 4 TE (one VME slot) wide, the front panel is of EMC shielding type. VIPA extractor handles are available on request or can be retrofitted by the user, if he wants to change to a VIPA crate at a later point in time.
In the drawing below you can find the flat cable (left hand side) and Lemo front panel layouts.

Note: Only the aluminium portion without the extractor handle mounting fixtures is shown



18.3 List of Jumpers

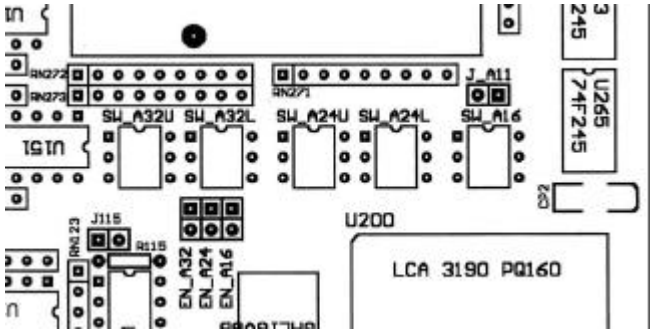
Find below a list of the jumpers and jumper arrays.

Jumper Name	Array/Single	Function
J101	Single	Input Termination Control Input 1
J102	Single	Input Termination Control Input 2
J103	Single	Input Termination Control Input 3
J104	Single	Input Termination Control Input 4
J105	Single	Input Termination Control Input 5
J106	Single	Input Termination Control Input 6
J107	Single	Input Termination Control Input 7
J108	Single	Input Termination Control Input 8
J115	Single	Level Configuration (not for end user)
J500	Array	Boot File Selection
J520	Single	VME SYSRESET Behaviour
EN_A16	Single	Enable A16 addressing
EN_A24	Single	Enable A24 addressing
EN_A32	Single	Enable A32 addressing
J_A11	Single	Address Bit 11 Selection

18.4 Jumper and rotary switch locations

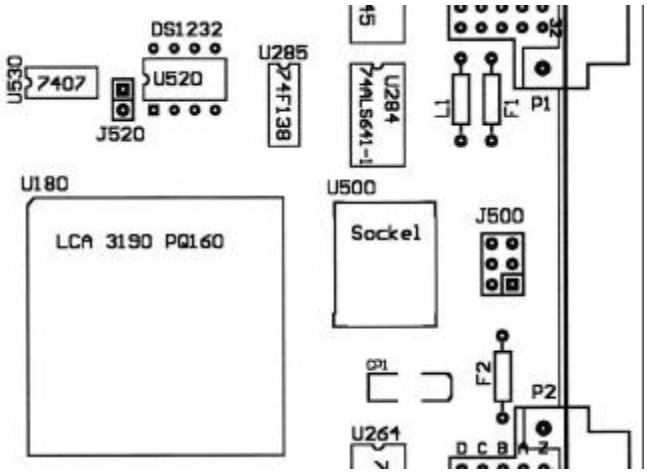
18.4.1 Addressing mode and base address selection

The EN_A32, EN_A24, EN_A16, A_11 and the 5 rotary switches are located int the middle of the upper section of the board close to the DC/DC converter, the corresponding section of the PCB is shown below.

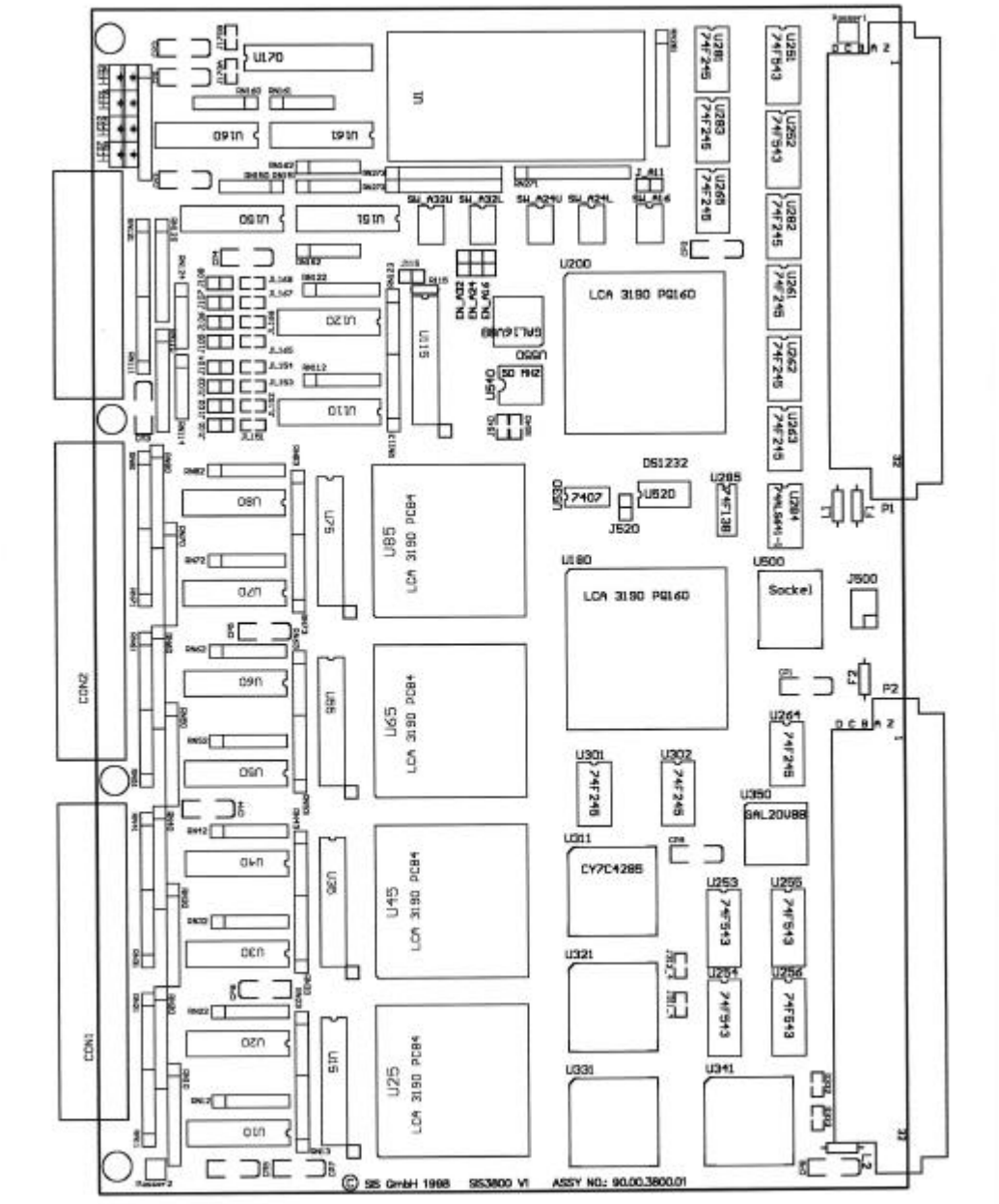


18.4.2 J500 (Bootfile Selection) and J520 (SYSRESET Behaviour)

The jumper array J500 is located between the P1 and the P2 connector. An open position in J500 defines a one (see also chapter 4), the lowest bit is next to the P2 connector.. J520 is located to the left of J500 and closer to the DC-DC converter. With jumper J520 closed the SIS3805 executes a key reset upon the VME SYSRESET signal. The section of the board with the jumper array and the SYSRESET jumper is shown below.



18.5 Board Layout



18.6 Cascaded FIFOs

The SIS3805 board can be stuffed with one or four synchronous FIFO chips, the standard unit comes with one FIFO chip (the V2 board has one 64 K chip as default, and 256 K as option). The FIFO flags are handled by a GAL, which is in the vicinity of the FIFO pads and the actual FIFO flag implementation for cascaded FIFOs will be described here in a later version of the manual.

18.7 FLASHPROM Versions

A list of available FLASHPROMs can be obtained from http://www.struck.de/sis3638firm.htm. Please note, that a special hardware configuration may be necessary for the firmware design of interest (the SIS3801 design requires the installation of a FIFO e.g.).
The table on the web is of the format shown below:

SIS36/38xx FLASHPROM table

Design Name	Design	Boot File (s)
SIS3800_201098	0	SIS3800 Version 1
SIS3801_201098	0	SIS3800 Version 1
	1	SIS3800 Version 2
	2	SIS3801 Version 1 (32-bit Design)
	3	SIS3801 Version 2 (24-bit Design)
SIS3803_280798	0	SIS3803 Version 1
SIS3805_301098	0	SIS3805 Version 1 (48-bit 2 bank design)
	1	SIS3805 Version 2 (48-bit shadow design)
	2	SIS3801 Version 1 (32-bit Design)
	3	SIS3801 Version 2 (24-bit Design)

18.8 Row d and z Pin Assignments

The SIS3805 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

18.9 Geographical Address Pin Assignments

The SIS38xx board series is prepared for geographical addressing via the geographical address pins GA0*, GA1*, GA2*, GA3*, GA4* and GAP*. The address pins are left open or tied to ground by the backplane as listed in the following table:

Slot Number	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

18.10 Additional Information on VME

The VME bus has become a popular platform for many realtime applications over the last decade. Information on VME can be obtained in printed form, via the web or from newsgroups. Among the sources are the VMEbus handbook, http://www.vita.com (the home page of the VME international trade association (VITA)) and comp.bus.arch.vmebus. In addition you will find useful links on many high energy physics labs like CERN or FNAL

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