SIS3600
VME Multi Event Latch

User Manual

SIS GmbH
Harksheiderstr.102A
22399 Hamburg
Germany

Phone: ++49 (0) 40 60 87 305 0
Fax: ++49 (0) 40 60 87 305 20

email: info@struck.de
http://www.struck.de

Version: sis3600-M-0-1-v126 as of 17.07.07

Revision Table:

Revision	Date	Modification
1.0		Generation
1.1	08.12.98	fast clear
1.11	06.07.99	revision table bug fix in output mode table
1.12	08.07.99	coincidence mode input timing bug fix in coincidence mode timing diagram
1.13	25.10.99	bug fix in default settings of control register
1.20	01.02.01	Firmware Version 2, no Broadcast functionality, CBLT style data readout
1.21	02.02.01	CBLT hints added
1.22	14.06.02	Bug fix in input/output section
1.23	24.11.03	Bug fix, fast clear register is write only
1.24	08.01.04	Remove D16 in FIFO read access
1.25	16.02.06	ESD note added Minimum LNE length increased to 25ns (from 10 ns)
1.26	17.07.07	Enable external next added to getting started sequence

1 Table of contents

2 Introduction

The SIS3600 is the multi event latch of the SIS360x/38xx VME board family. It can be operated in strobed or coincidence mode. One can also refer to the unit as 32-bit pattern unit. The SIS3600 is a single width (4 TE) 6U (double euro form factor) card. It was designed to capture the status of the outputs of discriminators or other front end electronics. An other application is the high speed readout of position or angular encoders, as no slow serial protocol like SSI (serial synchronous interface) is involved. Due to the fast OR output the unit can be used for the generation of higher level trigger decisions. A fast clear window allows the use of the latch in conjunction with 2nd level trigger electronics. Another application of the module comprises the acquisition of TTL, NIM or ECL data streams with some 20 MB/s. Due the FIFO architecture with up to 128 K longwords the following transfer to the system controller is decoupled from the incoming data stream.
This document was written with the focus on the user of the unit, who wants to integrate the board into a data acquisition system and interested parties who consider the module for future use in their setup and would like to get an overview on the designs capabilities.
The SIS360x/38xx card is a flexible concept to implement a variety of latch and counter firmware designs. The flexibility is based on two to six Xilinx FPGAs in conjunction with a FLASHPROM from which the firmware files are loaded into the FPGAs. Depending on the stuffing options of the printed circuit board, the user has the possibility to cover several purposes with the same card, hence the manual is a combination of firmware and hardware description .
All cards of the family are equipped with the 5 row VME64x VME connectors, a side cover and EMC front panel, as well as the VIPA LED set. For users with VME64xP subracks VIPA extractor handles can be installed. The base board is prepared for VIPA style addressing, the current first version of the SIS3600 firmware does not feature VIPA modes yet however.
As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm. A list of available firmware designs can be retrieved from http://www.struck.de/sis3638firm.htm

3 Technical Properties/Features

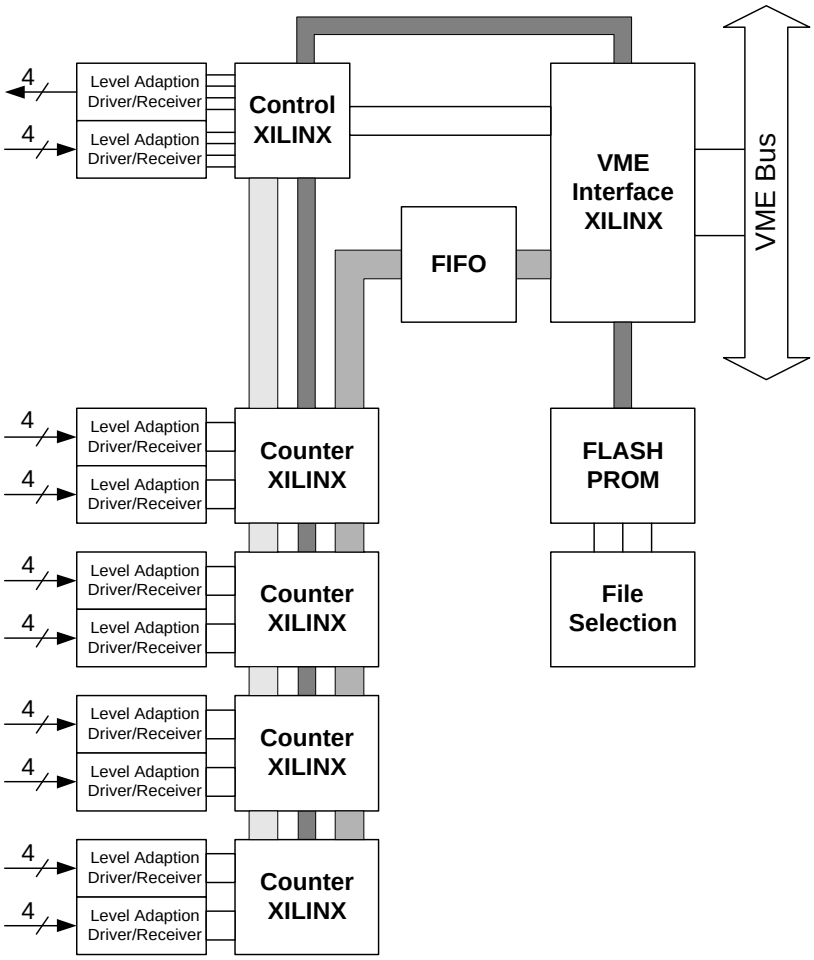
The SIS3600 is rather a firmware design in combination with given board stuffing options, than a name for the board (this is the reason, why the modules are named SIS360x/38xx on the front panel and the distinction of the units is made by the module identifier register). The firmware makes use of part of the possibilities of the SIS360x/38xx PCB, if the SIS3600 or other firmware designs of the family come close to what you need, but something is missing, a custom firmware design may be an option to consider.

Find below a list of key features of the SIS3600.

- 32-bit
- NIM/TTL/ECL versions
- flat cable (TTL/ECL) and LEMO (TTL/NIM) versions
- 64K (32K Event) FIFO (256K available on request)
- A16/A24/A32 D16/D32/BLT32 (CBLT32 with firmware version 2)
- broadcast functionality (with firmware version 1)
- user output bit
- fast OR output
- fast clear
- Base address settable via 5 rotary switches (A32-A12) and one jumper (A11)
- VME interrupt capability
- VIPA geographical addressing prepared
- VIPA LED set
- 100 ns minimum cycle time
- Pulser capability
- Up to eight firmware files
- single supply (+5 V)

3.1 Board Layout

Xilinx FPGAs are the working horses of the SIS360x/38xx board series. The counter (prescaler, latch, ...) logic is implemented in one to four chips, each chip handles eight front end channels. The VME interface and the input and output control logic reside in two Xilinx chips also. The actual firmware is loaded into the FPGAs upon power up from a FLASHPROM under jumper control. The user can select among up to eight different boot files by the means of a 3-bit jumper array. The counter inputs, the control inputs and the outputs can be factory configured for ECL, NIM and TTL levels. The front panel is available as flat cable (ECL and TTL) or LEMO (NIM and TTL) version. The board layout is illustrated with the block diagram below:



SIS3600 Block Diagram

3.2 Design and Modus Operandi

The latches are implemented in XILINX FPGAs. One of the latch FPGAs holds 8 channels (bits). The multi event capability is achieved with a FIFO. Data are copied from the frontend latch chips to the FIFO and can be read via the VMEBus asynchronous. The duration of the frontend to FIFO copy process is available on the Copy In Progress (CIP) front panel output for synchronisation of external hardware. The CIP signal allows the user also to check the minimum possible gap between two consecutive events, this was measured to be some 100 ns. If fast clear is enabled via the control register, data are copied to the FIFO if no external fast clear signal arrives within the programmed fast clear window, events with fast clear are skipped.

A side effect of the short copy to FIFO time is, that the SIS3600 latch can be used as a FIFO between ECL data streams and the VMEbus with input data rates in excess of 30MB/s in applications where no event structure or special requirements like the presence of an independent DSP readout bus are required.

3.3 Readout Considerations

One of the major advantages of a FIFO based latch is the decoupling of the front end readout and the actual VME readout of the data. Depending on the application the FIFO may be used to buffer one or two reads only, before a DSP processes the data on the fly, in this case the FIFO is used to establish readout pipelining, in other cases the maximum possible FIFO size is of interest to store a complete set of data points for a pulsed or non continuous measurement. Continuous readout can be established as long as the VME master can cope with the amount of data generated by the latch, i.e. the FIFO is never allowed to run into the FIFO full condition. The 64K default FIFO size of the SIS3600 is considered to be a save value for most applications, for more demanding applications the FIFO size can be increased to 256K. One as to keep in mind, that two FIFO words are needed to hold one 32-bit latch value, i.e. a 64K FIFO can hold 32K latch words (or events). The packing of the FIFO data into VME D32 words is handled without user intervention upon VME read cycles from the FIFO. In high data rate applications, the readout scheme will make use of the FIFO half full flag via a VME interrupt or polling in most cases, as a minimum known number of 32K longwords can be read out (being blocked into smaller chunks by VME) with a block transfer.
Example: Assume the latch is read out with a frequency of 1 MHz, the data rate is 4 MB/s and the FIFO half full interrupt or flag will be asserted for the first time after some 15 ms of data acquisition and the VME master has to digest 64Kbytes within less than 15 ms (including IRQ handling or polling) to prevent the FIFO from overflow.
Note: No new data can be acquired before a FIFO reset if the FIFO full condition has occurred (i.e. the FIFO full condition is considered an error condition, which should not occur in standard operation).

4 Getting Started

The minimum setup to operate the SIS3600 in strobed mode without the use of the fast clear capability requires the following steps:

- Check the proper firmware design is selected (should be design zero, i.e. all jumpers of jumper array J500 set.
- Select the VME base address for the desired addressing mode
- Select the VME SYSRESET behaviour via J520
- turn the VME crate power off
- install the latch in the VME crate
- connect your signals to the latch
- turn crate power back on
- issue a key reset by writing to 0x60
- issue FIFO clear by writing to 0x20
- configure CBLT setup register as needed (firmware version 2 only)
- enable next logic by writing to 0x28
- set bit 16 of control register 0x0 to enable external LNE pulses
- issue first next clock pulse to start counting by soft- or hardware
- after one or more subsequent next clock pulses data can be read from the FIFO from the addresses 0x100 through 0x1FC.

A good way of checking first time communication with the SIS3600 consists of switching on the user LED by a write to the control register at offset address 0x0 with data word 0x1 (the LED can be switched back off by writing 0x100 to the control register)..

4.1 Factory Default Settings

4.1.1 Adressing

SIS3600 boards are shipped with the En_A32, the En_A24 and the En_A16 jumpers installed and the rotary switches set to:

Switch	SW_A32U	SW_A32L	SW_A24U	SW_A24L	SW_A16	J A_11	Bits 7-4	Bits 3-0
Setting	3	8	3	8	3	8	0	0

Jumper A_11 is open (bit 11 set).
Hence the unit will respond to the following base addresses:

Mode	Base address
A32	0x38383800
A24	0x383800
A16	0x3800

4.1.2 Firmware Design

Design 0 (SIS3600, Version 1) of the FLASHPROM is selected (all jumpers of jumper array J500 closed).

4.1.3 System Reset Behaviour

J520 is set, i.e. the SIS3600 is reset upon VME reset.

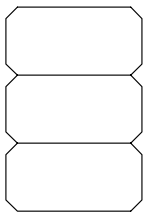
5 Firmware Selection

The FLASH PROM of a SIS360x/38xx board can contain several boot files. A list of available FLASHPROM versions can be found on our web site http://www.struck.de in the manuals page. If your FLASHPROM has more than one firmware design, you can select the desired firmware via the firmware selection jumper array J500 . You have to make sure, that the input/output configuration and FIFO configuration of your board are in compliance with the requirements of the selected firmware design (a base board without FIFO can not be operated as multi channel scaler e.g.). A total of 8 boot files from the FLASHPROM can be selected via the three bits of the jumper array. The array is located towards the rear of the card between the VME P1 and P2 connectors. The lowest bit sits towards the bottom of the card, a closed jumper represents a zero, an open jumper a one.

5.1 Examples

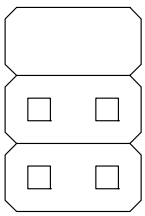
The figures below show jumper array 500 with the soldering side of the board facing the user and the VME connectors pointing to the right hand side.

Bootfile 0 selected



With all jumpers closed boot file 0 is selected

Bootfile 3 selected



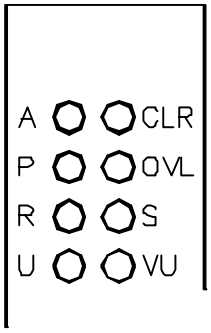
With the lowest two jumpers open bit 0 and bit 1 are set to 1 and hence boot file 3 is selected

Front Panel LEDs

The SIS3600 has 8 front panel LEDs to visualise part of the units status. Three LEDs according to the VME64xP standard (Power, Access and Ready) plus 5 additional LEDs.

Designation	LED	Color	Function with SIS3600 design
A	Access	yellow	Signals VME access to the unit
P	Power	red	Flags presence of VME power
R	Ready	green	Signals configured logic
U	VME user LED	green	To be switched on/off under user program control
CLR		yellow	Fast clear
OVL (CIP)	Copy in Progress	red	Signals copy in progress
S		green	Enabled
VU	VIPA user LED	green	for future use

The LED locations are shown in the portion of the front panel drawing below.



The VME Access, the Clear LED are monostable (i.e. the duration of the on phase is stretched for better visibility), the other LEDs reflect the current status.
An LED test cycle is performed upon power up (refer to chapter 16.1).

6 VME addressing

6.1 Address Space

As bit 11 is the lowest settable bit on the 360x/38xx board, an address space of 2 Kbytes (Offset plus 0x000 to 0x7ff) is occupied by the module.

6.2 Base Address

6.2.1 VME

The VME addressing mode (A16/A24/A32) is selected via the jumpers EN_A16, EN_A24 and EN_A32.The mode is selected by closing the corresponding jumper, it is possible to enable two or all three addressing modes simultaneously.
The base address is set via the five rotary switches SW_A32U, SW_A32L, SW_A24U, SW_A24L and SW_A16 and the jumper J_A11. The table below lists the switches and jumpers and their corresponding address bits.

Switch/Jumper	Affected Bits
SW_A32U	31-28
SW_A32L	27-24
SW_A24U	23-20
SW_A24L	19-16
SW_A16	15-12
J_A11	11

In the table below you can see, which jumpers and switches are used for address decoding in the three different addressing modes (fields marked with an x are used).

	SW_A32U	SW_A32L	SW_A24U	SW_A24L	SW_A16	J_A11
A32	x	x	x	x	x	x
A24			x	x	x	x
A16					x	x

Note: J_A11 closed represents a 0, J_A11 open a one

6.2.2 VIPA/VME64x

As the VME64x and the VME64xP (VIPA) standard are not yet standards to refer to and to declare conformity with, addressing modes (like geographical addressing e.g.) according to these standards are prepared but not yet implemented in the current firmware revisions.

6.3 Address Map

The SIS360x/38xx boards are operated via VME registers, VME key addresses and the FIFO (where installed). The following table gives an overview on all SIS3600 addresses and their offset from the base address, a closer description of the registers and their function is given in the following subsections.
Part of the addresses are present in firmware version 1 or 2 only, access to the address with the wrong firmware loaded will result in a bus error.

Offset	Key	Access	Type	Function
0x000		R/W	D16/D32	Control and Status register
0x004		R/W	D16/D32	Module Identification and IRQ control register
0x008		W	D16/D32	8-bit fast clear window value
0x00C		W	D16/D32	Output pulse frequency register
0x010		W	D16/D32	Write to FIFO (in FIFO test mode)
0x020	KA	W	D16/D32	clear FIFO and logic
0x024	KA	W	D16/D32	VME next clock
0x028	KA	W	D16/D32	Enable next clock logic
0x02C	KA	W	D16/D32	Disable next clock logic
0x030	KA	W	D16/D32	Broadcast, clear FIFO and logic (Version 1 only)
0x034	KA	W	D16/D32	Broadcast; VME next clock (Version 1 only)
0x038	KA	W	D16/D32	Broadcast; Enable next clock logic (Version 1 only)
0x03C	KA	W	D16/D32	Broadcast; Disable next clock logic (Version 1 only)
0x050	KA	W	D16/D32	Enable fast clear
0x054	KA	W	D16/D32	Disable fast clear
0x060	KA	W	D16/D32	reset register (global reset)
0x068	KA	W	D16/D32	Generate one output pulse
0x080		R/W	D16/D32	CBLT setup register (Version 2 only)
0x100-0x1FC		R	D32/BLT32	read FIFO

Note: D08 is not supported by the SIS360x/38xx boards

The shorthand KA stands for key address. Write access with arbitrary data to a key address initiates the specified function

7 Register Description

7.1 Status Register (0x0)

The status register reflects the current settings of most of the SIS3801 parameters in read access, in write access it functions as the control register.

Bit	Function
31	Status VME IRQ source 3 (FIFO full)
30	Status VME IRQ source 2 (FIFO half full)
29	Status VME IRQ source 1 (FIFO almost empty)
28	Status VME IRQ source 0 (start of CIP)
27	VME IRQ
26	internal VME IRQ
25	0
24	0
23	Status VME IRQ Enable Bit Source 3
22	Status VME IRQ Enable Bit Source 2
21	Status VME IRQ Enable Bit Source 1
20	Status VME IRQ Enable Bit Source 0
19	Status coincidence mode (0=strobed, 1=coincidence)
18	Status latch gate
17	Status enable external clear
16	Status enable external next
15	Status Enable next logic
14	Status fast clear (0=fast clear disabled, 1=fast clear enabled)
13	0
12	FIFO flag full
11	FIFO flag almost full0
10	FIFO flag half full
9	FIFO flag almost empty
8	FIFO flag empty
7	Status broadcast mode handshake controller
6	Status broadcast mode
5	Status pipe mode
4	Status enable output pulses
3	Status output mode bit 1
2	Status output mode bit 0
1	Status FIFO test mode
0	Status user LED/user output

The reading of the status register after power up or key reset is 0x300 (see default settings of control register).

7.2 Control Register (0x0)

The control register is in charge of the control of most of the basic properties of the SIS3600 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which has a different location within the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

Bit	Function
31	disable IRQ source 3 (*)
30	disable IRQ source 2 (*)
29	disable IRQ source 1 (*)
28	disable IRQ source 0 (*)
27	clear coincidence mode (*)
26	clear latch gate (*)
25	disable external clear (*)
24	disable external next (*)
23	enable IRQ source 3
22	enable IRQ source 2
21	enable IRQ source 1
20	enable IRQ source 0
19	set coincidence mode
18	set latch gate
17	enable external clear
16	enable external next
15	disable broadcast mode handshake controller (*)
14	disable broadcast mode (*)
13	disable pipeline mode (*) (see note below table also)
12	disable output pulses (*)
11	clear output mode bit 1 (*)
10	clear output mode bit 0 (*)
9	disable FIFO test mode
8	switch off user LED (and user output with output mode=2) (*)
7	enable handshake controller for broadcast mode
6	enable broadcast mode
5	enable pipeline mode (see note below table also)
4	enable output pulses
3	set output mode bit 1
2	set output mode bit 0
1	enable FIFO test mode
0	switch on user LED (and user output with output mode=2)

(*) denotes the default power up or key reset state

Note 1: Pipeline mode was established to facilitate the use of the SIS3600 in conjunction with SIS38xx multiscalers. As the first next pulse on a SIS multiscaler does not result in a readout, but in the start of the counting process, pipeline mode can be activated on the SIS3600 latch to achieve the same behaviour.
Note 2: set latch gate defines a software gate, which will not be reset until cleared with clear latch gate (i.e. a unit will record all leading edges in coincidence mode, no matter, what LNE length is present).

7.3 Module Identification and IRQ control register (0x4)

This register has two basic functions. The first is to give information on the active firmware design. This function is implemented via the read only upper 20 bits of the register. Bits 16-31 hold the four digits of the SIS module number (like 3801 or 3600 e.g.), bits 12-15 hold the version number. The version number allows a distinction between different implementations of the same module number, the SIS3801 for example has the 24-bit mode with user bits and the straight 32-bit mode as versions.

Bit	Read/Write access	Function	
31	read only	Module Identification Bit 15	Module Id Digit 3
30	read only	Module Identification Bit 14	
29	read only	Module Identification Bit 13	
28	read only	Module Identification Bit 12	
27	Read only	Module Identification Bit 11	Module Id Digit 2
26	read only	Module Identification Bit 10	
25	read only	Module Identification Bit 9	
24	read only	Module Identification Bit 8	
23	read only	Module Identification Bit 7	Module Id Digit 1
22	read only	Module Identification Bit 6	
21	read only	Module Identification Bit 5	
20	read only	Module Identification Bit 4	
19	read only	Module Identification Bit 3	Module Id Digit 0
18	read only	Module Identification Bit 2	
17	read only	Module Identification Bit 1	
16	read only	Module Identification Bit 0	
15	read only	Version Bit 3	
14	read only	Version Bit 2	
13	read only	Version Bit 1	
12	read only	Version Bit 0	
11	read/write	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	
10	read/write	VME IRQ Level Bit 2	
9	read/write	VME IRQ Level Bit 1	
8	read/write	VME IRQ Level Bit 0	
7	read/write	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	
6	read/write	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	
5	read/write	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	
4	read/write	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	
3	read/write	IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle	
2	read/write	IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle	
1	read/write	IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle	
0	read/write	IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle	

The second function of the register is interrupt control. The interrupter type of the SIS3600 is D08(O) . Via bits 0-7 of the module identifier and interrupt control register you can define the interrupt vector, which is placed on the VME bus during the interrupt acknowledge cycle. Bits 8 through 10 define the VME interrupt level, bit 11 is used to enable (bit set to 1) or disable (bit set to 0) interrupting.

Module identification and version example:
The register for a SIS3801 in straight 32-bit mode (version 1) reads 0x38011nnn, for a SIS3801 in 24-bit mode (version 2) it reads 0x38012nnn. (the status of the lower 3 nibbles is denoted with n in the example).

7.4 Fast Clear Window register 0x8

The 8-bit value, which is stored/written to the lowest 8-bits of this register defines the width of the fast clear window (FCW) if fast clear is enabled.
The length of the FCW is defined by:

FCW = (8-bit register value +1) x 100 ns + 120 ns

Hence the maximum length of the fast clear window is some 25 µs.
Events with a leading edge of the fast clear pulse inside of the fast clear window are not copied to the FIFO (i.e. are discarded). The fast clear is armed in the region from 65 to 85 ns after the leading edge of the next signal, for safe operation it is recommended to time the fast clear in a way, that it is arriving 85 ns or more after the next signal (what will be the case with typical trigger logic anyway).

7.5 Frequency register 0xC

Depending on the output mode the SIS3600 has up to four outputs which are driven from an internal pulser. These outputs can be routed to the external next input of the unit and additional external units like multiscalers or a readout controller to define the heartbeat of the setup. The frequency register is a 24-bit write only register and it actually defines the ouput pulse interval in steps of 100 ns. A setting of zero corresponds to a pulse gap of 100 ns (i.e. a frequency of 10 MHz), the maximum setting of 0xFFFFFF corresponds to a pulse spacing of some 1.68 s. The width of the output pulse has a constant value of 50 ns.

Pulse spacing = (24-bit register value +1) x 100 ns
Pulse width = 50 ns

7.6 CBLT setup register 0x80 (R/W)

This register defines, whether the SIS3811 will participate in a CBLT. The configuration of this register and the registers of other participating modules is essential for proper CBLT behaviour.

Bit	Function
31	CBLT address bit 31
30	CBLT address bit 30
29	CBLT address bit 29
28	CBLT address bit 28
27	CBLT address bit 27
26	CBLT address bit 26
25	CBLT address bit 25
24	CBLT address bit 24
23	0
22	0
21	0
20	0
19	0
18	0
17	0
16	0
15	Geographical address bit 4
14	Geographical address bit 3
13	Geographical address bit 2
12	Geographical address bit 1
11	Geographical address bit 0
10	0
9	0
8	0
7	0
6	0
5	0
4	0
3	0
2	First (to be set to 1 on the first module in the CBLT chain)
1	Last (to be set to 1 on the last module in the CBLT chain)
0	enable CBLT (to be set to 1 on all modules in the CBLT chain)

The function/meaning of the CBLT and the geographical address is illustrated in section. 18.6.1.

7.7 FIFO (0x100-0x1FC)

The FIFO can be accessed from addresses 0x100 through 0x1FC to facilitate the readout with different types of CPUs. For masters with block transfer capability without address increment its most convenient to read all data from address 0x100. For masters with block transfer address auto increment it is straightforward to set up repeated block reads with a length of 256 Bytes (the maximum VME block transfer size) from address 0x100 (and the autoincrement uses the addresses 0x100 through 0x1FC for the transfer).
If FIFO test mode is enabled data can be written to the FIFOs addresses. FIFO test mode is a good method to test the integrity of the FIFO as well as the complete VME readout chain including master and slave drivers and receivers and the VME backplane.

8 Broadcast Addressing (version 1 only)

Broadcast addressing is an efficient way to issue the same command to a number of modules. It can be used in A24 and A32 mode on SIS360x/38xx boards. The higher address bits are used to define the broadcast class, the distinction of the modules is done via the A16 rotary switch and the A_11 jumper. If broadcast addressing is used, the A32_U, the A_32_L, the A24_U and the A24_L rotary switches must have the same setting in A32 mode, in A24 mode the A24_U and A24_L setting must be the same on all participating units. One of the participating units must be configured as broadcast handshake controller by setting bit 7 in the units control register. All of the participating units must have set bit 6 (enable broadcast) in the control register. The broadcast time jitter was measured to be less than 40 ns within a VME crate, i.e. you have the possibility issue commands under software control with a maximum uncertainty of 40 ns (like clear all FIFOs), what sure is worse, than a hard wired front panel signal, but is much better than a VME single cycle loop over a number of units. The four broadcast commands are executed via the VME key addresses at offset 0x030 through 0x3C.

Note: Broadcast functionality is not implemented on firmware version 2

A32 Broadcast Example:
Let four SIS3600 participate by setting the A_32 jumper and setting the base address of the units to:

```
Unit 1: 0x32001000
Unit 2: 0x32001800
Unit 3: 0x32002000
Unit 4: 0x32002800
```

Switch on enable broadcast by setting bit 6 in the control register of the four units.
Enable broadcast handshake controller on unit 4 by setting bit 7 of its control register.
An A232 write to address 0x32000034 will issue one software next clock on units 1 through 4.

A24 Broadcast Example:
Let three SIS3600 participate by setting the A_24 jumper and setting the base address of the units to:

```
Unit 1: 0x541000
Unit 2: 0x542000
Unit 3: 0x543000
```

Switch on enable broadcast by setting bit 6 in the control register of the three units.
Enable broadcast handshake controller on unit 1 by setting bit 7 of its control register.
An A24 write to address 0x540030 will clear the FIFOs and the logic on units 1 through 3.

9 VME Interrupts

Four VME interrupt sources are implemented in the SIS3600 firmware design:

- start of CIP
- FIFO half full
- FIFO almost full
- FIFO full (error condition)

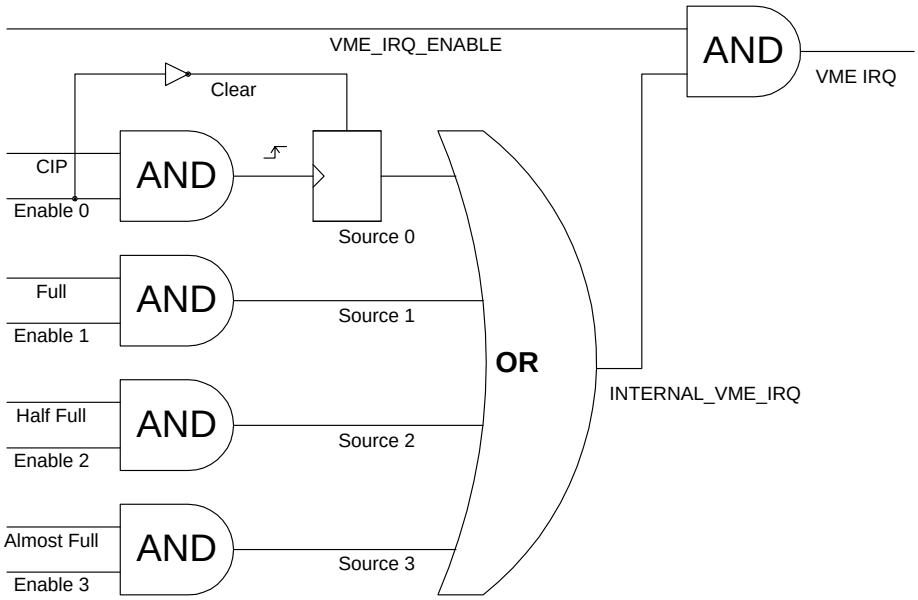
The interrupter is of type D8(O).

The interrupt logic is shown below. For VME interrupt generation the corresponding interrupt source has to be enabled by setting the respective bit in the VME control register (disabling is done with the sources J/K bit). Interrupt generation has to be enabled by setting bit 11 in the IRQ and version register. The internal VME interrupt flag can be used to check on an IRQ condition without actually making use of interrupts on the bus.

The VME interrupt level (1-7) is defined by bits 8 through 10, and the VME interrupt vector (0-255) by bits 0 through 7 of the VME IRQ and version register.

In general an interrupt condition is cleared by disabling the corresponding interrupt, clearing the interrupt condition (i.e. clear overflow) and enabling the IRQ again.

Note: In most cases your experiment may not require interrupt driven scaler readout, but the interrupt capability of the SIS3600 provides a way to overcome the problem of missing front panel inputs on most commercial VME CPUs.



10 Data Format

The 32-bit latched value is copied into the VME word in a straightforward fashion:

10.1.1 D16

	high Byte	low Byte
first read	Data Bits 31-24	Data Bits 23-16
second read	Data Bits 15-8	Data Bits 7-0

10.1.2 D32

Data Bits 31-24	Data Bits 23-16	Data Bits 15-8	Data Bits 7-0

11 Input Configuration

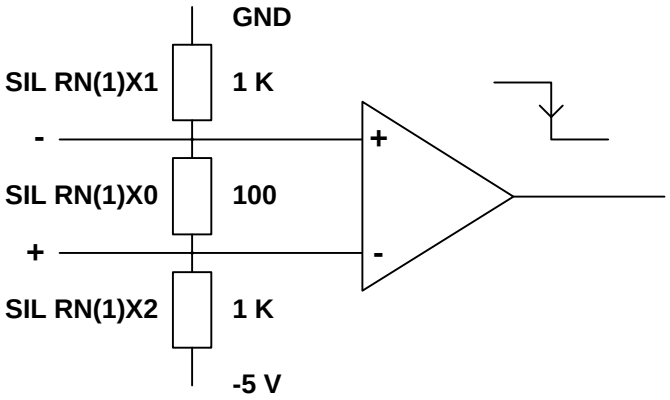
SIS36/38xx boards are available for NIM, TTL and ECL input levels and in LEMO and flat cable versions. The boards are factory configured for the specified input level and connector type, input termination is installed.

11.1 ECL

The 100 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

Network	Channels	1 K Networks
RN10	1-4	RN11/12
RN20	5-8	RN21/22
RN30	9-12	RN31/32
RN40	13-16	RN41/41
RN50	17-20	RN51/52
RN60	21-24	RN61/62
RN70	25-28	RN71/72
RN80	29-32	RN81/82
RN110	Control 1-4	RN111/RN112
RN120	Control 5-8	RN121/RN122

The schematics of the ECL input circuitry is shown below.

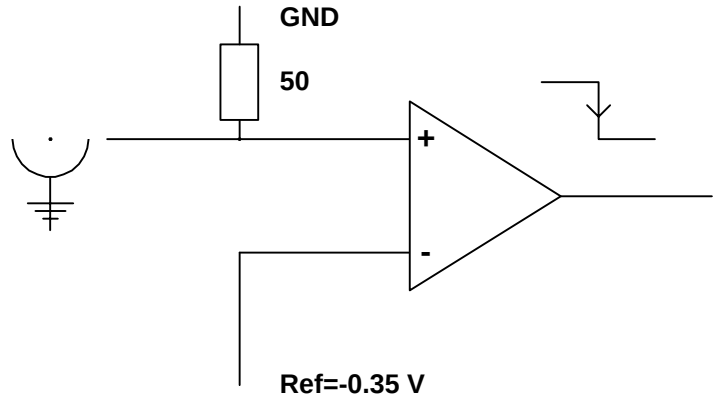


11.2 NIM

The 50 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

Network	Channels
U15 (Pins 10 to 6)	1-4
U15 (Pins 1 to 5)	5-8
U35 (Pins 10 to 6)	9-12
U35(Pins 1 to 5)	13-16
U55 (Pins 10 to 6)	17-20
U55 (Pins 1 to 5)	21-24
U75 (Pins 10 to 6)	25-28
U75 (Pins 1 to 5)	29-32
U115 (Pins 10 to 6)	Control 1-4
U115 (Pins 1 to 5)	Control 5-8

The schematics of the NIM input circuitry is shown below.

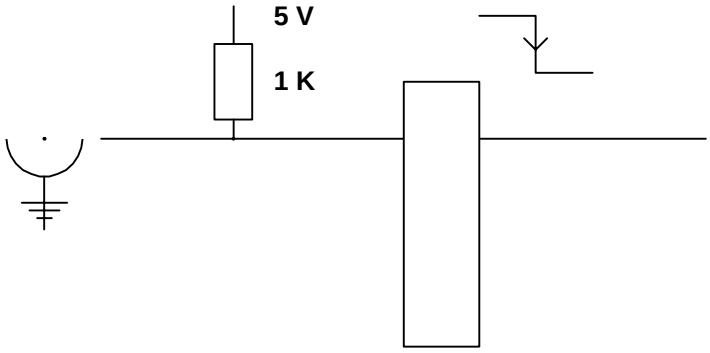


11.3 TTL

The TTL input level option is possible with LEMO and flat cable connectors.

11.3.1 TTL/LEMO

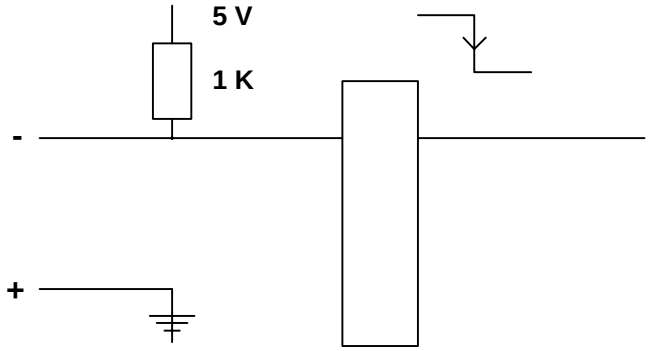
The (low active) TTL/LEMO input circuitry is sketched below. A high active version can be implemented by replacing the 74F245 with a 74F640



245

11.3.2 TTL/Flat Cable

In the flat cable TTL version the positive (right hand side) of the connector is tied to ground.



245

12 Connector Specification

The four different types of front panel and VME connectors used on the SIS360x and SIS38xx boards are:

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
20 pin header	Control (flat cable versions)	DIN41651 20 Pin (AMP e.g.)
34 pin header	Inputs (flat cable versions)	DIN41651 34 Pin (AMP e.g.)
LEMO	Control and Input (LEMO versions)	LEMO ERN.00.250.CTL

13 Control Output Modes

The assignment of the control outputs can be controlled via the output mode bits in the control register. With the default output mode (mode 0) the outputs are compatible with the output assignment of the SIS3801 multiscaler.

13.1 Outputs

Control Output Modes

Mode 0 (bit1=0, bit0=0):
control 8 -> FIFO full
control 7 -> FIFO half full
control 6 -> FIFO empty
control 5 -> CIP

Mode 1 (bit1=0, bit0=1):
control 8 -> FIFO full
control 7 -> FIFO half full
control 6 -> pulser output
control 5 -> CIP

Mode 2 (bit1=1, bit0=0):
control 8 -> fast or
control 7 -> user output
control 6 -> pulser output
control 5 -> CIP

Mode 3 (bit1=1, bit0=1):
control 8 -> pulser output
control 7 -> pulser output
control 6 -> pulser output
control 5 -> pulser output

13.2 Inputs

Four input signals are defined in the SIS3600 firmware, for the time being three of the inputs are actually used.

Signal	Control Signal
reserved	4
Fast Clear	3
RESET	2
External NEXT	1

14 Signal Specification

14.1 Control Signals

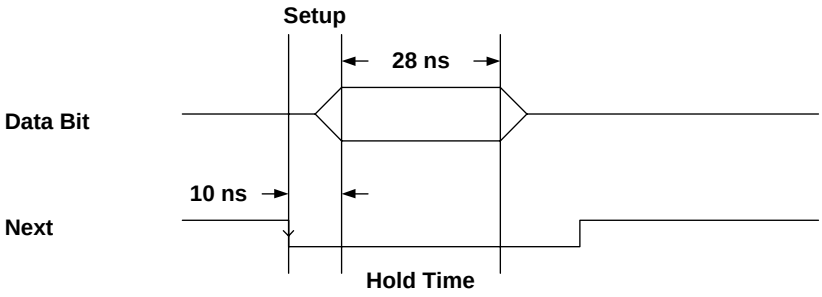
The width of the reset and external next pulse has to be greater or equal 25 ns.

14.2 Inputs

The inputs have to be in accordance with the signal specifications for the given input type (NIM, TTL or ECL). The behaviour of the latch depends on the selected operation mode (strobed/coincidence).

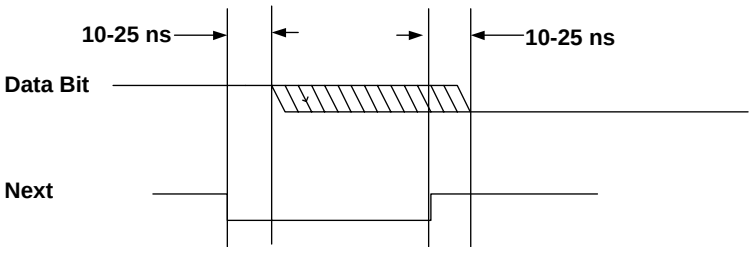
14.2.1 Strobed Mode Input Timing

The timing in strobed mode, which is the most common mode in particle physics, is sketched below. The status of the data bits is latched upon the leading edge of the external (or internal VME) next signal. The data bits should be stable during the setup time of 10 ns and the hold time of 28 ns as shown in the graphic to ensure stable conditions.



14.2.2 Coincidence Mode Input Timing

Coincidence mode is of interest in some applications to avoid the need for timing adaptations by delay cables. In coincidence mode input bits with a low to high transition during the width of the external next signal are latched as 1, all other signals (constant low, constant high and high to low transition during the gate) are latched as 0. As in strobed mode the setup and hold time have to be taken into account. A leading edge in the range from 10 to 25 ns may be recognised, for safe timing the signal has to be adjusted in a fashion, that the data bits are stable in the region from 25 ns after the start of the gate and 25 ns after the end of the gate.



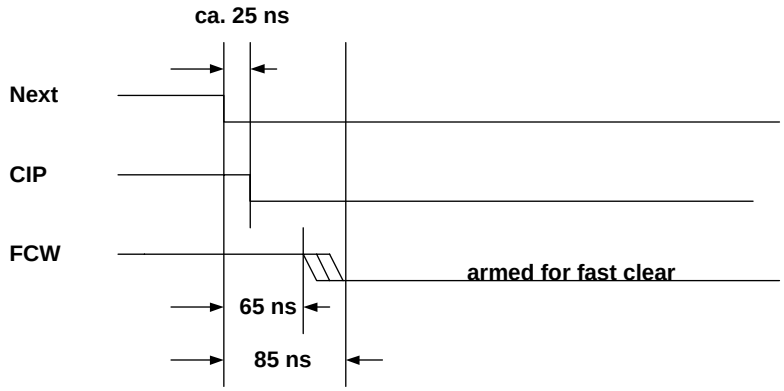
14.3 Outputs

14.3.1 Input to FAST OR Output Timing

The fast OR is implemented on the SIS3600 and can be routed to control signal 8 with output mode 2. The transition timing from signal input to the FAST OR output is of interest for trigger applications. The transition time was measured to be between 20 and 30 ns (the deviation is dominated by the transit time spread of the individual channels). A more accurate measurement with a TDC is yet to be done.
Note: It is possible to derive the next signal for one or more SIS3600 latches from the fast or output, if the pulse width is longer than the transition time plus setup and hold time and possible external deadtime circuitry.

14.3.2 Copy in progress (CIP)

The copy in progress output is routed to control signal 5 in input modes 0, 1 and 2. It is active from 25 ns after the leading edge of the gate until the latched data are copied to the FIFO. If fast clear is enabled the CIP signal will end either with an arriving fast clear pulse or the end of the fast clear window and the completion of the copy to FIFO process.



15 Operating conditions

15.1 Power Consumption/Voltage requirement

Although the SIS3600 is prepared for a number of VIPA features, it was decided to use an ob board DC/DC converter to generate the –5 V, which are needed for driver and receiver chips, to allow for the use of the module in all 6U VME environments. The power consumption is <15 W (+5V, <3A).

15.2 Cooling

Forced air flow is required for the operation of the SIS3600 board.

15.3 Insertion/Removal

Please note, that the VME standard does not support live insertion (hot swap). Hence crate power has to be turned off for installation and removal of SIS3600 latches.
The leading pins on the SIS3600 VME64x VME connectors and connected on board circuitry are designed for hot swap in conjunction with a VME64x backplane (a VME64x backplane can be recognised by the 5 row VME connectors, while the standard VME backplane has three row connectors only).

16 Test

The SIS3600 latches provide the user with a number of test features, which allow for debugging of the unit as well as for overall system setups.

16.1 LED (selftest)

During power up self test and LCA configuration all LEDs except the Ready (R) LED are on. After the initialisation phase is completed, all LEDs except the Ready (R) LED and the Power (P) have to go off. Differing behaviour indicates either a problem with the download of the firmware boot file or one or more LCA and/or the download logic.

16.2 Output pulser test

The frontend Xilinx chips and the drivers can be tested by enabling the output pulser with all four outputs assigned as pulser outputs. By cabling one pulse output to the external next input and a second output to the input bit under test you have the possibility to test data bit by data bit. One should keep in mind, that the maximum next rate is smaller than the maximum output pulser frequency of 10 MHz.

16.3 FIFO Test

FIFO tests via the VME bus are helpful to debug the FIFO on the SIS360x/SIS38xx in case of spurious data and to debug an overall VME system with driver problems on the CPU side or flaky VME termination e.g.. In FIFO test mode the user can write defined data into the units FIFO via the VME bus and to compare them wit the read back result.
FIFO test mode is enabled by setting bit one of the control register and disabled by setting bit 9 of the control register. With FIFO test mode enabled data can be written to the FIFO at the address offset +0x100 (through 0x1FC). Writing to the location with FIFO mode

17 Software Support

VME latch boards are tested at SIS with an OR VP6 VME CPU (Pentium II based) under Windows 95 and a National Instruments CVI user interface. The actual VME C code makes use of the OR Windows 95 DLL, which has straightforward to read and understand routines like:

```
VMEA24StdWriteWord(a32address + KEY_RESET, 0x0);   /* Key Reset */
rdata = VMEA24StdReadWord(a32address + STAT_REG);
```

In most cases the user setup will be using different hardware, a full fleshed real time operating system like VxWorks, and a different user interface. We still believe, that it is helpful to have a look at the code which is used to test the units and to take it as an example for the implementation of the actual scaler readout application. A floppy with our test software is enclosed with SIS3600 shipments.
Depending on the user feedback and co-operation we expect, that we will have drivers or at least example routines for the commonly used VME CPU operating systems at hand in the mid term.

17.1 Contents of the included Floppy

The Floppy contains a readme.txt file with the most up to date information, the CVI project file and all home made files from the project. The important part of the code for the implementation of your own program is sitting in the CVI call back routines.

18 Appendix

18.1 Address Modifier Overview

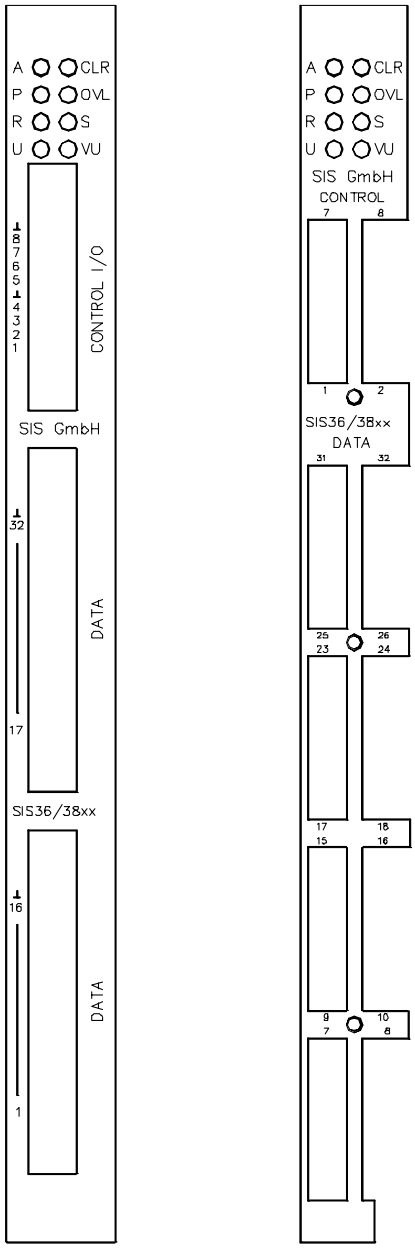
Find below the table of address modifiers, which can be used with the SIS360x/38xx (with the corresponding addressing mode enabled).

AM code	Mode
0x3F	A24 supervisory block transfer (BLT)
0x3D	A24 supervisory data access
0x3B	A24 non-privileged block transfer (BLT)
0x39	A24 non-privileged data access
0x2D	A16 supervisory access
0x29	A16 non-privileged access
0x0F	A32 supervisory block transfer (BLT)
0x0D	A32 supervisory data access
0x0B	A32 non-privileged block transfer (BLT)
0x09	A32 non privileged data access
	Future option: CBLT

18.2 Front Panel Layout

The front panel of the SIS3600 is equipped with 8 LEDs, 8 control in- and outputs and 32 counter inputs. On flat cable units (ECL and TTL) the control connector is a 20 pin header flat cable connector and the channel inputs are fed via two 34-pin headers. On LEMO (NIM and TTL) units the control in- and outputs are grouped to one 8 channel block and the counter inputs are grouped into 2 blocks of 16 channels. The units are 4 TE (one VME slot) wide, the front panel is of EMC shielding type. VIPA extractor handles are available on request or can be retrofitted by the user, if he wants to change to a VIPA crate at a later point in time.
In the drawing below you can find the flat cable (left hand side) and Lemo front panel layouts.

Note: Only the aluminium portion without the extractor handle mounting fixtures is shown



18.3 List of Jumpers

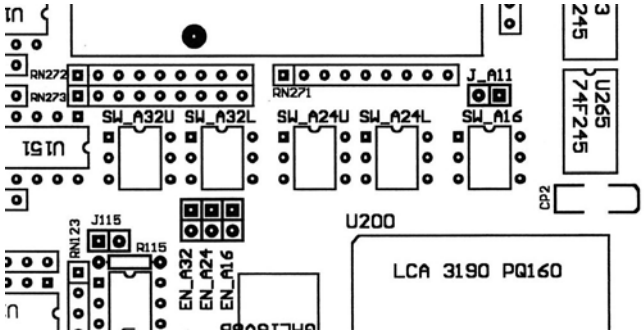
Find below a list of the jumpers and jumper arrays.

Jumper Name	Array/Single	Function
J101	Single	Input Termination Control Input 1
J102	Single	Input Termination Control Input 2
J103	Single	Input Termination Control Input 3
J104	Single	Input Termination Control Input 4
J105	Single	Input Termination Control Input 5
J106	Single	Input Termination Control Input 6
J107	Single	Input Termination Control Input 7
J108	Single	Input Termination Control Input 8
J115	Single	Level Configuration (not for end user)
J500	Array	Boot File Selection
J520	Single	VME SYSRESET Behaviour
EN_A16	Single	Enable A16 addressing
EN_A24	Single	Enable A24 addressing
EN_A32	Single	Enable A32 addressing
J_A11	Single	Address Bit 11 Selection

18.4 Jumper and rotary switch locations

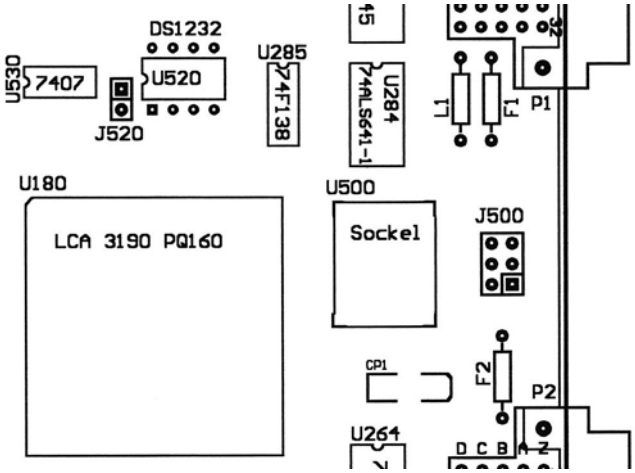
18.4.1 Addressing mode and base address selection

The EN_A32, EN_A24, EN_A16, A_11 and the 5 rotary switches are located int the middle of the upper section of the board close to the DC/DC converter, the corresponding section of the PCB is shown below.

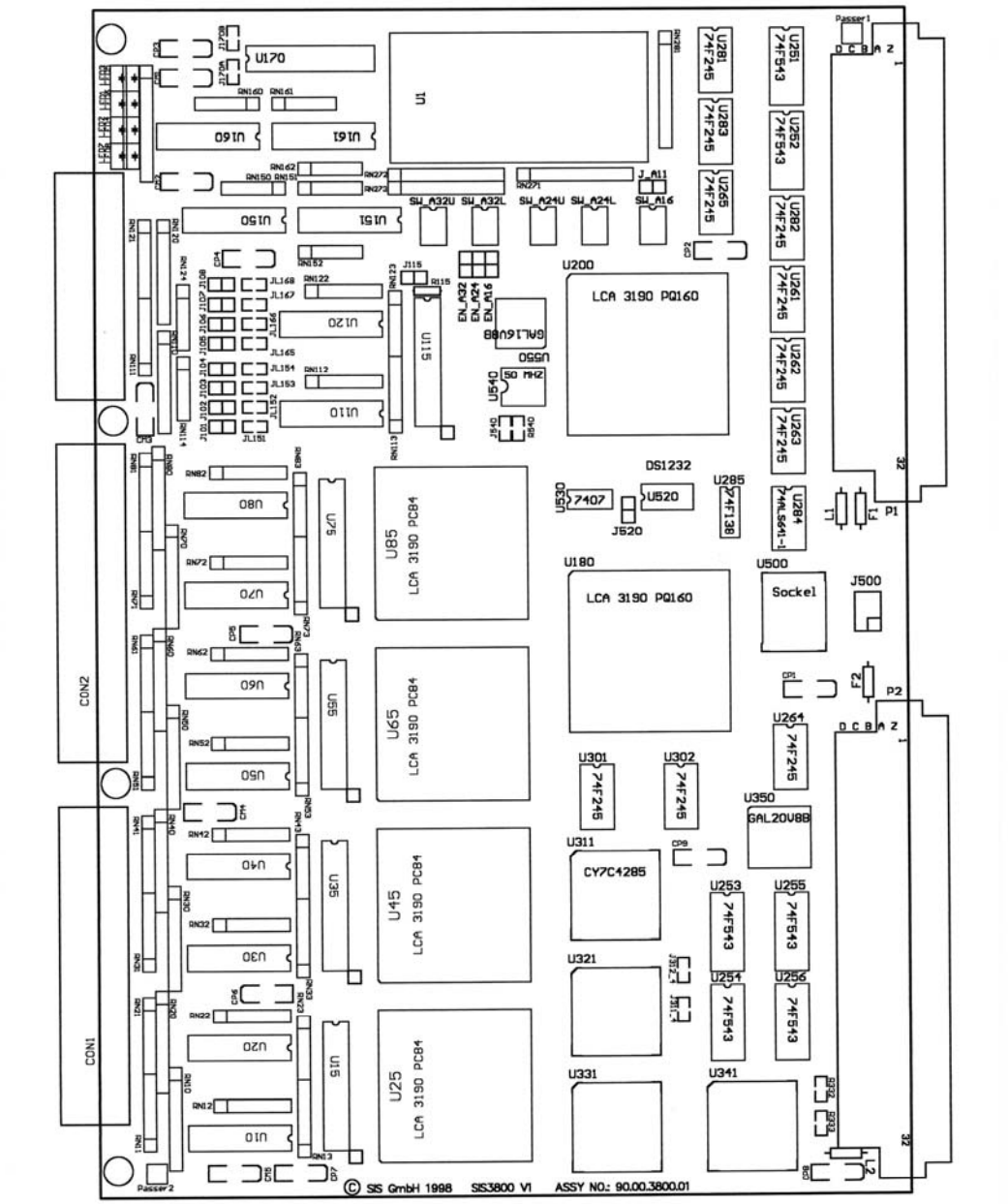


18.4.2 J500 (Bootfile Selection) and J520 (SYSRESET Behaviour)

The jumper array J500 is located between the P1 and the P2 connector. An open position in J500 defines a one (see also chapter 4), the lowest bit is next to the P2 connector.. J520 is located to the left of J500 and closer to the DC-DC converter. With jumper J520 closed the SIS3801 executes a key reset upon the VME SYSRESET signal. The section of the board with the jumper array and the SYSRESET jumper is shown below.

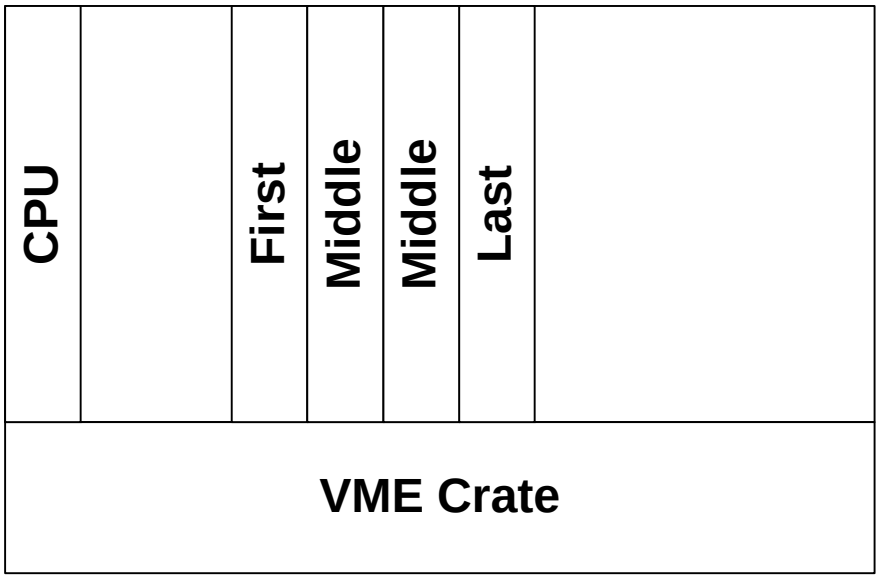


18.5 Board Layout



18.6 CBLT readout

CBLT is a method to speed up the readout of small amounts of data from a larger number of slaves in conjunction with long setup time masters. As header and trailer words are added in CBLT, this readout approach is less efficient than low setup overhead list sequencer readout of masters like the SIS3100 VME sequencer.
Modules which are supposed to participate in a CBLT have to get the same CBLT address, in the case of the SIS3600 the CBLT address is defined by the upper 8 bits of the CBLT setup register . The module closest to the CPU has to be defined as “First” CBLT module, the module at the end of the chain is defined as “Last” CBLT module. All modules have to have their CBLT enable bit set, the modules must occupy a contiguous set of VME slots as shown in the sketch below. The token is passed from the previous module to the next module via the IRQ daisy chain lines as soon as all data have been read. The last module in the chain terminates the transfer with a VME bus error (BERR). .



Schematic CBLT setup

18.6.1 CBLT Setup example

Assume 4 SIS3600 (as shown in the crate above) are supposed to participate in a CBLT. The modules are set to D32 addressing and VME base address configuration as shown in the table below. 0x45 is used as CBLT address and the CBLT setup registers of the three modules are configured as shown in the list.

Module number	D32 base address	VME slot	CBLT setup register	Comment
1	0x20000000	11	0x45000805	First, Geo 1, CBLT enable
2	0x21000000	12	0x45001001	CBLT enable, Geo 2
4	0x22000000	13	0x45001801	CBLT enable, Geo 3
4	0x23000000	14	0x45002003	Last, Geo 4, CBLT enable

A BLT32 read from VME address 0x45000000 will result in a CBLT over the 4 modules, with the selected geographical addresses showing up in the header and trailer words.
If the modules contain no scaler data, the resulting VME data will look like shown below.

32-bit data word	Content	Comment
1	0x08000000	Header module 1, Geo 1
2	0x08000008	Trailer module 1, 8 Bytes
3	0x10000000	Header module 2, Geo 2
4	0x10000008	Trailer module 2, 8 Bytes
5	0x18000000	Header module 3, Geo 3
6	0x18000008	Trailer module 3, 8 Bytes
7	0x20000000	Header module 4, Geo 4
8	0x20000008	Trailer module 4, 8 Bytes

18.6.2 CBLT hints

While it is trivial to setup a block of modules for CBLT readout, one has to be aware of specialities of this readout form.

- The user has to make sure, that the read access to the CBLT address is a block transfer (with address modifier AM=0xB e.g.), i.e. the modules will not respond to a read, which is broken down into many single reads (AM 0x9 e.g.). This can be verified with a VME diagnosis module like the VDIS or with an oscilloscope and an extender.
- The data have to be read in one big chunk, otherwise the transfer will re-commence in the first module of the block after a termination. Many CPUs have 256 Bytes as maximum block size to give a second VME master a chance to get bus mastership. If the anticipated maximum number of data words is bigger than that boundary, you may have to define several smaller CBLT setups, which will then stay below the boundary.
- In many cases the block size will not be known, as it may depend on the number of hits in an ADC or TDC. In that case the user will have to setup a CBLT with the number of possible words and rely on the capability of a block transfer terminated by a VME bus error and a returned Byte count to indicate the actual length of the transfer.
- SIS3600 latches and SIS3806/SIS3811 multiscalers will have their access LED lit as soon as the header word is passed to the VME bus in a CBLT. This gives you an easy way to make sure, that the modules are responding to an access to their CBLT address.

18.7 Cascaded FIFOs

The SIS3600 board can be stuffed with up to four synchronous FIFO chips, the standard unit comes with one FIFO chip (the current V1 board can be stuffed with 4 K, 8 K and 16 K chips, the V2 board will have one 64 K chip as default, i.e. up to a total of 256 K). The FIFO flags are handled by a GAL, which is in the vicinity of the FIFO pads and the actual FIFO flag implementation for cascaded FIFOs will be described here in a later version of the manual.

18.8 FLASHPROM Versions

A list of available FLASHPROMs can be obtained from http://www.struck.de/sis3638firm.htm. Please note, that a special hardware configuration may be necessary for the firmware design of interest (the SIS3801 design requires the installation of a FIFO e.g.).
The table on the web is of the format shown below, the lowest EPROM entry of this example table describes, the version that is currently shipped:

SIS36/38xx FLASHPROM table

Design Name	Design	Boot File (s)
SIS3800_201098	0	SIS3800 Version 1
SIS3801_201098	0	SIS3800 Version 1
	1	SIS3800 Version 2
	2	SIS3801 Version 1 (32-bit Design)
	3	SIS3801 Version 2 (24-bit Design)
SIS3803_280798	0	SIS3803 Version 1
SIS3600_010201	0	SIS3600 Version 1
	1	SIS3600 Version 2

18.9 Row d and z Pin Assignments

The SIS3600 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

18.10 Geographical Address Pin Assignments

The SIS36/38xx board series is prepared for geographical addressing via the geographical address pins GA0*, GA1*, GA2*, GA3*, GA4* and GAP*. The address pins are left open or tied to ground by the backplane as listed in the following table:

Slot Number	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

18.11 Additional Information on VME

The VME bus has become a popular platform for many realtime applications over the last decade. Information on VME can be obtained in printed form, via the web or from newsgroups. Among the sources are the VMEbus handbook, http://www.vita.com (the home page of the VME international trade association (VITA)) and comp.bus.arch.vmebus. In addition you will find useful links on many high energy physics labs like CERN or FNAL

19 Index