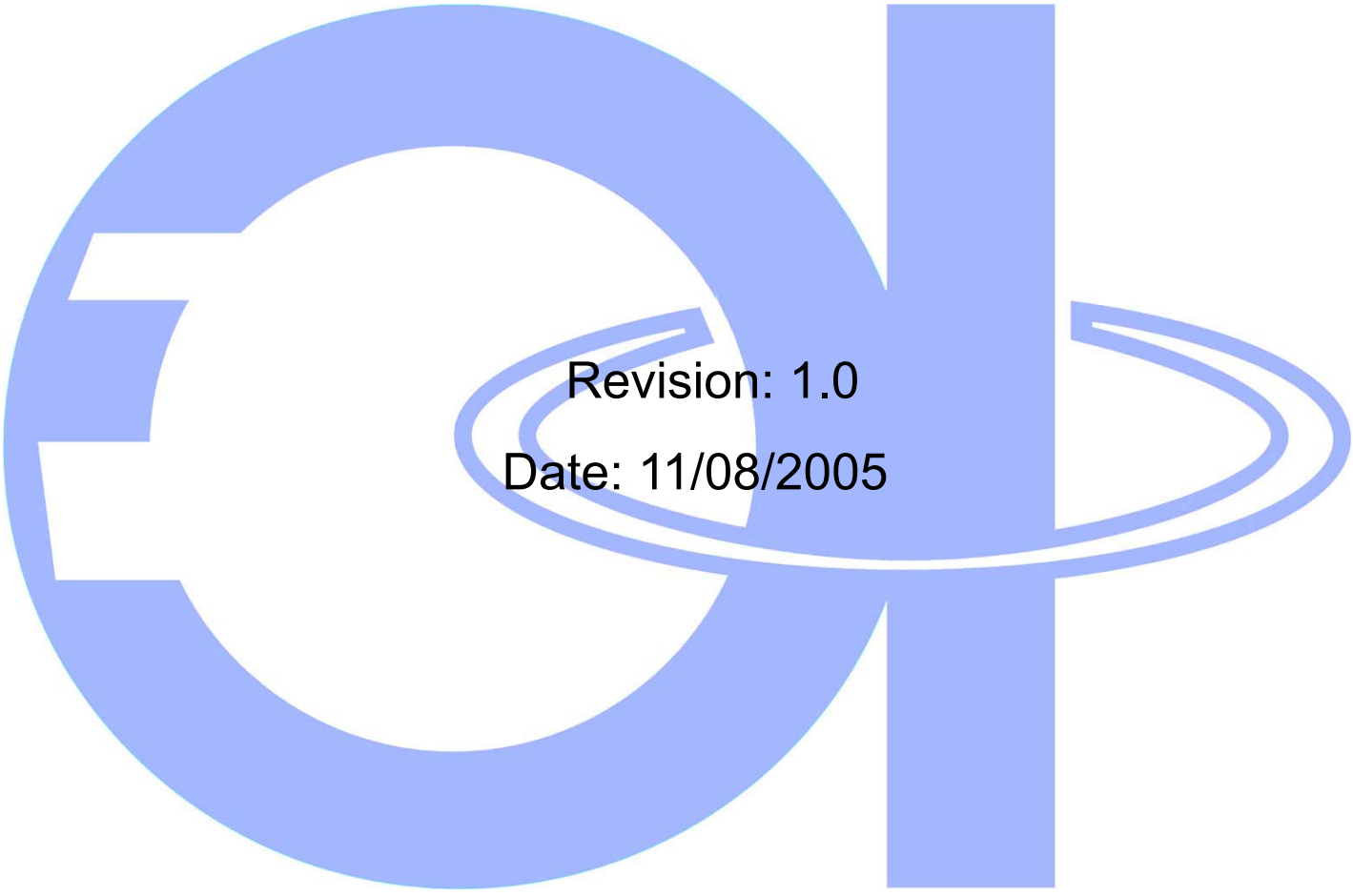
JL2005D

1.3M-Pixel Digital Camera Controller



Revision: 1.0

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Table of Contents

0. Revision History

Revision	Description of Changes	Date
1.0	First Release	2005/11/08

1. General Description

JL2005D is a low cost and highly integrated DSC controller. It consists of CMOS image sensor interface, image processing, image compression engine, low battery detect, status LCD interface, DDR/SDRAM interface, UART port and USB1.1 interface. JL2005D supports VGA and 1.3 mega-pixels CMOS sensors. It provides dual-mode operation, DSC mode and PC CAM mode. It is designed to fulfill the requirements of digital camera applications.

The JL2005D integrates excellent image processing features such as AE, bad-pixel cancellation, image compression engine. In DSC mode, it stores the compressed image data to an external SDRAM. In PC-Camera mode, the compressed image data is downloaded to PC though USB interface.

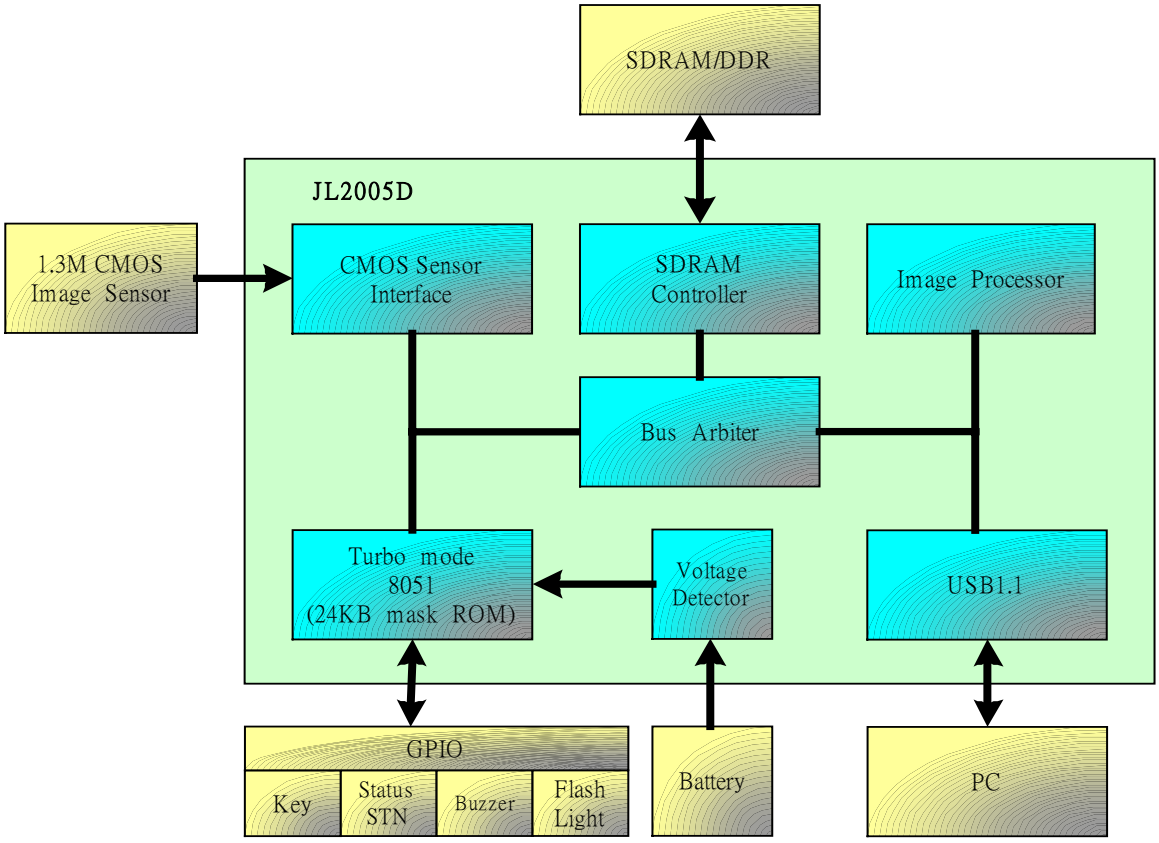
2. Features

- Dual mode operation
- Supports CMOS image sensor with CIF, VGA, and 1.3M resolution
- Auto bad-pixel cancellation
- AE measurement
- Built-in compressed engine
- Support 8/16-bit DDR/SDR SDRAM up to 128Mb (16Mb, 32Mb, 64Mb, 128Mb)
- SDRAM chip test and downgrade SDRAM address remapping
- Status LCD controller
- Embedded turbo mode 8051 with ISP function
- Built-in 24K bytes mask ROM
- Supports external ROM
- USB1.1 interface
- Provides multi-function GPIOs
- PWM waveform generator for mechanical shutter and flash light control
- Low battery detect
- 100-pin LQFP package/COB (Chip On Board)

3. Application

- Low Cost SDRAM DSC
- Web CAM
- PC CAM

4. Block Diagram



5. Pin Descriptions

Pin No.	Pin Name	Type	Description
1	VDD33_XSC	P	+3.3V Crystal pad power
2	XSCI	ICLK	Crystal oscillator pad input, connect to12 MHz crystal
3	XSCO	OCLK	Crystal oscillator pad output, connect to12 MHz crystal
4	VSS33_XSC	G	Crystal pad ground
5	/RESET	I, S	Power on reset, active low
6	S_PWDN	O2	CMOS image sensor power down signal
7	S_RESET	O2	CMOS image sensor reset signal
8	S_EXCLK	O2	CMOS image sensor system clock
9	S_PCLK	I	CMOS image sensor pixel clock
10	S_HSYNC	I	CMOS image sensor horizontal synchronous
11	S_VSYNC	I	CMOS image sensor vertical synchronous
12	S_D0	I	CMOS image sensor video data bus
13	S_D1	I	CMOS image sensor video data bus
14	S_D2	I	CMOS image sensor video data bus
15	S_D3	I	CMOS image sensor video data bus
16	S_D4	I	CMOS image sensor video data bus
17	S_D5	I	CMOS image sensor video data bus
18	S_D6	I	CMOS image sensor video data bus
19	S_D7	I	CMOS image sensor video data bus
20	SCL	OD	Serial clock output
21	SDA	OD	Serial data output
22	GPIO_0	B2	General purpose I/O 0 or Pattern generator 0 output [*6]
23	GPIO_1	B2	General purpose I/O 1 or Pattern generator 1 output [*6]
24	GPIO_2	B2	General purpose I/O 2 or External interrupt input, active low [*6]
25	GPIO_3	B2	General purpose I/O 3
26	GPIO_4	B2	General purpose I/O 4 or USB Plug-in input [*6]
27	GPIO_5	B2	General purpose I/O 5 or MPU data write enable output [*6], active low
28	GPIO_6	B2	General purpose I/O 6
29	VCC2.5V	P	+2.5V core power
30	GND	G	Ground
31	VCC3.3V	P	+3.3V I/O power
32	GPIO_7	B2	General purpose I/O 7 or MPU program read enable output, active low [*1]
33	GPIO_8	B2	General purpose I/O 8 [*1] or MPU program write enable output, active low
34	GPIO_9	B2	General purpose I/O 9 [*1] or MPU Address latch enable output, active high
35	GPIO_10	B2	General purpose I/O 10 [*1] or MPU address/data bit 0

Pin No.	Pin Name	Type	Description
36	GPIO_11	B2	General purpose I/O 11 *1 or MPU address/data bit 1
37	GPIO_12	B2	General purpose I/O 12 *1 or MPU address/data bit 2
38	GPIO_13	B2	General purpose I/O 13 *1 or MPU address/data bit 3
39	GPIO_14	B2	General purpose I/O 14 *1 or MPU address/data bit 4
40	GPIO_15	B2	General purpose I/O 15 *1 or MPU address/data bit 5
41	GPIO_16	B2	General purpose I/O 16 *1 or MPU address/data bit 6
42	GPIO_17	B2	General purpose I/O 17 *1 or MPU address/data bit 7
43	GPIO_18	B2	General purpose I/O 18 *1 or MPU address bit 8
44	GPIO_19	B2	General purpose I/O 19 *1 or MPU address bit 9
45	GPIO_20	B2	General purpose I/O 20 *1 or MPU address bit 10
46	GPIO_21	B2	General purpose I/O 21 *1 or MPU address bit 11
47	GPIO_22	B2	General purpose I/O 22 *1 or MPU address bit 12
48	GPIO_23	B2	General purpose I/O 23 *1 or MPU address bit 13
49	GPIO_24	B2	General purpose I/O 24 *1 or MPU address bit 14
50	GPIO_25	B2	General purpose I/O 25 *1 or MPU address bit 15
51	D_DQ0	B2	16 bit SDRAM data bit 0 or Key_0 *2 8 bit SDRAM data bit 0
52	D_DQ1	B2	16 bit SDRAM data bit 1 or Key_1 *2
53	D_DQ2	B2	16 bit SDRAM data bit 2 or Key_2 *2 8 bit SDRAM data bit 1
54	D_DQ3	B2	16 bit SDRAM data bit 3 or Key_3 *2
55	D_DQ4	B2	16 bit SDRAM data bit 4 or Key_4 *2 8 bit SDRAM data bit 2
56	D_DQ5	B2	16 bit SDRAM data bit 5 or Key_5 *2
57	D_DQ6	B2	16 bit SDRAM data bit 6 or Key_6 *2 8 bit SDRAM data bit 3
58	D_DQ7	B2	16 bit SDRAM data bit 7 or Key_7 *2
59	GPIO_26	B2	General purpose I/O 26 or DDR high byte data strobe output
60	D_LDQM	O2	DDR low byte data write mask or SDRAM low byte data input/output mask
61	/D_WE	O2	SDRAM write enable, active low
62	/D_CAS	O2	SDRAM column address strobe, active low
63	/D_RAS	O2	SDRAM raw address strobe, active low
64	D_BS0	O2	SDRAM bank address 0
65	D_BS1	O2	SDRAM bank address 1
66	D_A10	B2	SDRAM address bus or M51_nEA *5
67	D_A0	B2	SDRAM address bus or Firmware_CFG0 *4

Pin No.	Pin Name	Type	Description
68	D_A1	B2	SDRAM address bus or Firmware_CFG1 *4
69	D_A2	B2	SDRAM address bus or Firmware_CFG2 *4
70	VCC2.5V	P	+2.5V core power
71	GND	G	Ground
72	VCC3.3V	P	+3.3V I/O power
73	D_A3	B2	SDRAM address bus or Firmware_CFG3 *4
74	D_DQ15	B2	16 bit SDRAM data bit 15 or Firmware_CFG15 *4 8 bit SDRAM data bit 7
75	D_DQ14	B2	16 bit SDRAM data bit 14 or Firmware_CFG14 *4
76	D_DQ13	B2	16 bit SDRAM data bit 13 or Firmware_CFG13 *4 8 bit SDRAM data bit 6
77	D_DQ12	B2	16 bit SDRAM data bit 12 or Firmware_CFG12 *4
78	D_DQ11	B2	16 bit SDRAM data bit 11 or Firmware_CFG11 *4 8 bit SDRAM data bit 5
79	D_DQ10	B2	16 bit SDRAM data bit 10 or Firmware_CFG10 *4
80	D_DQ9	B2	16 bit SDRAM data bit 9 or Firmware_CFG9 *4 8 bit SDRAM data bit 4
81	D_DQ8	B2	16 bit SDRAM data bit 8: DQ_8 or Firmware_CFG8 *4
82	GPIO_27	B2	General purpose I/O 26 or DDR low byte data strobe output
83	D_UDQM	O2	DDR high byte data write mask or SDRAM high byte data input/output mask
84	/D_CLK	O2	DDR inverted clock
85	D_CLK	O2	DDR/SDRAM clock
86	D_CKE	O2	SDRAM clock enable
87	D_A11	B2	SDRAM address bus *3
88	D_A9	B2	SDRAM address bus *3
89	D_A8	B2	SDRAM address bus *3
90	D_A7	B2	SDRAM address bus or Firmware_CFG7 *4
91	D_A6	B2	SDRAM address bus or Firmware_CFG6 *4
92	D_A5	B2	SDRAM address bus or Firmware_CFG5 *4
93	D_A4	B2	SDRAM address bus or Firmware_CFG4 *4
94	VDD33_USB	P	+3.3V USB1.1 transceiver power
95	DM	USB	USB D- signal
96	DP	USB	USB D+ signal
97	VSS33_USB	G	USB1.1 transceiver ground
98	VDD25_PLL	P	+2.5V PLL and battery detect ADC power

Pin No.	Pin Name	Type	Description
99	VSS25_PLL	G	Ground for PLL and battery detect ADC
100	BAT_DET	AI	Low battery detect input

NOTE:

*1: This pin can be function as GPIO when internal mask ROM was enabled

*2: To prevent from disturbing normal SDRAM data access, please connect this pin to weak pull-up and weak pull-down resistor for input Key function.

*3: Must pull-down this pin for normal operation.

*4: Signals on this pin will be latched to internal register when power on reset was active. After power on reset was removed this pin will return to normal function as well.

*5: Pull-down this pin to select external ROM or pull-up this pin to select internal mask ROM.

*6: Each GPIO pin has it's own function select register Alt, firmware can program each GPIO pin to different function individually. It is as GPIO pin after power on reset.

Buffer Type Descriptions:

All CMOS input pin can take 5V tolerance

BUFFER	DESCRIPTION
I	3.3V CMOS Input pin
S	Schmitt-Trigger
B2	3.3V CMOS Bi-drectional pin with 2 mA drive
O2	3.3V CMOS Output pin with 2 mA drive
OD	3.3V CMOS Output pin with open drain
ICLK	XTAL clock input
OCLK	XTAL clock output
AI	Analog input
USB	USB Interface
P	Power pin
G	Ground pin

6. ELECTRICAL CHARATERISTICS

Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply (3.3V)	-0.3 to 3.6	V
V_{CC1}	Power Supply (2.5V)	-0.3 to 2.75	V
V_{IN}	Input Voltage	-0.3 to V_{CC}+0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{CC}+0.3	V
T_{STG}	Storage Temperature	-55 to 150	℃

Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply (3.3V)	3.0	3.3	3.6	V
V_{CC1}	Power Supply (2.5V)	2.25	2.5	2.75	V
T_{OPR}	Operating Temperature	0	25	70	℃

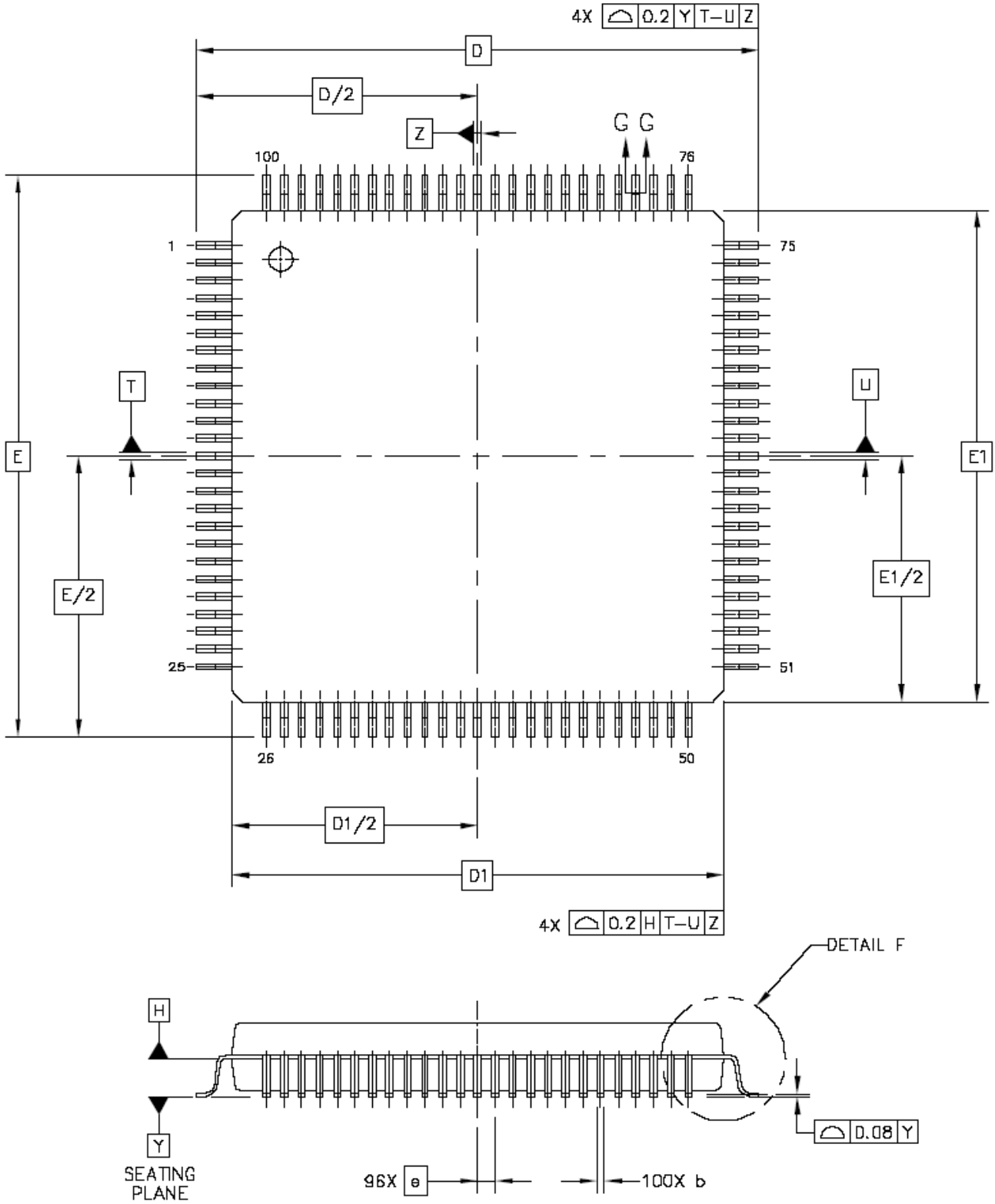
DC Electrical Characteristics for 3.3 volts operation

(Under Recommended Operating Conditions and V_{CC} = 3.0V~3.6V, T_j = 0℃ to +70℃)

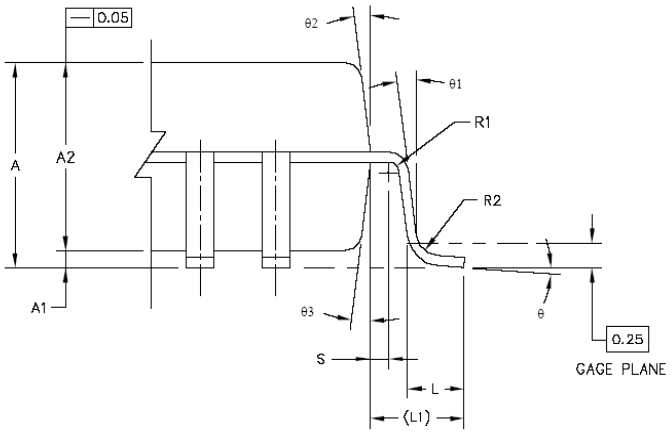
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		Vcc+0.3	V
V_{T-}	Schmitt Input Low Voltage		-0.3		0.8	V
V_{T+}	Schmitt Input High Voltage		2.0		Vcc+0.3	V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V

7. Package Outline and Dimension

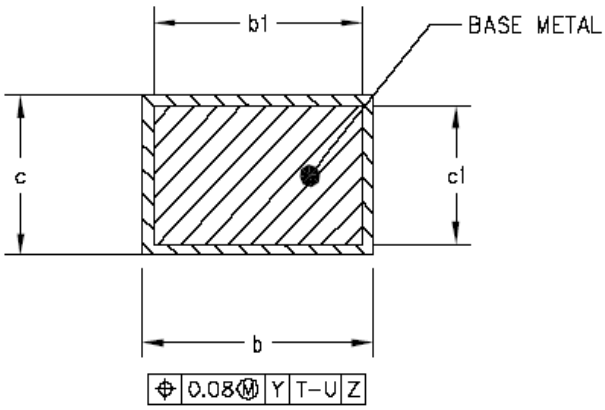
- **Package Outline (100-pin LQFP)**



- **Package Outline (100-pin LQFP) - continued**



DETAIL F



SECTION G-G

- **Dimension (100-pin LQFP)**

Symbol	Min	Nom	Max	Unit
A	-	-	1.6	mm
A1	0.05		0.15	mm
A2	1.35	1.40	1.45	mm
c	0.09		0.20	mm
b	0.17	0.2	0.27	mm
D	-	16	-	mm
D1	-	14	-	mm
e	-	0.5	-	mm
E	-	16	-	mm
E1	-	14	-	mm
L1	-	1	-	mm

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