DVI Compliant Receiver
TH161-G

User Guide
V0.7

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Se2ction 1 Introduction

1.1 Overview

The TH161-G is a low cost DVI receiver in 100-pin LQFP package. It is compliant to DVI Revision 1.0 specification and supports display resolution from VGA to UXGA (25 - 165MHz) in 1 or 2 pixels/clock mode. The build-in PLL requires no external component. The on-chip Link On detection circuit works even when the chip is put in Power Down mode.

1.2 Features

The DVI Receiver TH161-G includes these distinctive features:

- DVI specification 1.0 compliant
- Operation pixel frequency range: 25MHz - 165MHz
- PLL requires no external components
- High skew tolerance: 1 full input clock cycle
- Low current consumption in Power Down mode
- Link On detection even in Power Down mode
- Controllable tri-state for output port
- Single 3.3V CMOS design
- 100-pin LQFP (Pb free, compliant to JEDEC/IPC J-STD-006)
- Pin Compatible with Silicon Image SiI161B