

DAC-AVA-DMUX

SD/HD video DAC with optional frame-synchronized SDI outputs

User manual

Rev. A

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Revision history

Current revision of this document is the uppermost in the table below.

Rev.	Repl.	Date	Sign	Change description
Α	-	20131015	TB	Initial version.

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1 Product overview

The Flashlink DAC-AVA-DMUX is an HD-SDI/SD-SDI video DAC with built-in frame synchronizer, optional SDI outputs and optional audio and data outputs.

At the heart of the DAC-AVA-DMUX is an HD/SD frame synchronizer with an adjustable delay relative to the sync signal. The module accepts black & burst or a tri-level signal from the frame. The DAC-AVA-DMUX also has a de-glitcher to give error-free synchronous switching.

A set of configurable analog video outputs and two optional SDI digital outputs are provided.

The audio embedded in the HD-SDI or SD-SDI stream is de-embedded and can be delayed relative to video. Each audio channel can be swapped in an audio matrix before they are reembedded in the SD-SDI data output stream. It is also possible to turn embedding completely off and leave the SDI stream unaltered.

A selection of user parameters of the card can be controlled by switches on the board. Complete control of all parameters is available by use of the Flashlink RS422 Control Protocol Version 4, which is supported by the Multicon system controller.



Figure 1: DAC-AVA-DMUX-R block diagram

1.1 Hardware products

Two hardware versions of the DAC-AVA-DMUX exist:

DAC-AVA-DMUX+ SD/HD video DAC. Optional 2xSDI out, internal audio handling, and frame synchronizer functionality.

DAC-AVA-DMUX-R+ SD/HD video DAC with high sensitivity 9/125µm single mode optical input. Optional 2xSDI out, internal audio handling, and frame synchronizer functionality.

1.2 Software options

The base products DAC-AVA-DMUX / DAC-AVA-DMUX-R do not have the framesynchronized SDI outputs enabled, or the AES and analog audio outputs enabled. Nor do they have the ability to receive SD-SDI or HD-SDI input signals. This means that at least one these two input capabilities must be ordered as a factory option or purchased as a software key upgrade at a later time in order to have a useful product.

	Nevion option code
Hardware	DAC-AVA-DMUX+
(select <u>one</u>)	DAC-AVA-DMUX-R+
	+
Input formats	DAC OPT input HD
(select <u>at least</u> one)	DAC OPT input SD
	+
AES/analog audio outputs	DAC OPT audio

Table 1: Available options

At the bottom of the information page (the 'front page') of the module in Multicon GYDA a line will show which features are enabled:

Purchased features SD: Yes, HD: Yes, SDI: Yes, Audio: Yes

This example shows a module with all optional features present.

1.2.1 How to apply a software key that enables new options

 In Multicon Gyda, navigate to the DAC-AVA-DMUX module in question by first pressing the frame symbol and then pressing the icon for the DAC-AVA-DMUX. In the example picture below, two such modules are present in the same frame, and the one in slot 1 has been selected.

Multicon GYDA	• 1	2	3	4	5	6	7	8	9	10	PSU	PSU	•
0	U DAC				DAC								•



2) Check which features are already enabled in the module. At the bottom of the information page that is now shown will be a line that says "Purchased features", which lists the enabled input formats, whether the SDI outputs are enabled, and finally whether the AES/analog audio outputs are enabled or not. In the examples shown here, all optional features are already enabled and no further upgrades are available.

Purchased features	SD: Yes, HD: Yes, SDI: Yes, Audio: Yes
--------------------	--

Figure 3: How to see purchased features, new Multicon Gyda

Older versions of Multicon Gyda cannot display the line "Purchased features" properly, the words "SD:", "HD:", "SDI:" and "Audio:" will be missing.

Purchased features Yes, Yes, Yes, Yes

Figure 4: How to see purchased features, older Multicon Gyda

If for instance "HD:" should say "No", this feature can be purchased as a software key upgrade.

 If the customer decides to buy a feature upgrade, Nevion will need both the serial number of the module to be upgraded and a list of the new features the customer wishes to purchase for it.

The serial number can be found on the very bottom of the configuration page for the module (To navigate between the information page and the configuration page, press the "i" symbol and the wrench symbol, respectively).

Each new input format or feature has its own order number in the price list.

Card version	
FPGA	1.74
SW	1.00
Serial	1270109876543217
\bigcirc	

Figure 5: Where to find the serial number

4) The customer will receive a software key from Nevion. The key will be in the form of the string "optn 0" plus six groups of up to 10 digits. Like this, but with different numbers:

optn 0 1234567890 1234567890 1234567890 1234567890 1234567890 1234567890 1234567890

This software key is linked to the serial number of the module and must be sent to the module via the debug terminal in Multicon Gyda.

To access the debug terminal, hover the mouse over the cog wheels and select "Debug terminal" from the drop-down menu. See figure Figure 6 below.



Figure 6: How to get to the Debug terminal in the current Multicon version

In previous versions of Multicon, the user must first select "Config" in the top menu, and then press "Debug terminal", see Figure 7 and Figure 8 below.



Figure 7: Step one to access the Debug terminal in the previous Multicon version



Figure 8: Step two to access the Debug terminal in the previous Multicon version

5) Now comes the only tricky part of the procedure: To address a particular module through the debug terminal, one has to take the frame number and slot number and make a unique two-digit address from them. To do this, multiply the frame number from the Multicon GUI with 10, then add the slot number from the Multicon GUI, and finally subtract 1.

Another way of saying this is that the left digit of the address is the frame number, and the right digit is the slot number minus one, i.e. slots counted from 0 to 9, instead of 1 to 10 as they are displayed in the Multicon user interface. The two modules in our example were both in frame 0, but in slots 1 and 5 respectively. This gives us the addresses "00" (0*10 + 1 - 1) and "04" (0*10 + 5 - 1).

Before trying to send the software key it could be wise to check that the addressing is indeed correct. That can be done by sending a single question mark ("?") to the module. In the Flashlink protocol this is known as the "hello" command, and is basically a who-are-you command. The module should identify itself with the module type, version information, and serial number. In the example below the hello command has been sent to the module in frame 0/slot 5 (that is, address "04"), and the module has replied. Then the software key "optn 0 123456 123 ..." has been copy-pasted into the command field and is ready to be sent to the module. The command will be sent when the "Ok" button is pressed. The module will then reply with "ok", and restart with the new features enabled. It will take a few seconds before Multicon Gyda rediscovers the module after the restart.

Multicon 3.7.0-pre1-svn256:	32-pnordby		* [#]	((Ū))	甜
Debug term	inal				
0709? 0907DAC-AV SW rev 1.0 FPGA rev 1 Serial rev protocol v *46EC 0709optn 0	A-DMUX-R 1 .75 12701 er 4.0				
0907optn 0 *18A5	inact				
Card Gyda	Comman	d	Action		

 07
 09
 \$88861604 2538200853
 Ok
 No checksum
 Cancel
 Clear

 Figure 9: The debug terminal, actual serial number and product key greyed out.

6) Remember to check that the module now has the new features enabled. Please refer to step 2).

2 Specifications

Optical SDI input (optional)

Data rate optical:	270 – 1485 Mbps
 HD-SDI (1485 Mbps): SD-SDI (270 Mbps): Detector overload threshold: Detector damage threshold: Optical wavelength: 	Better than -22dBm Better than -22dBm Min3dBm >+1dBm 1200-1620nm
Transmission circuit fiber: Connector return loss: Connector:	9/125um Single Mode >40dB w/ SM fiber SC/UPC
Electrical SDI input	
Connectors Equalization	75 Ohm BNC Automatic: - >300m @270Mbps w/Belden 8281, BER < 10E-12 >100m @1485Mbps w/Belden 16940_BER < 10E-12
Input Return loss Jitter tolerance	 >100m @ 1400mbp3 w/beiden 1004A, BER < 10E112 >15dB, 5MHz -1.5GHz SD limit: 10Hz-1kHz: >1 UI 10kHz – 5MHz: >0.2 UI HD limit: 10Hz-100kHz: >1 UI 100kHz–10MHz: >0.2 UI
Electrical Sync input	
Connector Format Input Return loss	75 Ohm BNC Black & Burst, Tri-level <-35dB @ < 10MHz,

Electrical SDI outputs (optional)

Number of outputs	2
Connectors	75 Ohm BNC
Output Return loss	>15dB, 5MHz -1.5GHz
Output signal level	800mV +/- 10%
Output signal rise /	- SD limit: [0.4ns – 1.5ns]; <0.5ns rise/fall var.
fall time, 20% - 80%	- HD limit: < 270ps, <100ps rise/fall var.
Amplitude overshoot	<10%
Output timing jitter	- SD: <0.2 UI
	- HD: <1 UI
Output alignment jitter	- SD: <0.15 UI
,	- HD: <0.15 UI

30dB @ < 30MHz

Analog Video output, NTSC/PAL

Number of outputs	1 Component RGB/ YUV or 3 CVBS
Connector	3 x 75R BNC
DC offset	< 0±15mV

White level, NTSC Sync level, NTSC Return loss White level, PAL Sync level, PAL Diff gain Diff phase AM noise PM noise S/N 2T K-factor (2T pulse distortion) Luma non-linearity Output resolution	100±1 IRE 40±1 IRE > 35dB @ 10MHz, >40dB @ 5MHz 100±1 IRE 40±1 IRE <0.5% <1deg < -60dB < -60dB < 0.5% < 2% 10 bits
Analog Video output, HD	
Number of outputs Connector DC offset White level Return loss Output resolution	1 component RGB/ YPbPr 3 x 75R BNC < 0±15mV 100±1 IRE > 30dB @ 30MHz 10 bits
Analog Audio output	
Number of outputs Connectors Impedance	1 stereo pair 2 x WECO audio connectors < 66R

Number of outputs	1 stereo pair
Connectors	2 x WECO audio connec
Impedance	< 66R
Dynamic range	>100dB(A)
Crosstalk	< -60dB 20Hz-20kHz
THD+N	-70dB
Frequency response	20Hz-20kHz +/- 0.5dB
Output level	24dBu +/- 1dB
Common mode DC	0-48V
immunity	
Level adjustment range	0 – 24dBu with 1db step
Two tone intermodulation	< -80dB
Output resolution	24 bits

AES output

Number of outputs1ConnectorsWECOReturn loss110R +/Output jitter<0.0025</td>

1 WECO audio connector 110R +/-20% 0.1MHz – 6.144MHz <0.0025UI peak

Supported standards

SD, 270 Mbps	SMPTE 259M, SMPTE 272M-AC
HD, 1485 Mbps	SMPTE 292M, SMPTE 274M, SMPTE 291M, SMPTE 296M,
	SMPTE 299M
Analog video	SMPTE 170M, SMPTE 274M, ITU-R. BT.470,
-	ITU-R. BT.709 Part 2
Video switch point	SMPTE RP168 (tri-level), SMPTE 170M, ITU-R. BT.470

definition and sync AES Optical EDH Video Payload Identification

AES3-1996 SMPTE 297M, SMPTE 292M Compliant to SMPTE RP165 SMPTE 352M-2002

Other

Power consumption

5 V - 4.8 W (4.4 W without optional optical receiver) 15 V - 2.7 W - 15 V - 0.8 W

3 How to get started

3.1 Power requirements

The absolute maximum total power consumption for this module is 8.3 W, of which 4.8 W are drawn from the +5 V supply, 2.7 W are drawn from the +15 V supply, and 0.8 W are drawn from the -15 V supply. These numbers include 0.4 W from the +5 V supply for the optional optical input module, and the calculation of how many modules can be powered by a single power supply can thus be based on 4.4 W for the DAC-AVA-DMUX and 4.8 W for the DAC-AVA-DMUX-R.

Note that the module will draw its power from multiple supply voltages. When calculating the number of modules that can safely be used in one frame, it's important to consider each supply voltage separately for the power supply in question. In general there will be no load-sharing between the supply voltages, and the number of modules will be limited by the worst-case result from the individual calculations. Example calculation with 75 W power supply, limited to 9A on +5 V (45 W) and 1 A each on +15 V and -15 V (15 W each): 45 W / 4.8 W = 9 , 15 W / 2.7 W = 5 , 15 W / 0.7 W = 21 The +15 V output of this power supply will thus limit the number of DAC-AVA-DMUX-R cards to just five, even though the +5 V and -15 V could handle more.

3.2 Physical connections



Figure 10: The cable side of the backplane, DAC-AVA-DMUX-C1

The backplane for the DAC-AVA-DMUX is labeled 'DAC-AVA-DMUX+' or 'DAC-AVA-DMUX-R+' depending on the type of module it was sold with. It is designed to be fitted in a Flashlink frame and to take up a single slot. The table below is an overview of the connectors and their associated functions.

Function	Label	Connector type
HD/SD-SDI input	IN	BNC
HD/SD-SDI sync output 1	01	BNC
HD/SD-SDI sync output 2	O2	BNC
Analog video output, Y/G/CVBS	Y/G/CVBS	BNC
Analog video output, Pb/B/Y	PB/B/Y	BNC
Analog video output, Pr/R/C	PR/R/C	BNC
Analog audio output, left	AAL	WECO Audio connector
channel		O Positive
		🔲 O 🛛 GND
		O Negative
Analog audio output, right	AAR	WECO Audio connector
channel		O Positive
		GND GND
		O Negative
AES digital audio outputt	AES	WECO Audio connector
		O Positive
		GND GND
		O Negative
Optical input	No label	BSC-II (for SC input)
Sync input,	SYNC	BNC
Black&Burst or Tri-Level		

Table 2: Connector functions

Unused SDI inputs/outputs should be terminated with 75 Ohm.

Diode \ state	Red LED	Orange LED	Green LED	No light
Card status	PTC fuse has been triggered or FPGA loading has failed	FPGA loading. If more than a few seconds: DIPs 14+15 both set to the 'On' position, or module not programmed	FPGA loaded, module OK	Module has no power
SDI input status	Video signal absent	Video signal present but card not able to lock VCXO	Video input signal in lock	Module not programmed, or DIPs 14+15 both set to the 'On' position
Sync input status	Sync signal absent	Sync signal present but card unable to lock VCXO	B&B or Tri- level sync in lock	Module not programmed, or DIPs 14+15 both set to the 'On' position
Audio input status	No audio embedded in incoming video	One, two or three audio groups embedded in incoming video	4 audio groups embedded in incoming video	Module not programmed, or DIPs 14+15 both set to the 'On' position

3.3 What the LEDs mean

Table	3: L	.ED	states	and	what	thev	mean
			0.000	ana	minar		moun

3.3.1 Exceptions/special conditions for the LEDS

The *locate* command will make all four LEDs blink on and off synchronously to quickly identify the module in a larger installation. The operation of the card is not otherwise affected by the command, only the appearance of the LEDs will change. The LEDs will return to their normal states and functions after the special locate condition times out.

FPGA firmware upgrades will activate running lights after the firmware download has finished. Do not remove power to the card when running lights are active, the card is unpacking and installing the new firmware. The DAC-AVA-DMUX will automatically reboot after a successful upgrade, and the LEDs will then also return to their normal functions.

3.4 Selecting between Gyda mode or Manual mode

The board can be configured either either 'manually' (i.e. via DIP switches on the board itself) or via the system controller Multicon GYDA. Since there's a limited number of switches available compared to the total number of settings available for the module, only a subset of the parameters can be adjusted when operating in manual mode. Generally, the parameters that cannot be directly controlled by the DIP switches will take their settings from the previous Multicon GYDA session. This means that for a specific manual setup it may be necessary to configure the module with a Multicon GYDA before switching to manual mode.

To reach manual mode, the lower DIP (labeled OVR) on the module must be switched to the "On" position (to the right) and the board must be re-booted. This isolates the board from Multicon GYDA control, but the module will still accept commands to retrieve its status, and also the commands necessary to initiate and perform firmware upgrades.

In addition to the DIP switches, manual mode will also activate the rotary switch and the two push-buttons at the front of the module. These are used to control the phase delay for the sync-pulse generator.

3.5 A very brief guide to Multicon Gyda mode set-up

All of these settings are covered in more detail in chapter 4.3, 'Detailed control in Gyda mode'. These are just the most important settings to get started:

Arguably the most important setting is where to take the input from. If the module was purchased with the electrical input only, this would be a good starting point:

	Mode: 🗛 🔽 Main: E	Electrical 🔽	
Video in	Backup 1: 🛛 Video gen. 💌	Backup 2: - 💽 Latch: Rese	et
	Hold time: 500 ms	Lock time: 500 ms	

What this means is that the electrical input will be chosen whenever a signal is present, and if a signal is not present, the output will frame freeze for 500 ms before resorting to an internal fallback generator. Here this generator is set to produce just black video frames.

If the module was purchased with the optical input option, the setup could either be like above, or most likely the 'Optical' input would take the place of the 'Electrical' input in the illustration above. Alternatively, one input could serve as a backup for the other, with a final fallback to generator, as illustrated below:

	Mode: Auto 💌 Main: Optical 💌	-
Video in	Backup 1: Electrical 💌 Backup 2: Video gen. 💌 Latch: Reset	
	Hold time: 500 ms Lock time: 500 ms	

The rest of the settings on the configuration page either deal with setup of the frame synchronizer, or with the selection of formats for the module outputs. See chapter 4.3.7 for more detailed description of all the available options.

Once the input is taken care of, the output should be configured. The video DAC has three BNC outputs that can be configured to have these combinations (for SD output):

- CVBS/CVBS/CVBS
- CVBS/Y/C
- Y/Pb/Pr
- R/G/B

When the output is HD, the output setting will be overridden and the output will always be Y/Pb/Pr. For CVBS and S-Video the following modulations are available:

- PAL B/G
- NTSC
- PAL M
- PAL N

The board can handle 50Hz-based input signals as well as 60Hz-based (with and without pull-down) but it can't convert a 50Hz-based input to a 60Hz-based output and vice versa. The modulation setting is therefore split in two, one to select between NTSC and PAL M output for 60Hz-based sources, and one to select between PAL B/G and PAL N for 50Hz-based sources.

The Black setup ("pedestal") "On" or "Off" setting only applies to NTSC.

3.6 How to get back to factory defaults

To access the function that will reset the module and reload the factory default settings, the module must briefly be put into manual mode. The entire procedure is described in chapter 4.2.1.

4 Configuration

4.1 Selecting between Gyda mode or Manual mode

The board can be configured either 'manually' (i.e. via DIP switches on the board itself) or via the system controller Multicon GYDA. Since there's a limited number of switches available compared to the total number of settings available for the module, only a subset of the parameters can be adjusted when operating in manual mode. Generally, the parameters that cannot be directly controlled by the DIP switches will take their settings from the previous Multicon GYDA session. This means that for a specific manual setup it may be necessary to configure the module with a Multicon GYDA before switching to manual mode.

To reach manual mode, the lower DIP (labeled OVR) on the module must be switched to the "On" position (to the right) and the board must be re-booted. This isolates the board from Multicon GYDA control, but the module will still accept commands to retrieve its status, and also the commands necessary to initiate and perform firmware upgrades.

4.2 Detailed control in DIP switch mode

The two sets of DIP switches are labeled with a number running from 1 to 15. The 16th DIP is labeled *OVR*. Note that the left DIP switch of the horizontal DIP package is number 1. The top DIP switch of the vertical DIP package is number 9. Default settings as delivered from factory should be all DIPs in the Off position. The module will then be under Multicon Gyda control, see description of DIP switch 16 below.

Switch #	Function name	Function DIPs	Comment
1	SDI OUT 1	Off: processed mode On: through mode	In through mode the video goes through a re-clocker only.
2	SDI OUT 2	Off: processed mode On: through mode	In through mode the video goes through a re-clocker only.
3 - 4	Frame delay	DIP[3 4] = [Off Off] => 0 frames DIP[3 4] = [Off On] => 1 frames DIP[3 4] = [On Off] => 2 frames DIP[3 4] = [On On] => Previous setting preserved	These 2 DIPs control the Frame part of the video delay. For line and samples settings, see chapter 4.2.2 below. "Previous setting preserved": With DIPs in this position before the module is booted into manual mode; the module will keep the previous value set by Gyda.
5 - 6	SD video DAC format	DIP[5 6] = [Off Off] => CVBS DIP[5 6] = [Off On] => YPbPr DIP[5 6] = [On Off] => SVideo DIP[5 6] = [On On] => RGB	These two DIPs choose video DAC output format for SD output. Analog HD is always YPbPr.
7	SD video DAC	Off: PAL B/G + NTSC	Selection between

Table 4: DIP SWITCH FUNCTIONS

0			0
Switch #	Function name	Function DIPs	Comment
	modulation	On: PAL N + PAL M	PAL B/G and NTSC
			or PAL M and PAL N
			is automatic, based
			on video input.
8	Black setup	Off: Black setup for NTSC	For NTSC only.
	disable	On: No black setup	
9	Input priority	Off: Optical input has priority	This switch has no
		On: Electrical input has priority	effect for boards
			without the optical
			input (-R option).
10 - 11	Audio DAC and	DIP[10 11] = [Off Off] => Gr1	The 2 first of these 4
	AES group	DIP[10, 11] = [Off On] => Gr2	DIPS select one of
	, 120 gi o ap	DIP[10, 11] = [On Off] => Gr3	the de-embedded
		DIP[10, 11] = [On, On] = Gr4	groups. The next two
10			DIPs select a
12	Audio DAC	On: Ch2	channel pair (within
	Channel	(from colocted group)	this group) for the
10			
13	AES channel		for the AES output
		On: Ch2	roopostively
		(from selected group)	respectively.
		0% 4500	
14	AES/Dlink	Off: AES3 out on AES output	I he two slide
		On: Data link out on AES output	switches on the
			bottom side of the
			board must also be
			switched.
			See ch. 4.2.3below.
15	RESET	Off: Use values preset by GYDA	This DIP is only read
		On: RESET to factory defaults	during boot. The
			board will not start
			when DIP 16 and
			this DIP are both set
			to On. After returning
			the DIP to normal
			position, the card
			must be restarted
			and kept powered for
			a minimum of 10s to
			complete the reset
			The reset will only
			affect settings not
			nortaining to DIDa
			and the reterv
			and the rotary
10			SWITCH.
16	UVK		I NIS DIP IS ONLY read
		On: Manual mode	at power up.
			OVR is short term for
			GYDA override.

4.2.1 Factory reset function

A factory reset is a 3 step process:

- Set DIP 15 to 'on' and reboot the card. The Status LED will now stay orange, and the card will not complete the boot sequence.

- Remove power and set DIP 15 back to the normal position ('off')
- Power up the card once again. The operation of the card will immediately reflect the freshly loaded default settings. However, the card must be kept powered for at least 10 seconds to ensure that these settings are stored locally to be retrieved again at the next start-up. The card's operational environment must also be kept static during those 10 seconds (i.e. no change in incoming video standard, no commands issued). Failing to meet this requirement could result in an incomplete reset and require the user to start the factory reset sequence over again.

4.2.2 Rotary switch and push buttons

The *rotary switch*, labeled DLY, adjusts the phase delay from -5 to +4 video lines. It is only functional when a sync signal, black & burst or tri-level, is present at the sync input. The rotary switch is accessible from the front of the board.

The *push buttons,* labeled INC and DEC, are used to fine adjust the phase delay by samples. It can adjust $\pm \frac{1}{2}$ video line for the current video standard (or the last video standard the board was able to lock to). Pressing a button and keeping it pressed will accelerate the change. The LED adjacent to the button will flash for a short period of time when the end of the adjustment range has been reached. Pressing both buttons at the same time will return to the middle of the adjustment range, and the board will acknowledge by flashing the INPUT and SYNC LEDs simultaneously.

4.2.3 Slide switches

The two switches at the top of the module (rear side) switch between AES out and Data out. It DC couples the output signal when in DATA out mode, and AC couples the signal when in AES mode.

Note that to enable Data link output on the AES connector it is also necessary to set DIP 8 to the Off position when the board is in Manual mode (DIP 16 = On), or when the board is in Gyda mode (DIP 16 = Off), to select Data link over AES output in Gyda. Slide switches moved to the right routes out AES.

The switch on the left card edge switches between backplane sync input and Flashlink distributed sync (Future feature upgrade of Flashlink frame). Switch moved up routes the backplane sync to the card.



Figure 11: The figure shows a bottom view component printout of the board. Note the location of the slide-switches.

4.3 Detailed control in Gyda mode

4.3.1 Video DAC

The video DAC has three configurable outputs, with the following combinations available:

- CVBS/CVBS/CVBS
- CVBS/Y/C
- Y/Pb/Pr
- R/G/B

This setting only applies to SD video. When HD video is routed to the video DAC, the output will always be YPbPr. For CVBS and S-Video the following modulations are available:

- PAL B/G
- NTSC
- PAL M
- PAL N

The board can handle 50Hz-based input signals as well as 60Hz-based with and without pulldown, but can't convert a 50Hz-based input to a 60Hz-based output and vice versa. The modulation setting is therefore split in two, one to select between NTSC and PAL M output for 60Hz-based sources, and one to select between PAL B/G and PAL N for 50Hz-based sources.

It is also possible to turn black setup ("pedestal") on or off. This setting only applies to NTSC.

PAL Wide Screen Signaling (WSS) is also supported, and while the HD input is always 16:9, SD inputs can have WSS values already embedded. The user can select to strip off any existing WSS information by setting mode to Off, or to override the current WSS value by setting mode to On and specifying a new value, or set the mode to Auto. The Auto mode will signal 4:3 or 16:9 based on the aspect ratio bit in SMPTE 352M byte 3, or turn WSS off if no SMPTE 352M packages are available.

When specifying WSS values, the user should observe that the WSS value is really a 14-bit number with other information besides just aspect ratio. Aspect ratio is contained in the lower 4 bits, and the table below covers only those bits.

WSS value	Aspect ratio	Picture placement	Active lines
0+8=8	4:3	Full	576
1+0=1	14:9	Letterbox centre	504
2+0=2	14:9	Letterbox top	504
3+8=11	16:9	Letterbox centre	430
4+0=4	16:9	Letterbox top	430
5+8=13	>16:9	Letterbox deeper than 16:9	undefined
6+8=14	14:9	Full-height 4:3, framed to be "14:9-safe"	576
7+0=7	16:9	Full-height 16:9 (anamorphic)	576

Note the occasional "+8" in the first column above. It stems from the fourth aspect ratio bit, a parity bit over the first three.

4.3.2 De-glitcher

The de-glitcher corrects timing errors within a single video line. The de-glitcher has a 2048 samples buffer. When the first signal is present, we call it the "initial phase signal", data is taken from the centre of this buffer. If the timing reference of the video signal changes,

when for instance a new source being switched into the signal path, the timing errors occurring by this change will be corrected if the new timing reference is within +/-1024 samples of the "initial phase signal". This also goes for all consecutive timing references.

If a signal is more than +/-1024 samples off relative to the "initial phase signal", the output will repeat the last frame, refill the 2048 samples buffer and take out data from the centre of the buffer. This new signal is now considered the "initial phase signal". Audio will fade out when a frame repeat is being done, and fade in at the new frame.

Hence, it produces an error free video output without frame wrapping when the video input comes from a router with synchronous input video signals that all lies within +/-1024 samples of each other.

The de-glitcher output is always seamless. When a signal is repeated the audio is faded out. It fades in at the new frame.

4.3.3 Frame synchronizer

The frame synchronizer consists of a frame store buffer and some control logic. The frame store buffer can store up to 8 full HD frames. Data is fetched from this buffer according to the user settings by force of the control logic. The control logic sets the frame synchronizer into different modes dependent on the presence of a sync input.

4.3.4 Frame synchronizer in 'Frame sync' mode

If a sync input (B&B or Tri-level) is present, the frame synchronizer will output a signal that has a delay relative to this signal. Two parameters can be set: "**Phase delay**" and "**Frame delay**".

Phase delay	0	lines	0	samples	
Video frame delay	2	frames			



Let us first focus on the *phase delay*, which also may be called "output phase delay". This parameter can be positive or negative, and determines the relationship between the outgoing video and the sync signal.

The *phase delay* can thus be written in several ways, a large positive delay will equal a small negative delay, because there is wrap-around on a frame basis. It follows that it is not useful to specify a *phase delay* larger than 1 frame. Strictly speaking the range could have been limited to -1/2 frame to 1/2 frame. For convenience, the delay range is allowed to be from -1 frame + 1100 samples to 1 frame – 1100 samples.

In addition to the *phase delay,* the user may specify additional frames delay. When *frame delay* is set to 1 frame, the delay through the card will be between 1 and 2 frames, depending on the input phase between SDI-input and sync input.

The frames and lines are measured in units of the output SDI video standard. If the output SDI standard is 1080i25, a delay of one line is equal to 35.5us. If the output SDI standard is 720p50, a delay of one line is equal to 26.6us. If the output SDI standard is 625i25, a delay of one line is equal to 64us.

For a scenario where the card receives different HD video standards, (e.g. 1080i25 and 720p50) the user may want to conserve a specific delay in microseconds for all HD video standards. This is accomplished by specifying the delay in number of samples instead of frames and lines. (For HD video standards the sample frequency is equal over standards, but the line and frame frequencies are different for the different standards).

If video input disappears

Given that stable SDI input and sync input exists: If the SDI input disappears, the picture will freeze for *<hold time>* and then go to video generator if the card is in default configuration.

If video input reappears

Given stable sync input, the video will reappear after *<lock time>* of locked video input if card is in default settings.

If sync input disappears

Given that stable SDI input and sync input exists: If the sync signal disappears, the card will act as in frame delay mode, see chapter 4.3.5.

NOTE: This will result in a frame roll as the delay changes.

If sync input reappears

Given that a stable SDI input exists: If the sync signal reappears the delay mode will change back to Frame Sync mode. Hence the internal clock will be locked to the sync signal and the delay will again change.

NOTE: This will result in a frame roll as the delay changes.

If both signals disappear

The picture will first freeze for *<hold time>* and then go to video generator. The output is now referenced to the local clock source. However, this clock source will be kept within 1 ppm of the last sync source.

4.3.5 Frame synchronizer in 'Frame delay' mode

In this mode a sync signal is not present. The phase delay will now be relative to the SDIinput. The phase delay + additional frame delay together set the total video delay.

If video signal disappears

The picture will first freeze *<hold time>* and then go to video generator. The output is now referenced to the local clock source. However, this clock source will be kept within 1 ppm of the last video source.

If video signal reappears

If the input video signal reappears, the video will reappear on the output *<lock time>* after stable input video. The delay will be set to the same delay as before losing input.

NOTE: This may cause a frame roll.

If a sync input appears

Given that a stable SDI input exists: If a sync signal appears the delay mode will change to Frame Sync mode, see chapter 4.3.4. Hence the internal clock will be locked to the sync signal and the delay will again change.

NOTE: This will result in a frame roll as the delay changes.

4.3.6 Relative audio delay

An audio delay relative to the video output can be specified for all de-embedded channels at once. This is done in Multicon GYDA. The audio delay is specified in audio samples relative to the output video, and can be both positive and negative. The negative audio delay is limited by the positive video delay.

Note that as the audio delay is relative to the video output, it's possible to specify an audio delay that will be an actual negative delay, i.e. request that audio will be output before the video containing those audio samples has arrived. This will inevitably cause audio errors.

Since the audio delay is always relative to the video, the only way to give the audio a negative delay is to delay the video by a positive amount. To go beyond this limit would require the audio to be re-embedded before it had even been de-embedded from the incoming video, and that is of course impossible.

The positive audio delay is limited by the fact that the sum of the video delay and the relative audio delay cannot be larger than 32000 audio samples (approx. 0.67 ms with 48 kHz audio). If the video delay is set to minimum, the full 32000 audio samples will be available, but if the video delay is set to – say – 5 frames, the maximum relative audio delay is reduced to 20000 audio samples (assuming 25 frames per second, 5 frames equals 0.2 seconds, which in turn equals 12000 audio samples, and 32000-12000=20000). When doing these calculations, remember that if a sync reference is present, a video delay setting of N frames means that the actual video delay can vary continuously between N and (N+1) frames. The calculations should therefore be based on (N+1) frames.

|--|

Figure 13: Multicon GYDA view of the relative audio delay setting

4.3.7 Video input selection

The DAC-AVA-DMUX has one electrical and one (optional) optical input. The input can be chosen either by an automatic selection with priorities and rule of switching, or by direct manual selection. When the input selection is done manually from the Mode menu, no fallback to other sources is available, but there will be a *frame freeze* for as long as the input is gone.

	Mode:	Electrical	Main:	Electrical 🔽			
Video in	Backup	Auto 🌱 Electrical	n. 💌	Backup 2: 🔤	T	Latch: Reset	
	Hold tir	Optical Video non		Lock time: 500	ms		
		Mute Mute -					

Manual selection mode



Automatic selection mode

	Mode: Auto 💌	Main:	Optical 🛛 💌		•
Video in	Backup 1: Electrical	•	Electrical Optical	Video gen. 💌	Latch: Reset
	Hold time: 500 ms		Video gen. 🗟	500 ms	
			-		

Figure 15: Multicon GYDA view of the input selection

If the *Video in Mode* choice is set to auto in Multicon GYDA, three input choices (priorities) can be made. The available choices are electrical, optical, internal generator, muted, or '-' (none). When the signal is missing on the input selected as 'Main', the change-over logic will switch to the next priority and look for a signal there, and so on. If the user doesn't want to use all three priority levels, the unused ones can be set to '-'. Should the user specify a list of priorities where it is actually impossible to reach one or both of the backup levels

(because the main input is selected to be an internal generator, and therefore always present), the card will also display the unreachable levels as '-'.

The switching is always latching, and to get back to the main input while the other input is still present, the user must press *Reset*. Note that if the fallback also disappears, the module will start searching at the main input again.

Hold time and lock time can also be adjusted. They specify how long a signal can be missing before the next input in the prioritized list is attempted, and how long a lost signal has to be present before it is considered OK again, respectively.

4.3.8 Video generator

The video generator can produce several simple signals: Color bar, Color bar with a moving box, Check field and Flat field.

The flat field feature is controlled by setting the luma and chroma values (each is a 10bit value, 0-1023), or by selecting one of the pre-defined colors (black, white, yellow, cyan, green, magenta, red, or blue).

By default he generator is selected as the video source if there is no video signal present at either of the video inputs. The video standard will then be determined by the legal video input last seen by the card. *The Video format selector has no effect in this mode.*

The generator may also be forced on from Multicon GYDA by selecting the video generator as main input in Video in. The video standard is then determined by the Video format selector. This selector will override video input but the internal generator will still be locked to the input signal. In other words: For correct generator output in this mode, the input must either be missing or the input must be of the same frequency base as the selected output standard.

Video generator	Video format:	720/50p	-				
	Pattern:	Black	-	O Flat: Y: 0	Cb: 0	Cr: 0	

Figure 16: Multicon GYDA view of the video generator

4.3.9 Video processing

The video processing block consists of a *gain and offset* adjustment, and a video payload *legalizer*.

Video processing	Legalizer: 💿 On	○ Off		•
		Y	Cb	Cr
	Gain:	1.0000	1.0000	1.0000
	Offset:	0.0000	0.0000	0.0000

Figure 17: Multicon GYDA view of the video processing block

4.3.9.1 Gain and offset

The gain and offset adjustments are done separately for the Y, Cb and Cr samples.

Range Multicon GYDA

Luma gain	0 – 3.9999
Chroma gain	0 – 3.9999
Luma offset (gain =1)	511.75 – 511.75 in sample values
Chroma offset (gain = 1)	255.75 - 255.75 in sample values

4.3.9.2 Video payload legalizer

The legalizer hard clips the upper and lower limit of the video payload. With the legalizer enabled these limits are:

Upper limit	Luma:	3ACh		
	Chroma:	3C0h		

Lower limit Luma: 040h Chroma: 040h

With the legalizer disabled the video processing block hard clips both luma and chroma to 3FBh and 004h.

4.3.10 SDI output selectors

The board has four outputs organized as two pairs, each consisting of one inverting and one non-inverting output. The signal to each of these two pairs can be routed either directly from the re-clocker ("Through") or from the audio/video processing unit ("Processed").

SDI out 1	Main: Through Processed
SDI out 2	Main: Through C Processed

Figure 18: Multicon GYDA view of SDI output selection block

All features that requires modification of the video content (video generator, label overlay, etc.) requires that the output is set to Processed. Note that when the internal video generator is selected (either because it was selected as main in Video in, or because it was selected as fallback for a missing input), outputs set to Through will behave as if Mute was selected.

4.3.11 EDH processing block

If enabled, the EDH processing block extracts the EDH package from the video, updates the EDH flags according to SMPTE RP165 and inserts the EDH package into the ancillary data of the video.

If disabled, The EDH processing block only reads, processes and reports the EDH package without changing it in the video stream.

4.3.12 Signal integrity

The DAC-AVA-DMUX module can detect a number of errors in incoming video, and in some cases also correct them. Each type of error has its own bit in what is known as an error mask, and the user can select which of the errors will be ignored and which will be counted in the error counter. This error counter is in turn the Multicon tool to raise alarms if the maximum error rate is exceeded. The types of errors that are detected and counted are shown dynamically on the module's Information page.

Signal integrity	Max error	rate:	10	errors/s	S	Max en	ror count:	250	error	s	Alarm	hold tin	ne: 60	s	▼
	Error mask	APV	FFV	NO_EDH	VS	FF-CRC	AP-CRC	LOCK	CCS	YCS	CCRC	YCRC	LNUM	SAV	EAV
	Count:			•	۲	۲	•	۲	۲	۲	۲	۲	•	۲	۲
	Ignore:			0	0	0	0	0	0	0	0	0	0	0	0

Figure 19: Multicon GYDA view of the signal integrity block

The error types that the module can detect are:

NO_EDH: No EDH flags detected

VS: SMPTE-352M package and the video frame are not consistent

FF-CRC: Full-frame checksum error

AP-CRC: Active picture checksum error

LOCK: Can't lock to incoming video standard

CCS / YCS: Checksum error in ancillary data packets, Y or C data space.

CCRC / YCRC: Line checksum error, Y or C (HD only)

LNUM: Unexpected line number sequence (HD only)

SAV: Unexpected occurrence of Start-of-active-video flag

EAV: Unexpected occurrence of End-of-active-video flag

4.3.13 Label generator

The label generator consists of 2 lines of 16 characters each that are placed at the lower left corner of the active area.

The "On" tick-box will show the label at all times, while the "Off" will turn the label generator off at all times. If "Auto" is ticked, the label will be shown as an overlay on the internal video generator only. Typically, the internal video generator will be used as a fallback for the physical video inputs, and hence this feature provides a means to identify the card with the missing input in a long chain of cards.

Note that in order to see the label on an output, the video output selector must be set to 'Processed' for the output in question.

Label generator	○ Enable	to St	Style: White, normal 💌			
	VIDEO					
	LABEL					

Figure 20: Multicon GYDA view of the label generator

The label can be shown in black or white, and in two different sizes. One of these four combinations can be selected as the 'Style' for the label.

4.3.14 Audio overview



Figure 21: Audio function block

4.3.15 Audio de-embedder

The Audio de-embedder extracts all audio embedded in the video stream. The deembedder is always enabled when the input is HD. When the input is SD and the board operates as an SD frame synchronizer, embedding can be globally disabled. The effect is to leave the SDI stream unaltered, except for repeated or removed video frames.

4.3.16 Audio delay

An audio delay can be specified relative to the video output. It is situated before the audio cross point matrix and is common for all de-embedded channels. See chapter 4.3.6, 'Relative audio delay'.

4.3.17 Audio cross point matrix

The audio cross point matrix is a 10x10 cross point with inputs and outputs as shown in **Error! Reference source not found.** The 8 de-embedded channels, a 1 kHz sine and "black sound" are selectable inputs. "Black sound" is explained in chapter **Error! Reference source not found.** The outputs of the cross points are 8 stereo channels for re-embedding, one analog audio output and one AES output.

4.3.18 Audio fallback options

The 10 output channels from the cross point matrix have configurable fallbacks, used when their corresponding matrix inputs are missing. A common fallback setting is used for all eight re-embedded channels, whereas the audio DAC channel and AES out have their own independent fallback settings. The priorities can be selected between *matrix* (being the selected channel in the cross point matrix) or the internally generated *sine* or *black sound*.

4.3.19 Audio generator

The stereo audio generator is available as an input to the audio cross point matrix, and as a fallback option. There are therefore three slightly different ways to select the generator: select it in the matrix directly, select it as the first priority under audio fallback, or to set it as second priority behind a missing input.

The generator signal is a high purity 1 kHz sine wave with a 250ms interruption on the left channel every 3 seconds. The audio level may be set to one of two standards. The two levels are -18 dBFS and -20 dBFS. These two levels correspond to EBU R68 and SMPTE RP155.

4.3.20 Audio processing block

The output of each stereo signal from the audio cross point matrix may be manipulated in the audio processing block (LL, RR, LR, RL !LR, L!R, (L+R)/2, MS).

The stereo signals may be output in one of the following ways:

- LR, Left / Right Normal, no change.
- RL, Right/ Left Channels are swapped.
- LL, Left/ Left Left Left channel is copied into the right channel.
- RR, Right/ Right Right channel is copied into the left channel.
- !LR, ØLeft/ Right The left channel is phase inverted.
- L!R, Left/ ØRight The right channel is phase inverted.
- MM, (Left + Right)/2 The left and right channels are summed.
- MS, MS/AB The left and right channels are converted from AB stereo to MS stereo.

4.3.21 Audio embedder

The audio embedder can be enabled/disabled per group. When a group to be embedded is disabled the audio inside that group is removed.

A 24-bit audio signal uses the Extended Audio Data Packet for the 4 least significant bits. Not all equipment can handle Extended Audio Data Packets correctly, so the option exists to truncate all audio data to 20 bits. **This setting is common for all embedded channels.**

The insertion of Audio Control Packages can also be switched on and off. **This setting is also common for all embedded channels.**

For SD input (i.e. operation as a frame synchronizer) the audio embedder can also be switched off all together. In this state all audio embedded on the input signal is left unchanged.

4.3.22 Analog audio output

The level of the analog audio output can be adjusted in GYDA. The minimum step is 0.5dB (input will be rounded to nearest 0.5dB) and the range is from -95.5dBu to 24dBu. It is also possible to mute the output completely.

General environmental requirements for Nevion equipment

- 1. The equipment will meet the guaranteed performance specification under the following environmental conditions:
- Operating room temperature range: 0°C to 45°C
- Operating relative humidity range: <90% (non-condensing)
- 2. The equipment will operate without damage under the following environmental conditions:
 - Temperature range:
- -10°C to 55°C
- Relative humidity range: <95% (non-condensing)

Product Warranty

The warranty terms and conditions for the product(s) covered by this manual follow the General Sales Conditions by Nevion, which are available on the company web site:

www.nevion.com

Appendix A Materials declaration and recycling information

A.1 Materials declaration

For product sold into China after 1st March 2007, we comply with the "Administrative Measure on the Control of Pollution by Electronic Information Products". In the first stage of this legislation, content of six hazardous materials has to be declared. The table below shows the required information.

	Toxic or hazardous substances and elements							
組成名稱 Part Name	鉛 Lead (Pb)	汞 Mercury (Hg)	镉 Cadmium (Cd)	六价铬 Hexavalent Chromium (Cr(VI))	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)		
DAC-AVA-DMUX+ / DAC-AVA-DMUX-R+	0	0	0	О	0	0		

O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.

X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.

This is indicated by the product marking:



A.2 Recycling information

Nevion provides assistance to customers and recyclers through our web site <u>http://www.nevion.com/</u>. Please contact Nevion's Customer Support for assistance with recycling if this site does not show the information you require.

Where it is not possible to return the product to Nevion or its agents for recycling, the following general information may be of assistance:

- Before attempting disassembly, ensure the product is completely disconnected from power and signal connections.
- All major parts are marked or labeled to show their material content.
- Depending on the date of manufacture, this product may contain lead in solder.
- Some circuit boards may contain battery-backed memory devices.