Digilent Plug-in for Xilinx 12.x Tools User Manual

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Overview

The Digilent Plug-in for Xilinx tools allows Xilinx software tools to directly use the Digilent USB-JTAG FPGA configuration circuitry. For 12.x, Xilinx Impact, Chipscope Pro, EDK Xilinx Microprocessor Debugger (XMD) command line mode, and EDK Software Development Kit (SDK) are currently supported by the Plug-in. Refer to http://www.xilinx.com/ for more information about these Xilinx design tools. Demonstration Designs for the Nexys2 and Basys2 boards are provided to verify correct operation of the plug-in.

Software Versions Tested:

Xilinx ISE Design Suite Version 12.x only (Refer to <u>http://www.digilentinc.com/</u> for versions of the plugin for later Xilinx ISE versions)

Digilent Adept System 2.4 (or Digilent Runtime 2.3 for Linux) or greater Supported Operating Systems:

- Microsoft Windows 32-bit and 64-bit Operating Systems
- Linux: Red Hat and CentOS 4.8, 5.4 (x86/x64), and SUSE 11.2 (x86/x64)

Windows Installation

To begin, ensure that the Xilinx ISE Suite (12.x only) and Digilent Adept System 2.4 (or greater) is installed on the host computer. The Plug-in files "libCseDigilent.dll" and "libCseDigilent.xml" must be copied into the ISE Design Suite installation.

For the ISE Design Suite, the typical location is C:\Xilinx\12.1\ISE_DS\ISE\lib\nt\plugins\Digilent\libCseDigilent Note: For 64-bit Windows, use nt64 in place of nt





Linux Installation

To begin, ensure that the Xilinx ISE Suite (12.x only) and Digilent Adept Runtime 2.3 (or greater) is installed on the host computer. The Plug-in files "libCseDigilent.so" and "libCseDigilent.xml" must be copied into the ISE Design Suite installation.

For the ISE Design Suite, the typical location is **\$XILINX/lib/lin/plugins/Digilent/libCseDigilent** Note: For 64-bit Linux, use **lin64** in place of **lin**

Nexys2 Demonstration Project

The Nexys2 Demonstration Project can be used to verify correct installation and operation of the Plugin.

Chipscope Pro Setup

The Nexys2 Demonstration Project is a Xilinx EDK design with an embedded Chipscope Pro Virtual IO module. Refer to <u>http://www.xilinx.com/</u> for more information about these Xilinx design tools.

Launch Chipscope Pro Analyzer and Select the "JTAG Chain→Open Plug-in..." menu item.

🗐 ChipSco	pe Pro	Analy	zer [nev	v projectj]
<u>F</u> ile ⊻iew	JTAG	Chain	<u>D</u> evice	<u>W</u> indow	<u>H</u> elp
to e		Server	<u>H</u> ost Set	ting	
New Project		JTAG (Chain <u>S</u> et	up	
JTAG Chain	able				
	0	Xilinx F	Platform <u>U</u>	<u>J</u> SB Cable	
	۲	<u>O</u> pen l	Plug-in		
		<u>C</u> lose	Cable		
		Get Ca	ible <u>I</u> nforr	mation	
		<u>A</u> uto C	ore Statu	s Poll	

Type "digilent_plugin" into the dialog box:

ChipSco	pe Pro Analyzer [new project] Open Plug-in	
?	Plug-in Parameters digilent_plugin	4
	OK Cancel	

Chipscope Pro Analyzer will automatically detect the devices on the Nexys2 board:



ChipScop	oe Pro Analyzer				×			
_E JTAG C	hain Device Order:							
Index	Name	Device Name	IR Length	Device IDCODE	USERCODE			
0	MyDevice0	XC3S500E	6	41c22093				
1	MyDevice1	XCF04S	8	f5046093				
Advanced >>								
	Ok	Cancel	Read US	ERCODES				

Right Click on "MyDevice0 (XC3S500E)" and select "Configure...":

New Pr	oject							
JTAG Chain								
- DE\	/:0 MvDevice0 (XC3S500E)							
- DE/	<u>R</u> ename							
	<u>C</u> onfigure							
	Show IDCODE							
	Show <u>U</u> SERCODE							
	Show Configuration Status							
	Show JTAG Instruction Register							

Select the "download.bit" file in the nexys2\binaries directory:



ChipScope Pro A	Analyzer [new project]	X					
_JTAG Configura	tion						
File:	download.bit						
Directory:	C:\Digilent\nexys2\binaries						
	Select New File						
	n-level CDC File peration cannot be undone.)C File						
🔲 Auto-c	Auto-create Buses						
File:	File:						
Directory:	C:\Digilent\nexys2\binaries						
	Select New File						
	OK Cancel						

After selecting "OK", Chipscope Pro Analyzer will configure the FPGA with the "download.bit" configuration file. After successful configuration, the Yellow "Done" LED should be light on the Nexys2 board. The GUI will show there is one VIO Console device attached:



Double Click on the "VIO Console" item which brings up that window:



👹 VIO Console - DEV:0 MyDevice0 (XC3S500E) ¤ ⊂ ☑ 🛛						
Bus/Signal	Value					
AsyncIn[0]	0					
-AsyncIn[1]	0					
-AsyncIn[2]	0					
-AsyncOut[0]	0					
-AsyncOut[1]	0					
-AsyncOut[2]	0					
-AsyncOut[3]	0					
-AsyncOut[4]	0					
-AsyncOut[5]	0					
-AsyncOut[6]	0					
AsyncOut[7]	0					

Press BTN3 on the Nexys2 board and notice the VIO Console displays that action.

🏽 VIO Console - DEV:0 MyDevice0 (XC3S500E) 🗗 🗹					
Bus/Signal	Value				
AsyncIn[0]	0				
-AsyncIn[1]	0				
-AsyncIn[2]	1 1				
-AsyncOut[0]	0				
-AsyncOut[1]	0				
-AsyncOut[2]	0				
-AsyncOut[3]	0				
-AsyncOut[4]	0				
-AsyncOut[5]	0				
-AsyncOut[6]	0				
AsyncOut[7]	0				

The AsyncOut values are connected to the 8 LEDs on the Nexys2 board. Click on any of the Value cells to change their contents. The following configuration lights up 4 LEDs in a row:



👹 VIO Console - DEV:0 MyDevice0 (XC3S500E) ¤ ⊂ Z 🛛						
Bus/Signal	Value					
AsyncIn[0]	0					
-AsyncIn[1]	0					
-AsyncIn[2]	0					
-AsyncOut[0]	1					
-AsyncOut[1]	1					
-AsyncOut[2]	1					
- AsyncOut[3]	1					
-AsyncOut[4]	0					
- AsyncOut[5]	0					
-AsyncOut[6]	0					
AsyncOut[7]	0					

Close Chipscope Pro Analyzer. This concludes the Chipscope Pro part of the Demonstration Project. While only the Virtual IO Console was used in this design, any Chipscope Pro module can be utilized to assist in debugging the design.

Xilinx Microprocessor Debugger (XMD) Setup

The Plug-in can also be used with Xilinx Microprocessor Debugger (XMD) command line mode. By adding the option "-cable type xilinx_plugin modulename digilent_plugin" to commands which interface with the hardware, XMD will utilize the Plug-in.

Note: Answer Record #35580 contains an updated XMD version for 12.1: <u>http://www.xilinx.com/support/answers/35580.htm</u>

Here is an annotated example iteration. Launch the EDK Bash Shell and type the following commands in **bold**.

www.digilopting.com		nore 6 of 10
XMD% XMD% fpga -f download.bit -cable type	xilinx_plugin modulename	digilent_plugin
Copyright (c) 1995-2009 Xilinx, Inc.	All rights reserved.	Configure FPGA
Xilinx EDK 12.1 Build EDK_MS1.53d	(
Xilinx Microprocessor Debugger (XMD)	Engine	
\$ xmd		
~ /cygdrive/c/digilent/nexys2/binarie		
<pre>\$ cd /cygdrive/c/digilent/nexys2/bina</pre>	Launch xmd	
~		
Copyright (c) 1995-2010 Xilinx, Inc.	All rights reserved.	
Xilinx EDK 12.1 Build EDK_MS1.53b		
Xilinx Bash Shell		

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Fpga Pro	gramming Prog	ress	Done				
JTAG cha	in configurat	ion			(
Device	ID Code	IR Lengt	ch Pa	art Name		Connect to Microblaze	
1 2	41c22093	6 8		C3S500E CF04S		Processor I	
Ζ	£5046093	0	X	JE 045			sobug port
	ully download nect mb mdm -			_plugin m	odulename	digilent_p	lugin
MicroBla	ze Processor (Configurati	lon :				
Version. Optimiza Intercom MMU Type No of PC No of Re. No of Wr. Instruct. Data Cacl Exception FPU Supp Hard Div. Hard Mul	tion nect Breakpoints. ad Addr/Data M ite Addr/Data ion Cache Supp he Support ns Support port ider Support. tiplier Support.	Watchpoints Watchpoint port	7.20 Area PLBv 0	a v 46 MMU			
	hifter Suppor set Instructio						
Compare	Instruction St	upport	on				
Data Cacl	he Write-back	Support	off	ſ	Download	d Program	
Starting	d to "mb" tare GDB server fo executable.e	or "mb" tar		d	executabl	•	
	eset DONI						
	ing Program section, .vec section, .vec section, .vec section, .tex section, .tex section, .ini section, .fin section, .roda section, .dat section, .dat	tors.reset: tors.sw_exc tors.intern tors.hw_exc t: 0x000000 t: 0x000000 tat: 0x00000 ta2: 0x00000 ta2: 0x00000 frame: 0x00000 frame: 0x00007 0x000007 0: 0x000007 ck: 0x00000	: 0x0000 ception cupt: 02 ception 050-0x00 500-0x00 0062c-02 00662-02 0000788-02 0000788-02 0000788-02 0000000000000000000000000000000000	: 0x00000 x000005eb 000060f 000062b x00000661 x00000667 0000777 0000077f 00000787 -0x000007 00078f 0007b3 00009b7 00000db7 0x0000000	008-0x000 -0x000000 020-0x000	13 00023	1
XMD% rea	d_uart d to MDM UART	Target		Display	UART outp	out in XMD	J
XMD% con	XMD% Ente:	ring main()		Start Mi	croblaze E	xecuting]
Exiti	ng main()	Ling main()		Stop Mic	roblaze Ex	ecution	
XMD% sto XMD%	p			Display I	Microblaze	registers	
www.digile	entinc.com						page 7 of 12

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XMD% rrd							
r0: 00000000	r8:	00000000	r16:	00000000	r24:	0000000	
r1: 00000d88	r9:	00000000	r17:	00000000	r25:	0000000	
r2: 00000668	r10:	00000000	r18:	00000000	r26:	0000000	
r3: 0000000	r11:	00000000	r19:	00000000	r27:	0000000	
r4: 00000000	r12:	00000000	r20:	00000000	r28:	0000000	
r5: 0000000	r13:	00000790	r21:	00000000	r29:	0000000	
r6: 0000000	r14:	00000000	r22:	00000000	r30:	0000000	
r7: 00000000	r15:	000003a8	r23:	00000000	r31:	0000000	
pc: 000006c	msr:	00000000					
XMD% mrd 0x81400000	\sim	S Read	the value	s of the 8 S	lide Swite	ches via GPIO	
81400000: 00000069		Ticuu					
XMD% mrd 0x81400000	<	Monually	Change	the Clide C	witch noo	itiana and ra read the vel	
81400000: 00000095	l	wanuany	Change	the Slide Sl	which pos	itions and re-read the val	ues
XMD% exit							

^{~ /}cygdrive/c/digilent/nexys2/binaries

This concludes the Xilinx Microprocessor Debugger (XMD) part of the Demonstration Project.

Impact Setup

Xilinx Impact is used to download FPGA bitstreams to FPGA boards. The following steps show how to use Impact with the Plug-in. First, launch Impact and Select "Output→Cable Setup…" menu item.

😺 ISE iMPACT (M. 53d) - [Bour	idary Scan]	
🛞 File Edit View Operations	Output Debug Window Help	- 8 ×
i 🗋 ờ 🔒 i 🔓 📾 💥 🛱	Cable Auto Connect	
MPACT Flows Boundary Scan SystemACE Create PROM File (PROM File	Disconnect All Cables SVF File	
iMPACT Processes	STAPL File XSVF File ↔ □ □ □ ×	
Available Operations are:		
	Boundary Scan 🔀	
Console		⇔⊡₽×
Cable connection fail PROGRESS_END - End Op Elapsed time = 3		× • • • • • • • • • • • • • • • • • • •
	Varnings	/
Examine and change cable communical		en [[[.:

Select "Open Cable Plug-in" and type in "digilent_plugin":



😓 Cable Communication Setup 🛛 🛛 🔀				
Communication Mode				
O Parallel Cable III				
Parallel Cable IV				
	Advanced USB Cable Setup			
TCK Speed/Baud Rate:	Port:			
Default Speed 🛛 😽	~			
Cable Location				
Local Remote Host Name:				
Cable Plug-in				
✓ Open Cable Plug-in. Select or enter	a Plug-in from the list below:			
digilent_plugin				
OK Car	Help			

Right Click in the "Boundary Scan" window to "Initialize Chain":

🐉 ISE iMPACT (M.53d) - [Boundary Scan]					
🐼 File Edit View Operations Output Debug Window Help		- 8 ×			
i 🗋 ờ 🛃 i 🕼 🛱 i 🗟 🖬 i 🥕 🕅					
IMPACT Flows ↔ □ 日 ×					
Boundary Scan SystemACE Create PROM File (PROM File Formatter) Right click to Add Device o	r Initialize JTAG chain				
IMPACT Processes ↔ □					
Available Operations are:	Add Xilinx Device Add Non-Xilinx Device	Ctrl+D Ctrl+K			
	Initialize Chain	Ctrl+I			
Boundary Scan 🗵	Cable Auto Connect Cable Setup				
Console	Output File Type	► ×			
<pre>UNFO:iMPACT - Digilent Plugin: Firmware Version: 0303 UNFO:iMPACT - Digilent Plugin: JTAG Port Number: 0 UNFO:iMPACT - Digilent Plugin: JTAG Clock Frequency: 1600000 Hz</pre>					
		>			
Config	uration Onboard USB 160	0000			

Impact is now ready to communicate with the FPGA on the board:





EDK Software Development Kit (SDK) Setup

The following steps show how to use the EDK Software Development Kit (SDK) with the Plug-in. First, launch SDK and Select "Xilinx Tools \rightarrow Configure JTAG Settings" menu item.





Select "3rd Party Cable, Xilinx Plug-in" and type in "-cable type xilinx_plugin modulename digilent_plugin" into the "Other Options:" field.

🐵 Configure J	ITAG Settings		
Configure JTA	\G Settings		***
	5 cable to use for communication and 3 iffect how XMD connects to the FPGA.		the target board.
JTAG Cable			
Туре:	3rd Party Cable, Xilinx Plug-in 🔽		
Port:			
Frequency:	~		
Other Options:	-cable type xilinx_plugin modulename	e digilent_plugin	
	ain / Discover Devices on JTAG Chain iguration of JTAG Chain		
FPGA? D	evice Name	ID Code	IR Length
?			OK Cancel

SDK is now setup to use the Plug-in to communicate with the FPGA on the board.

Basys2 Demonstration Project

The Basys2 Demonstration Project can be used to verify correct installation and operation of the Plugin. It is functionally equivalent to the Nexys2 design. Please follow the procedure documented in the Nexys2 Demonstration Project section above.