Unistep LabMaster Series

PLL

PHASE-LOCK LOOP MODULE

USER MANUAL

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USER MANUAL

1. INTRODUCTION

The PLL module is designed to function as a versatile platform that can be used to experiment with many aspects and applications of the basic PLL circuit. The module has an on-board reference oscillator, a prescaler, phase comparators, a VCO, and a divide-by-n counter. The complete circuit is fundamentally very similar to the ones used in all present-day frequency synthesized receivers and transmitters with digital tuners. The circuit can be configured as a frequency synthesizer to synthesize the actual short-wave broadcast frequencies between the 120m – 11m bands. With an external signal generator, PLL operation can be observed and analyzed in the entire 1 MHz - 20 MHZ band.

1.1 Features

- On-board oscillator and reference frequency generator
- Provision for generating various reference frequencies
- Choice of two phase comparators (X-OR and J-K flip-flop edge detector)
- Lock detector with indicator and pulse discriminator
- VCO with excellent frequency linearity
- Basic PLL operation between ~20 Hz - 25 MHz
- External signal input with gating control for analyzing step response of the PLL circuit
- Socketed passive components for reconfiguring PLL parameters
- Demodulator output for detailed analysis of the circuit behaviour
- Full control of center frequency and PLL lock, capture, and other loop response properties
- Fully configurable divide-by-n counter for frequency synthesis applications
- Reverse polarity input power protection
- Fully socketed IC's for ease of repairs and maintenance

1.2 Package Contents

Please make sure that you have the following items in the ICL package:

1. The PLL Module (1)
2. User manual
3. Documentation CD

2. CIRCUIT DESCRIPTION

2.1 Schematic Diagram

Full circuit diagram is included at the end of this manual. You may find it useful to keep it open while reading the following sections about the circuit details.

2.2 Circuit Operation

We can analyze the operation of the PLL circuit as several functional blocks:

- Reference Oscillator and Prescaler
- Phase Comparator
- VCO
- Input Signal Gating
- Divide-by-N Counter
- Power Input

Reference Oscillator and Prescaler

U1 IC works as the master oscillator and the first stage prescaler. The 5.120 MHz oscillator frequency is divided down to obtain the reference signal. A bank of jumper pins, JP1, allows tapping the U1 divider chain at different points to obtain different reference signals as follows:

JP1-1 20.00 kHz
JP1-2 10.00 kHz
JP1-3 5.00 kHz
JP1-4 1.25 kHz

The last stage of the prescaler is a divide-by-two circuit inside the U5 IC. This final stage can be bypassed by using the JP2 jumper.

JP2-1 Stage-2 bypass
JP2-2 Stage-2 include

Phase Comparator

The two phase comparators are housed inside the U2 IC. These two comparators share a common signal input path, but the output to be fed to the VCO input can be selected by using the JP5 jumper block:

JP5-1 PC2, J-K Flip-Flop edge detector comparator in use
JP5-2 PC1, X-OR phase comparator in use

Since the X-OR phase comparator needs a 50% duty cycle wave shape both at the reference input and also at the signal input, the second half of the U5 is included in the phase comparator circuitry to help obtain the required duty cycle on the signal input. Input of the this divide-by-2 Flip-Flop circuit is always from the divide-by-n counter stage, but its output signal can be included in the feedback signal path by using the JP4 jumper block.

To facilitate straight PLL experiments that do not use the divide-by-n counter section, again the JP4 jumper block can be used to bypass this counter and feed VCO output directly into the phase comparator.

Here is a list of what can be fed into the phase comparator circuit by using the jumper selection of the JP4 jumper block:

JP4-1 Output from VCO
JP4-2 Output from the divide-by-n stage
JP4-3 Output of divide-by-n + divide-by-2 circuits (divide-by-n+1?)

The lock detect function is obtained by feeding the LD (Lock Detect) signal from the phase comparator to the pulse detector circuit built with the U7 IC. When the PLL circuit is acquiring lock, a stream of pulses that steer the internal charge pump circuit are also available at this output. When the PLL acquires lock, no more pulses are generated, and the U7 circuit detects this condition to turn on the Lock Detect indicator LED, D19.

Voltage-Controlled Oscillator

The VCO section of the PLL circuit is also housed inside the U2. Its input can be connected to either of the phase comparators using the JP5 jumper block, as mentioned above:

JP5-1 VCO input is from PC2 output, the JK Flip-Flop edge detector
JP5-2 VCO input is from PC1 output, the X-OR phase comparator

The output of the VCO is taken to the J2 terminal block (J2-4) for external use and observation, as well as being fed back into the different PLL circuit sections.

The error signal that is internally used by the VCO circuit is also brought out as the demodulator signal (Dem) on U2-10 and is also available at the output terminal block, J2-3. This signal can be used to carry out FM demodulation experiments.

For more detailed investigation of the capabilities and operation of the U2 IC, please consult the datasheet included on the Documentation CD. Datasheet has extensive information on the design procedures for using this device in very different ways.

Input Signal Gating

To facilitate various PLL and FM demodulation experiments, the PLL module has provision for accepting an external signal instead of the output from the reference oscillator section. This selection is done with the JP3 jumper block as follows:

JP3-1 Output of the reference oscillator
JP3-2 External input signal from J2-1

The input signal can be gated on/off with the on-board CMOS Analog Switch, U6, by supplying a gating signal to the J2-2 terminal block. Such an arrangement would be required if transient response of the PLL circuit needs to be analyzed or observed. By gating the input signal on/off at a suitable rate, parameters like loop response time, settling time, overshoot and damping can be observed.

The complete input terminal block, J2, assignments are as follows:

Terminal 1	External Signal Input
Terminal 2	Input Gating Signal (TTL level, High: ON, Low: OFF)
Terminal 3	VCO Demodulator Output
Terminal 4	VCO signal output
Terminal 5	Ground

Divide-By-N Circuit

At the core of the divide-by-n circuit is the fully configurable and very capable IC, U3. Using the S1, S2, and S3 DIP switches, U3 can be set to work as a divide-by-n counter across a very wide range. LED indicators connected to the DIP switches S1 and S2 provide a visible feedback while setting the divisor ratio.

Different operating modes for the U3 can be selected with the S2 DIP switch. Mode 5 seems to be useful for most common applications, so the PLL module comes with the DIP switch S3 set to "5". The U4 IC, along with the components around it provide a master reset to U3 for proper configuration setting.

For more detailed investigation of the capabilities and operation of the U3 IC, please consult the datasheet included on the Documentation CD. Datasheet has extensive information on the different modes of operation that is possible with this device.

Power Input

This is the circuit built around the Q1 Power MOSFET. It does two functions: **a)** Reverse power polarity protection with Q1 and R1, and **b)** Power supply filtering and decoupling with C1 and C2.

3. FUNCTIONAL TESTING

The procedure included here can be used to make a quick but thorough check of all the circuit sections included on the PLL module.

Equipment required:

1. 40 MHz oscilloscope
2. 20 MHz frequency counter
3. 1 MHz Function Generator
4. 5 V DC power supply

Test Procedure

- ☐ 1. Apply power by connecting the power supply to the binding posts. D18 green LED should come on.
- ☐ 2. Measure the voltage at TP1. It should be about 40 mV less than the power supply voltage.
- ☐ 3. Measure/observe the signal with a scope at U1-9 for the presence of the 5.120 MHz oscillator output.
- ☐ 4. Make sure JP1 is at position 3 and measure the frequency of the signal at TP2. It should be 5.000 kHz.
- ☐ 5. Make sure JP2, JP3 and JP5 are all at position 1, and JP4 is at position2.
- ☐ 6. Set all DIP switches to OPEN, except for S2-6 which should be CLOSED.
- ☐ 7. Measure the output signal at TP3 and confirm that the frequency is 10.000 MHz.
- ☐ 8. Confirm that the LOCK indicator is ON.
- ☐ 9. Move the Jumper JP1 to position 2 and confirm that the output is around 20.000 MHz. The LOCK indicator should be OFF or flickering to indicate that the PLL is having trouble maintaining lock.
- ☐ 10. Move jumper JP2 to position 2 and measure the output signal. It should be back at 10.000 MHz with the LOCK indicator ON.
- ☐ 11. Move the jumper JP4 to position 3 to include the divide-by-2 stage. Output should loose lock and move back up to around 20.00 MHz.
- ☐ 12. Move JP1 to position 4, and JP5 to position 2 to test the PC1. The output should be 2.500 MHz, with the LOCK indicator ON.
- ☐ 13. Move the jumper JP4 to position 1 for direct feedback from the VCO, and JP5 back to 1 for connection to PC2. You should see the VCO drift somewhere around 50 kHz without locking onto the reference signal (PLL capture range, as shipped from the factory, does not extend below 3 MHz. The circuit will still function, however, with quite a bit of frequency jitter down to about 50 kHz.)
- ☐ 14. Set the Jumper blocks as follows: JP1 at 3, JP2 at 1, JP3 at 2, JP4 at 1, JP5 at 1.
- ☐ 15. Set all DIP switches to OPEN, except for S1-6 which should be CLOSED. This sets the divide-by-n circuit divisor ratio to 20.
- ☐ 16. Set the function generator to about 100 KHz, and connect the output to J2-1, External Input. You should see the output signal steady at about 2.00 MHz.
- ☐ 17. Observe the input signal at U2-14 or JP3-2 and confirm that it is the 100 kHz input signal.
- ☐ 18. Carefully connect the J2-2 Gating input to Ground with an external jumper cable. You should see the signal at U2-14 (or JP3-2) disappear and the output drop to about 50 kHz.
- ☐ 19. Remove the external jumper and slowly increase the function generator frequency to past 1 MHz. You should see the output of the VCO track your sweep until the VCO maxes out at around 24 MHz.

If all the steps above check out, then you have a fairly healthy PLL module in your hands. Please do not forget to set all jumpers and DIP switches back to their default positions.

4. CHALLENGE COMPONENTS

If you have the PLL Challenge Module, you will notice that some components are not soldered to the PCB, but are instead mounted on single-pin machined sockets. These components are also marked on the schematic diagram with a dashed rectangular box around them.

These challenge components are the resistors and capacitors that determine the basic behaviour or response of their circuit sections. It is possible to modify the characteristics of these sections to new parameters by redesigning the circuit and replacing these components with different ones.

The design guidelines are included in the datasheets of the IC's, including some worked examples.

The single pin sockets have a good grip on the components leads for good electrical connection, so care should be taken while removing or inserting the challenge components. A good pair of long-nose pliers is almost a must while working with the challenge components.

5. APPLICATIONS

The following is a sample collection of some ideas for experimentation that is possible with the PLL module.

1. PLL SYSTEM DESIGN

Using the Challenge Module, students design the PLL system with the parameters specified by the instructor. Full design procedure and a sample design case are included in the product documentation.

2. PLL PERFORMANCE ANALYSIS

This would be the more conventional PLL experiment where the students use an external oscillator to observe and analyze the behaviour of the PLL system with respect to the design parameters.

3. FREQUENCY SYNTHESIZER DESIGN

Using all configurable elements of the Challenge Module, students design a frequency synthesizer as specified by the instructor. Once again, full design procedure and a sample design are included in the product documentation.

4. FREQUENCY SYNTHESIZER OPERATION AND PERFORMANCE ANALYSIS

This would be the experiment where the students analyze the performance of the frequency synthesis circuit they have designed. If facilities exist, and if the instructor wishes, a PC can be used to supply the digital input required for the divide-by-N circuit.

5. X-OR PHASE DETECTOR ANALYSIS

In this experiment students observe the behaviour of the X-OR phase detector section of the circuit with respect to its sensitivity to noise, interference, and harmonics of the center frequency. X-OR phase detectors have excellent noise immunity, but they will also lock onto harmonics of the center frequency.

6. J-K FLIP-FLOP PHASE DETECTOR ANALYSIS

In this experiment students observe the behaviour of the J-K Flip-Flop edge detecting phase detector section of the circuit with respect to its sensitivity to noise, interference, and harmonics of the center frequency. Edge detecting phase detectors are insensitive to the harmonics of the design frequency, but they are more sensitive to noise and interference.

7. FM DEMODULATOR ANALYSIS

If an FM modulated signal is applied to the external input of the PLL module, demodulated FM signal can be observed at the demodulator output of the PLL VCO. Depending on the method and type of modulation used, several experiments are possible in this area.

8. FREQUENCY-HOPPING EXPERIMENTS

Since the PLL module lends itself to external digital control from a PC, this feature can be used to build a simple application program that implements a frequency hopping spread spectrum scheme. Depending on the available equipment, and the extent to which the instructor intends to go, several experiments ranging from observing a FHSS system in action to measuring the RF energy spread can be carried out around this topic.

6. SPECIFICATIONS

Power Requirements	+5V DC @ 70 mA typical, 150 mA max.
VCO Range	20 Hz – 25 MHz typical with different components
PLL Capture Range	Same as VCO operation, with different components 3.0 MHz to 17 MHz as shipped from the factory
Dimensions	3.0”W x 4.0”L x 1.5”H

7. SUPPORT

We are here to help if you need assistance in using or troubleshooting the PLL Module. Please do not hesitate to contact Unistep Tech Support using any of the means listed below:

Internet Our web site www.unistep.ca has some support information and we are adding new material all the time.

E-Mail This is the preferred method of contacting our support staff. Please use our support address support@unistep.ca for any questions, comments, or recommendations you may wish to send our way.

Phone You can call us at 416-619-9308 and talk to our support staff concerning any technical assistance you may need. If you leave a message, we strive to return calls within one business day.