User Manual: CubeSat 1U Electronic Power System and Batteries: CS-1UEPS2-NB/-10/-20

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Document Control

Issue	Date	Section	Description of Change	Reason for Change
A	21/07/10	All	First Release	

Revision Control

Product	Part Number	Revisions covered	Notes
Cubesat 1U Electronic Power System 2G with no battery	CS-1UEPS2-NB	A	
Cubesat 1U Electronic Power System 2G with 10Wh battery	CS-1UEPS2-10	A	
Cubesat 1U Electronic Power System 2G with 20Wh battery	CS-1UEPS2-20	A	

Acronyms and Abbreviations

BCR	Battery Charge Regulator
PCM	Power Conditioning Module
PDM	Power Distribution Module
MPPT	Maximum Power Point Tracker
USB	Universal Serial Bus
ESD	Electro Static Discharge
TLM	Telemetry
EPS	Electrical Power System
EoC	End of Charge
AMUX	Analogue Multiplexer
ADC	Analogue to Digital Converter
AIT	Assembly, Integration and Testing
1U	1 Unit (Cubesat standard size)
3U	3 Unit (Cubesat standard size)
FleXU	FleXible Unit (suitable for various satellite configurations)
rh	Relative Humidity
Wh	Watt Hour
Ah	Ampere Hour
DoD	Depth of Discharge
$Kbits^{-1}$	Kilobits per second
Voc	Open Circuit Voltage
Isc	Short Circuit Current
2s1p	Battery configuration – 2 cells in series, 1 battery in parallel (single string)

2s2p	Battery configuration – 2 cells in series, 2 batteries in parallel
2s3p	Battery configuration – 2 cells in series, 3 batteries in parallel

Related Documents

No.	Document Name	Doc Ref.
RD-1	CubeSat Design Specification	CubeSat Design Specification Rev. 12
RD-2	NASA General Environmental Verification Standard	GSFC-STD-7000 April 2005
RD-3	CubeSat Kit Manual	UM-3
RD-4	Solar Panel User Document	TBC
RD-5	Power System Design and Performance on the World's Most Advanced In-Orbit Nanosatellite	As named

#	⚠ Warning ⚠	Risk
⚠1	Ensure headers H1 and H2 are correctly aligned before mating boards	If misaligned, battery positive can short to ground, causing failure of the battery and EPS
⚠2	Ensure switching configuration is implemented correctly before applying power to EPS	If power is applied with incorrect switch configuration, the output of the BCR can be blown, causing failure of the EPS and subsequent damage to the battery
⚠3	Observe ESD precautions at all times	The battery is a static sensitive system. Failure to observe ESD precautions can result in failure of the battery
⚠4	Ensure not to exceed the maximum stated limits	Exceeding any of the stated maximum limits can result in failure of the battery
⚠5	Ensure batteries are fully isolated during storage	If not fully isolated (by switch configuration or separation) the battery may over-discharge, resulting in failure of the battery
⚠6	No connection should be made to H2.35-36	These pins are used to connect the battery to the EPS. Any connections to the unregulated battery bus should be made to pins H2.43-44
⚠7	H1 and H2 pins should not be shorted at any time	These headers have exposed live pins which should not be shorted at any time. Particular care should be taken regarding the surfaces these are placed on.
⚠8	Battery should only be operated when integrated with an EPS	The EPS includes a number of protection circuits for the battery. Operation without these protections may lead to damage of the batteries
⚠9	Do not discharge batteries below 6V	If the battery is discharged to a voltage below 6V the cells have been compromised and will no longer hold capacity
⚠10	If batteries are over-discharged DO NOT attempt to recharge	If the battery is over discharged (below 6V) it should not be recharged as this may lead to cell rupture.

1. Introduction

This document provides information on the features, operation, handling and storage of the Clyde Space second generation 1U EPS with integrated 10Wh or 20Wh batteries. The 1U EPS is designed to integrate with a suitable battery and solar arrays to form a complete power system for use on a 1U CubeSat.

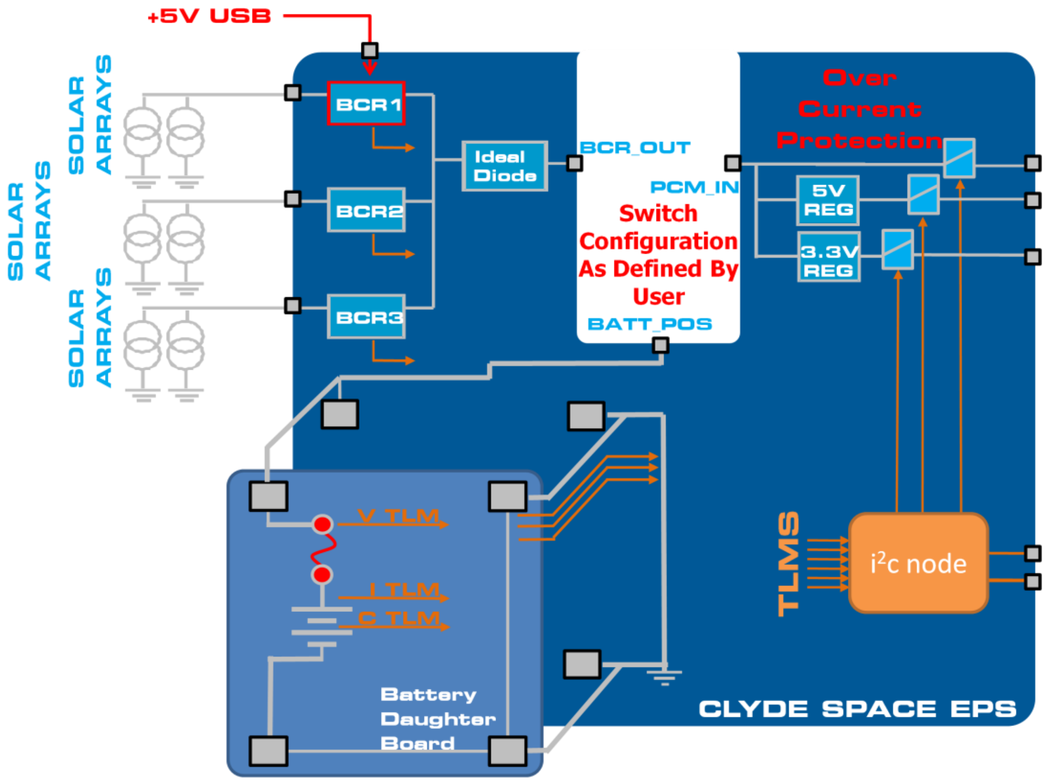


Figure 1-1 System Diagram

1.1 Additional Information Available Online

Additional Information on CubeSats and Clyde Space Systems can be found here: http://www.clyde-space.com. You will need to login to our website to access certain documents.

1.2 Continuous Improvement

At Clyde Space we are continuously improving our processes and products. We aim to provide full visibility of the changes and updates that we make, and information of these changes can be found by logging in to our website: http://www.clyde-space.com.

1.3 Document Revisions

In addition to hardware and software updates, we also make regular updates to our documentation and online information. Notes of updates to documents can also be found at http://www.clyde-space.com.

2. OVERVIEW

This is the second generation of Clyde Space CubeSat Electronic Power System and Batteries, developed by our team of Spacecraft Power Systems and Electronics Engineers.

Since introducing the first generation in 2006, Clyde Space has shipped over 120 EPS and Batteries to a variety of customers in Europe, Asia and North America. The second generation EPS builds on the heritage gained with the first generation, whilst increasing power delivery capability by approximately 50%. Furthermore, we have implemented an ideal diode mechanism, which ensures that there will be zero draw on the battery in launch configuration.

The batteries utilise Lithium Ion Polymer technology to offer world leading power to mass ratios in a form factor ideally suited to the volume constraints of CubeSats. In addition to this, testing has been carried out by both ESA and NASA, and the batteries have been cleared for launch on NASA manned flights.

Clyde Space is the World leading supplier of power system components for CubeSats. We have been designing, manufacturing, testing and supplying batteries, power system electronics and solar panels for space programmes since 2006. Our customers range from universities running student led missions, to major space companies and government organisations.

3. Maximum Ratings[(1)]

OVER OPERATING TEMPERATURE RANGE (UNLESS OTHERWISE STATED)				
		BCR	**Value**	**Unit**
Input Voltage[(2)]	SA1 (pin 1 **or** pin 4)	BCR1 (3W)	10	V
	SA2 (pin 1 **or** pin 4)	BCR2 (3W)	10	V
	SA3 (pin 1 **or** pin 4)	BCR3 (3W)	10	V
	Battery		8.3	V
	5V Bus		5.05	V
	3.3V Bus		3.33	V
		Notes	**Value**	**Unit**
Input Current	SA1	@6V	750	mA
	SA2	@6V	750	mA
	SA3	@6V	750	mA
			Value	**Unit**
Charge Limits	Voltage	max	8.4	V
	Current	max	1.25	A
	Current Rate	max	C	Fraction of Capacity
Discharge Limits	Voltage	min	6.0	V
	Current	max	1.25	A
	Current Rate	max	C	Fraction of Capacity
			Value	**Unit**
Output Current	Battery Bus	@8.26V	6	A
	5V Bus	@5V	4	A
	3.3V Bus	@3.3V	4	A
			Value	**Unit**
Operating Temperature			-40 to 85	°C
Storage Temperature			-50 to 100	°C
Vacuum			10^{-5}	torr
Radiation Tolerance			(TBC)	kRad
Shock			(TBC)	
Vibration			To [RD-2]	

Table 3-1 Max Ratings of the 1U EPS and Batteries

(1) Stresses Beyond those listed under maximum ratings may cause permanent damage to the EPS and Batteries. These are the stress ratings only. Operation of the EPS and Batteries at conditions beyond those indicated is not recommended. Exposure to absolute maximum ratings for extended periods may affect EPS and Batteries reliability

(2) De-rating of power critical components is in accordance to ECSS guidelines.

4. Electrical Characteristics

Description	Conditions	Min	Typical	Max	Unit
3W BCR					
Input Voltage		3.5	--	8	V
Output Voltage		6.2	--	8.26	V
Output Current		0	--	0.5	A
Operating Frequency		160	170	180	KHz
Efficiency	@6V input, Full Load	77%	79%	80%	
Battery Charge Conditions					
EoC Voltage		8.22	8.26	8.30	V
Charge Current	Recommended maximum C/2	--	0.625	--	A
Battery Discharge Conditions					
Full Discharge Voltage		6.16	6.2	6.24	V
Discharge Current	CS-EPS2-NB		N/A		
	CS-EPS2-10 Recommended max C/2	--	--	0.625	A
	CS-EPS2-20 Recommended max C/2	--	--	1.25	A
Depth of Discharge	Recommended	--	20%	--	Capacity
Battery Capacity					
CS-EPS2-NB	N/A				
CS-EPS2-10	@discharge rate C/5, 20°C		1.276		Ah
CS-EPS2-20	@discharge rate C/5, 20°C		2.552		Ah
Unregulated Battery Bus					
Output Voltage		6.2	--	8.26	V
Output Current		--	--	4	A
Operating Frequency		--	--	--	
Efficiency	@8.26V input, Full Load	98.5%	99%	99.5%	
5V Bus					
Output Voltage		4.95	5	5.05	V
Output Current		--	--	1.5	A
Operating Frequency		470	480	490	kHz
Efficiency	@5V input, Full Load	95%	96%	98%	
3.3V Bus					
Output Voltage		3.276	3.3	3.333	V
Output Current		--	--	1.2	A
Operating Frequency		470	480	490	kHz
Efficiency	@3.3V input, Full Load	94%	95%	97%	
Communications					
Protocol		--	I^2C	--	
Transmission speed		--	100	400	KBps
Bus voltage		3.26V	3.3V	3.33V	
Node address		--	0x2D	--	Hex
Address scheme		--	7bit	--	
Node operating frequency		--	8MHz	--	
Quiescent Operation					

Power Draw	Flight Configuration of Switches	--	--	<0.2	W
Power Drawn for heater when active	CS-1UEPS2-10, from 3.3V Bus		0.22	0.3	W
	CS-1UEPS2-20, from 3.3V Bus		0.44	0.6	W
Physical		**L**	**W**	**H**	
Dimensions	CS-1UEPS2-NB (H is bottom of EPS board to top of tallest component)	95	90	12.65	mm
	CS-1UEPS2-10(H is bottom of EPS board to top of tallest component)	95	90	15.4	mm
	CS-1UEPS2-20(H is bottom of EPS board to top of tallest component)	95	90	22.0	mm
Weight	CS-1UEPS2-NB	-	83	86	g
	CS-1UEPS2-10	-	163	169	g
	CS-1UEPS2-20	-	229	237	g

Table 4-1 Performance Characteristics of the 1U EPS and Batteries

5. Handling and Storage

The EPS and batteries require specific guidelines to be observed for handling, transportation and storage. These are stated below. Failure to follow these guidelines may result in damage to the units or degradation in performance.

5.1 Electro Static Discharge (ESD) Protection

This system incorporates static sensitive devices and care should be taken during handling. Do not touch the EPS and batteries without proper electrostatic protection in place. All work carried out on the system should be done in a static dissipative environment.

5.2 General Handling

The EPS and batteries are designed to be robust and withstand flight conditions. However, care must be taken when handling the device. Care should be taken not to drop the devices. There are live connections between the battery systems and the EPS on the CubeSat Kit headers. All metal objects (including probes) should be kept clear of these headers.

Gloves should be worn when handling all flight hardware.

Flight hardware should only be removed from packaging in a class 100000 (or better) clean room environment.

The exterior surface of the cells is covered with space grade Kapton adhesive tape; this provides insulation for the cells and is not to be removed.

5.3 Shipping and Storage

The devices are shipped in anti-static, vacuum sealed packaging enclosed in a hard protective case. This case should be used for storage. All hardware should be stored in anti-static packaging.

Rate of capacity degradation of lithium polymer cells in storage is dependent on the storage environment, particularly temperature, and cell state of charge. It is recommended that the batteries are stored with voltages approximately 7.4V (50% DoD), at a temperature between +5°C and +15°C and in a humidity-controlled environment of 40-60%rh.

The most serious degradation occurs when cells are stored in a fully charged state.

If batteries are stored for long periods of time, they may over discharge. To prevent this, batteries should be charged periodically to maintain ~7.4V. It is also recommended that the Pull Pin is left in place/replaced during periods of storage.

The shelf-life of this product is estimated at 5 years when stored appropriately.

6. Materials and Processes

6.1 Materials Used

	Material	Manufacturer	%TML	%CVCM	%WVR	Application
1.	Araldite 2014 Epoxy	Huntsman	0.97	0.05	0.33	Adhesive fixing
2.	1B31 Acrylic	Humiseal	3.89	0.11	0.09	Conformal Coating
3.	DC 6-1104	Dow Corning	0.17	0.02	0.06	Adhesive fixing on modifications
4.	Stycast 4952	Emerson & Cuming	0.42	0.17	0.01	Thermally Conductive RTV
5.	PCB material	FR4	0.62	0	0.1	Note: worst case on NASA out-gassing list
6.	Solder Resist	CARAPACE EMP110 or XV501T-4	0.95 or 0.995	0.02 Or 0.001	0.31	-
7.	Solder	Sn62 or Sn63 (Tin/Lead)	-	-	-	-
8.	Flux	Alpha Rosin Flux, RF800, ROL 0	-	-	-	Note: ESA Recommended

Table 6-1 Materials List

Part Used	Manufacturer	Contact	Insulator	Type	Use
DF13-6P-1.25DSA(50)	Hirose	Gold Plated	Polyamide	PTH	Solar Array Connectors
ESQ-126-39-G-D	Samtec	Gold Plated	Black Glass Filled Polyester	PTH	CubeSat Kit Compatible Headers
DF13-6S-1.25C	Hirose	N/A	Polyamide	Crimp Housing	Harness for Solar Arrays (sold separately)
DF13-2630SCFA(04)	Hirose	Gold Plated	N/A	Crimp	Harness for Solar Arrays (sold separately)

Table 6-2 Connector Headers

6.2 Processes and Procedures

All assembly is carried out and inspected to ESA Workmanship Standards; ECSS-Q-ST-70-08C and ECSS-Q-ST-70-38C.

7. System Description

The Clyde Space 1U EPS is optimised for Low Earth Orbit (LEO) missions with a maximum altitude of 850km. The EPS is designed for integration with spacecraft that have six or less body mounted solar panels (i.e. one on each spacecraft facet). The EPS can accommodate various solar panel configurations, and has been designed to be versatile; please consult our support team if you have specific requirements for connecting the EPS to your spacecraft.

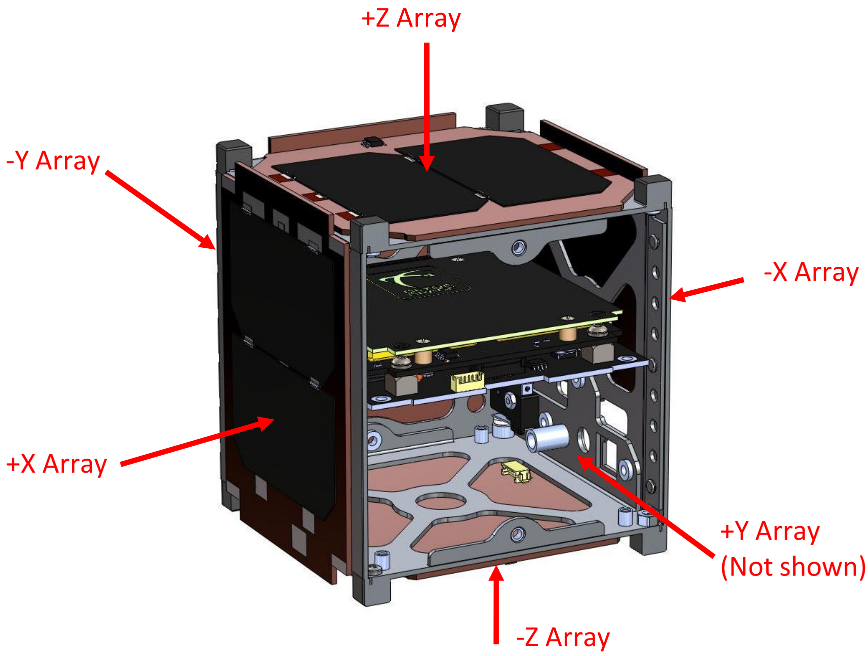
The Clyde Space EPS connects to the solar panels via three independent Battery Charge Regulators (BCRs). These are connected as shown in Figure 7-1 and Figure 7-2 with panels on opposing faces of the satellite connected to the same BCR (i.e. –X array and +X array are connected to BCR1, -Y and +Y to BCR2 and –Z and +Z to BCR3). In this configuration only one panel per pair can be directly illuminated at any given time, with the second panel providing a limited amount of energy due to albedo illumination. Each of the BCRs has an inbuilt Maximum Power Point Tracker (MPPT). This MPPT will track the dominant panel of the connected pair (the directly illuminated panel).

The output of the three BCRs are then connected together and, via the switch network, (described in Section 7.2), supply charge to the battery, Power Conditioning Modules (PCMs) and Power Distribution Modules (PDMs) via the switch network.

Clyde Space batteries offer high capacity with low weight and volume. The battery systems all have integrated heater systems to enhance operation at low temperatures. There is over current protection incorporated to protect the cells in the event of a power line fault.

The battery heater is an independent analogue circuit which maintains the battery temperature above 0°C. The heater is thermostatically controlled to automatically turn on when the battery temperature falls below 0°C, and switch off again when the temperature rises above 5°C. The heater can also be switched off by I^2C command for power conservation through the EPS.

The PCM/PDM network has an unregulated Battery Voltage Bus, a regulated 5V supply and a regulated 3.3V supply available on the satellite bus. The EPS also has multiple inbuilt protection methods to ensure safe operation during the mission and a full range of EPS telemetries, power bus resets and a heater off command via the I^2C network. These are discussed in detail in Sections 10 and **Error! Reference source not found.** respectively.



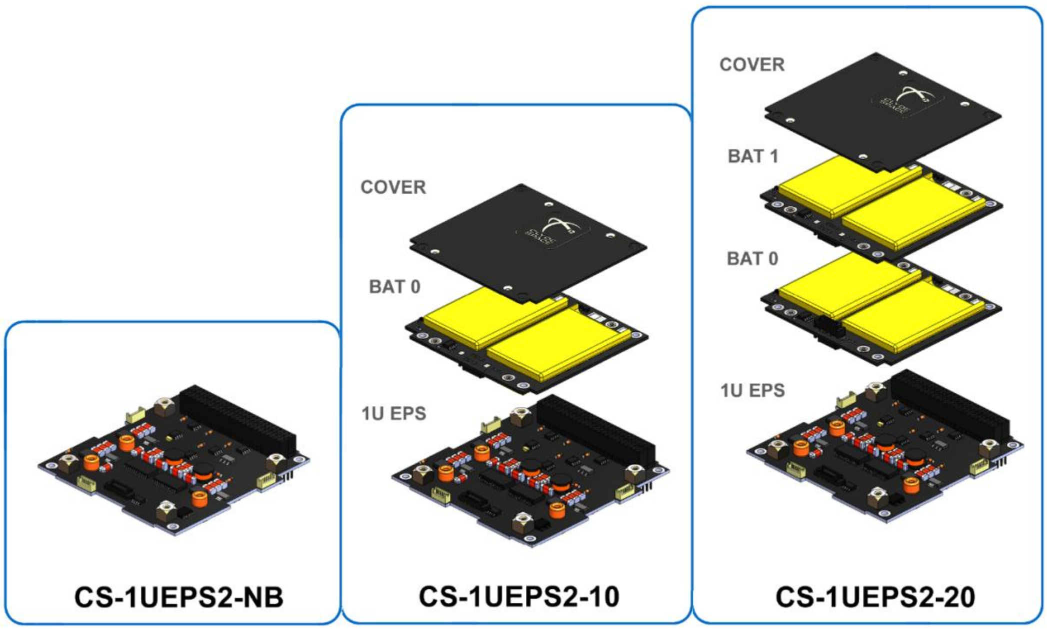


Figure 7-1 Configurations

7.1 System Overview

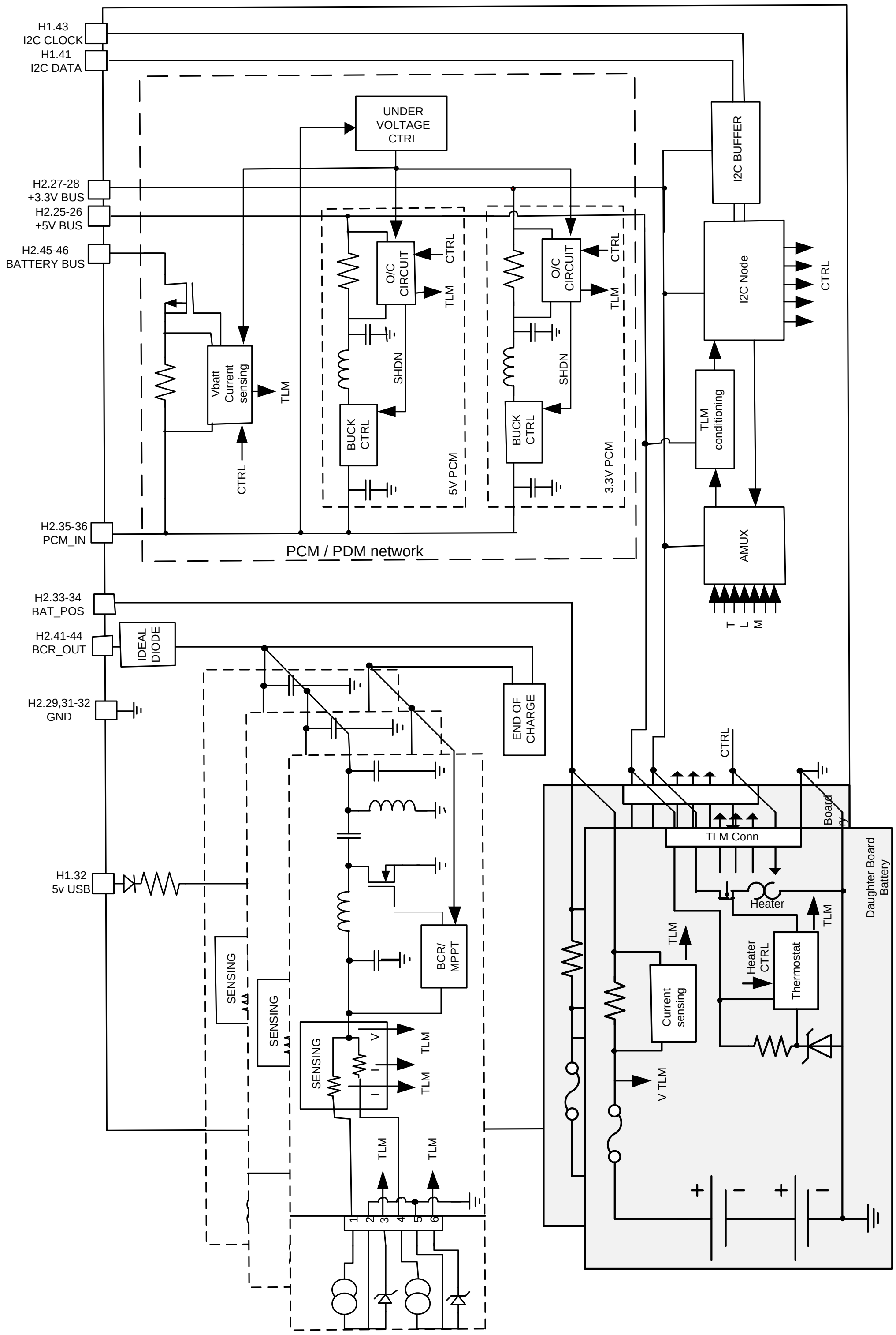


Figure 7-2 Function Diagram

7.2 Protection and Redundancy

BCRs

All the BCR power stages feature full system autonomy. They operate solely from the solar array input and do not require any power from the battery systems. This feature gives the system inbuilt redundancy as the failure of one BCR does not affect the remaining BCRs. Failure of the battery on the CS-1UEPS2-10 will not damage the BCRs but, due to the MPPT, will result in an intermittent interruption on all power buses (approximately every 2.5 seconds). Failure of one battery on the CS-1UEPS2-20 will not damage the BCRs and the system can continue to operate with a reduced capacity of 10Wh.

Batteries

All batteries have integrated over current protection. This is achieved by using polyswitches which are designed to trip when an over current event occurs. To protect the battery and satellite from power faults, such as over current or under voltage, a system of monitoring and shutdown is required. The system must be able to detect and shutdown any power line which has encountered a fault.

On the CS-1UEPS2-20, the loss of one pair of cells, (i.e. one battery in the stack) will not affect the performance of the remaining batteries – power will continue to be supplied to the system.

The rest of the power system is a robustly designed single string.

7.3 Quiescent Power Consumption

All power system efficiencies detailed (BCRs and PCMs) take into consideration the low level control electronics associated with them. As such these numbers are not included in the quiescent power consumption figures.

The I^2C node is the only circuitry not covered in the efficiency figures, and has a quiescent power consumption of ≈0.1W, which is the figure for the complete EPS.

When the heater is active the power drawn from the 3.3V Bus will rise to ≈0.22W on the CS-1UEPS2-10 and ≈0.44W on the CS-1UEPS2-20.

7.4 Mass and Mechanical Configuration

The mass of the EPS is approximately 83g and is contained on a single PC/104 size card, compatible with the Cubesat Kit bus. The -10 and -20 versions require one and two battery daughter boards respectively to be fitted. The mass of these systems, including the cover protection board, are approximately 163g and 229g.

Other versions of the EPS are available without the Cubesat Kit bus header.

The dimensions of the EPS, including all connector positions are shown in Figure 7-3.

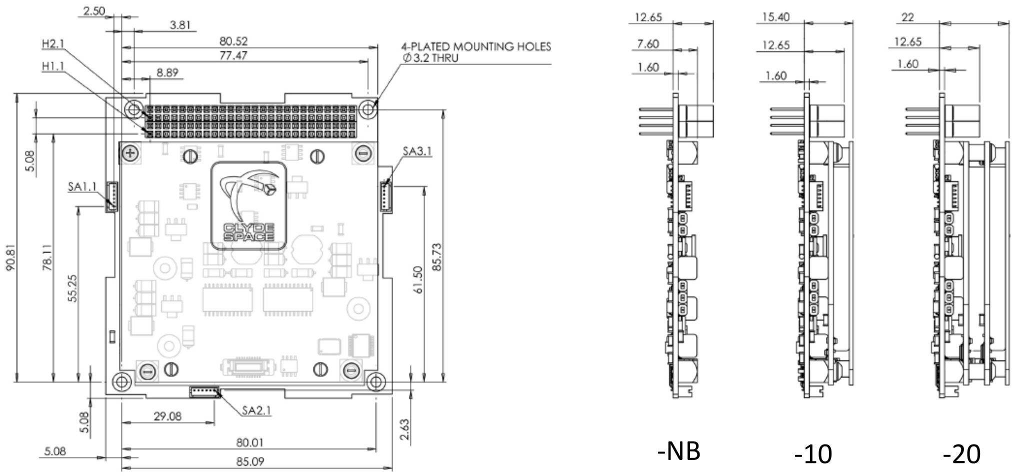


Figure 7-3 Board dimensions (mm)

8. INTERFACING

The interfacing of the EPS is outlined in Figure 8-1, including the solar array inputs, connection to the switch configuration, output of the power buses and communication to the I^2C node. In the following section it is assumed that the EPS will be integrated with a Clyde Space Battery.

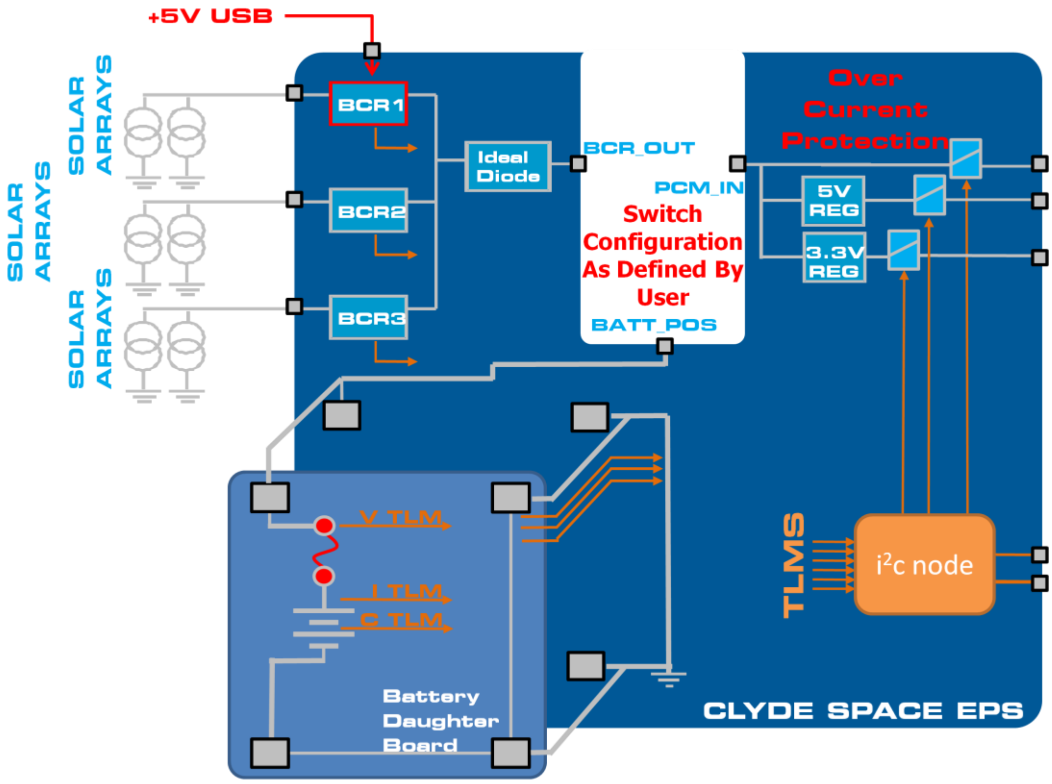


Figure 8-1 Clyde Space EPS and Battery Simplified Connection Diagram

8.1 Connector Layout

The connector positions are shown in Figure 7.3, and described in Table 8.1.

Connector	Function
SA1	Solar Array connector for 3W +/-Y arrays
SA2	Solar array connector for 3W +/-X arrays
SA3	Solar array connector for 3W +/-Z arrays
H1	Cubesat Kit bus compatible Header 1
H2	Cubesat Kit bus compatible Header 2

Table 8-1 Connector functions

8.2 Solar Array Connection

The EPS has three connectors for the attachment of solar arrays. Each interface accommodates inputs from two arrays with temperature telemetry for each.

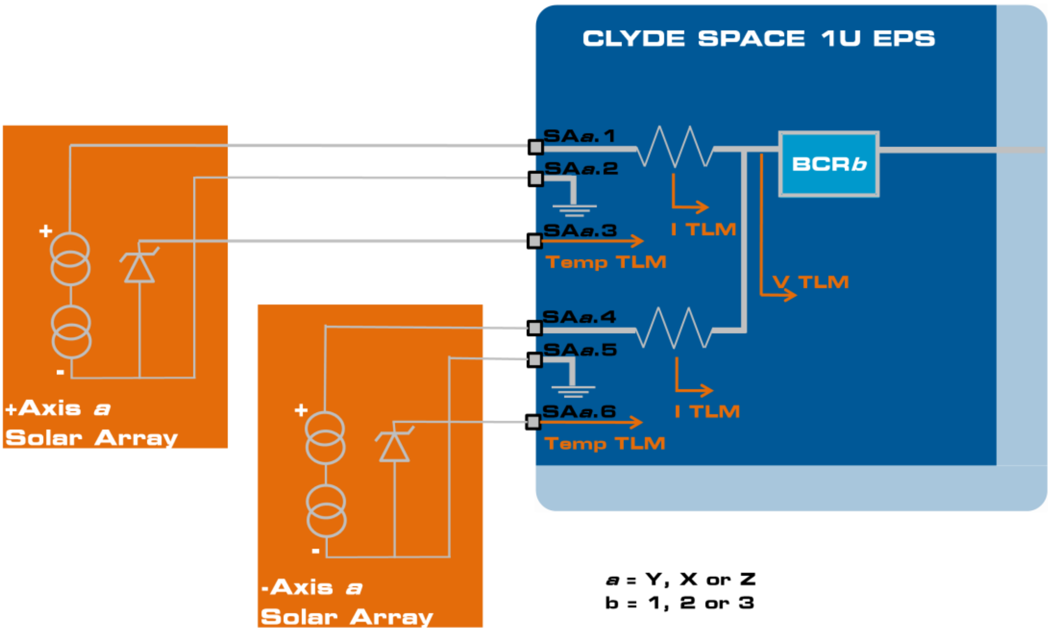


Figure 8-2 Solar Array Configuration

HIROSE DP12-6P-1.25 DSA connector sockets are used on the EPS. These are labelled SA1, SA2 and SA3, routed to BCR1, BCR2 and BCR3 respectively. Each of the BCRs are capable of interfacing to 3W panels and should be harnessed to arrays on opposing faces of the satellite. The string length should be 2 triple junction cells.

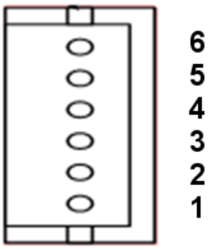


Figure 8-3 Solar Array Pin Numbering

Pin	Name	Use	Notes
1	+Y_ARRAY	+Y Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	+Y_TEMP_TELEM	+Y Array Telemetry	Telemetry
4	-Y_ARRAY	-Y Power Line	Power
5	GND	Ground Line	Power RTN and GND connection for Temp Sensor
6	-Y_TEMP_TELEM	-Y Array Telemetry	Telemetry

Table 8-2 Pin out for Header SA1

Pin	Name	Use	Notes
1	+X_ARRAY	+X Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	+X_TEMP_TELEM	+X Array Telemetry	Telemetry
4	-X_ARRAY	-X Power Line	Power
5	GND	Ground Line	Power RTN and GND connection for Temp Sensor
6	-X_TEMP_TELEM	-X Array Telemetry	Telemetry

Table 8-3 Pin out for Header SA2

Pin	Name	Use	Notes
1	+Z_ARRAY	+Z Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	+Z_TEMP_TELEM	+Z Array Telemetry	Telemetry
4	-Z_ARRAY	-Z Power Line	Power
5	GND	Ground Line	Power RTN and GND connection for Temp Sensor
6	-Z_TEMP_TELEM	-Z Array Telemetry	Telemetry

Table 8-4 Pin out for Header SA3

8.3 Solar Array Harness

Clyde Space supply harnesses (sold separately) to connect the solar panels to the EPS comprising of two Hirose DF13-6S-1.25C connected at each end of the cable, one end connects to the EPS, with two halves of the harness connecting to opposing solar panels. Clyde Space solar arrays use Hirose DF13-6P-1.25H as the interface connector to the harness.

8.4 Temperature Sensing Interface

Temperature sensing telemetry is provided for each solar array connected to the EPS. A compatible temperature sensor (LM335M) is fitted as standard on Clyde Space solar arrays (for non-Clyde Space panels refer to section 8.5). The output from the LM335M sensor is then passed to the telemetry system via on board signal conditioning. Due to the nature of the signal conditioning, the system is only compatible with zener based temperature sensors i.e. LM335M or equivalent. Thermistor or thermocouple type sensors are incompatible with the conditioning circuit.

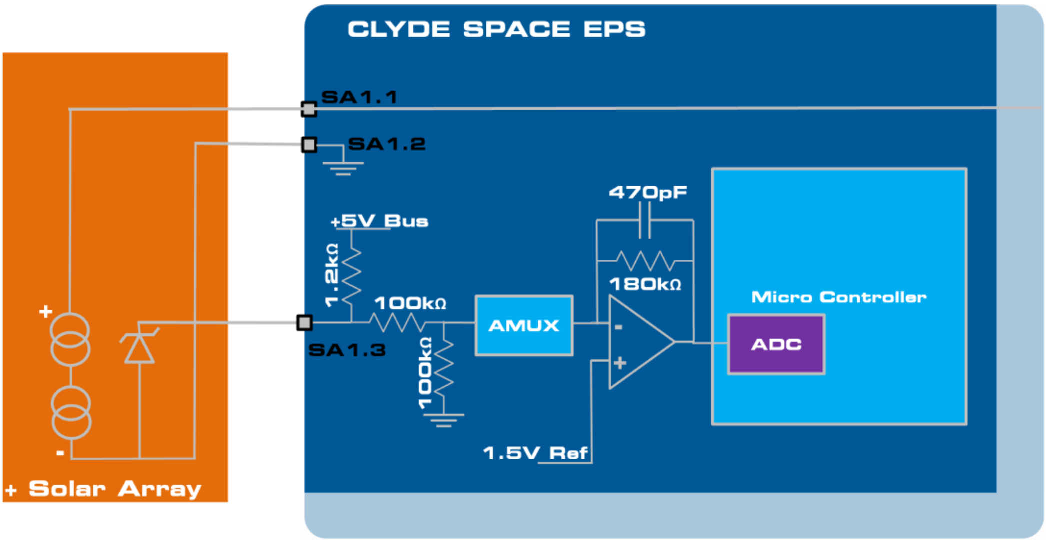


Figure 8-6 Temperature sensor block diagram

8.5 Non-Clyde Space Solar Arrays

When connecting non-Clyde Space solar arrays, care must be taken with the polarity. Pins 1, 2 and 3 are for array(+) and pins 4, 5 and 6 relate to the opposite array(-). Cells used should be of triple junction type. If other cells are to be interfaced please contact Clyde Space.

8.6 CubeSat Kit Compatible Headers

Connections from the EPS to the bus of the satellite are made via the CubeSat Kit compatible headers H1 and H2, as shown in Figure 8-6.

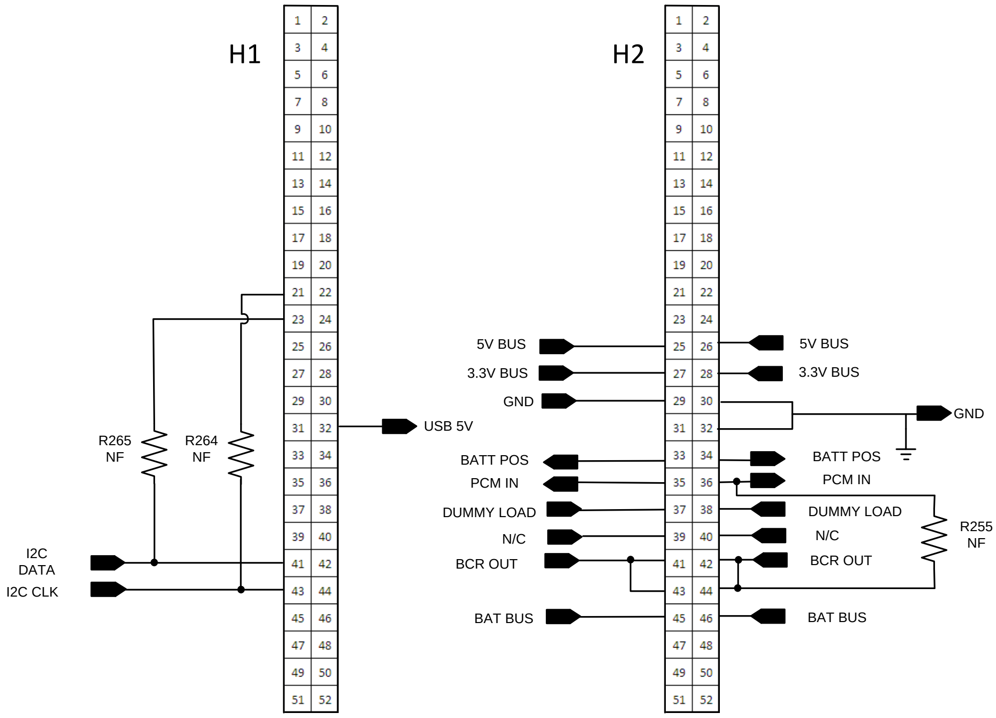


Figure 8-5 CubeSat Kit Header Schematic

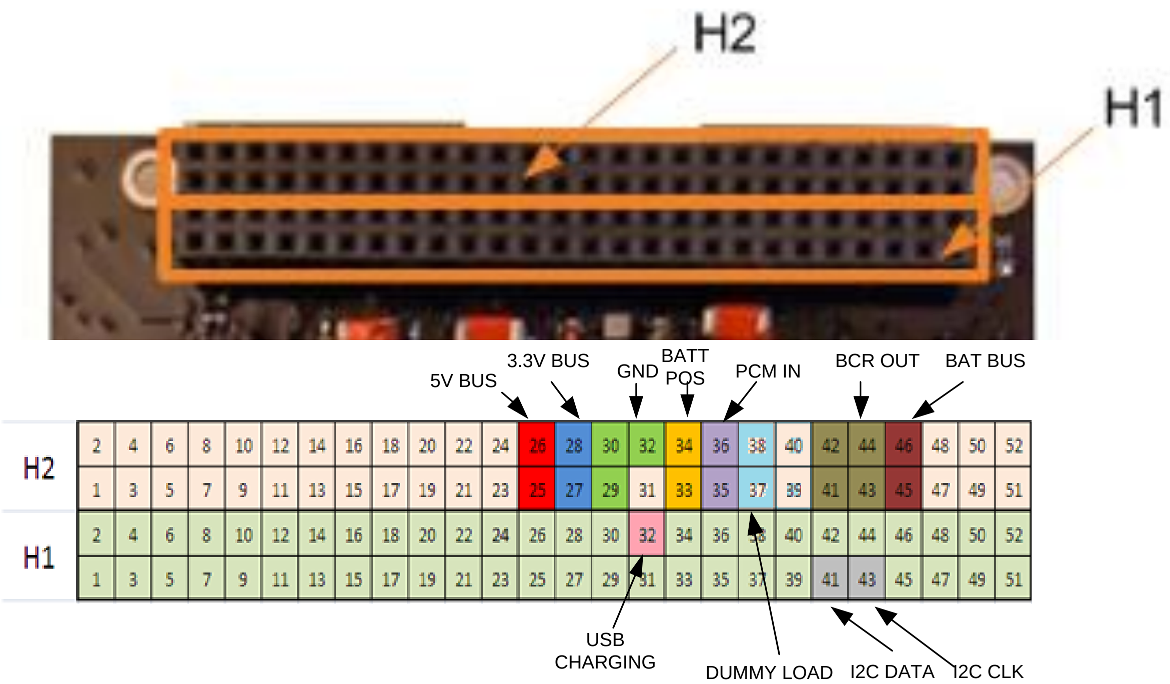


Figure 8-6 EPS Connector Pin Identification

8.7 Cubesat Kit Header Pin Definitions

HEADER 1				HEADER 2			
Pin	Name	Use	Notes	Pin	Name	Use	Notes
1	NC	Not Connected	Not Connected	1	NC	Not Connected	Not Connected
2	NC	Not Connected	Not Connected	2	NC	Not Connected	Not Connected
3	NC	Not Connected	Not Connected	3	NC	Not Connected	Not Connected
4	NC	Not Connected	Not Connected	4	NC	Not Connected	Not Connected
5	NC	Not Connected	Not Connected	5	NC	Not Connected	Not Connected
6	NC	Not Connected	Not Connected	6	NC	Not Connected	Not Connected
7	NC	Not Connected	Not Connected	7	NC	Not Connected	Not Connected
8	NC	Not Connected	Not Connected	8	NC	Not Connected	Not Connected
9	NC	Not Connected	Not Connected	9	NC	Not Connected	Not Connected
10	NC	Not Connected	Not Connected	10	NC	Not Connected	Not Connected
11	NC	Not Connected	Not Connected	11	NC	Not Connected	Not Connected
12	NC	Not Connected	Not Connected	12	NC	Not Connected	Not Connected
13	NC	Not Connected	Not Connected	13	NC	Not Connected	Not Connected
14	NC	Not Connected	Not Connected	14	NC	Not Connected	Not Connected
15	NC	Not Connected	Not Connected	15	NC	Not Connected	Not Connected
16	NC	Not Connected	Not Connected	16	NC	Not Connected	Not Connected
17	NC	Not Connected	Not Connected	17	NC	Not Connected	Not Connected
18	NC	Not Connected	Not Connected	18	NC	Not Connected	Not Connected
19	NC	Not Connected	Not Connected	19	NC	Not Connected	Not Connected
20	NC	Not Connected	Not Connected	20	NC	Not Connected	Not Connected
21	ALT I^2C CLK	Alt I^2C clock connection	0ohm resistor R265 (must fit to operate)	21	NC	Not Connected	Not Connected
22	NC	Not Connected	Not Connected	22	NC	Not Connected	Not Connected
23	ALT I^2C DATA	Alt I^2C data connection	0ohm resistor R264 (must fit to operate)	23	NC	Not Connected	Not Connected
24	NC	Not Connected	Not Connected	24	NC	Not Connected	Not Connected
25	NC	Not Connected	Not Connected	25	+5V BUS	+5V Power bus	Regulated 5V bus
26	NC	Not Connected	Not Connected	26	+5V BUS	+5V Power bus	Regulated 5V bus
27	NC	Not Connected	Not Connected	27	+3.3V BUS	+3V3 Power bus	Regulated 3V3 bus
28	NC	Not Connected	Not Connected	28	+3.3V BUS	+3V3 Power bus	Regulated 3V3 bus
29	NC	Not Connected	Not Connected	29	GND	Ground connection	System power return
30	NC	Not Connected	Not Connected	30	GND	Ground connection	System power return
31	NC	Not Connected	Not Connected	31	NC	Not Connected	Not Connected
32	USB_5	USB 5+v	Use to charge battery via USB	32	GND	Ground connection	System power return
33	NC	Not Connected	Not Connected	33	BATT POS	Power line	Pull pin normally connected pin
34	NC	Not Connected	Not Connected	34	BATT POS	Power line	Pull pin normally connected pin
35	NC	Not Connected	Not Connected	35	PCM IN	Power line	Sep SW normally connected pin
36	NC	Not Connected	Not Connected	36	PCM IN	Power line	Sep SW normally connected pin
37	NC	Not Connected	Not Connected	37	DL	Dummy Load Protection	Pull pin normally open pin
38	NC	Not Connected	Not Connected	38	DL	Dummy Load Protection	Pull pin normally open pin
39	NC	Not Connected	Not Connected	39	NC	Not Connected	Not Connected
40	NC	Not Connected	Not Connected	40	NC	Not Connected	Not Connected
41	I^2C DATA	I^2C data	Data for I^2C communications	41	BCR OUT	Power line	Common point PP +SS pins
42	NC	Not Connected	Not Connected	42	BCR OUT	Power line	Common point PP +SS pins
43	I^2C CLK	I^2C clock	Clock for I^2C communications	43	BCR OUT	Power line	Common point PP +SS pins
44	NC	Not Connected	Not Connected	44	BCR OUT	Power line	Common point PP +SS pins
45	NC	Not Connected	Not Connected	45	Battery Bus	Power line	Output to battery bus
46	NC	Not Connected	Not Connected	46	Battery Bus	Power line	Output to battery bus
47	NC	Not Connected	Not Connected	47	NC	Not Connected	Not Connected
48	NC	Not Connected	Not Connected	48	NC	Not Connected	Not Connected

HEADER 1				HEADER 2			
Pin	Name	Use	Notes	Pin	Name	Use	Notes
49	NC	Not Connected	Not Connected	49	NC	Not Connected	Not Connected
50	NC	Not Connected	Not Connected	50	NC	Not Connected	Not Connected
51	NC	Not Connected	Not Connected	51	NC	Not Connected	Not Connected
52	NC	Not Connected	Not Connected	52	NC	Not Connected	Not Connected

Table 8-5 Pin Descriptions for Header H1 and H2

6

NODE	HEADER	CUBESAT KIT NAME	NOTES
+5V BUS	2.25-26	+5V	5V Regulated **Bus** Output
+3.3V BUS	2.27-28	VCC SYS	3.3V Regulated **Bus** Output
BATT POS	2.33-34	SW0	Positive Terminal of Battery (**not** Battery Bus) **DO NOT CONNECT**
PCM IN	2.35-36	SW1	(Switches →) Input to PCMs and PDMs
DUMMY LOAD	2.37-38	SW2	(Switches →)
N/C	2.39-40	SW3	(Switches N/C) Unused connection of launch switch closed state
BCR OUT	2.41-44	SW4	Output of BCRs (→ Switches)
BCR OUT	2.41-44	SW5	Output of BCRs (→ Switches)
BATTERY BUS	2.45-46	VBATT+	Battery Unregulated **Bus** Output

Table 8-6 Header pin name descriptions relating CubeSat Kit names to CS names

8.8 Switch Options

The Clyde Space EPS has three connection points for switch attachments, as shown in Figure 8-7. There are a number of possible switch configurations for implementation. Each configuration must ensure that the buses are isolated from the arrays and battery during launch. The batteries should also be isolated from the BCRs during launch in order to conform to Cubesat standard (RD-1).

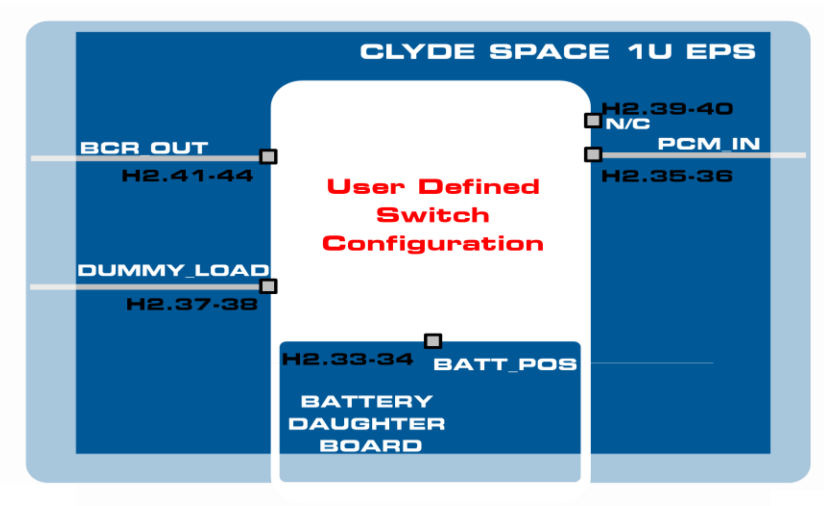


Figure 8-7 Switch connection points

Dummy Load

The Dummy Load is available as an additional ground support protection system, providing a load for the BCRs when the pull pin is inserted using the normally open (NO) connection of the Pull Pin. By connecting this Dummy Load to the NO pin BCR damage can be circumvented. The wiring arrangement for the dummy load is indicated in Figure 8-8.

The load protects the battery charge regulator from damage when the USB or array power is attached and the batteries are not connected. This system is not operational during flight and is only included as a ground support protection.

The Clyde Space Dummy Load system has been a standard feature from revision D of the EPS onwards. If the Dummy Load is required for an earlier revision please contact Clyde Space for fitting instructions.

Options 1 and 2 below are two suggested methods of switch configuration, but are by no means exhaustive. If you wish to discuss other possible configurations please contact Clyde Space.

Option 1

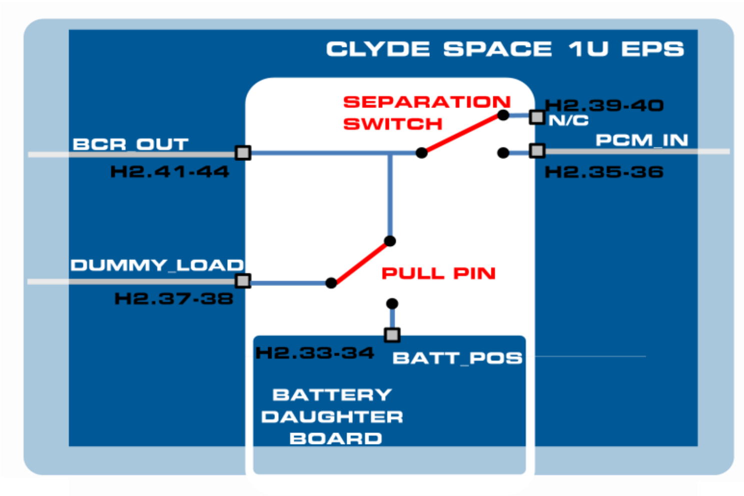


Figure 8-8 Switch Configuration Option 1

Option 1 accommodates the CubeSat Kit bus available switches offering two-stage isolation. The separation switch provides isolation of the power buses during the launch. The pull pin may be used for ground based isolation of the batteries, though it does not provide any isolation during launch.

NOTE: The second generation Clyde Space EPS has zero-current draw when the pull pin is removed – i.e. there will be no current drawn from the battery while on the launch vehicle.

When pull pin is inserted, the battery is isolated from the output of the BCRs. Under these conditions, if power is applied to the input of the arrays, or by connecting the USB there is a possibility of damaging the system. In order to mitigate this risk a “Dummy Load” fitted on the EPS.

Option 2

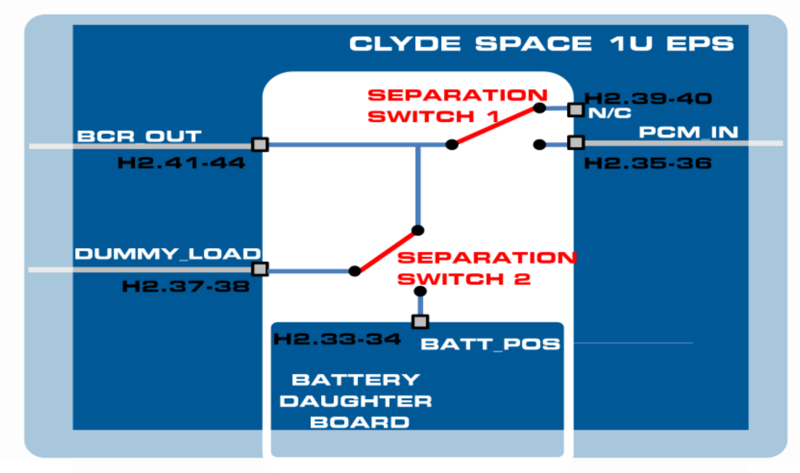


Figure 8-9 Switch Configuration Option 2

Option 2 is compatible with structures incorporating two separation switches, providing complete isolation in the launch configuration. The dummy load is not activated in this configuration.

Care should be taken to ensure that the switches used are rated to the appropriate current levels.

Please contact Clyde Space for information on implementing alternative switch or dummy load configurations.

8.9 Battery Connection

Connection of the battery systems on the 1U EPS is via the fixing screws for power transfer and an additional telemetry connector for all signals. Once mounted on the EPS, the pins on the mother board are live. When integrating the mother board ensure that the pins are aligned, and located in the correct position, as any offset can cause the battery to be shorted to ground, leading to catastrophic failure of the battery and damage to the EPS. Failure to observe these precautions will result in the voiding of any warranty.

When integrating to the bus ensure that the pins are aligned, and located in the correct position, as any offset can cause the battery to be shorted to ground, leading to catastrophic failure of the battery and damage to the EPS. Failure to observe these precautions will result in the voiding of any warranty.

When the battery is connected to the EPS, the battery will be fully isolated until implementing and connecting a switch configuration, as discussed in Section 8.8. Ensure that the battery is fully isolated during periods of extended storage.

When a battery board is connected to the CubeSat Kit header, there are live, unprotected battery pins accessible (H2.33-34). These pins should not be routed to any connections other than the switches and Clyde Space EPS, otherwise all protections will be bypassed and significant battery damage can be sustained.

8.10 Buses

All power buses are accessible via the CubeSat Kit headers and are listed and described in Table 8-5. These are the only power connections that should be used by the platform as they follow all battery and bus over-current protections.

All I^2C communications can are accessible via the CubeSat Kit header. See Section 11.

9. Technical Description

This section gives a complete overview of the operational modes of the EPS and battery and the testing undertaken to ensure their suitability for space. It is assumed that a complete Clyde Space system is in operation for the following sections.

9.1 Charge Method

The BCR charging system has two modes of operation: Maximum Power Point Tracking (MPPT) mode and End of Charge (EoC) mode. These modes are governed by the state of charge of the battery.

MPPT Mode

If the battery voltage is below the preset EoC voltage the system is in MPPT mode. This is based on constant current charge method, operating at the maximum power point of the solar panel for maximum power transfer.

EoC Mode

Once the EoC voltage has been reached the BCR changes to EoC mode, which is a constant voltage charging regime. The EoC voltage is held constant and a tapering current from the panels is supplied to top up the battery until at full capacity. In EoC mode the MPPT circuitry moves the solar array operation point away from the maximum power point of the array, drawing only the required power from the panels. The excess power is left on the arrays as heat, which is transferred to the structure via the array's thermal dissipation methods incorporated in the panels.

The operation of these two modes can be seen in Figure 9-1.

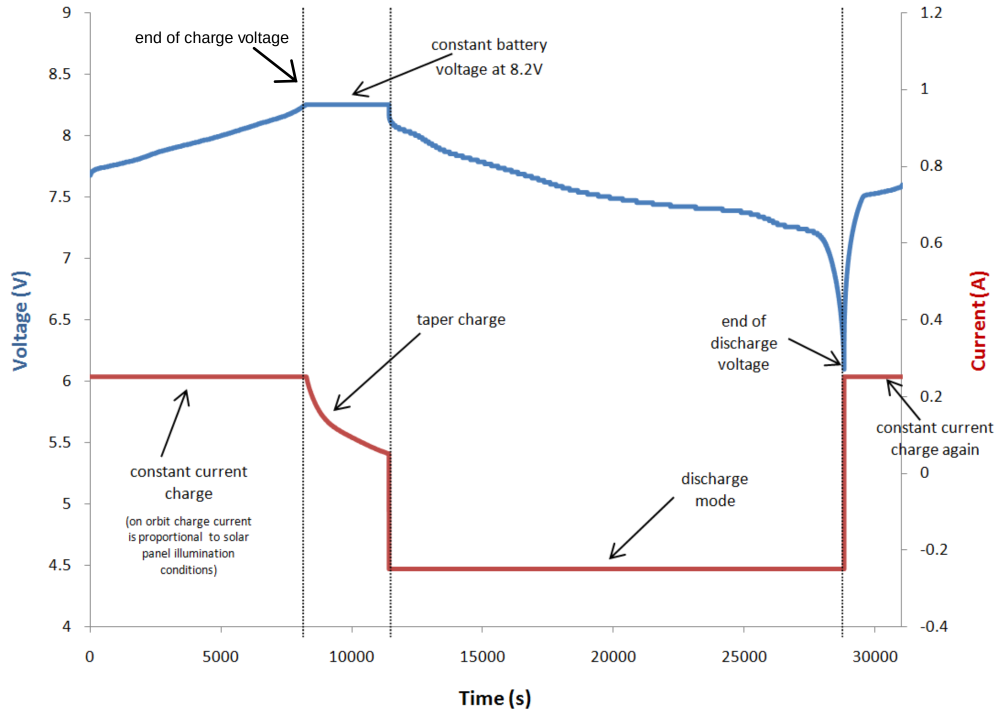


Figure 9-1 Tapered charging method

The application of constant current/constant voltage charge method on a spacecraft is described in more detail in RD-5. In this document there is on-orbit data showing the operation and how the current fluctuates with changing illumination conditions and orientation of the spacecraft with respect to the Sun.

9.2 BCR Power Stage Overview

As discussed in Section 8 the EPS has three separate, independent BCRs, each designed to interface to two parallel solar arrays on opposing faces of the satellite.

The design offers a highly reliable system that can deliver up to 80% of the power delivered from the solar array network at full load.

3W BCR Power Stage Design

Each 3W BCR uses a high efficiency SEPIC converter, interfacing to solar arrays of two triple junction cells in series. This will deliver up to 80% output at full load. The BCR will operate with an input of between 3V and 6V and a maximum output of 8.26V (7.4V nominal).

9.3 MPPT

Each of the BCRs can have two solar arrays connected at any given time; only one array can be illuminated by sunlight, although the other may receive illumination by albedo reflection from earth. The dominant array is in sunlight and this will operate the MPPT for that BCR string. The MPPT monitors the power supplied from the solar array. The data from this is then used to calculate the maximum power point of the array. The system tracks this point by periodically adjusting the BCRs to maintain the maximum power derived from the arrays. This technique ensures that the solar arrays can deliver much greater usable power, increasing the overall system performance.

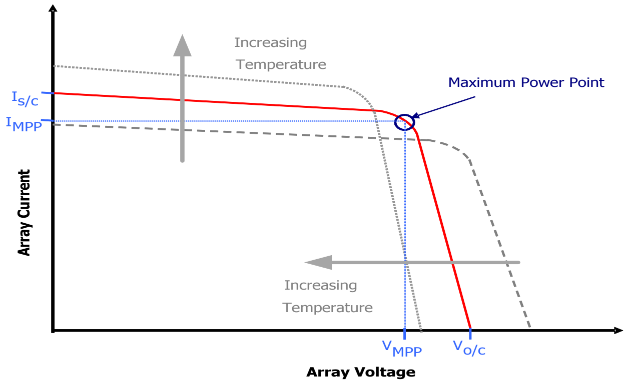


Figure 9-2 Solar Array Maximum Power Point

The monitoring of the MPP is done approximately every 2.5 seconds. During this tracking the output voltage from the array will step to o/c voltage, as shown in Figure 9.3.

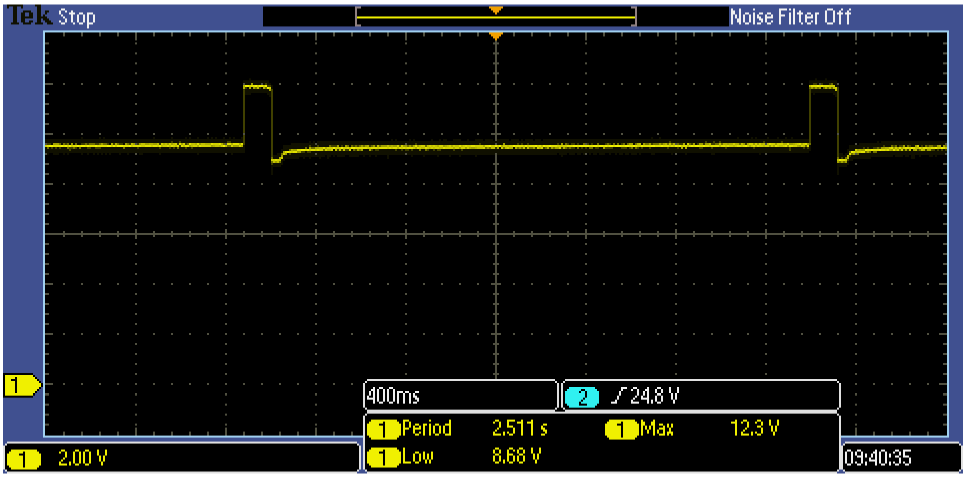


Figure 9-3 Input waveform with Maximum Power Point Tracking

9.4 Discharge

⚠ The central section in Figure 9.1 shows the profile of a full discharge of the battery at a C/5 rate (0.25A for a 2s1p battery). A full discharge cycle is carried out on all Clyde Space batteries prior to shipment to verify their capacity. In order to maximise the cycle life of the battery, it is recommended to discharge the battery to a maximum of 20% DoD.

9.5 5V and 3.3V PCM

The 5V and 3.3V regulators both use buck switching topology regulators as their main converter stage. The regulator incorporates intelligent feedback systems to ensure the voltage regulation is maintained to +/- 1% deviation. The efficiency of each unit at full load is approximately 96% for the 5V CPM and 95% for the 3.3V PCM. Full load on each of the regulator have a nominal output current of 2.5A (which is upgradable to 4.5A). Each regulator operates at a frequency of 480 kHz.

9.6 Battery Heater

Each battery board has its own autonomous heater, designed to maintain the temperature of the batteries above 0°C to maximise the capacity of the battery.

The heater is controlled by a thermostat circuit with hysteresis. This monitoring circuit is normally active, drawing ~2.5mW from the 5V Bus. When the temperature of the board drops below 0°C the heater on each board will switch on, drawing approximately 0.22W from the 3.3V Bus. This can be observed via the current telemetry on the 3.3V Bus. Once the temperature rises above 5°C the heater will switch off again.

The heater can be forced and held off with a telecommand, as described in Section 11, allowing a reduction in power consumption if required (~2.5mW from the 5V Bus). If this command is sent the battery temperature may drop below zero, reducing the achievable capacity of the batteries, as discussed in Section 9.7. Once this command has been sent all heaters will remain off. By resetting this command the heater can be re-enabled, at which point the thermostat circuit will become operational again. It is not possible to force the heater to switch on.

9.7 Cell Lot Acceptance Testing

In order to determine the cell's suitability for space applications, Clyde Space undertakes an extensive Lot Acceptance Testing regime. The process is detailed in this section.

Destructive Parts Analysis

Destructive Physical Analysis (DPA) of the cell reveals a stacked cell architecture, as shown in Figure 9-2.

The cell is hermetically sealed in a plastic coated foil casing. The cell 'stack' (pictured on the left hand side of the photograph in Figure 9-2) consists of 12 layers. The top layer is shown separated as far as possible in the figure. The individual components are well adhered (confirming the presence of a polymer electrolyte) but can be separated into; current collectors, separators, and active materials. The active material can be removed with a scalpel to reveal the copper electrode.

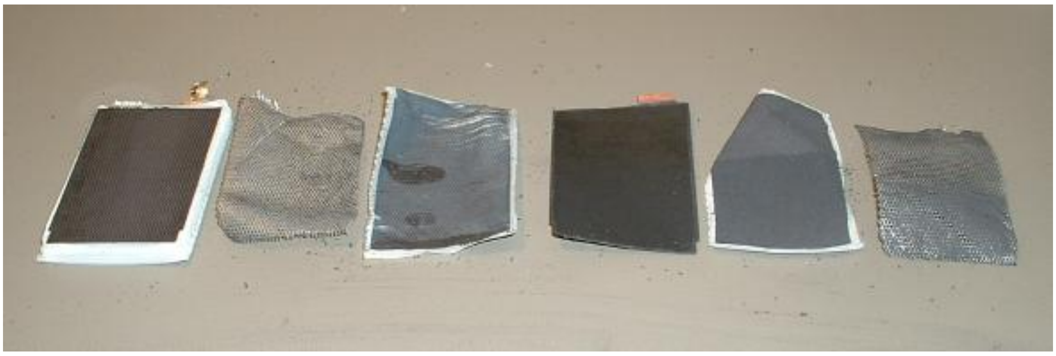


Figure 9-2 DPA showing separated cell components

Capacity Variation with Discharge Rate and Temperature

Discharge plots are shown in Figures 9-3 to 9-6 for rates of C/15, C/10, C/5, C/2 and C at 40°C (Figure 9-3), 20°C (Figure 9-4), 0°C (Figure 9-5), and -20°C (Figure 9-6). In Figures 9-7 to 9-11, capacities for each discharge rate are compared for all temperatures. Note that these measurements were carried out per cell. A summary of the results is shown in Table 9-1.

T (°C)	Discharge Rate and (measured capacity (Ah))				
40	C/15 (1.437)	C/10 (1.435)	C/5 (1.283)	C/2 (1.208)	C (1.171)
20	C/15 (1.501)	C/10 (1.430)	C/5 (1.276)	C/2 (1.226)	C (1.145)
0	C/15 (1.358)	C/10 (1.294)	C/5 (1.161)	C/2 (0.716)	C (0.182)
-20	C/15 (1.055)	C/10 (0.914)	C/5 (0.568)	C/2 (0.044)	C (0.026)

Table 9-1 Measured capacities at different discharge rates and temperatures.

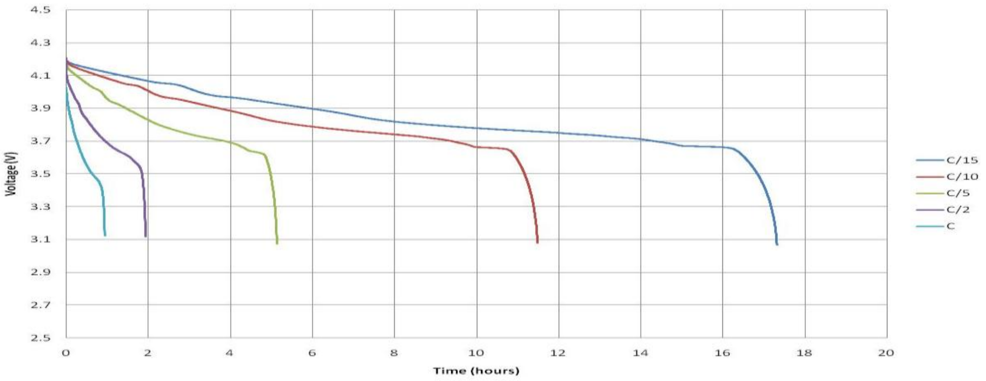


Figure 9-3 Discharge traces at 40°C at C/15, C/10, C/5, C/2, and C rates

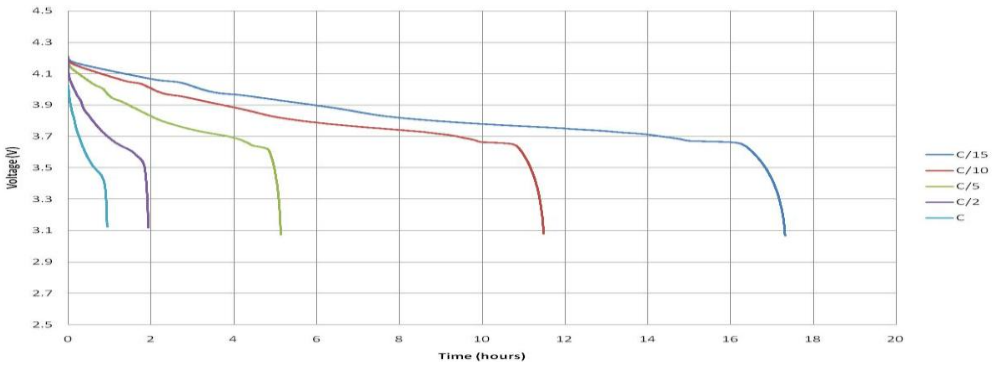


Figure 9-4 Discharge traces at 20°C at C/15, C/10, C/5, C/2, and C rates

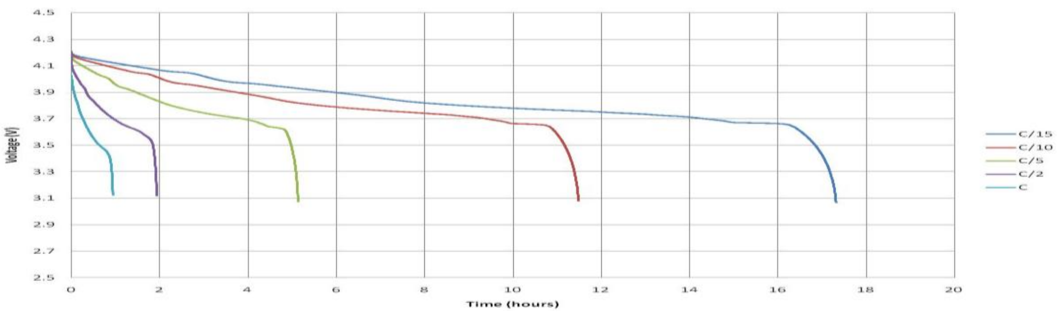


Figure 9-5 Discharge traces at 0°C at C/15, C/10, C/5, C/2, and C rates

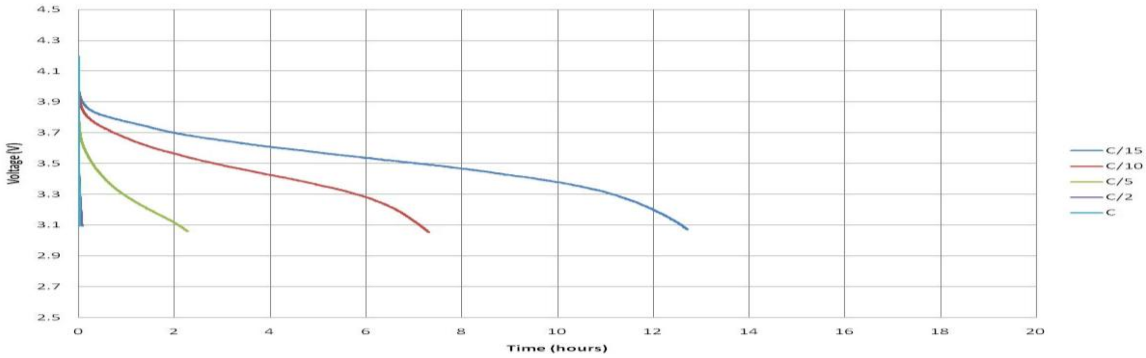


Figure 9-6 Discharge traces at -20°C at C/15, C/10, C/5, C/2, and C rates

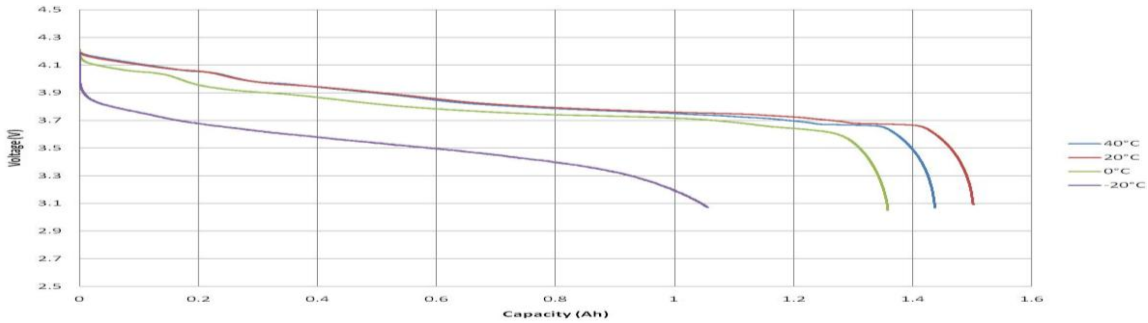


Figure 9-7 Discharge traces at C/15 rate, at different temperatures.

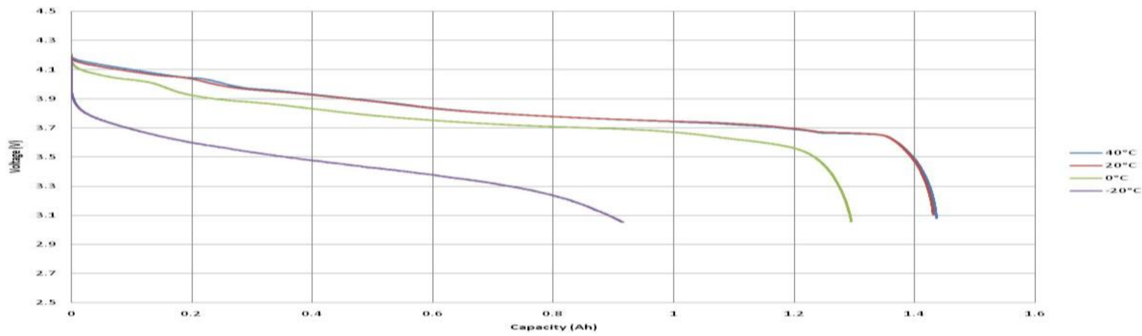


Figure 9-8 Discharge traces at C/10 rate, at different temperatures.

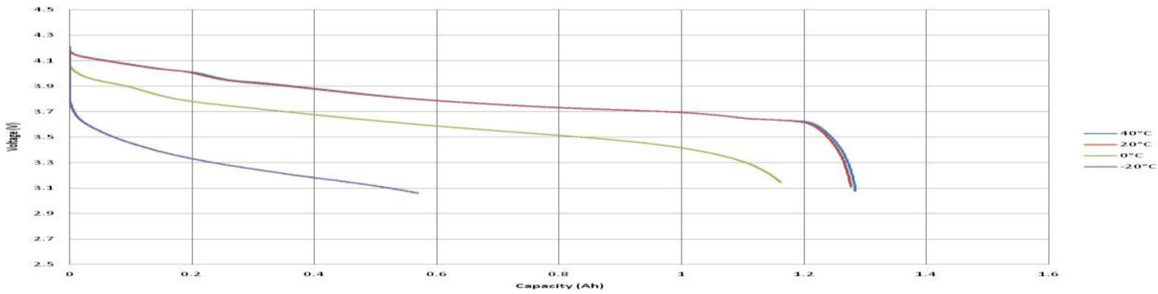


Figure 9-9 Discharge traces at C/5 rate, at different temperatures

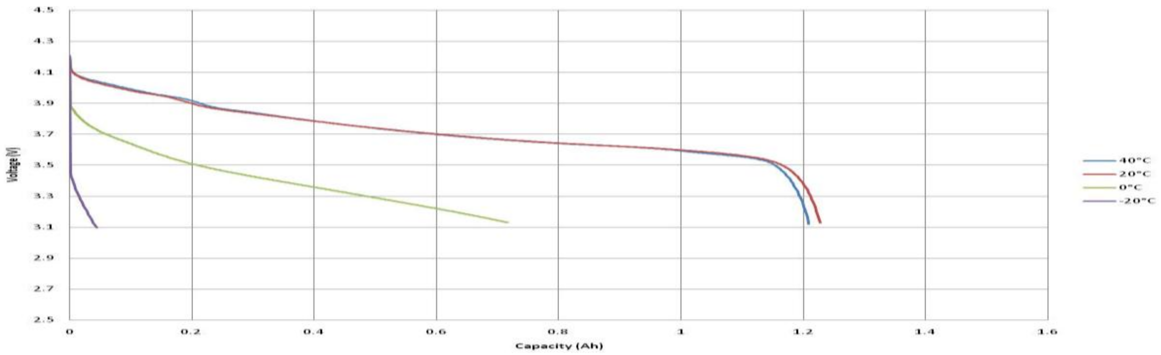


Figure 9-10 Discharge traces at C/2 rate, at different temperatures.

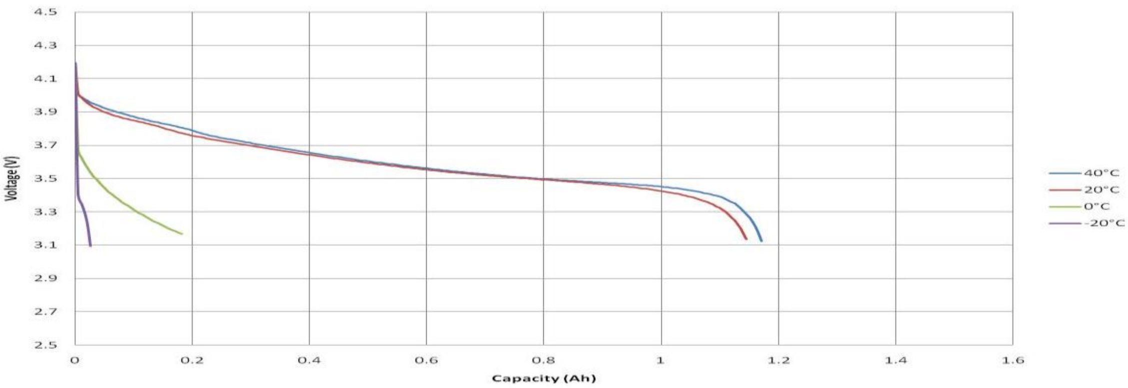


Figure 9-11 Discharge traces at C rate, at different temperatures.

Self Discharge/Optimum Storage Condition

Optimum storage conditions were examined at different temperatures and depths of discharge. The results indicated that the best conditions in which to maintain the cell, and therefore battery capacity, are to store at a depth of discharge around 50% (~7.4V), and at temperatures between -10°C and +10°C. It is therefore recommended that when not in use, batteries are stored in a refrigerator, or similar.

Vacuum Cycling

Vacuum cycling was carried out in a chamber at 19mbar pressure and at ambient temperature. A plot of cell voltage vs. time for 10 cycles is shown in Figure 9-12. Capacity variation with cycle number is indicated in Table 9-2.

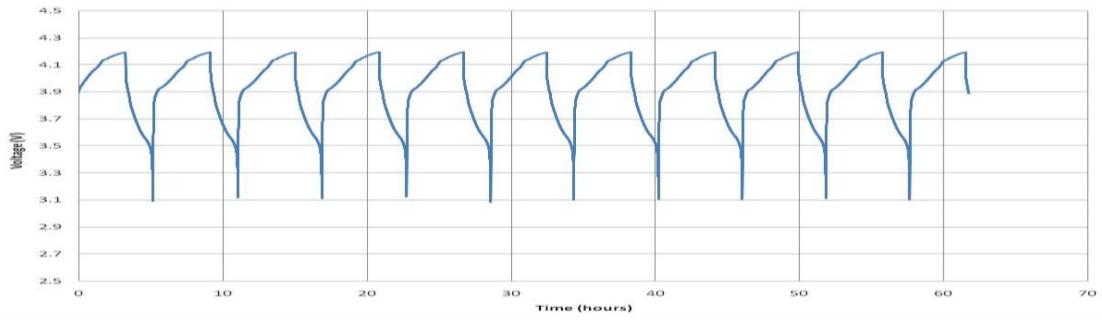


Figure 9-12 Cell cycled at C/2 rate in a vacuum of 19mbar

Cycle number	Capacity (Ah)
1	1.193
2	1.193
3	1.172
4	1.200
5	1.198
6	1.190
7	1.197
8	1.195
9	1.190
10	1.187

Table 9-2 Cell capacity variation with vacuum cycle number

No change in cell weight was observed following the vacuum cycling (weights measured to 2 decimal places), and there was no evidence of any cell leakage, or any unusual behaviour in the cycling profile.

The cell capacity varied slightly with subsequent cycles with a decrease of 0.5% in the measured capacity between cycle 1 and cycle 10.

Standard capacity measurements were carried out following the vacuum cycling. Very little difference was seen in the capacity measured before and after vacuum cycling (1.257Ah before, 1.243Ah after). Vacuum cycling therefore did not have any significant detrimental effect on the cell capacity.

Although the cells 'bulge' in a vacuum, the stack arrangement of the cell, and use of polymer electrolyte means that there is no separation of cell components in a vacuum, and therefore little effect on the cell cyclability.

EMF vs SoC

Cells were cycled at a slow rate, C/50, in order to minimise the cell internal resistance and therefore measure the cell capacity. This test was carried out at room temperature.

A plot of voltage vs. capacity is shown in Figure 9-13.

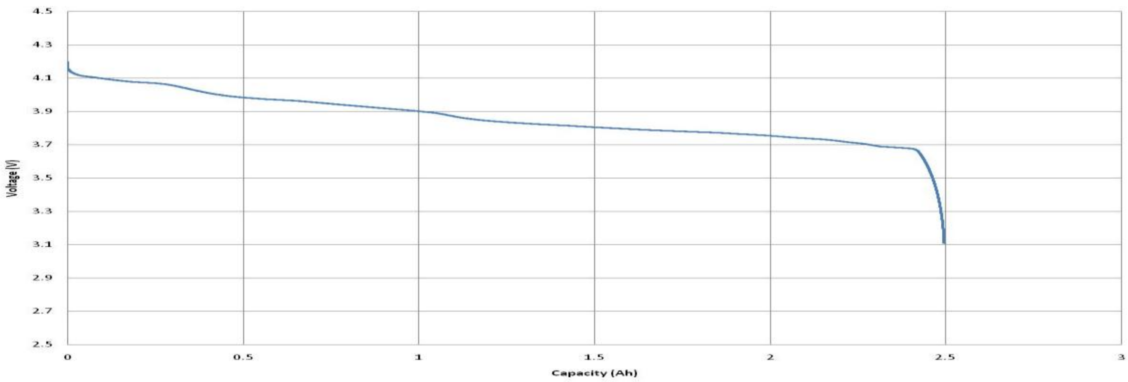


Figure 9-13 Discharge trace at C/50 rate at 20°C.

The capacity of the cell discharged at C/50 was 2.495Ah, which is almost double the cell nameplate capacity and indicates the effect of internal resistance on the cell capacity. Internal resistances have been estimated from previous figures at the cross-over point from discharge to charge. Cells cycled at C/2 have an estimated internal resistance of ~0.525ohms, and at C/5 an estimated internal resistance of ~0.412ohms. These figures show that the cell internal resistance increases as the charge/discharge rate also increases.

In Table 9-3, the cell voltage at different depth of discharge is shown for discharge rates of C/5 compared with C/50. It is clear from the table that the voltage remains higher as the discharge progresses at C/50 rate compared to C/5.

DoD (%)	Voltage of cell discharged at C/5 (V)	Voltage of cell discharged at C/50 (V)
0	4.200	4.200
5	4.078	4.091
10	4.030	4.069
15	3.994	4.022
20	3.918	3.983
25	3.890	3.967
30	3.861	3.946
35	3.829	3.923
40	3.799	3.902
45	3.775	3.862
50	3.756	3.835
55	3.738	3.820
60	3.722	3.805
65	3.709	3.791
70	3.700	3.780

DoD (%)	Voltage of cell discharged at C/5 (V)	Voltage of cell discharged at C/50 (V)
75	3.692	3.769
80	3.676	3.754
85	3.646	3.736
90	3.627	3.710
95	3.581	3.682
100	3.000	3.000

Table 9-3 Voltage variation with DoD at C/5, and at C/50

10. General Protection

The EPS and batteries have a number of inbuilt protections and safety features designed to maintain safe operation of the EPS, battery and all subsystems supplied by the EPS buses.

10.1 Over-Current Bus Protection

The EPS features bus protection systems to safeguard the battery, EPS and attached satellite sub-systems. This is achieved using current monitors and a shut down network within the PDMs.

Over-current shutdowns are present on all buses for sub system protection. These are solid state switches that monitor the current and shutdown at predetermined load levels, see Table 10-1. The bus protection will then monitor the fault periodically and reset when the fault clears. The fault detection and clear is illustrated in the waveform in Figure 10-1.

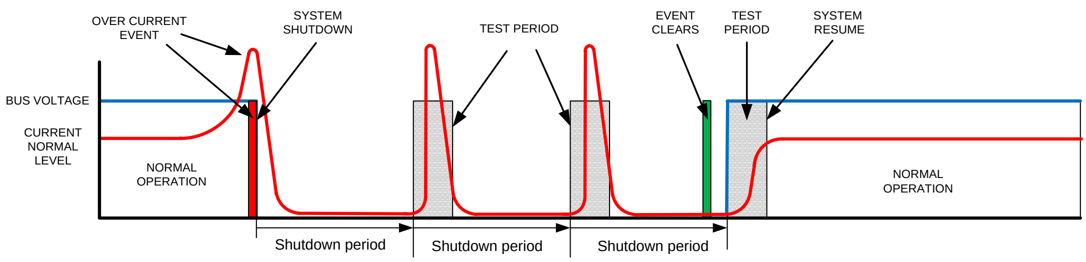


Figure 10-1 Current protection system diagram

Bus	Period	Approximate Duration (ms)
Battery Bus	Shutdown period	650
	Test period	60
5V Bus	Shutdown period	585
	Test period	30
3.3V Bus	Shutdown period	525
	Test period	30

Table 10-1 Bus protection data

10.2 Battery Under-voltage Protection

In order to prevent the over-discharge of the battery the EPS has inbuilt under-voltage shutdown. This is controlled by a comparator circuit with hysteresis. In the event of the battery discharging to ~6.2V (slightly above the 6.1V that results in significant battery degradation) the EPS will shutdown the supply buses. This will also result in the I^2C node shutting down. When a power source is applied to the EPS (e.g. an illuminated solar panel) the battery will begin charging immediately. The buses, however, will not reactivate until the battery voltage has risen to ~7V. This allows the battery to charge to a level capable of sustaining the power lines once a load is applied.

It is recommended that the battery state of charge is monitored and loading adjusted appropriately (turning off of non critical systems) when the battery capacity is approaching the lower limit. This will prevent the hard shutdown provided by the EPS.

Once the under-voltage protection is activated there is a monitoring circuit used to monitor the voltage of the battery. This will draw approximately 2mA for the duration of shutdown. As the EPS is designed for LEO orbit the maximum expected period in under-voltage is estimated to be ~40mins. When ground testing this should be taken into consideration, and the battery should be recharged within 40mins of reaching under-voltage, otherwise permanent damage may be sustained.

10.3 Over-current Polyswitch Protection

A polyswitch is fitted in line with each string of the battery. This is a resettable fuse, designed to blow when an over-current, either charge or discharge, is observed by the string. The approximate fusing currents are shown in Table 10-1

Temperature (°C)	Approximate Trip Current (A)
-40	7.0
-20	6.3
0	5.5
20	5.0
40	4.0
60	3.3

Table 10-1 Polyswitch Trip Current Variation with Temperature

If the cause of the over-current subsequently clears, the fuse will reset, allowing current to flow to and from the battery again.

Once a polyswitch has been fused and reset once the resistance is unknown – as such the efficiency may be degraded following this event. Hence, if a polyswitch is fused during ground testing, it should be replaced.

11. TELEMETRY AND TELECOMMAND

The telemetry system monitors certain stages of the power system and battery while also allowing a small degree of control over the PDM stages and battery heater. The telemetry system transfers data via an I^2C bus. The telemetry system operates in slave mode and requires an I^2C master to supply commands and the clock signal. Control systems within the EPS offer the user the ability to temporarily isolate the EPS buses from the on-board computer systems.

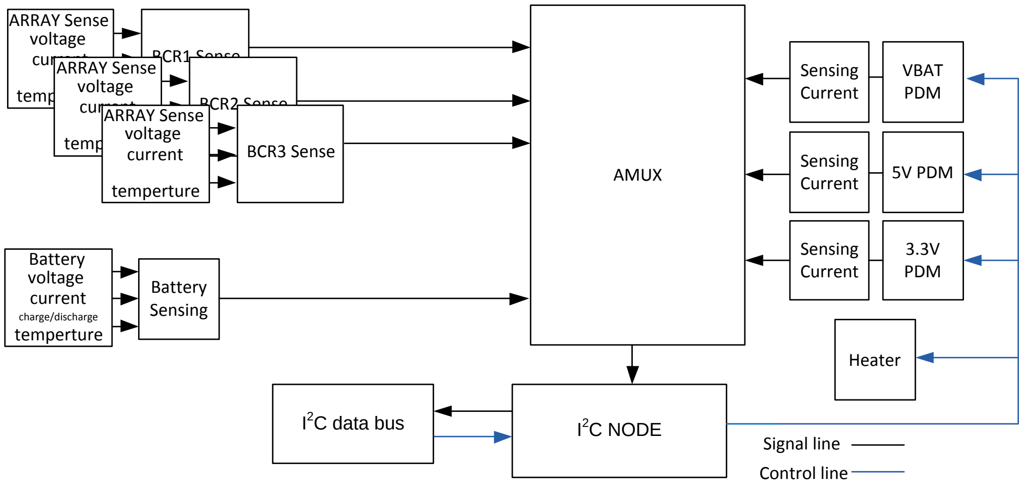


Figure 111-1 Telemetry functional diagram

11.1 I^2C Node

The I^2C Node is based on the Microchip PIC16F690. The device node is configured to act as a single channel analogue to digital converter. The microcontroller controls the analogue multiplexer that routes the signals from the sensors. The PIC16F690 program is designed to operate as a slave sensor node on the I^2C bus. The program will select and then convert the desired signal data from the telemetry network on demand. There is also a control feature that can briefly shutdown PDMs within the EPS.

The following sections briefly describe the hardware that is used.

Analogue Multiplexer

A 32 channel analogue multiplexer is used for selecting the correct sensor signal. The multiplexer is controlled from the microcontroller.

Additional Hardware

Further required hardware includes an oscillator and an I^2C bus extender. The oscillator provides a robust clock signal for the microcontroller. The bus extender provides greater robustness to signal noise on the I^2C bus during integration and operations.

11.2 I^2C Command Interface

All communications to the Telemetry and Telecommand, TTC, Node are via an I^2C interface. The TTC Node is configured as a slave and only responds to direct commands from a master I^2C node. No unsolicited telemetry is transmitted. A maximum 400Kbit bus speed is supported, with typical bus speeds of 100Kbit. The address of the TTC Node is factory set. The address is 0x2D.

Message Formats

Two message structures are available to the master; a write command and a read command. The write command is used to initiate an event and the read command returns the result. All commands start with the 7 bit slave address and are followed by two data bytes. The first data byte should be the command. The second byte represents the data that is used as part of the command. An example of the data is the analogue to digital channel to read.

An example of a read command would be:

- The master transmits the slave address with write flag, command type (0x00) and data (ADC channel)
- The slave acts on the commands, sets the correct channel and reads the analogue to digital converter
- The master transmits the slave address with read flag
- The slave responds with a two-byte value

If a read message does not have a preceding write message, the value 0xF000 is returned. All bit level communication to and from the board is done by sending the MSB first. If both bytes are not read then the system may become unstable.

ADC

The I²C node acts as a multi channel Analogue to digital convertor which allows the board to supply sensor data to the user. When the command is received, a delay, approximately 1.2ms, is inserted to allow the analogue reading to settle. After this delay the result can be retrieved. The result is a 10 bit value with the first byte received containing the two most significant bits and the second byte received the remaining 8 bits.

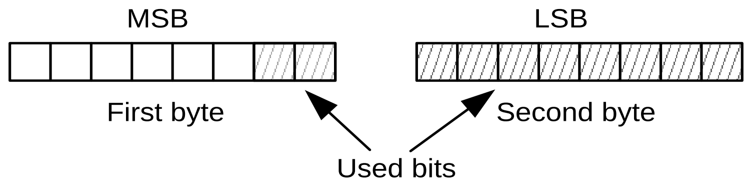


Figure 11-2 ADC 10bit data packet

To retrieve a sensor reading the following procedure should be used:

Send 0x00 followed by 0x0*X*, where *X* represents the channel number in Hex format. This instructs the I²C node that the user wishes to retrieve a sensor value and which sensor to take the reading from.

After a small delay, approximately 1.2ms, the user can issue a read command and the result will be transmitted. The most significant byte is sent first followed by the least significant byte.

The result received should then be entered into the conversion equations, covered in a further section, which calculates the requested parameter.

If the reading is not yet ready 0xF000 is returned

This process should be followed for all ADC channels.

11.3 Command Summary

Table 11-1, below, provides a list of the commands for the EPS. The data that should accompany the commands is included in the table. Descriptions of the commands follow the table.

Command Type		Command Value Range	Description
Decimal	Name	Decimal	
0	ADC	0-31	Read ADC Channel
1	Status	N/A	Request Status Bytes
2	PDM Off	0-7	Turns off the selected PDM for a short time
4	Version	N/A	Request Firmware Version
5	Heater Force Off	0-1	Forces Battery Heater off
128	Watchdog	N/A	Causes a soft reset of the micro

Table 11-1 Command Summary

Status

The status bytes are designed to supply operational data about the I^2C Node. To retrieve the two bytes that represent the status the command 0x01 should be sent. The meaning of each bit of the status byte is shown in Table 11-2.

PDM Off

There may be a time when the user wishes to turn of the PDM's for a short period. They may wish to do this to create a hard reset of a circuit. To carry this out the command 0x0002 is sent followed by the data byte. The data byte has a range of 0 to 7. Bit 0 corresponds to the battery bus, bit 1 the 5V bus and bit 2 the 3.3V bus. Any combination of busses can be turned off, however is should be noted that if the user switches the 3.3V PDM off the I^2C node will be reset.

Version

The firmware version number can be accessed by the user using this command. Please contact Clyde Space to learn the version number on your board.

WatchDog

The Watchdog command allows the user to force a reset of the I^2C node. If the user detects or suspects an error in the operation of the I^2C node then this command should be issued. When issued the I^2C node will reset and return to an initial state.

Heater

Pin 10 of the PIC microcontroller (RB7) is configured as an override control for the battery heater. The heater can only be turned off, it cannot be forced on. This is controlled by the board temperature.

If a value of 0x01 is written as the command value, the output is driven high (turning the heater off). The heater will remain off until a value of 0x00 is written as the command value, allowing the thermostat circuit to take control of the heater.

If any other command values written, the command is ignored and UnknownCommandValue is set (bit1, byte 0 of TTC status).

Byte	Bit	Description	If Low (0)	If High (1)	Note
0	0	Unknown Command Type	Last command OK	Last Command Unknown	Bit cleared when read
	1	Unknown Command Value	Last Command Value OK	Last Command Value Out of Range	Bit cleared when read
	2	ADC Result Not Ready	ADC Result Ready	ADC Result Not Ready	Bit cleared when read
	3	Not Used	-	-	Reads as '0'
	4	Oscillator bit	External Oscillator running	External Oscillator failure	-
	5	Watchdog Reset Occurred	No Watchdog Reset	Watchdog Reset Occurred	Bit cleared when read
	6	Power On Reset Occurred	Power On Reset Occurred	No Power On Reset Occurred	Bit cleared when read
	7	Brown Out Reset Occurred	Brown Out Reset Occurred	No Brown Out Reset Occurred	Bit cleared when read
1	0	I2C Error	No I2C Errors	I2C Error Occurred	Bit cleared when read
	1	I2C Write Collision	No I2C Write Collision	I2C Write Collision Occurred	-
	2	I2C Overflow	No I2C Overflow	I2C Overflow Occurred	-
	3	Received Message too Long	Received Messages Correct Length	Last Message incorrect Length	
	4-7	Not Used	-	-	Reads as '0'

Table 11-2 Status Bytes

11.4 ADC Channels

Each of the analogue channels, when read, returns a number between 0-1023. To retrieve the value of the analogue signal this number, ADC, is to be entered into an equation. When the equation is used the value calculated is the value of the input analogue signal. Table 11-4 contains example equations of the conversions of each of the channels. To get more accurate equations full calibration test should be carried out.

ADC Channel	Signal	Approx Conversion Equations	Units	Notes
0	GND	*NA*	-	
1	Array +Y Current	*-0.5 x ADC count +515.7*	*mA*	
2	Array +Y Temperature	*-0.163 x ADC Count +110.338*	*°C*	
3	Array pair Y Voltage	*-0.0086 x ADC Count +8.81*	*V*	
4	Array -X Current	*-0.5 x ADC count +515.7*	*mA*	
5	Array -X Temperature	*-0.163 x ADC Count +110.338*	*°C*	
6	Array pair X Voltage	*-0.0086 x ADC Count +8.81*	*V*	
7	Array +X Current	*-0.5 x ADC count +515.7*	*mA*	
8	Array +X Temperature	*-0.163 x ADC Count +110.338*	*°C*	
9	Array pair Z Voltage	*-0.0086 x ADC Count +8.81*	*V*	
10	Array +Z Current	*-0.5 x ADC count +515.7*	*mA*	
11	Array +Z Temperature	*-0.163 x ADC Count +110.338*	*°C*	
12	GND	*NA*	-	
13	Array -Y Current	*-0.5 x ADC count +515.7*	*mA*	
14	Array -Y Temperature	*-0.163 x ADC Count +110.338*	*°C*	
15	GND	*NA*	-	
16	GND	*NA*	-	
17	Battery Bus Current	*-3.153 x ADC Count + 3250.815*	*mA*	
18	BAT1 Temperature	*-0.163 x ADC Count +110.835*	*°C*	*CS-1UEPS2-20 only*
19	BAT1 Full Voltage	*-0.0939x ADC Count + 9.791*	*V*	*CS-1UEPS2-20 only*
20	GND	*NA*	-	
21	BAT1 Current Direction	*High – Bat charge* *Low Bat discharge*	*Chg/Dis* *Chg*	*CS-1UEPS2-20 only*
22	BAT1 Current	*-3.20 x ADC Count + 2926.22*	*mA*	*CS-1UEPS2-20 only*

23	BAT0 Temperature	*-0.163 x ADC Count +110.835*	*°C*	*CS-1UEPS2-10 and CS-1UEPS2-20 only*
24	BAT0 Full Voltage	*-0.0939x ADC Count + 9.791*	*V*	*CS-1UEPS2-10 and CS-1UEPS2-20 only*
25	GND	*NA*	*V*	
26	5V Bus Current	*-3.500 x ADC Count + 3611.509*	*mA*	
27	3.3V Bus Current	*-4.039 x ADC Count + 4155.271*	*mA*	
28	BAT0 Current Direction	*High – Bat charge* *Low Bat discharge*	*Chg/Dis Chg*	*CS-1UEPS2-10 and CS-1UEPS2-20 only*
29	BAT0 Current	*-3.20 x ADC Count + 2926.22*	*mA*	*CS-1UEPS2-10 and CS-1UEPS2-20 only*
30	Array -Z Temperature	*-0.163 x ADC Count +110.338*	*°C*	
31	Array -Z Current	*-0.5 x ADC count +515.7*	*mA*	

Table 11-3 ADC Channels

12. TEST

All EPS are fully tested prior to shipping, and test reports are supplied. In order to verify the operation of the EPS please use the following outlined instructions.

Step by step intro of how to connect and verify operation:

In order to test the functionality of the EPS you will require:

- EPS
- Battery (or simulated battery)
- Breakout Connector (with connections as per Figure 12-1)
- Array Input (test panel, solar array simulator or power supply and limiting resistor)
- Oscilloscope
- Multimeter
- Electronic Load
- Aardvark I2C connector (or other means of communicating on the i2c bus)

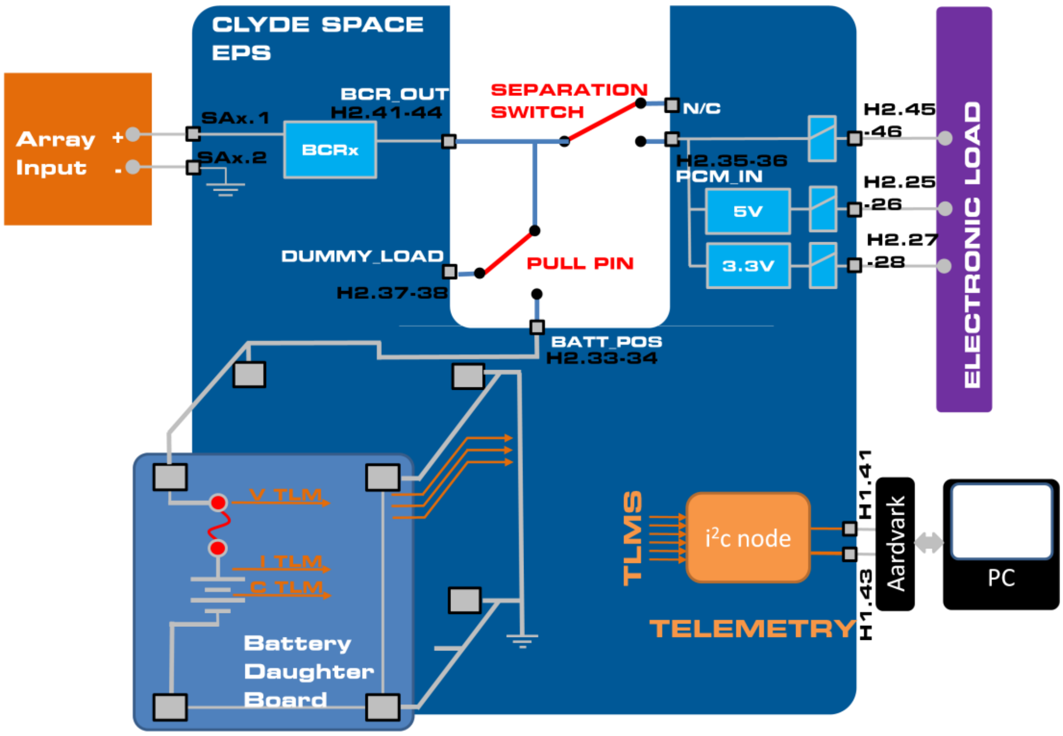


Figure 12-1 Suggested Test Setup

The breakout connector should be wired with the switch configuration to be used under mission conditions.

12.1 Power up/Down Procedure

The order of assembly should follow the order detailed below:

- Breakout connector assembled with switches set to launch vehicle configuration (as shown in Figure 12-1)
- Fit Breakout connector to EPS
- Connect battery to stack
- Connect electronic load (no load) to buses

- Remove Pull Pin
- Activate Separation Switch
- Connect array input

When powering down this process should be followed in reverse.

12.2 Solar Array Input

There are 3 options for the array input section:

- A solar array
- A solar array simulator
- A benchtop power supply with current limiting resistor

When using a solar array or solar array simulator the limits should not exceed those outlined in Table 12-1

	Voc (V)	Isc (mA)
BCR1 (SA1)	6.13	464
BCR2 (SA2)	6.13	464
BCR3 (SA3)	6.13	464

Table 12-1 solar array limits

When using a power supply and resistor setup to simulate a solar panel the required setup is shown in Figure 12-2.

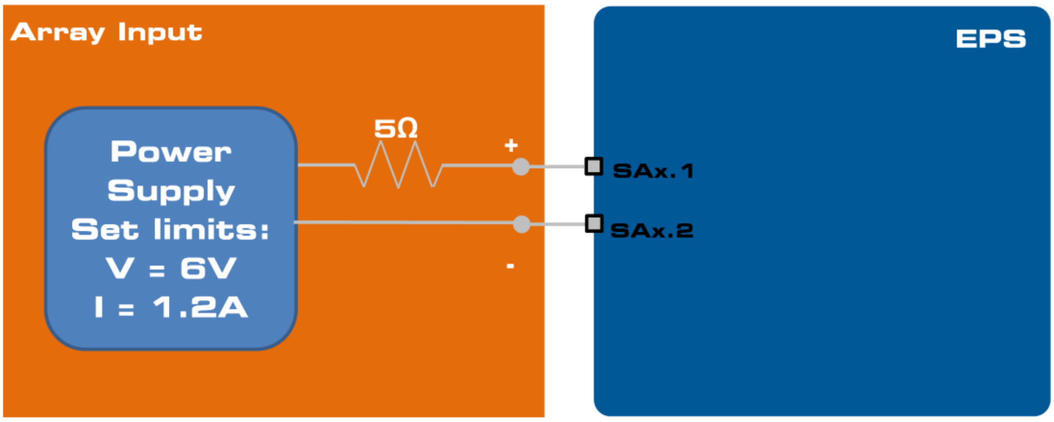


Figure 12-2 Solar Panel using power supply

12.3 Battery Setup

The system should be tested with a battery in the system. If a Clyde Space battery is not available this can be done using a power supply and load to simulate the behavior of a battery. This setup is shown in Figure 12-3.

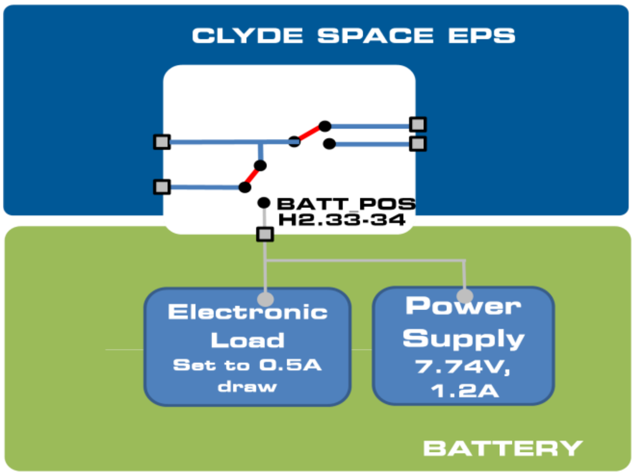


Figure 12-3 Simulated Battery Setup

12.4 Configuration and Testing

The following section outlines the procedure for performing basic functional testing

PCM Testing

In order to test the PCMs power must be applied to the PCM_IN connection. In order to do this the "Pull Pin" should be removed, connection the battery, as shown in Figure 12-4.

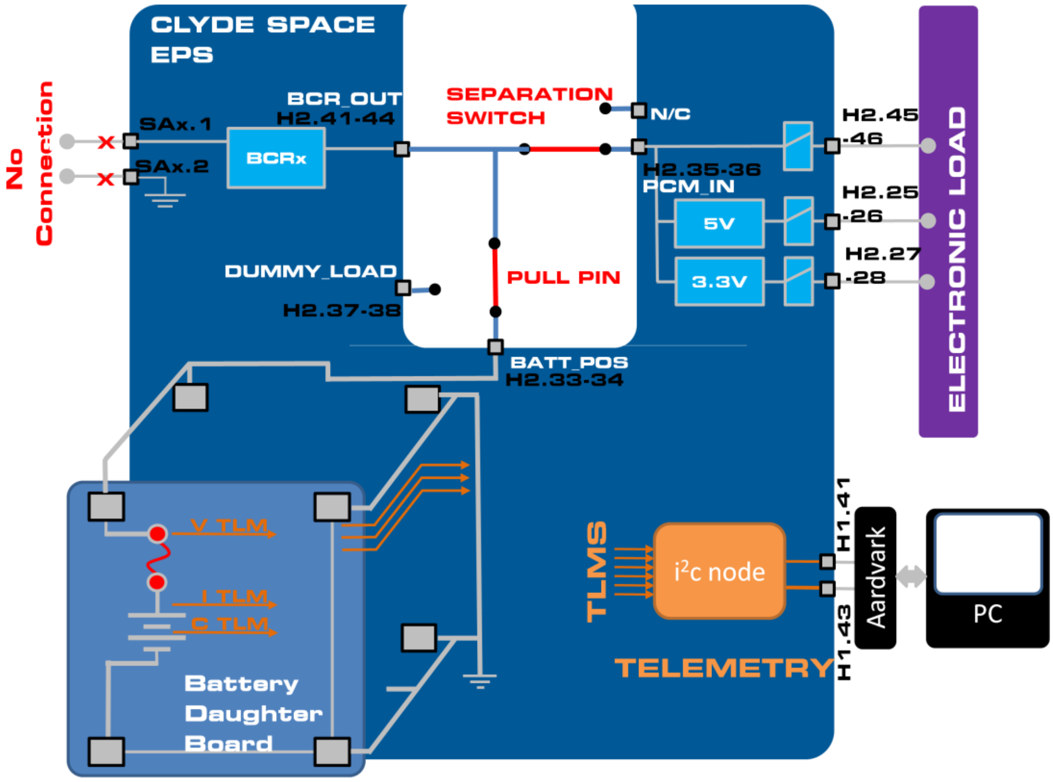


Figure 12-4 Test set-up with Pull Pin Removed

In this configuration all buses will be activated and can be measured with a multimeter.

By increasing the load on each of the buses you will be able to see the current trip points' activation, as discussed in Section 10.1.

Undervoltage Protection

When using a simulated battery it is possible to trigger the undervoltage protection. Using the same test setup as detailed above, with a simulated battery if the voltage is dropped to below ~6.2V the undervoltage will be activated. This can be observed by the power buses shutting down.

Note: This test takes the battery to 100% DoD and should always be followed by a charge cycle.

BCR Testing

In order to test the operation of the BCRs the separation switches should be moved to flight configuration, as shown in Figure 12-5, (with the pull pin still removed). Once this is done the array input can be connected.

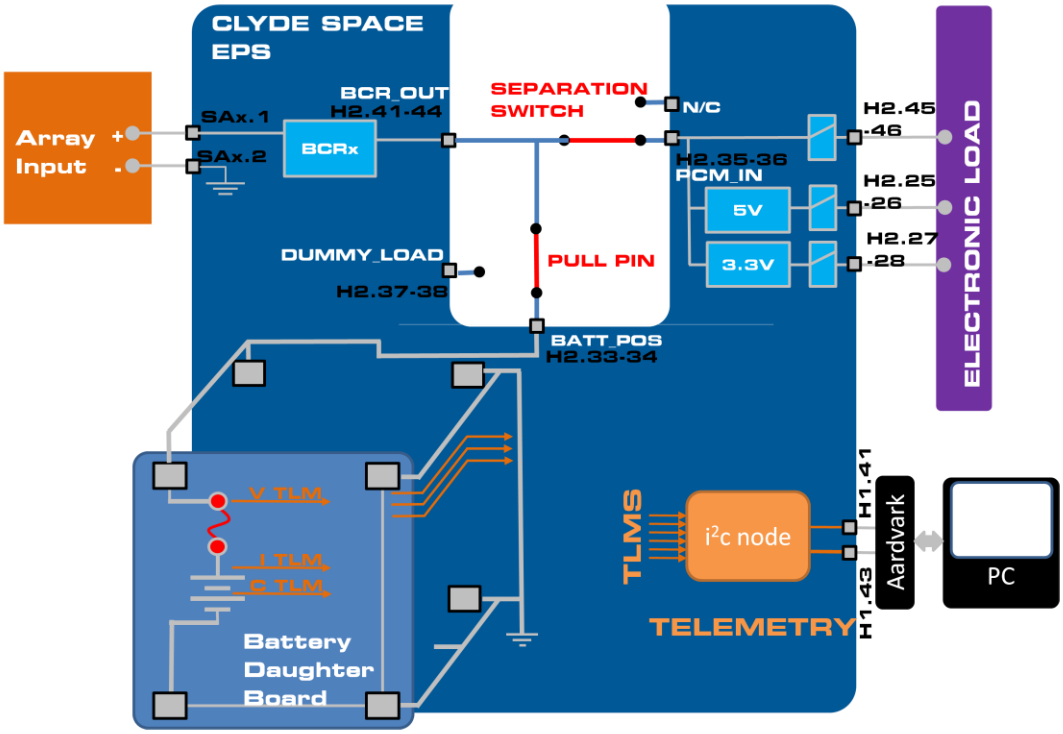


Figure 12-5 Test set-up in Flight Configuration

To check the operation of the BCR/MPPT an oscilloscope probe should be placed at pin 1 of the active solar array connector (not at the power supply). The wave form should resemble Figure 12-6.

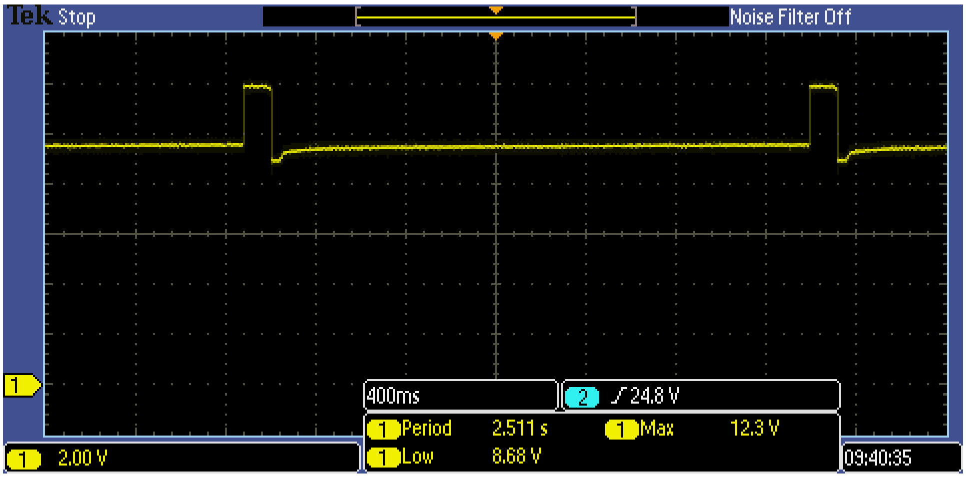


Figure 12-6 Waveform of Solar Array Input

EoC Operation

Using the test setup detailed in Figure 12-5 the EoC operation can be demonstrated. By raising the voltage of the simulated battery above ~8.26V the EoC mode will be activated. This can be observed using an ammeter coming from the Array input, which will decrease towards 0A (it will never actually reach 0A, closer to 10mA as the BCR low level electronics will still draw form the array).

5V USB Charging

Figure 12-7 shows the test setup for the 5V USB charging.

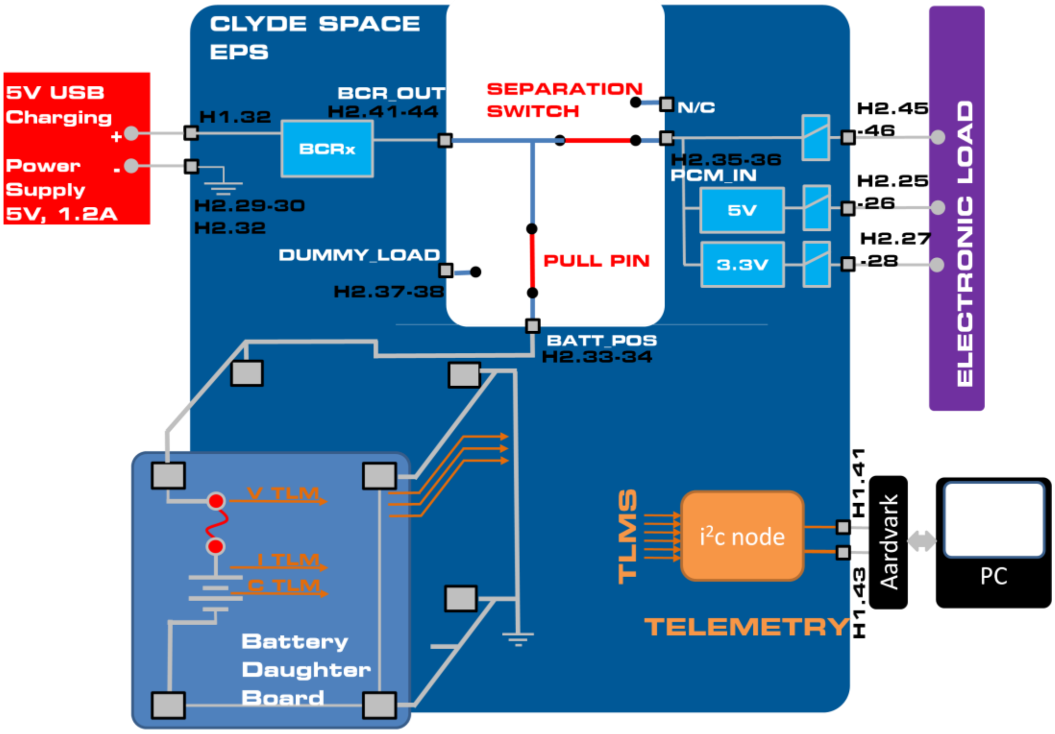


Figure 12-7 5V USB charge setup

This setup should only be used for top up charge on the battery, not for mission simulation testing.

13. DEVELOPER AIT

AIT of the EPS with other CubeSat modules or subsystems is the responsibility of the CubeSat developer. Whilst Clyde Space outlines a generic process which could be applicable to your particular system in this section we are not able to offer more specific advice unless integration is between other Clyde Space products (or those of compatible products), see Table 14-1. AIT is at the risk of the developer and particular care must be taken that all subsystems are cross-compatible.

Throughout the AIT process it is recommended that comprehensive records of all actions be maintained tracking each subsystem specifically. Photo or video detailing of any procedure also helps to document this process. Comprehensive records are useful to both the developer and Clyde Space; in the event of any anomalies complete and rapid resolution will only be possible if good records are kept. The record should contain at least;

- Subsystem and activity
- Dates and times of activity (start, finish, key milestones)
- Operator(s) and QAs
- Calibration of any equipment
- Other subsystems involved
- Method followed
- Success condition or results
- Any anomalous behaviour

Before integration each module or element should undergo an acceptance or pre-integration review to ensure that the developer is satisfied that the subsystem meets its specification through analysis, inspection, review, testing, or otherwise. Activities might include:

- Satisfactory inspection and functional test of the subsystem
- Review of all supporting documentation
- Review of all AIT procedural plans, identifying equipment and personnel needs and outlining clear pass/fail criteria
- Dry runs of the procedures in the plan

Obviously testing and analysis is not possible for all aspects of a subsystem specification, and Clyde Space is able to provide data on operations which have been performed on the system, as detailed in Table 13-1.

	Performed on	Availability	
Functional	Module supplied	Provided with module	
Calibration	Module supplied	Provided with module	
Vacuum	Performed on module prototype	In manual	
Thermal	Performed on module prototype	In manual	
Simulation & modelling	Not performed	Not available	

Table 13-1 Acceptance test data

Following this review, it is recommended the system undergoes further testing for verification against the developer's own requirements. Commonly requirement compliance is presented in a compliance matrix, as shown in Table 13-2.

ID	Requirement	Procedure	Result (X)	Success criteria	Compliance (pass / fail)
SYS-0030	The system mass shall be no more than 1 kg	TEST-01	0.957 kg	X < 1 kg	PASS
SYS-0040	The error LED remains off at initialisation	TEST-02	LED flashing	LED off	FAIL
SYS-0050	…	…	…	…	…

Table 13-2 Compliance matrix example

All procedural plans carried out on the EPS should conform to the test setups and procedures covered in Section 12.

During testing it is recommended that a buddy system is employed where one individual acts as the quality assurance manager and one or more perform the actions, working from a documented and reviewed test procedure. The operator(s) should clearly announce each action and wait for confirmation from their QA. This simple practice provides a useful first check and helps to eliminate common errors or mistakes which could catastrophically damage the subsystem.

Verification is project dependant, but should typically start with lower-level subsystem-specific requirements which can be verified before subsystems are integrated; in particular attention should be paid to the subsystem interfaces to ensure cross-compatibility. Verification should work upwards towards confirming top-level requirements as the system integration continues. This could be achieved by selecting a base subsystem (such as the EPS, OBC or payload) and progressively integrating modules into a stack before structural integration. Dependent upon the specific systems and qualification requirements further system-level tests can be undertaken.

When a subsystem or system is not being operated upon it should be stowed in a suitable container, as per Section 5.

14. Compatible Systems

	Compatibility	Notes
Stacking Connector	CubeSat Kit Bus	CubeSat Kit definition pin compatible
	Non-standard Wire Connector	User defined
	Other Connectors	Please contact Clyde Space
Batteries	Lithium Polymer 8.2v	(2s1p) to (2s2p)[(1)] More strings can be connected in parallel to increase capacity if required
	Lithium Ion 8.2v	(2s1p) to (2s2p)[(1)] More strings can be connected in parallel to increase capacity if required
	Other Batteries	Please contact Clyde Space
Solar Arrays	Clyde Space 3W solar array	Connects to BCR 1-3 via SA1-3
	3W triple junction cell arrays	2 in series connection
	Other array technologies	Any that conform to the input ratings for Voltage and Current[(2)]
Structure	Pumpkin	CubeSat 1U structure
	ISIS	CubeSat 1U compatible
	Other structures	Please contact Clyde Space

Table 14-1 Compatibilities

(1) Refers to series and parallel connections of the battery cells within the battery system. e.g. 2s1p indicates a single string of two cells in series.

(2) Will require some alteration to MPPT. Please contact Clyde Space.