



LCD Television Service Manual

Chassis: MTK8222

Ver 1.2

Hisense Electric Co., Ltd.

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Contents

Contents	- 2 -
Service Manual	- 3 -
1. Precautions and notices.....	- 3 -
1.1 Warning.....	- 4 -
1.2 Notes.....	- 7 -
2. Factory/Service OSD Menu and Adjustment.....	- 10 -
2.1 To enter the Factory OSD Menu.....	- 10 -
2.2 Factory OSD Menu.....	- 10 -
3 Software Upgrading.....	- 14 -
3.1 Before upgrading, read the following.....	- 14 -
3.2 Get ready for upgrading.....	- 14 -
3.3 Upgrading with the MtkTool	- 16 -
3.4 Update with USB directly.....	- 21 -
4. Circuit instruction	- 23 -
4.1 Power assign and block diagram	- 23 -
4.2 Image and signal process	- 25 -
4.3 The main IC description	- 29 -
4.4 Troubleshooting	- 54 -
4.4.1 Troubleshooting for Remote Control	- 54 -
4.4.2 Troubleshooting for Function Key	- 55 -
4.4.3 TV won't Power On.....	- 56 -
4.4.4 Troubleshooting for Audio.....	- 57 -
4.4.5 Troubleshooting for TV/VGA/HDMI input.....	- 58 -
4.4.6 Troubleshooting for YPbPr input.....	- 59 -
4.4.7 Troubleshooting for Video/S-Video input.....	- 60 -
5. Explode View.....	- 61 -
6. Schematic circuit diagram	- 61 -

Service Manual

1. Precautions and notices

BEFORE SERVICING THE LCD TV, READ THE SAFETY PRECAUTIONS IN THIS MANUAL.

WHEN REPLACEMENT PARTS ARE REQUIRED, BE SURE TO USE REPLACEMENT PARTS SPECIFIED BY THE MANUFACTURER.

Proper service and repair is important to the safe, reliable operation of all Hisense Electric Co., Ltd Equipment. The service procedures recommended by Hisense and described in this Service Guide are effective methods of performing service operations. Some of these service operations require the use of tools specially designed for the purpose. The special tools should be used when and as recommended.

It is important to note that this manual contains various CAUTIONS and NOTICES which should be carefully read in order to minimize the risk of personal injury to service personnel. The possibility exists that improper service methods may damage the equipment. It is also important to understand that these CAUTIONS and NOTICES ARE NOT EXHAUSTIVE. Hisense could not possibly know, evaluate and advise the service trade of all conceivable ways in which service might be done or of the possible hazardous consequences of each way. Consequently, Hisense has not undertaken any such broad evaluation. Accordingly, a serviceman that uses a service procedure or tools,

which are not recommended by Hisense, must first satisfy himself thoroughly that neither his safety nor the safe of the equipment will be jeopardized by the service method selected.

Hereafter throughout this manual, Hisense Electric Co., Ltd will be referred to as Hisense.

1.1 Warning

1.1.1

Critical components having special safety characteristics are identified with a **▲** by the Ref. No. in the parts list. Use of substitute replacement parts, which do not have the same specified safety characteristics, may create shock, fire, or other hazards.

Under no circumstances should the original design be modified or altered without written permission from Hisense. Hisense assumes no liability, express or implied, arising out of any unauthorized modification of design. Serviceman assumes all liability.

DANGER CAUTION

TO ENSURE THE CONTINUED RELIABILITY OF THIS PRODUCT, USE ONLY ORIGINAL MANUFACTURER'S REPLACEMENT PARTS, WHICH ARE LISTED WITH THEIR PART NUMBERS IN THE PARTS LIST SECTION OF THIS SERVICE GUIDE.

1.1.2.

All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD).

Careless handling during repair can reduce life drastically. When repairing, make sure

that you are connected with the same potential as the mass of the set by a wristband with resistance. Keep components and tools also at this same potential.

1. Never replace modules or other components while the unit is switched on.

2. When making settings, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

1.1.3

To prevent electrical shock, do not use this polarized ac plug with an extension cord, receptacle, or the outlet unless the blades can be fully inserted to prevent blade exposure.

To prevent electrical shock, match wide blade or plug to wide slot, fully insert.

1.1.4

When replacement parts are required, be sure to use replacement parts specified by the manufacturer or have the same characteristics as the original part. Unauthorized substitutions may result in fire, electric shock, or other hazards.

1.1.5

Safety regulations require that after a repair the set must be returned in its original condition. In particular attention should be paid to the following points.

- Note: The wire trees should be routed correctly and fixed with the mounted cable clamps.

- The insulation of the mains lead should be checked for external damage.

1.1.6

- (1) Do not touch Signal and Power Connector while this product operates. Do not

touch EMI ground part and Heat Sink of Film Filter.

(2) Do not supply a voltage higher than that specified to this product. This may damage the product and may cause a fire.

(3) Do not use this product in locations where the humidity is extremely high, where it may be splashed with water, or where flammable materials surround it. Do not install or use the product in a location that does not satisfy the specified environmental conditions. This may damage the product and may cause a fire.

(4) If a foreign substance (such as water, metal, or liquid) gets inside the panel module, immediately turn off the power. Continuing to use the product may cause fire or electric shock.

(5) If the product emits smoke, and abnormal smell, or makes an abnormal sound, immediately turn off the power. Continuing to use the product, it may cause fire or electric shock.

(6) Do not disconnect or connect the connector while power to the product is on. It takes some time for the voltage to drop to a sufficiently low level after the power has been turned off. Confirm that the voltage has dropped to a safe level before disconnecting or connecting the connector.

(7) Do not pull out or insert the power cable from/to an outlet with wet hands. It may cause electric shock.

(8) Do not damage or modify the power cable. It may cause fire or electric shock.

(9) If the power cable is damaged, or if the connector is loose, do not use the product:

otherwise, this can lead to fire or electric shock.

(10) If the power connector or the connector of the power cable becomes dirty or dusty, wipe it with a dry cloth. Otherwise, this can lead to fire.

(11) Use only with the cart, stand, tripod, bracket, or table specified by the manufacturer, or sold with the apparatus. When a cart is used, use caution when moving the cart/apparatus combination to avoid injury from tip-over.

1.2 Notes

Notes on Safe Handling of the LCD panel and during service

The work procedures shown with the Note indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.

- Before starting the work, secure a sufficient working space.
- At all times other than when adjusting and checking the product, be sure to turn OFF the POWER Button and disconnect the power cable from the power source of the TV during servicing.
- To prevent electric shock and breakage of PC board, start the servicing work at least 30 seconds after the main power has been turned off. Especially when installing and removing the power board, start servicing at least 2 minutes after the main power has been turned off.
- While the main power is on, do not touch any parts or circuits other than the ones specified. If any connection other than the one specified is made between the measuring

equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.

- When installing the LCD module in, and removing it from the packing carton, be sure to have at least two persons perform the work.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in, the surface of the panel being scratched by foreign matter.
- When handling the circuit board, be sure to remove static electricity from your body before handling the circuit board.
- Be sure to handle the circuit board by holding the large parts as the heat sink or transformer. Failure to observe this precaution may result in the occurrence of an abnormality in the soldered areas.
- Do not stack the circuit boards. Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed. All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring

that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.

- Perform a safety check when servicing is completed. Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original setup.



The lightning flash with arrowhead symbol, within an equilateral triangle is intended to alert the user to the presence of uninsulated dangerous voltage within the products enclosure that may be of sufficient magnitude to constitute a risk of electric shock.



The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the set.

2. Factory/Service OSD Menu and Adjustment

2.1 To enter the Factory OSD Menu

- a. With factory RC (remote control)
1. Press “M” button and enter factory mode.
 2. Press “Menu” button and enter factory OSD menu.
 3. Press “CH+”/“CH-” button select the function menu, press “VOL+”/“VOL-” enter the selected function menu. Press “VOL+”/“VOL-” button adjust values in the menu.
- b. With user’s RC
1. Power TV On
 2. Press Menu button and call up User OSD Menu
 3. Select Audio-> Balance
 4. Enter 0->5->3 ->2 in sequence. If re-do number keys not appear the OSD, then renew enter 1->9->6 ->9 in sequence.
 5. Factory OSD appears.
 6. Press Menu again and leave factory OSD.

2.2 Factory OSD Menu

2.2.1 White Balance

Note: Different source has different WB values. Before adjusting, please change to desired source.

1. Auto Color

For VGA and Component Video sources, WB values must be adjusted. And at others signal sources, the “auto colour “does not work.

Before adjusting, prepare the signal instruments such as DVD or K-8256 first, and find the video picture with gray and color bars. Then please change to desired source.

	source	Timing	Pattern	Notes
1	ADC VGA	1024*768	gray-3color	For VGA source
2	ADC HDTV	720P	gray-3color	For Component Video

Notes:

- a. Press “M” button and enter factory mode.
- b. Press “Menu” button and enter factory OSD menu.
- c. Select the item “Auto Color” .
- d. Press VOL+ button to auto color.
- e. Close the OSD menu after 5 seconds.

LCD TV Service Manual

2.2.2 Factory Option

Item 0	Item 1	Note
White Balance	R DRV	Red Driver adjust
	G DRV	Green Driver adjust
	B DRV	Blue Driver adjust
	R CUT	Red Cut adjust
	G CUT	Green Cut adjust
	B CUT	Blue Cut adjust
Note: Before adjusting, please change to desired source. Different source has different WB values.		
Factory RESET	Zhong Shi	Qingdao Jiangxi Road factory
	Huang Dao	Huangdao Industrial Park
	Gui Yang	Gui Yang Industrial Park
	Liao Ning	Liao Ning Industrial Park
	Hungary	Hisense Hungary
	Australia	Hisense Australia
	France	Hisense France
	Clean Protected	Clean data except WB data and Auto Color data
	Clean All	Clean all data
Auto Color	For VGA and Component Video sources, WB values must be adjusted	And at others signal sources, the "auto colour "does not work.
Color Temp	Color	Standard
	R Offset	
	G Offset	
	B Offset	
Picture Mode	Brightness Min	Min Brightness
	Brightness Mid	Mid Brightness
	Brightness Max	Max Brightness
	Contrast Min	Min Contrast
	Contrast Mid	Mid Contrast
	Contrast Max	Max Contrast s
	Saturation Min	Min Saturation
	Saturation Mid	Mid Saturation
	Saturation Max	Max Saturation
Factory Option	OSD	English
	Logo Option	Devant
	To FAC	M
MODE "M" is only used for factory production.		

LCD TV Service Manual

SW Version	Version:	Current Software version
	Panel Info:	The date of current version
	Flash:	

Note: The factory menu date varies according to different sources. In case changing the factory data by error, you can choose to “Clean Protected”, by which you can resume the default value.

To clear the EEPROM:

- a. Select the item “Clean All” .
- b. Press VOL+ button to clear the EEPROM data.
- c. Close the OSD menu after 5 seconds.
- d. Restart the TV.

2.3 Designer Menu

Item 0	Item 1	Item 2	Note
Designer Menu	Picture Mode	SOURCE	The current program source
		Brightness Brightness	Brightness of VIVID mode
		Brightness Contrast	Contrast of VIVID mode
		Brightness Saturation	Saturation of VIVID mode
		STD Brightness	Brightness of STD mode
		STD Contrast	Contrast of STD mode
		STD Saturation	Saturation of STD mode
		Soft Brightness	Brightness of Movie mode
		Soft Contrast	Contrast of Movie mode
		Soft Saturation	Saturation of Movie mode
	Audio Set	Volume Min	When value is 1 Think about the Audio out power before adjusting
		Volume 25	When value is 25 Think about the Audio out power

LCD TV Service Manual

			before adjusting
		Volume Mid	When value is 50 Think about the Audio out power before adjusting
		Volume 75	When value is 75 Think about the Audio out power before adjusting
		Volume Max	When value is 100 Think about the Audio out power before adjusting
	Audio Mode	Audio Mode	Standard 、 user 、 Music 、 Speech, Music
		120HZ	Different frequencies for different Audio Mode
		500HZ	
		1.5kHz	
		5kHz	
		10kHz	
	Backlight co	PVM 0-350	
		PVM 350-500	
		PVM500-1000	
		PVM 1000-10000	
		PVM 10000-	
	EMI	0	
	Power Mode	Last station	

The above “Factory/Service OSD Menu” are reference only, please refer to the actual units to determine the appearances.

3 Software Upgrading

3.1 Before upgrading, read the following.

- 1、 Before upgrading, Write down the ADC Calibration values of the sources of VGA and component.
- 2、 Upgrade the software.
- 3、 To clear the EEPROM .
 - A Select the item “Clear Unprotected”.
 - B Press VOL+ button to clear the EEPROM data.
 - C Close the OSD menu after 5 seconds.
 - D Restart the TV.
- 4 Write the ADC Calibration values copied just now into the the channels of VGA and component.
- 5、 After the operation above all, necessarily, Renew search the channels for the users.

The first upgrading method:

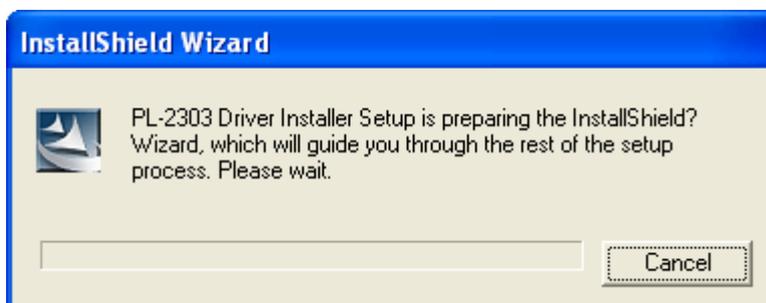
The software is upgraded by a burning toll-MtkTool, which can burn the program file *.bin to the main board of the unit.

3.2 Get ready for upgrading

3.2.1 Install the driver



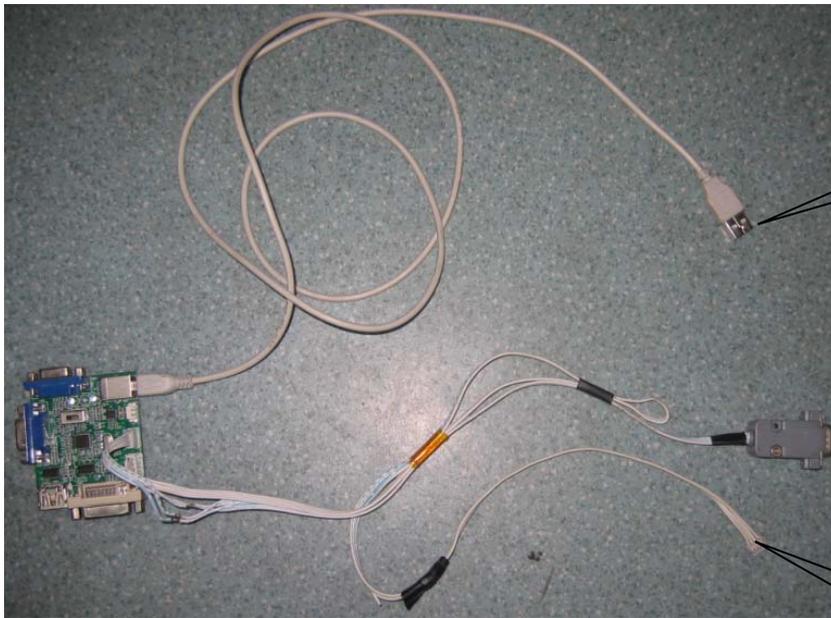
Double click the icon MTKtools2.44.04+cp210xDriver.rar , install the driver.



Select the default value, the driver will be installed step by step.

3.2.2 Hardware connecting

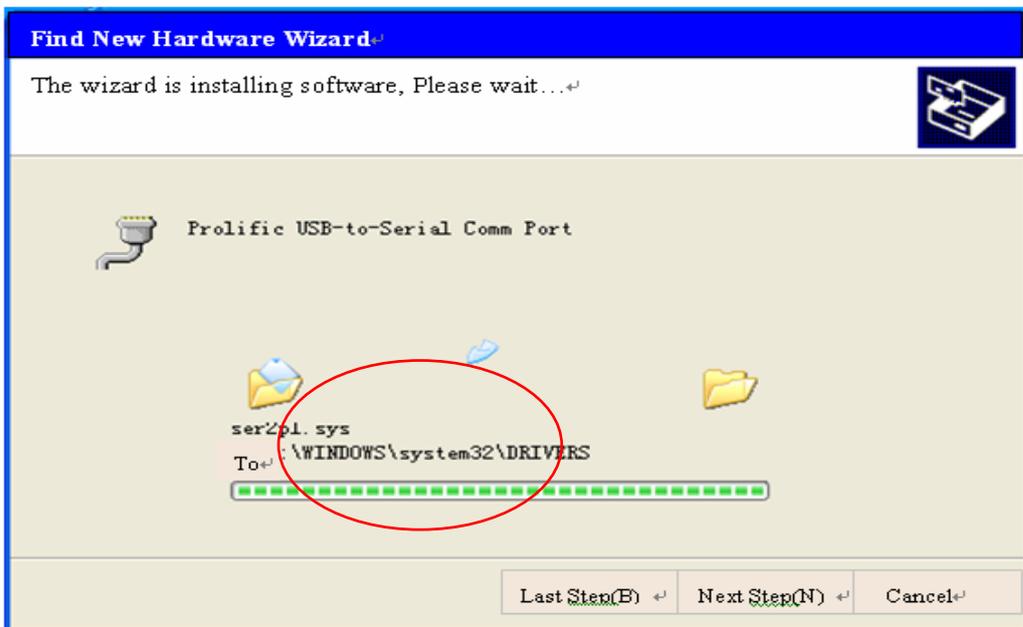
Connect the unit to your pc with a USB-to-serial port cable. USB port connects to your pc, and serial port to the TV's RS232 port.

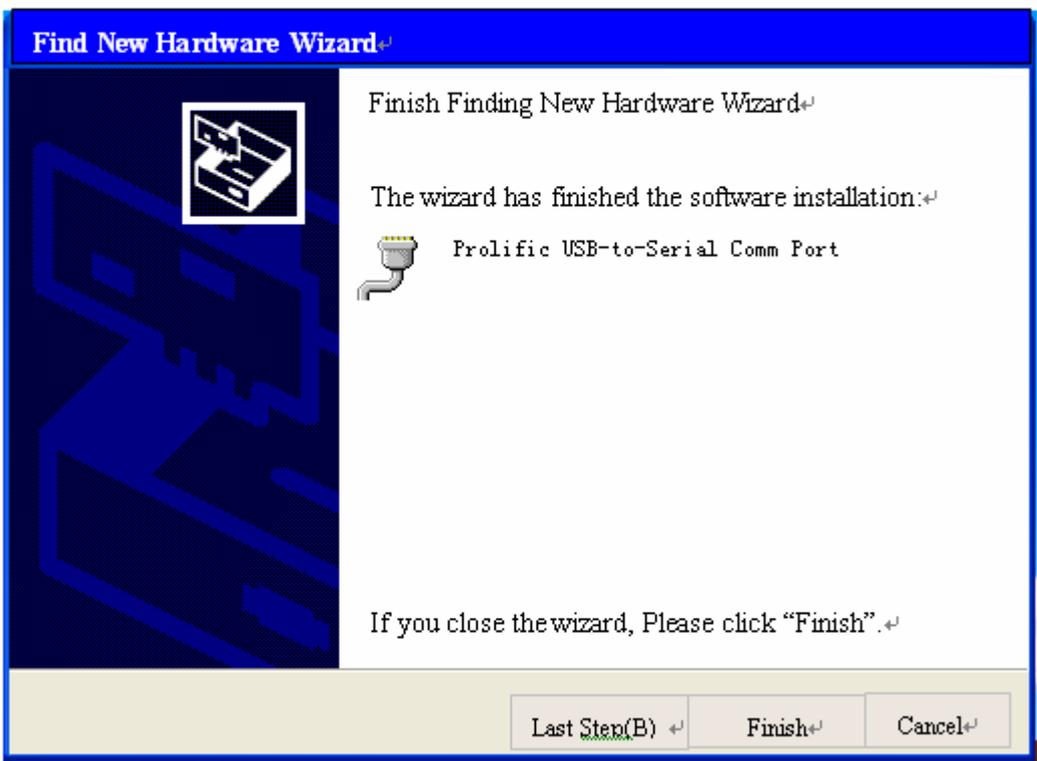


USB connector: to PC.

Serial connector: to TV's RS232 port.

For the first connecting, the pc will recognize and automatically install the USB device. The process is just like the installation of a mini disk, see the following picture.





3.3 Upgrading with the MtkTool

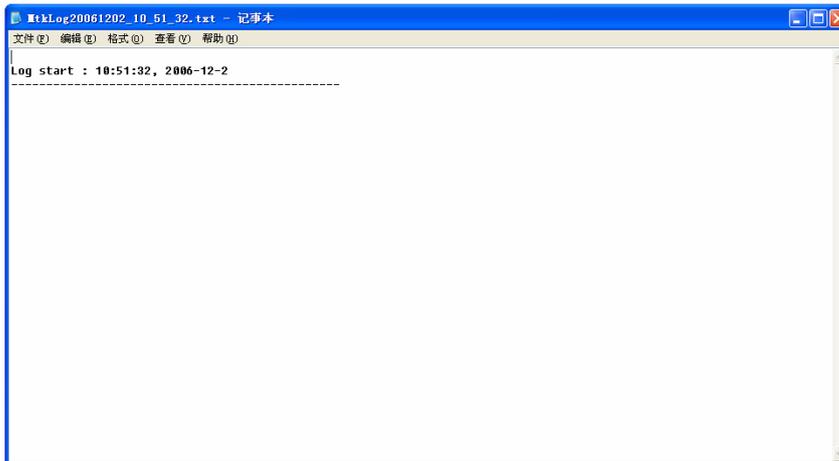
MTKtool is a green program needing no installation. It is saved in the folder



. There are five folders/files in this folder altogether.



The MtkTool using log is restored in the MtkLog folder. It records the running time and date whenever the tool is used. The log will be a txt file named by the date and time.



MtkTool.exe

After connecting the TV with your PC, double click  icon, open the MtkTool.

If following error appears, it means the related port is not be set properly.



Ignore these errors, click “Confirm” and enter the MtkTool main interface, see the following picture.

Flash chip model

Please refer to follow steps to update the software:

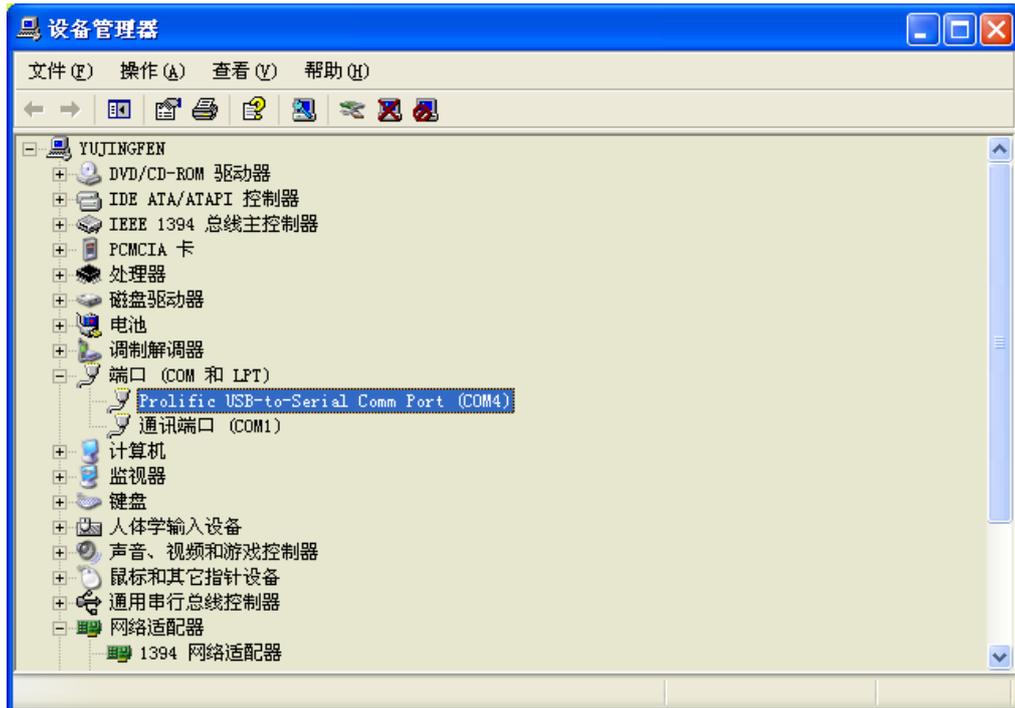
- 1—Select mode of Flash chip to MT8226 as the below picture.
- 2—Refer to the next page instruction to select the communicate port.
- 3—Press the icon beside the baud rate and make sure it is green as the below picture.
- 4—Set the flash baud rate to 115200 as the below picture.
- 5—Click the browse button to select the *.bin file that will be updated.
- 6—Click the “start” button to update software.

LCD TV Service Manual

The screenshot shows the MtkTool - [Flash Upgrade] window. The interface includes a menu bar (Port, Baud rate, Window, Operation, Tool, Help), a toolbar with icons for refresh, lightning bolt, file, folder, and VGA, and a main control area. The main area contains fields for 'Load Bin file' (D:\Pub\Dev\MTK_8226\src\8280_011) and 'Backup file' (backup), with 'Browse' buttons. It also features 'Upgrade' and 'Backup' buttons. A 'USB Config' section has radio buttons for RS-232, Usb --> M, Usb --> Dram, Usb --> Flash, and RS232->MT. Below this are checkboxes for 'Verify', 'BlankCheck', 'High Speed', 'USB to UART Bridge Controller', and 'ShakeHand'. There are also input fields for 'Custom Burning Address' (0) and 'Custom Burning End' (800000) in HEX, and a 'Direct Control' checkbox. A 'Clear MSG' button and the MTK logo are at the bottom.

Callouts and annotations:

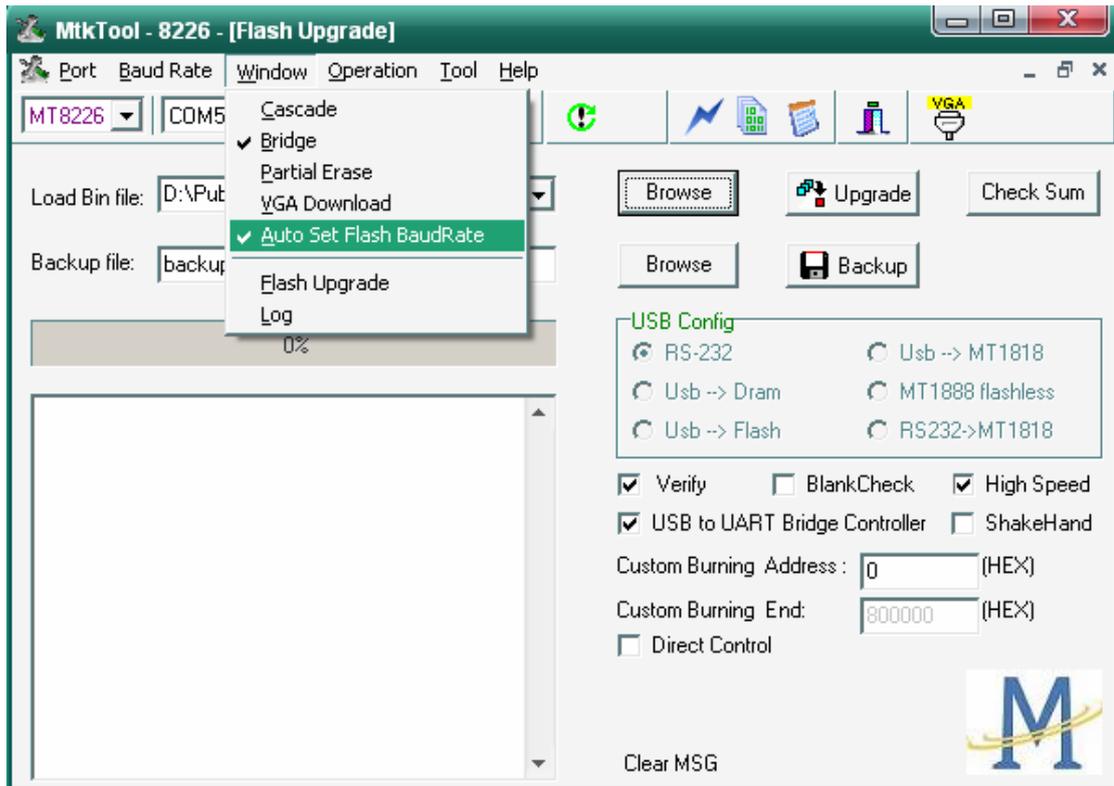
- Select mode of Flash chip**: Points to the 'MT8226' dropdown menu.
- Communicate port**: Points to the 'COM1' dropdown menu.
- Set Flash Baud Rate**: Points to the '175200' dropdown menu.
- Select *.bin file**: Points to the 'Load Bin file' field.
- Choose the current USB conversion Port Later choose com5**: A green callout pointing to the 'USB Config' section.
- Start upgrade**: Points to the 'Upgrade' button.
- Information of upgrade process**: Points to the main area of the software window.



Open “Device Manager” and find which port is connected with the TV. In this operation, COM5 is connected to the TV; so, select “COM5” in the MtkTool main interface. Select the right baud rate according to chip model. For this unit(chip model is MT8226), select 115200..So choose “Auto Set Flash BaudRate”

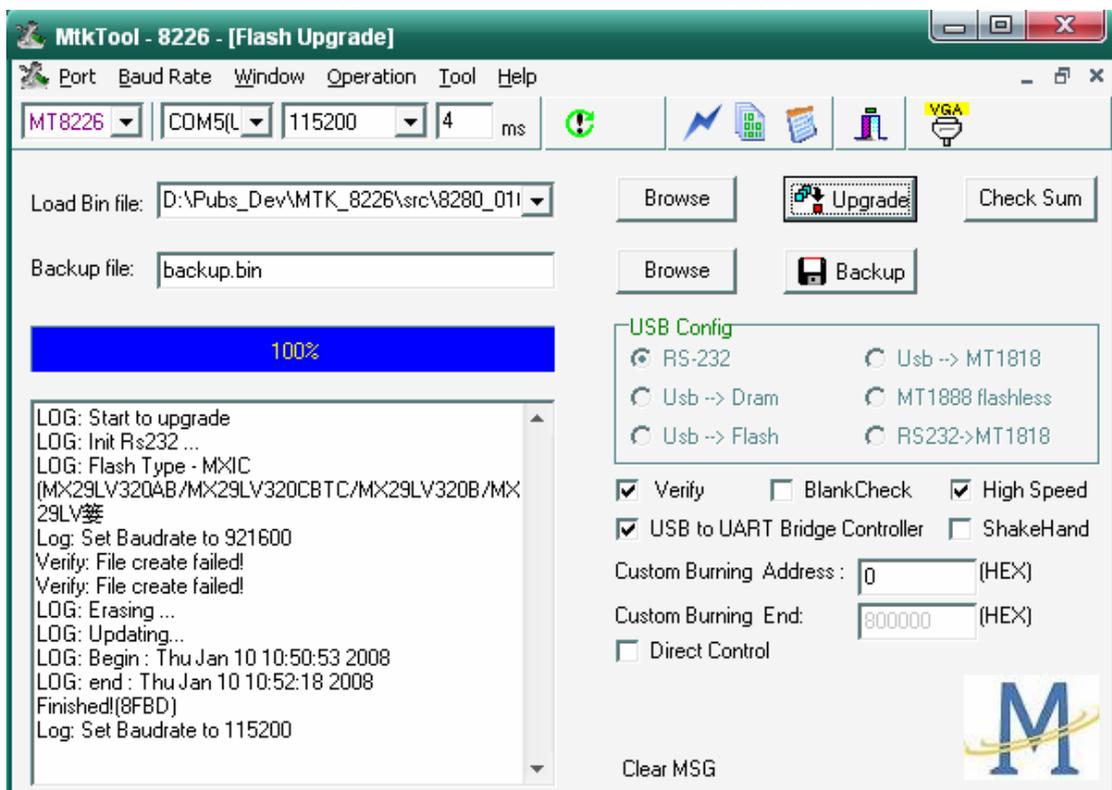
Note: Whether or not click the “Auto Set Flash Baud Rate” in the “window” menu depends on the chip type. If the flash chip does not support high speed transport, do not select this option; otherwise, reserve the selected mood.

LCD TV Service Manual



Click “Browse” button, find the upgrading program file, and select it. Press “Upgrade” button and start upgrading.

The following interface appears on the screen, indicating upgrading successfully.



3.4 Update with USB directly

The second update method is with USB directly:

MTK8222 Series can update with USB, the software name should be **HISENSE.bin**.

The Updating Steps is set the Source to "DMP interface", insert the USB(the update file **HISENSE.bin**,which should be in root directory),The TV automatic identify the upgrading software. step by step according as the informations of the upgrading process.



(USB to the Main board directly)



After upgrading, you must confirm the software in the “Factory Menu ” and you'd better "CLEAR UNPROTECTLY".

4. Circuit instruction

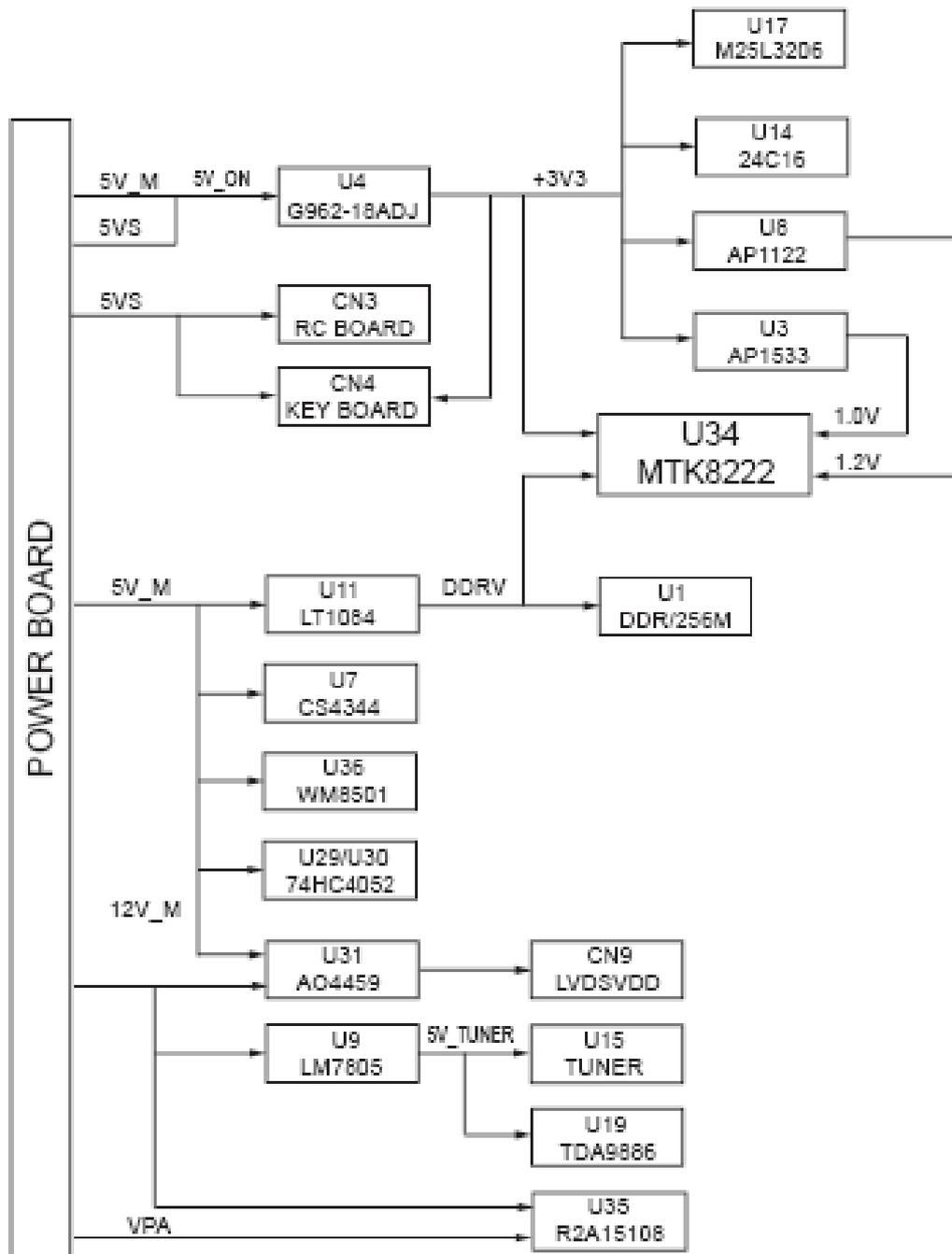
4.1 Power assign and block diagram

Power assign:

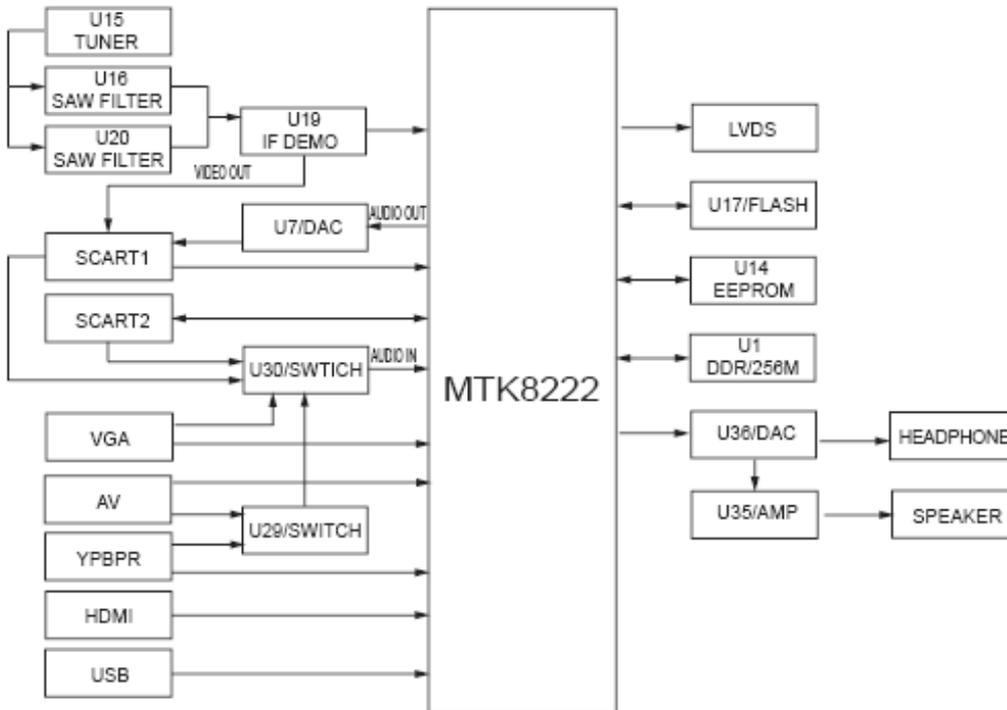
Power voltage includes 12V_M、5V_M、5VS and VPA(Voltage Power for Audio, normally 14~16V), some small size TV's(small than 37 inch) VPA will use 12V_M directly .All other voltages are converted from the above voltages.

- a. 5V_TUNER that power supply for Tuner is converted by U9 from 12_M; The power supply for panel is converted by chosen output between U31 from 12_M and 5V_M ; The power supply for the audio IC (U35) of small size TVs is converted by the output of 12V_M connects ferrite bead and VPA; the last, the 33V rising circuit and mute circuit are converted by the 12_M directly.
- b. Both of the 5VM and 5VS pass through diodes then output 5V_ON, which used for 3.3V/1.2V/DV10 conversion. U36 (DAC)、U29/U30 (audio switch)、U7 (DAC)、U19 (IF) and USB are converted from 5V_M directly ; The power supply for DDR(U1,2.6V) is converted by U11 from 5V_M too
- c. 3.3V supply for U17(FLASH), U14(EEPROM)is converted by U4 from 5V_ON . 1.0V supply for U34(the main IC \MT8222)is converted by U3 from the 3.3V ; 1.2V power supply for the main IC \MT8222. is converted by the 3.3V

Block diagram:



4.2 Image and signal process



RF signal:

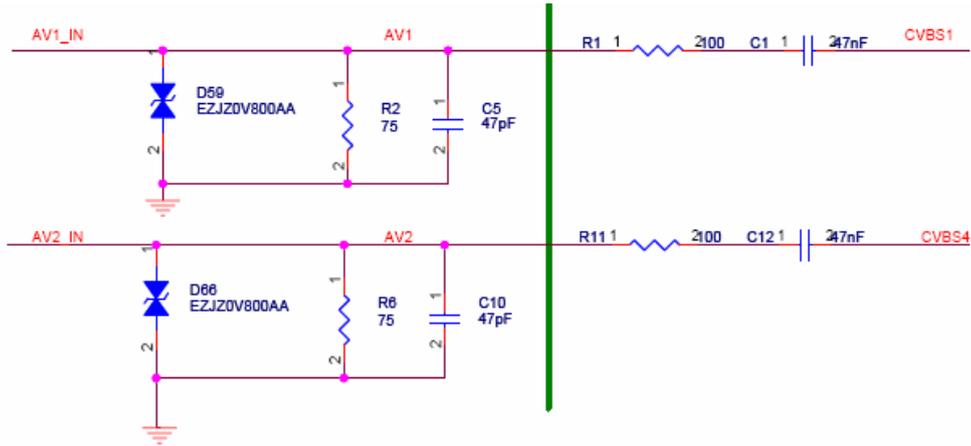
After the RF Signal enter TV Tuner, the RF Signal will become IF Signal after the TV Tuner converted, and then the Signal will become SIF and VIF signal by sawfilter U16 and U20, finally send to Main IC through U19.

Video signal:

Video of AV1 input through P16B, pass by R2, C5, R1, C1, enter No.1 feet of U34

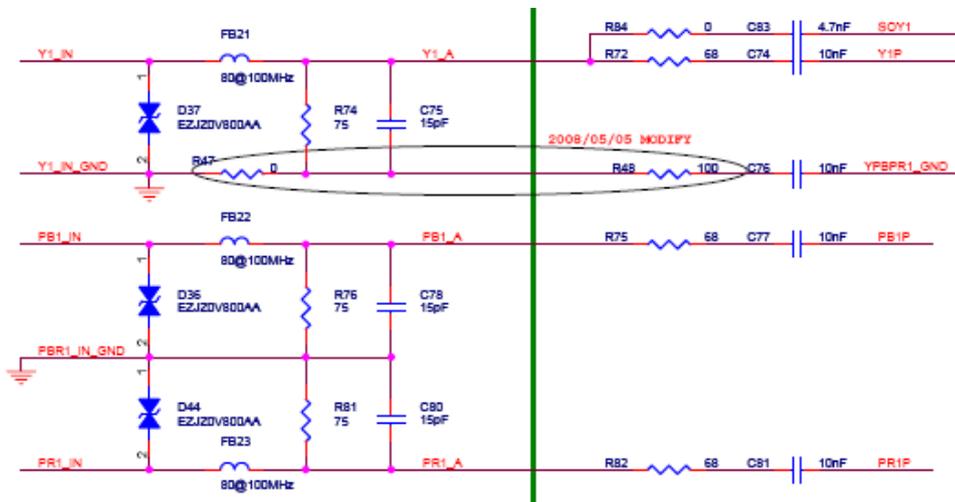
Video of AV2 input through P16A, pass by R6, C10, R11, C12, enter No.4 feet of U34

LCD TV Service Manual



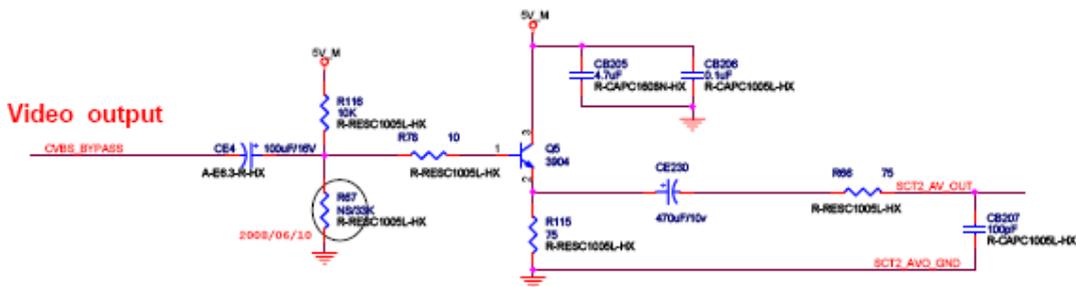
Input by P9, pass the below circuit diagram and enter U34 for disposal.

PC signal enter through XS11, input U34 by passing the below similar disposal, check the diagram for detail.



The Audio signal of HDMI and USB directly input U34 for disposal.

AV output send out by the No.11 feet of U34, through the below diagram, finally come out by P4.

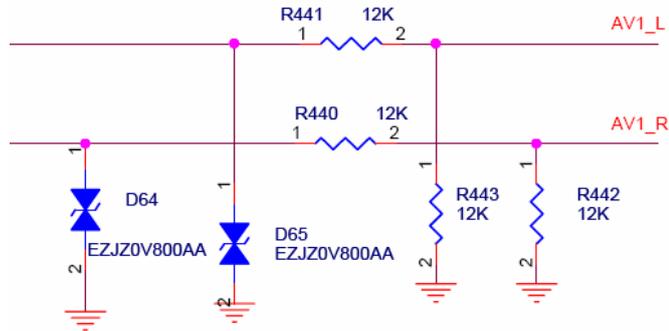


The input Video signal send out the LVDS signal after the U34 managed, the LVDS signal will pass CN9 and go to LCD panel display.

Audio signal

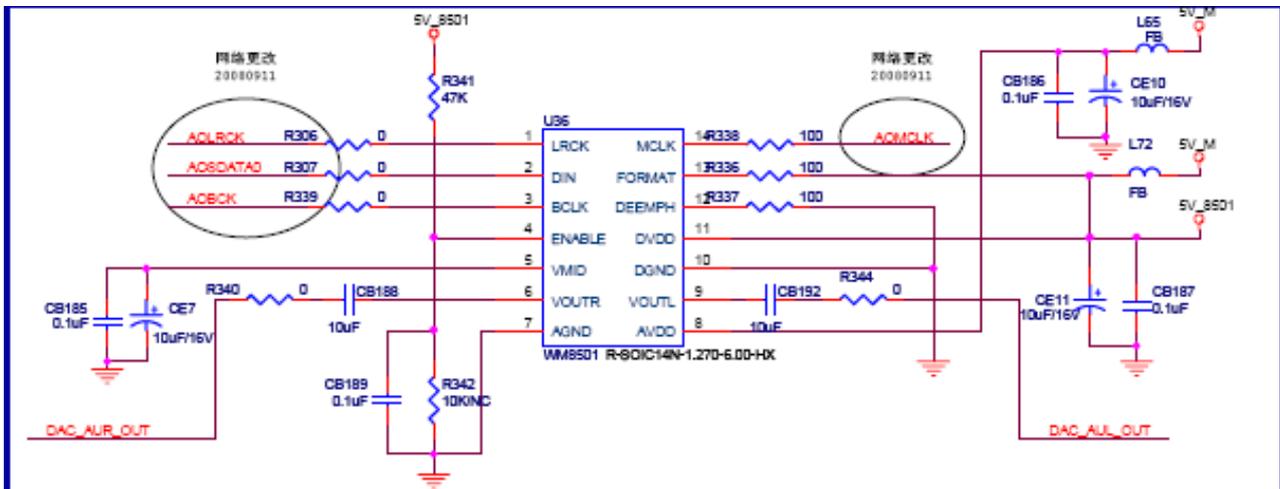
TV Audio signal is get by SIF signal which is come out through TV Tuner, after the U19 managed, and then directly go out to U34.

The Audio of AV1, AV2 and YPbPr input by P16B, P16A and P9, firstly pass the below diagram to reduce it.



And then pass U29 to do the shift and choose one, then together with PC and SCART Audio to do the conversion through U30, choose one input U34 for disposal.

Digital audio signal output by feet 47-50 after the disposal of U34, transfer digital to analogue from the U36, change to analogue Signal. One pass the driving diagram to earphone, the other one pass the sound IC to speaker.



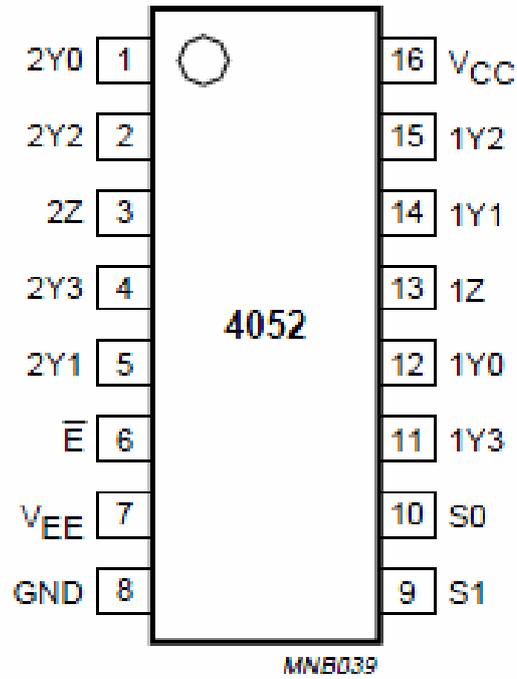
LCD TV Service Manual

The main control signal, as list:

Control Signal	Internet mark	Instruction	Remark
Standby signal	UP31	Low level power on	
		High level power on	UP31pass Q29 inverse phase
Power control	SW	High level power on	
	----	Low level power on	
BL-control	UP34	Low level BL on	
	BL-ON/OFF	Low level BL on	UP34 passQ2 inverse phase
BL-brightness	PWM0	Adjust duty ratio	
	BL-ADJUST		PWM0passQ18 inverse phase
E2prom written protect	PWM2		
Flash written protect	FRESET#	High voltage for protect	
Key “0”	ADIN0		key
Key “1”	ADIN1		key
IR signal	IR-IN		
Tuner 33V	PWM1	Adjust duty ratio	
	TU_33V		PWM1 rise voltage
Audio amplify mute	GPIO_21	Low-level mute	

4.3 The main IC description

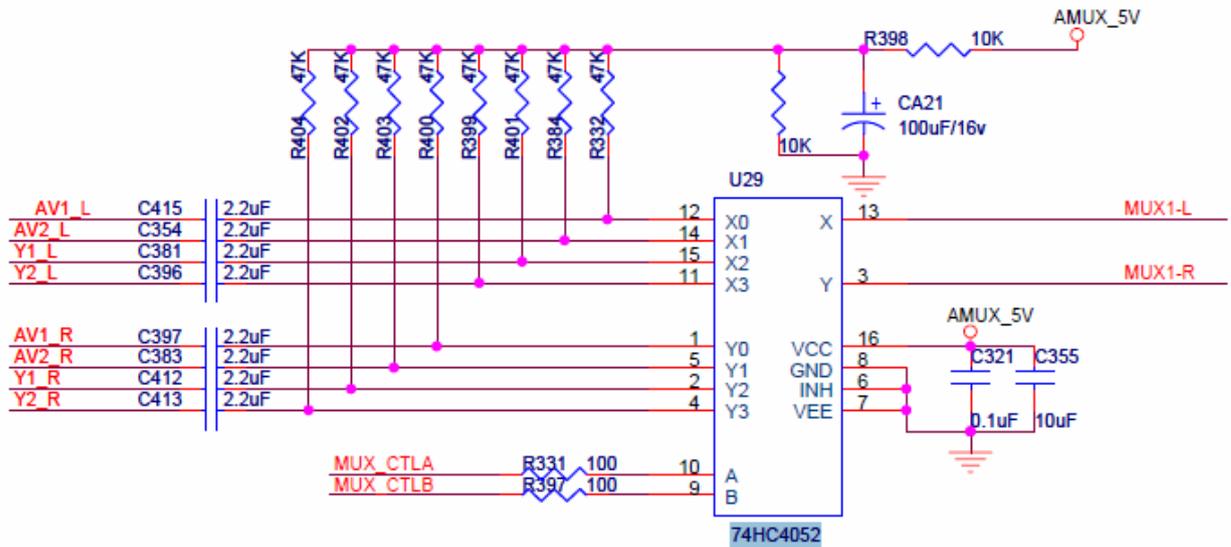
74HC4052D:



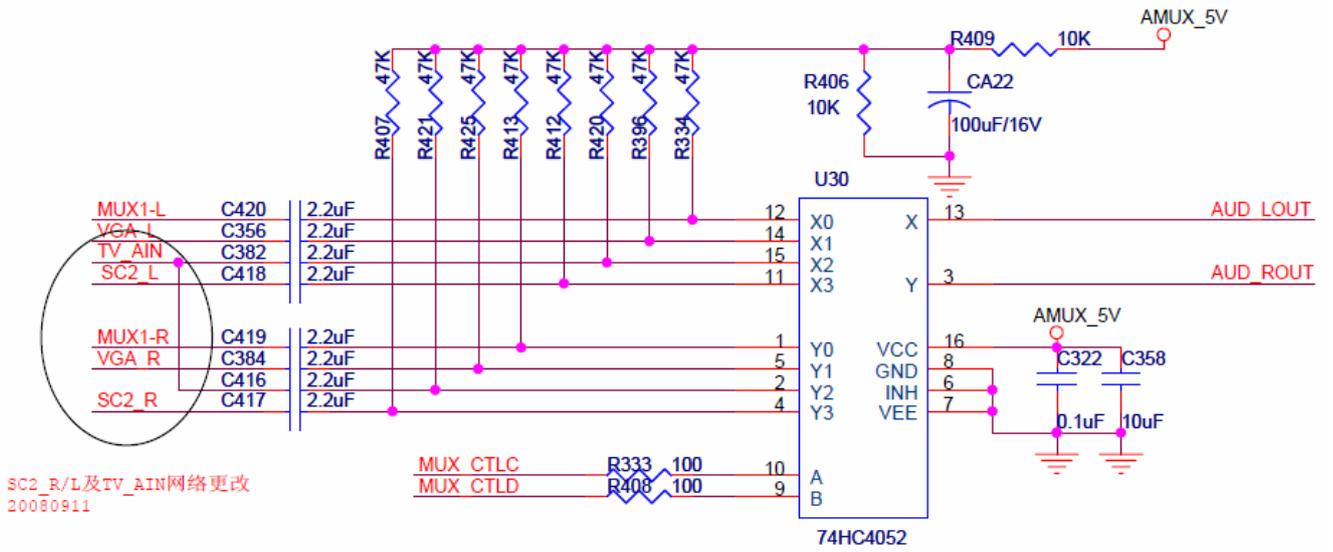
LCD TV Service Manual

PINNING

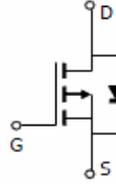
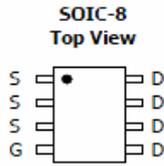
PIN	SYMBOL	DESCRIPTION
1	2Y0	independent input or output
2	2Y2	independent input or output
3	2Z	common input or output
4	2Y3	independent input or output
5	2Y1	independent input or output
6	\bar{E}	enable input (active LOW)
7	V _{EE}	negative supply voltage
8	GND	ground (0 V)
9	S1	select logic input
10	S0	select logic input
11	1Y3	independent input or output
12	1Y0	independent input or output
13	1Z	common input or output
14	1Y1	independent input or output
15	1Y2	independent input or output
16	V _{CC}	positive supply voltage



LCD TV Service Manual



AO4459:



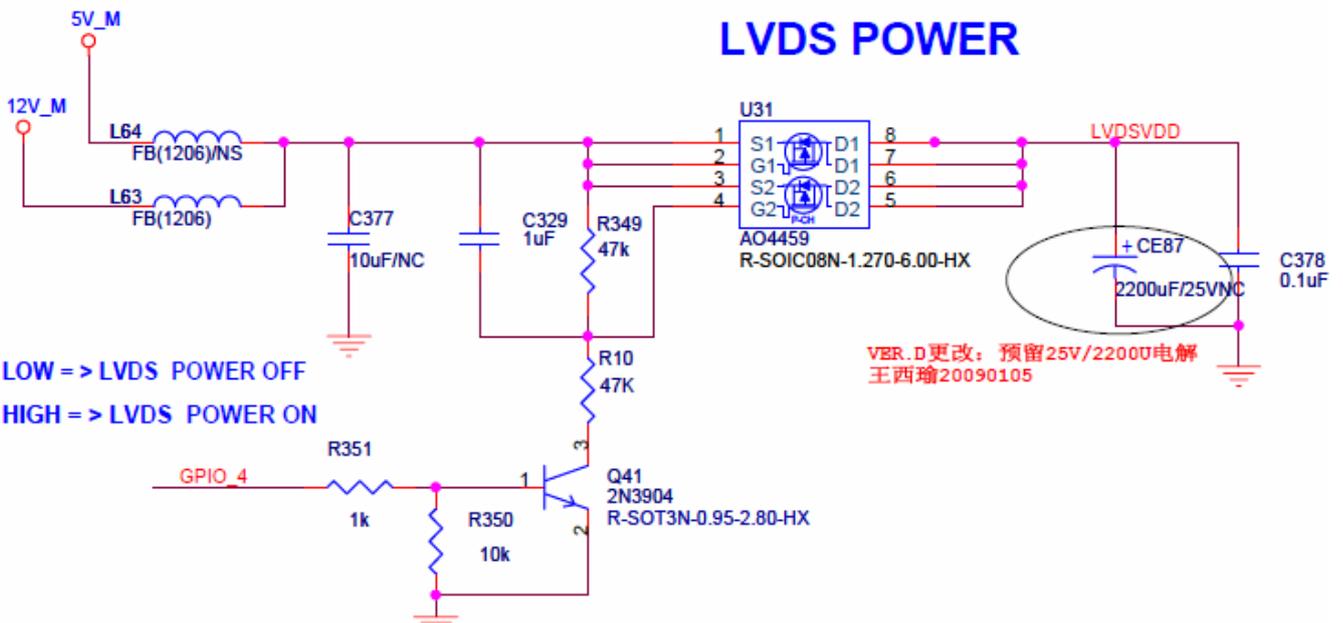
Absolute Maximum Ratings $T_A=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	$T_A=25^{\circ}\text{C}$	-6.5	A
	$T_A=70^{\circ}\text{C}$	-5.3	
Pulsed Drain Current ^B	I_{DM}	-30	
Power Dissipation ^A	$T_A=25^{\circ}\text{C}$	3.1	W
	$T_A=70^{\circ}\text{C}$	2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$

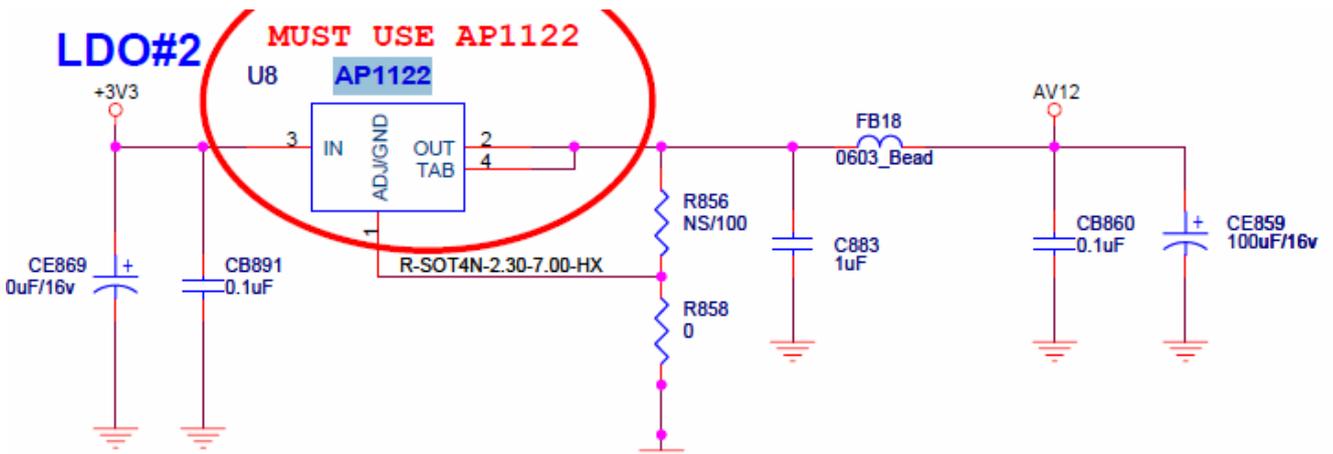
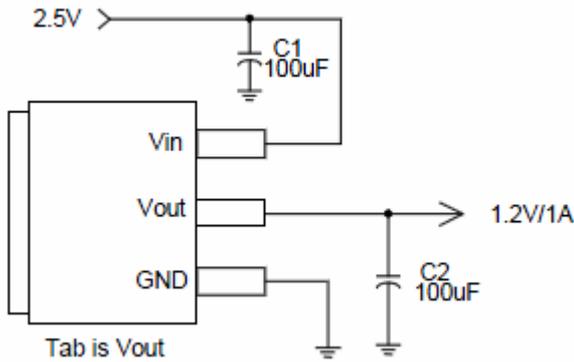
Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$	33	$^{\circ}\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	62	
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	18	24	$^{\circ}\text{C/W}$

LVDS POWER

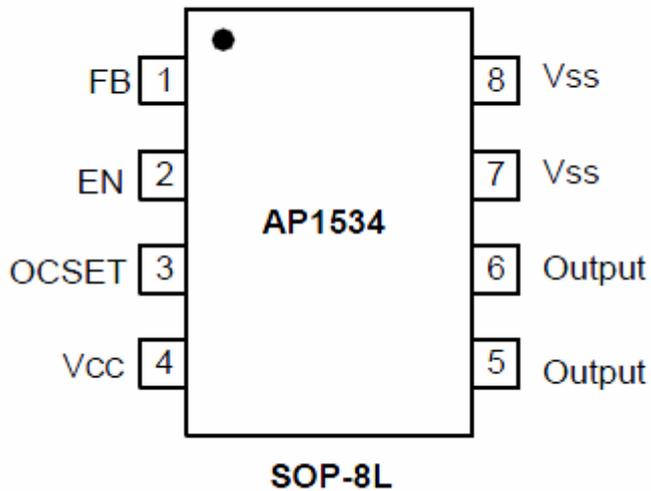


AP1122EA:



AP1534

- Input voltage: 4.4V to 18V
- Output voltage: 0.8V to V_{CC} .
- Duty ratio: 0% to 99% PWM control
- Oscillation frequency: 300KHz typ.
- Current limit, Enable function
- Thermal Shutdown function
- Built-in internal SW P-channel MOS
- SOP-8L: Available in "Green" Molding Compound (no Br, Sb)
- Lead Free Finish/RoHS Compliant (Note 1)



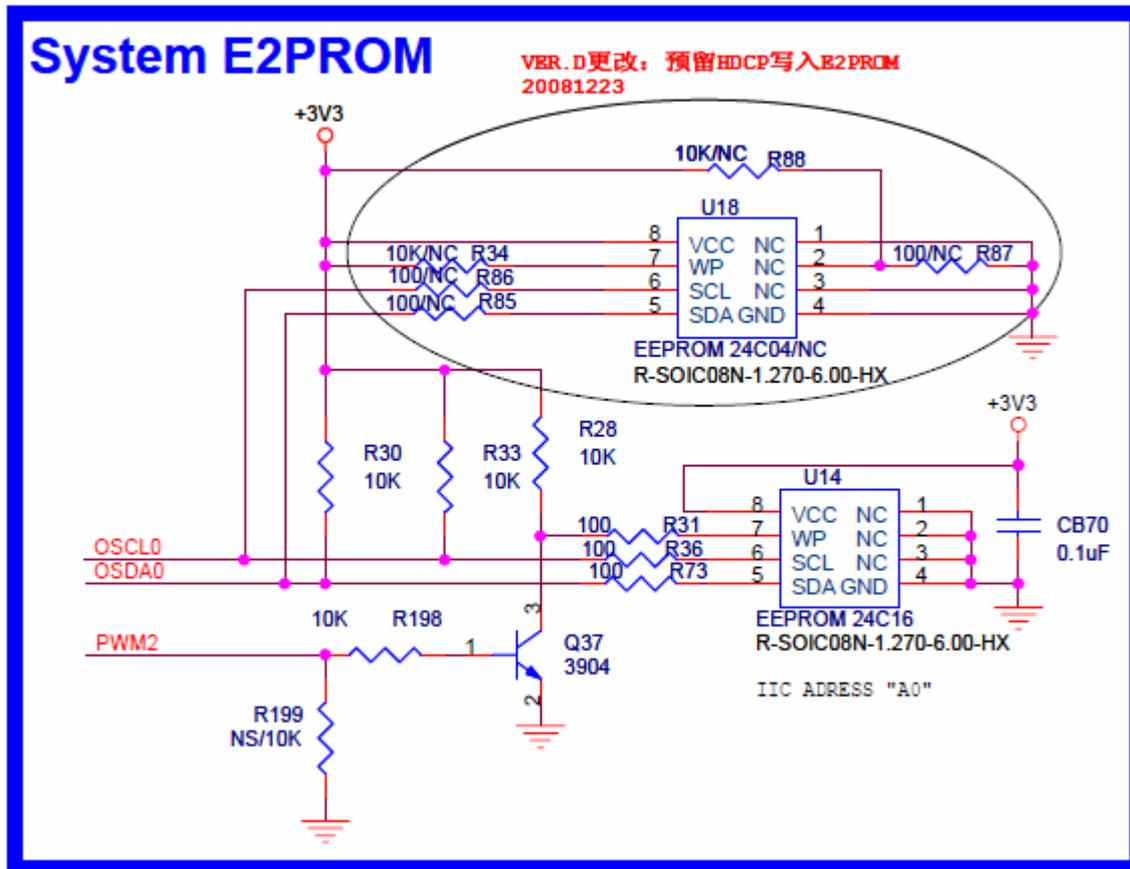
Pin Descriptions

Pin Name	Pin No.	Description
FB	1	Feedback pin
EN	2	Power-off pin H: Normal operation (Step-down operation) L: Step-down operation stopped (All circuits deactivated)
OCSET	3	Add an external resistor to set max output current
V _{CC}	4	IC power supply pin
Output	5, 6	Switch Pin. Connect external inductor/diode here. Minimize trace area at this pin to reduce EMI
V _{SS}	7, 8	GND Pin

AT24C08AN-10SU-2.7:

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect
GND	Ground
VCC	Power Supply

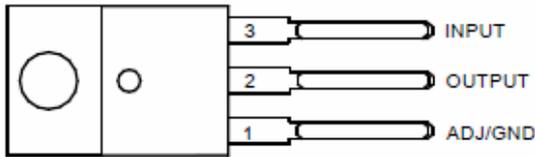
- Memory Organization** **AT24C01A, 1K SERIAL EEPROM:** Internally organized with 16 pages of 8 bytes each, the 1K requires a 7-bit data word address for random word addressing.
- AT24C02, 2K SERIAL EEPROM:** Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.
- AT24C04, 4K SERIAL EEPROM:** Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.
- AT24C08A, 8K SERIAL EEPROM:** Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.
- AT24C16A, 16K SERIAL EEPROM:** Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.



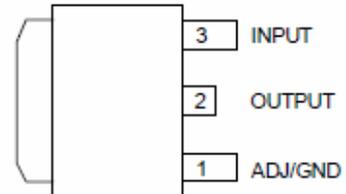
AZ1084:

Pin Configuration

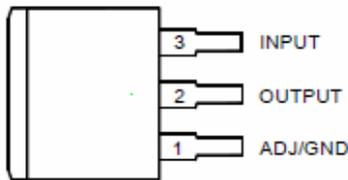
T Package
(TO-220-3)



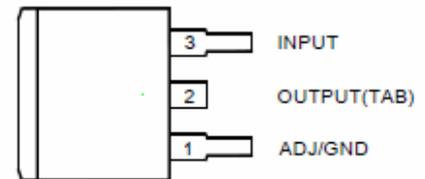
D Package
(TO-252-2(1))



S Package
(TO-263-3/TO-263-3 (u))



S2 Package
(TO-263-2)



5A LOW DROPOUT LINEAR REGULATOR

AZ1084

General Description

The AZ1084 is a series of low dropout positive voltage regulators with a maximum dropout of 1.5V at 5A of load current.

The series features on-chip thermal limiting which provides protection against any combination of overload and ambient temperatures that would create excessive junction temperatures. It also includes a trimmed band-gap reference and a current limiting circuit.

The AZ1084 is available in 1.5V, 1.8V, 2.5V, 3.3V and 5.0V versions. The fixed versions integrate the adjust resistors. It is also available in an adjustable version which can set the output voltage with two external resistors.

The AZ1084 series is available in standard packages of TO-263-2, TO-263-3, TO-220-3 and TO-252-2 (1).

Features

- Low Dropout Voltage: 1.3V Typical at 5A
- Current Limiting and Thermal Protection
- Output Current: 5A
- Current Limit: 6.5A
- Operating Junction Temperature Range: 0 to 125°C
- Line Regulation (Adj Version): 0.015% (Typical)
- Load Regulation (Adj Version): 0.1% (Typical)

Applications

- High Efficiency Linear Regulators
- Battery Chargers
- Post Regulation for Switching Supply
- Microprocessor Supply
- Desktop PCs, RISC and Embedded Processors' Supply

cs4344czz:

10-Pin, 24-Bit, 192 kHz Stereo D/A Converter

Features

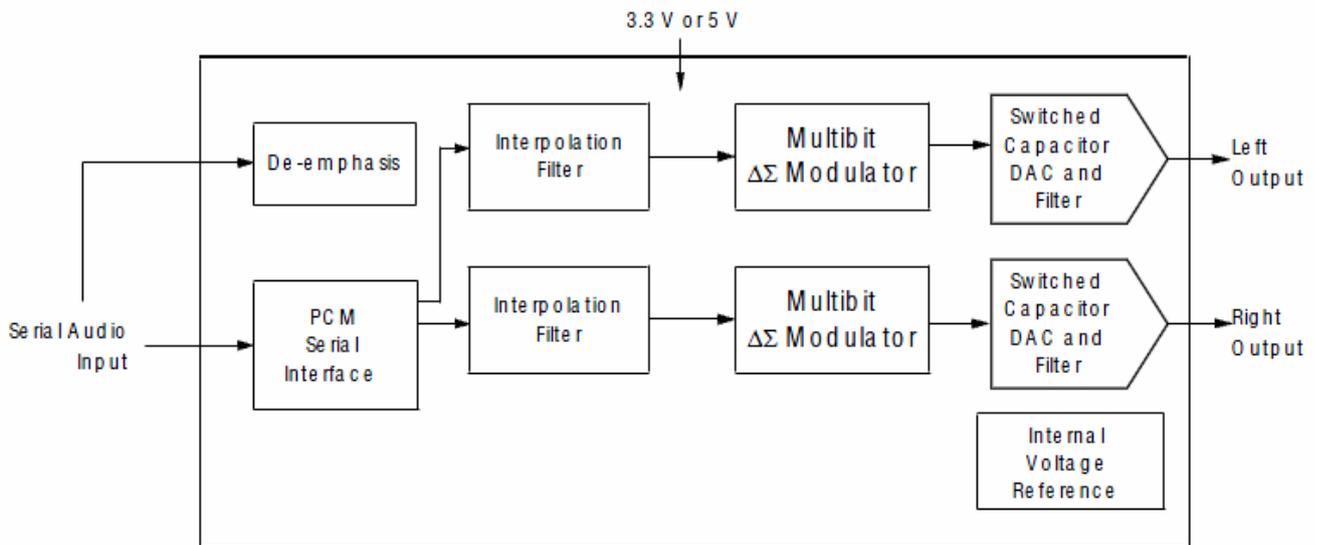
- ❑ Multi-bit Delta-Sigma Modulator
- ❑ 24-Bit Conversion
- ❑ Automatically Detects Sample Rates up to 192 kHz
- ❑ 105 dB Dynamic Range
- ❑ -95 dB THD+N
- ❑ Low Clock Jitter Sensitivity
- ❑ Single +3.3 V or +5 V Power Supply
- ❑ Filtered Line Level Outputs
- ❑ On-Chip Digital De-emphasis
- ❑ Popguard™ Technology
- ❑ Small 10-Pin TSSOP Package

Description

The CS4344 family members are complete, stereo digital-to-analog output systems including interpolation, multi-bit D/A conversion and output analog filtering in a 10-pin package. The CS4344/5/6/8 support all major audio data interface formats, and the individual devices differ only in the supported interface format.

The CS4344 family is based on a fourth order multi-bit delta-sigma modulator with a linear analog low-pass filter. This family also includes auto-speed mode detection using both sample rate and master clock ratio as a method of auto-selecting sampling rates between 2 kHz and 200 kHz.

The CS4344 family contains on-chip digital de-emphasis, operates from a single +3.3 V or +5 V power supply, and requires minimal support circuitry. These features are ideal for DVD players & recorders, digital televisions, home theater and set top box products, and automotive audio systems.



EM6AA160256DDR.:**Features**

- Fast clock rate: 250/200MHz
- Differential Clock CK & \overline{CK}
- Bi-directional DQS
- DLL enable/disable by EMRS
- Fully synchronous operation
- Internal pipeline architecture
- Four internal banks, 4M x 16-bit for each bank
- Programmable Mode and Extended Mode registers
 - CAS Latency: 3
 - Burst length: 2, 4, 8
 - Burst Type: Sequential & Interleaved
- Individual byte write mask control
- DM Write Latency = 0
- Auto Refresh and Self Refresh
- 8192 refresh cycles / 64ms
- Precharge & active power down
- Power supplies:
 - VDD = 2.5V \pm 5%
 - VDDQ = 2.5V \pm 5%
- Interface: SSTL_2 I/O Interface
- Package: 66 Pin TSOP II, 0.65mm pin pitch
 - Pb and Halogen free

Overview

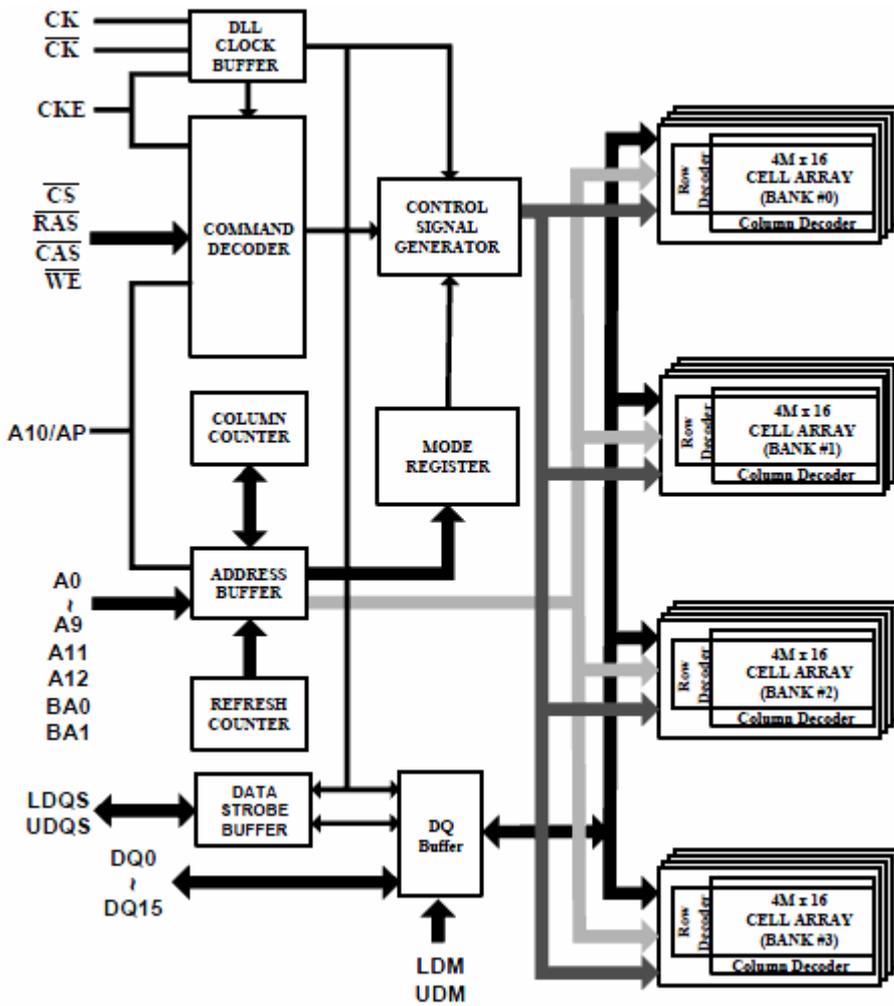
The EM6AA160 SDRAM is a high-speed CMOS double data rate synchronous DRAM containing 256 Mbits. It is internally configured as a quad 4M x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK). Data outputs occur at both rising edges of CK and \overline{CK} . Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The EM6AA160 provides programmable Read or Write burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. In addition, EM6AA160 features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth, result in a device particularly well suited to high performance main memory and graphics applications.

LCD TV Service Manual

Pin Assignment (Top View)

VDD	1	66	VSS
DQ0	2	65	DQ15
VDDQ	3	64	VSSQ
DQ1	4	63	DQ14
DQ2	5	62	DQ13
VSSQ	6	61	VDDQ
DQ3	7	60	DQ12
DQ4	8	59	DQ11
VDDQ	9	58	VSSQ
DQ5	10	57	DQ10
DQ6	11	56	DQ9
VSSQ	12	55	VDDQ
DQ7	13	54	DQ8
NC	14	53	NC
VDDQ	15	52	VSSQ
LDQS	16	51	UDQS
NC	17	50	NC
VDD	18	49	VREF
NC	19	48	VSS
LDM	20	47	UDM
WE	21	46	CK
CAS	22	45	CK
RAS	23	44	CKE
CS	24	43	NC
NC	25	42	A12
BA0	26	41	A11
BA1	27	40	A9
A10/AP	28	39	A8
A0	29	38	A7
A1	30	37	A6
A2	31	36	A5
A3	32	35	A4
VDD	33	34	VSS

Block Diagram



G962:

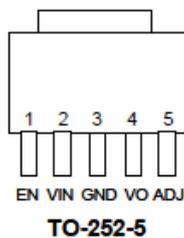
Features

- Adjustable Output from 1.2V to 4.8V Using External Resistors
- 1.5V, 1.8V and 2.5V options by Setting ADJ Pin Below 0.2V
- Over current and over temperature protection
- 500mV dropout @2A
- Enable pin
- 10µA quiescent current in shutdown
- Output recovery mode in OTP
- Connect ADJ to GND for fixed output mode
- TO-252-5 Package

Applications

- Battery powered systems
- Motherboards
- Peripheral cards
- Set Top Boxes
- Notebook Computers

Pin Configuration

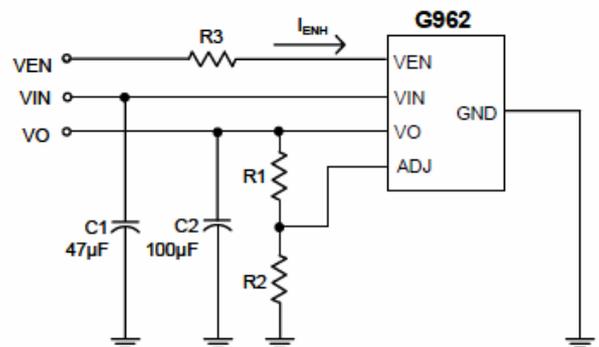


General Description

The G962 is a high performance positive voltage regulator designed for use in applications requiring very low dropout voltage at up to 2 Amps. Since it has superior dropout characteristics compared to regular LDOs, it can be used to supply 2.5V on motherboards or 1.5V, 1.8V on peripheral cards from the 3.3V supply thus allowing the elimination of costly heatsinks. An enable pin further reduces power dissipation while shut down. The G962 provides excellent regulation over variations in line, load and temperature.

The TO-252-5 is available with 1.5V, 1.8V and 2.5V internally preset outputs that are also adjustable using external resistors.

Typical Application Circuit



$$VO = \frac{1.2 (R1+R2)}{R2} \text{ Volts}$$

R2=12kΩ is recommended
R3 should be connected for current I_{ENH} restriction as $V_{EN} > V_{IN} + 0.3V$

MX29LV320DT:

32M-BIT [4M x 8 / 2M x 16] 3V SUPPLY FLASH MEMORY

FEATURES

GENERAL FEATURES

- Byte/Word switchable
 - 4,194,304 x 8 / 2,097,152 x 16
- Sector Structure
 - 8K-Byte x 8 and 64K-Byte x 63
- Extra 64K-Byte sector for security
 - Features factory locked and identifiable, and customer lockable
- Twenty-Four Sector Groups
 - Provides sector group protect function to prevent program or erase operation in the protected sector group
 - Provides chip unprotect function to allow code changing
 - Provides temporary sector group unprotect function for code changing in previously protected sector groups
- Power Supply Operation
 - Vcc 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to 1.5 x Vcc
- Low Vcc write inhibit : Vcc <= Viko
- Compatible with JEDEC standard
 - Pinout and software compatible to single power supply Flash
- **Functional compatible with MX29LV320C T/B device**

PERFORMANCE

- High Performance
 - Fast access time: 70ns
 - Fast program time: 11us/word typical utilizing accelerate function
 - Fast erase time: 0.7s/sector, 35s/chip (typical)
- Low Power Consumption
 - Low active read current: 10mA (typical) at 5MHz
 - Low standby current: 5uA (typical)
- Typical 100,000 erase/program cycle
- 10 years data retention

SOFTWARE FEATURES

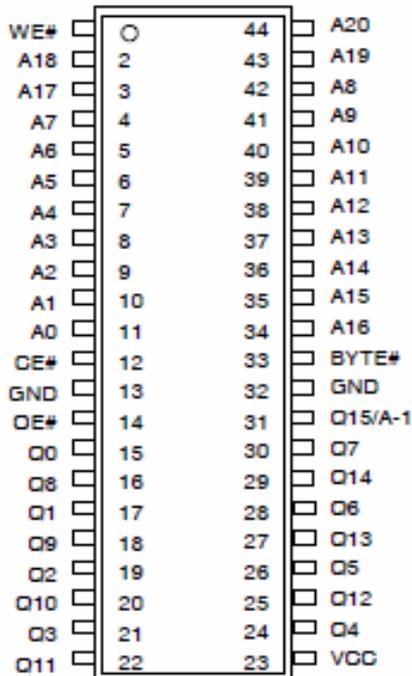
- Erase Suspend/ Erase Resume
 - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
 - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
 - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
 - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
 - Provides accelerated program capability

PIN CONFIGURATION

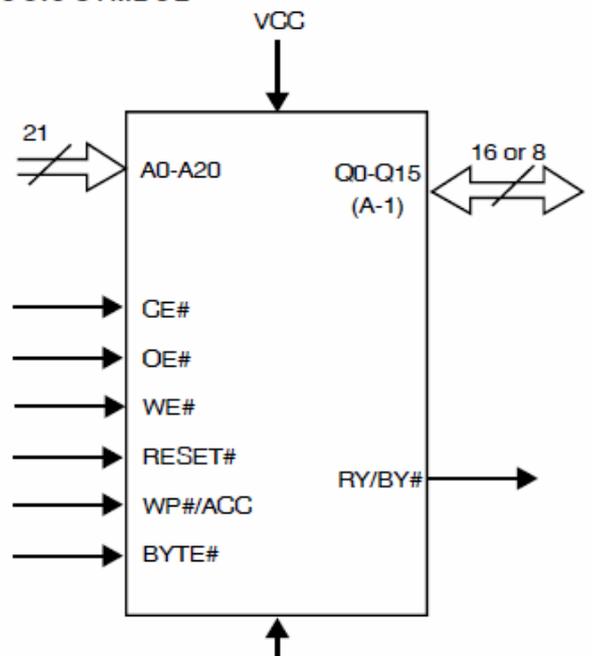
44 SOP



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A20	Address Input
Q0~Q14	15 Data Inputs/Outputs
Q15/A-1	Q15(Data Input/Output, word mode); A-1(LSB Address Input, byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
BYTE#	Word/Byte Selection Input
RESET#	Hardware Reset Pin, Active Low
RY/BY#	Ready/Busy Output
Vcc	3.0 volt-only single power supply
WP#/ACC	Hardware Write Protect/Acceleration Pin
GND	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



R2A15108FP:

2ch x 15W / 8 Ω DIGITAL AUDIO POWER AMPLIFIER

R2A15108FP

1 General Description

R2A15108FP is a Digital Power Amplifier Standard IC developed for FPD or Home audio etc.

R2A15108FP can realize maximum Power 15W x 2ch (VD=15V, THD=10%, BTL) at 8 Ω load.

It is possible to replace from the conventional analog amplifier system to the digital amplifier system easily.

2 Features

- Output Power 15W at RL=8 Ω , VD=15V, THD=10%

(Note) Basically, it is necessary thermal-pad is connected with the board heat radiation part with solder.

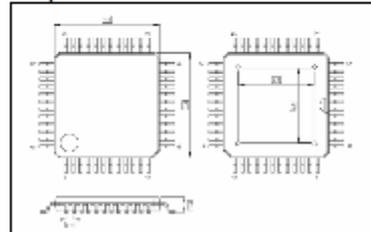
A continuous output is 10W \times 2ch at Ta=60°C by Renesas 2layer EVB.

- Built-in DC offset detection circuit of Speaker output.
- Built-in the 2 channels(BTL) output drivers by Nch-MOS FET
- Power supply voltage:
 - Single power supply operation 11V to 24V recommendation
- Built-in Over Current Protection, Over Temperature Protection, and Under Voltage Protection are built into.
- Built-in monitor terminal for protection mode.
- The over-current protection value can be adjusted by external Resistor.
- The carrier frequency can be adjusted by external Resistor.
- The gain can be changed to four setting by two terminals.

Package: 48 pins HTQFP

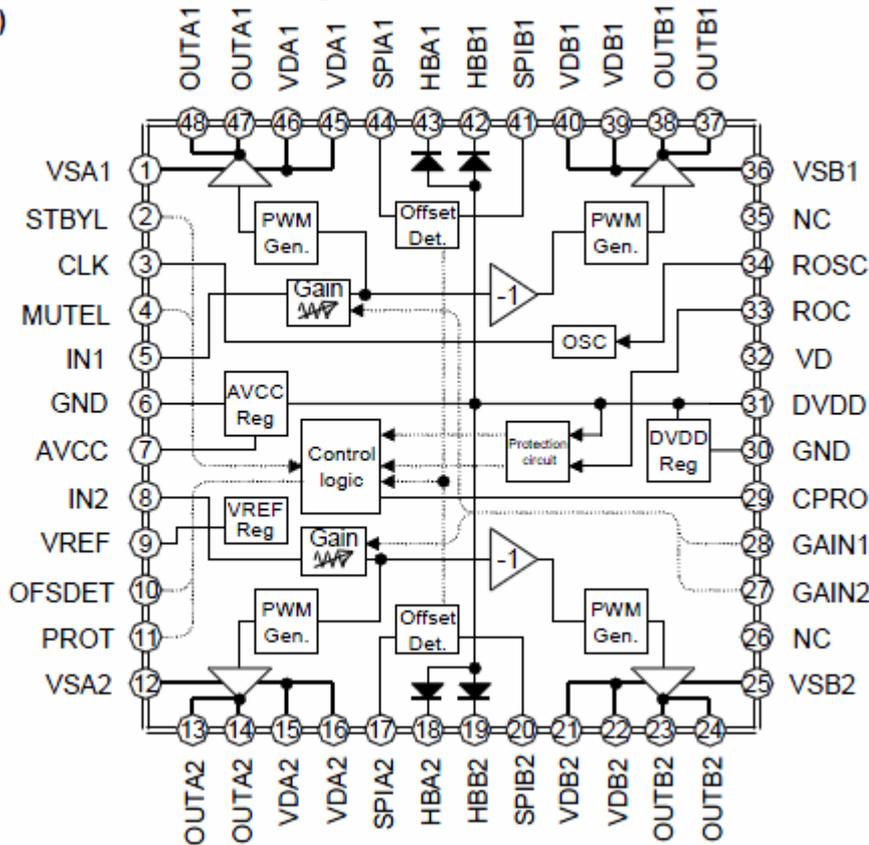
(Body : 7x7mm Lead pitch : 0.5mm)

48pin HTQFP



LCD TV Service Manual

Pin Layout and Internal Block Diagram (Top View)



No.	Name	I/O	Description
1	VSA1	—	CH1-A block: Ground pin for power output stage
2	STBYL	I	Stand-by control pin. "L": Stand-by status. This terminal has pull-down 50 k Ω (typ).
3	CLK	I/O	The carrier clock is output at Master mode and is input at slave mode. Carrier frequency is triangle wave.
4	MUTEL	I	Mute control pin. "L": Mute status.
5	IN1	I	CH1 Analog signal input pin
6	GND	—	Ground pin
7	AVCC	O	Filter pin of 5V with built-in analog
8	IN2	I	CH2 Analog signal input pin
9	VREF	I/O	Reference power supply filter pin in analog part
10	OFSDET	O	This terminal shows DC offset mode. "L": Detect (Open drain output)
11	PROT	O	Protection mode monitor. "L": Protection status. (Open drain output)
12	VSA2	—	CH2-A block: Ground pin for power output stage
13	OUTA2	—	CH2-A block: Power output pin
14	OUTA2	O	CH2-A block: Power output pin
15	VDA2	—	CH2-A block: Power supply for power output stage (VD is supplied)
16	VDA2	—	CH2-A block: Power supply for power output stage (VD is supplied)
17	SPIA2	I	CH2-A block: Input pin for detecting DC offset voltage at speaker pin
18	HBA2	I/O	CH2-A block: Capacitor connection pin for bootstrap on "H" side
19	HBB2	I/O	CH2-B block: Capacitor connection pin for bootstrap on "H" side
20	SPIB2	I	CH2-B block: Unusual detection input pin of DC offset voltage of speaker pin
21	VDB2	—	CH2-B block: Power supply for power output stage (VD is supplied)
22	VDB2	—	CH2-B block: Power supply for power output stage (VD is supplied)
23	OUTB2	O	CH2-B block: Power output pin
24	OUTB2	—	CH2-B block: Power output pin
25	VSB2	—	CH2-B block: Ground pin for power output stage
26	(N.C.)	—	—
27	GAIN2	I	Gain setting terminal L: GND H: Open (Built-in Pull-up Resistance)

LCD TV Service Manual

28	GAIN1	I	Gain setting terminal L:GND H:Open (Built-in Pull-up Resistance)
29	CPRO	O	The time from protection mode to normal mode can be set by external capacitor.
30	GND	—	Ground pin
31	DVDD	O	Pre circuit:10V in built-in power supply filter pin
32	VD	—	power supply pin
33	ROC	I	Adjustment for overcurrent detection value by external resistance.
34	ROSC	I	Adjustment for carrier frequency by external resistance. When it is connected to the AVCC, the IC's mode becomes a slave mode.
35	(N.C.)	—	—
36	VSB1	—	CH1-B block: Ground pin for power output stage
37	OUTB1	O	CH1-B block: Power output pin
38	OUTB1	O	CH1-B block: Power output pin
39	VDB1	—	CH1-B block: Power supply for power output stage(VD is supplied)
40	VDB1	—	CH1-B block: Power supply for power output stage(VD is supplied)
41	SPIB1	I	CH1-B block: Unusual detection input pin of DC offset voltage of speaker pin
42	HBB1	I/O	CH1-B block: Capacitor connection pin for bootstrap on "H" side
43	HBA1	I/O	CH1-A block: Capacitor connection pin for bootstrap on "H" side
44	SPIA1	I	CH1-A block: Input pin for detecting unusual operations of DC offset voltage at speaker pin
45	VDA1	—	CH1-A block: Power supply for power output stage(VD is supplied)
46	VDA1	—	CH1-A block: Power supply for power output stage(VD is supplied)
47	OUTA1	O	CH1-A block: Power output pin
48	OUTA1	—	CH1-A block: Power output pin

TDA9885TS:

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

1 FEATURES

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier, AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics, and excellent pulse response
- Gated phase detector for L and L-accnt standard
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I²C-bus
- Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75, and 58.75 MHz
- 4 MHz reference frequency input: signal from Phase-Locked Loop (PLL) tuning system or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- External AGC setting via pin OP1
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I²C-bus
- TakeOver Point (TOP) adjustable via I²C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0, and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled



- SIF-AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I²C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- Four selectable I²C-bus addresses
- I²C-bus control for all functions
- I²C-bus transceiver with pin programmable Module Address (MAD).

2 GENERAL DESCRIPTION

The TDA9885 is an alignment-free multistandard (PAL and NTSC) vision and sound IF signal PLL demodulator for negative modulation only and FM processing.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing.

3 APPLICATIONS

- TV, VTR, PC, and STB applications.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9885T/V3	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9885TS/V3	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9885HN/V3	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3
TDA9886T/V4	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9886TS/V4	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9886HN/V4	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

TJ2996–R1.3:

DDR Termination Regulator

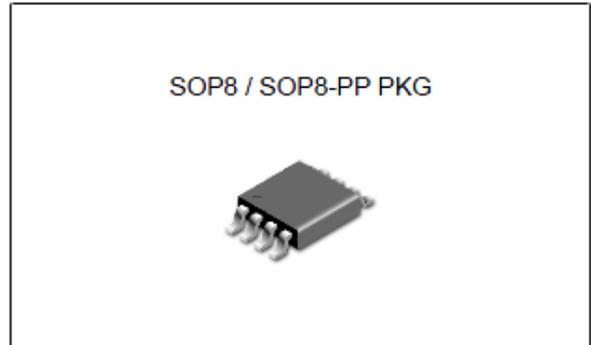
TJ2996

FEATURES

- Source and sink current
- Low output voltage offset
- No external resistors required
- Linear topology
- Suspend to Ram (STR) functionality
- Low external component count
- Thermal Shutdown
- Available in SOP8, SOP8-PP Packages

APPLICATION

- DDR-I and DDR-II Termination Voltage
- SSTL-2 and SSTL-3 Termination
- HSTL Termination



ORDERING INFORMATION

Device (Marking)	Package
TJ2996D	SOP8
TJ2996DP	SOP8-PP

DESCRIPTION

The TJ2996 linear regulator is designed to meet the JEDEC SSTL-2 and SSTL-3 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. The TJ2996 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DIMMs. An additional feature found on the TJ2996 is an active low shutdown (\overline{SD}) pin that provides Suspend To RAM (STR) functionality. When \overline{SD} is pulled low the V_{TT} output will tri-state providing a high impedance output, but, V_{REF} will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage to GND	PV_{IN}	-0.3	6.0	V
	AV_{IN}	-0.3	6.0	
	V_{DDQ}	-0.3	6.0	
Lead Temperature (Soldering, 10 sec)	T_{SOL}		260	°C
Storage Temperature Range	T_{STG}	-65	150	°C
Operating Junction Temperature Range	T_{JOPR}	-40	125	°C

LCD TV Service Manual

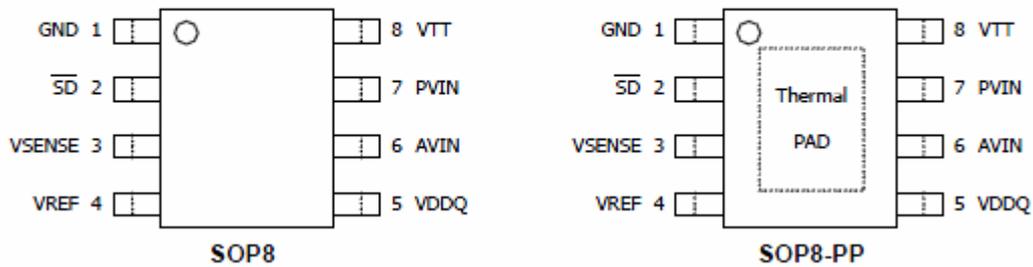
Recommended Operation Range

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
AV _{IN} to GND	AV _{IN}	2.3	5.5	V
PV _{IN} & SDV _{IN} to GND	PV _{IN} & SD Input	0	AV _{IN}	V

Ordering Information

Package	Order No.	Description	Package Marking	Supplied As
SOP8	TJ2996D	DDR Termination Regulator	TJ2996	Reel
SOP8-PP	TJ2996DP	DDR Termination Regulator	TJ2996	Reel

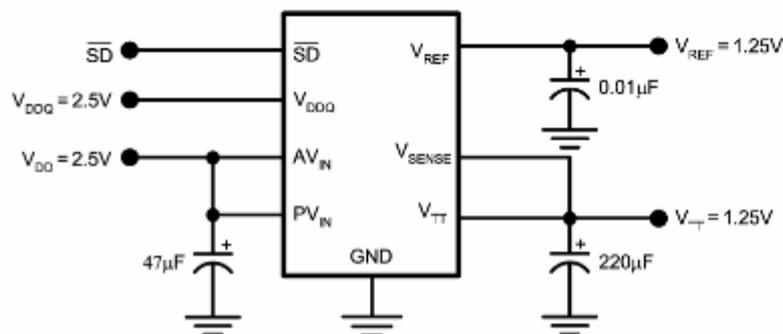
PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	Pin Function
1	GND	Ground
2	\overline{SD}	Shutdown
3	VSENSE	Feedback Pin for Regulating V _{TT}
4	VREF	Buffered Internal Reference Voltage of V _{DDQ} /2
5	VDDQ	Input for Internal Reference Equal to V _{DDQ} /2
6	AVIN	Analog Input Pin
7	PVIN	Power Input Pin
8	VTT	Output Voltage for Connection to Termination Resistors
	Exposed Thermal PAD	Exposed Thermal Connection. Connect to Soft Ground. (SOP8-PP Only)

TYPICAL APPLICATION



WM8501:**24-bit 192kHz Stereo DAC with 1.7Vrms Line Driver****DESCRIPTION**

The WM8501 is a high performance stereo DAC with an integrated 1.7Vrms line driver. It is designed for audio applications that require a high voltage output along with enhanced load drive capability.

The WM8501 supports data input word lengths from 16 to 24-bits and sampling rates up to 192kHz. The WM8501 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and stereo DAC in a 14-lead SOIC package.

The hardware control interface is used for the selection of audio data interface format, enable and de-emphasis. The WM8501 supports I²S, right Justified or DSP interfaces.

Operating on separate analog and digital supplies the WM8501 offers very lower power consumption from the digital section, whilst supporting enhanced load drive from the analogue output.

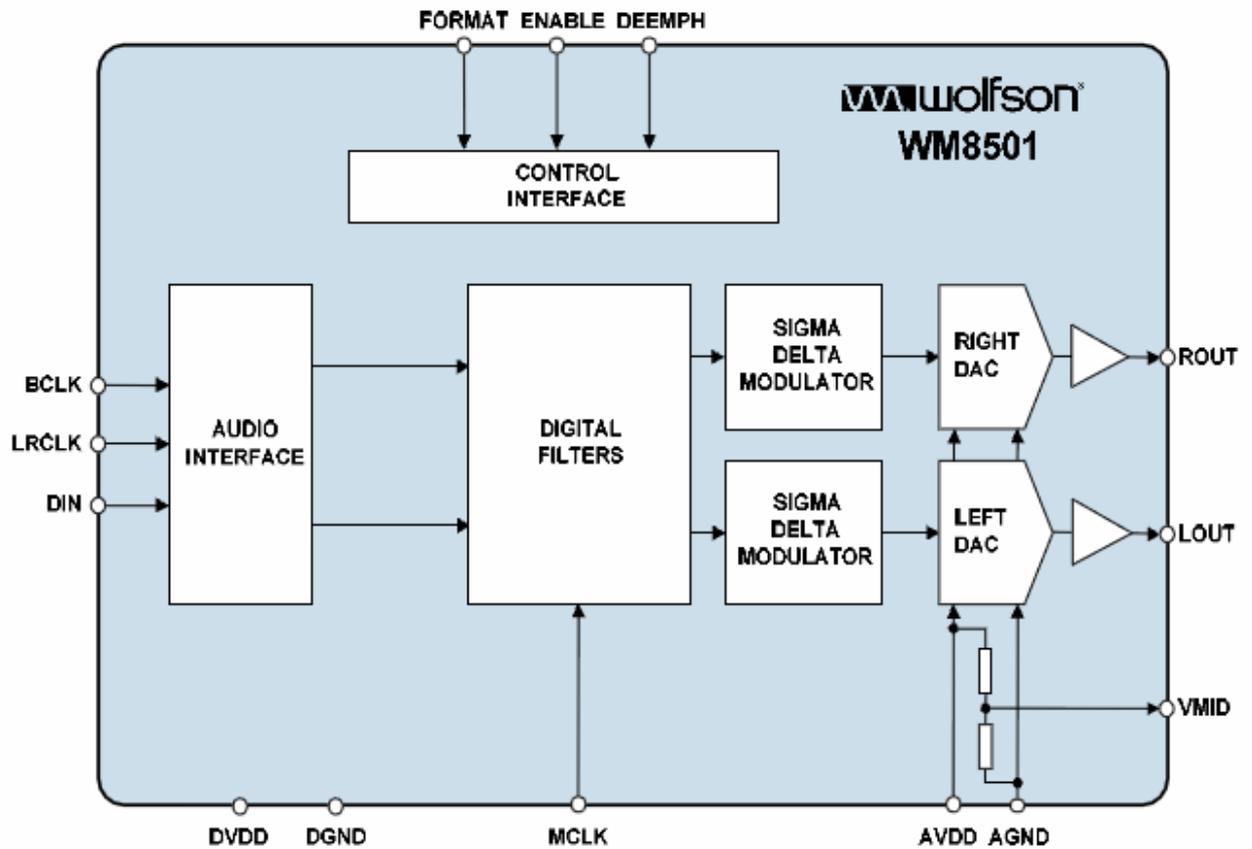
FEATURES

- Stereo DAC with 1.7Vrms line driver from 5V analogue supply
- Audio performance
 - 100dB SNR ('A' weighted @ 48kHz)
 - -88dB THD
- DAC Sampling Frequency: 8kHz – 192kHz
- Pin Selectable Audio Data Interface Format
 - I²S, 16-bit Right Justified or DSP
- 14-lead SOIC package
- 4.5V - 5.5V analogue, 2.7V - 5.5V digital supply operation

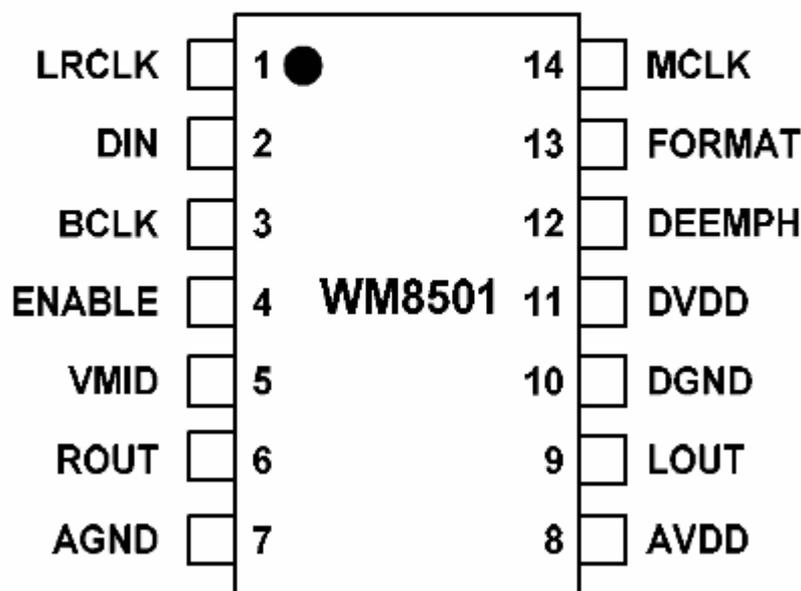
APPLICATIONS

- STB
- DVD
- Digital TV

BLOCK DIAGRAM



PIN CONFIGURATION



LCD TV Service Manual

PIN DESCRIPTION

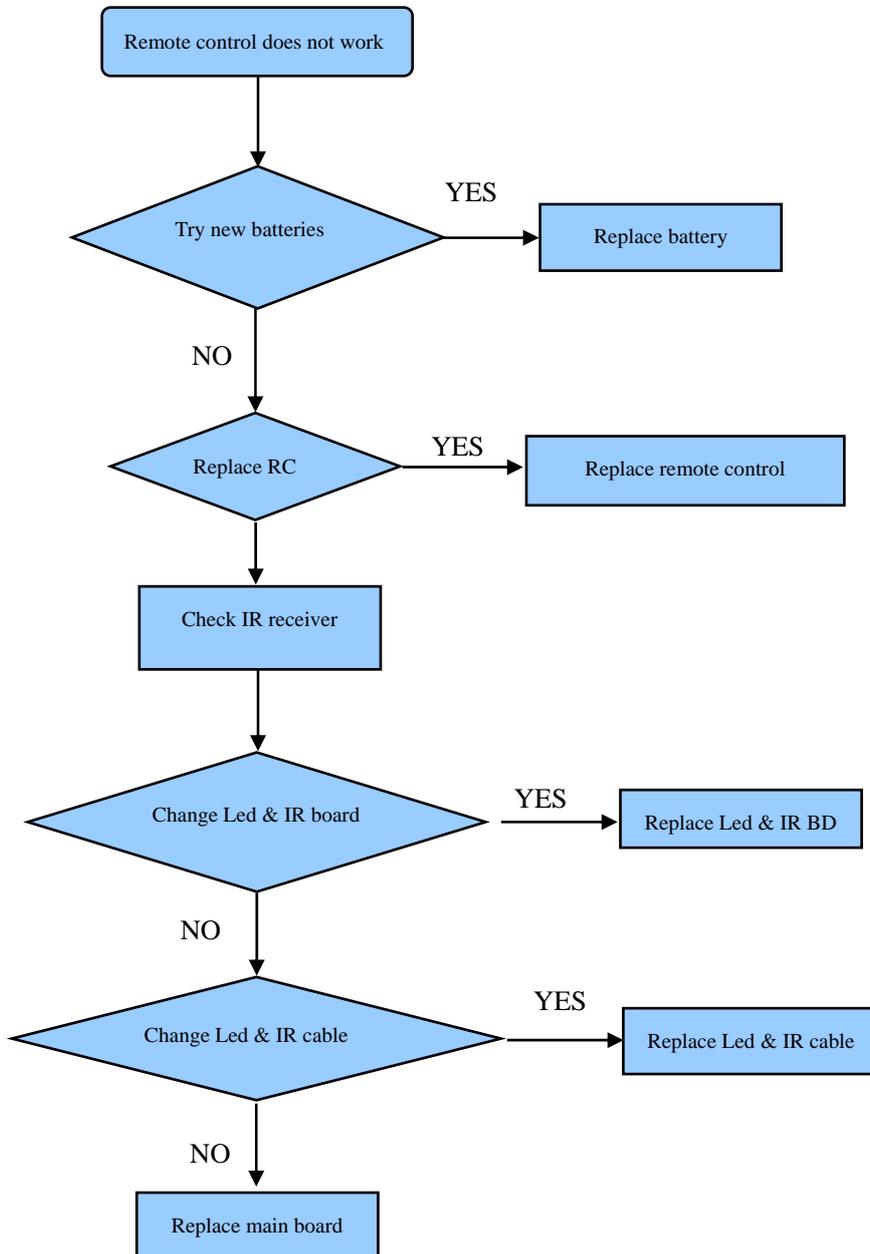
PIN	NAME	TYPE	DESCRIPTION
1	LRCLK	Digital input	Sample rate clock input
2	DIN	Digital input	Serial audio data input
3	BCLK	Digital input	Bit clock input
4	ENABLE	Digital input	Enable input – 0 = powered down, 1 = enabled
5	VMID	Analogue output	Analogue internal reference
6	ROUT	Analogue output	Right channel DAC output
7	AGND	Supply	Ground reference for analog circuits and substrate connection
8	AVDD	Supply	Positive supply for analog circuits
9	LOUT	Analogue output	Left channel DAC output
10	DGND	Digital Supply	Digital ground supply
11	DVDD	Digital Supply	Digital positive supply
12	DEEMPH	Digital input	De-emphasis select, Internal pull down High = de-emphasis ON Low = de-emphasis OFF
13	FORMAT	Digital input	Data input format select, Internal pull up Low = 16-bit right justified or DSP (Mode B) High = 16-24-bit I ² S or DSP (Mode A)
14	MCLK	Digital input	Master clock input

Note:

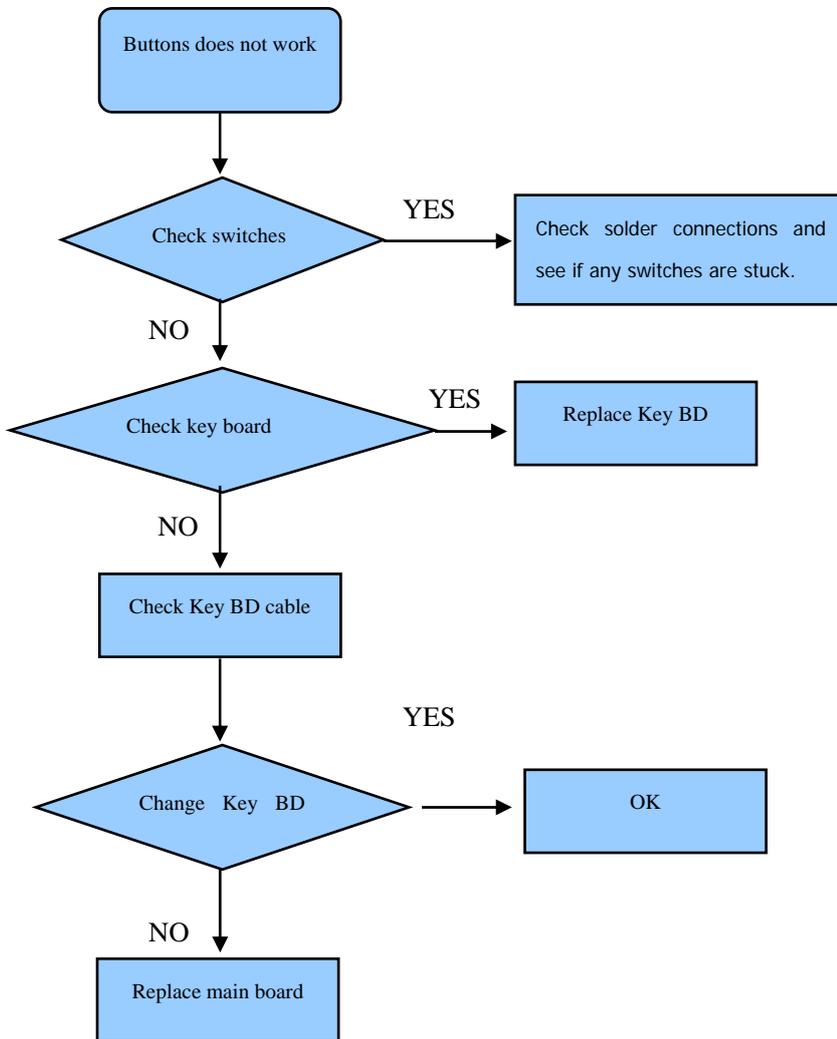
1. Digital input pins have Schmitt trigger input buffers.

4.4 Troubleshooting

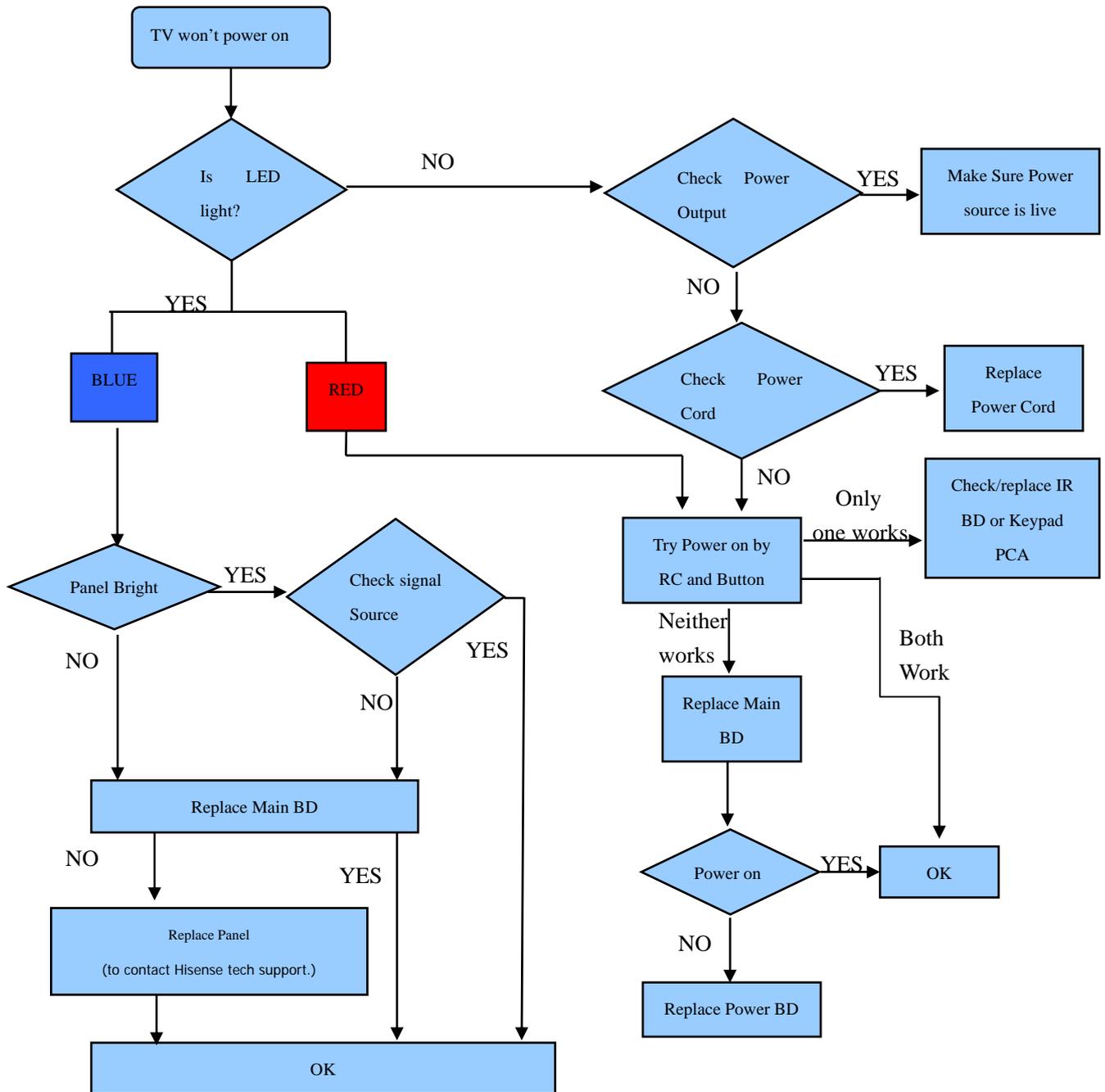
4.4.1 Troubleshooting for Remote Control



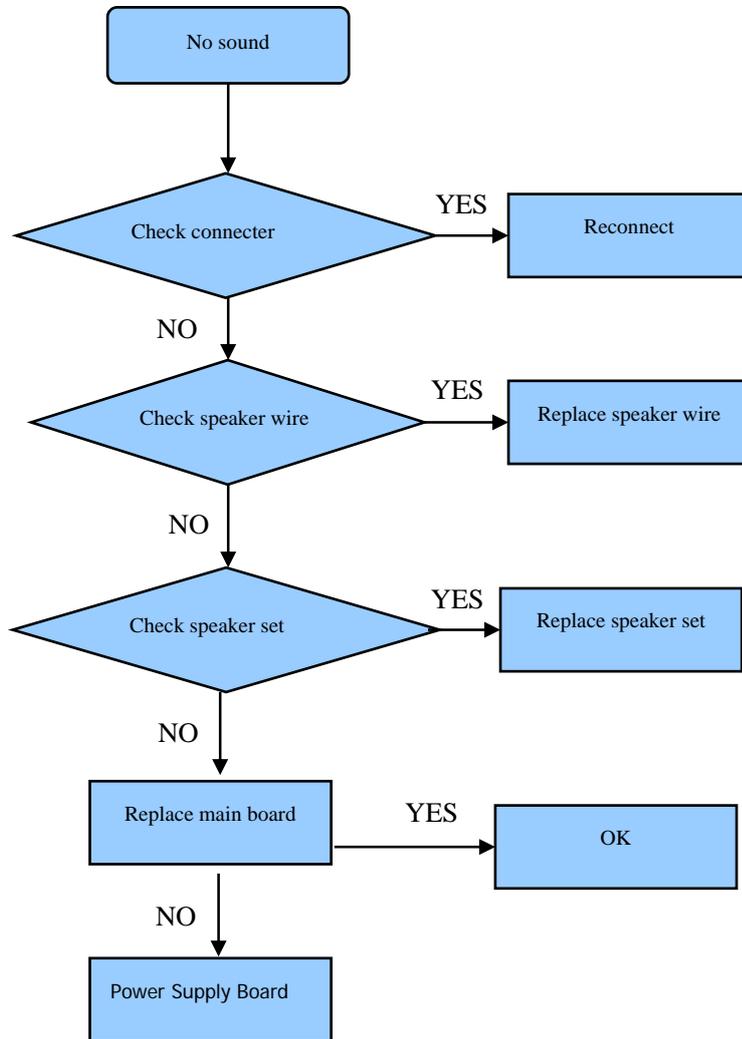
4.4.2 Troubleshooting for Function Key



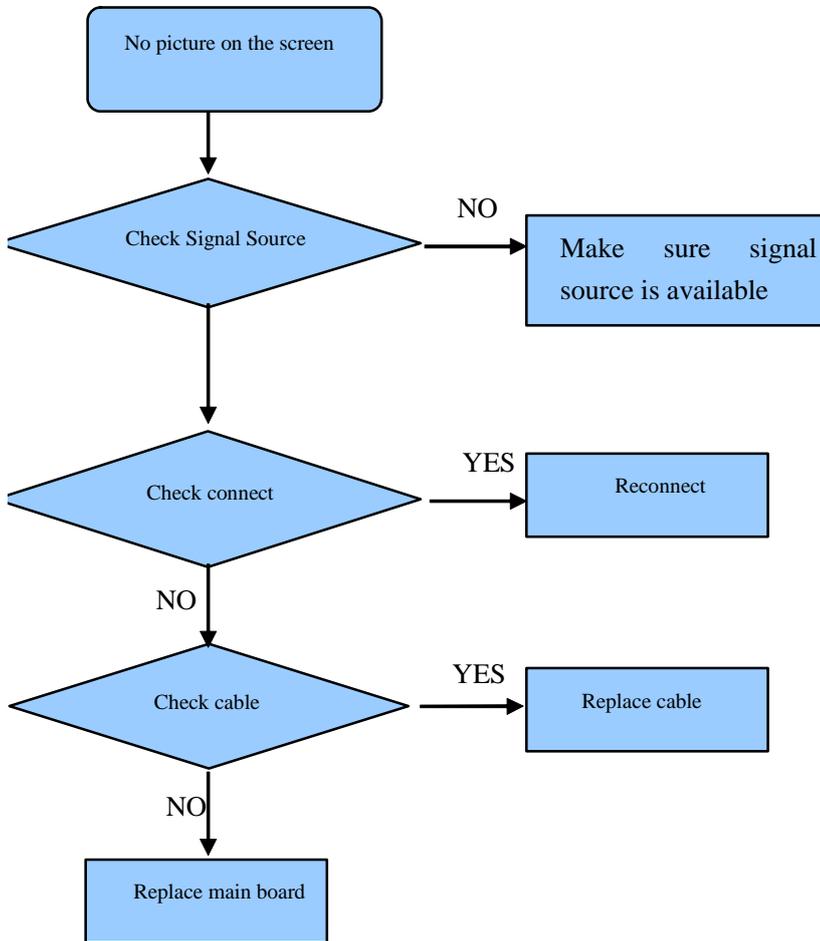
4.4.3 TV won't Power On



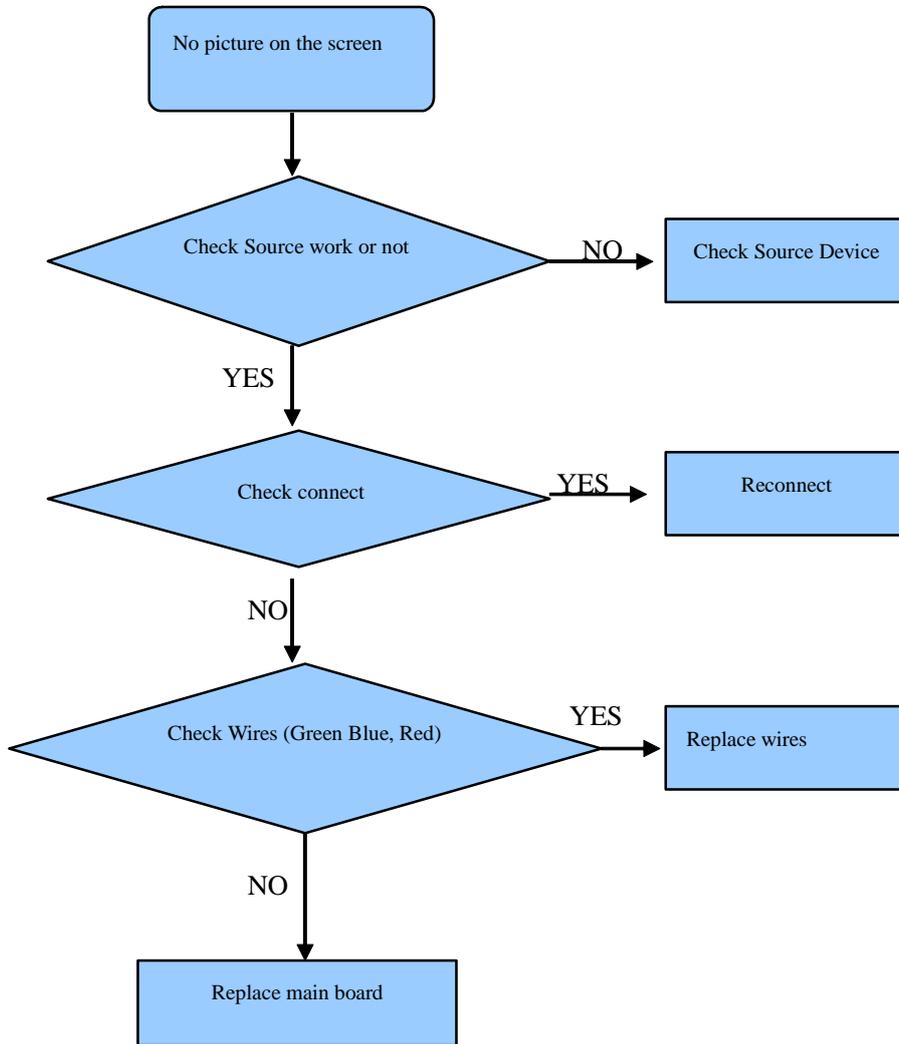
4.4.4 Troubleshooting for Audio



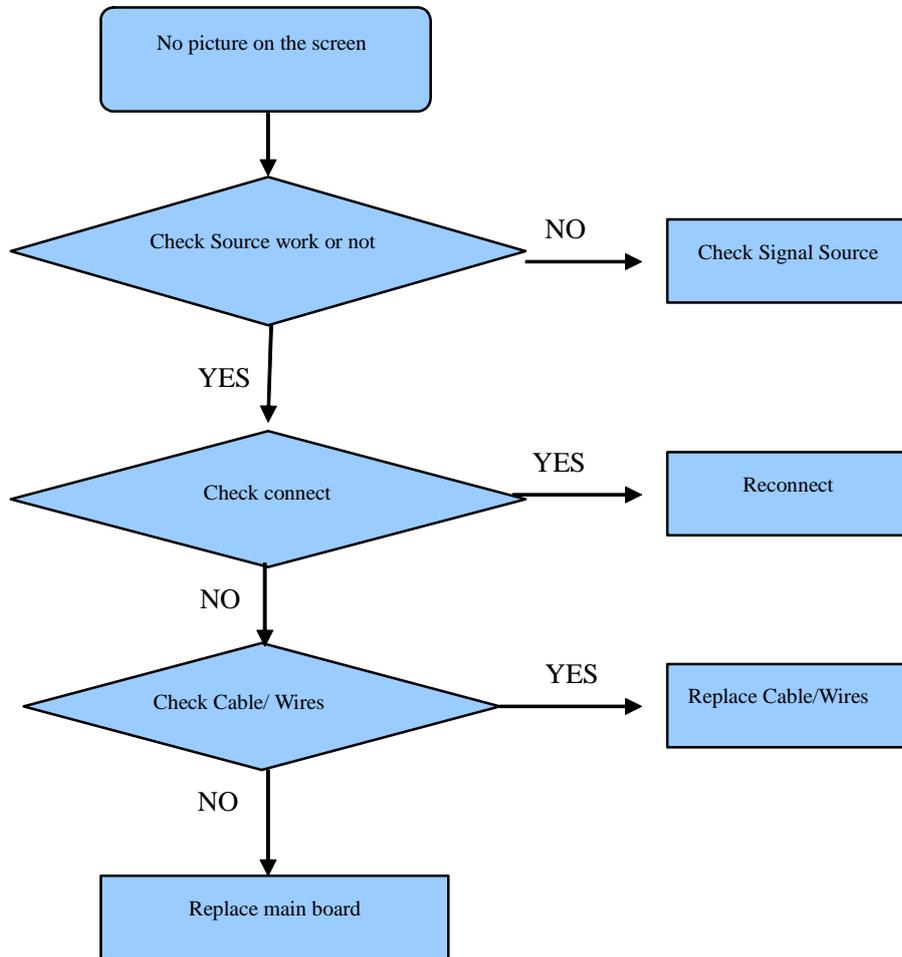
4.4.5 Troubleshooting for TV/VGA/HDMI input



4.4.6 Troubleshooting for YPbPr input

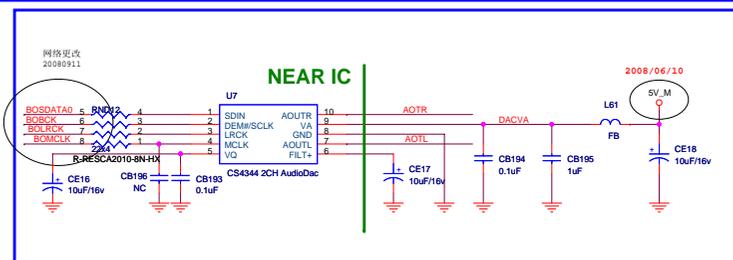
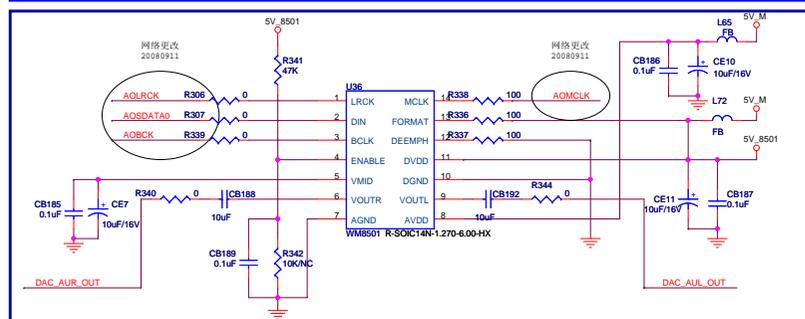
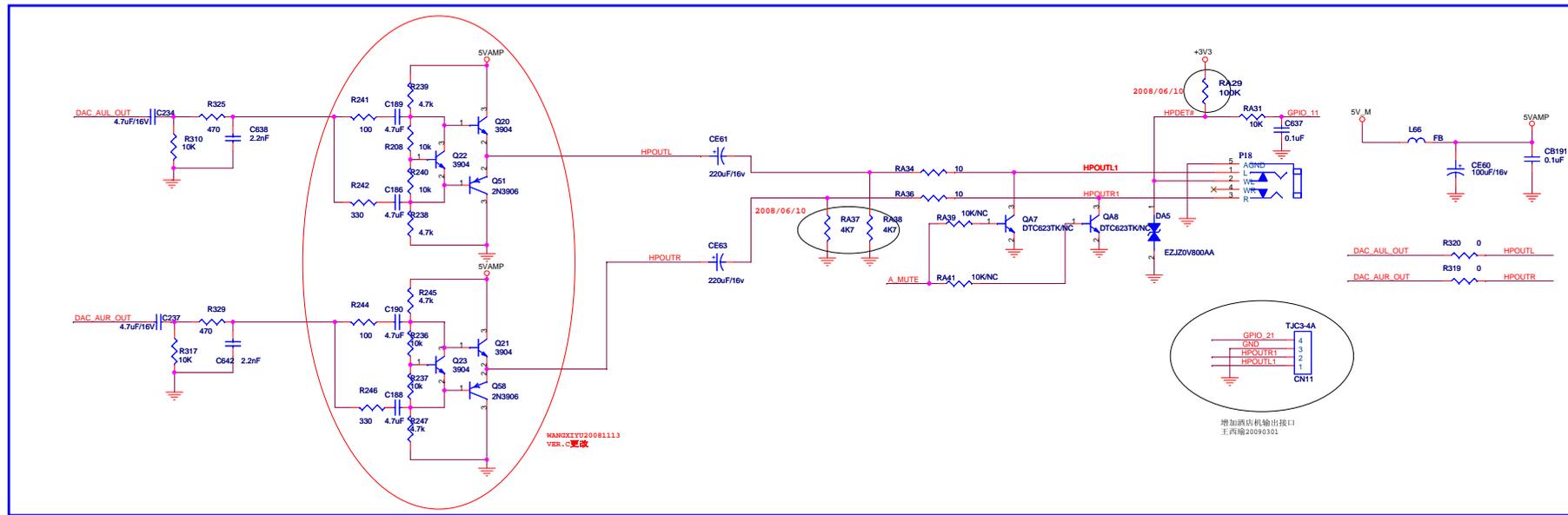
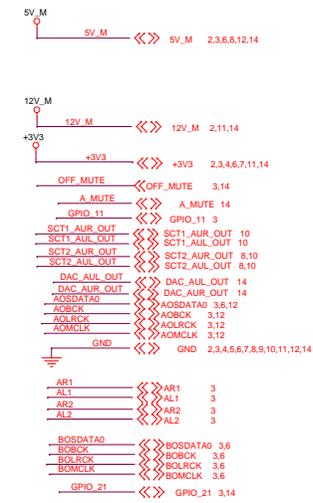
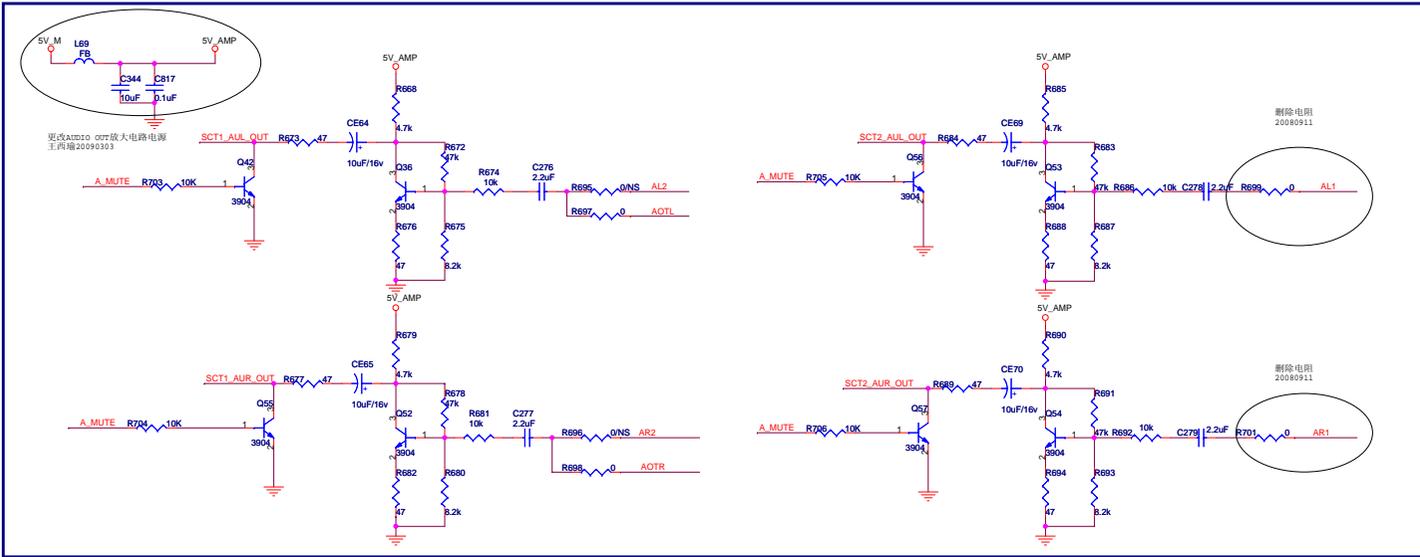


4.4.7 Troubleshooting for Video/S-Video input

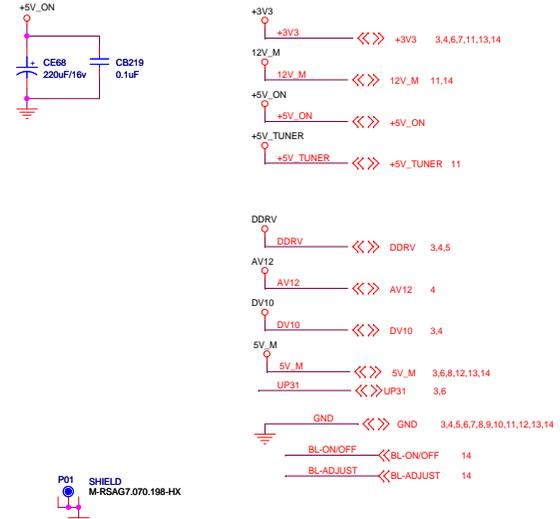
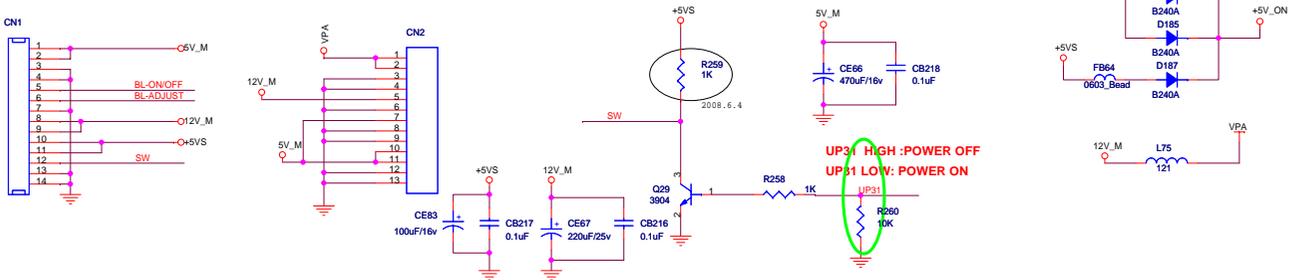


5. Explode View

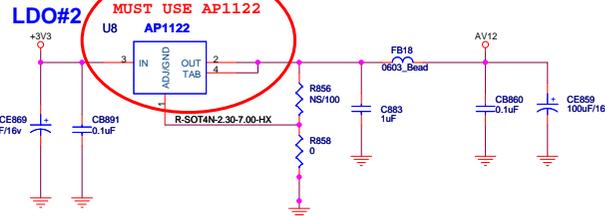
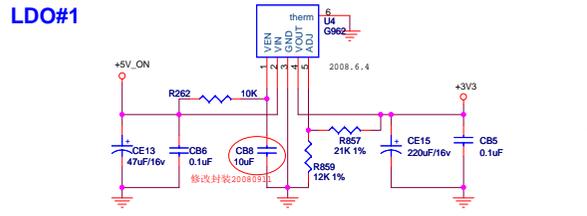
6. Schematic circuit diagram



MAIN POWER



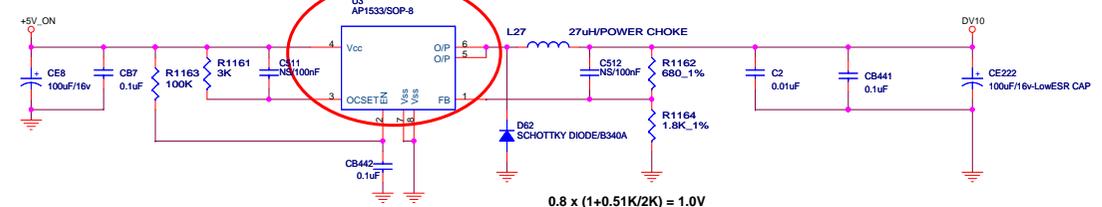
Power for MT8222 only (Always on)



1.2 x (21K+12K)/12K= 3.3V
 5V to 3.3V
 Estimated Power consumed : ??? A

3.3V to 1.2V
 Estimated Power consumed : ??? A

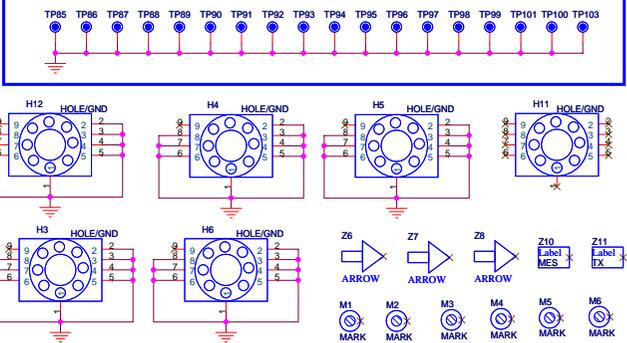
Switch Regulator MUST USE AP1533 Core Power 1.0V



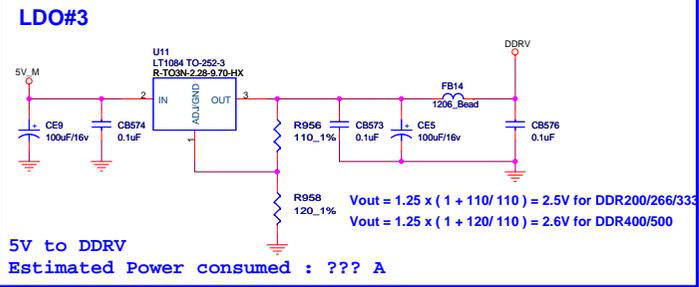
5V to 1.0V
 Estimated Power consumed : ??? A

$0.8 \times (1+0.51K/2K) = 1.0V$

Test GND Pin (Spread Around PCB)

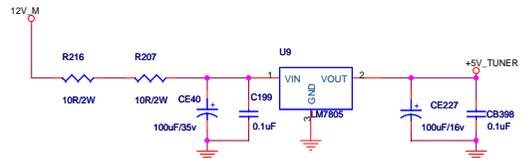


Works at normal mode



5V to DDRV
 Estimated Power consumed : ??? A

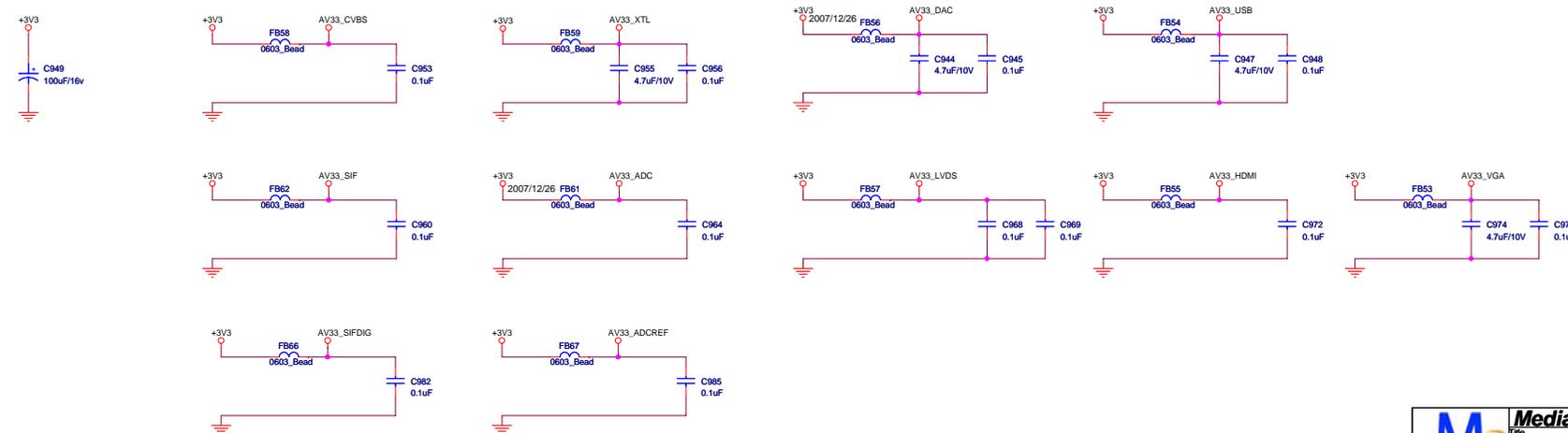
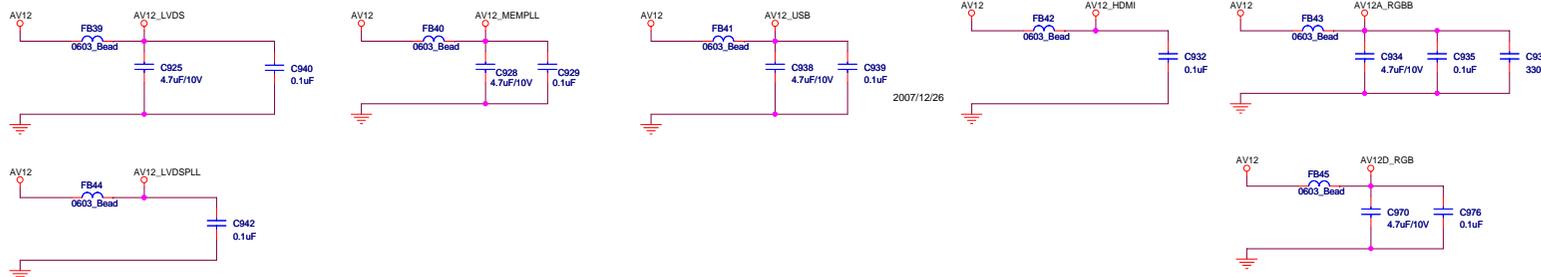
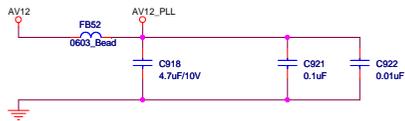
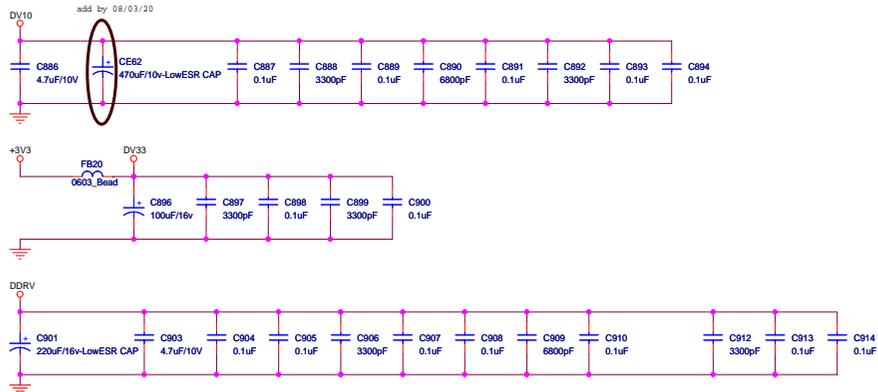
$V_{out} = 1.25 \times (1 + 110/110) = 2.5V$ for DDR200/266/333
 $V_{out} = 1.25 \times (1 + 120/110) = 2.6V$ for DDR400/500



12V to 5V
 For Tuner 5V power

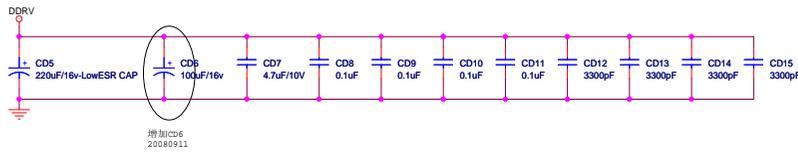
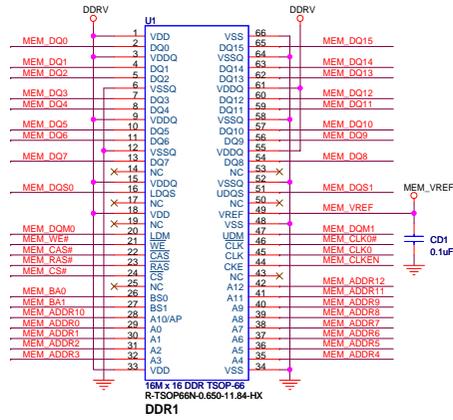
If use sdram ,NC FB14
 If use ddr ,NC FB14

(Bypass CAPs around MT8222)

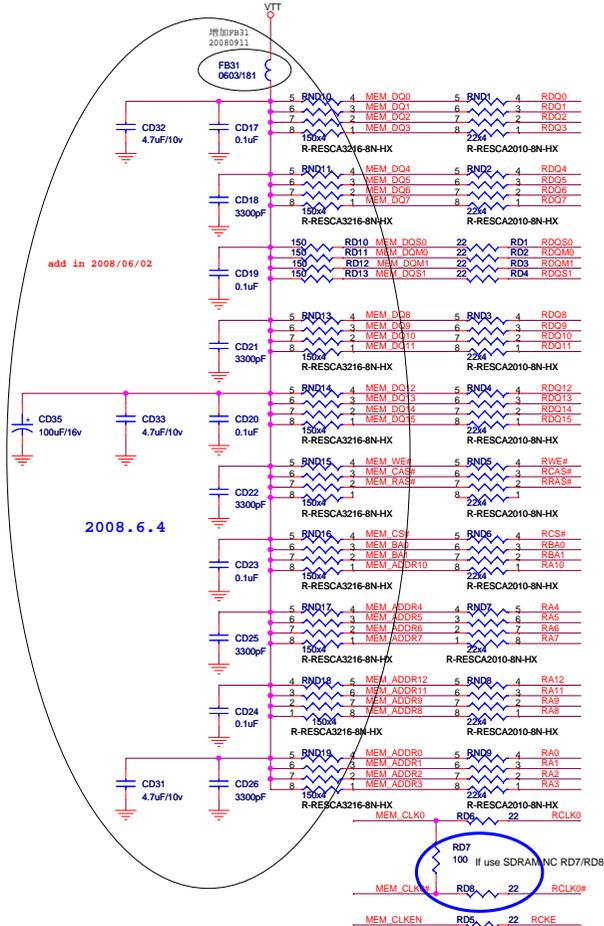
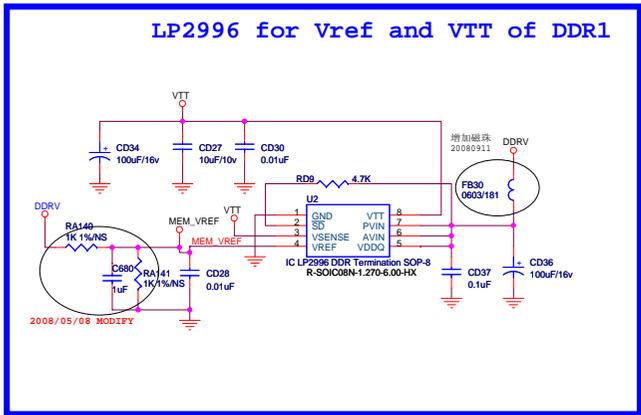


AV33_SIFDIG	AV33_SIFDIG	AV33_SIFDIG	3
AV12D_RGB	AV12D_RGB	AV12D_RGB	3
AV33_ADCREF	AV33_ADCREF	AV33_ADCREF	3
AV12A_RGGB	AV12A_RGGB	AV12A_RGGB	3
DV10	DV10	DV10	2,3
+3V3	+3V3	+3V3	2,3,6,7,11,13,14
DV33	DV33	DV33	3
AV12	AV12	AV12	2
DDRV	DDRV	DDRV	2,3,5
AV12_USB	AV12_USB	AV12_USB	3
AV12_HDMI	AV12_HDMI	AV12_HDMI	3
AV12_PLL	AV12_PLL	AV12_PLL	3
AV12_MEMPLL	AV12_MEMPLL	AV12_MEMPLL	3
AV12_LVDS	AV12_LVDS	AV12_LVDS	3
AV12_LVDSPLL	AV12_LVDSPLL	AV12_LVDSPLL	3
AV33_CVBS	AV33_CVBS	AV33_CVBS	3
AV33_SIF	AV33_SIF	AV33_SIF	3
AV33_XTL	AV33_XTL	AV33_XTL	3
AV33_ADC	AV33_ADC	AV33_ADC	3
AV33_DAC	AV33_DAC	AV33_DAC	3
AV33_LVDS	AV33_LVDS	AV33_LVDS	3
AV33_USB	AV33_USB	AV33_USB	3
AV33_HDMI	AV33_HDMI	AV33_HDMI	3
AV33_VGA	AV33_VGA	AV33_VGA	3
GND	GND	GND	2,3,5,6,7,8,9,10,11,12,13,14

(DDR1 DRAM With Termination)

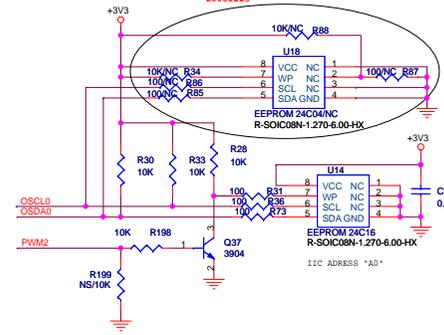


If use sdram CD34 CD26 CD27 RD9 CD28 CD29 CD30 UD2 NC
 If use ddr CD34 CD26 CD27 RD9 CD28 CD29 CD30 UD2 ON

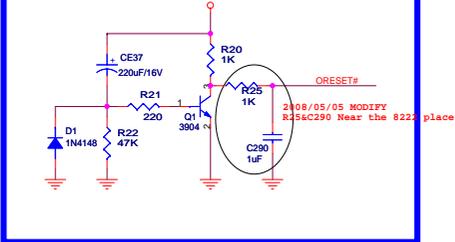


- RDQS0 <<<> RDQS0 3
- RDQS1 <<<> RDQS1 3
- RDQM0 <<<> RDQM0 3
- RDQM1 <<<> RDQM1 3
- RWE# <<<> RWE# 3
- RCAS# <<<> RCAS# 3
- RRAS# <<<> RRAS# 3
- RCS# <<<> RCS# 3
- RCKE <<<> RCKE 3
- RDQ[15..0] <<<> RDQ[15..0] 3
- RA[12..0] <<<> RA[12..0] 3
- RCLK0 <<<> RCLK0 3
- RCLK# <<<> RCLK# 3
- RBA0 <<<> RBA0 3
- RBA1 <<<> RBA1 3
- MEM_VREF <<<> MEM_VREF 3
- DDRV <<<> DDRV 2,3,4
- GND <<<> GND 2,3,4,6,7,8,9,10,11,12,13,14

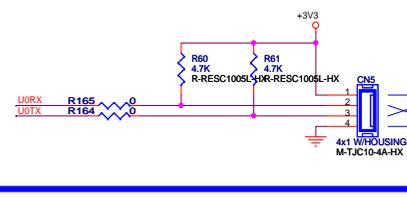
System E2PROM



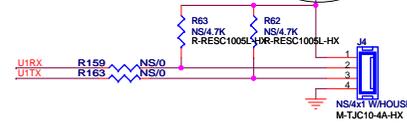
System Reset#



1st UART IF (For Code download and Debug)



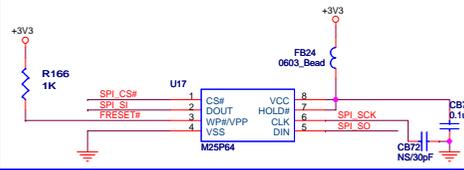
2nd UART IF



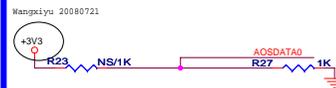
- PWM2 >>> PWM2 3
- ORESET# >>> ORESET# 3
- OIRI >>> OIRI 3
- UORX >>> UORX 3
- UOTX >>> UOTX 3
- U1RX >>> U1RX 3
- U1TX >>> U1TX 3
- USB_DP0 >>> USB_DP0 3
- USB_DM0 >>> USB_DM0 3
- USB_DP1 >>> USB_DP1 3
- USB_DM1 >>> USB_DM1 3
- OSCL0 >>> OSCL0 3,8,11,14
- OSDA0 >>> OSDA0 3,8,11,14
- GPIO_2 >>> GPIO_2 3,13
- GPIO_3 >>> GPIO_3 3,13
- GPIO_5 >>> GPIO_5 3,13
- GPIO_6 >>> GPIO_6 3,13
- GPIO_7 >>> GPIO_7 3,13
- GPIO_8 >>> GPIO_8 3
- GPIO_9 >>> GPIO_9 3
- GPIO_10 >>> GPIO_10 3

Serial Flash

位置尽量靠近8222, 附近若有IO需要串磁珠并且避让, EMC问题



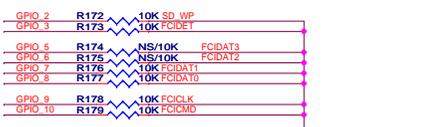
MT8222 Trapping



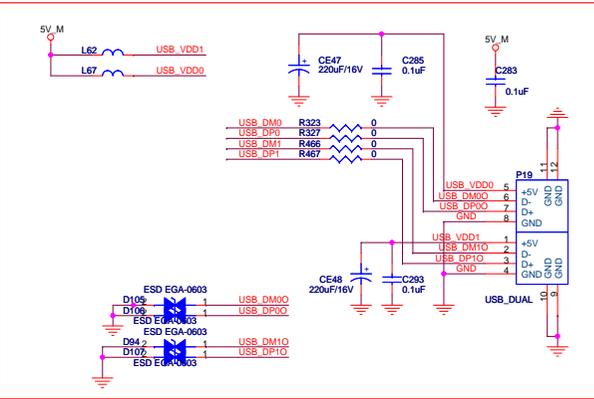
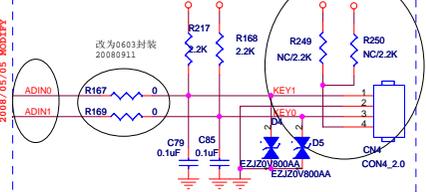
Status	ICE	AOBCLK	AOLRCK	Description
Normal	0v	0v	0v	Normal operation ST/SST flash
TEST_ICE	1v	0v	0v	ICE mode
TEST_CPLM	1v	0v	1v	Used in simulation and pattern generation
TEST_SCAN	1v	1v	0v	Used to generate ATPG test patterns
OLT_MODE	1v	1v	1v	OLT mode

AOSDATA0	Description
0v	ST/SST flash
1v	ATMEL flash

MEMORY CARD I/F GPIO RESERVED

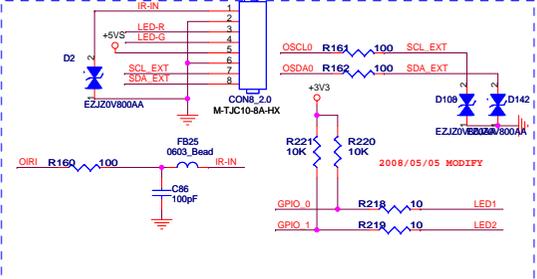


ADC KEYPAD



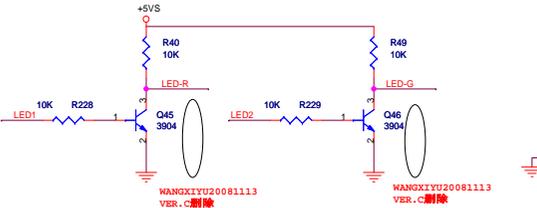
- +3V3 >>> +3V3 2,3,4,7,11,13,14
- +5V_ON >>> +5V_ON 2
- 5V_M >>> 5V_M 2,3,8,12,13,14
- GND >>> GND 2,3,4,5,7,8,9,10,11,12,13,14
- ICE_AOSDATA0 >>> ICE_AOSDATA0 3,12,13
- ADIN0 <<< ADIN0 3
- ADIN1 <<< ADIN1 3
- GPIO_0 <<< GPIO_0 3
- GPIO_1 <<< GPIO_1 3
- CEC <<< CEC 3,7
- UP31 <<< UP31 2,3

IR



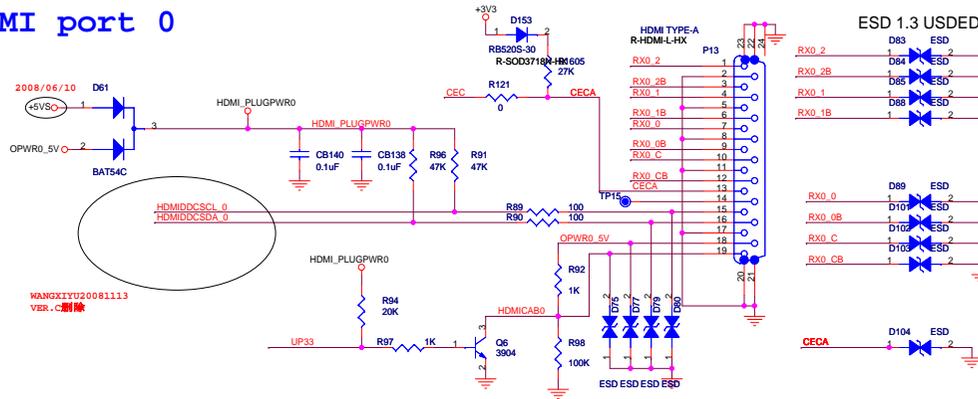
OPTION for CEC Stand by Function

VER.D 更改: 删除CEC部分元器件
王西瑜 20090105

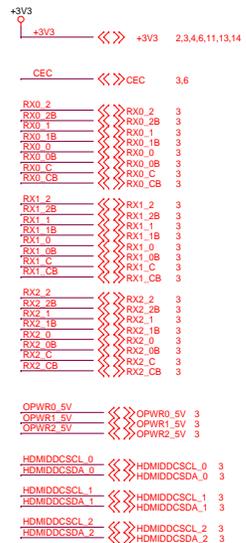
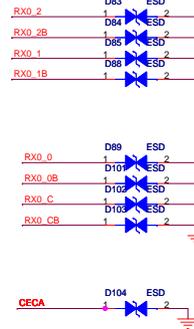


MediaTek Confidential

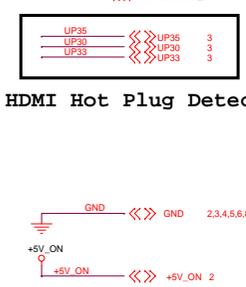
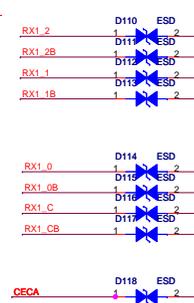
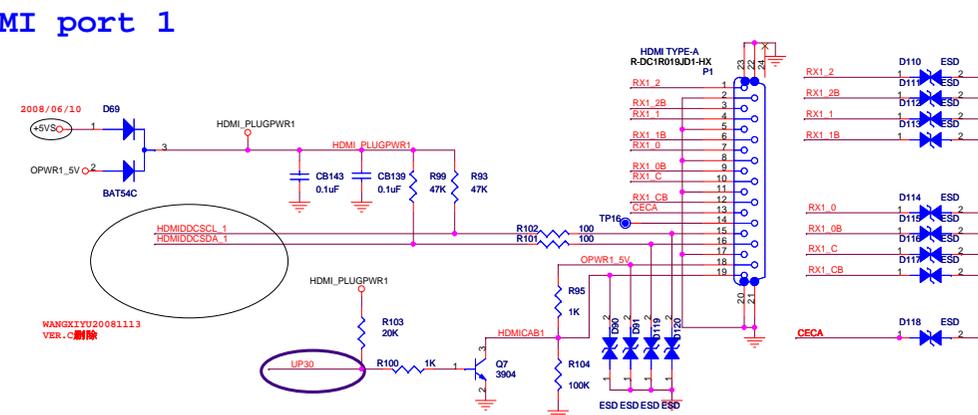
HDMI port 0



ESD 1.3 USED

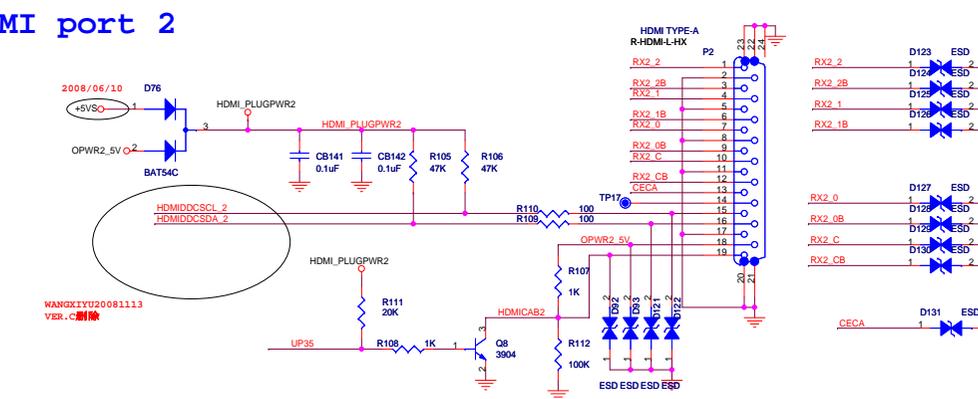


HDMI port 1

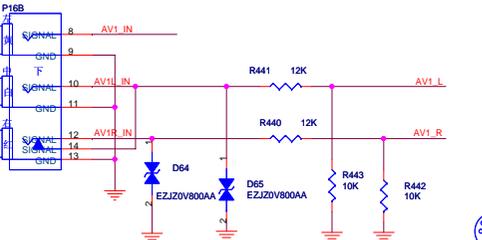


(HDMI Hot Plug Detect)

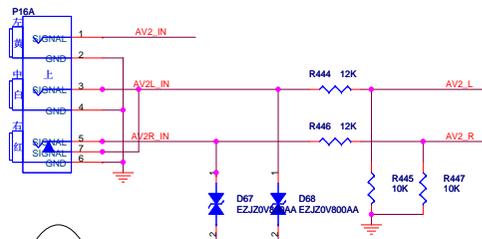
HDMI port 2



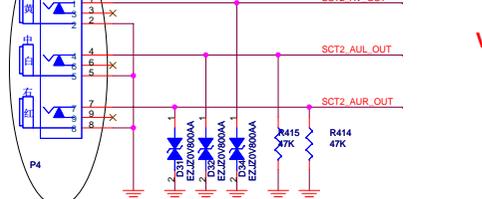
AV1+S-Video1 Input



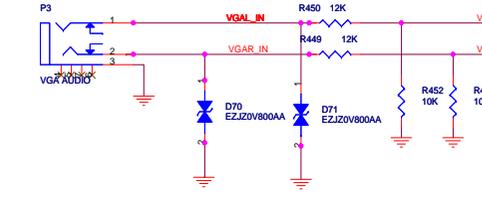
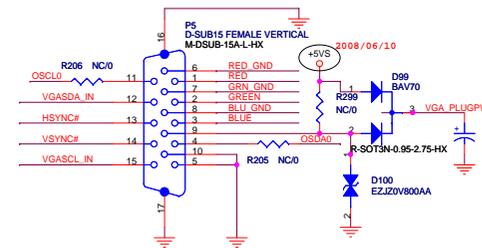
AV2 Input



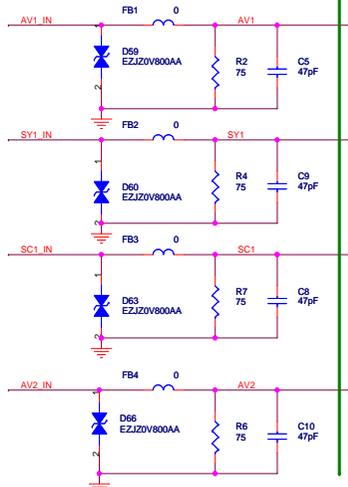
AV OUTPUT



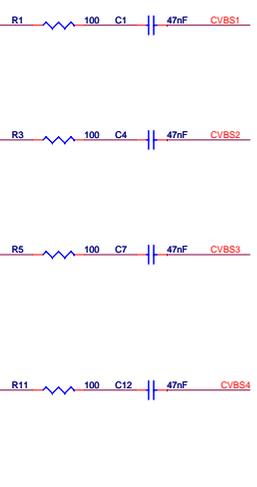
Only for US, EU not stuff



NEAR CONNECTOR



NEAR IC



- CVBS1 <-> CVBS1 3
- CVBS2 <-> CVBS3 3
- CVBS3 <-> CVBS3 3
- CVBS4 <-> CVBS4 3

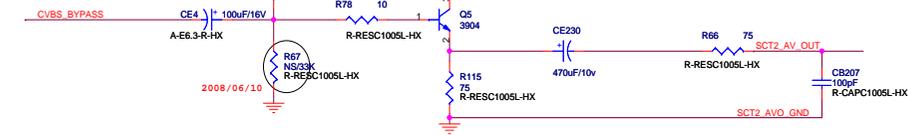
- GND <-> GND 2,3,4,5,6,7,9,10,11,12,13,14

- AV1_L <-> AV1_L 12
- AV1_R <-> AV1_R 12
- AV2_L <-> AV2_L 12
- AV2_R <-> AV2_R 12

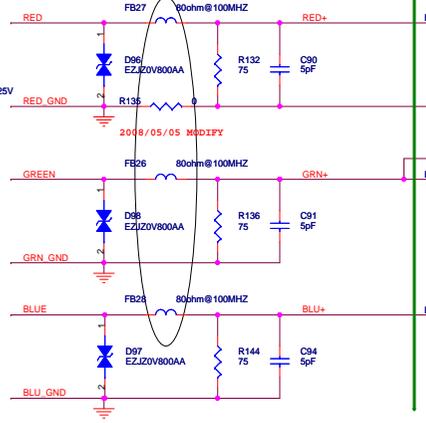
- 5V_M <-> 5V_M 2,3,6,12,13,14

- SCT2_AV_OUT <-> SCT2_AV_OUT 10
- SCT2_AUR_OUT <-> SCT2_AUR_OUT 10,13
- SCT2_AUL_OUT <-> SCT2_AUL_OUT 10,13
- CVBS_BYPASS <-> CVBS_BYPASS 3

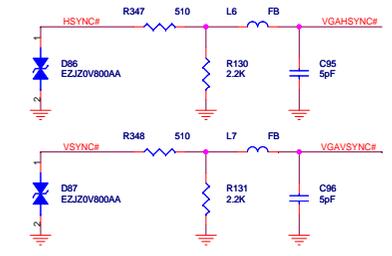
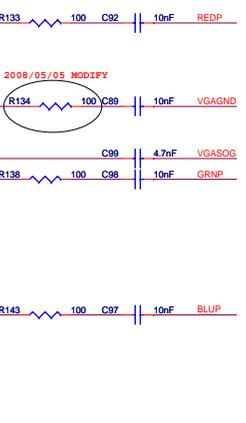
Video output



NEAR CONNECTOR



NEAR IC



- +5V_ON <-> +5V_ON 2
- VGASOG <-> VGASOG 3
- REDP <-> REDP 3
- VGAGND <-> VGAGND 3
- GRNP <-> GRNP 3
- BLUP <-> BLUP 3
- VGASync# <-> VGASync# 3
- VGASync# <-> VGASync# 3

- 5V_M <-> 5V_M 2,3,6,12,13,14

- VGASCL_IN <-> VGASCL 100
- VGASDA_IN <-> VGASDA 100
- VGASCL <-> VGASCL 3
- VGASDA <-> VGASDA 3

- VGA_L <-> VGA_L 12
- VGA_R <-> VGA_R 12
- OSDA0 <-> OSDA0 3,6,11,14
- OSCL0 <-> OSCL0 3,6,11,14

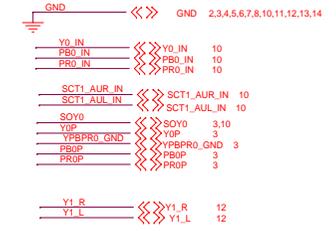
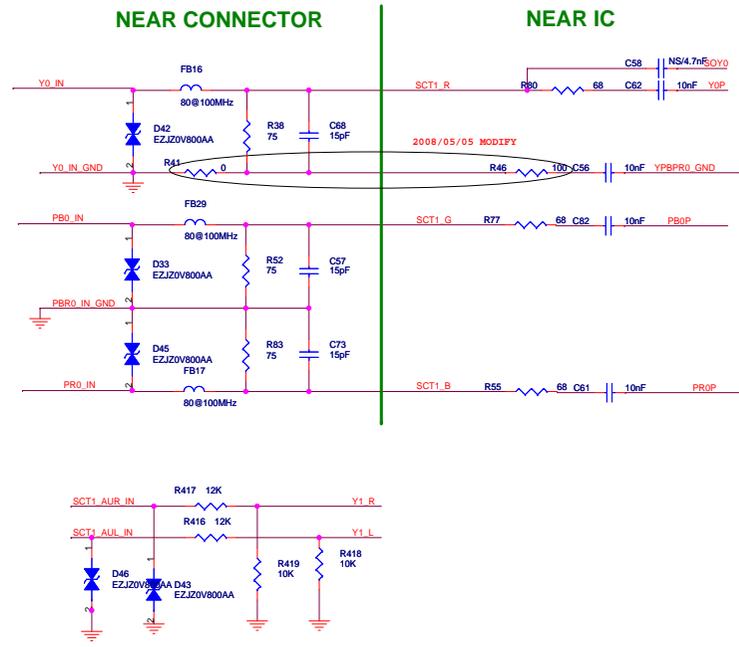
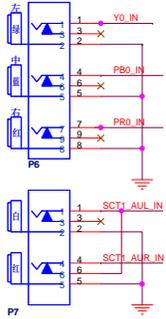
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MediaTek (ShenZhen) Inc.
 Title: CVBS/ S-Video / VGA
 Size: C
 Document Number: HISENSE_MT8222_EU
 Date: 2008/1/25

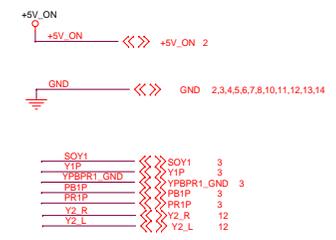
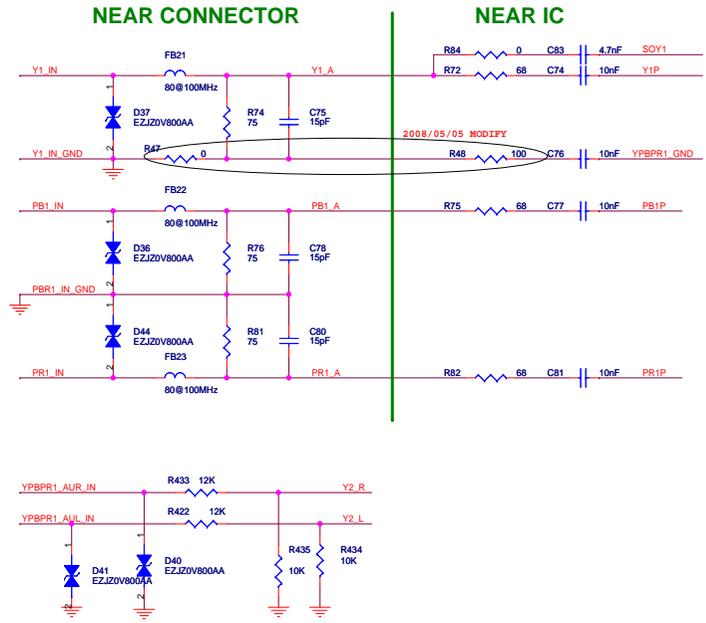
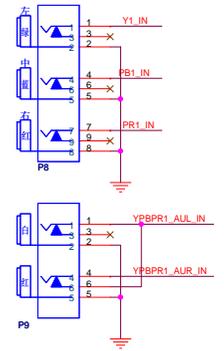
Drawn: Jiu.Ni
 Sheet: 8 of 14

Only for US, EU not stuff

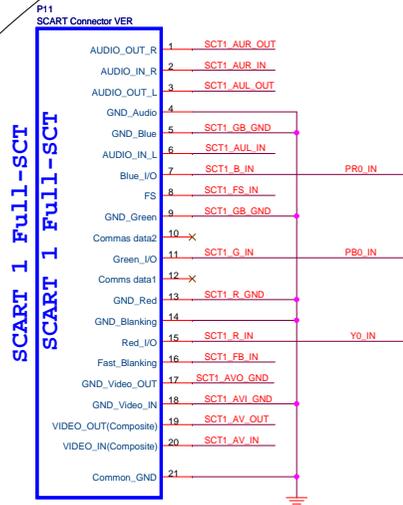
YPbPr0 port



YPbPr1 port

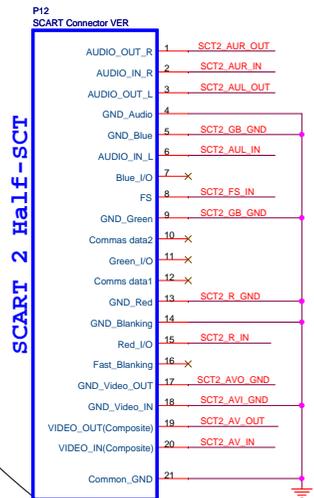
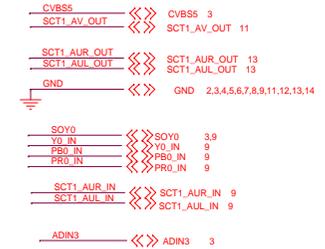
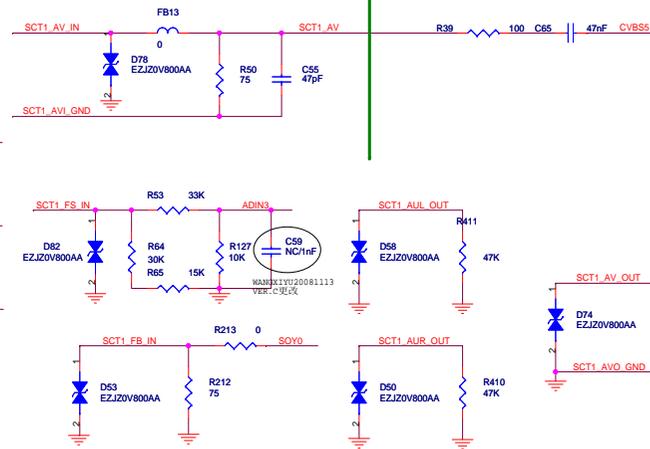


Only for EU, US not stuff



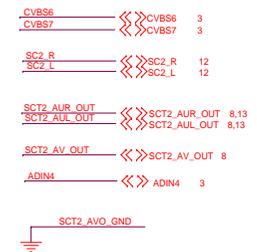
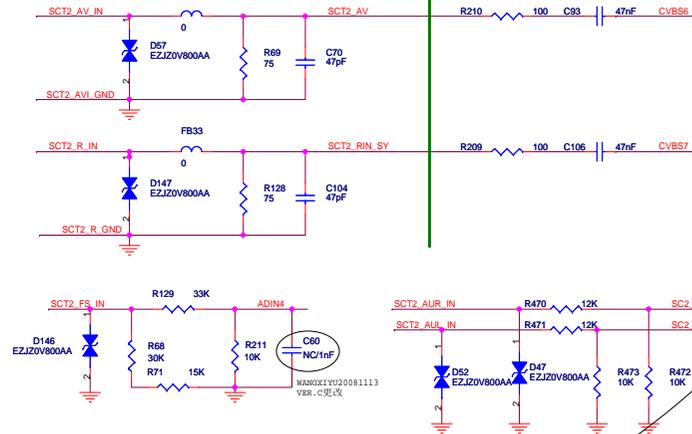
NEAR CONNECTOR

Near switch

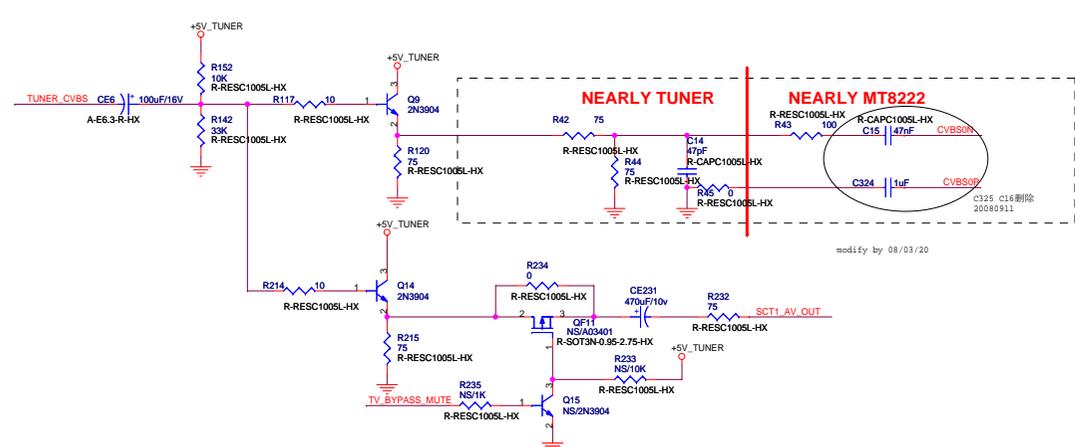
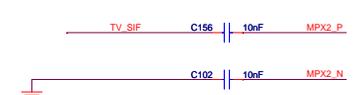
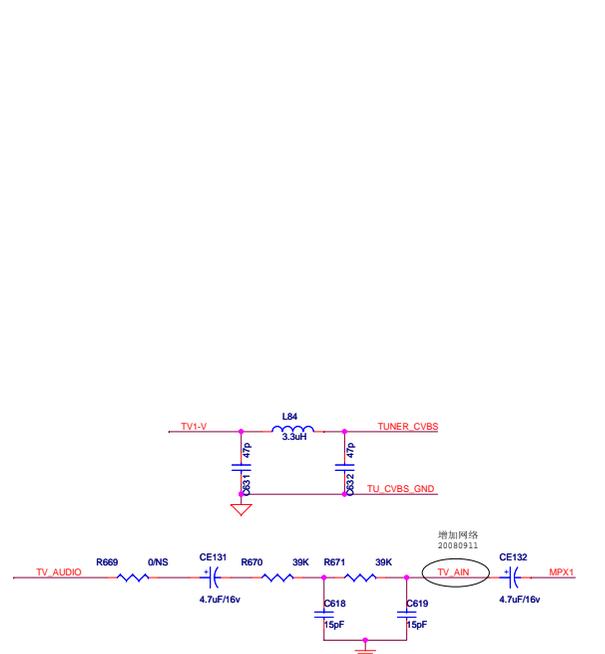
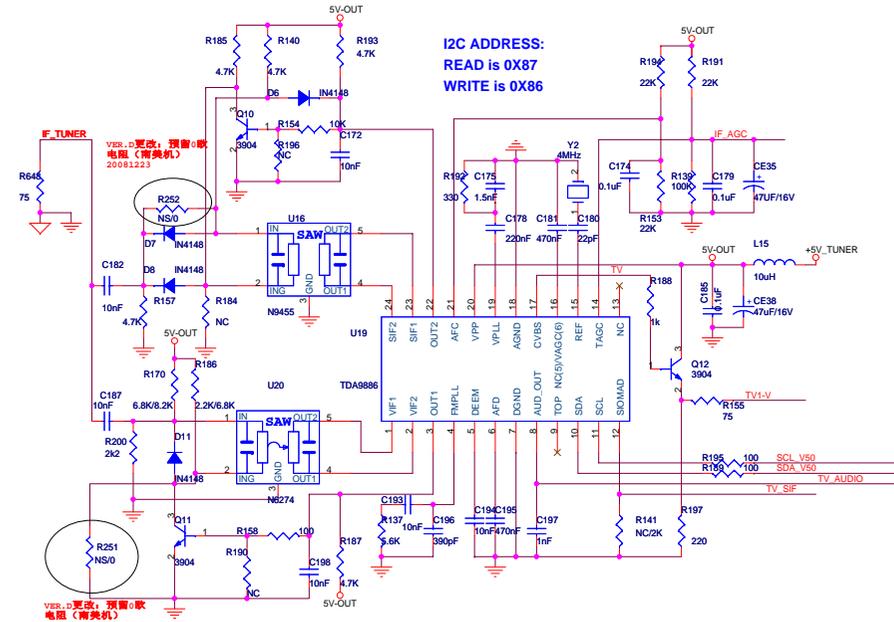
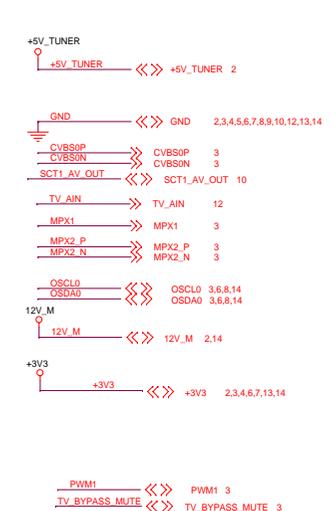
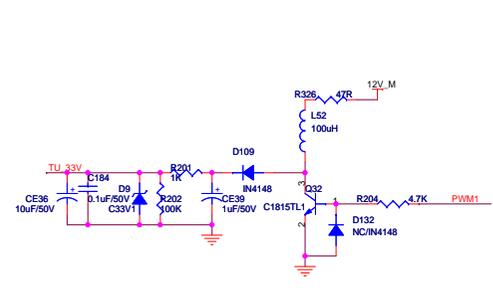
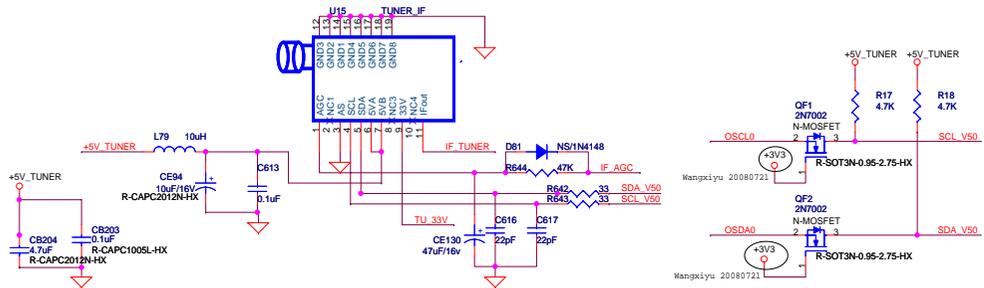


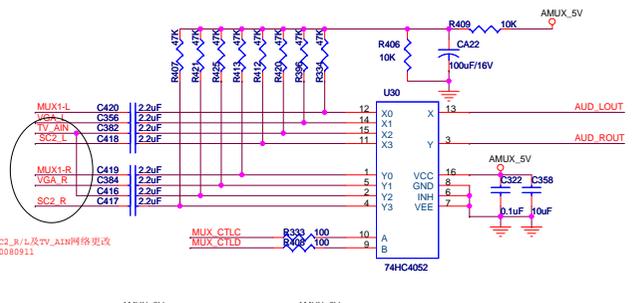
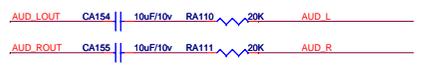
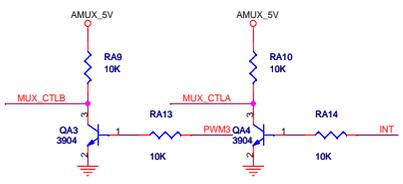
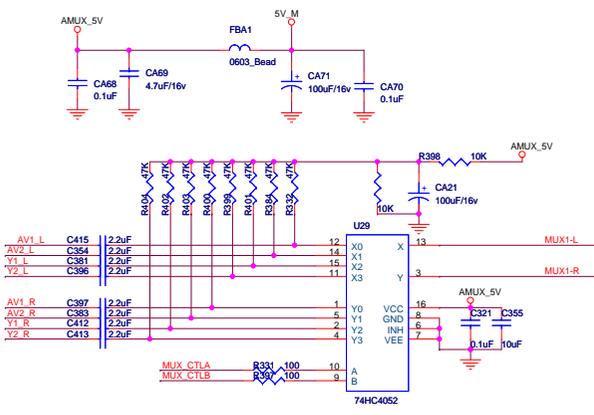
NEAR CONNECTOR

NEAR IC

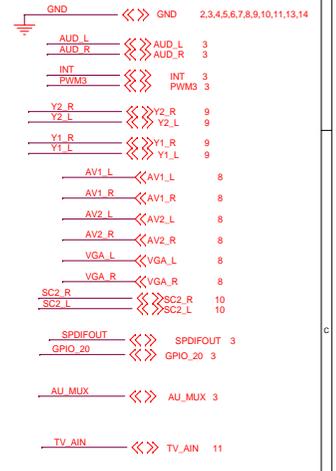
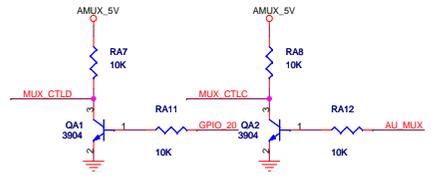


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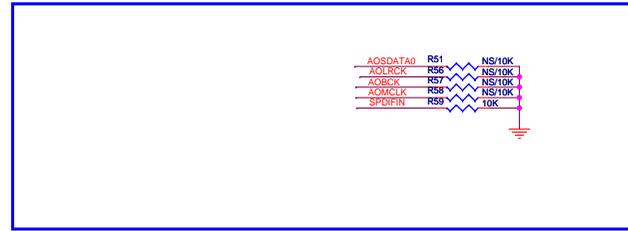
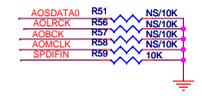
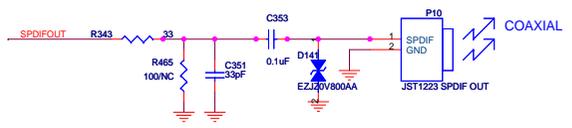




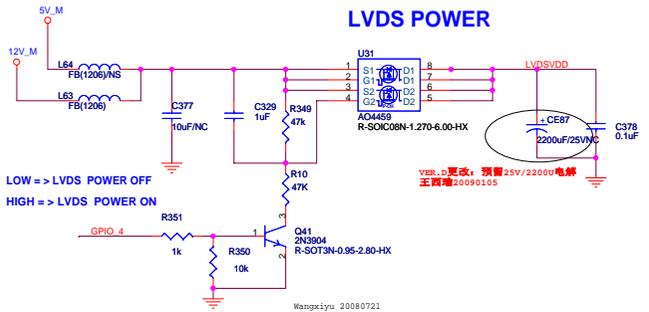
SC2_R/L及TV_AIN网络更改
20080911



PWM3	INT	GPIO_20	AU_MUX	AUDIO OUTPUT
1	1	1	1	AV1 OUT
1	0	1	1	AV2 OUT
0	1	1	1	YPBPR1 OUT
0	0	1	1	YPBPR2 OUT
X	X	1	0	VGA OUT
X	X	0	1	TV AUDIO OUT
X	X	0	0	SCART2 OUT

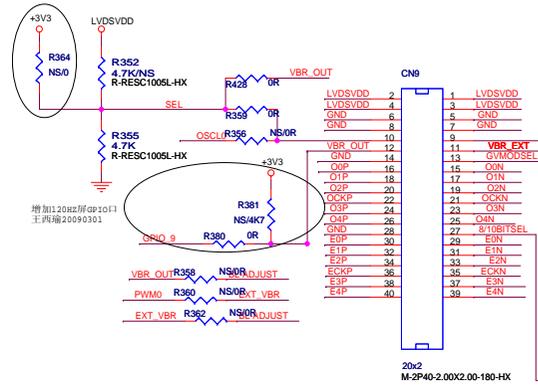


LVDS POWER

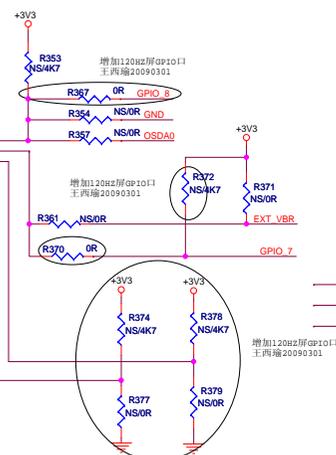


LOW => LVDS POWER OFF
HIGH => LVDS POWER ON

VER.D更改: 预留 25V/2200uF 电解
王西瑞 20090301



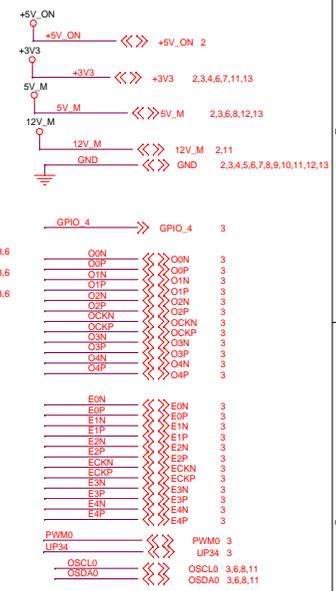
增加120Hz屏@P101
王西瑞 20090301



增加120Hz屏@P101
王西瑞 20090301

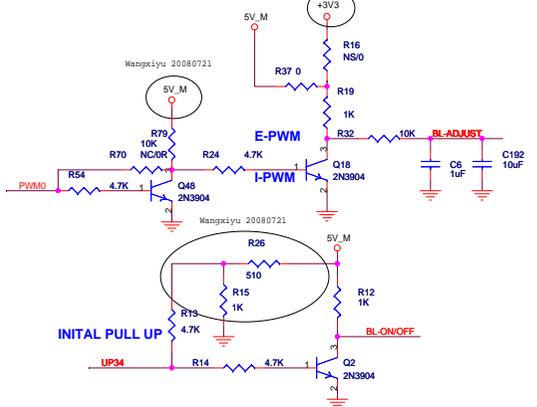
增加120Hz屏@P101
王西瑞 20090301

增加120Hz屏@P101
王西瑞 20090301

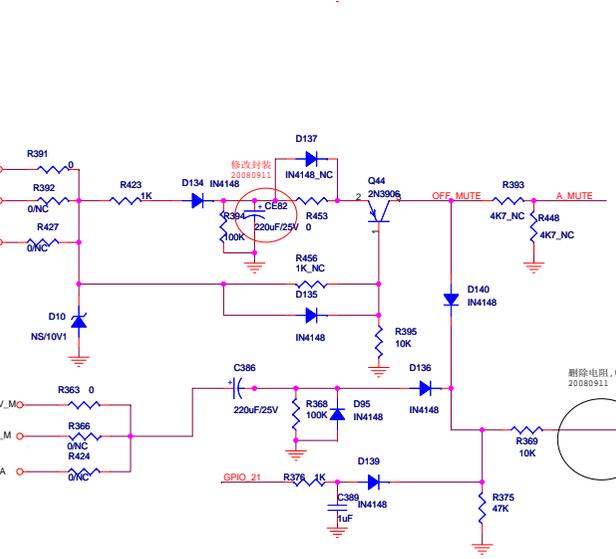


MUTEL: LOW FOR MUTE

Amplifier Gain(dB)	AGAIN1	AGAIN0
20	0	0
26	0	1
32	1	0
36	1	1



INITIAL PULL UP



静音功放左右输入反
20080911

删除电阻, 电容
20080911

