VitalNet Co-Processor Daughter PCB With PTC Capability

ASTS USA Part No.
N12301102

- Operation
- Description

Proprietary Notice

Important Notice

ASTS USA constantly strives to improve our products and keep our customers apprised of changes in technology. Following the recommendations contained in the attached service manual will provide our customers with optimum operational reliability. The data contained herein purports solely to describe the product, and does not create any warranties.

Within the scope of the attached manual, it is impossible to take into account every eventuality that may arise with technical equipment in service. Please consult an ASTS USA local sales representative in the event of any irregularities with our product.

ASTS USA expressly disclaims liability resulting from any improper handling or use of our equipment, even if these instructions contain no specific indication in this respect. We strongly recommend that only approved ASTS USA spare parts are used as replacements.

Revision History

REV.	DATE	NATURE OF REVISION
1	February 2010	Initial release

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1 GENERAL INFORMATION

This document provides a description of the PTC VitalNet Co-Processor PCB that handles Positive Train control (PTC) functionality.

1.1 Abbreviations and Acronyms

The following are abbreviations and acronyms used in this manual along with their associated meanings.

2oo2	Two out of two
ASTS USA	Ansaldo STS USA, Inc. (formerly known as Union Switch & Signal Inc.)
ATP	Automatic Train Protection
CPU	Central Processing Unit
EMC	Electromagnetic compatibility
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
PCB	Printed Circuit Board
PTC	Positive Train Control
SNMP	Simple Network Management Protocol
TMC	Train Management Computer
WCM	Wayside Communications Module
WIU	Wayside Interface Unit
WSM	Wayside Status Message

2 GENERAL DESCRIPTION

The VitalNet Co-Processor Daughter PCB mounts directly on the Microlok II Central Processor Unit (CPU) (ASTS USA part number N17067601) motherboard PCB. The combined assembly is referred to as the MicroLok® II VitalNet™ CPU (ASTS USA part number N17067602). The addition of the Co-Processor daughter PCB enables integrated Positive Train Control (PTC) Wayside Interface Unit (WIU) functionality directly within the ASTS Microlok II interlocking control system. Refer to ASTS USA Service Manual SM 1D1.0028 for information on the motherboard PCB.

2.1 CAPABILITIES

The MicroLok® II VitalNet™ CPU transfers vital interlocking data messages, containing Wayside signal indications, switch positions and hazard indicator statuses, to a radio that forwards it to the carborne ATP equipment of approaching vehicles.

NOTE

Wireless media could be data radio, 802.11x, cell phone, or satellite phone.

2.2 System Functional Description

The Microlok II VitalNet™ CPU monitors the states of the wayside devices and vitally constructs a message that depicts those states. The message is delivered to a Wayside Communications Module (WCM) that chooses the most appropriate media to send the message to a train.

The VitalNet Co-Processor daughter PCB communicates to the Microlok II CPU through a vital communications protocol over the Ansaldo STS G96 bus. The Co-processor utilizes two diverse FPGAs to implement a 2 out of 2 voting architecture, which provides vital reception of Microlok input and output states, and vital generation and transmission of PTC messages to the data radio or back office.

2.2.1 Ethernet Communication

The system contains two independent and isolated Ethernet connections through RJ-45 connectors on the front panel of the N17067602 assembly. The two Ethernet ports may be used simultaneously. The ports are intende for use with the WCM to send and receive messages from the train, and to respond to inquiries from the central office. Additionally, the Ethernet ports are to be used for maintenance functions. The Ethernet ports may be configured as DHCP clients for connection to a WCM or existing IP network; or, may be configured to serve as DHCP hosts for maintenance functions without the need to change Network settings on the maintainer's PC. The VitalNet Co-processor contains an embedded web server interface so that a user can connect a laptop PC to the Ethernet port to configure the device, modify the PTC application settings, upload and download software, and view diagnostic and event data.

2.2.2 Co-Processor Reset Pushbutton

The PTC Reset pushbutton is located below the Ethernet Ports on the faceplate of the MicroLok® II VitalNet™ CPU assembly. This reset pushbutton is used to:

- Authorize vital configuration access requests when pressed less than 3 seconds
- Resets the Co-Processor PCB, when held for more than 3 seconds

The timing of the pushbutton is software configurable.

2.2.3 Co-Processor Jumper Switches

There are two series of DIP Switches on the VitalNet Co-Processor Daughter PCB. Each series of DIP switch contains 10 switches that can be set to either an ON or OFF position. These switches can be used to reset default IP and login passwords on the device. The SW1 switch corresponds to the Altera FPGA device, and SW2 corresponds to the Xilinx FPGA device.

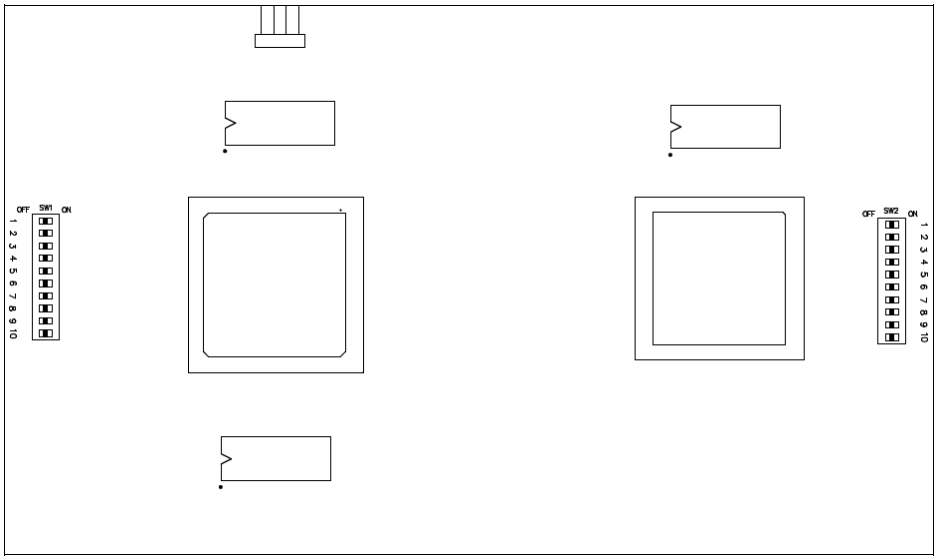

Figure 2-1. Co-Processor Daughter PCB Switches

Table 2-1. Switch SW1 Settings

Switch Reference	Description	Setting
1	Network Configuration	ON = boot using default network configuration and password **OFF = boot using application specific network configuration and password**
2	Factory Use Only	**Must be set to OFF**
3	Maintainer Login Password Reset	ON = boot using default maintainer login password **OFF = boot using specific user-configured maintainer login password**
4 through 10	Factory Use Only	**Must be set to OFF**

Table 2-2. Switch SW2 Settings

Switch Reference	Description	Setting
1 through 10	Factory Use Only	**Must be set to OFF**

2.3 VitalNet Co-Processor PCB Installation

The Microlok II CPU PCB (ASTS USA part number N17067601) can be purchased separately from the MicroLok II VitalNet CPU (ASTS USA part number N17067602). The Microlok II CPU PCB can be upgraded to the Microlok II VitalNet CPU with the addition of an installation kit (ASTS USA part number X17000001), which contains the VitalNet Co-Processor daughter PCB and all of the necessary screws, washers, and lock washers to attach the PCB. See Table 2-3 for the kit's parts list. The Item Numbers in Table 2-3 are keyed to the callouts shown in Figure 2–2.

Refer to for Section 2.3.1 for the installation procedure.

Table 2-3. Co-Processor PCB installation Kit Parts List

Item Number	Description	Part Number
2	J5072970104	Screw, 4-40X1/4 Pan Hd, SS
3	J4751200106	Washer, #4 Flat SS
4	J4751210105	Washer, SST Lock, #4

2.3.1 Installation Procedure

CAUTION

When handling any Microlok II circuit board or board component, observe all electrostatic discharge (ESD) precautions. Improper handling of boards or components may result in damage to static sensitive circuitry.

If the CPU PCB needs to be removed from the Microlok Cardfile, begin with Step 1. If the CPU PCB is already removed from the Microlok cardfile, begin with step 5.

CAUTION

Before removing power from the Microlok II cardfile, make certain that Rail traffic is prohibited from entering the associated Interlocking.

1. Remove Power from the Microlok II Cardfile.
2. Un-screw the two retaining screws on the faceplate of the CPU PCB.
3. Press upward and downward on the respective top and bottom card ejectors on the CPU PCB until the card releases from its position in the cardfile.
4. Remove the CPU PCB from the cardfile by gently sliding the board out along its plastic card guides inside the cardfile.
5. Place the Microlok II CPU PCB on a flat, stable surface with the component side facing upwards.
6. Align the five mating connectors on the Co-Processor PCB with the five mating connectors on the Microlok CPU PCB. Gently press the two PCBs together until the connectors mate tightly with one another.
7. Secure the Co-Processor PCB to the six standoffs (1) using a flat washer (3), lock washer (4), and screw (2). See Figure 2-1.

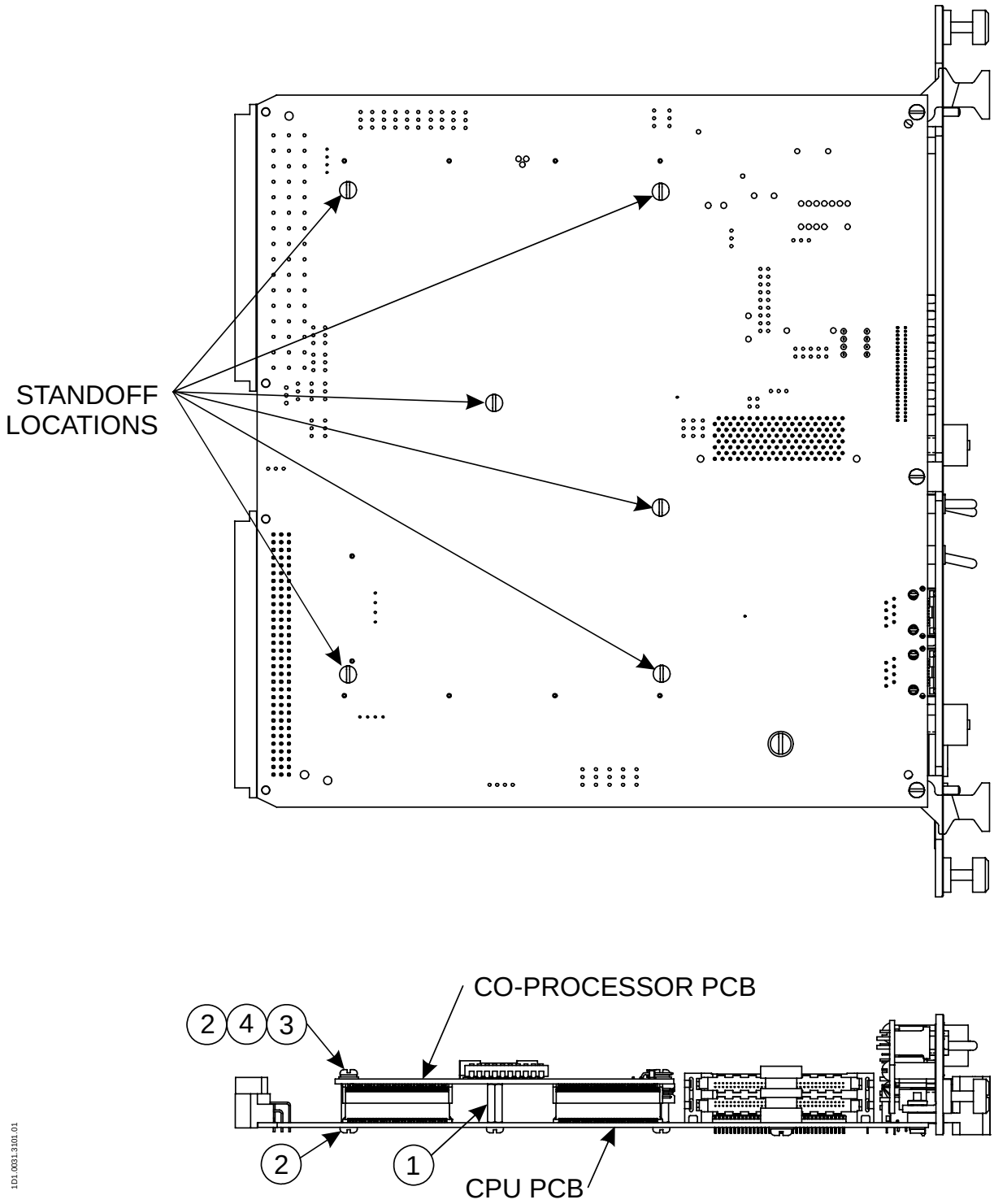

Figure 2–2. PCB Installation

2.3.2 Reinstalling the Microlok CPU PCB

Proceed as follows to reinstall the Microlok CPU PCB into the cardfile.

CAUTION

When installing any Microlok II circuit board into the card file, do not attempt to force the board into the slot. Damage to the circuit board and motherboard 96-pin connectors may result. If resistance is encountered when installing a board, gently rock the board to engage the male and female connectors. If the board still cannot be fully inserted into the card slot, remove the board from the cardfile and attempt to determine the source of the resistance.

1. Insert the CPU with Co-Processor PCB into the plastic card guides inside the Microlok II cardfile.

2. Gently push on the top and bottom corners of the PCB and slide it into the cardfile until the PCB and cardfile connectors are fully engaged.

3. Tighten the two retaining screws on the faceplate of the CPU PCB.

CAUTION

Before applying power to the Microlok II cardfile, make certain that Rail traffic is prohibited from entering the associated Interlocking.

4. Apply +12 VDC battery power to the Microlok II cardfile. Verify that the 5V ON LED on the cardfile power supply board is illuminated.

5. Allow the PCB to re-boot and verify that the Microlok II CPU enters into on-line mode.

NOTE

The PTC indicator light on the faceplate will not become active unless the Microlok Executive 8.60 (or above) software has been loaded onto the unit.

Refer to section “UPLOADING MICROLOK EXECUTIVE” in the Microlok II SM-6800C Service Manual, and update the Executive to the latest revision.

3 SOFTWARE INSTALLATION

After a Co-Processor PCB is installed on a Microlok II CPU PCB, the following software must be loaded onto the unit:

- Microlok Executive revision 8.6 or above
- Location-Specific Microlok Application
- Location-Specific PTC Application
- Location-Specific PTC Configuration

NOTE

Information regarding the building of PTC Applications, and full description of software screens and configuration settings are described in detail in the VitalNet Microlok II PTC Application Logic Programming Guide and Software User Manual SM-1D1.0034.

3.1.1 Updating Microlok Executive Software

Proceed as follows to update the Microlok II executive software:

1. Connect a null-modem RS-232 cable from a laptop PC to the Microlok II CPU RS-232 connection on the faceplate of the CPU.

2. Refer to section “UPLOADING MICROLOK EXECUTIVE” in the Microlok II SM-6800C Service Manual, and update the Executive to revision 8.6 or above.

3. Once the device has finished updating and re-boots, verify that the front panel display indicates that PTC Executive 8.60 (or above) is loaded. The upper four-character display will display “ASTS USA MICROLOK II” in place of the “US&S MICROLOK II”.

4. The PTC indicator light on the faceplate of the CPU should now be active.

3.1.2 Accessing the PTC Co-processor

Proceed as follows to access the PTC Co-processor device:

1. Connect a standard Cat5e Ethernet cable from the network connection on a laptop PC to the RJ-45 connector on front panel of the CPU. Straight-through or crossover cables can be used. The Ethernet ports on the device are configured as DHCP servers by default, and will serve an IP address to the laptop.

NOTE

Third-party PC firewall software or internet browser proxy server settings may prevent connectivity to the device.

If you are having difficulty connecting to the device, verify your IP address and proxy settings, and disable any firewall software.

If you have verified the settings above, and you are still having difficulty connecting, contact your network administrator.

2. Launch any internet browser running on the laptop PC, and type the IP Address, or device name http://myasts, into the address bar on the browser. The factory default IP addresses are as follows:

Table 3-1. Default Device IP Address Settings

Port	IP Address
Port 1	169.254.1.10
Port 2	169.254.2.10

3. Log into the WIU device by entering the device administrator username and password. The default administrator username and password are as follows:

Table 3-2. Default Device Username and Password Settings

Username	Password
admin	admin

4 PTC CONFIGURATION TOOL

The following sections describe basic software functionality required to upgrade the device software and firmware.

4.1 HOME/DEVICE STATUS SCREEN

When the web server on the VitalNet Co-Processor Daughter PCB device is first accessed with an Internet Browser, the home page (see Figure 4–1) will be displayed. If an application is already loaded, the home page shows the status of the devices that are configured within the PTC Application. If no application is loaded, the home page will be automatically forwarded to the Application Builder page

Changes to the configuration cannot be made until a user login name and password is entered. A Login User Name and Password area is located at the top right corner of the page.

1. Click on the “Sign Out” hyperlink located in the top-right corner of the page, and a Log-in Screen will be displayed.

2. On the Log-in screen, type in a valid username and password.

If the username and password combination is valid, the tool will return from the Log-in screen, and the current logged-in user level will be displayed in the top-right corner of the screen next to the user icon. Once logged-in, additional configuration options will be made available within the displayed menu bar, relative to the access level granted to the user.

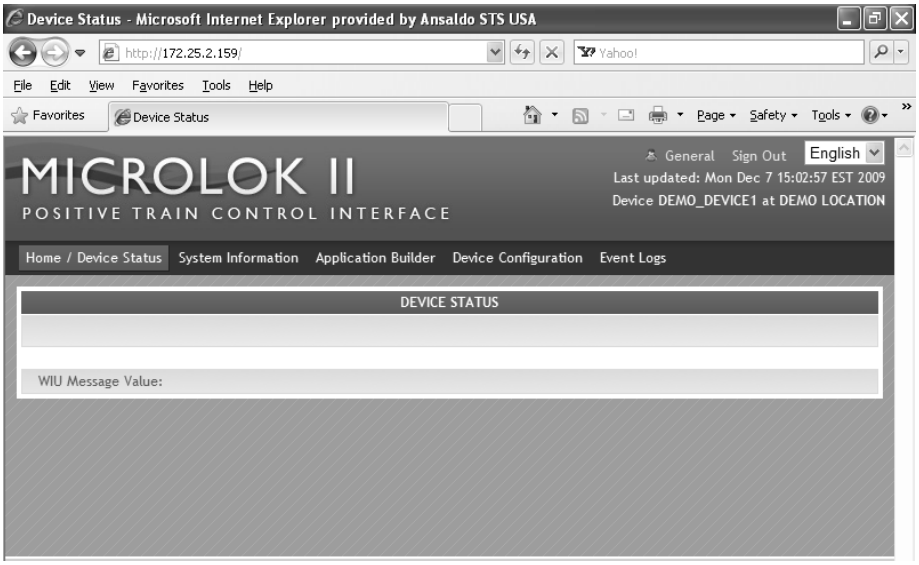

Figure 4–1. Home Page

4.2 SOFTWARE/FIRMWARE UPLOAD

The VitalNet Co-processor CPU will ship from the Ansaldo STS manufacturing facility pre-loaded with the latest PTC Executive software available at the time of release. As updates occur to the PTC WIU Specification due to interoperability requirements, changes in protocol specifications, or new feature releases from ASTS, it will be necessary to update the PTC software and firmware running on the device.

To update the Software / Firmware on the device, perform the following steps after logging in as an administrator:

1. Click on the “Device Configuration” tab located on the main menu bar of the page.

2. Click on the “Firmware Update” link on the Device Configuration sub-menu.

3. Click on the “Browse” button on the Firmware Update page to display a standard file-open window.

4. Browse to the latest update file (update files will be provided only by ASTS, and will have a .tar file extension). Select the file and click OK to return and close the file-open window.

5. Click on the “Update Firmware” button to begin the Firmware Update process. Follow the onscreen instructions to complete the update process.

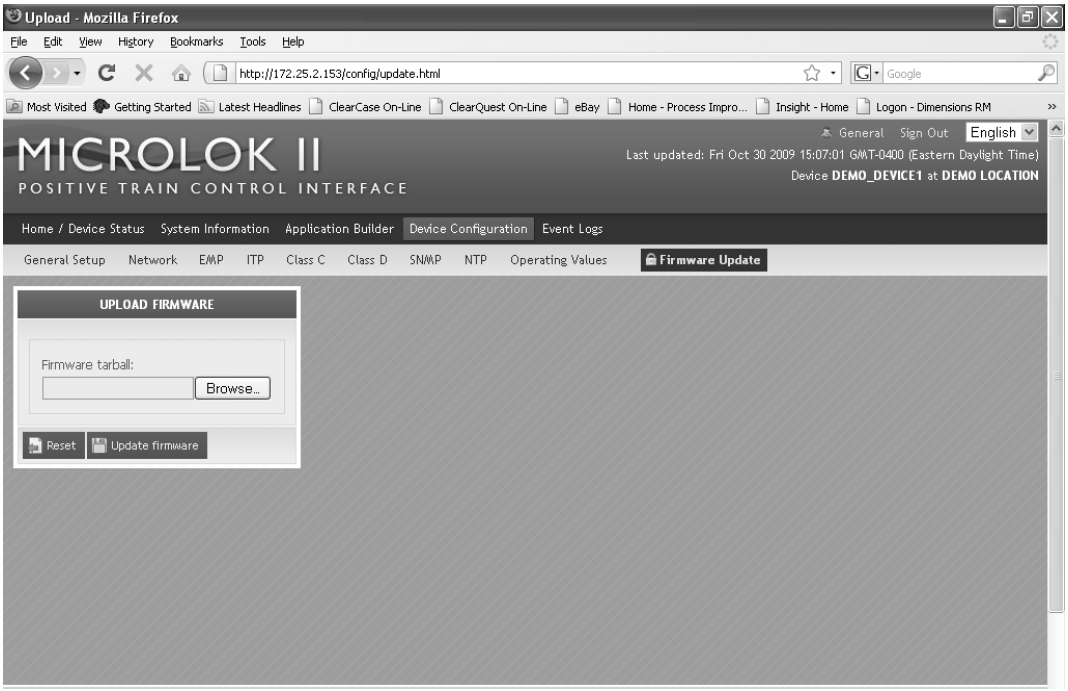

Figure 4–2. Software/Firmware Upload Screen

4.3 SYSTEM INFORMATION SCREEN

The System Information screen provides information about a particular system, including hardware part numbers, serial numbers, Application CRC values, current device time and software and firmware part numbers.

After uploading the latest software and firmware to the device, verify that the version numbers match the version of software uploaded in Section 4.2.

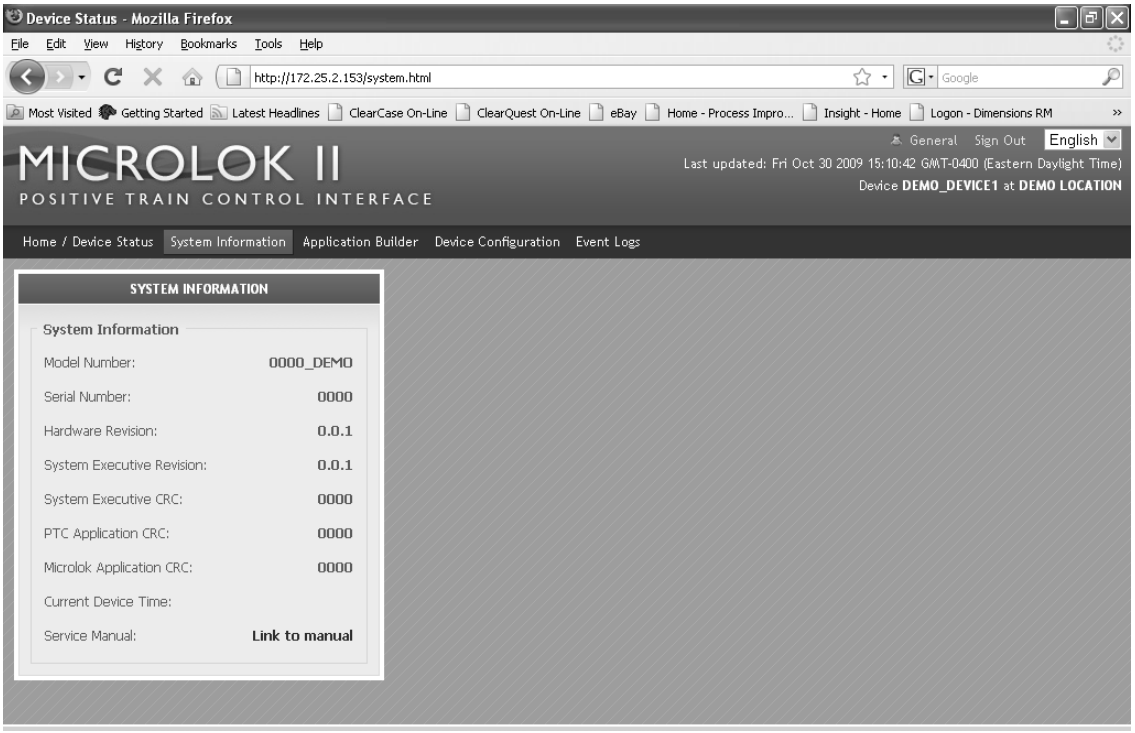

Figure 4–3. System Screen

5 RAIL TEAM AND TECHNICAL SUPPORT

The Rapid Action Information Link Team (RAIL Team) is a group of experienced product and application engineers ready to assist you to resolve any technical issues concerning this product. Contact the RAIL Team in the United States at 1-800-652-7276 or by e-mail at railteam@ansaldo-sts.us.

End of Manual