

INTRODUCTION

The digital integrated circuit has revolutioned the electronics industry. Through the digital IC, designers' dreams are becoming realities. Areas such as pocket calculators, digital computers, and all phases of a heretofore analog world are exploding with more complex, compact, and powerful products than ever before. *But this advance in electronics has not come without a price. The digital integrated circuit has also brought a major headache in maintaining and repairing these products. Fundamental differences between analog and digital circuits and the resulting need for new instrumentation and troubleshooting techniques are responsible for these problems.*

This application note discusses the fundamental differences between discrete analog circuits and those built from digital integrated circuits. An analysis of the failure modes of digital IC's suggests an algorithm for digital troubleshooting. The application of this algorithm and HP's IC TROUBLESHOOTERS (Logic Comparator, Probe, Pulser, and Clip) can significantly increase the efficiency of today's troubleshooter. It is essential that the reader understand the operation of the IC TROUBLESHOOTERS before studying this algorithm. (If not thoroughly familiar, the reader should study Appendices I and II before proceeding.)

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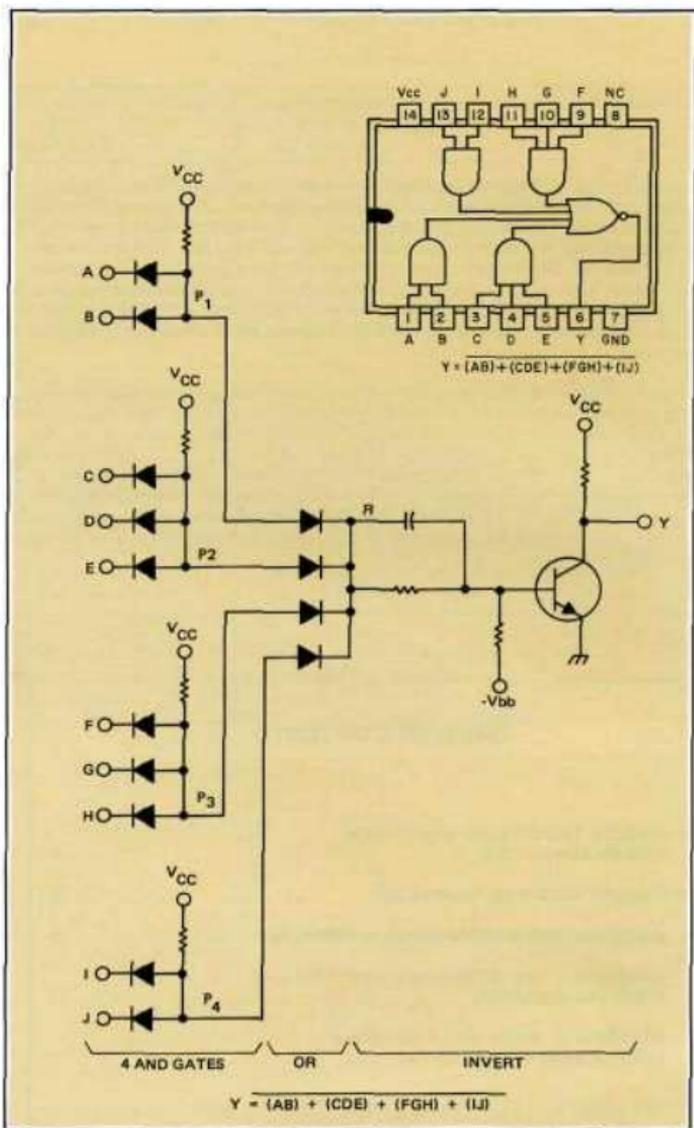


Figure 1. Discrete Vs. Integrated Circuits. Troubleshooting circuits built from discrete components requires verifying relatively simple characteristics such as resistance, capacitance, or turn-on voltages. Today's circuits built from digital IC's require the verification of complex digital waveforms defined by the truth table of the IC.

I. ANALOG TECHNIQUES AND DIGITAL TROUBLESHOOTING

When troubleshooting circuits built from analog components, the task is one of verifying relatively simple characteristics such as resistance, capacitance, or turn-on voltages of components with two or at most three nodes. While the function of the total circuit may be quite complex, each component in that circuit performs a relatively simple task and proper operation is easily verified. In Figure 1, each diode, resistor, capacitor and transistor can be tested using a signal generator and a voltmeter, ohmmeter, diode checker, or oscilloscope—the traditional troubleshooting tools. But when this circuit is built in integrated circuit form, these components are no longer accessible. It now becomes necessary to test the operation of the complete circuit function.

Thus an important difference between discrete circuitry and today's circuits built from digital IC's is in the complexity of the functions performed by these new "components". Unlike the resistor, capacitor, diode or transistor, which must be interconnected to form a circuit function, today's digital IC performs complete, complex functions. Instead of observing simple characteristics, it is now necessary to observe complex digital signals and decide if these signals are correct according to the function the IC is meant to perform.

Verifying proper component operation now requires stimulating and observing many inputs (in Figure 1 there are 10 inputs) while simultaneously observing several outputs (often 2 or 3 and at times as many as 8). Thus another fundamental difference between circuitry built from discrete components and digital IC's is the number of inputs and outputs associated with each component and the need to stimulate and observe these simultaneously.

In addition to the problems of simultaneity of signals and complexity of functions at the component level, the digital IC has introduced a new degree of complexity at the circuit level. Circuits which perplex all but their designer are commonplace. Given enough time, these circuits can be studied and their operation understood, but this is not an affordable luxury for those involved in troubleshooting electronic circuits. Without understanding a circuit's intricate operation, it becomes necessary to have a technique of quickly testing each component rather than attempting to isolate a failure to a particular circuit segment by testing for expected signals.

In order to solve these problems and to make the troubleshooting of digital circuits more efficient, it is necessary to take advantage of the digital nature of the signals involved. Tools and techniques designed to troubleshoot analog circuits do not take advantage of this digital nature and thus are less efficient when used to troubleshoot digital circuits.

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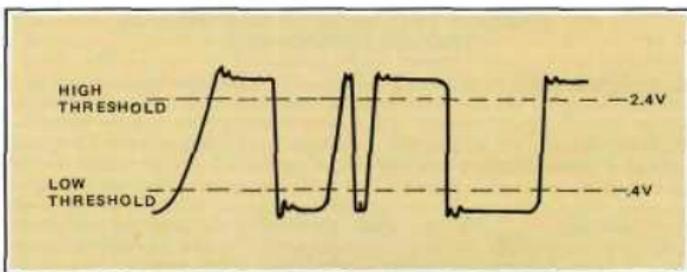


Figure 2. TTL Signal. In the digital world, the relative value of a signal voltage with respect to the threshold voltages determines the operation of the circuit. A signal above the high threshold is in the high state and whether it is 2.8V or 3.0V is unimportant to the operation of the circuit.

Figure 2 shows a typical TTL (Transistor-Transistor-Logic) signal. This might as well be any analog signal when viewed on an oscilloscope. The oscilloscope displays absolute voltage with respect to time, but in the digital world absolute values are unimportant. A digital signal exists in one of two or three states—high, low, and undefined or in-between level—each determined by a threshold voltage. It is the relative value of the signal voltage with respect to these thresholds that determines the state of the digital signal and this digital state determines the operation of the IC, not absolute levels. In Figure 2, if the signal is greater than 2.4 volts, it is a high state and it is unimportant whether the level is 2.8 or 3.0 volts. Similarly for a low state the voltage must be below .4 volts. It is not important what the absolute level is as long as it is below this threshold. Thus when using an oscilloscope, the troubleshooter must over and over again determine if the signal meets the threshold requirement for the desired digital state.

Within a digital logic family, such as TTL, the timing characteristics of each component are well defined. Each gate in the TTL logic family displays a characteristic propagation delay time, rise time, and fall time. The effects of these timing parameters on circuit operation are taken into account by the designer. Once a design has been developed beyond breadboard or prototype stage and is into production, problems due to design have hopefully been corrected. An important characteristic of digital IC's is that when they fail, they fail catastrophically. This means that timing parameters rarely degrade or become marginal. Thus observing on an oscilloscope and making repeated decisions on the validity of timing parameters is time consuming and contributes very little to the troubleshooting process. Once problems due to design are corrected, the fact that pulse activity exists is usually enough indication of proper IC operation without further observation of pulse width, repetition rate, rise time or fall time.

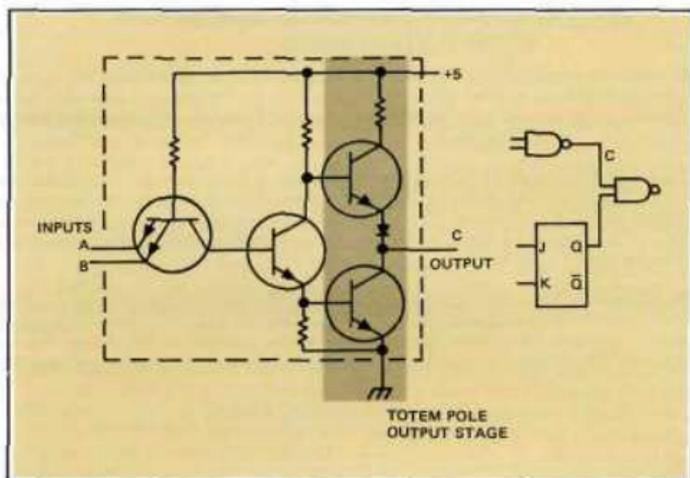


Figure 3. When stimulating a node in circuit, such as C above, it is necessary to override the low impedance totem pole output stage driving that node. When the output is in the low state, it is a saturated transistor to ground. Presently used signal sources are not powerful enough to override this low state.

Figure 3 shows a problem created by the TTL logic family. The output stage of a TTL device is a transistor totem pole. In either the high or low state, it is a low impedance. In the low state it is a saturated transistor to ground. It thus appears as 5–10 ohms to ground. This presents a problem to in-circuit stimulation. A signal source used to inject a pulse at a node which is driven by a TTL output must have sufficient power to override the low impedance output state. Most sources presently used for troubleshooting do not provide this capability. It has been necessary for the troubleshooter to either cut printed circuit traces or pull IC leads in order to stimulate the circuit being tested. Both of these practices are time consuming and lead to unreliable repairs.

Thus the use of the traditional oscilloscope and the traditional signal sources is inefficient. Since the diodes and transistors are packaged in the IC, use of diode checkers is also marginal. These tools are general purpose tools that can be applied to any situation if the troubleshooter has enough time. But with the quantity and complexity of today's electronic circuits, it makes sense to find the most efficient solution to the problem at hand. This suggests using the oscilloscope, diode checkers and voltmeter on analog circuits where they really shine and using instruments that take advantage of the digital nature of signals on the digital circuitry to be repaired.

II. FAILURE MODES OF DIGITAL IC'S

In order to troubleshoot efficiently, it is important to understand the type of failures found in digital circuits. These can be categorized into two main classes—those caused by a failure internal to an IC and those caused by a failure in the circuit external to the IC.

There are four types of failures that can occur internally to an IC. These are (1) an open bond on either an input or output, (2) a short between an input or output and Vcc or ground, (3) a short between two pins (neither of which are Vcc or ground), and (4) a failure in the internal circuitry (often called the steering circuitry) of the IC.

In addition to these four failures internal to an IC, there are four failures that can occur in the circuit external to the IC. These are (1) a short between a node and Vcc or ground, (2) a short between two nodes (neither of which are Vcc or ground), (3) an open signal path, and (4) a failure of an analog component.

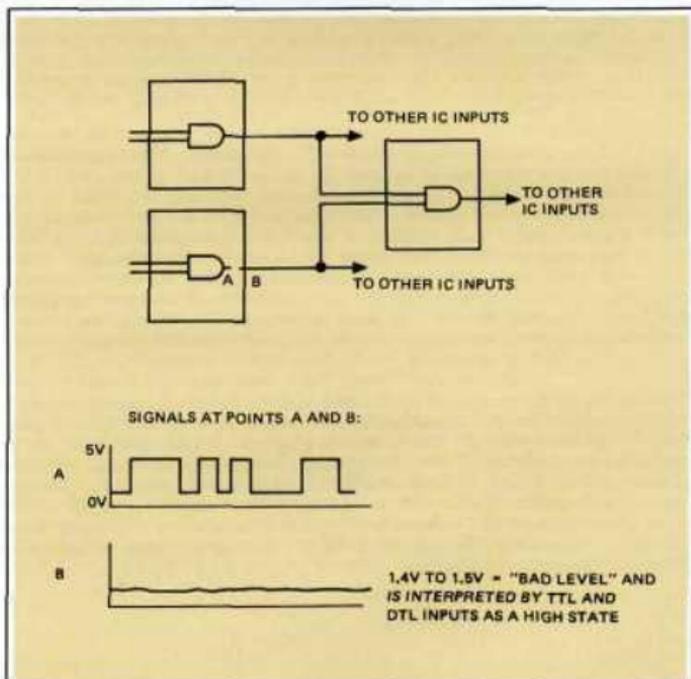


Figure 4. The Effect of an Open Output Bond Upon Circuit Operation. An open output bond allows all inputs driven by that output to float to a "bad level." This level is usually interpreted as a logic high state by the inputs. Thus the inputs driven by an open output bond will respond as though a static logic high signal was applied.

Before discussing how to detect each of these failures we will discuss the effect each has upon circuit operation. The first failure internal to an IC mentioned was an open bond on either an input or output. This failure has a different effect depending upon whether it is an open output bond or an open input bond. In the case of an open output bond (Figure 4), the inputs driven by that output are left to float. In TTL and DTL circuits a floating input rises to approximately 1.4 to 1.5 volts and usually has the same effect on circuit operation as a high logic level. Thus an open output bond will cause all inputs driven by that output to float to a bad level since 1.5 volts is less than the high threshold level of 2.0 volts and greater than the low threshold level of .4 volt. In TTL and DTL, a floating input is interpreted as a high level. Thus the effect will be that these inputs will respond to this bad level as though it were a static high signal.

In the case of an open input bond (Figure 5), we find that the open circuit blocks the signal driving the input from entering the IC chip. The input on the chip is thus allowed to float and will respond as though it were a static high signal. It is important to realize that since the open occurs on the input inside the IC, the digital signal driving this input will be unaffected by the open and will be detectable when looking at the input pin (such as at Point A in Figure 5). The effect will be to block this signal inside the IC and the resulting IC operation will be as though the input were a static high.

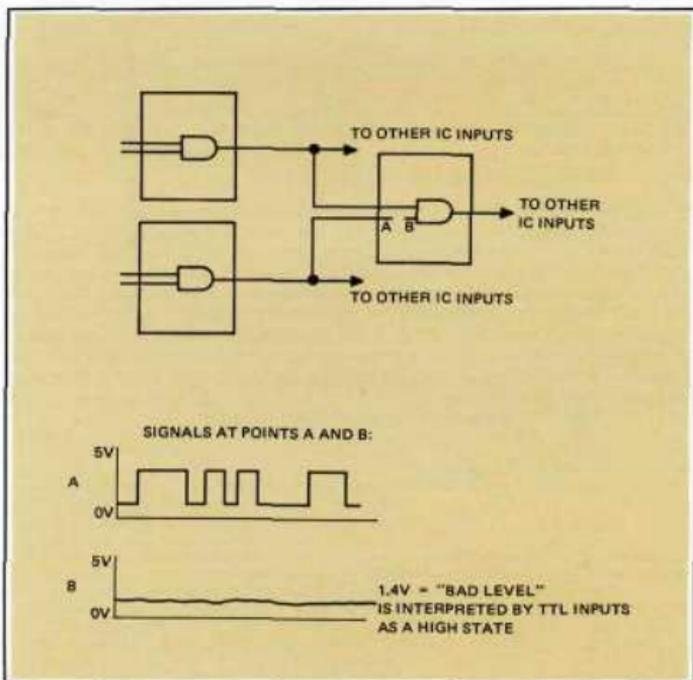


Figure 5. The Effect of an Open Input Bond Upon Circuit Operation. An open bond on an input has the effect of blocking the input signal from reaching the chip and allows the input of the chip to float to a "bad level." Thus even though the signal can be viewed at an external point such as Point A, the input of the chip responds to the "bad level" as though it were a static high level.

A short between an input or output and Vcc or ground has the effect of holding all signal lines connected to that input or output either high (in the case of a short to Vcc) or low (if shorted to ground) (Figure 6). In many cases, this will cause expected signal activity at points beyond the short to disappear and thus this type of failure is catastrophic in terms of circuit operation.

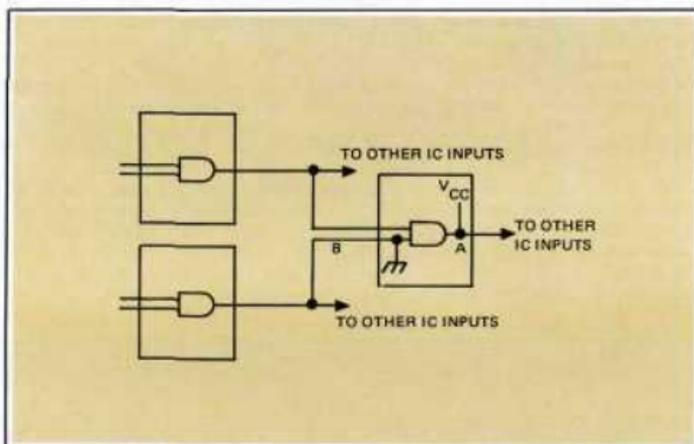


Figure 6. The Effect of a Short Between an Input or Output and Vcc or Gnd. All signal lines connected to Point A are held in the high state. All signal lines connected to Point B are held in the low state.

A short between two pins is not as straightforward to analyze as the short to Vcc or ground. When two pins are shorted the outputs driving those pins oppose each other when one attempts to pull the pins high while the other attempts to pull them low (Figure 7). In this situation the output attempting to go high will supply current through the upper saturated transistor of its totem pole output stage while the output attempting to go low will sink this current through the saturated lower transistor of its totem pole output stage. The net effect is that the short will be pulled to a low state by the saturated transistor to ground. Whenever both outputs attempt to go high simultaneously or to go low simultaneously, the shorted pins will respond properly. But whenever one output attempts to go low the short will be constrained to be low.

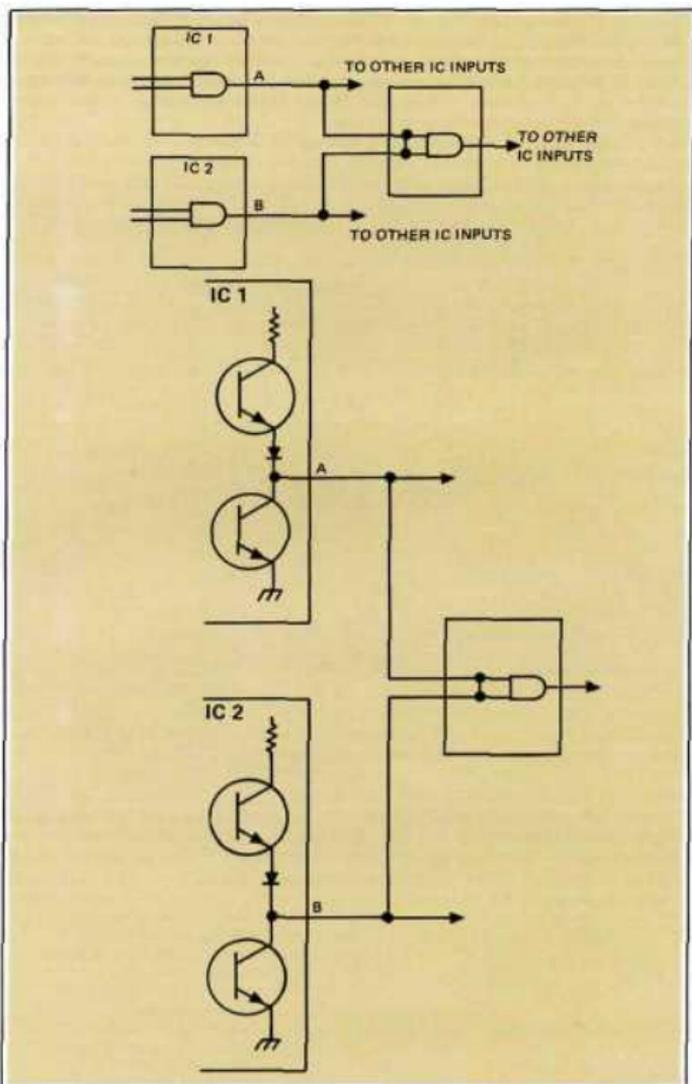


Figure 7. The error effect of a short between two pins occurs when the outputs driving those pins attempt to pull the short to opposite states. In this case, the output attempting to pull the node high will be supplying current while the output attempting to pull the node low is a saturated transistor to ground and will be sinking the current. The saturated transistor to ground will thus pull the node to a low state.

The fourth failure internal to an IC is a failure of the internal (steering circuitry) of the IC (Figure 8). This has the effect of permanently turning on either the upper transistor of the output totem pole thus locking the output in the high state or turning on the lower transistor of the totem pole thus locking the output in the low state. Thus this failure blocks the signal flow and has a catastrophic effect upon circuit operation.

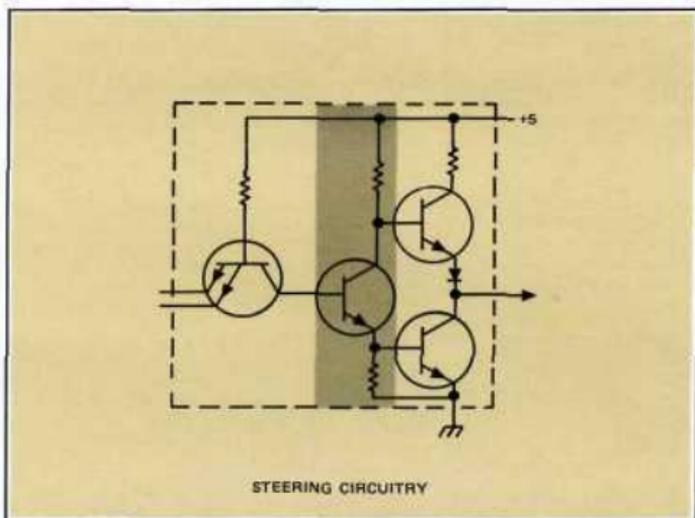


Figure 8. The Effect of a Failure of the Internal Circuitry of the IC Upon Circuit Operation. A failure of the steering circuitry of an IC will either cause the output to be in a static high state or a static low state.

A short between a node and Vcc or ground external to the IC is indistinguishable from a short internal to the IC. Both will cause the signal lines connected to the node to be either always high (for shorts to Vcc) or always low (for shorts to ground). When this type of failure is encountered only a very close physical examination of the circuit will reveal if the failure is external to the IC.

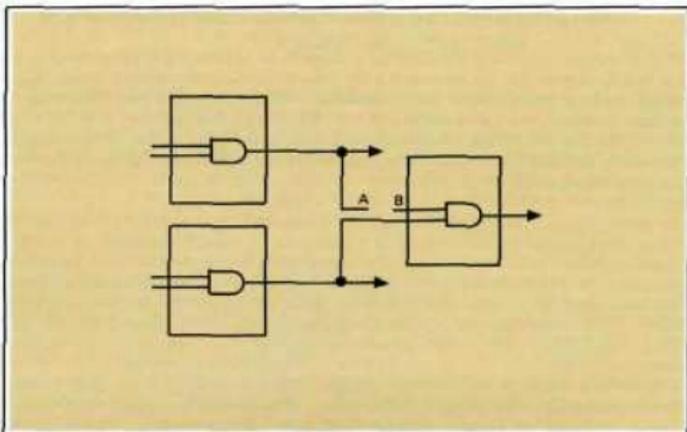


Figure 9. The Effect of an Open in the Circuit External to an IC. All inputs attached to the node at Point A will be driven properly. All inputs to the right of the open (Point B) will be left to float to a "bad level" and will therefore look like a static high state.

An open signal path in the circuit has a similar effect as an open output bond driving the node (Figure 9). All inputs to the right of the open will be allowed to float to a bad level and will thus appear as a static high level in circuit operation. Those inputs to the left of the open will be unaffected by the open and will thus respond as expected.

III. A DIGITAL TROUBLESHOOTING ALGORITHM

The first step in any troubleshooting process is to narrow the malfunctioning area as much as possible by examining the observable characteristics of the failure. This is often called "front panel milking." From the front panel operation (or rather mis-operation) the failure should be localized to as few circuits as possible. At this point it is necessary to narrow further the failure to one suspected circuit by looking for improper key signals between circuits. The Logic Probe can be very effective here.*

In many cases, a signal will completely disappear. By rapidly probing the interconnecting signal paths, a missing signal can be readily detected. Another important failure is the occurrence of a signal on a line that should not have had a signal. The Pulse Memory option for the Logic Probe allows such signal lines to be monitored for single shot pulses or pulse activity over extended periods of time. The occurrence of a signal will be stored and indicated on the Pulse Memory's LED.

Dependence upon a well-written service manual is the key to this phase of troubleshooting. Isolating a failure to a single circuit requires knowledge of the *instrument or system and its operating characteristics*. A well written manual will indicate key signals to be observed. The Logic Probe will provide a rapid means of observing the presence of these signals.

Once a failure has been isolated to a single circuit, the IC Troubleshooters (Logic Probe, Pulser, Clip, Comparator) can be used to observe the effect of the failure on circuit operation and to locate the failure to its cause (either an IC or a fault in the circuit external to the IC). The technique described below for applying the IC Troubleshooters to this task allows significant (4 to 1) improvements over existing troubleshooting techniques by providing a digital solution to the digital troubleshooting problem.

With today's circuits containing as many as several hundred IC's, the problem of troubleshooting becomes one of physically isolating the trouble to the 2 or 3 IC's affected by the failure. A majority of today's troubleshooting time is spent looking at signals which are good and determining that they are good. This is time not spent solving the problem but rather time spent getting to the problem! The Logic Comparator offers the opportunity to reduce drastically this time and quickly to isolate the failure to only a few nodes out of the hundreds that exist on a digital circuit thus allowing more time and talent to be spent analyzing the trouble.

The first step in the troubleshooting algorithm (Figure 10) is to use the Logic Comparator to test all *testable* IC's (see Appendix II for testable IC's) in the circuit or portion of the circuit which is suspected of failing and to note the IC's and pins that the Comparator indicates as failing.** This will rapidly focus attention on the physical areas of the circuit which are malfunctioning. Experience shows that this operation will require approximately 30 seconds per IC.

* It is essential that the reader understand the operation of the Logic Probe, Clip, Pulser, and Comparator; if not thoroughly familiar, the reader should study Appendix I before proceeding.

**Often, the sensitive Logic Comparator indicates a failure because its clip is not making good contact especially when the IC's have been sprayed with a sealer. Thus before deciding that a node definitely does not compare, squeeze the clip's jaws tightly and apply a slight twisting motion.



STEP 1. Test all IC's using the Logic Comparator or Logic Probe, Pulser and Clip and note the failing nodes.



STEP 3. Test for a short to Vcc or GND using the Logic Pulser and Probe. By simultaneously probing and pulsing the bad node a short to Vcc or GND can be detected since the Pulser is unable to inject a pulse into such a short.

Steps 2 thru 5 should be repeated for each failing node noted in step 1.



STEP 4. Test for a short between two nodes using the Logic Probe and Pulser or an ohmmeter.



STEP 2. Test for an open output bond driving the failing node using the Logic Probe. If an open output bond is indicated, replace the IC driving the failing node.



STEP 5. If the failure is not found in steps 2 thru 4 then the failure is either an open input bond or a failure of the internal circuitry of the IC driving the failing node. In either case the IC driving the failing node should be replaced.

Figure 10. Digital Troubleshooting Algorithm. After Step 1, the mapping step, the LOGIC PROBE, and PULSER are used to eliminate systematically the causes of IC failures discussed in Chapter III. In Step 5 the cause is determined by induction from the results of Steps 2 through 4.

For those IC's that are not testable with the Logic Comparator or for which a reference card does not exist, the Logic Probe, Pulser, and Clip can be used to verify proper IC operation. The Logic Probe can be used to observe the signal activity on inputs and to view the resulting output signals. From this information, a decision can be made as to the proper operation of the IC. For example, if a clock signal is occurring on a decade counter and the enabling inputs (usually reset lines) are in the enabled state then the output should be counting. The Logic Probe will allow the clock and enabling inputs to be observed, and, if pulse activity is indicated on the outputs, then the IC can be assumed to be operating properly. As stated before, usually it is not necessary to see the actual timing of the output signals since IC's fail catastrophically. The occurrence of pulse activity is often enough indication of proper operation.

When more detailed study is desired or when input signal activity is missing, the Logic Pulser can be used to inject input signals and the Logic Clip or Probe used to monitor the response. This technique is especially good when testing digital gates and other combinatorial devices. The Logic Pulser can be used to change the inputs to go to a state which will cause a change in the output state. For example, a three-input NAND gate which has high, low, low inputs will have a high output. By pulsing the two low inputs high using the Logic Pulser (and the Multi-pin Stimulus Kit, if necessary) the output will pulse low and can be detected by the Logic Probe. This then indicates that the IC is operating properly. The Logic Pulser is also valuable for replacing the clock in digital circuit thus allowing the circuit to be single-stepped while the Logic Probe and Clip are used to observe the changes in circuit's state.

This first step might be called the "mapping" step since the effect is to map out the problem areas for further investigation. It is important to do a complete "mapping" of the circuit before proceeding to analyze each of the indicated failures. Prematurely studying a fault can result in overlooking of faults which cause multiple failures such as shorts between two nodes. This then often leads to the needless replacement of a good IC and much wasted time. With a complete trouble-area "map" we can begin to determine the type and cause of the failures. We do this by systematically eliminating the possible failures of digital circuits discussed above.

The first failure to test for is an open bond in the IC driving the failed node. The Logic Probe provides a quick and accurate test for this failure. If the output bond is open, then the node will float to a bad level. By probing the node, the Logic Probe will quickly indicate a bad level. If a bad level is indicated then the IC driving the node should be replaced and retested with the Logic Comparator.

If the node is not a bad level then a test for a short to Vcc or ground should be made next. This can be done easily using the Logic Pulser and Probe. While the Logic Pulser is powerful enough to override even a low impedance TTL output it is not powerful enough to effect a change in state on a Vcc or ground bus. Thus if the Logic Pulser is used to inject a pulse while the Logic Probe is used simultaneously on the same node to observe the pulse, a short to Vcc or ground can be detected. The occurrence of a pulse indicates that the node is not shorted, and the absence of a pulse indicates the node is shorted to Vcc (if it is a high) or ground (if it is a low).

If the node is shorted to Vcc or ground there are two possible causes. The first is a short in the circuit external to the IC's and the other is a short internal to one of the IC's attached to the node. The external short should be detected by an examination of the circuit. If no external short is found then the cause is equally likely to be any one of the IC's attached to the node. The only suggestion that can be made (based upon experience) is to first replace the IC driving the node and if that does not solve the problem try each of the other IC's individually until the short is eliminated. (It might be noted that on occasion analog components such as resistors or capacitors attached to the node have shorted.)

If the node is not shorted to Vcc or ground nor is it an open output bond then we should look for a short between two nodes. This can be done in one of two ways. First the Logic Pulser can be used to pulse the failing node being studied and the Logic Probe can be used to observe each of the remaining failing nodes. If a short exists between the node being studied and one of the other failing nodes, then the Pulser will cause the node being probed to change state (i.e., the Probe will detect a pulse). To ensure that a short exists, the Probe and Pulser should be reversed and the test made again. If a pulse is again detected then a short is definitely indicated. As a further test or as another way of testing for a short between two nodes, the circuit can be removed from the instrument or system and an ohmmeter can be used to measure the impedance between the two failing nodes. A short between them will be easily detected.

If the failure is a short then there are two possible causes. The most likely is a problem in the circuit external to the IC's. This can be detected by physically examining the circuit and repairing any solder bridges or loose wire shorts found. Only if the two nodes which are shorted are common to one IC can the failure be internal to that IC. If after examining the circuit no short can be found external to the IC, then the IC should be replaced.

If the failure is not a short between two nodes then there are only two possibilities left. They are that the failure is an open input bond or a failure of the internal circuitry of the IC that the Comparator indicates has failed. In either case, this IC should now be replaced. Thus, by systematically eliminating the IC failures, the cause can be located.

An important step at any point where an IC is replaced is the retesting of the circuit with the Logic Comparator. If the Comparator again indicates a failure, then more study of the problem must be made with the knowledge that the failure is not in the IC that has just been replaced.

There is one type of failure that was not discussed in the algorithm, and that is an open signal path in the circuit external to the IC (Figure 11). This type of failure will not be indicated by the Logic Comparator and will therefore not be shown on the trouble-area map. If after using the Logic Comparator to test all the IC's, no nodes are indicated as failing, or, if after finding the cause of the failures indicated by the Logic Comparator, the circuit is still malfunctioning, then an open signal path can be suspected.

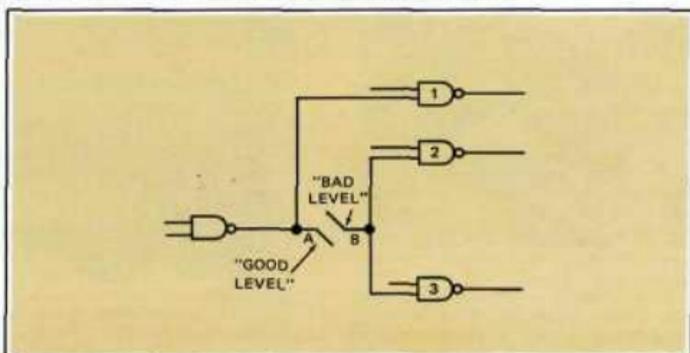


Figure 11. The Effect of an Open Signal Path External to the IC's. The open causes Point B to float to a bad level while Point A is driven by proper TTL or DTL signal levels. Starting at the input of gate 3 or 4 and proceeding back toward gate 1, the exact location of the open can be determined using the Logic Probe.

The Logic Probe provides a rapid means of not only detecting but also physically locating the open. Since an open signal path allows the input to the "right" of the open to float to a bad level, the Logic Probe can be used to test the input of each IC for a bad level. Once an input floating at a bad level is detected, the Logic Probe can be used to follow the circuit back from the input looking for the open. This can be done because the circuit to the "left" of the open will be a good logic level (either high, low, or pulsing) while the circuit to the right will be a bad level. Thus probing back along the signal path will indicate a bad level until the open is passed. Thus the Probe can be used to locate precisely the open. The open can then be repaired and the circuit tested.

This systematic elimination of possible failures in digital circuits coupled with the digital IC Troubleshooters will ensure a rapid and accurate repair. Because the IC Troubleshooters provide a digital solution to the digital problem, improvements in troubleshooting time of at least 4 to 1 are easily achieved.

APPENDIX I. THE IC TROUBLESHOOTERS— A DIGITAL SOLUTION

The LOGIC PROBE is a digital state (highs and lows) indicator which provides at the user's fingertips an indication of a high level, low level, or bad level signal. Internal threshold detectors determine if the signal being probed is above the high threshold level (see Figure A1), below the low threshold level, or in-between these two. A lamp indicator then glows brightly for a high level, goes off for a low level, and glows dimly for a signal that is between the two thresholds.

Since it is necessary to observe dynamic signal activity as well as the static levels described above, the LOGIC PROBE also has pulse stretching circuitry which detects pulses as narrow as 10 ns and stretches them to give a .1 sec blink of the lamp indicator. Thus if a low signal pulses high, the LOGIC PROBE will blink "ON" and if a high signal pulses low, it will blink "OFF." When the PULSE MEMORY OPTION is used with the LOGIC PROBE, monitoring of a signal line for single shot or low frequency pulses over extended periods of time is possible. An L.E.D. in the *Pulse Memory* will light upon the occurrence of a pulse and will remain on until reset by the user.

In addition to single shot pulses, the LOGIC PROBE will also indicate pulse trains of frequencies up to 50 MHz. It does this by blinking the lamp indicator at a constant 10 Hz rate.

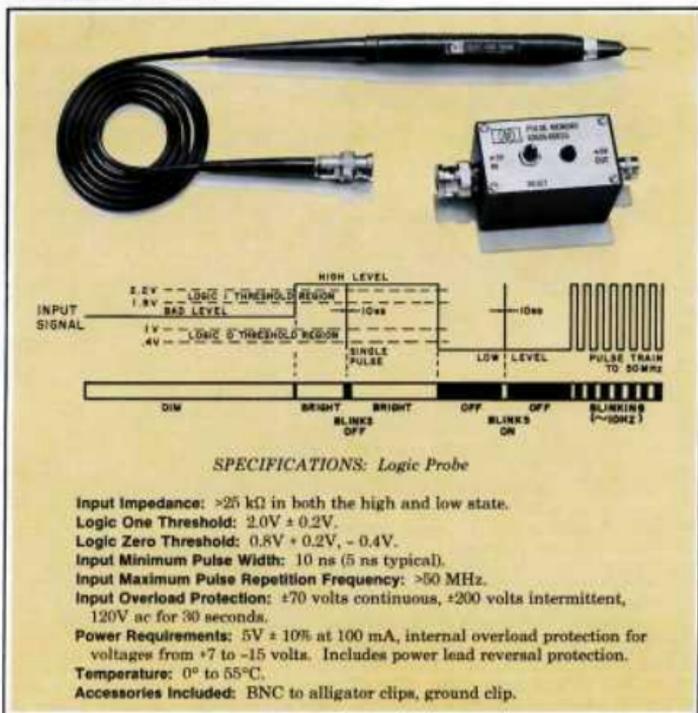


Figure A1. 10525T Logic Probe.

Thus the LOGIC PROBE allows the user to view static signals, single shot pulses, and pulse trains at his finger tip. Automatic threshold detection eliminates the need to determine repeatedly if a signal is above or below the threshold. The response of the lamp indicator is so intuitively related to the actual signal activity that interpretation is rapid and simple.

The LOGIC CLIP is another digital state indicator (Figure A2). It allows up to 16 signals on a single IC to be observed simultaneously. The LOGIC CLIP has a single threshold level. If a signal on a given IC pin is above this level, an LED in the CLIP is turned on corresponding to that pin. If the signal is below this level the LED is turned off. Thanks to internal power seeking circuitry, the LOGIC CLIP cannot be attached improperly. Regardless of how it is clipped onto the IC, it will display the desired signal.

The LOGIC CLIP differs from the LOGIC PROBE in two important ways. First, it has a single threshold as opposed to the two threshold in the LOGIC PROBE and will therefore not indicate a bad level. It will respond to a bad level signal in the same way a TTL or DTL gate will, as a logic high state. Secondly the LOGIC CLIP does not have pulse stretching circuitry. In order to view high frequency or single shot narrow pulses, the LOGIC PROBE should be used.

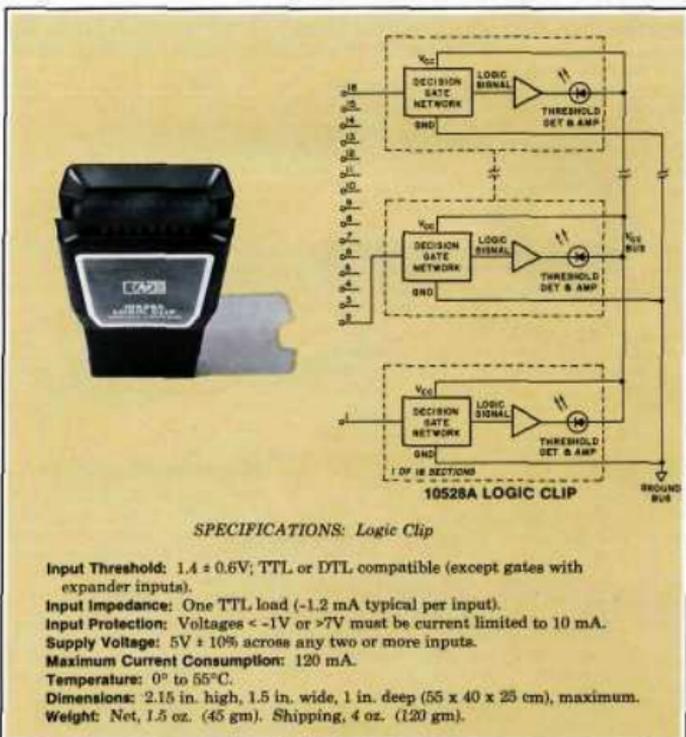


Figure A2. 10528A Logic Clip. With the Logic Clip, up to 16 signals on a given IC can be observed simultaneously. Internal power seeking circuitry allows the clip to be attached in any orientation and makes its operation completely portable.

The ability to view signal activity on several pins simultaneously is a tremendous time saver. Consider the problem of testing a decade counter (e.g., 7490). It is necessary to view at least one input and four outputs simultaneously to determine if this device is operating properly. With the LOGIC CLIP this is no problem.

The LOGIC PROBE and CLIP provide a response mode of operation to the user that is optimized to digital signals. But the mainstay of all troubleshooting is stimulus-response testing. It is necessary to apply a signal and observe the response to determine if the device is operating properly. As was pointed out previously, this is very difficult to do in TTL circuits.

The LOGIC PULSER provides the solution in an easy to use probe package (Figure A3). The LOGIC PULSER injects into the circuit a single 300 ns wide pulse of proper amplitude and polarity each time its button is pushed. If the node was low, it will be pulsed high and if it was high it will be pulsed low without the need to readjust the PULSER. The PULSER is capable of sourcing or sinking .75A for the 300 ns pulse width to ensure that the node is pulsed. The narrow width (300 ns) will not damage the IC's being pulsed.

Thus it now becomes possible to jump rapidly from point to point in the circuit applying pulses and observing the responses. Together the LOGIC PULSER, LOGIC PROBE and LOGIC CLIP provide total in-circuit stimulus response testing for all TTL families, DTL, and other 5 volt logic.



Figure A3. 10526T Logic Pulser. The Logic Pulser provides a solution to the in-circuit stimulus problem of TTL and DTL circuits. Nodes are automatically pulsed from their current digital state to the opposite state for 300 ns with the press of a finger.

While stimulus-response testing is the mainstay of electronic troubleshooting, the digital nature of the signals of the circuit being tested allows for an even faster means of verifying proper component operation. It is component comparison testing. By stimulating a known good device with the same signals as used to stimulate the device under test and comparing the response of the two components, one can verify that the device under test is operating properly. This is exactly what the 10529A LOGIC COMPARATOR does. For the TTL and DTL logic families, the COMPARATOR steals the input signals stimulating the device under test to stimulate simultaneously a known good device. Any difference in their response is indicated by an "ON" LED corresponding to the output which failed the comparison.

The 10529A LOGIC COMPARATOR has pulse stretching circuitry which allows dynamic, single shot or intermittent errors to be detected and displayed as well as static errors. Errors as short as 200 ns are detected and displayed as a .1 sec blink on the LED display. This means the most difficult type of error possible, intermittent failures, will be easily detected and displayed.

The COMPARATOR removes the burden of analyzing long, complex digital signals from the troubleshooter by automatically determining if the signal is a good "high" or "low" level and if that level is correct according to the expected truth table of the circuit being tested. Thus, the LOGIC COMPARATOR vastly reduces troubleshooting time. (See Appendix II for more details on the LOGIC COMPARATOR.)



10529A Logic Comparator.

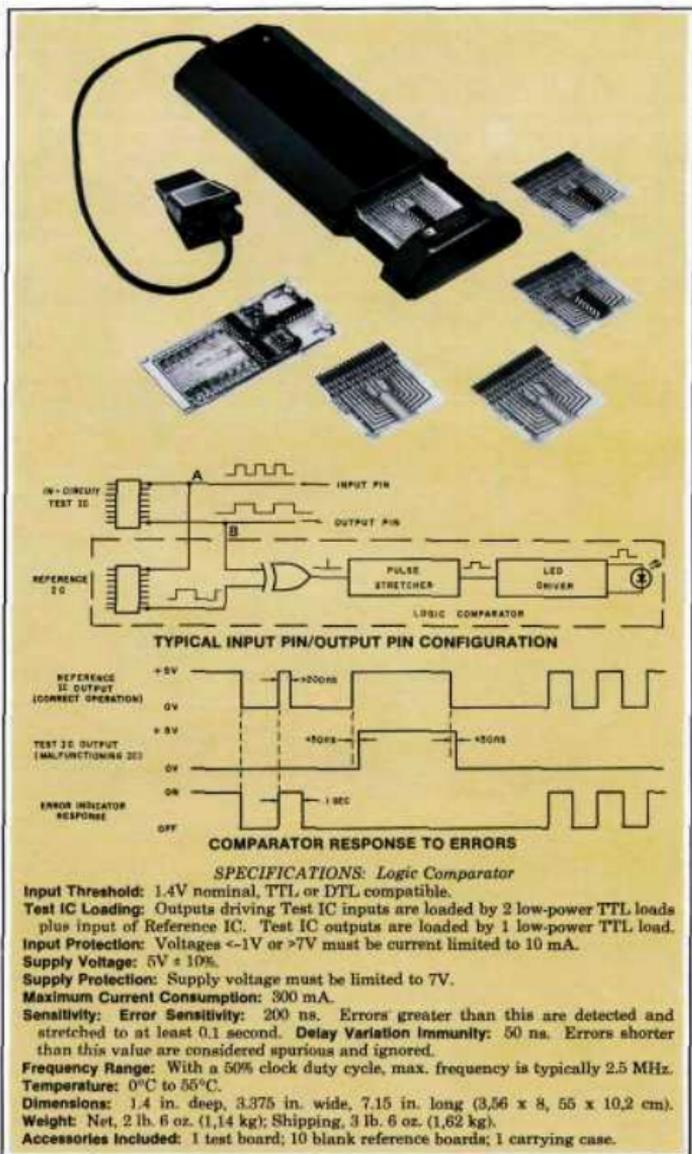


Figure A4. 10529A Logic Comparator. The Logic Comparator uses the test circuits signals to stimulate a reference IC which is mounted on a reference card. The resulting output signals are compared and any differences longer than 200 ns are displayed on the corresponding LED in the Logic Comparator.

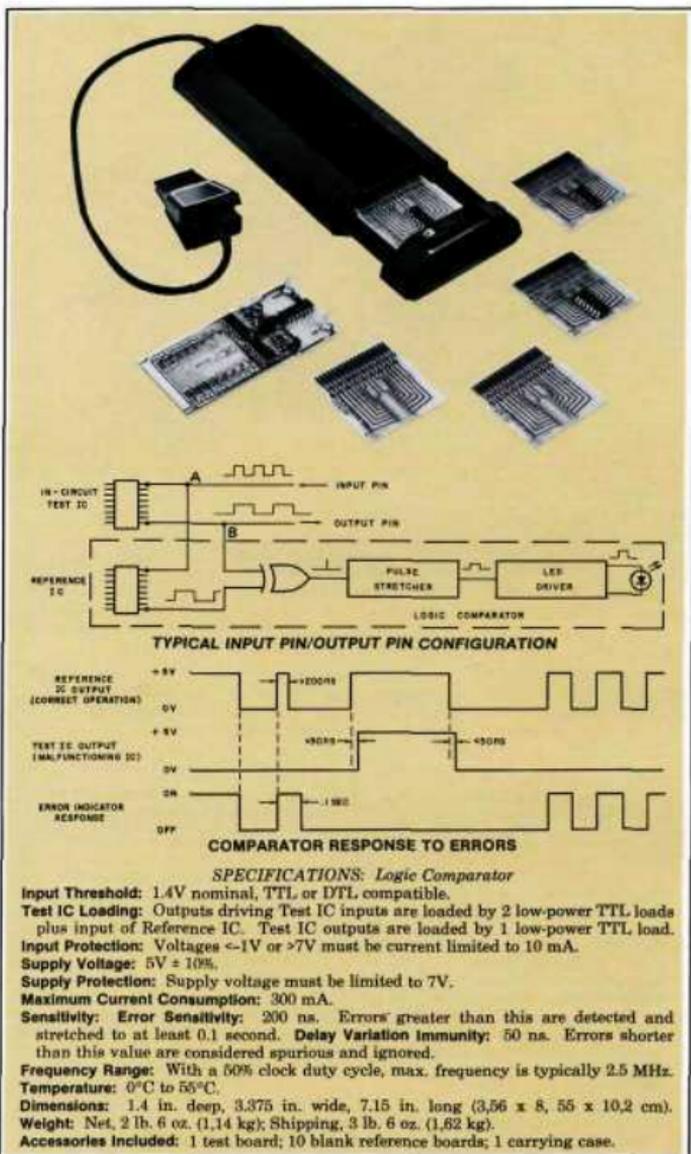


Figure A4. 10529A Logic Comparator. The Logic Comparator uses the test circuits signals to stimulate a reference IC which is mounted on a reference card. The resulting output signals are compared and any differences longer than 200 ns are displayed on the corresponding LED in the Logic Comparator.

APPENDIX II. WHAT WILL THE 10529A LOGIC COMPARATOR TEST?

Before discussing what the COMPARATOR will test, it is important to understand how it works. Through a reference board, the inputs of a reference IC are connected to the inputs of the test IC (Point A in Figure A4), thus the reference IC is exercised by the same signals that stimulate the test IC. The outputs of the reference and test IC are compared (Point B in Figure A4) and any differences greater than 200 nsec in duration signal a failure. Also the reference IC and the COMPARATOR are powered by the circuit under test through the reference board. Thus, the LOGIC COMPARATOR observes simultaneously all outputs of the test IC and determines the validity of these signals based both upon proper voltage levels and proper truth table response to the input signals.

An important consideration in using the LOGIC COMPARATOR is circuit loading. The loading considerations can be divided into two parts. The first is the type of load the COMPARATOR presents to the outputs of the IC to which the COMPARATOR is attached and the second is the load presented to the inputs. These loads are summarized in Table A1.

Table A1. Comparator Loading Chart

IC UNDER TEST TYPE	ADDITIONAL LOAD TO THE IC UNDER TEST'S INPUTS AND OUTPUTS DUE TO COMPARATOR AND REFERENCE IC	
	INPUTS	OUTPUTS
DTL	1.2 DTL loads	.1 DTL load
7400 Series TTL	1.2 7400 Series loads	.1 7400 Series load
Low Power TTL (74L00 Series)	5 low power loads	1 low power load
High Speed/Schottky TTL (74H00 or 74S00 Series)	1.5 7400 Series loads or 1.2 high speed/ Schottky loads	.1 7400 Series load or .1 high speed/ Schottky loads
NOTE: 1 low power load = .1 7400 Series load.		

The LOGIC COMPARATOR presents a different load to inputs than outputs. Table A1 describes in terms of fan out loads the affect of the COMPARATOR on both inputs and outputs.

Under most conditions, this additional loading will not affect the circuit operation. One major exception is when analog components, such as R's, C's, or transistors are used to control circuit timing or to buffer signals (see Figure A6). Since the COMPARATOR loads these circuits as described above, the timing or drive capability of the circuit may be affected. This loading should be considered when testing these circuits.

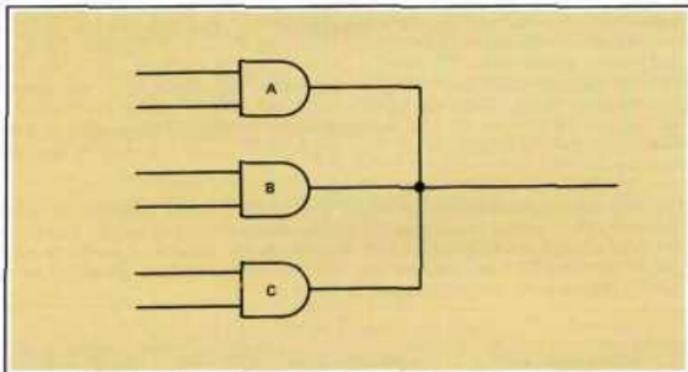


Figure A5. The "Open Collector" Problem. When gates are connected in the "wired-OR" arrangement, the output of one IC can constrain the outputs of the other IC's to be in a state other than that defined by the gates truth table and input states.

One problem faced by all troubleshooting instrumentation is what is fondly called the "open-collector evil." In the family of TTL IC's there is a sub-family called "open-collector" gates. These are circuits whose outputs can be tied together (sometimes called "wire-ORed" or "wire-AND") such that one circuit's output can constrain the other circuits' outputs to be in a given state regardless of their inputs. For example, gates A, B, and C are "wire-ORed" together. Under certain conditions gate A's output can cause gates B's and C's outputs to be a TTL low regardless of their input state. Thus from a truth table point of view the gates B and C are constrained to operate improperly.

This then is the "open-collector evil." Because the COMPARATOR tests for output states according to the truth table of the test IC, a fault will be indicated when the output is constrained as described above. Using conventional instrumentation such as voltmeters and oscilloscopes does not solve this problem either. When a problem is thought to be caused by "open collector" gates, the usual solution is to replace the gates one at a time until the problem is solved or to unsolder the outputs and to test the IC's individually. The COMPARATOR can be used if this last technique is followed.

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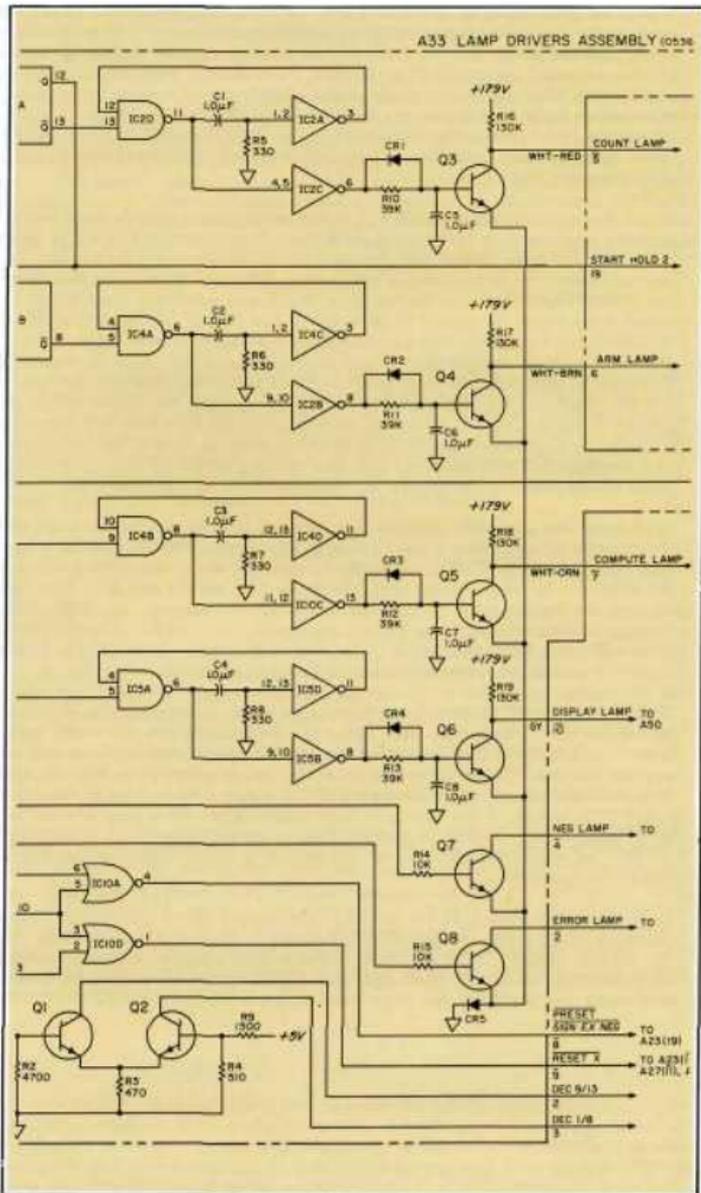


Figure A6. Analog components used to control circuit timing or to buffer signals may be loaded by the Logic Comparator. Care should be taken in testing these circuits.

The class of integrated circuits known as sequential integrated circuits presents today's troubleshooters with many difficult problems. IC's such as memories, shift registers, and flip-flops whose present outputs depend on previous inputs are called sequential IC's. Testing these devices with conventional tools requires the observation and study of the relationship of several waveforms. In some cases these *waveforms are long and complex and verification of proper IC operation is practically impossible.* The 10529A LOGIC COMPARATOR, when used properly, provides a very efficient and simple solution to troubleshooting these IC's.

Since the operation of a flip-flop or other sequential device depends upon the previous input to that device, and since the reference device will not in general have had the same "prior" set of inputs as the device being tested, it is necessary to "reset" the devices before comparing. This can be done by first clipping the COMPARATOR to the device to be tested and causing a reset signal to be supplied by either the circuit to be tested or the 10526T LOGIC PULSER. The PULSER can be used to inject a reset pulse into the IC's reset input. This then ensures that both devices start in the same state and will react the same to the sequence of input signals they receive. The COMPARATOR will now flip and not flop when the flip-flop flips. If the test IC is good, the output states of the reference and test IC will always agree and the COMPARATOR will not indicate a fault. In some cases the reset lines are connected directly to Vcc or ground and are thus not pulseable. In this case turning power off and back on sometimes brings both the test IC and the reference IC up to the same state.

With memories and shift registers, the problem is quite similar as stated above. But instead of supplying a reset pulse to the circuit to bring them to a known state, the COMPARATOR must merely be attached to the test IC long enough for the reference IC to be loaded with the same data as the test IC. This should require no longer than 1 complete cycle of the memory or shift register. During the time the reference IC is being loaded with the data, the COMPARATOR will give fault indications. If after a few cycle times the fault is still indicated, a fault has indeed occurred at the node indicated.

The 10529A LOGIC COMPARATOR provides rapid, incircuit testing of TTL integrated circuits. While the vast majority of these devices are easily testable with the COMPARATOR, some devices require special consideration and some are not testable. Table A2 is meant to be a quick reference to help the digital troubleshooter decide upon the testability of a given component in the 54/7400 series TTL family. (The 5400 and 7400 numbers are often used to refer to the set of devices with a 54 or 74 prefix.) This is not meant to be an exhaustive list of TTL or even 54/7400 devices, but rather a quick reference for the most widely used devices.

As a general summary of the LOGIC COMPARATOR's capabilities, Table A3 describes applicability of the COMPARATOR to general digital devices. While the 10529A LOGIC COMPARATOR is not a total solution, as indeed no single instrument is, it is the most powerful digital troubleshooting tool available in a world that is rapidly changing from analog to digital electronics.

Table A2. 54/7400 Testability Chart*

54/7400 TESTABILITY CHART*

T = TESTABLE; OT = OFTEN TESTABLE; NT = NOT TESTABLE

	T	OT	NT	NOTE		T	OT	NT	NOTE		T	OT	NT	NOTE		T	OT	NT	NOTE
7400	X				7445			X	2	7487	X				74151	X			
7401		X		1	7446			X	2	7488	X			5	74152	X			
7402	X				7447			X	2	7489	X			6	74153	X			
7403		X		1	7448					7490	X			8	74154	X			
7404	X				7449	X				7492	X			8	74155	X			
7405		X		1	7450			X	2	7493	X			8	74156		X		1
7406		X		1	7451	X				7494	X			6	74160	X			8
7407		X		1	7452			X	2	7495	X			6	74161	X			8
7408	X				7453			X	2	7496	X			6	74162	X			8
7409	X				7454	X				7497	X			8	74163	X			8
7410	X				7455			X	2	7498	X			6	74164	X			6
7411	X				7460			X	2	7499	X			6	74165	X			6
7412		X		1	7461			X	2	74100	X			4	74166	X			6
7413	X				7462			X	2	74101	X			3	74167	X			
7415		X		1	7464	X				74102	X			3	74170		X		1
7416		X		1	7465		X		1	74103	X			3	74180	X			
7417		X		1	7470	X			3	74104	X			3	74181	X			
7420	X				7471	X			3	74105	X			3	74182	X			
7421	X				7472	X			3	74106	X			3	74183	X			
7422		X		1	7473	X			3	74107	X			3	74184	X			
7423			X	2	7474	X			4	74108	X			3	74185	X			
7425	X				7475	X			4	74110	X			3	74190				8
7426			X	2	7476	X			3	74111	X			3	74191	X			8
7427	X				7477	X			4	74112	X			3	74192	X			8
7430	X				7478	X			3	74113	X			3	74193	X			8
7432	X				7480	X				74114	X			3	74194	X			6
7437	X				7481	X				74121		X		7	74195	X			6
7438		X		1	7482	X				74122		X		7	74196	X			8
7440	X				7483	X				74123		X		7	74197	X			8
7442	X				7484	X				74141			X	2	74198	X			8
7443	X				7485	X				74145			X	2	74199	X			6
7444	X				7486	X				74150	X								

1. Open collector device. Testable when not "wire-or'ed" (i.e., several outputs wired together).
2. Device with noncompatible input or output signals (i.e., expander or expandable gates, Nixie drivers).
3. JK flip-flop—if J = K = high or low, then reference IC and IC under test may be out of phase. Pulse set or clear or randomly pulse J or K.
4. D type or latch flip-flop—presents no trouble.
5. ROM—no trouble.
6. RAM, shift register—comparator must be attached long enough for reference IC and IC under test to be loaded with same data.
7. Monostable—circuit timing may be affected.
8. Counters—the reference IC and the IC under test often need to be synchronized. Pulse set or clear input.

* This is not meant to be an exhaustive list of TTL or even 54/7400 devices, but rather a quick reference for the most widely used devices.

Table A3. Comparator Capabilities Chart

(16 or Less Pin Dual-in-Line DTL, TTL)

Combinatorial Logic (AND, NAND, XOR, etc.	Excellent. This also includes expandable IC's. This category includes the vast majority of IC's in use.
Sequential Logic (Flip-Flops)	Excellent. Reference and test IC must be synchronized by a pulse on the "Reset" input.
Memories, Shift Registers	Excellent. Chip must be attached long enough for reference and test IC to contain the same information.
Low Power TTL	Good. The Comparator is an in load of 5 for the driving device.
One-shots	Usually good. Since reference and test IC share the RC timing components, circuit timing will be affected.
Open collector and Tri-state Logic	Usually poor. When outputs are bussed together a good gate is constrained to operate improperly and this will be indicated by the Comparator.
Expanders, Analog and Linear IC's	No. Their outputs are analog and cannot be tested by the Comparator.
MOS Devices	No. They require different power supplies exceeding the 7V input limit and will damage the Comparator.



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